

## Applying clock uncertainty for cascaded PLL and non-dedicated clock path for Arria 10<sup>®</sup> device family

If you are connecting PLL reference clock from a PLL output or a non-dedicated clock pin in your Arria<sup>®</sup> 10 design. This jitter can be compensated by adding 100ps clock uncertainty constraint at the **output clocks of the downstream PLL** in the design.

### Case#1: Cascaded input from IOPLL or XCVR PLL (FPLL/ATXPLL/CDRPLL)



Table1: Supported and unsupported PLL cascading configuration

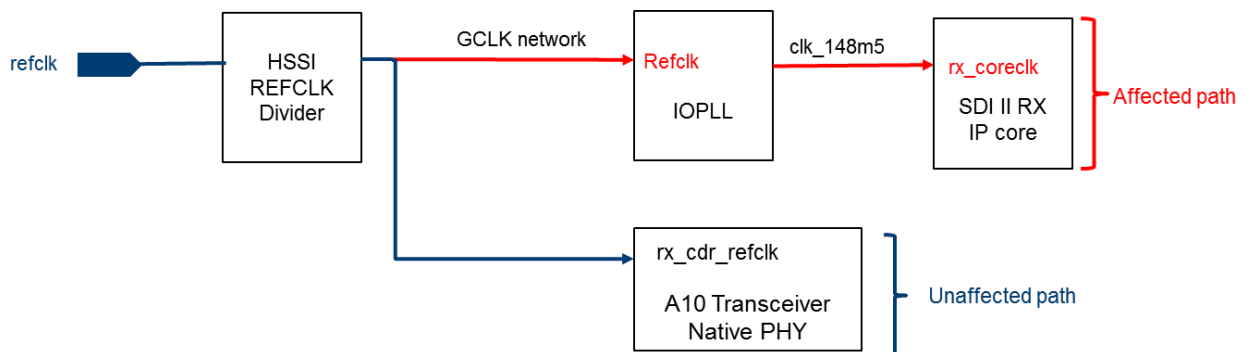
		Upstream PLL				
		FPLL	ATX	CDR	CMU	IOPLL
Downstream PLL	FPLL					
	ATX					
	CDR					
	CMU					
	IOPLL					

■ Affected cases  
■ Unsupported PLL cascading

### Case#2: Core Reference Clock



- Example: Reference clock from XCVR is routed on GCLK network and fed to reference clock of downstream IOPLL

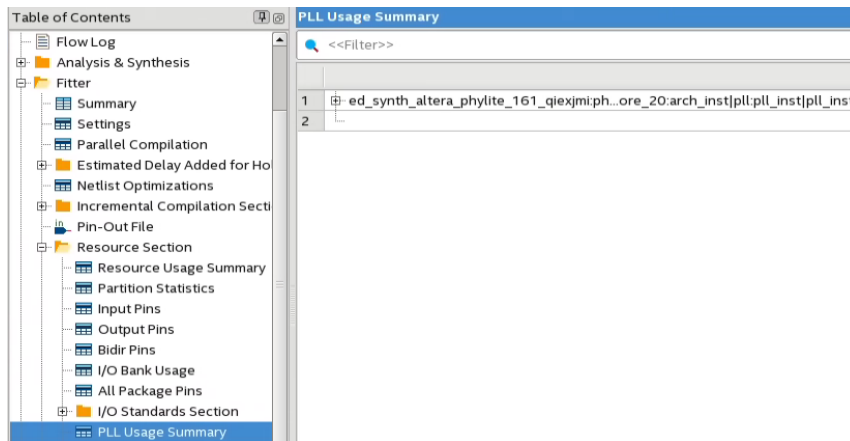


Data Arrival Path						
Incr	RF	Type	Fanout	Location	HS/LP	Element
0.000						launch edge time
5.499						clock path
0.000						source latency
0.000			1	PIN_AN37		inclk
0.000	RR	IC	1	IOIBUF_X0_Y9_N108		inclk~input i
0.070	RR	CELL	1	IOIBUF_X0_Y9_N108		inclk~input o
0.000	RR	IC	1	HSSIREFCLKDIVIDER_1CB		inclk~inputFITTER_INSERTED refclk_inp
0.000	RR	CELL	1	HSSIREFCLKDIVIDER_1CB		inclk~inputFITTER_INSERTED refclk_a
0.903	RR	CELL	1	HSSIREFCLKDIVIDER_1CB		inclk~inputFITTER_INSERTED~hssi_tile/~ma_fpll_fbclkout_lc_lvpecl_to_coreclk
0.000	RR	IC	2	CLKCTRL_1C_G_I15		inclk~inputFITTER_INSERTEDCLKENA0 inclk
0.278	RR	CELL	1	CLKCTRL_1C_G_I15		inclk~inputFITTER_INSERTEDCLKENA0 outclk
2.353	RR	IC	1	IOPLL_2L	High Speed	inst iopl1_0 altera_iopl1_ twentynm_pll iopl1_inst refclk[0]
0.605	RR	CELL	1	IOPLL_2L		inst iopl1_0 altera_iopl1_ twentynm_pll iopl1_inst~vco_refclk
0.001	RR	CELL	1	IOPLL_2L		inst iopl1_0 altera_iopl1_ twentynm_pll iopl1_inst~vctrl

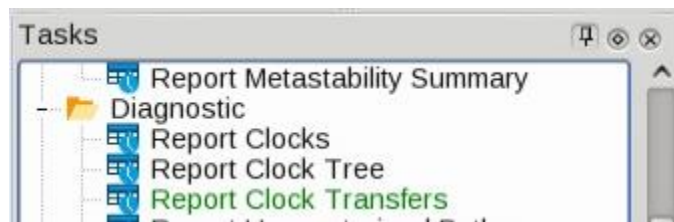
The HSSI refclk goes through HSSI refclk divider and core clock network via CLKCTRL

Following are the steps to apply the clock uncertainty to the design:

1. Identify all the PLLs in the design. Go to Fitter → Resource Section → PLL Usage Summary



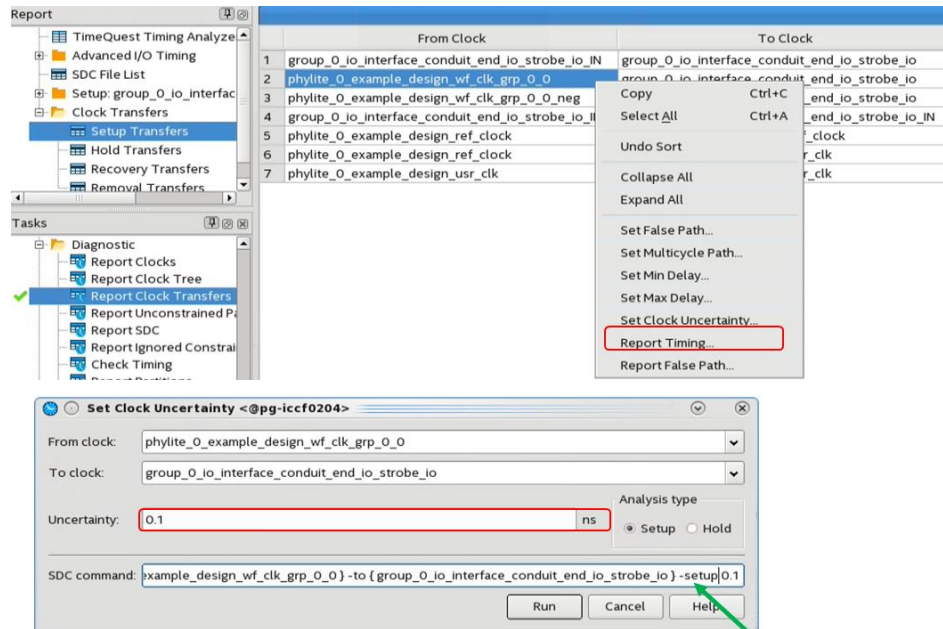
2. Report clock transfers in TimeQuest



3. Find out clock transfer/s that has/have output of the downstream PLL: From/To/Both

	From Clock	To Clock	RR Paths	FR Paths	RF Paths	FF Paths
1	group_0_io_interface_conduit_end_io_strobe_io_IN	group_0_io_interface_conduit_end_io_strobe_io	false path	0	false path	0
2	phylite_0_example_design_wf_clk_grp_0_0	group_0_io_interface_conduit_end_io_strobe_io	4	false path	false path	false path
3	phylite_0_example_design_wf_clk_grp_0_0_neg	group_0_io_interface_conduit_end_io_strobe_io	false path	false path	4	false path
4	group_0_io_interface_conduit_end_io_strobe_io_IN	group_0_io_interface_conduit_end_io_strobe_io_IN	2	0	2	0
5	phylite_0_example_design_ref_clock	phylite_0_example_design_ref_clock	239	0	0	0
6	phylite_0_example_design_ref_clock	phylite_0_example_design_usr_clk	1	0	0	0
7	phylite_0_example_design_usr_clk	phylite_0_example_design_usr_clk	33	0	0	0

4. Create the set\_clock\_uncertainty using the macro to add extra 100ps clock uncertainty



Remove “-setup” and put “-add”, please refer to next step for details

5. Add the constraint into the sdc file based on the following conditions:

- if the existing clock uncertainty only comes from derive\_clock\_uncertainty  
**set\_clock\_uncertainty -add -to <clock x> -from <clock y> 0.1**
- if the existing clock uncertainty comes from derive\_clock\_uncertainty + additional “set\_clock\_uncertainty -add”  
**set\_clock\_uncertainty -add -to <clock x> -from <clock y> [expr <existing\_value> +0.1]**
- if derive\_clock\_uncertainty is overridden by “set\_clock\_uncertainty” (no -add)  
**set\_clock\_uncertainty -to <clock x> -from <clock y> [expr <existing\_value> +0.1]**

Note:

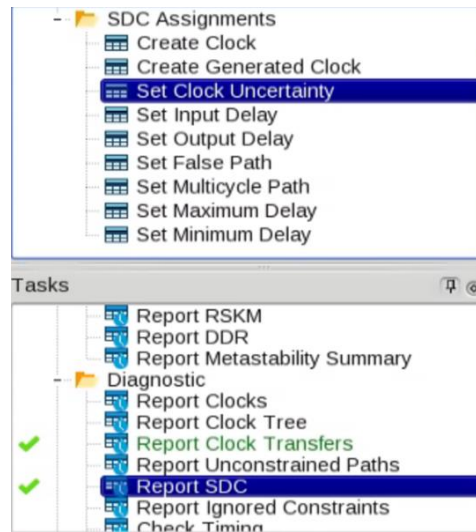
“set\_clock\_uncertainty -add”

- The clock uncertainty value will be added to the value from “derive\_clock\_uncertainty”
- If multiple “-add” constraint present, only the value from the last constraint will be added

“set\_clock\_uncertainty” (no -add)

- overrides any previous clock uncertainty value including “derive\_clock\_uncertainty”

6. Report SDC and check in the SDC Assignments>Set Clock Uncertainty report, make sure the extra 100ps is added into the affected clock transfer paths



7. Retime or recompile the design and ensure timing closure
8. Perform rigorous hardware testing to ensure design is working properly before going into production