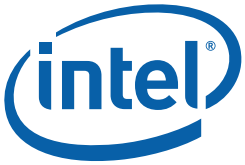

Intel® 965 Express Chipset Family Memory Technology and Configuration Guide

White Paper

- For the Intel® 82Q965, 82Q963, 82G965 Graphics and Memory Controller Hub (GMCH) and Intel® 82P965 Memory Controller Hub (MCH)

July 2006

Document Number: 313207-002

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Revision History

Revision Number	Description	Revision Date
-001	• Initial release	June 2006
-002	• Added support for 82Q965, 82G965, and 82Q963 GMCH components.	July 2006

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1 Introduction

This document details the Intel® 965 Express chipset family (G)MCH's technology enhancements, supported memory configurations, and memory organizations. It is intended for a technical audience interested in learning about the performance enhancements and simplified population rules offered by Intel® Fast Memory Access and Intel® Flex Memory Technology in the platforms based on the Intel 965 Express chipset family.

Note: Unless otherwise specified, the information in this document applies to the Intel® 82Q965/82Q963/82G965 Graphics and Memory Controller Hubs (GMCH) and the Intel® 82P965 Memory Controller Hub (MCH).

Note: The term (G)MCH refers to the 82Q965/82Q963/82G965 GMCH and 82P965 MCH.

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2 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

This chapter details the (G)MCH's technology enhancements of its DDR2 DRAM controller know as Intel® Fast Memory Access (Intel® FMA).

With the growing reliance on faster and less latent memory technologies to feed today's high performance platforms, it has become necessary to not only increase system memory clock speeds, but to also streamline usage of the DDR2 protocol in novel and intelligent ways to decrease latency and optimize memory bandwidth. To do this, several Intel technologies, known collectively as Intel FMA, have been added to this generation of Intel's Express chipsets.

The following sections outline and explain the technology enhancements: Just In Time Scheduling, Command Overlap, Out of Order Scheduling, and Opportunistic Writes. See **Error! Reference source not found.** for a visual example showing Intel FMA compared to previous generations chipsets.

2.1 Just in Time Command Scheduling

In previous generations of Intel chipsets, all memory access requests had to go individually through an arbitration mechanism forcing requests to be executed one at a time. If by chance the request in the queue could be started without interfering with the current request, then Command Overlap would allow for concurrent issuing of the requests. Now, in the 965 Express chipset family, the arbitration mechanism has been replaced with an advanced scheduler and all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just In Time to make optimal use of Command Overlapping. This allows optimizing of bandwidth while retaining DDR2 protocol, and reducing latency.

2.2 Command Overlap

Command Overlap allows for the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. This allows for situations where multiple commands can be issued in an overlapping manner, increasing the efficiency of DDR2 protocol.

Although Command Overlap was introduced in previous generations of Intel chipsets, it is leveraged in the 965 Express chipset family to enable other latency reducing and performance enhancing technologies.

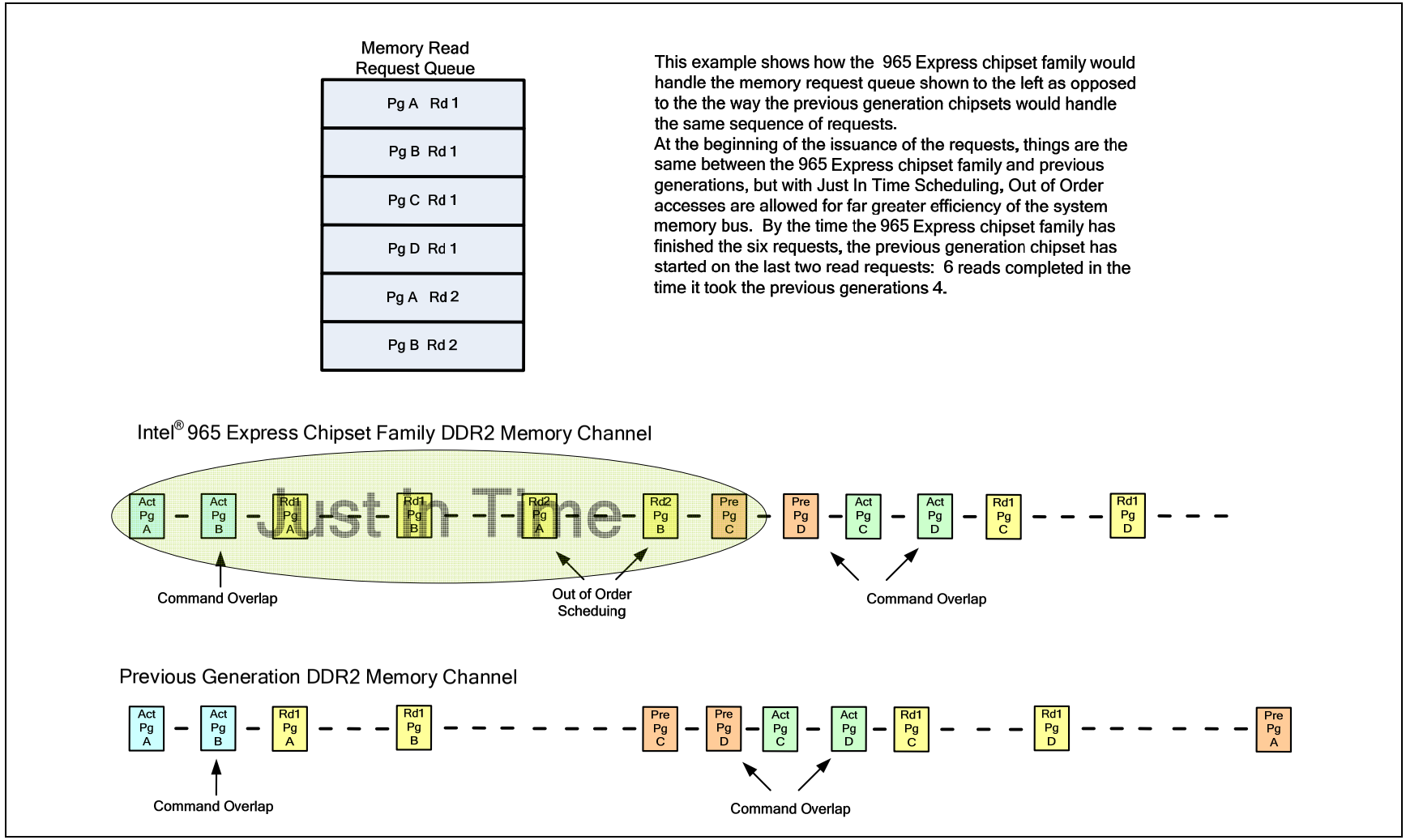
2.3 Out of Order Scheduling

Leveraging Just In Time Scheduling and Command Overlap, the 965 Express chipset family continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the Intel 965 Express chipset family to further reduce latency and increase bandwidth efficiency. This is especially important for helping overcome the in-order manner of the Front Side Bus between the (G)MCH and the processor to minimize processor starvation.

2.4 Opportunistic Writes

Processor requests for memory reads usually are weighted more heavily than writes to memory to avoid cases of starving the processor of data to process while the writes are issued to system memory. In previous generations of Intel chipsets, writes were issued to a pending queue to be flushed to memory when certain watermarks were reached. During this write flush, if the processor needed data in system memory, it would have to wait for the write flush to finish, starving the processor of data to process. To avoid this, the Intel 965 Express chipset family monitors system memory requests and issues pending write requests to memory at times when they will not impact memory read requests, allowing for an almost continuous flow of data to the processor for processing.

Figure 1. Intel 965 Express chipset family Memory Performance vs. Previous Generation Chipsets



3 Supported Memory Technologies

3.1 Memory Technology Supported

The (G)MCH supports DDR2 non-ECC DIMMs and memory technologies in the following configurations:

- DDR2-533 (PC2-4200), DDR2-667 (PC2-5300), and DDR2-800 (PC2-6400)

Table 1. Memory Technology Support

DRAM Data Rate	DRAM Technology	Smallest Increments (One x16SS DIMM)	Largest Increments (One x8DS DIMM)	Maximum Capacity (Four x8DS DIMMs)
533 MT/s	256 Mb	128 MB	512 MB	2048 MB
533 MT/s	512 Mb	256 MB	1024 MB	4096 MB
533 MT/s	1 Gb	512 MB	2000 MB	8000 MB
667 MT/s	256 Mb	128 MB	512 MB	2048 MB
667 MT/s	512 Mb	256 MB	1024 MB	4096 MB
667 MT/s	1 Gb	512 MB	2000 MB	8000 MB
800 MT/s	256 Mb	128 MB	512 MB	2048 MB
800 MT/s	512 Mb	256 MB	1024 MB	4096 MB

Note: The (G)MCH has a minimum total memory requirement of 256 MB.

3.2 DRAM Device Speed Bin Support

The (G)MCH supports the following DDR2 DRAM Device Speed Bin Timings on the main memory interface.

Table 2. DDR2 DRAM Device Speed Bin Timing Support

DRAM Data Rate	t_{CL}	t_{RCD}	t_{RP}	Units
533 MT/s	4	4	4	tCK
667 MT/s	5	5	5	tCK
800 MT/s	5	5	5	tCK
800 MT/s	6	6	6	tCK

3.3 ECC Support

The Intel 965 Express chipset family does **NOT** support ECC.

3.4 DDR2 SDRAM Un-buffered DIMM Support

The (G)MCH supports the following DDR2 240-Pin Un-buffered DIMMs on the main memory interface.

Table 3. Un-buffered DDR2 DIMM Support

DRAM Data Rate	DIMM Type	Number of Physical Ranks	ECC/Non-ECC	Number of DRAM Devices	Raw Card Version
533 MT/s	X8SS	1	Non-ECC	8	A
533 MT/s	X8DS	2	Non-ECC	16	B
533 MT/s	X16SS	1	Non-ECC	4	C
667 MT/s	X8SS	1	Non-ECC	8	D
667 MT/s	X8DS	2	Non-ECC	16	E
667 MT/s	X16SS	1	Non-ECC	4	C
800 MT/s	X8SS	1	Non-ECC	8	D
800 MT/s	X8DS	2	Non-ECC	16	E
800 MT/s	X16SS	1	Non-ECC	4	C

3.5 Valid Front Side Bus and Memory Speeds

The (G)MCH supports the following Front Side Bus (FSB) and system memory speed configurations.

Table 4. Valid FSB/Memory Speed Configurations

FSB	DRAM Data Rate	DRAM Type	Single Channel Peak Bandwidth	Dual Channel Peak Bandwidth
1066 MHz	533 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s
1066 MHz	667 MT/s	DDR2 - DRAM	5.32 GB/s	10.6 GB/s
1066 MHz	800 MT/s	DDR2 - DRAM	6.4 GB/s	12.8 GB/s
800 MHz	533 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s
800 MHz	667 MT/s	DDR2 - DRAM	5.32 GB/s	10.6 GB/s
800 MHz	800 MT/s	DDR2 - DRAM	6.4 GB/s	12.8 GB/s
533 MHz	533 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s
533 MHz	667 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s
533 MHz	800 MT/s	DDR2 - DRAM	4.25 GB/s	8.5 GB/s

Note: The (G)MCH does not support system memory frequencies that exceed the frequency of the Front Side Bus. If memory with higher frequency capabilities than that of the FSB is populated, the memory will be under-clocked to align with the FSB.

3.6 Invalid Configurations

The following configurations are not valid with the Intel 965 Express chipset family:

- 64-Mb, 128-Mb, 2-Gb, and 4-Gb Memory Technologies for DDR2
- x4, x32 DIMMs
- DDR2-533 with any Speed Bin Timing combination other then 4-4-4
- DDR2-667 with any Speed Bin Timing combination other then 5-5-5
- DDR2-800 with any Speed Bin Timing combination other then 5-5-5 or 6-6-6
- Double-Sided x16 DIMMs
- Registered DIMMs
- DDR DIMMs
- Any DIMM with ECC technology

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4 Memory Organization and Operating Modes

The (G)MCH memory interface is designed with Intel® Flex Memory Technology so that it can be configured to support single-channel or dual-channel DDR2 memory configurations.

Depending upon how the DIMMs are populated in each memory channel, a number of different configurations can exist for DDR2:

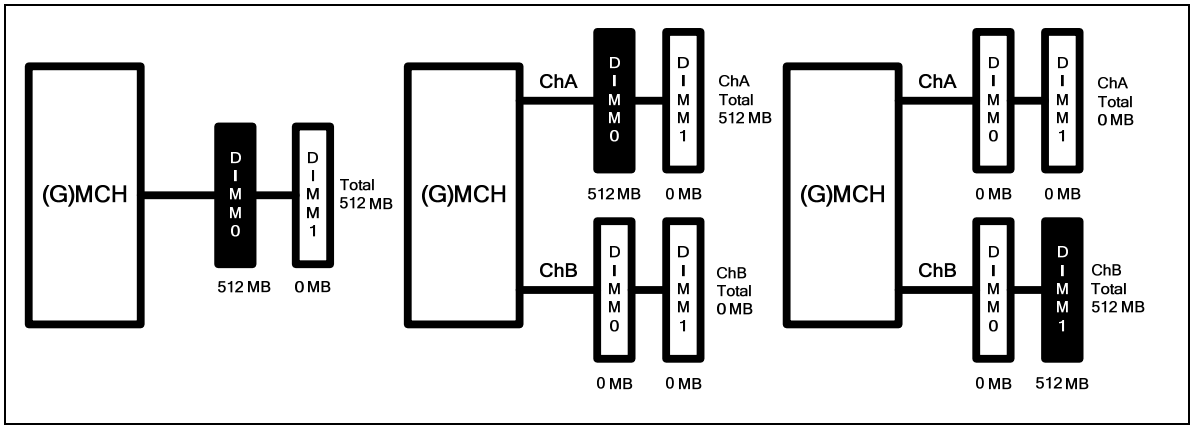
- Single Channel – only one channel of memory is routed and populated, or if two-channels of memory are routed, but only one channel is populated; can be either channel A or channel B.
- Dual Channel Asymmetric – both channels are populated, but each channel has a different amount (MB) of total memory.
- Dual Channel Symmetric – both channels are populated where each channel has the same amount (MB) of total memory.

The following sections explain and show the different memory configurations that are supported by the Intel 965 Express chipset family.

4.1 Single-Channel

The system will enter single-channel mode when only one channel of memory is routed on the motherboard, or if two-channels of memory are routed, but only one channel is populated. In this configuration, all memory cycles are directed to a single channel.

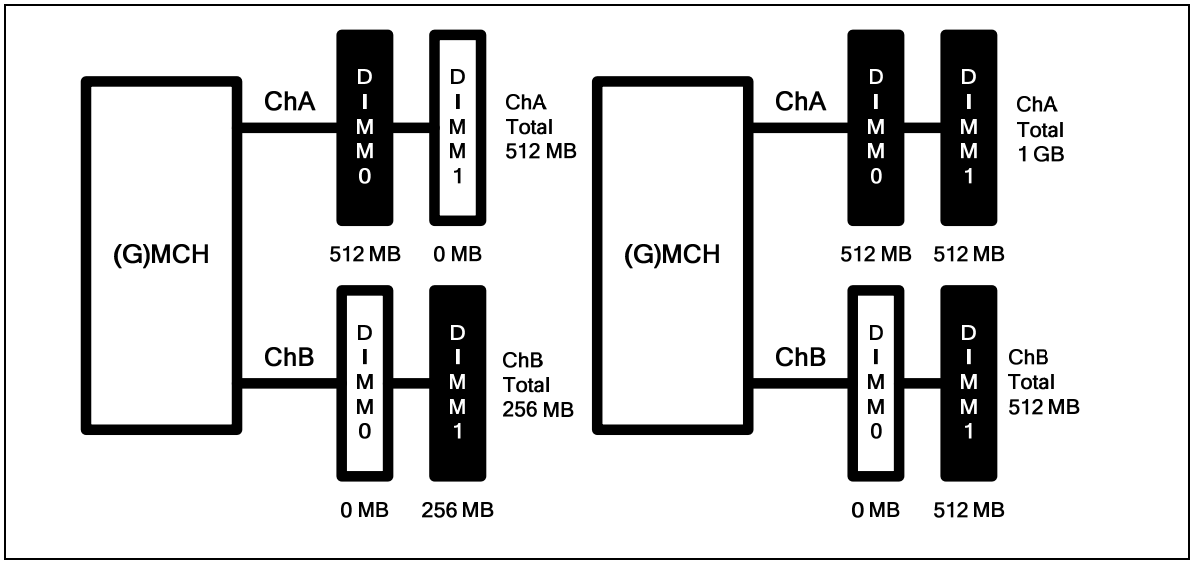
Figure 2. Single-Channel Memory Mode Example



4.2 Dual-Channel Asymmetric

This mode is entered when both memory channels are routed and populated with different amounts (MB) of total memory. With the aid of Intel Flex Memory Technology this configuration allows addresses to be bounced between channels in interleaved mode until the top of the smaller channel's memory is reached, allowing for full dual channel performance in that range. Access to higher addresses will all be to the channel with the larger amount of memory populated; thus giving single channel performance through those addresses.

Figure 3. Dual-Channel Asymmetric Memory Mode Example



4.3 Dual-Channel Symmetric

This mode allows the end user to achieve maximum performance on real applications by using the full 64-bit dual-channel memory interface in parallel across the channels. The end user is only required to populate both channels with the same amount (MB) of total memory to achieve this mode. The DRAM component technology, device width, device ranks, and page size may vary from one channel to another.

Addresses are bounced between the channels, and the switch happens after each cache line (64-byte boundary). If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels.

Figure 4. Dual-Channel Symmetric Memory Mode Example

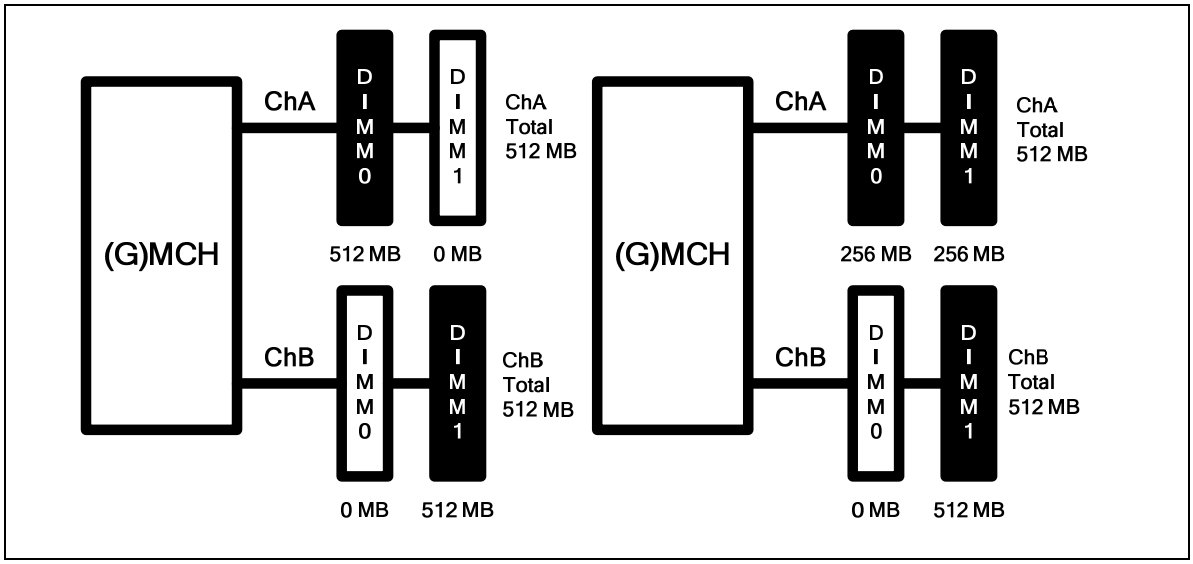
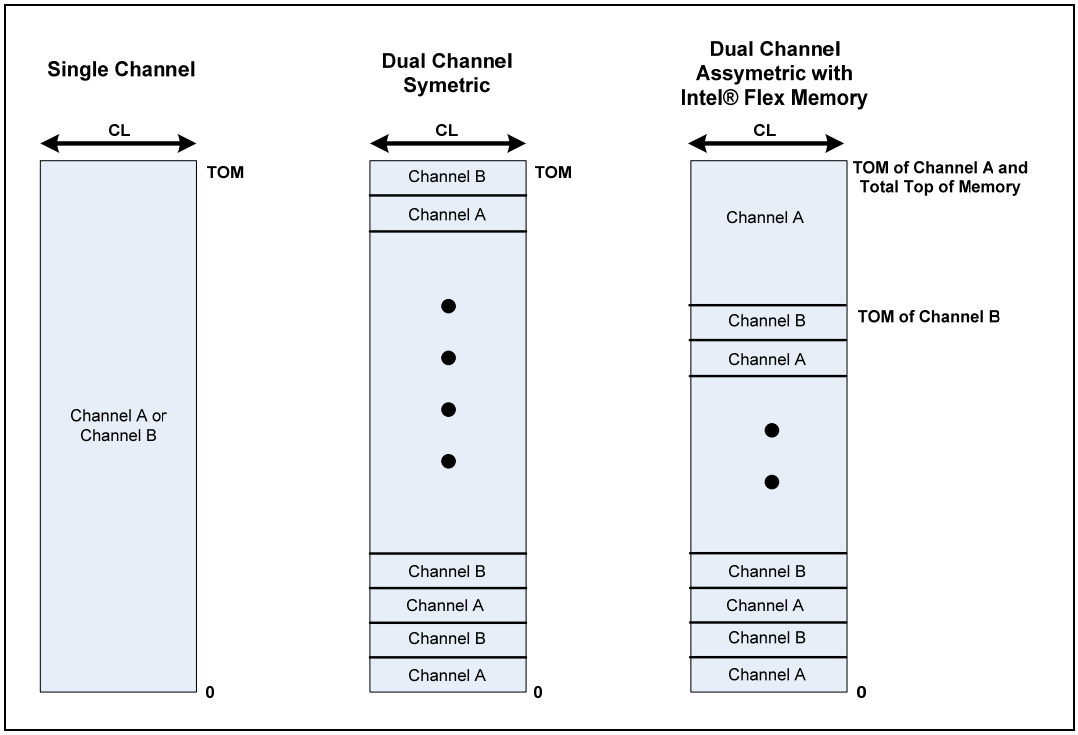


Figure 5. System Memory Mode Styles



4.4 Mixed DRAM Memory Speeds

The (G)MCH will accept mixed DDR2 speed populations, assuming the SPDs on the DIMMs are programmed with the correct information and the BIOS is programmed as outlined in Intel's BIOS reference code.

In all operating modes (Single-Channel, Dual Channel Asymmetric, and Dual-Channel Symmetric) the frequency of the System Memory will be set to the lowest frequency with its supported speed bin timings of all DIMMs populated in the system, as determined through the SPD registers on the DIMMs.

For example, a DDR2-667 DIMM with supported 5-5-5 speed bin timings installed with a DDR2-533 DIMM with supported 4-4-4 speed bin timings should run at 533 MHz with supported 4-4-4 speed bin timings. The DDR2-667 DIMM should downshift to DDR2-533 timings, thus allowing the system to run at 533 MHz with supported 4-4-4 speed bin timings. The DDR2-667 DIMM will only downshift to DDR2-533, if the timings for DDR2-533 are programmed in the DDR2-667 DIMMs SPD.

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