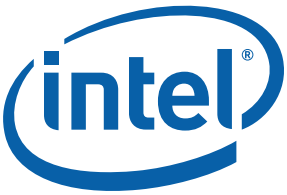

Intel® X48 Express Chipset Memory Controller Hub (MCH)

Specification Update

March 2008

Document Number: 319123-001

Contents

Revision History

Revision	Description	Date
-001	• Initial Release	March 2008

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Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents

Title	Number
Intel® X48 Express Chipset Memory Controller Hub (MCH) Datasheet	319122-001

Nomenclature

Errata are design defects or errors. These may cause the Intel X48 Express Chipset MCH's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the MCH product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations.

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata

Number	Steppings	Status	ERRATA
	A1		
1	X	No Fix	PCIe 1.1 cards in PCIe slots off the MCH lead to boot failures
2	X	No Fix	Intermittent IERR# hangs during cold boot does not detect PCIe cards
3	X	No Fix	IERR due to DMI/PCIe Link Not Trained

Specification Changes

No.	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

Specification Clarifications

No.	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

Documentation Changes

No.	DOCUMENTATION CHANGES
	There are no Documentation Changes in this Specification Update revision.

Identification Information

Component Identification via Programming Interface

The Intel® X48 Express Chipset MCH stepping can be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision ID[3]	Notes
A1	8086h	29E0	01h	

Notes:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00-01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02-03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.
4. The Intel® X48 Express Chipset MCH and Intel® X38 Express chipset MCH share the same Device ID. The CAPID0 (Capability Register, bit 89) is used to determine the differences between both chipsets. See the CAPID0 (Capability Register) in the datasheet for additional component identification details.

Component Marking Information

The Intel® X48 Express Chipset MCH stepping can be identified by the following component markings:

Stepping	S-Spec	Top Marking	Notes
A1	SLASF	NU82X48	MCH Production Sample

Errata

1. PCIe 1.1 Cards in PCIe Slots off the MCH Lead to Boot Failures

Problem: The Intel X48 Express Chipset sets the TS1 Ordered Set - Symbol 4 Bit[6] to 1b when a PCIe 1.1 card is plugged in. This is a reserved bit which is used in PCIe 2.0 to broadcast support for selectable de-emphasis. PCIe 1.1 Specification states that Bit[6] should be set to 0b. With some 2.5 GT/s PCIe 1.1 I/O cards of widths x8/x4/x1, system restarts and hangs were exhibited during PCIe link initialization when populated in MCH slots.

Implication: System unable to train some 2.5 GT/s PCIe 1.1 cards that don't comply with the PCIe 1.1 Specification. Failures have occurred across multiple vendors and different types of PCIe 1.1 cards.

Workaround: See latest Bearlake Chipset BIOS Specification (Revision 2.1 or later) for more information. Modification to the Link Stability/Recovery Algorithm will fix this issue when using non-compliant cards but customers should continue working with their card vendors for PCIe 1.1 Spec compliancy.

Status: For affected steppings, see the Summary Table of Changes.

2. Intermittent IERR# Hangs During Cold Boot Does Not Detect PCIe Cards

Problem: During cold boots, the MCH may hang during power-on and assert IERR or may not detect PCIe cards off the primary port or secondary port. The 1.8V on-die voltage regulator which powers the PCIe & DMI PLL may not be stable when powering on, causing above issues.

Implication: PLL not operating correctly could result in not detecting PCIe cards or DMI may not operate correctly, resulting in system hang and IERR# assertion.

Workaround: Motherboard designers are required to implement board changes:

- Require 1.25V through LC filter on MCH VCCAPLL_EXT (Ball A20) & VCCAPLL_EXT2 (Ball AR10).
- Require 1.25V on MCH VCC_EXP_PLL (Ball AB13).
- BIOS must disable 1.8V on-die VR. Contact your Intel field representative for the latest BIOS information.

Status: For affected steppings, see the Summary Table of Changes.

3. IERR due to DMI/PCIe Link Not Trained

Problem: The MCH has a rare meta-stability condition within the DMI/primary PCIe and secondary PCIe receiver PLL divider circuitry. The MCH DMI/primary PCIe receiver may not be locked at the correct internal clock phase during warm or cold reset - causing the DMI/primary PCIe link to not train. The MCH secondary PCIe receiver may not be locked - causing the secondary PCIe link to not train. Each lock independently. If the DMI/PCIe receiver divider locked the correct clock phase, the receiver divider stays locked - and the link stays trained - until the next warm or cold reset.

Implication:

- If the rare meta-stability condition occurs, the processor may assert IERR due to traffic across the DMI link not completing. If the ICH Watch Dog Timer is enabled, the timer will time out and reboot the system. On the subsequent reset, the DMI/primary PCIe receiver may lock at the correct phase - and normal operation continues.
- In the extremely rare event that meta-stability occurs on back-to-back resets, the system could hang due to the DMI link not being trained. The Watch Dog Timer has timed out once, and would not timeout again to reboot the system. Intel has not observed the occurence of back-to-back meta-stable conditions.
- If the rare meta-stability condition occurs when the system is in ACPI S3 state, data saved in memory may be lost.
- If the rare meta-stability condition occurs on the secondary PCIe receiver PLL divider circuity, a PCIe add-in card present in the slot would not be trained.

Workaround:

- BIOS enable ICH Watch Dog Tiimer.
- If a PCIe add-in card is present but not trained, the BIOS resets the secondary PCIe link to retrain the card. Contact your Intel field representative for the latest BIOS information.
- There is no workaround for S3. However, the occurence of this meta-stability condition during resume from S3 is rare.

Status: For affected steppings, see the Summary Table of Changes.

Specification Changes

There are no Specification Changes in this Specification Update revision.

Specification Clarifications

There are no Specification Clarifications in this Specification Update revision.

Documentation Changes

There are no Documentation Changes in this Specification Update revision.

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