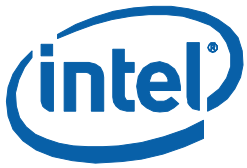

Mobile Intel® 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH

Specification Update

May 2012

Revision 009

Document Number: 316274-009

Contents

Revision History

Document Number	Revision	Description	Date
316274	-001	Initial release	May 2007
316274	-002	Changes made to disclaimer page	June 2007
316274	-003	• Updated Identification Information and component marking information for the Mobile Intel® GME965 Express Chipset. • Updated Identification Information and component marking information for the Mobile Intel® GLE960 Express Chipset. • Updated Identification Information and component marking information for the Mobile Intel® GL960 Express Chipset.	June 2007
316274	-004	• Added Errata 3 to the *Mobile Intel® 965 Express Family Graphics Memory Controller Hub Specification Update* Document # 316274 • Added Errata #4 *Visual Corruption with Integrated Graphics & Intel® Flex Memory Technology Enabled using Microsoft Windows Vista* operating system* • Added Errata #5 *Mobile Intel 965 Express Chipset Family MSI De-feature* (Device 2 only) • Added Errata #6 *Mobile Intel 965 Express Chipset Family Display Brightness* • Added Doc Change #1 *Remove Section 10.2 Thermal Characteristics form the Mobile Intel® 965 Express Family Datasheet* • Added Doc Change #2 *SDVOB_INT and SDVOC_INT Signal Naming Mobile Intel® 965 Express Family Datasheet* • Added Doc Change #3 *Host/Memory/Graphics Clock Frequency Support for 1.05-V Core Voltage the Mobile Intel GM965 and GL960 Express Chipsets Mobile Intel® 965 Express Family Datasheet* • Corrected Component Marking Information Device ID for GLE960 and GME965	September 2007
316274	-005	• Added Doc Change #4 *1Gb x 16 DDR2 device support added to System Memory Organization Support for DDR2* • Added Doc Change #5 *HSync to Vsync Voltage should be 3.3v* • Added Spec Clarification #1 *DMA Transfer Completion For Latency Sensitive Devices*	October 2007
316274	-006	• Added Doc Change #6 Add Section 5.3.1.1 Single Channel population rules for systems with Intel Management Engine enabled • Made correction to table 9 of Section 5.1 of Doc Change #4 *1 Gb x 16 DDR2 device support added to System Memory Organization Support for DDR2*	November 2007

Document Number	Revision	Description	Date
316274	-007	• Added Errata #7 Incorrect Low-Priority Interrupt Redirection by Mobile Intel® 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH on C5 Exit	December 2007
316274	-008	• Added Errata #8 Mobile Intel® 965 Express Chipset Family Unexpected DDR RCOMP Update	March 2008
316274	-009	• Updated parts information to include FLI Consolidation to 65 nm	May 2012

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Preface

This document is an update to the specification contained in the following Affected Documents table. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers or applications, operating systems, or tools.

Information types defined in the Nomenclature section are consolidated into the specification update and are no longer published in other documents.

Affected Documents

Document Title	Document Number/Location
Mobile Intel® 965 Express Chipset Family Datasheet	316274-007

Nomenclature

Errata are design defects or errors. Errata may cause the Mobile Intel® 965 Express Chipset family behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Summary Tables of Changes

The following table indicates the Errata, Specification Changes, Specification Clarifications or Documentation Changes, which apply to the listed MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

ERRATA			
Number	**Stepping**	**Status**	**TITLE**
	C0		
1	x	No Fix	(G)MCH PCI Express* Improper Error Logic Handling
2	x	No Fix	Mobile Intel® 965 Express Chipset Family Rare Visual Defect with Intel® S2DDT
3	X	No Fix	Mobile Intel® 965 Express Chipset Family PCI*Express Link Might Not Switch from x1 to x16
4	X	No Fix	Visual Corruption with Integrated Graphics and Intel® Flex Memory Technology Enabled using Microsoft Windows Vista* Operating System
5	X	No Fix	Mobile Intel® 965 Express Chipset Family MSI De-feature (Device 2 only)
6	X	No Fix	Mobile Intel® 965 Express Chipset Family Display Brightness
7	X	No Fix	Incorrect Low-Priority Interrupt Redirection by Mobile Intel® 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH on C5 Exit
8	x	No Fix	Mobile Intel® 965 Express Chipset Family Unexpected DDR RCOMP Update

Number	SPECIFICATION CHANGES
	There are no specification changes in this Specification Update revision.

Number	SPECIFICATION CLARIFICATIONS
1	DMA Transfer Completion For Latency Sensitive Devices

Number	DOCUMENTATION CHANGES
1	Removed Section 10.2 Thermal Characteristics
2	SDVOB_INT and SDVOB_INT Signal Naming
3	Host/Memory/Graphics Clock Frequency Support for 1.05-V Core Voltage the Mobile Intel GM965 and GL960 Express Chipsets
4	1 Gb x 16 DDR2 Device Support Added to System Memory Organization Support for DDR2
5	HSync to Vsync Voltage Should Be 3.3 V
6	Added Section 5.3.1.1 Single Channel Population Rules for Systems with Intel Management Engine Enabled

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Identification Information

Component Marking Information

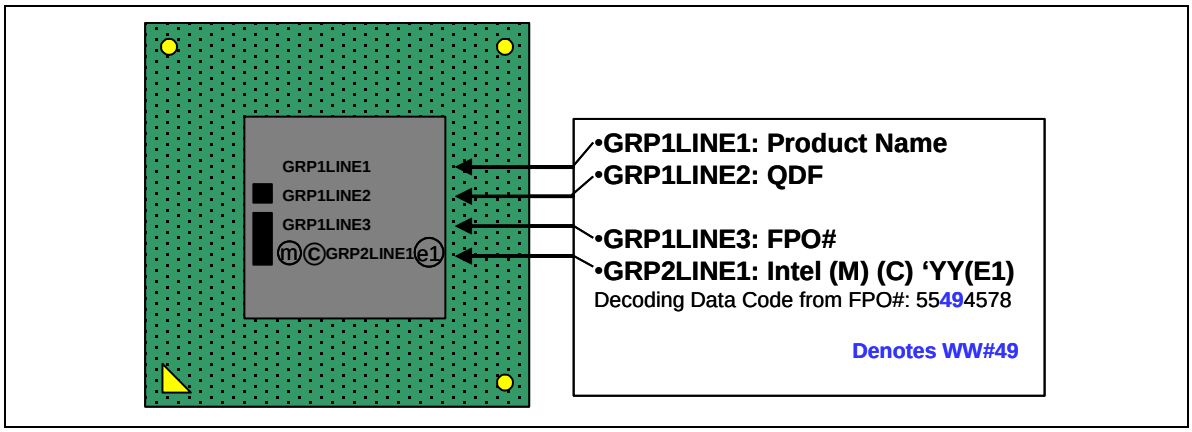
Component identification via marking Information and programmed registers is detailed below for the currently available steppings of the Mobile Intel 965 Express Chipset family silicon.

Product	QDF/S-Spec	Stepping	MM#	CRID[1]	SRID[1]	Device ID[2]	Description
GL960 (Lead Free)	SLA5V	C0	891184	0Ch	03h	2A00h	Production
GLE960 (Lead Free)	SLA9G	C0	891185	0Ch	03h	2A10h	Production
GLE960 (Lead Free)	SLJA5	C0	915749	0Ch	03h	2A10h	Production[3]
GM965 (Lead Free)	SLA5T	C0	891181	0Ch	03h	2A00h	Production
GM965 (Lead Free)	SLJA3	C0	915748	0Ch	03h	2A00h	Production[3]
GME965 (Lead Free)	SLA9F	C0	891183	0Ch	03h	2A10h	Production
GME965 (Lead Free)	SLJ9Z	C0	915746	0Ch	03h	2A10h	Production[3]
PM965 (Lead Free)	SLA5U	C0	891182	0Ch	03h	2A00h	Production

NOTES:

1. CRID/SRID can be determined by reading the register at B/D/F/Type – 0/0/0/PCI Offset 08h.
2. DID can be determined by reading the register at B/D/F/Type – 0/0/0/PCI Offset 02h.
3. Manufactured on 65 nm process.

Figure 1. Mobile Intel® 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH Lead-Free Package Markings



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Errata

1. (G)MCH PCI Express* Improper Error Logic Handling

Problem: The Mobile Intel 965 Express Chipset Family (G)MCH may not properly handle certain PCI Express* bit errors in the TLP header

- Specifically bit errors in the "Format of the packet", "Type of the packet", "Traffic class", or "Length for any associated data" type of fields.
- Bit errors in these fields may cause TLPs to become Malformed TLPs.
- Malformed TLP received along with (G)MCH buffer full condition may result in a system hang.

Implication: PCI Express devices, which generate the errors above may cause system hang.

- Customers should contact their third-party vendor to ensure the PCI Express devices do not generate bit errors.
- To date, Intel has not seen any PCI Express production devices that generate these errors. Issue has only been seen with known bad PCI Express engineering sample cards that generate a high volume of bit errors.

Workaround: None

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

2. Mobile Intel 965 Express Chipset Family Rare Visual Defect with Intel® S2DDT

Problem: With Intel® Smart 2D Display Technology (Intel® S2DDT) enabled, a handshake violation may occur on a single frame due to rare race conditions.

Implication: There is no functional impact. There may be a minor visual impact such as display distortion on a single frame out of hundreds of thousands displayed, when running an application that will update the display with different objects.

- This issue has only been observed in a synthetic test environment.
- Intel recommends keeping Intel Smart 2D Display Technology enabled.

Workaround: None

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

3. Mobile Intel® 965 Express Chipset Family PCI express Link Might Not Switch from x1 to x16

Problem: The (G)MCH PCI Express Link does not train up (x1 to x16) after a train down (x16 to x1) in the "configuration" state.

Implication: Lane switching is a mechanism to improve power/performance management (i.e., train down to x1 to save power and train up to x16 to get the performance); therefore the link will remain in x1.

Workaround: For graphics controllers that perform run-time lane switching during "configuration" state, a driver workaround has been identified. Please contact graphics controller vendor for driver status.

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

4. Visual Corruption with Integrated Graphics and Intel® Flex Memory Technology Enabled Using Microsoft Windows Vista* Operating System

Problem: Visual corruption is observed with the Mobile Intel 965 Express Chipset GMCH using new Microsoft Windows Vista* paging model when Intel® Flex Memory Technology is enabled in the Dual Channel Asymmetric configuration

Implication: Visual graphics corruption on the display when running 3D applications.

Workaround: Use latest Intel® Graphics Driver (Revision 15.4.3 or later).

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

5. Mobile Intel 965 Express Chipset Family MSI De-Feature (Device 2 only)

Problem: Mobile Intel 965 Express Chipset Integrated Graphics (Device 2) interrupt may be delayed or missed on (G)MCH with Message Signaled Interrupt enabled.

Implication: System may generate TDR- Timeout Detection and Recovery message, which results in a graphics hardware reset.

Workaround: Disable MSI for Device 2. MSI is already disabled in the Intel® Graphics Media Accelerator Driver.

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

6. Mobile Intel® 965 Express Chipset Family Display Brightness Erratum

Problem: Writes to an integrated graphics display register are not always detected by the (G)MCH.

Implication: Display brightness might not change as expected.

Workaround: A driver workaround has been implemented in the Intel® Graphics Media Accelerator Driver, Rev 15.6 for Windows Vista* and Rev 14.31 for Windows* XP operating system.

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

7. Incorrect Low-Priority Interrupt Redirection by Mobile Intel 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH on C5 Exit

Problem: Upon C5 exit, the Mobile Intel 965 Express Chipset Family Graphics Memory Controller Hub (G)MCH may redirect a low priority interrupt to a CPU core that it was not assigned.

Implication: May result in OS error message.

- This error has not been observed with any commercially-available software**.**

Workaround: Operating systems should not enable low-priority interrupts to the processor.

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

8. Mobile Intel 965 Express Chipset Family Unexpected DDR RCOMP Update

Problem: Following boot or resume from S3, S4, S5, M1, or MOFF, the Mobile Intel 965 Express Chipset may experience an internal clock crossing issue causing the Force DDR RCOMP configuration bit to be incorrectly left enabled (='1'), after SW attempts to clear the bit.

Implication: Unexpected system behavior may be experienced due to an unexpected update of DDR RCOMP occurring during a memory write cycle

- No failures have been observed during normal operation. This erratum has only been observed under a synthetic test environment where:
  - DRAM write occurs during unexpected DDR RCOMP update
  - DDR RCOMP buffer update values to roll over from '1Fh to 20h' during the memory write
  - FSB to DDR Clocking Ratio 800 MHz to 667 MHz
  - No failures observed for FSB to DDR Clocking Ratios:
    - 800 MHz to 533 MHz or 533 MHz to 533 MHz

Workaround: A workaround exist contact your local Intel representative for details

Status: No Fix. For additional stepping information, see the Summary Tables of Changes.

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Specification Changes

There are no specification changes in this Specification Update revision.

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Specification Clarifications

1. DMA Transfer Completion for Latency Sensitive Devices

It has been seen that DMA transfers on some latency sensitive devices may incur completion delays during heavy external PCI Express Graphics traffic to cacheable memory regions. These latency sensitive devices have been typically used in AC mode.

The completion delays do not violate platform or industry specifications.

If such completion delays are encountered, a system BIOS configuration change to disable C3 may allow a device to be serviced during heavy external PCI Express Graphics traffic.

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Documentation Changes

1. Removing Section 10.2 Thermal Characteristics

Contact your local Intel field representative for additional information regarding for the latest thermal characteristics specifications.

2. SDVOB_INT and SDVOC_INT Signal Naming

Changes are in RED font.

Section 2.3.1 Table 1 SDVO and PCI Express*-Based Graphics Port Signal Mapping (Sheet 2 of 2)

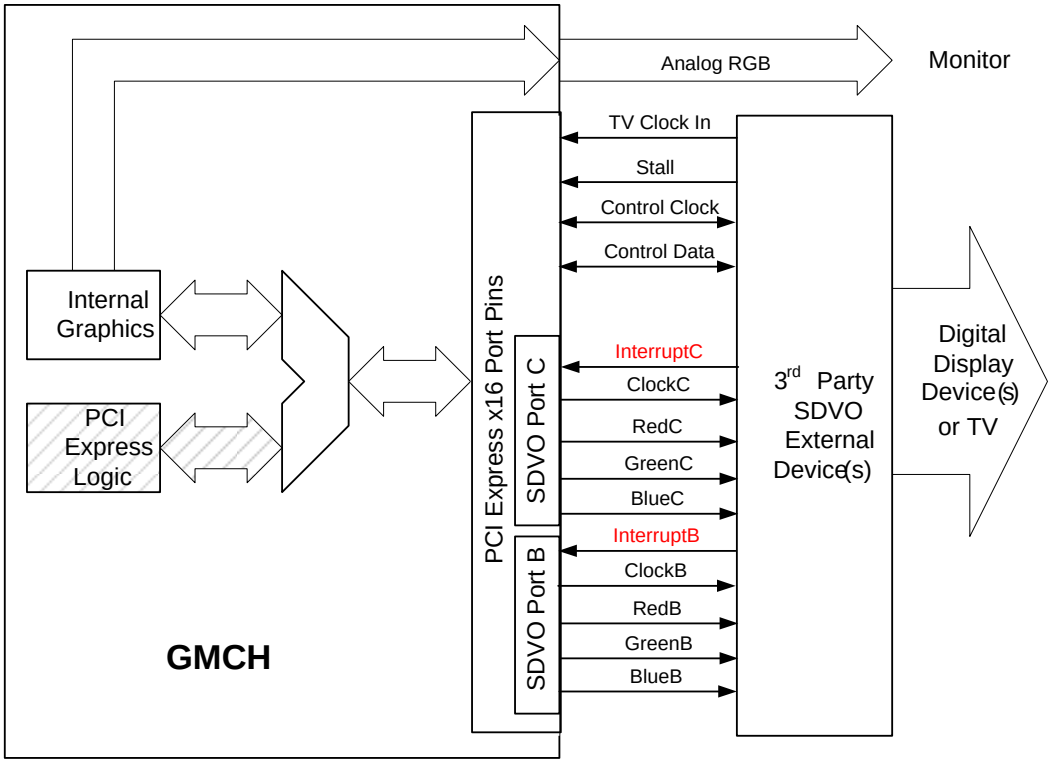
SDVO Mode	PCI Express Mode
SDVOB_INT	PEG_RXP1
SDVOB_INT#	PEG_RXN1
SDVOC_INT	PEG_RXP5
SDVOC_INT#	PEG_RXN5

Section 2.5.4 Serial DVO Interface

Signal Name	Type	Description
SDVO B Interface		
SDVOB_INT	I PCI Express	**Serial Digital Video Field Stall Complement:** Multiplexed with PEG_RXP1
SDVOB_INT#	I PCI Express	**Serial Digital Video Field Stall Complement:** Multiplexed with PEG_RXN1
SDVO C Interface		
SDVOC_INT	I PCI Express	**Serial Digital Video Field Stall Complement:** Multiplexed with PEG_RXP5
SDVOC_INT#	I PCI Express	**Serial Digital Video Field Stall Complement:** Multiplexed with PEG_RXN5

SDVO Common Signals		
~~SDVOB_INT~~	~~I~~ ~~PCI Express~~	~~**Serial Digital Video Field Stall Complement:**~~ ~~Multiplexed with PEG_RXP1~~
~~SDVOB_INT#~~	~~I~~ ~~PCI Express~~	~~**Serial Digital Video Field Stall Complement:**~~ ~~Multiplexed with PEG_RXN1~~

Section 6.3.1 Figure 10 SDVO Conceptual Block Diagram



Section 12 Table 27 Signal Groups (Sheet 1 of 4)

Signal Group	Signal Type	Signals	Notes
Serial DVO or PCI-Express Graphics Interface Signal Groups			
(f)	I PCI Express	**PCI-E GFX Interface:** PEG_RX[15:0], PEG_RX#[15:0] **SDVO Interface:** SDVO_TVCLKIN#, SDVO_TVCLKIN, ~~SDVO_INT#, SDVO_INT~~, SDVOB_INT#, SDVOB_INT, SDVOC_INT#, SDVOC_INT, SDVO_FLD_STALL#, SDVOB_FLD_STALL	Refer to Table 1 "SDVO and PCI Express* Based Graphics Port Signal Mapping" for pin multiplexed mapping

3. Host/Memory/Graphics Clock Frequency Support for 1.05-V Core Voltage the Mobile Intel GM965 and GL960 Express Chipsets

Changes are in RED font.

Table 31 (*Mobile Intel ® 965 Express Chipset Family Datasheet*)
Host/Memory/Graphics Clock Frequency Support for 1.05 V core voltage the Mobile Intel GM965 and GL960 Express Chipsets

Host (MHz)	Memory (MHz)	Display Clock (MHz)	Render Clock (MHz)
667	DDR2-533	333	267(GM956)/333(GM965)/ 444(GM965)

4. 1 Gb x 16 DDR2 device support added to System Memory Organization Support for DDR2

Changes are in RED font.

Section 5.1 Table 9 System Memory Organization Support for DDR2

DDR2								
Tech	**SDRAM Org**	**SO-DIMM Size**	**SO-DIMM Org**	**Banks**	**Ranks**	**Page Size (dev/ module)**	**Max Capacity (2 SO-DIMMs)**	**Freq**
256 Mb	x8	256 MB	32Mx64	4	1	1K/8k	512 MB	533/667
256 Mb	x16	128 MB	16Mx64	4	1	1K/4k	256 MB	533/667
256 Mb	x16	256 MB	32Mx64	4	2	1K/4k	512 MB	533/667
512 Mb	x8	512 MB	64Mx64	4	1	1K/8k	1 GB	533/667
512 Mb	x8	1GB	128Mx64	4	2	1K/8k	2 GB	533/667
512 Mb	x16	256 MB	32Mx64	4	1	~~1K~~2k/8k	512Mb	533/667
512 Mb	x16	512 MB	64Mx64	4	2	2K/8K	1 GB	533/667
1 Gb	x8	1 GB	128Mx64	8	1	~~2K~~1k/8K	2 GB	533/667
1 Gb	x8	~~1~~2 GB	256Mx64	8	2	1K/8k	4 GB	533/667
1 Gb	x16	512 MB	~~32~~64Mx64	8	1	~~1~~2K/4K	1 GB	533/667
1 Gb	x16	1 GB	128Mx64	8	2	~~1~~2K/4K	2 GB	533/667

5. Analog Port Characteristic for HSYNC/VSYNC

Changes are in RED font.

Section 8.4.1 Table 15 Analog Port Characteristics

Signal	Port Characteristics	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	~~2.5v~~ 3.3 V
-	Enable/Disable	Port Control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5 V
	Control	Through GPIO interface

6. Add Section 5.3.1.1 Single Channel Population Rules for Systems with Intel® Management Engine Enabled

Channel 0 should always be populated in either of the below cases, as it will be required for Intel Management Engine operation:

- Intel® Active Management Technology (Intel® AMT) Enabled

In the case of Non-AMT systems, either channel 0 or channel 1 may be populated.

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