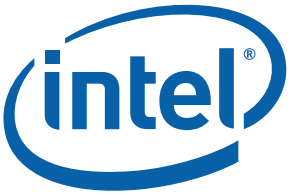

Intel® I/O Controller Hub 8 (ICH8) Family

Specification Update

– For the Intel® 82801HB ICH8, 82801HR ICH8R, 82801HH ICH8DH, and 82801HO ICH8DO, 82801HBM ICH8M, and 82801HEM ICH8M-E I/O Controller Hubs

May 2012

Notice: The Intel® ICH8 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Order Number: 313057-025

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Revision History

NDA Revision	Description	Date
-001	• Initial Release	June 2006
-002	• Added 82801HH ICH8DH and 82801HO ICH8DO.	July 2006
-003	• Added Items: • Errata: 5-Intel® ICH8 PCI Express* Root Port Power State Value, 6-Intel® ICH8 LAN APM Wakeup After G3	August 2006
-004	• Added Items: • Errata: 7-Intel® ICH8 Integrated LAN DMA Error, 8-Intel® ICH8 ICH8 PCI Express* Upstream Link Base Address Register Bit 0 • Specification Clarifications: 1-Thermal Sensors Functionality Clarification, 2-Internal Voltage Regulator Usage Clarification • Document Changes: 2-Thermal Sensors Register Change	September 2006
-005	• Added Items: • Errata: 9-Intel® ICH8 Simple Serial Transport (SST) TH0 and TH1Timing • Specification Changes: 1-t294 Timing Change, 2-Power Plane Table Change, 3-t313 Timing Addition • Specification Clarifications: 3-ICH8 ME Soft Strap Clarification, 4-MCH ME Soft Strap Clarification, 5-Functional Strap Clarification, 6-Boot BIOS Strap Register Clarification, 7-PCI Express* Strapping Clarification, 8-PCI Express* Overview Clarification, 9-Signal Description Clarifications, 10-Host Power Cycle Clarification, 11-SATA Register Clarifications, 12-SYNC Field Clarification • Document Changes: 3-Device 31 Interrupt Pin Register Change, 4-Device 30 Interrupt Pin Register Change, 5-Device 26 Interrupt Route Register Change, 6-Device 25 Interrupt Route Register Change, 7-Root Port Configuration Register Change, 8-Timing Diagram Updates, 9-SPI Register Change, 10-Timer Configuration and Capabilities Register Change, 11-RTC Update Cycle Inhibit (SET) Bit Correction	November 2006
-006	• Added Items: • Errata: 10-ICH8 PCI Express* Endpoint L0/L1 Acceptable Latency Bits • Specification Changes: 4-t294 Timing Change and t307 Addition • Document Changes: 12-t294 Timing Change and t307 Addition, 13-AHCI Support Clarification	December 2006
-007	• Added Items: • Errata: 11-ICH8 USB K-State Reflection on Resume • Document Changes: 14-Pull-Up on GPIO[33], 15-WOL_EN Signal Description Clarification, 16-Flash Region (FLREG) Registers Clarification, 17-Interrupt Mapping Clarification, 18-8259 Interrupt Controller Clarification, 19-APIC Enable (AEN) Bit Clarification, 20-Reset Control Register (CF9h) Clarification • Modified Specification #4: Removed RSMRST# from Figure 30. • Modified Document Change #8: Removed RSMRST# from Figure 36	February 2007
-008	• Added Items: • Errata: 12-ICH8 UHCI Hang with USB Reset, 13-ICH8 Thermal Sensor Temperature Reading • Document Changes: 21-Write Combining Correction, 22-GPIO_USE_SEL Registers Correction, 23- PWROK Glitch-free Clarification	March 2007

NDA Revision	Description	Date
-009	• Added Mobile ICH8M products (82801HBM ICH8M, and 82801HEM ICH8M-E I/O Controller Hubs) • Removed items as this information has been added to the datasheet, Revision -003: — Specification Changes 1-4 — Specification Clarifications 1-12 — Documentation Changes 2-23 Note: Documentation Change 1 (Revision ID and Device ID information) was moved to the Identification Information section • Added Errata 14-15	May 2007
-010	• Added: — Errata: 16-High Speed (HS) USB 2.0 D+ and D- maximum Driven Signal Level, 17-GbE Packet Buffer Writing Error, 18-ICH8 THRM Polarity on SMBus. — Specification Changes:1-SPI Specification Addition. — Specification Clarifications: 1-RTC Register A Clarification, 2-GLANCLK High Time/ Low Time Clarification. — Document Changes: 1-Bit 0 Function Disable Register Correction.	September 2007
-011	• Added: — Errata: 19-AHCI Reset and MSI Request, 20-PET Alerts on SMBus, 21-High-speed USB 2.0 V_{HSOH} — Specification Changes:2-USB 2.0 Power Management Description, 3-Removing Support for USB Wake from S5. — Specification Clarifications: 3-USB UHCI Run/Stop Bit Clarification — Document Changes: 2-PWROK Description Correction, 3-SMBus/SMLink Connectivity Clarification • Updated Device ID and Revision ID table to include information on ICH8M B1 stepping	November 2007
-012	• Added: — Errata: 22-SMBus Host Controller May Hang, 23-SATA Gen1 Initialization / LPM Erratum. — Specification Changes: 4-Addition of EHCI Parity Error Response.	April 2008
-013	• This revision was for administrative management only and was not released	
-014	• Added: — Document Changes: 4-CK_PWRGD Pin State Correction, 5-SATA Registers Corrections • Updated Identification Information Section to include top marking and Device ID for ICH8M B2 stepping	June 2008
-015	• Added: — Errata: 24-ICH8M B2 Stepping Gigabit Ethernet Controller RID with CRID Enabled Erratum	July 2008
-016	• Added: — Document Changes: 6-SATA Interlock Switch State (ISS) Bit Clarification, 7-HPET Timer, 8-Timing Figure Clarification	September 2008
-017	• Added: — Specification Clarifications: 4-t290 and t294 Clarification — Document Changes:9-GPIO_USE_SEL Override Register Description Correction	October 2008
-018	• Added: — Document Change: 10-Add ballout AH19(VSS) to Table 147	April 2009
-019	• Added: — Errata: 25-Intel® I/O Controller Hub 8 (ICH8) Family PCI Express Function Disable — Document Change: 11-Correct Section 5.13.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure	October 2009
-020	• Added: • Document Change: 12 - Correct section 9.1.21 Bits 15:2 definition • Document Change: 13 - Correct Figure 20 and Figure 21 Ballout information	May 2010
-021	• Updated Document Change 13 - Correct Figure 20 and Figure 21 Ballout information • Added: • Document Change: 14 - Correct section 11.1.43 bit 0 definition	June 2010

NDA Revision	Description	Date
-022	• Added Items: — Document Changes: 15 - Correct A20M#Signal Description — Document Changes: 16 - Update Section 8.2 in the Datasheet — Errata: 26 Intel® ICH8 SATA GEN3 Device Detection	December 2010
-023	• Updated: • Errata: 26 Intel® ICH8 SATA GEN3 Device Detection	March 2011
-024	• Added Items: — Document Changes: 17 - Correct OUTSTRMPAY Register information — Document Changes: 18 - Correct INSTRMPAY Register information	December 2011
-025	• Added Items: — Errata: 27-Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled — Specification Change: 5-ROAEI options removal for OCW2.	May 2012

§ §

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Note: Throughout this specification update, ICH8 is used as a general ICH8 term and refers to the 82801HB ICH8, 82801HR ICH8R, 82801HDH ICH8DH, and 82801HDO ICH8DO, 82801HBM ICH8M and 82801HEM ICH8M-E components, unless specifically noted otherwise.

Affected Documents/Related Documents

Title	Document Number
Intel® I/O Controller Hub 8 (ICH8) Family Datasheet	313056-003

Nomenclature

Errata are design defects or errors. Errata may cause the ICH8's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the Intel® I/O Controller Hub 8 (ICH8) family. Intel intends to fix some of the errata in a future stepping of the component(s), and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Specification Change, Erratum, Specification Clarification or Documentation Change that applies to a stepping or to this product line.

(No mark) or

(Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc: Document change or update that will be implemented.

PlanFix: This erratum may be fixed in a future stepping of the product.

Fixed: This erratum has been previously fixed.

No Fix: There are no plans to fix this erratum.

Bar: This item is either new or modified from the previous version of the document.

NO.	Stepping			Status	ERRATA
	B0	B1	B2		
1	X			No fix	Intel ICH8 TCO Mode Strap
2	X	X		No Fix	Intel ICH8 1.5-Gb/s SATA Signal Voltage Level
3	X	X		No Fix	Intel ICH8 Reset Command Received through SMBus during Suspend
4	X	X		No Fix	Intel ICH8 Forced Shutdown Event with Integrated GbE LAN (ICH8/ICH8R/ICH8DH Only)
5	X	X		No Fix	Intel ICH8 PCI Express Root Port Power State Value
6	X			No Fix	Intel ICH8 LAN APM Wakeup after G3
7	X			No Fix	Intel ICH8 Integrated LAN DMA Error
8	X	X	X	No Fix	Intel ICH8 PCI Express Upstream Link Base Address Register Bit 0

NO.	Stepping			Status	ERRATA
	B0	B1	B2		
9	X			No Fix	Intel ICH8 Simple Serial Transport (SST) TH0 and TH1Timing
10	X	X	X	No Fix	ICH8/ICH8M PCI Express* Endpoint L0/L1 Acceptable Latency Bits
11	X	X	X	No Fix	ICH8 USB K-State Reflection on Resume
12	X	X	X	No Fix	Intel(R) ICH8/ICH8M UHCI hang with USB reset
13	X			No Fix	ICH8 Thermal Sensor Temperature Reading
14	X	X	X	No Fix	Intel(R) ICH8/ICH8M USB Resume EOP missing
15		X	X	No Fix	Intel(R) ICH8M IDE input buffer V+ & Vih spec violation
16	X	X	X	No Fix	ICH8 High Speed (HS) USB 2.0 D+ and D- maximum Driven Signal Level
17	X	X	X	No Fix	ICH8 GbE Packet Buffer Writing Error
18	X	X	X	No Fix	ICH8 THRM Polarity on SMBus
19	X	X	X	No Fix	AHCI Reset and MSI Request
20	X	X	X	No Fix	PET Alerts on SMBus
21	X	X	X	No Fix	High-speed USB 2.0 V_{HSOH}
22	X	X	X	No Fix	SMBus Host Controller May Hang
23	X	X		No Fix (Desktop) Fixed (Mobile)	SATA Gen1 Initialization/LPM Erratum
24			X		ICH8M B2 Stepping Gigabit Ethernet Controller RID with CRID Enabled Erratum
25	X	X	X	No Fix	Intel® I/O Controller Hub 8 (ICH8) Family PCI Express Function Disable
26	X	X	X	No Fix	Intel® ICH8 SATA GEN3 Device Detection
27	X	X	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

No.	SPECIFICATION CHANGES
1	SPI Specification Addition
2	USB 2.0 Power Management Description,
3	Removing Support for USB Wake from S5
4	Addition of EHCI Parity Error Response.
5	ROAEI options removal for OCW2

No.	SPECIFICATION CLARIFICATIONS
1	RTC Register A Clarification

No.	SPECIFICATION CLARIFICATIONS
2	GLANCLK High Time/Low Time Clarification
3	USB UHCI Run/Stop Bit Clarification
4	t290 and t294 Clarification

No.	DOCUMENTATION CHANGES
1	Bit 0 Function Disable Register Correction
2	PWROK Description Correction,
3	SMBus/SMLink Connectivity Clarification
4	CK_PWRGD Pin State Correction
5	SATA Registers Corrections
6	SATA Interlock Switch State (ISS) Bit Clarification
7	HPET Timer
8	Timing Figure Clarification
9	GPIO_USE_SEL Override Register Description Correction
10	Add ballout AH19(Vss) to Table 147
11	Correct Section 5.13.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure
12	Correct section 9.1.21 Bits 15:2 definition
13	Correct Figure 20 and Figure 21 Ballout information
14	Correct section 11.1.43 bit 0 definition
15	Correct A20M#Signal Description
16	Update Section 8.2 in the Datasheet
17	
18	

Identification Information

Markings

ICH8 Stepping	S-Spec	Top Marking	Notes
B0	SL9MN	NH82801HB	82801HB ICH8 Base
B0	SL9MK	NH82801HR	82801HR ICH8R
B0	SL9ML	NH82801HH	82801HH ICH8DH
BO	SL9MM	NH82801HO	82801HO ICH8DO
B1	SLA5Q	NH82801HBM	82801HBM ICH8M Base
B1	SLA5R	NH82801HEM	82801HME ICH8M-E Enhanced
B2	SLB9A	NH82801HBM	82801HBM ICH8M Base
B2	SLB9B	NH82801HEM	82801HEM ICH8M-E Enhanced

Device ID and Revision ID Values

PCI Revision ID Register values and Device ID Register values for all ICH8 functions are shown below. This information is not in the datasheet. This is the standard reference document.

Device Function	Description	Intel® ICH8 Dev ID[1]	ICH8 B0 Rev ID	ICH8 B1 Rev ID	ICH8 B2 Rev ID	Comments
D31:F0	LPC	2810h	02h	N/A	N/A	ICH8, ICH8R
		2815h	02h	03h	04h	ICH8M
		2812h	02h	N/A	N/A	ICH8DH
		2814h	02h	N/A	N/A	ICH8DO
		2811h	02h	03h	04h	ICH8M-E
D31:F2	SATA	2820h	02h	N/A	N/A	Desktop Non-AHCI and Non-RAID Mode[1]
		2821h	02h	N/A	N/A	Desktop AHCI Mode supporting 6 ports[1]
		2822h	02h	N/A	N/A	Desktop RAID 0/1/5 Mode[1]
		2824h	02h	N/A	N/A	Desktop AHCI Mode supporting 4 ports[1]
		2828h	02h	03h	04h	Mobile Non-AHCI and Non-RAID Mode[1]
		2829h	02h	03h	04h	Mobile AHCI Mode
		282Ah	02h	03h	04h	Mobile RAID 0/1 Mode[1]
D31:F5	SATA	2825h	02h	N/A	N/A	Desktop Non-AHCI and Non-RAID Mode[1]
D31:F3	SMBus	283Eh	02h	03h	04h	
D31:F6	Thermal	284Fh	02h	03h	04h	
D31:F1	IDE	2850h	02h	03h	04h	ICH8M
D30:F0	DMI to PCI Bridge	244Eh	F2h	N/A	N/A	Desktop
		2448h	F2h	F3h	F4h	Mobile
D29:F0	USB UHCI #1	2830h	02h	03h	04h	
D29:F1	USB UHCI #2	2831h	02h	03h	04h	
D29:F2	USB UHCI #3	2832h	02h	03h	04h	
D29:F7	USB EHCI #1	2836h	02h	03h	04h	
D26:F0	USB UHCI #4	2834h	02h	03h	04h	
D26:F1	USB UHCI #5	2835h	02h	03h	04h	
D26:F7	USB EHCI #2	283Ah	02h	03h	04h	
D28:F0	PCI Express* Port 1	283Fh	02h	03h	04h	
D28:F1	PCI Express Port 2	2841h	02h	03h	04h	
D28:F2	PCI Express Port 3	2843h	02h	03h	04h	
D28:F3	PCI Express Port 4	2845h	02h	03h	04h	
D28:F4	PCI Express Port 5	2847h	02h	03h	04h	
D28:F5	PCI Express Port 6	2849h	02h	03h	04h	
D27:F0	Intel® High Definition Audio	284Bh	02h	03h	04h	
D25:F0	LAN	104Bh[2]	02h	03h	04h	

Notes:

1. ICH8 contains two SATA devices (for Desktop Only). The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the ICH8 component.
2. Loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the device ID location, then 104Bh is used. Refer to the ICH8 EEPROM Map and Programming Guide for LAN Device IDs.

Errata

1. Intel® ICH8 TCO Mode Strap

Problem: The ICH8 B0 stepping implements the TCO Mode soft strap in the VccCL power well. When VccCL power is lost or a global reset is asserted, the TCO Slave Unit Mode will be set to Legacy TCO mode.

Implication: When in Legacy TCO mode, all ICH8 TCO SMBus slave unit functionality is assigned to the SMLINK[1:0] interface, not the SMBus interface. SMBus masters connected to the SMBus will not be able to access the ICH8 TCO slave unit.

Workaround: All Desktop platforms

- Connect SMBus and SMLINK pins together (connect SMLINK0 to SMBCLK and SMLINK1 to SMBDATA) and program STRP0.TCOMODE (FISBA+000h:bit 7) to '0b' in the flash descriptor region in the SPI part.
  - — If no descriptor region is in SPI or SPI is not used, connect the SMBus and SMLINK pins together as described above.

Status: No fix (Desktop Only). For affected steppings, see the *Summary Table of Changes*.

2. Intel® ICH8 1.5 Gb/s SATA Signal Voltage Level

Problem: The ICH8 1.5 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the ICH8 SATA 1.5 Gb/s (Gen1i) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 7.2.1 of Serial ATA Specification, rev 2.5).

Implication: None known.

Workaround: None.

Status: No plan to fix. For affected steppings, see the *Summary Table of Changes*.

3. Intel® ICH8 Reset Command Received Through SMBus During Suspend

Problem: If the ICH8 is sent a 'Hard Reset Without Cycling' command on SMBus while the system is in S3, the reset command and any other write commands accepted by the ICH8 SMBus will not be executed until the next wake event. The ASF Spec, rev 2.0, requires the ICH8 to execute the Hard Reset Without Cycling immediately.

Implication: SMBus write commands that are accepted by the ICH8 are not lost, but completion occurs after the next system wake event. This also applies to any SMBus wake commands accepted after a 'Hard Reset Without Cycling' command, such that the SMBus wake command will not cause the system to wake.

Note: Intel® Active Management Technology is not impacted as Intel® AMT does not use the Hard Reset Without Cycling command while the system is in S3.

Note: Any SMBus read that is accepted by the ICH8 will complete normally.

Workaround: Do not send a Hard Reset Without Cycling command while the system is in S3.

Note: Exposure to this issue can be reduced by issuing a wake command prior to issuing the Hard Reset Without Cycling command.

Status: No Fix. For affected steppings, see the *Summary Table of Changes*.

4. Intel® ICH8 Forced Shutdown Event with Integrated GbE LAN

Problem: If all of the following occur:

1. Forced Shutdown/Reset event occurs thru one of the following means:
   - — Power Button Override
   - — THRMTRIP# signal assertion
   - — CF9-type reset with CF9h Global Reset policy bit set to 1: A) Write of 06h or 0Eh to CF9h register; or B) Shutdown VDM received with Shutdown Policy Select bit set.
   - — Core Power Failure occurs (PWROK or VRMPWRGD deasserting)
2. While the system is connected at 1000 Mbps with ICH8 integrated GbE LAN
3. And the LAN_RST# signal remains deasserted during the forced shutdown/reset event,

Then the ICH8 integrated GbE LAN may not properly transition to 10/100 mode. This is because the LCD Configuration Area read to the NVM may not complete and the integrated GbE LAN may not enter the appropriate state.

Note: Typically, LAN_RST# remains de-asserted when remote system management is enabled (e.g., Wake On LAN). LAN_RST# implementation is platform-specific.

Implication: System may hang on next reboot. The hang occurs at the first access to ICH8 integrated GbE LAN memory space.

Workaround: Driver and GbE NVM workaround available (both elements are required for workaround):

- Driver: Use Build 123461 Version 11.0C0279 or later.
- GbE NVM: Disable the LCD Configuration Area read to the NVM by setting bit 13 of Word 0x14h to 0 in the ICH8 GbE NVM image. This is implemented in NVM version 1.0 and later.

Status: No Fix. For affected steppings, see the *Summary Table of Changes*.

5. Inte®l ICH8 PCI Express* Root Port Power State Value

Problem: The ICH8 PCI Express root ports support the D3 and D0 states, but also accept writes of values corresponding to the D2 and D1 states in the Power State bit field of the Power Management Control and Status registers (D28:F0/F1/F2/F3/F4/F5:A4h). The

ICH8 PCI Express root port PCI Power Management Capabilities Registers (D28:F0/F1/F2/F3/F4/F5:A2h) do not claim support of D2 and D1 power states.

Implication: No functional implications known. Writes of values corresponding to the D2 and D1 states (i.e., 10b or 01b) do not cause behavioral changes within the ICH8, but the value is displayed in the Power State bit field.

Workaround: Software should not write unsupported power state values (i.e., 10b or 01b) to the Power State bit field of the Power Management Control and Status register.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

6. Intel ICH8 LAN APM Wakeup After G3

Problem: The APM Wakeup enable bit, which controls if the ICH8 supports Wake on LAN (WOL) in response to a magic packet in S5, is in a region of the LAN NVM (Nonvolatile Memory) that is read only after PLTRST# deasserts when the system boots to S0.

Implication: Integrated LAN does not provide support for WOL after a G3 to S5 transition until PLTRST# deasserts because the default state of the APM Wakeup enable bit is disabled. Additionally, because WOL is disabled, a LAN link will not be established and LAN will remain in the off state until PLTRST# deasserts.

Implication: Platform must briefly transition to S0 and then may return to S5. BIOS workaround available; Contact your Intel field representative for the latest BIOS information

Status: No Fix (Desktop Only). For steppings affected, see the *Summary Tables of Changes*.

7. Intel ICH8 Integrated LAN DMA Error

Problem: The ICH8 integrated LAN DMA engine may experience an internal error on some systems where a specific alignment of internal logic clock domains may exist and when all of the following additional conditions are met:

- An internal DMA buffer is full
- A read request directly follows a write request to the DMA buffer
- The next request packet size is larger than 128 Bytes
- Alignment of DMA buffer read and write pointers

Note: Issue has only been reproduced under synthetic lab conditions.

Implication: The LAN DMA engine error may cause transmitted data from the ICH8 integrated LAN to be incorrect.

Note: Data error occurs before CRC calculation; erroneous data cannot be detected by CRC check by LAN interface partner.

Workaround: Update ICH8 NVM to version 1.1 or later to cover all known failures. Update Intel LAN driver to Trout Lake version 1.1 Build 125734 or later as soon as feasible to cover both all known and theoretical failures.

- NVM Change: Program bit 1 of Word 0x13h to 0 in the ICH8 GbE NVM image. This is implemented in NVM version 1.1 and later.
- Through extensive validation and focused testing, Intel has not observed failures with bit 1 of Word 0x13h set to 0 in the ICH8 NVM image. To protect against a theoretical case where the issue could occur even when the NVM image is updated, Intel recommends a driver update that customers should implement as soon as feasible.

Note: If able to immediately implement driver workaround, NVM change is not required.

Status: No Fix. (Desktop Only). For steppings affected, see the *Summary Tables of Changes*.

8. Intel® ICH8 PCI Express* Upstream Link Base Address Register Bit 0

Problem: The ICH8 PCI Express root ports' Upstream Link Base Address (ULBA) Register (D28:F0/F1/F2/F3/F4/F5:198h) bit 0 mirrors the value of bit 0 in the ICH8 RCBA

register (D31:F0:F0h). During normal system operation, bit 0 of the RCBA register is set to 1. This results in bit 0 of the ULBA also being set to 1. The PCI Express specification, rev 1.1, requires that bit 0 of the ULBA be 0.

Implication: No functional implications known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

9. Intel® ICH8 Simple Serial Transport (SST) TH0 and TH1 Timing

Problem: The ICH8 may violate the SST TH0 and TH1 minimum specification when driving the SST bus.

Implication: The SST controller may not be able to access the SST device that utilizes sampling times above 0.56xTBIT.
Note: a SST-spec compliant device can utilize sampling times above 0.56xTBIT and up to 0.60xTBIT

Workaround: If SST supported device samples the bus at 0.56xTBIT or above then the board designer may implement a capacitor to ground on the SST signal. The value of the capacitor can be determined using the following formula:

Cap Value = (SSTSysCReq) – (MBLength*MBTraceC) – [(NumberSSTDev + 1)*SSTDevC]

Where: SSTSysCReg = SST System Capacitance Requirement (100 pF min, 140 pF typ, 170 pF max)
MBLength = Total SST trace length on the motherboard (inch)
MBTraceC = Motherboard Trace Capacitance per inch (2.6 pF min, 3.2 pF typ, 3.8 pF max)
NumberSSTDev = Total number of SST devices implemented on motherboard
SSTDevC = Capacitance of SST device (6 pF min, 8 pF typ, 10pF max)
Note: Recommended capacitor value can be obtained using the typ values
Capacitor value range can be determined using min and max values
Do not mix and match min, typ and max values in the calculation

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

10. ICH8 PCI Express* Endpoint L0/L1 Acceptable Latency Bits

Problem: The ICH8 implements the PCI Express* Endpoint L0/L1 Acceptable Latency bits (bits [8:6] and [11:9] in Device Capabilities Register) as RO with the value of '1'. The PCI Express Specification rev 1.1 requires the bits to be RO with the value of '0'.

Implication: There is no known impact to platform functionality. The platform may flag a failure for each bit field with Microsoft Vista* Compliance test.

Workaround: None.
Intel is working with Microsoft to get contingencies for the failures.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

11. ICH8 USB K-State Reflection on Resume

Problem: Upon resuming from a USB wake-up event from S3-S4, the ICH8 USB host controller (UHCI or EHCI) may not reflect the resume K-state sent by the USB device back onto the bus as required by the USB 2.0 Specification.

Implication: A USB LS/FS device that wakes the system may stop functioning after the system resumes from S3-S4.

Note: A USB HS device that wakes the system is not impacted as the USB driver will reset the port when the device is not responding after resume.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

12. ICH8 UHCI Hang with USB Reset

Problem: When SW initiates a Host Controller Reset or a USB Global Reset while concurrent traffic occurs on at least three UHCI controllers, the UHCI controller(s) may hang. The issue has only been replicated in a synthetic reset test environment.

Implication: System may hang.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: No Fix. For stepping affected, see the *Summary Tables of Changes.*

13. ICH8 Thermal Sensor Temperature Reading

Problem: The ICH8 thermal sensor reading, which is available through Intel® Quiet System Technology (Intel® QST), may not update and not reflect the actual ICH8 sensor temperature.

Implication: System with Intel® QST may not display the actual ICH temperature using a temperature displaying SW. The temperature reading may appear to be stuck at a value, normally 63 C.

Note: There is no known impact to the Intel® QST operation, nor thermal impact to the ICH8.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: No Fix. For stepping affected, see the *Summary Tables of Changes.*

14. Intel ICH8M USB Resume EOP

Problem: Upon resume from a USB wake-up event, the ICH8M USB UHCI host controller may not send the resume EOP as required by the USB 2.0 specification.

Implication: A USB LS/FS device that wakes the system may stop functioning after the system resumes from S3-S4. There is no known impact to USB HS devices.

Workaround: BIOS workaround available; Contact your Intel field representative for the latest BIOS information

Status: No Fix. For steppings affected, see the Summary Tables of Changes.

15. Intel ICH8M IDE input buffer V+ & Vih Specification Violation

Problem: Under maximum voltage condition of the Vcc3_3 power rail (3.4655 V), the ICH8M may violate the PATA IDE V+ max (low-to-high input threshold) and Vih15 min (input high voltage) specifications. The limit in both cases is specified as 2.0V.

Implication: The ICH8M may not switch on a low-to-high transition until V+ max is at a2.1V, and may not register a logic high until Vih15 min is at 2.1V. There is no known impact to system functionality. This issue has only been seen in a synthetic test environment, as an IDE device typically drives the input to 3.3V.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

16. ICH8 High Speed (HS) USB2.0 D+ and D- Maximum Driven Signal Level

Problem: During Start-of-Packet (SOP)/End-of-Packet (EOP), the ICH8 may drive D+ and D- lines to a level greater than USB 2.0 spec +/-200mV max.

Implication: May cause High Speed (HS) USB 2.0 devices to be unrecognized by OS or may not be readable/writable if the following two conditions are met:

- The receiver is pseudo differential design
- The receiver is not able to ignore SE1 (single-ended) state

Note: Intel has only observed this issue with a motherboard down HS USB 2.0 device using pseudo differential design. This issue will not affect HS USB 2.0 devices with complementary differential design or Low Speed (LS) and Full Speed (FS) devices

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

17. ICH8 GbE Packet Buffer Writing Error

Problem: With System Defense enabled, the ICH8 integrated LAN's Packet Buffer writing mechanism may encounter an internal error when there are two consecutive write requests to the same address of the Packet Buffer.

Note: Issue has only been reproduced under synthetic lab conditions. In addition, two consecutive write requests to the same address in the Packet Buffer do not happen under typical operating conditions.

Implication: Incorrect data may be transmitted from the ICH8 integrated LAN controller

Note: The erroneous data will be detected by the receiver's checksum calculation and will not get to the application level. The packet will be either re-transmitted (TCP protocol) or dropped (UCP protocol).

Workaround: Driver workaround available

- Use released driver version 9.7.32.0 or later for NDIS 6
- Use released driver version 9.7.34.0 or later for NDIS 5.x

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

18. ICH8 THRM Polarity on SMBus

Problem: When THRM#_POL (PMBASE+42h:bit0) is set to high, the THRM# pin state as reported to the SMBus TCO unit is logically inverted.

Implication: If the THRM#_POL bit is set to high, an external SMBus master reading the BTI Temperature Event status will not receive the correct state of the THRM# pin. The value will be logically inverted. If THRM#_POL set to low, value is correct.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.

19. AHCI Reset and MSI Request

Problem: If the ICH8 AHCI SATA controller receives a HBA reset while MSI interrupts are enabled, a boundary condition exists where the ICH8 SATA controller may respond to a non-posted request that is intended for another ICH8 function.

Implication: Issue has only been observed in a synthetic test environment. Unexpected system behavior may occur. System implication may vary depending on the non-posted request that is fulfilled.

Note: Intel® Matrix Storage Manager AHCI driver does not use the HBA reset command. Linux may enable MSIs and use the HBA reset command. No other third-party software known to utilize MSI interrupts.

Workaround: Prior to performing an HBA reset, software should disable AHCI interrupts by writing a '0' to Interrupt Enable bit (ABAR+04h, bit 1) and then perform a read to the AHCI GHC register (ABAR+04h).

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

20. PET Alerts on SMBus

Problem: When using the ICH8 SMBus for Platform Event Trap (PET) alerts on a system with the Intel® Management Engine (ME) enabled, the SMBus packet headers may be corrupted if all of the following conditions are met:

- SMBus slave is the target of an external PET generating master on SMBus/SMLink
- The ME is in the middle of M0-M1 transitions
- SMBus slave receives back-to-back PET alerts of which some PET alerts are incomplete (i.e. the packet is truncated to less than 6 bytes)

Note: This issue has only been observed under a synthetic test environment.

Implication: Intel® ME firmware may stop functioning, which could cause a system hang.

Workaround: None

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

21. High-speed USB 2.0 V_{HSOH}

Problem: ICH8 High-speed USB 2.0 V_{HSOH} may not meet the USB 2.0 specification.

- The maximum expected V_{HSOH} is 460mV.

Implication: None known.

Workaround: None.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

22. SMBus Host Controller May Hang

Problem: During heavy SMBus traffic utilization, the ICH8 SMBUS host controller may attempt to start a transaction while the bus is busy.

Note: This issue has only been observed under a synthetic test environment.

Implication: May cause the SMBUS host controller to hang.

- After boot:
  - — SMBUS host controller transaction may not complete.
  - — External master transaction in progress targeting ICH8 SMBUS slave may get NACK or timeout.
  - — There is no impact to any other transaction that was in progress by an external master.
- This issue has not been observed during boot as SMBUS utilization tends to be light.

Workaround: BIOS workaround available. See latest BIOS Spec Update for details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes.*

23. SATA Gen1 Initialization/LPM Erratum

Problem: During SATA Initialization routines or while resuming from a Link Power Managed (LPM) state, the ICH8 SATA link to Gen1 (1.5 Gb/s) devices may fail to be established.

Implication: One or more of the following symptoms may occur:

- During Boot or Resume from S4/S5: SATA Gen1 devices may not be detected, resulting in "Operating System Not Found" error.
- During Resume from S3: System may hang when attempting to initialize SATA Gen1 devices.

- During S0: If LPM is enabled and ALL SATA Gen1 devices within the system support LPM, slow SATA Gen1 performance may occur.

Workaround: BIOS workaround available.
Contact your Intel field representative for details.

Status: Desktop: No Fix. Mobile: Plan Fix.
For steppings affected, see the *Summary Tables of Changes.*

24. ICH8M B2 Stepping Gigabit Ethernet Controller RID with CRID Enabled Erratum

Problem: The ICH8M B2 Stepping Gigabit Ethernet Controller (B0:D25:F0) may report an incorrect Revision-ID when Compatibly Revision-ID is enabled.

Implication: The OS image may re-enumerate the Intel ICH8M B2 Gigabit Ethernet Controller when Compatibly Revision-ID is enabled.

- LAN devices affected are Intel® 82566 and Intel® 82562V.

- This may impact customer platforms that are part of Intel® Stable Image Platform Program (Intel® SIPP).
- This issue does not result in functional failures.

Workaround: BIOS workaround available.

Contact your Intel field representative for details.

Status: No Fix. For steppings affected, see the *Summary Tables of Changes*.\

25. Intel® I/O Controller Hub 8 (ICH8) Family PCI Express Function Disable

Problem: Intel® ICH8 Family PCI Express [1:6] Disable bit in Function Disable Register may not put the PCI Express Port into a link down state if a PCI Express Device is attached.

Implication: ICH8M:

PCI Express port [1:6] with a PCI Express device attached may remain in L0 state and DMI may not be able to go into L1 state.

ICH8, ICH8R, ICH8DH, ICH8DO, and ICH8M-E:

PCI Express port [1:6] with a PCI Express device attached may remain in L0 state.

Workaround: A BIOS code change update has been identified.

Status: No Fix. For steppings affected, see the *Summary Table of Changes.*

26. Intel® ICH8 SATA 6.0 Gbps Device Detection

Problem: Intel® ICH8 may not be able to complete SATA Out Of Band (OOB) Signaling with SATA 6.0 Gbps Devices and down shift to SATA 3.0 Gbps speed.

Implication: ICH8 may not detect SATA 6.0 Gbps Devices upon power up or resume from S3, S4 or S5 State.

Workaround: None.

Status: No Plan to Fix.

27. Incorrect IRQ(x) Vector Returned for 8259 Interrupts with RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an incorrect IRQ(x) vector may be returned to the CPU.

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

Specification Changes

1. SPI Specification Addition

Add the following specification to Table 155 of the Datasheet.

I_{LI5}	Input Leakage Current – SPI signals	- 10	+10	µA	

2. USB 2.0 Power Management Description

The following changes apply to Section 5.19.7 of the Datasheet as indicated below.

5.19.7 USB 2.0 Power Management

5.19.7.1 Pause Feature

This feature allows platforms (especially mobile systems) to dynamically enter low-power states during brief periods when the system is idle (i.e., between keystrokes). This is useful for enabling power management features like Intel SpeedStep® technology in the ICH8. The policies for entering these states typically are based on the recent history of system bus activity to incrementally enter deeper power management states. Normally, when the EHC is enabled, it regularly accesses main memory while traversing the DMA schedules looking for work to do; this activity is viewed by the power management software as a non-idle system, thus preventing the power managed states to be entered. Suspending all of the enabled ports can prevent the memory accesses from occurring, but there is an inherent latency overhead with entering and exiting the suspended state on the USB ports that makes this unacceptable for the purpose of dynamic power management. As a result, the EHCI software drivers are allowed to pause the EHC's DMA engines when it knows that the traffic patterns of the attached devices can afford the delay. The pause only prevents the EHC from generating memory accesses; the SOF packets continue to be generated on the USB ports (unlike the suspended state)

5.19.7.2 USB Pre-Fetch Based Pause (Mobile Only)

The Pre-Fetch Based Pause is a power management feature in USB (EHCI) host controllers to ensure maximum C3/C4 CPU power state time with C2 popup. This feature applies to the period schedule and works by allowing the DMA engine to identify periods of idleness and prevents the DMA engine from accessing memory when the periodic schedule is idle. Typically in the presence of periodic devices with multiple millisecond poll periods, the periodic schedule will be idle for several frames between polls.

The USB Pre-Fetch Based Pause feature is disabled by setting bit 4 of EHCI Configuration Register Section 15.1.30

3. Removing Support for USB Wake from S5

Support for USB wake from S5 is removed from the Datasheet as indicated below.

a. Update Intel® ICH8 Features page of the Datasheet as follows:

USB 2.0

—NEW: Up to five UHCI Host Controllers, supporting ten external ports
—NEW: Up to two EHCI Host Controllers that support ten external ports
—NEW: Per-Port-Disable Capability
—NEW: Includes up to two USB 2.0 High-speed Debug Ports
—Supports wake-up from sleeping states S1–S4
—Supports legacy Keyboard/Mouse software

b. Update Table 5-31 as follows:

Table 5-31. Causes of Wake Events

Cause	States Can Wake From	How Enabled
Classic USB	S1–S4	Set USB1_EN, USB 2_EN, USB3_EN, USB4_EN, and USB5_EN, bits in GPE0_EN register

4. Addition of EHCI Parity Error Response

Parity Error Response is supported by the ICH8 Enhanced Host Controller (EHC). The following changes apply to Section 20.1.3 of the EDS and Section 15.1.3 of the Datasheet to reflect the added capability.

8	**SERR# Enable (SERR_EN)** — R/W 0 = Disables EHC's capability to generate an SERR#. 1 = The Enhanced Host Controller (EHC) is capable of generating (internally) SERR# in the following cases: - When it receives a completion status other than "successful" for one of its DMA -initiated memory reads on DMI (and subsequently on its internal interface). - When it detects an address or command parity error and the Parity Error Response bit is set. - When it detects a data parity error (when the data is going into the EHC) and the Parity Error Response bit is set.
6	**Parity Error Response (PER)** — R/W. 0 = The EHC is not checking for correct parity (on its internal interface). 1 = The EHC is checking for correct parity (on its internal interface) and halt operation when bad parity is detected during the data phase. **NOTE:** If the EHC detects bad parity on the address or command phases when the bit is set to 1, the host controller does not take the cycle. It halts the host controller (if currently not halted) and sets the Host System Error bit in the USBSTS register. This applies to both requests and completions from the system interface. This bit must be set in order for the parity errors to generate SERR#.

5. ROAEI options removal for OCW2

Remove bit setting "000" and "100" for Operational Control Word 2 Register bits [7:5] in section 9.4.8.

9.4.8 OCW2—Operational Control Word 2 Register (LPC I/F-D31:F0)

Offset Address:	Master Controller – 020h	Attribute:	WO
	Slave Controller – 0A0h	Size:	8 bits
Default Value:	Bit[4:0]=undefined, Bit[7:5]=001		

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI) —WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = ~~Rotate in Auto EOI Mode (Clear)~~ Reserved 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = ~~Rotate in Auto EOI Mode (Set)~~ Reserved 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used

Specification Clarifications

1. RTC Register A Clarification (Datasheet Only)

Update the description for bits [6:4] in the RTC Register A in Section 9.6.2.1 as follows:

6:4	**Division Chain Select (DV[2:0])** — R/W. These three bits control the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal. DV2 corresponds to bit 6. 010 = Normal Operation 11X = Divider Reset 101 = Bypass 15 stages (test mode only) 100 = Bypass 10 stages (test mode only) 011 = Bypass 5 stages (test mode only) 001 = Invalid 000 = Invalid

2. GLANCLK High Time/Low Time Clarification

The following changes apply to Table 156 of the Datasheet.

tglanhi	High Time	6.4		ns		
tglanlo	Low Time	6.4		ns		

3. USB UHCI Run/Stop Bit Clarification

The following change applies to Section 14.2.1 of the Datasheet.

0	**Run/Stop (RS)** — R/W. When set to 1, the ICH8 proceeds with execution of the schedule. The ICH8 continues execution as long as this bit is set. When this bit is cleared, the ICH8 completes the current transaction on the USB and then halts. The HC Halted bit in the status register indicates when the host controller has finished the transaction and has entered the stopped state. The host controller clears this bit when the following fatal errors occur: consistency check failure, memory access errors. 0 = Stop 1 = Run **NOTE:** This bit should only be cleared if there are no active Transaction Descriptors in the executable schedule or software will reset the host controller prior to setting this bit again.

4. t290 and t294 Clarification

a. Note 23 in Table 173 of the Datasheet is changed as indicated below:

23. t294 applies during S0 to S3/S4/S5 and S0 to G3 transitions. The timing is not applied to V5REF. V5REF timings are bounded by power sequencing.

b. Figure 52 and Figure 53 of the Datasheet is modified to S0 to S3/S4/S5 and G3 Timings.

Document Changes

1. Bit 0 Function Disable Register Correction

The following change applies to bit 0 of the Function Disable register in Section 7.1.71 of the Datahshet.

0	BIOS must set this bit to 1b.

2. PWROK Description Correction

The following change applies to Section 5.13.11.3 of the Datasheet.

The PWROK input should go active no sooner than 99 ms after the core supply voltages become valid. PWROK must not glitch, even if RSMRST# is low.

3. SMBus/SMLink Connectivity Clarification

The following change applies to the 4th paragraph in Section 5.20.1 of the Datasheet.

The ICH8 supports the *System Management Bus (SMBus) Specification,* Version 2.0. Slave functionality, including the Host Notify protocol, is available on the SMBus pins. The SMLink and SMBus signals can be tied together externally depending on the TCO mode used. Refer to Section 5.14.2 for more details.

4. CK_PWRGD Pin State Correction

The state of CK_PWRGD pin during S3 and S4/S5 is changed to ‘Low’ instead of ‘High’ in Table 33 and Table 34 of the Datasheet.

5. SATA Registers Corrections

1. Section 12.2.3.1, 12.2.3.2, 12.2.3.3, 13.2.3.1, 13.2.3.2, and 13.2.3.3 are removed from the Datasheet.
2. The following registers will be added as new sections after both Section 12.3.2 and Section 13.3.2 of the Datasheet.

PxSSTS—Serial ATA Status Register (D31:F2)

Address Offset: Attribute: RO
Default Value: 00000000h Size: 32 bits

SDATA when SINDX.RIDX is 00h. This is a 32-bit register that conveys the current state of the interface and host. The ICH8 updates it continuously and asynchronously. When the ICH8 transmits a COMRESET to the device, this register is updated to its reset values.

Bit	Description
31:12	Reserved

Bit	Description
11:8	**Interface Power Management (IPM)** — RO. Indicates the current interface state: **Value** **Description** 0h Device not present or communication not established 1h Interface in active state 2h Interface in PARTIAL power management state 6h Interface in SLUMBER power management state All other values reserved.
7:4	**Current Interface Speed (SPD)** — RO. Indicates the negotiated interface communication speed. **Value** **Description** 0h Device not present or communication not established 1h Generation 1 communication rate negotiated 2h Generation 2 communication rate negotiated All other values reserved. ICH8 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection (DET)** — RO. Indicates the interface device detection and Phy state: **Value** **Description** 0h No device detected and Phy communication not established 1h Device presence detected but Phy communication not established 3h Device presence detected and Phy communication established 4h Phy in offline mode as a result of the interface being disabled or running in a BIST loopback mode All other values reserved.

PxSCTL — Serial ATA Control Register (D31:F2)

Address Offset: Attribute: R/W, RO
Default Value: 00000004h Size: 32 bits

SDATA when SINDX.RIDX is 01h. This is a 32-bit read-write register by which software controls SATA capabilities. Writes to the SControl register result in an action being taken by the ICH8 or the interface. Reads from the register return the last value written to it.

Bit	Description
31:20	Reserved
19:16	Port Multiplier Port (PMP) — RO. This field is not used by AHCI.
15:12	Select Power Management (SPM) — RO. This field is not used by AHCI.

Bit	Description
11:8	**Interface Power Management Transitions Allowed (IPM)** — R/W. Indicates which power states the ICH8 is allowed to transition to: **Value** **Description** 0h No interface restrictions 1h Transitions to the PARTIAL state disabled 2h Transitions to the SLUMBER state disabled 3h Transitions to both PARTIAL and SLUMBER states disabled All other values reserved
7:4	**Speed Allowed (SPD)** — R/W. Indicates the highest allowable speed of the interface. This speed is limited by the CAP.ISS (ABAR+00h:bit 23:20) field. **Value** **Description** 0h No speed negotiation restrictions 1h Limit speed negotiation to Generation 1 communication rate 2h Limit speed negotiation to Generation 2 communication rate All other values reserved. ICH8 Supports Generation 1 communication rates (1.5 Gb/s) and Gen 2 rates (3.0 Gb/s).
3:0	**Device Detection Initialization (DET)** — R/W. Controls the ICH8's device detection and interface initialization. **Value** **Description** 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications re-initialized 4h Disable the Serial ATA interface and put Phy in offline mode All other values reserved. When this field is written to a 1h, the ICH8 initiates COMRESET and starts the initialization process. When the initialization is complete, this field shall remain 1h until set to another value by software. This field may only be changed to 1h or 4h when PxCMD.ST is 0. Changing this field while the ICH8 is running results in undefined behavior.

PxSERR—Serial ATA Error Register (D31:F2)

Address Offset: Attribute: R/WC
Default Value: 00000000h Size: 32 bits

SDATA when SINDx.RIDX is 02h.

Bits 26:16 of this register contains diagnostic error information for use by diagnostic software in validating correct operation or isolating failure modes. Bits 11:0 contain error information used by host software in determining the appropriate response to the error condition. If one or more of bits 11:8 of this register are set, the controller will stop the current transfer.

Bit	Description
31:27	Reserved

Bit	Description
26	**Exchanged (X)**: When set to one this bit indicates that a change in device presence has been detected since the last time this bit was cleared. This bit shall always be set to 1 anytime a COMINIT signal is received. This bit is reflected in the P0IS.PCS bit.
25	**Unrecognized FIS Type (F)**: Indicates that one or more FISs were received by the Transport layer with good CRC, but had a type field that was not recognized.
24	**Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
23	**Transport state transition error (T)**: Indicates that an error has occurred in the transition from one state to another within the Transport layer since the last time this bit was cleared.
22	**Handshake (H)**: Indicates that one or more R_ERR handshake response was received in response to frame transmission. Such errors may be the result of a CRC error detected by the recipient, a disparity or 8b/10b decoding error, or other error condition leading to a negative handshake on a transmitted frame.
21	**CRC Error (C)**: Indicates that one or more CRC errors occurred with the Link Layer.
20	**Disparity Error (D)**: This field is not used by AHCI.
19	**10b to 8b Decode Error (B)**: Indicates that one or more 10b to 8b decoding errors occurred.
18	**Comm Wake (W)**: Indicates that a Comm Wake signal was detected by the Phy.
17	**Phy Internal Error (I)**: Indicates that the Phy detected some internal error.
16	**PhyRdy Change (N)**: When set to 1 this bit indicates that the internal PhyRdy signal changed state since the last time this bit was cleared. In the ICH8, this bit will be set when PhyRdy changes from a 0 -> 1 or a 1 -> 0. The state of this bit is then reflected in the PxIS.PRCS interrupt status bit and an interrupt will be generated if enabled. Software clears this bit by writing a 1 to it.
15:12	Reserved
11	**Internal Error (E)**: The SATA controller failed due to a master or target abort when attempting to access system memory.
10	**Protocol Error (P)**: A violation of the Serial ATA protocol was detected. Note: The ICH8 does not set this bit for all protocol violations that may occur on the SATA link.
9	**Persistent Communication or Data Integrity Error (C)**: A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.
8	**Transient Data Integrity Error (T)**: A data integrity error occurred that was not recovered by the interface.
7:2	Reserved.
1	**Recovered Communications Error (M)**: Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.
0	**Recovered Data Integrity Error (I)**: A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.

6. SATA Interlock Switch State (ISS) Bit Clarification

The following change applies to Section 12.4.2.7 of the Datasheet.

13	**Interlock Switch State (ISS)**— RO. For systems that support interlock switches (via CAP.SIS [ABAR+00h:bit28]), if an interlock switch exists on this port (via ISP in this register), this bit indicates the current state of the interlock switch. A 0 indicates the switch is closed, and a 1 indicates the switch is opened. For systems that do not support interlock switches (CAP.SIS=0), this bit reports 0.

7. HPET Timer

The following change applies to Section 5.17.1 of the Datasheet.

The main counter is clocked by the 14.31818 MHz clock, synchronized into the 125 MHz domain.

8. Timing Figure Clarification

In Figure 43 of the Datasheet, t216 is removed from the timing figure.

9. GPIO_USE_SEL Override Register Description Correction

The following change applies to Section 9.10.4 of the Datasheet.

Bit	Description
31:0	**GPIO_USE_SEL Override [31:0]** — R/W. Each bit in this register corresponds to one of the GPIO signals (if it exists). 0 = GPIO_USE_SEL register determines the pin usage of native function or GPIO. 1 = Signal is used as native function regardeless of setting in GPIO_USE_SEL register. Once a bit is set to 1b, it can only be cleared by a reset. Bits 31:24 and 15:8 are cleared by RSMRST# and CF9h events. Bits 23:16 and 7:0 are cleared by PLTRST# events. If the corresponding GPIO is not muxed with Native functionality or not implemented at all, this bit has no effect. This register corresponds to GPIO[31:0].

10. Add Ballout AH19(VSS) to Table 147

The following is added to Table 147: Ballout by Signal Name (Mobile Only) of the Datasheet

Ball Name	Ball#
VSS	AH19

11. Correct section 5.13.7.5 Sx-G3-Sx, Handling Power Failures regarding possible wake events following a power failure

Correct section 5.13.7.5 Sx-G3-Sx, Handling Power Failures in the Datasheet.

Section 5.13.7.5 Sx-G3-Sx, Handling Power Failures§

Depending on when the power failure occurs and how the system is designed, different transitions could occur due to a power failure.

The AFTER_G3 bit provides the ability to program whether or not the system should boot once power returns after a power loss event. If the policy is to not boot, the system remains in an S5 state (unless previously in S4). ~~There are only three possible events that will wake the system after a power failure.~~ The following wake events can wake the system following a power loss by either RSMRST# going low and enabling by default, the enable bits reside in the RCT well or the wake event is always enabled.

1. **PWRBTN#:** PWRBTN# is always enabled as a wake event. When RSMRST# is low (G3 state), the PWRBTN_STS bit is reset. When the ICH8 exits G3 after power returns (RSMRST# goes high), the PWRBTN# signal is already high (because VCC-standby goes high before RSMRST# goes high) and the PWRBTN_STS bit is 0.

2. **RI#:** RI# does not have an internal pull-up. Therefore, if this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit is set and the system interprets that as a wake event.

3. **RTC Alarm:** The RTC_EN bit is in the RTC well and is preserved after a power loss. Like PWRBTN_STS the RTC_STS bit is cleared when RSMRST# goes low.

4. **PCI Express Wake# Signal:** The PCIEXPWAK_DIS bit is cleared by RSMRST# going low enabling PCI Express Ports to wake the platform after a power loss. The PCIEXPWAK_STS bit is also cleared when RSMRST# goes low.

5. **PME_B0:** PME_B0_EN is in the RTC Well and is preserved after a power loss. The PME_B0_STS bit is also cleared when RSMRST# goes low.

6. **PME: PME_EN:** is in the RTC Well and is preserved after a power loss. The PME_STS bit is also cleared when RSMRST# goes low.

7. **Host SMBUS:** SMBALERT# or Slave Wake message is always enabled as Wake Event

8. **ME Non-Maskable Wake:** Always enabled as Wake Event.

The ICH8 monitors both PWROK and RSMRST# to detect for power failures. If PWROK goes low, the PWROK_FLR bit is set. If RSMRST# goes low, PWR_FLR is set.

~~***Note:*** Although PME_EN is in the RTC well, this signal cannot wake the system after a power loss. PME_EN is cleared by RTCRST#, and PME_STS is cleared by RSMRST#.~~

12. Correct section 9.1.21 Bits 15:2 definition

Correct section 9.1.21 GEN1_DEC-LPC I/F Generic Decode Range 1 Register in the Datasheet

9.1.21 GEN1_DEC-LPC I/F Generic Decode Range 1 Register (LPC I/F-D31:F0)

Offset Address:84h–87h Attribute: R/W
Default Value:00000000h Size: 32 bit
Power Well: Core

Bit	Description
31:24	Reserved
23:18	**Generic I/O Decode Range Address[7:2] Mask** — R/W. A 1 in any bit position indicates that any value in the corresponding address bit in a received cycle will be treated as a match. The corresponding bit in the Address field, below, is ignored. The mask is only provided for the lower 6 bits of the DWord address, allowing for decoding blocks up to 256 bytes in size.
17:16	Reserved
15:2	**Generic I/O Decode Range 1 Base Address (GEN1_BASE)** — R/W. ~~This address is aligned on a 128-byte boundary, and must have address lines 31:16 as 0.~~ **NOTE:** The ICH Does not provide decode down to the word or byte level.
1	Reserved
0	**Generic Decode Range 1 Enable (GEN1_EN)** — R/W. 0 = Disable. 1 = Enable the GEN1 I/O range to be forwarded to the LPC I/F.

13. Correct Figure 20 and Figure 21 Ballout information

Correct the Ball Names in Figure 20 and Figure 21 Ballout (Mobile Only) in the Datasheet with the Ball Names listed below for the following Ball Numbers.

Ball#	Change Ball Name to:
AG29	CPUPWRGD/GPIO49
C22	LAN_RXD2
C23	SPI_CLK
AJ6	VccSATAPLL
AJ26	SMBCLK
D5	VCC3_3
W23	VCC1_5_A
AJ10	SATA1GP/GPIO19
AH10	VSS

14. Correct section 11.1.43 bit 0 definition

Correct section 11.1.43 CIR5 - Chipset Initialization Register 5 in the EDS and Datasheet

11.1.43 CIR5—Chipset Initialization Register 5

Offset Address: 1D40h–1D47h Attribute: R/W, R/WL
Default Value: 0000000000000000h Size: 64-bit

Bit	Description
63:~~1~~0	Reserved
~~0~~	~~CIR5 Field 1 - R/W. BIOS must program this field to 1b.~~

15. Correct A20M# Signal Description

Correct A20M# signal description in Table 2-12: Processor Interface Signals in the ICH8 Datasheet.

Name	Type	Description
A20M#	O	**Mask A20:** A20M# will go ~~active~~ inactive based on either setting the appropriate bit in the Port 92h register, or based on the A20GATE input being active.

16. Update Section 8.2 in the Datasheet

The title of section 8.2 of the ICH8 Datasheet is changed as below.

8.2 Absolute Maximum and Minimum Ratings

The following paragraphs are added to section 8.2:

Table 8-1 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the ICH8 contains protective circuitry to resist damage from Electro - Static Discharge (ESD), precautions should always be taken to avoid high static coltages or electric fields.

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