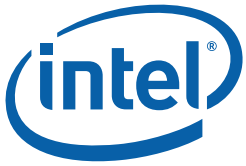

Intel® 965 Express Chipset Family

Specification Update

- For the Intel® 82Q965, 82Q963, 82G965 Graphics and Memory Controller Hub (GMCH) and Intel® 82P965 Memory Controller Hub (MCH)

September 2006

Document Number: 313054-003

Contents

Revision History

Rev.	Draft/Changes	Date
-001	• Initial Release	June 2006
-002	• Added 82Q965, 82G965, and 82Q963 GMCH components. • Added Errata 3 and 4.	July 2006
-003	• Added Errata 5 and 6. • Added document changes 1 – 4.	September 2006

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Note: Unless otherwise specified, the information in this document applies to the Intel® 82Q965 Graphics and Memory Controller Hub (GMCH), Intel® 82Q963 Graphics and Memory Controller Hub (GMCH), Intel® 82G965 Graphics and Memory Controller Hub (GMCH), and Intel® 82P965 Memory Controller Hub (MCH).

Note: The term (G)MCH refers to the 82Q965/82Q963/82G965 GMCH and 82P965 MCH.

Affected Documents

Affected Documents/Related Documents

Document Title	Document Number
Intel® 965 Express Chipset Family Datasheet	313053

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the Intel 82Q965 GMCH, 82Q963 GMCH, 82G965 GMCH and 82P965 MCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

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Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Erratum, Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank Box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

Doc:	Document change or update that will be implemented.
PlanFix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.

Row

Shaded:	This item is either new or modified from the previous version of the document.

NO.	C1	C2	PLANS	ERRATA
1	X		Fixed	MCH ME ROM Initialization Hang
2	X		Fixed	P965 Express Chipset Platforms Intermittently Lockup after Start\Shutdown initiated from OS or from Power Button.
3	X	X	NoFix	The SRID (Stepping Revision ID) for the (G)MCH-C2 is the Same as (G)MCH-C1
4	X	X	NoFix	Data Recovery Clock (DRC) Lock-Up
5	X	X	NoFix	VGA Engine Hangs with Upper-left Centering Mode
6	X	X	Doc	ME Warm Reset Hang

NO.	SPECIFICATION CHANGES
	There are no specification changes.

NO.	SPECIFICATION CLARIFICATIONS
	There are no specification clarifications.

NO.	DOCUMENTATION CHANGES
1	Feature page graphics core frequency and pixel rate
2	System memory bandwidth reference
3	DX support feature correction
4	Graphics to memory bandwidth correction

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Identification Information

Component Identification via Programming Interface

The Intel 82Q965 GMCH, 82Q963 GMCH, 82G965 GMCH and 82P965 MCH may be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Revision Number[3]
C1	8086h	82P965 = 29A0h	02h
C2	8086	82Q963 = 2990h	02h
		82Q965 = 2990h	02h
		82G965 = 29A0h	02h
		82P965 = 29A0h	02h

NOTES:
1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 82Q965 GMCH, 82Q963 GMCH, 82G965 GMCH and 82P965 MCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
C1	82P965 MCH	SL9NU	LE82P965	Production – pb free
C2	82Q963 GMCH	SL9R2	LE82Q963	Production – pb free
C2	82Q965 GMCH	SL9QZ	LE82Q965	Production – pb free
C2	82G965 GMCH	SL9R5	LE82G965	Production – pb free
C2	82P965 MCH	SL9NU	LE82P965	Production – pb free

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Errata

1. MCH ME ROM Initialization Hang

Problem: The C-0 MCH internal ROM programming causes two ICH8 B-0 logic devices to have conflicting resource base addresses preventing LAN initialization.

Implication: The system may not boot if the Intel® ICH8 internal LAN is enabled.

Workaround: An updated MCH ROM Programming sequence is available through a firmware update on the engineering portal of ARMS.

Use firmware build Beta 2.0.0.1067 (under Kit #9050) or greater for platforms supporting ME (Intel® Active Management Technology (Intel® AMT), ASF and Intel® Quiet System Technology (Intel® QST)).

Use firmware build version 2.0.0.1061 (ARMs->Product Documentation & Other Software->Test Software-> “Build 1061 (no ME)”) for platforms NOT supporting ME (Intel AMT, ASF Intel QST)

Notes: Exact steps for implementing workaround depend upon method of building SPI image. See release notes for details.

This workaround only required for pre-production systems; work around should be backed out for production systems.

Status: PlanFix. For affected steppings, see the *Summary Table of Changes*.

2. P965 Express Chipset Platforms Intermittently Lockup after Start\Shutdown initiated from OS or from Power Button

Problem: When powering down to/from S0 to S3, S4, or S5 a P965 Express chipset-based platform with an enabled Integrated Graphics Device or PCI Express* Device from either DOS or the Microsoft Windows* Operating System, the system may hang if the power button or Start/Shutdown option is utilized.

Implication: Powering cycling a platform from S0 to S3, S4 or S5 may cause the system to hang.

Workaround: Under Investigation.

Status: PlanFix. For affected steppings, see the *Summary Table of Changes*.

3. The SRID (Stepping Revision ID) for (G)MCH-C2 is the Same as (G)MCH-C1

Problem: A (G)MCH-C2 part outside of the topside marking will look the same to the system BIOS as a (G)MCH-C1 part.

Implication: Customers have no method for telling (G)MCH-C2 from (G)MCH-C1.

Workaround: B/F/D 0/0/0 offset 0xE4 bit [3]

if = 1: Stepping = C2

if = 0: Stepping = C1.

Download latest Graphics Driver (14.21.4598 and above) for proper overlay operation with (G)MCH-C2. Contact your Intel representative for the latest BIOS information.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

4. Data Recovery Clock (DRC) Lock-Up

Problem: If the S1 ACPI state is enabled on the Intel® 965 Express chipset family and L1 PCI Express* Link Power Management is supported by a PCI Express*card inserted into the x16 PCI Express* port, the system may on rare occasions experience abnormal system behavior upon resuming from S1.

Implication: On rare occasions when performing S1 ACPI stress test cycling on an Intel® 965 Express chipset platform, the system may experience abnormal behavior such as correctable bit errors, system hang, or a blank screen.

Workaround: Disable S1 support via BIOS.

or

Ensure L1 PCI Express* link power management is not supported by an external PCI Express* card.

Status: NoFix. For affected steppings, see the *Summary Table of Changes*.

5. VGA Engine Hangs with Upper-left Centering Mode

Problem: On an Intel® Q96x/G965 based platform, when launching some legacy 2D DOS applications that use non-standard VGA programming on a monitor that requires panel fitting/scaling using upper-left centering mode abnormal system behavior is observed.

Notes:

Non-standard programming refers to applications that program the VGA timing registers in a manner that the “vertical display enable end” value is greater than the “vertical blank start” value.

- The “vertical display enable end” value specifies the number of scan lines that form the vertical active display area. This is the value programmed in VGA registers CR12 bits 7 through 0 and CR07 bits 6 and 1.
- The “vertical blank start” specifies the beginning of the vertical blanking period relative to the beginning of the active display area of the screen. This is the value programmed in VGA registers CR12 bits 7 through 0, CR09 bit 5, and CR07 bit 3.

Implication: The display monitor may blank screen and the system hang. Note: Native VGA mode on CRT’s or Flat Panels operates as intended.

Workaround: None

Status: NoFix For affected steppings, see the Summary Table of Changes.

6. ME Warm Reset Hang

Problem: If the default setting for the “Minimum Power-down exit to Non-Read command spacing” (sd0_cr_txp in register MCHBAR 0x260[13:10]) is programmed, Intel® Q96x, G965 and P965 Express Chipset family based platforms will violate the JEDEC tXSNR timing specification during self refresh exit when Intel® Management Engine is enabled.

Implication: Depending on DIMM sensitivity to tXSNR timing violations, on rare occasions the system may experience abnormal system behavior upon resuming from warm resets and ACPI S3 state when Intel® Management Engine is enabled for Intel® Active Management Technology, Intel® Quiet System Technology, or Alert Standard Format (ASF).

Workaround: BIOS workaround - See latest Broadwater Chipset BIOS Specification and Updates.

Status: Doc. For affected steppings, see the *Summary Table of Changes*.

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Specification Changes

There are no Specification Changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

1. Feature page graphics core frequency and pixel rate

On page 17 of the Intel® 965 Express Chipset Family Datasheet the Integrated Graphics Device sub bullet will be updated with the correct graphics core frequency and pixel rate as shown below.

-Core frequency of 667MHz
-1.33Gp/s pixel rate

2. System memory bandwidth reference

Section 10.5 on page 348 of the Intel® 965 Express Chipset Family Datasheet will be updated with the correct memory bandwidth access rate of 12.8GB/s.

3. DX support feature correction

In Section 10.5.1.1 on page 348 of the Intel® 965 Express Chipset Family Datasheet the first paragraph is to be updated to show support for only DX9.0c

4. Graphics to memory bandwidth correction

In Section 10.5.1.1 on page 349 of the Intel® 965 Express Chipset Family Datasheet the last paragraph of the section will be updated as follows.

Memory bandwidth is very critical to 3D graphics performance. The 82Q9965, 82Q963, and 82G965 GMCH graphic's capability addresses this potential issue by sharing the two channels of memory bandwidth that allows for up to 12.8GB/s.

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