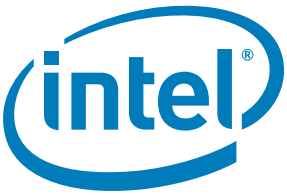

Dual-Core Intel® Xeon® Processor 5000 Series

Thermal/Mechanical Design Guidelines

May 2006

Document Number: 313062-002

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Contents

Figures

Tables

Revision History

Revision	Description	Date
001	Initial Release of this document	June 2006
002	Updated Enabled Supplier Information	June 2006

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1 Introduction

1.1 Objective

To describe the reference thermal solution and design parameters required for the Dual-Core Intel® Xeon® Processor 5000 Series. It is also the intent of this document to comprehend and demonstrate the processor cooling solution features and requirements. Furthermore, this document provides an understanding of the processor thermal characteristics, and discusses guidelines for meeting the thermal requirements imposed on the entire life of the processor. The thermal/mechanical solutions described in this document are intended to aid component and system designers in the development and evaluation of processor compatible thermal/mechanical solutions.

1.2 Scope

The thermal/mechanical solutions described in this document pertain only to a solution(s) intended for use with the Dual-Core Intel Xeon Processor 5000 Series in 1U, 2U, 2U+ and workstation form factor systems. This document contains the mechanical and thermal requirements of the processor cooling solution. In case of conflict, the data in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* supersedes any data in this document. Additional information is provided as a reference in the appendices.

1.3 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

Document	Comment
European Blue Angel Recycling Standards	http://www.blauer-engel.de
Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide	See Note at bottom table.
LGA771 Socket Mechanical Design Guide	See Note following table.
Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications	See Note following table.
Dual-Core Intel® Xeon® Processor 5000 Sequence Common Enabling Kit and Package Mechanical Models (in IGES and ProE* format)	Available electronically
Dual-Core Intel® Xeon® Processor 5000 Sequence Common Enabling Kit Thermal Models (in Flotherm* and Icepak*)	Available electronically
Dual-Core Intel® Xeon® Processor 5000 Sequence Package Thermal Models (in Flotherm* and Icepak*)	Available electronically
Cedar Mill Processor Family BIOS Writer's Guide (BWG)	See Note following table.
Thin Electronics Bay Specification (A Server System Infrastructure (SSI) Specification for Rack Optimized Servers	www.ssiforum.com
4-Wire Pulse Width Modulation (PWM) Controlled Fans Specification	www.Formfactors.org

Note: Contact your Intel field sales representative for the latest revision and order number of this document.

1.4 Definition of Terms

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
FMB	Flexible Motherboard Guideline: an estimate of the maximum value of a processor specification over certain time periods. System designers should meet the FMB values to ensure their systems are compatible with future processor releases.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
LGA771 Socket	The Dual-Core Intel Xeon Processor 5000 Series interfaces to the baseboard through this surface mount, 771 Land socket. See the *LGA771 Socket Mechanical Design Guide* for details regarding this socket.
P_{MAX}	The maximum power dissipated by a semiconductor component.
Ψ_{CA}	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA})$ / Total Package Power. Heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S)$ / Total Package Power.
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA})$ / Total Package Power.
T_{CASE}	The case temperature of the processor, measured at the geometric center of the topside of the IHS.
T_{CASE_MAX}	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation when the die temperature is very near its operating limits.
$T_{CONTROL}$	A processor unique value for use in fan speed control mechanisms. $T_{CONTROL}$ is a temperature specification based on a temperature reading from the processor's thermal diode. $T_{CONTROL}$ can be described as a trigger point for fan speed control implementation. $T_{CONTROL}$ = Tcontrol_Base + Tcontrol_Offset.
Tcontrol_Offset	An offset value from the Tcontrol_Base value specified in the processor EMTS or data sheet. This value is programmed into each processor during manufacturing and can be obtained by reading the IA_32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to the *Cedar Mill Processor Family BIOS Writer's Guide* for further details.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Diode Correction Factor	A processor unique value, which defines the error correction that is to be applied to all thermal diode readings. Thermal Diode Correction Factor = Thermal Diode_Base + Thermal Diode_Offset.
Thermal Diode_Offset	A signed (+/-) offset value from the Thermal Diode_Base value specified in the processor EMTS or data sheet. This value is programmed into each processor during manufacturing and can be obtained by reading the IA_32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to the *Cedar Mill Processor Family BIOS Writer's Guide* for further details.
Thermal Monitor	A feature on the processor that can keep the processor's die temperature within factory specifications under normal operating conditions, and with a thermal solution that satisfies the processor thermal profile specification.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.

Table 1-2. Terms and Descriptions (Sheet 2 of 2)

T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so on.

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2 Thermal/Mechanical Reference Design

This chapter describes the thermal/mechanical reference design for the Dual-Core Intel Xeon Processor 5000 Series. The Dual-Core Intel Xeon Processor 5080 is the performance processor with a front side bus speed of 1066 MHz, while the Dual-Core Intel Xeon Processor 5050 is the value processor with a front side bus speed of 667 MHz. Both processors are targeted for the full range of form factors (2U, 2U+ and 1U/ volumetrically constrained). The Dual-Core Intel Xeon Processor 5063 (MV) is targeted primarily at the 1U or volumetrically constrained form factors.

2.1 Mechanical Requirements

The mechanical performance of the processor cooling solution must satisfy the requirements described in this section.

2.1.1 Processor Mechanical Parameters

Table 2-1. Processor Mechanical Parameters Table

Parameter	Minimum	Maximum	Unit	Notes
Volumetric Requirements and Keepouts				1
Static Compressive Load				3
Static Board Deflection				3
Dynamic Compressive Load				3
Transient Bend				3
Shear Load		70 311	lbf N	2,4,5
Tensile Load		25 111	lbf N	2,4,6
Torsion Load		35 3.95	in*lbf N*m	2,4,7

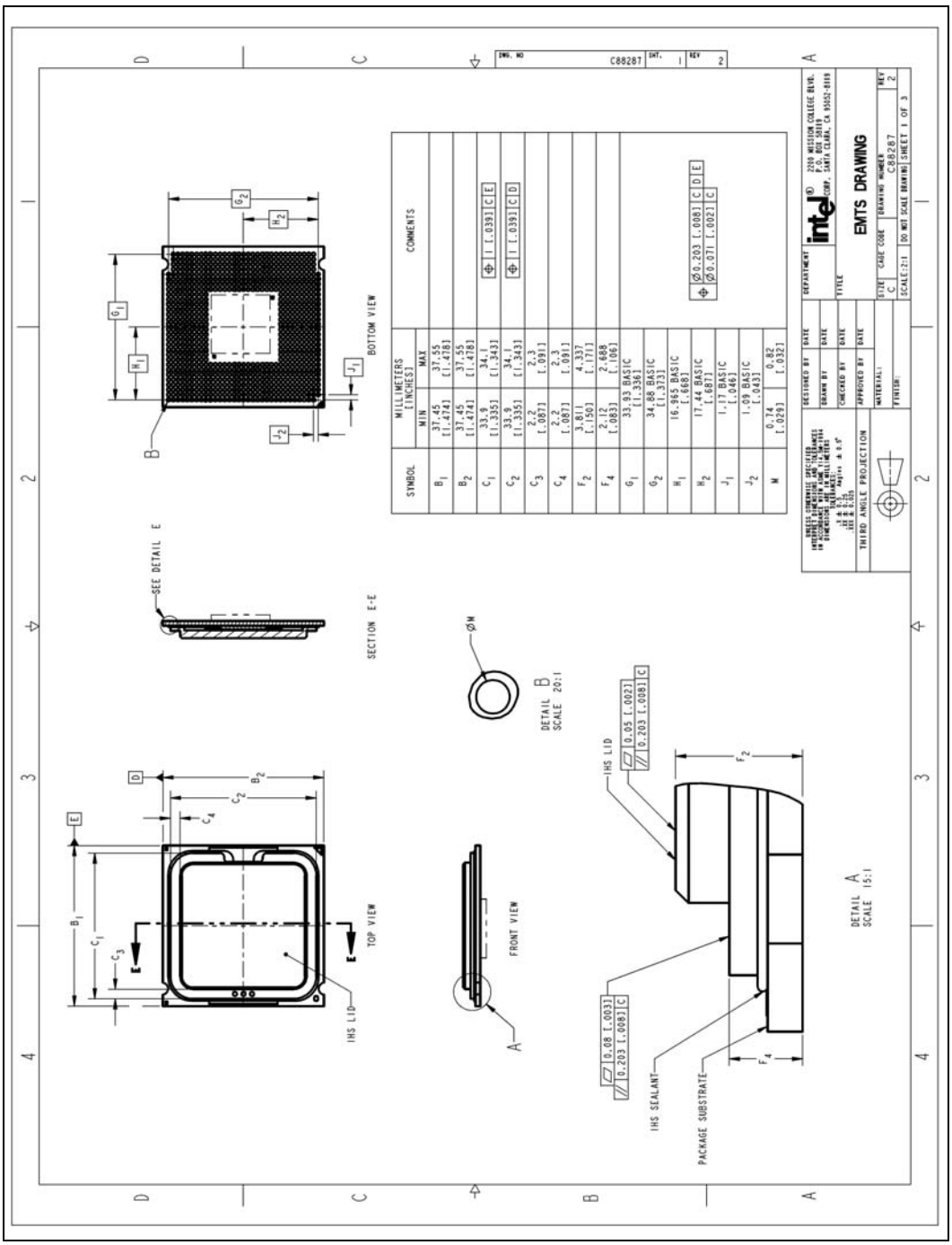
Notes:
1. Refer to drawings in Appendix A.
2. In the case of a discrepancy, the most recent *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* and *LGA771 Socket Mechanical Design Guide* supersede targets listed in Table 2-1 above.
3. These socket limits are defined in the *LGA771 Socket Mechanical Design Guide*.
4. These package handling limits are defined in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications.*
5. Shear load that can be applied to the package IHS.
6. Tensile load that can be applied to the package IHS.
7. Torque that can be applied to the package IHS.

2.1.2 Dual-Core Intel® Xeon® Processor 5000 Series Package

The Dual-Core Intel Xeon Processor 5000 Series is packaged using the flip-chip land grid array (FC-LGA6) package technology. Please refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for detailed mechanical specifications. The Dual-Core Intel Xeon Processor 5000 Series Mechanical

drawing, Figure 2-1, provides the mechanical information for the Dual-Core Intel Xeon Processor 5000 Series. The stack up height of the processor in the socket is shown in Appendix A. The drawing is superseded with the drawing in the processor EMTS, should there be any conflicts. Integrated package/socket stack-up height information is provided in the *LGA771 Socket Mechanical Design Guide*.

Figure 2-1. Dual-Core Intel® Xeon® Processor 5000 Series Mechanical Drawing



The package includes an integrated heat spreader (IHS). The IHS transfers the non-uniform heat from the die to the top of the IHS, out of which the heat flux is more uniform and spreads over a larger surface area (not the entire IHS area). This allows more efficient heat transfer out of the package to an attached cooling device. The IHS is designed to be the interface for contacting a heatsink. Details can be found in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications*.

The processor connects to the baseboard through a 771-land surface mount socket. A description of the socket can be found in the *LGA771 Socket Mechanical Design Guide*.

The processor package and socket have mechanical load limits that are specified in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* and the *LGA771 Socket Mechanical Design Guide.* These load limits should not be exceeded during heatsink installation, removal, mechanical stress testing, or standard shipping conditions. For example, when a compressive static load is necessary to ensure thermal performance of the Thermal Interface Material (TIM) between the heatsink base and the IHS, it should not exceed the corresponding specification given in the *LGA771 Socket Mechanical Design Guide*.

The heatsink mass can also add additional dynamic compressive load to the package during a mechanical shock event. Amplification factors due to the impact force during shock must be taken into account in dynamic load calculations. The total combination of dynamic and static compressive load should not then exceed the processor/socket compressive dynamic load specified in the *LGA771 Socket Mechanical Design Guide* during a vertical shock. It is not recommended to use any portion of the processor substrate as a mechanical reference or load- bearing surface in either static or dynamic compressive load conditions.

2.1.3 Dual-Core Intel® Xeon® Processor 5000 Series Considerations

An attachment mechanism must be designed to support the heatsink since there are no features on the LGA771 socket to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially ones based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Refer to Section 2.4.2 and Section 2.4.7.2 for information on tradeoffs made with TIM selection. Designs should consider possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attach mechanism. Their design should provide a means for protecting LGA771 socket solder joints as well as preventing package pullout from the socket.

Note: The load applied by the attachment mechanism must comply with the package and socket specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as identified in Section 2.1.1.

A potential mechanical solution for heavy heatsinks is the direct attachment of the heatsink to the chassis pan. In this case, the strength of the chassis pan can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

The Intel reference design for the Dual-Core Intel Xeon Processor 5000 Series is using such a heatsink attachment scheme. Refer to Section 2.4 for further information regarding the Intel reference mechanical solution.

2.2 Processor Thermal Parameters and Features

2.2.1 Thermal Control Circuit and TDP

The operating thermal limits of the processor are defined by the Thermal Profile. The intent of the Thermal Profile specification is to support acoustic noise reduction through fan speed control and ensure the long-term reliability of the processor. This specification requires that the temperature at the center of the processor IHS, known as (T_{CASE}) remains within a certain temperature specification. Compliance with the T_{CASE} specification is required to achieve optimal operation and long-term reliability (See the *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide* for Case Temperature definition and measurement methods).

To ease the burden on thermal solutions, the Thermal Monitor feature and associated logic have been integrated into the silicon of the processor. One feature of the Thermal Monitor is the Thermal Control Circuit (TCC). When active, the TCC lowers the processor temperature by reducing the power consumed by the processor. This is done by changing the duty cycle of the internal processor clocks, resulting in a lower effective frequency. When active, the TCC turns the processor clocks off and then back on with a predetermined duty cycle.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by the thermal profile) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime, and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, the case temperature, or the thermal diode temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, PROCHOT#, or Tdiode on random processor samples.

By taking advantage of the Thermal Monitor features, system designers may reduce thermal solution cost by designing to the Thermal Design Power (TDP) instead of maximum power. TDP should be used for processor thermal solution design targets. TDP is not the maximum power that the processor can dissipate. TDP is based on measurements of processor power consumption while running various high power applications. This data set is used to determine those applications that are interesting from a power perspective. These applications are then evaluated in a controlled thermal environment to determine their sensitivity to activation of the thermal control circuit. This data set is then used to derive the TDP targets published in the processor EMTS. The Thermal Monitor can protect the processor in rare workload excursions above TDP. Therefore, thermal solutions should be designed to dissipate this target power level. The thermal management logic and thermal monitor features are discussed in extensive detail in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications*.

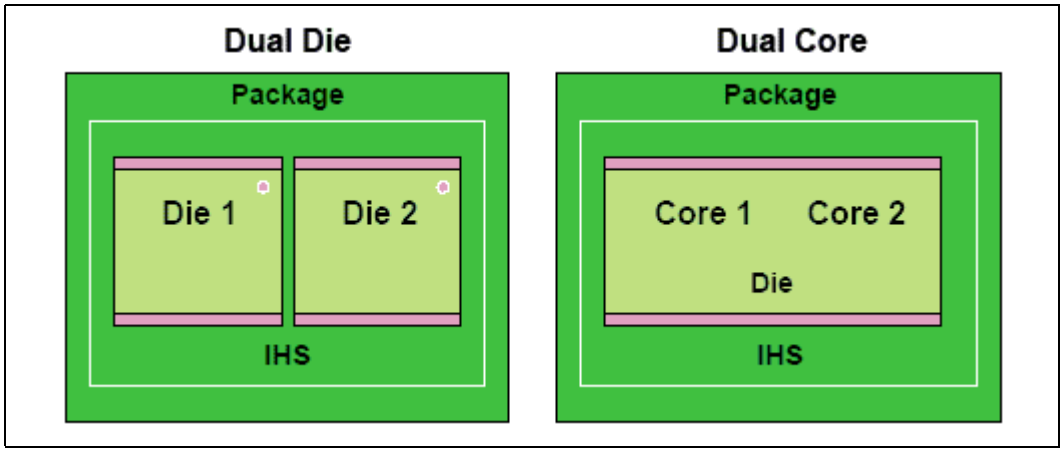
In addition, on-die thermal management features called THERMTRIP# and FORCEPR# are available on the Dual-Core Intel Xeon Processor 5000 Series processors. They provide a thermal management approach to support the continued increases in processor frequency and performance. Please see the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for guidance on these thermal management features.

2.2.2 Dual-Die Special Considerations

2.2.2.1 Thermal Monitor for Dual-Die and Dual-Core Products

The thermal management for dual-die and dual-core products do not change from previous generations. There will still be only one $T_{CONTROL}$ value, and if either diode temperature is greater than or equal to $T_{CONTROL}$, the processor case temperature must remain at or below the temperature as specified by the thermal profile. See Section 2.4 for information on $T_{CONTROL}$. See Figure 2-2 for a visual depiction of the difference between dual-die and dual-core processors. The Dual-Core Intel Xeon Processor 5000 Series is dual-die, utilizing two physical Intel NetBurst® microarchitecture dies in one package.

Figure 2-2. Dual-Core versus Dual-Die



Note: Figure is not to scale – for illustration only.

2.2.2.2 Fan Speed Control for the Dual-Die Dual-Core Intel® Xeon® Processor 5000 Series

For the dual-die Dual-Core Intel Xeon Processor 5000 Series, there are two additional pins on the LGA771 socket for the second thermal diode: THERMDA2 and THERMDC2. The platform hardware and corresponding software will have to be modified to accommodate the new signal pin. Figure 2-3 provides an illustration of the fan speed signals for the dual-die Dual-Core Intel Xeon Processor 5000 Series.

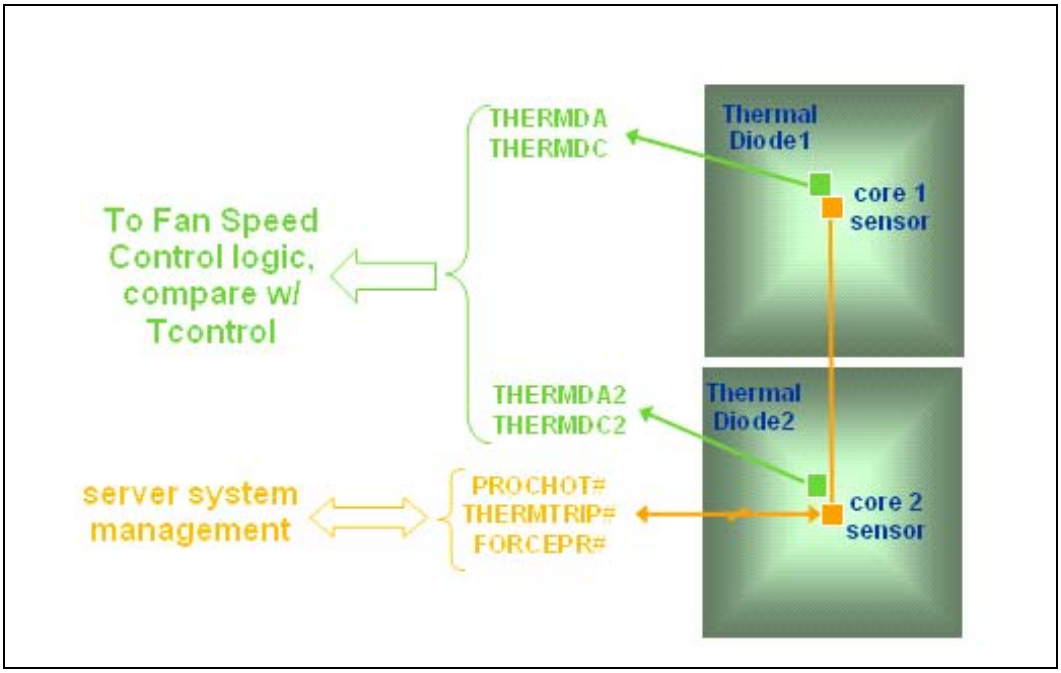


Figure 2-3. Fan Speed Control for Dual-Die Dual-Core Intel® Xeon® Processor 5000 Series

2.2.2.3 PROCHOT#, THERMTRIP#, and FORCEPR#

The PROCHOT# and THERMTRIP# outputs will be shared by each die. The first die to reach TCC activation will assert PROCHOT#. A single FORCEPR# input will be shared by each core. Table 2-2 provides an overview of input and output conditions for the dual-die Dual-Core Intel Xeon Processor 5000 Series thermal management features.

Table 2-2. Input and Output Conditions for the Dual-Die Dual-Core Intel® Xeon® Processor 5000 Series Thermal Management Features

Item	Input		Output	
	Core1	Core2	Core1	Core2
TM1	TCC Activation		TCC Activation	
		TCC Activation		TCC Activation
	TCC Activation	TCC Activation	TCC Activation	TCC Activation
PROCHOT#	TCC Activation		PROCHOT# Asserted	
		TCC Activation		
	TCC Activation	TCC Activation		
THERMTRIP#	THERMTRIP # reached		THERMTRIP# Asserted, both cores shut down	
		THERMTRIP # reached		
	THERMTRIP # reached	THERMTRIP # reached		
FORCEPR#	FORCEPR# Asserted		TCC Activation	TCC Activation

Note: For more information on PROCHOT#, THERMTRIP#, and FORCEPR# see the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications*.

2.2.2.4 Heatpipe Orientation for Multiple Core Processors

Thermal management of multiple core processors can be achieved without the use of heatpipe heatsinks, as demonstrated by the Intel Reference Thermal Solution discussed in Section 2.4.

To assist customers interested in designing heatpipe heatsinks, processor core locations have been provided. In some cases, this may influence the designer's selection of heatpipe orientation. For this purpose, the core geometric center locations, as illustrated in Figure 2-4, are provided in Table 2-3. Dimensions originate from the vertical edge of the IHS nearest to the pin 1 fiducial as shown in Figure 2-4.

Figure 2-4. Processor Core Geometric Center Locations

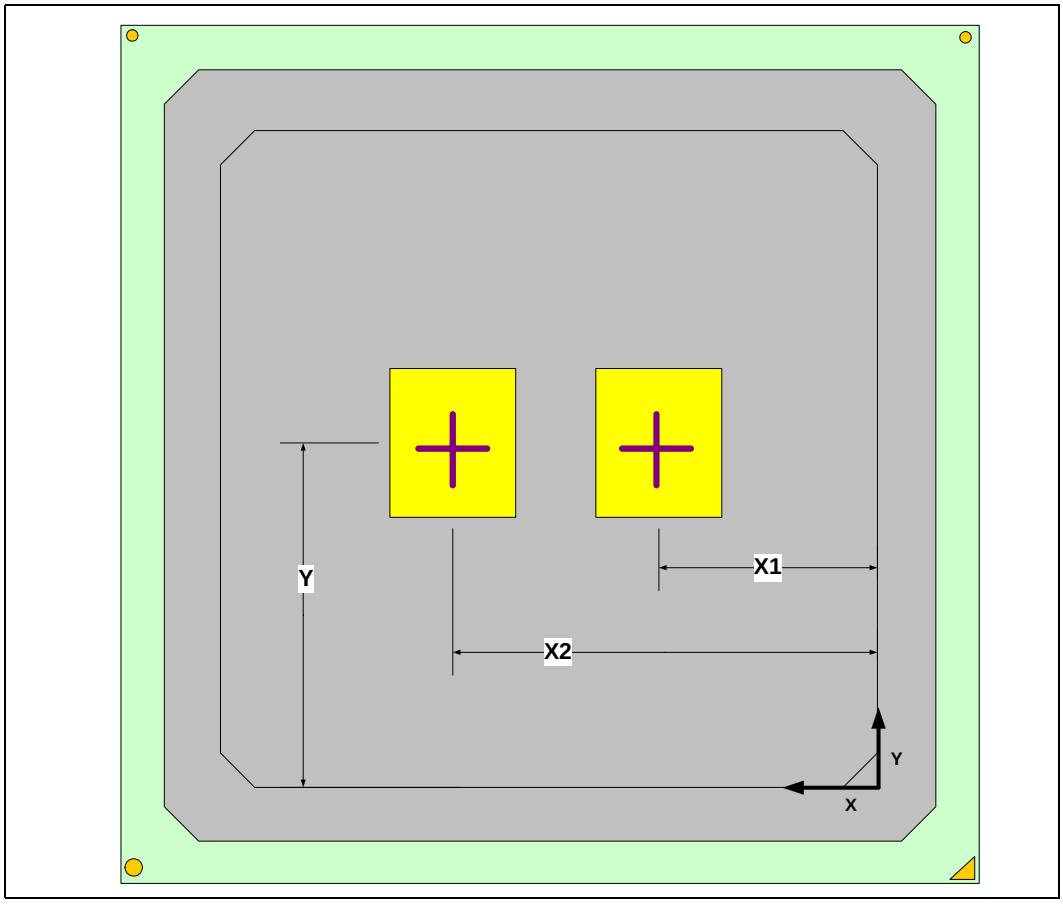


Table 2-3. Processor Core Geometric Center Dimensions

Feature	X Dimension	Y Dimension
Core 1	9.70 mm	14.75 mm
Core 2	19.80 mm	14.75 mm

2.2.3 Thermal Profile

The thermal profile is a linear line that defines the relationship between a processor's case temperature and its power consumption as shown in Figure 2-5. The equation of the thermal profile is defined as:

Equation 2-1.y = ax + b

Where:

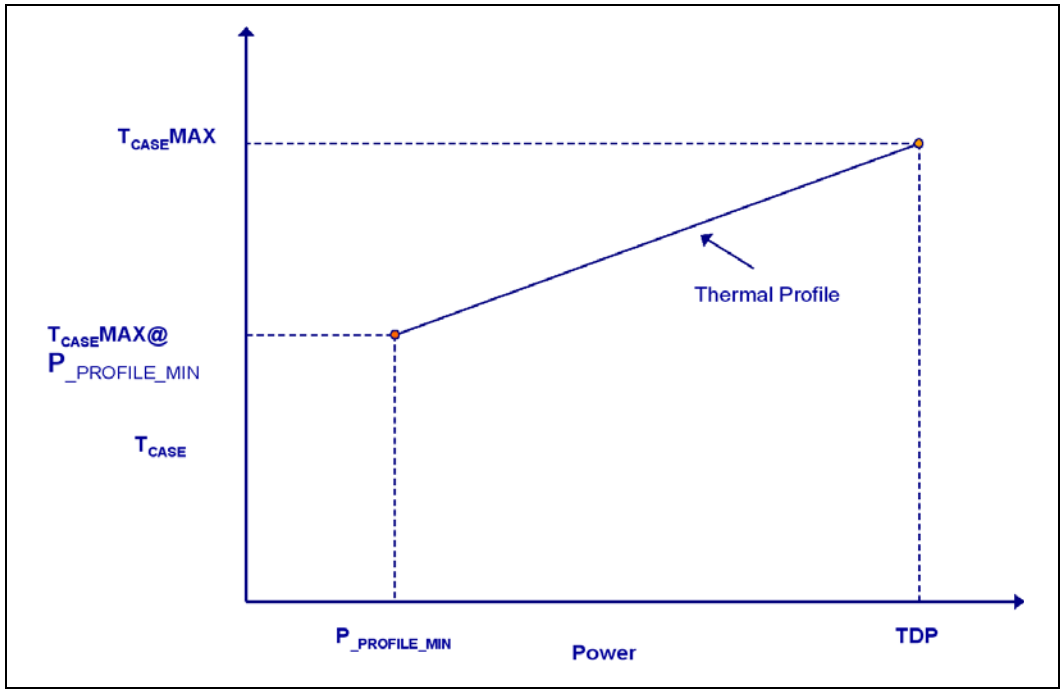
y=Processor case temperature, TCASE (°C)

x=Processor power consumption (W)

a=Case-to-ambient thermal resistance, YCA (°C/W)

b=Processor local ambient temperature, TLA (°C)

Figure 2-5. Thermal Profile Diagram



The higher end point of the Thermal Profile represents the processor's TDP and the associated maximum case temperature (T_{CASE}MAX). The lower end point of the Thermal Profile represents the power value ($P_{\_PROFILE\_MIN}$) and the associated case temperature (T_{CASE}MAX@ $P_{\_PROFILE\_MIN}$) for the lowest possible theoretical value of $T_{CONTROL}$ (see Section 2.2.4). The slope of the Thermal Profile line represents the case-to-ambient resistance of the thermal solution with the y-intercept being the local processor ambient temperature. The slope of the Thermal Profile is constant between $P_{\_PROFILE\_MIN}$ and TDP, which indicates that all frequencies of a processor defined by the Thermal Profile will require the same heatsink case-to-ambient resistance.

In order to satisfy the Thermal Profile specification, a thermal solution must be at or below the Thermal Profile line for the given processor when its diode temperature is greater than $T_{CONTROL}$ (refer to Section 2.2.4). The Thermal Profile allows the customers to make a trade-off between the thermal solution case-to-ambient resistance and the processor local ambient temperature that best suits their platform implementation (refer to Section 2.3.4). There can be multiple combinations of thermal solution case-to-ambient resistance and processor local ambient temperature that can

meet a given Thermal Profile. If the case-to-ambient resistance and the local ambient temperature are known for a specific thermal solution, the Thermal Profile of that solution can easily be plotted against the Thermal Profile specification. As explained above, the case-to-ambient resistance represents the slope of the line and the processor local ambient temperature represents the y-axis intercept. Hence the T_{CASE} values of a specific solution can be calculated at the TDP and $P_{\_PROFILE\_MIN}$ power levels. Once these points are determined, they can be joined by a line, which represents the Thermal Profile of the specific solution. If that line stays at or below the Thermal Profile specification, then that particular solution is deemed as a compliant solution.

2.2.4 $T_{CONTROL}$ Definition

$T_{CONTROL}$ is a temperature specification based on a temperature reading from the processor's thermal diode. $T_{CONTROL}$ can be described as a trigger point for fan speed control implementation. The value for $T_{CONTROL}$ is calibrated in manufacturing and configured for each processor individually. For the Dual-Core Intel Xeon Processor 5000 Series, the $T_{CONTROL}$ value is obtained by reading a processor model specific register (MSR) and adding this offset value to a base value. The equation for calculating $T_{CONTROL}$ is:

Equation 2-2. $T_{CONTROL} = T_{CONTROL\_BASE} + T_{CONTROL\_OFFSET}$

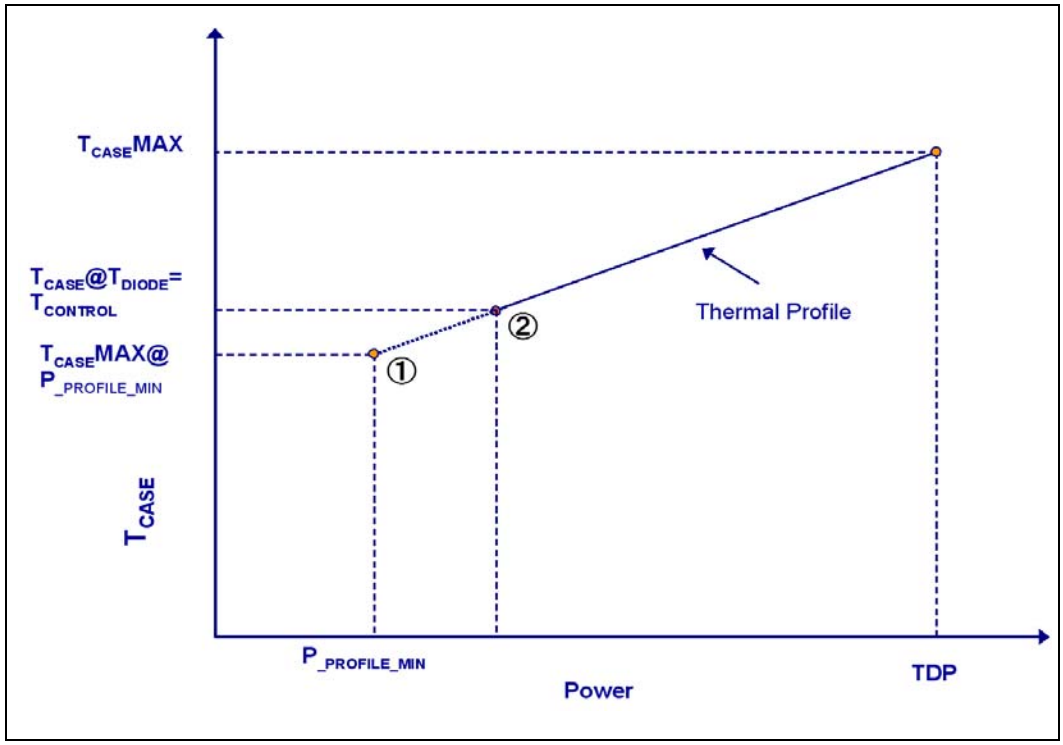
Where:

$T_{CONTROL\_BASE}$ = A fixed base value defined for a given processor generation as published in the processor EMTS.

$T_{CONTROL\_OFFSET}$ = A value programmed into each processor during manufacturing that can be obtained by reading the IA32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to the *Cedar Mill Processor Family BIOS Writer's Guide (BWG)* for further details.

The $T_{CONTROL\_BASE}$ value for the Dual-Core Intel Xeon Processor 5000 Series is 60°C. The Offset value, which is also a diode-based value, depends on several factors (for example, leakage current). The Offset value can be any number between 0 and Tdiode@T_{CASE}MAX - $T_{CONTROL\_BASE}$. Figure 2-6 depicts the interaction between the Thermal Profile and $T_{CONTROL}$.

Figure 2-6. $T_{CONTROL}$ and Thermal Profile Interaction



Since $T_{CONTROL}$ is based on a processor diode temperature value, an equivalent T_{CASE} temperature must be determined to plot the T_{CASE} MAX @ $T_{CONTROL}$ point on the Thermal Profile graph. Location 1 on the Thermal Profile represents a T_{CASE} value corresponding to $P_{\_PROFILE\_MIN}$. Location 2 on the Thermal Profile represents a T_{CASE} value corresponding to Tdiode = $T_{CONTROL}$. If the diode temperature is less than $T_{CONTROL}$, then the case temperature is permitted to exceed the Thermal Profile, but the diode temperature must remain at or below $T_{CONTROL}$. The thermal solution for the processor must be able to keep the processor's T_{CASE} at or below the T_{CASE} values defined by the Thermal Profile between the T_{CASE}MAX @$P_{_PROFILE_MIN}$and T_{CASE}MAX points at the corresponding power levels.

Refer to Section 2.3.1 for the implementation of the $T_{CONTROL}$ value in support of fan speed control (FSC) design to achieve better acoustic performance.

2.2.4.1 Thermal Diode Correction Factor

The Dual-Core Intel Xeon Processor 5000 Series requires error correction to the processor's thermal diode reading. The parameter to assist designers in managing the error correction has been defined as the thermal diode (Tdiode) correction factor, $T_{DIODE\_CORRECTION\_FACTOR}$.

$T_{DIODE\_CORRECTION\_FACTOR}$ is a processor unique value, which defines the error correction that is to be applied to all thermal diode readings. The value for $T_{DIODE\_CORRECTION\_FACTOR}$ is calibrated in manufacturing and configured for each processor individually. For the Dual-Core Intel Xeon Processor 5000 Series, the $T_{DIODE\_CORRECTION\_FACTOR}$ value is obtained by reading a processor model specific register (MSR) and adding this offset value to a base value. The equation for calculating $T_{DIODE\_CORRECTION\_FACTOR}$ is:

Equation 2-3.$T_{DIODE\_CORRECTION\_FACTOR} = T_{DIODE\_BASE} + T_{DIODE\_OFFSET}$

Where:

T_{DIODE_BASE} = A fixed base value defined for a given processor generation as published in the processor EMTS or data sheet.

T_{DIODE_OFFSET} = A signed (+/-) offset value from the Thermal Diode_Base value specified in the processor EMTS or data sheet. This value is programmed into each processor during manufacturing and can be obtained by reading the IA_32_TEMPERATURE_TARGET MSR. This is a static and a unique value. Refer to the *Cedar Mill Processor Family BIOS Writer's Guide (BWG)* for further details.

The T_{DIODE_BASE} value for the Dual-Core Intel Xeon Processor 5000 Series is 0°C. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for the latest T_{DIODE_BASE} value. The T_{DIODE_OFFSET} value, which depends on several factors, can provide up to 28 degrees (+/-14 degrees) of correction.

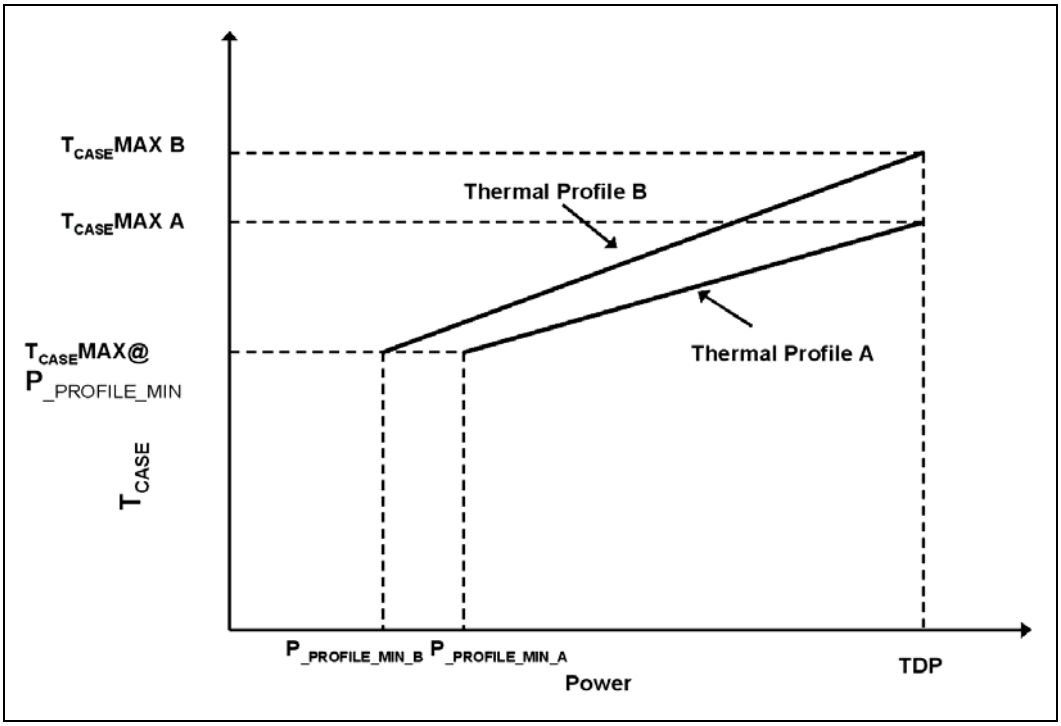
Fan speed control components that utilized the diode model will need to apply the thermal diode correction factor. Fan speed control components that use a transistor model can ignore the thermal diode correction factor. Refer to Section 2.3.2 for the implementation of the thermal diode correction factor in support of fan speed control (FSC) design to achieve better acoustic performance

2.2.5 Thermal Profile Concepts for the Dual-Core Intel® Xeon® Processor 5000 Series

2.2.5.1 Dual Thermal Profile Concept for the Dual-Core Intel Xeon Processor 5000 Series Processors

The Dual-Core Intel Xeon Processor 5000 Series processors are designed to go into various form factors, including the volumetrically constrained 1U and custom blade form factors. Due to certain limitations of such form factors (for example, airflow, thermal solution height), it is very challenging to meet the thermal requirements of the processor. To mitigate these form factor constraints, Intel has developed a dual Thermal Profile specification, shown in Figure 2-7.

Figure 2-7. Dual Thermal Profile Diagram



The Thermal Profile A is based on Intel's 2U+ air cooling solution. Designing to Thermal Profile A ensures that no measurable performance loss due to Thermal Control Circuit (TCC) activation is observed in the processor. It is expected that TCC would only be activated for very brief periods of time when running a worst-case real world application in a worst-case thermal condition. These brief instances of TCC activation are not expected to impact the performance of the processor. A worst case real world application is defined as a commercially available, useful application which dissipates a power equal to, or above, the TDP for a thermally relevant timeframe. One example of a worst-case thermal condition is when a processor local ambient temperature is at or above 42.7°C for Dual-Core Intel Xeon Processor 5000 Series Thermal Profile A.

Thermal Profile B supports volumetrically constrained platforms (for example, 1U, blades, and so on), and is based on Intel's 1U air cooling solution. Because of the reduced capability represented by such thermal solutions, designing to Thermal Profile B results in an increased probability of TCC activation and an associated measurable performance loss. Measurable performance loss is defined to be any degradation in the processor's performance greater than 1.5%. The 1.5% number is chosen as the baseline since the run-to-run variation in a given performance benchmark is typically between 1–2%.

Although designing to Thermal Profile B results in increased T_{CASE} temperatures compared to Thermal Profile A at a given power level, both of these Thermal Profiles ensure that Intel's long-term processor reliability requirements are satisfied. In other words, designing to Thermal Profile B does not impose any additional risk to Intel's long-term reliability requirements. Thermal solutions that exceed Thermal Profile B specification are considered incompliant and will adversely affect the long-term reliability of the processor.

Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* or Section 2.2.6 for the Thermal Profile A and Thermal Profile B specifications. Section 2.4 of this document also provides details on the 2U+ and 1U Intel reference thermal solutions that are designed to meet the Dual-Core Intel Xeon Processor 5000 Series Thermal Profile A and Thermal Profile B respectively.

2.2.5.2 Thermal Profile Concept for the Dual-Core Intel Xeon Processor 5063 (MV)

The Dual-Core Intel Xeon Processor 5063 (MV) is designed to go primarily into volumetrically constrained 1U and custom blade form factors.

The Thermal Profile is based on Intel's 1U air cooling solution. Designing to the Thermal Profile ensures that no measurable performance loss due to Thermal Control Circuit (TCC) activation is observed in the processor. It is expected that TCC would only be activated for very brief periods of time when running a worst-case real world application in a worst-case thermal condition. These brief instances of TCC activation are not expected to impact the performance of the processor. A worst case real world application is defined as a commercially available, useful application which dissipates a power equal to, or above, the TDP for a thermally relevant timeframe. One example of a worst-case thermal condition is when a processor local ambient temperature is at or above 42.7°C for Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile.

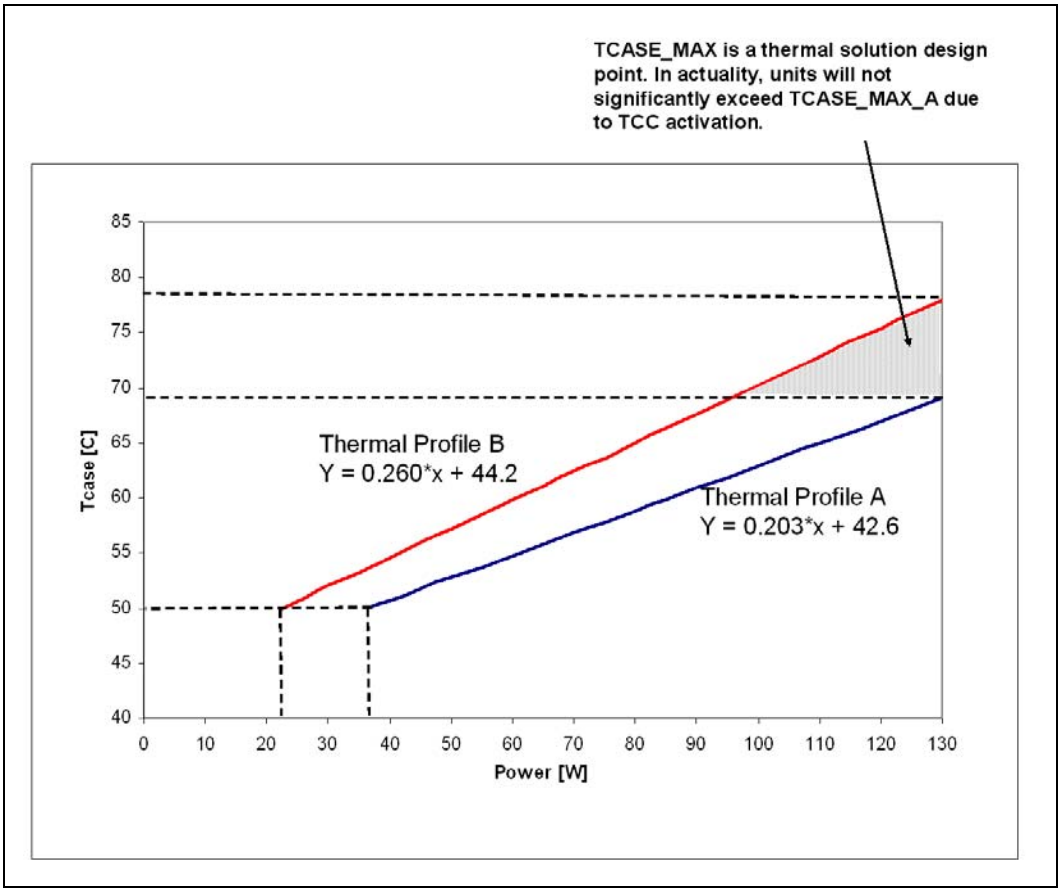
Thermal solutions that exceed the Thermal Profile specification are considered incompliant and will adversely affect the long-term reliability of the processor.

Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* or Section 2.2.6 for the Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile specifications. Section 2.4 of this document also provides details on the 1U Intel reference thermal solutions that is designed to meet the Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile.

2.2.6 Performance Targets

The Thermal Profile specifications for this processor are published in the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications*. These Thermal Profile specifications are shown as a reference in the subsequent discussions.

Figure 2-8. Thermal Profiles A and B for the Dual-Core Intel® Xeon® Processor 5080



Note: The thermal specifications shown in this graph are for reference only. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for the Thermal Profile specifications. In case of conflict, the data information in the EMTS supersedes any data in this figure.

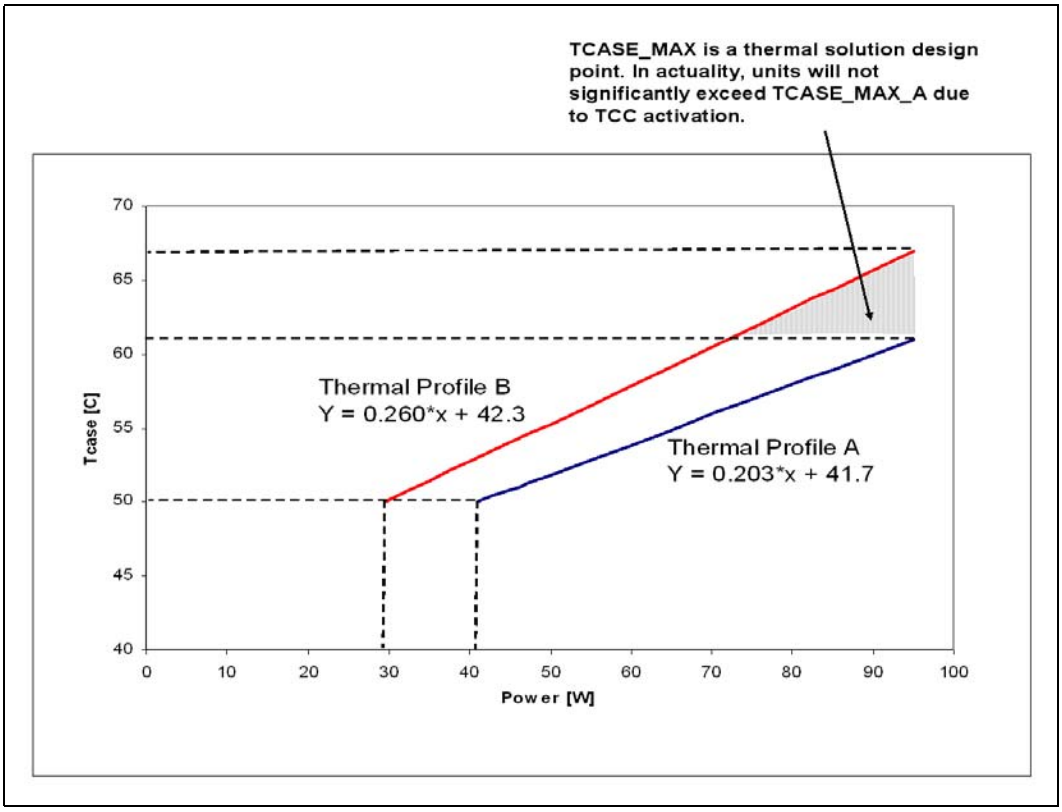
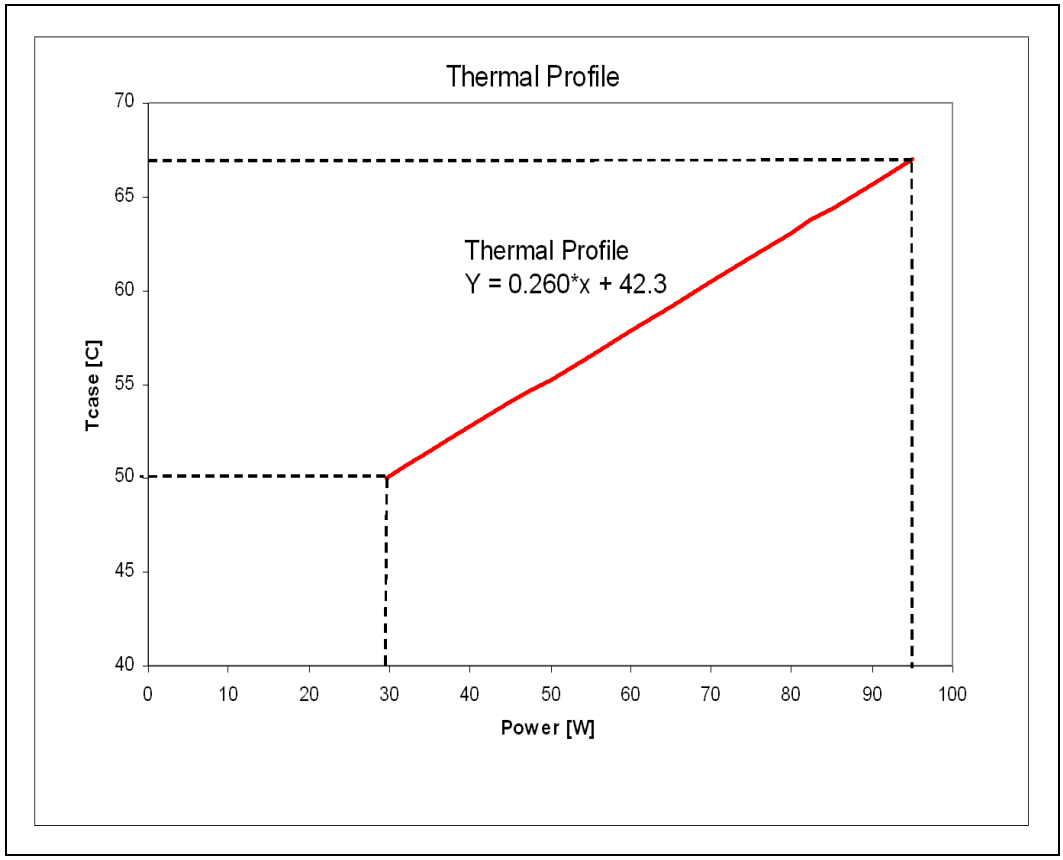


Figure 2-9. Thermal Profiles A and B for the Dual-Core Intel® Xeon® Processor 5050

Note: The thermal specifications shown in this graph are for reference only. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for the Thermal Profile specifications. In case of conflict, the data information in the EMTS supersedes any data in this figure.

Figure 2-10. Thermal Profile for the Dual-Core Intel® Xeon® Processor 5063 (MV)



Note: The thermal specifications shown in this graph are for reference only. Refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* for the Thermal Profile specifications. In case of conflict, the data information in the EMTS supersedes any data in this figure.

Table 2-4, Table 2-5 and Table 2-6 describe thermal performance targets for the Dual-Core Intel Xeon Processor 5000 Series cooling solution enabled by Intel.

Table 2-4. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5080

Parameter	Maximum	Unit	Notes
Altitude	Sea-level	m	Heatsink designed at 0 meters
T_{LA}	40	°C	
TDP	130	W	
2U+ Reference Solution, Thermal Profile A			
$T_{CASE\_MAX\_A}$	69	°C	
T_{CASE_MAX} @ P_profile_min	50	°C	P_profile_min= 36.5 W.
Airflow	27 45.9	CFM m^3 / hr	Airflow through the heatsink fins
Pressure Drop	0.182 45.3	Inches of H_2O Pa	
Ψ_{CA}	0.217	°C/W	Mean + 3σ
1U Reference Solution, Thermal Profile B			
$T_{CASE\_MAX\_B}$ (Profile B)	78	°C	
T_{CASE_MAX} @ P_profile_min (Profile B)	50	°C	P_profile_min = 22.3 W.
Airflow	15 25.5	CFM m^3 / hr	Airflow through the heatsink fins
Pressure Drop	0.331 82.4	Inches of H_2O Pa	
Ψ_{CA}	0.276	°C/W	Mean + 3σ

Note: In case of conflict, the processor EMTS supersedes the information contained in the TMDG.

Table 2-5. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5050 (Sheet 1 of 2)

Parameter	Maximum	Unit	Notes
Altitude	Sea-level	m	Heatsink designed at 0 meters
T_{LA}	40	°C	
TDP	95	W	
2U+ Reference Solution, Thermal Profile A			
$T_{CASE\_MAX\_A}$	61	°C	
T_{CASE_MAX} @ P_profile_min	50	°C	P_profile_min = 40.9 W.
Airflow	27 45.9	CFM m^3 / hr	Airflow through the heatsink fins
Pressure Drop	0.182 45.3	Inches of H_2O Pa	
Ψ_{CA}	0.217	°C/W	Mean + 3σ
1U Reference Solution, Thermal Profile B			
$T_{CASE\_MAX\_B}$ (Profile B)	67	°C	

Table 2-5. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5050 (Sheet 2 of 2)

T_{CASE_MAX} @ P_profile_min (Profile B)	50	°C	P_profile_min = 29.6 W.
Airflow	15 25.5	CFM m^3 / hr	Airflow through the heatsink fins
Pressure Drop	0.331 82.4	Inches of H_2O Pa	
Ψ_{CA}	0.276	°C/W	Mean + 3σ

Note: In case of conflict, the processor EMTS supersedes the information contained in the TMDG.

Table 2-6. Intel Reference Heatsink Performance Targets for the Dual-Core Intel® Xeon® Processor 5063 (MV)

Parameter	Maximum	Unit	Notes
Altitude	Sea-level	m	Heatsink designed at 0 meters
T_{LA}	40	°C	
TDP	95	W	
Reference Solution, Thermal Profile			
T_{CASE_MAX}	67	°C	
T_{CASE_MAX} @ P_profile_min	50	°C	P_profile_min = 29.6 W.
Airflow	15 25.5	CFM m^3 / hr	Airflow through the heatsink fins
Pressure Drop	0.331 82.4	Inches of H_2O Pa	
Ψ_{CA}	0.276	°C/W	Mean + 3σ

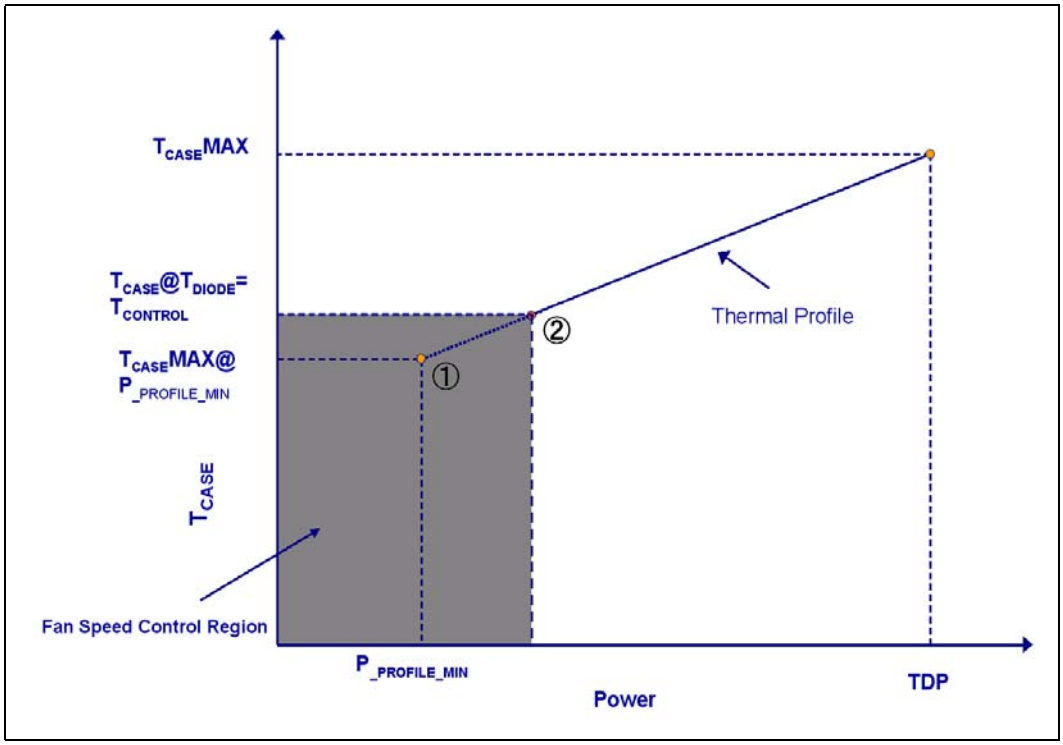
Note: In case of conflict, the processor EMTS supersedes the information contained in the TMDG.

2.3 Characterizing Cooling Solution Performance Requirements

2.3.1 Fan Speed Control

Fan speed control (FSC) techniques to reduce system level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determine the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the T_{CASE} of the processor at a given power level. Since the T_{CASE} of a processor is an important parameter in the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the Thermal Profile and hence the long-term reliability requirements. For this purpose, the parameter called $T_{CONTROL}$ as explained in Section 2.2.1, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system level acoustic noise down. Figure 2-11 depicts the relationship between $T_{CONTROL}$ and FSC methodology.

Figure 2-11. $T_{CONTROL}$ and Fan Speed Control

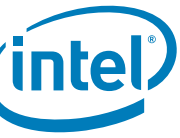


Once the $T_{CONTROL}$ value is determined as explained earlier, the thermal diode temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in Table 2-7 without compromising the long-term reliability of the processor.

Table 2-7. Fan Speed Control, $T_{CONTROL}$ and T_{DIODE} Relationship

Condition	FSC Scheme
$T_{DIODE} \leq T_{CONTROL}$	FSC can adjust fan speed to maintain $T_{DIODE} = T_{CONTROL}$ (low acoustic region).
$T_{DIODE} > T_{CONTROL}$	FSC should adjust fan speed to keep T_{CASE} at or below the Thermal Profile specification (increased acoustic region).

There are many different ways of implementing fan speed control, including FSC based on processor ambient temperature, FSC based on processor thermal diode temperature (T_{DIODE}) or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the thermal diode, sustained temperatures above $T_{CONTROL}$ drives fans to maximum RPM. If FSC is based both on ambient and thermal diode, ambient temperature can be used to scale the fan RPM controlled by the thermal diode. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the Thermal Profile specification is met when the processor diode temperature exceeds the T_{CONTOL} value for a given processor.

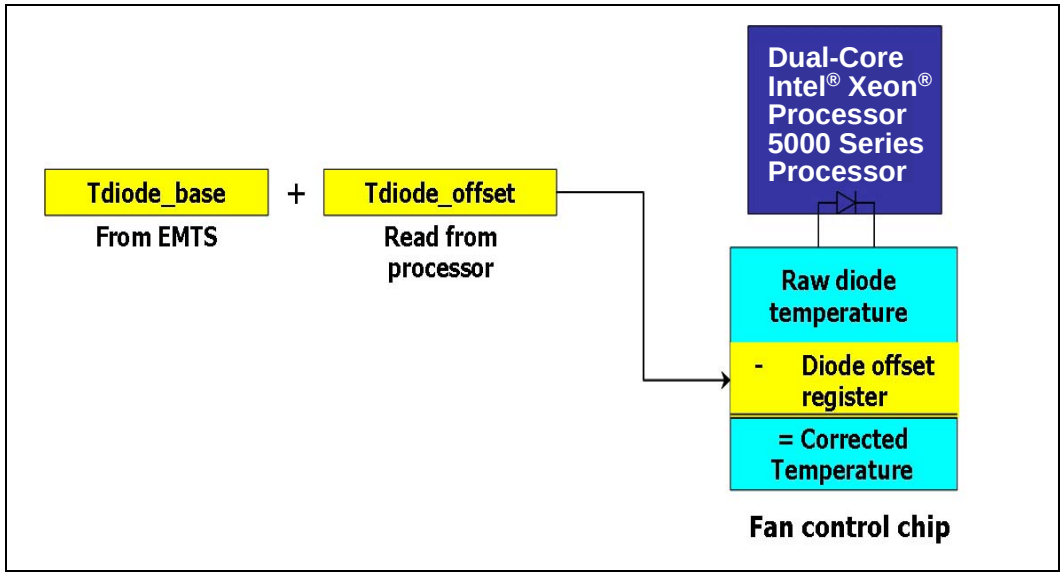


2.3.2 Thermal Diode Correction Factor and Fan Speed Control

The Dual-Core Intel Xeon Processor 5000 Series requires that a correction factor be applied to the thermal diode value before passing the thermal diode value to Fan Speed Control applications.

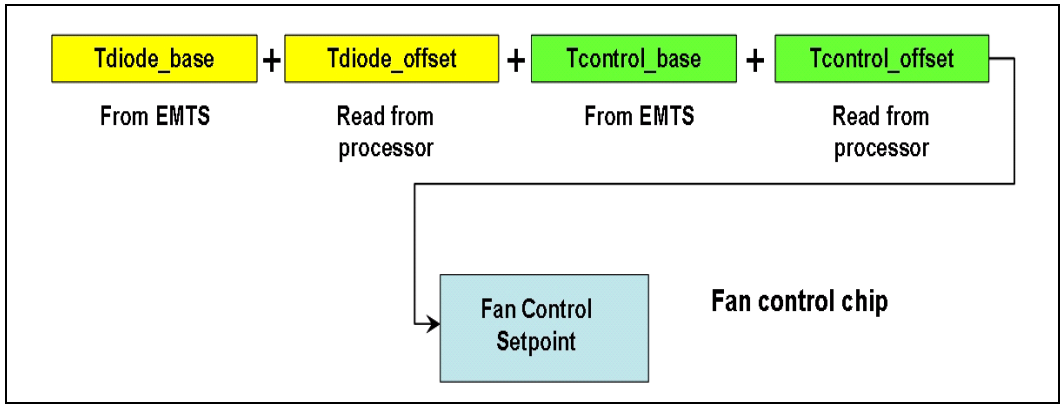
For fan speed control devices with a built-in offset register, the BIOS will read the thermal diode offset value from the processor and will add it to the base thermal diode value, then this combined value will be written to the offset register of the fan control device. In this usage model, once the offset register is programmed in the fan speed control device, all future temperature readings from the thermal diode will be automatically adjusted as shown in Figure 2-12.

Figure 2-12. Diode Error Correction Usage Model for Fan Speed Control with Offset Register



For fan speed control devices without a built-in offset register, the thermal diode correction factor will need to be applied to the thermal diode value when determining the fan control setpoint. This is illustrated in Figure 2-13.

Figure 2-13. Diode Error Correction Usage Model for Fan Speed Control without Offset Register



2.3.3 Processor Thermal Characterization Parameter Relationships

The idea of a “thermal characterization parameter”, Ψ (psi), is a convenient way to characterize the performance needed for the thermal solution and to compare thermal solutions in identical conditions (heating source, local ambient conditions). A thermal characterization parameter is convenient in that it is calculated using total package power, whereas actual thermal resistance, θ (theta), is calculated using actual power dissipated between two points. Measuring actual power dissipated into the heatsink is difficult, since some of the power is dissipated via heat transfer into the socket and board. Be aware, however, of the limitations of lumped parameters such as Ψ when it comes to a real design. Heat transfer is a three-dimensional phenomenon that can rarely be accurately and easily modeled by lump values.

The case-to-local ambient thermal characterization parameter value (Ψ_{CA}) is used as a measure of the thermal performance of the overall thermal solution that is attached to the processor package. It is defined by the following equation, and measured in units of °C/W:

Equation 2-4. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

Ψ_{CA}=Case-to-local ambient thermal characterization parameter (°C/W).

T_{CASE}=Processor case temperature (°C).

T_{LA}=Local ambient temperature in chassis at processor (°C).

TDP=TDP dissipation (W) (assumes all power dissipates through the integrated heat spreader (IHS)).

The case-to-local ambient thermal characterization parameter of the processor, Ψ_{CA}, is comprised of Ψ_{CS}, the TIM thermal characterization parameter, and of Ψ_{SA}, the sink-to-local ambient thermal characterization parameter:

Equation 2-5. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

Where:

Ψ_{CS}=Thermal characterization parameter of the TIM (°C/W).

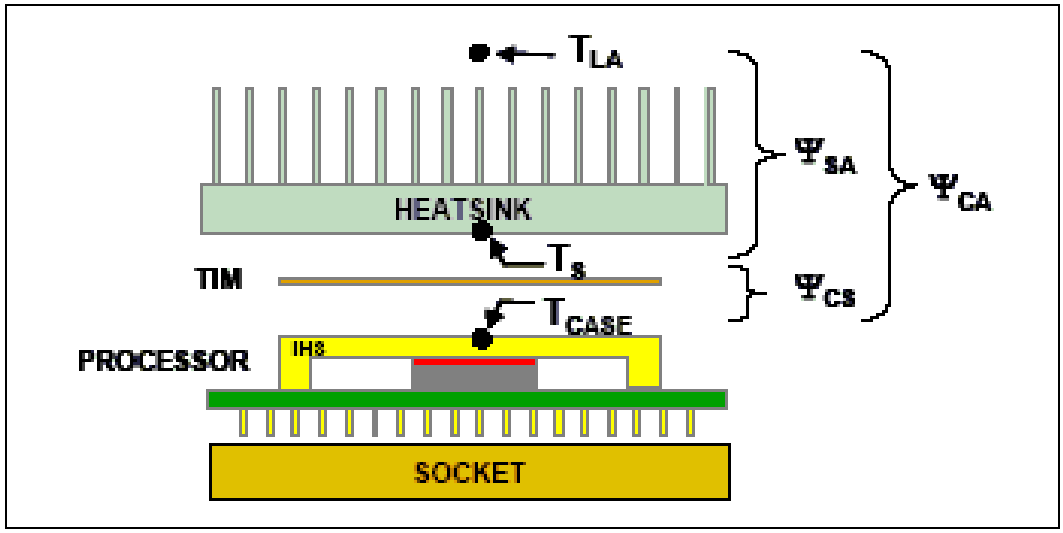
Ψ_{SA}=Thermal characterization parameter from heatsink-to-local ambient (°C/W).

Ψ_{CS} is strongly dependent on the thermal conductivity and thickness of the TIM between the heatsink and IHS.

Ψ_{SA} is a measure of the thermal characterization parameter from the bottom of the heatsink to the local ambient air. Ψ_{SA} is dependent on the heatsink material, thermal conductivity, and geometry. It is also strongly dependent on the air velocity through the fins of the heatsink.

Figure 2-14 illustrates the combination of the different thermal characterization parameters.

Figure 2-14. Processor Thermal Characterization Parameter Relationships



2.3.3.1 Example

The cooling performance, $\Psi_{CA,}$ is then defined using the principle of thermal characterization parameter described above:

- Define a target case temperature $T_{CASE-MAX}$ and corresponding TDP, given in the processor EMTS.
- Define a target local ambient temperature at the processor, T_{LA}.

The following provides an illustration of how one might determine the appropriate performance targets. The example power and temperature numbers used here are not related to any Intel processor thermal specifications, and are for illustrative purposes only.

Assume the EMTS TDP is 85 W and the case temperature specification is 68°C. Assume as well that the system airflow has been designed such that the local processor ambient temperature is 45°C. Then the following could be calculated using equation (2-3) from above:

Equation 2-6. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 - 45) / 85 = 0.27°C/W$

To determine the required heatsink performance, a heatsink solution provider would need to determine Ψ_{CS} performance for the selected TIM and mechanical load configuration. If the heatsink solution was designed to work with a TIM material performing at $\Psi_{CS} \leq 0.05$°C/W, solving for equation (2-4) from above, the performance of the heatsink would be:

Equation 2-7. $\Psi_{SA} = \Psi_{CA} - \Psi_{CS} = 0.27 - 0.05 = 0.22°C/W$

If the local processor ambient temperature is assumed to be 40°C, the same calculation can be carried out to determine the new case-to-ambient thermal resistance:

Equation 2-8. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP = (68 - 40) / 85 = 0.33°C/W$

It is evident from the above calculations that, a reduction in the local processor ambient temperature has a significant positive effect on the case-to-ambient thermal resistance requirement.

2.3.4 Chassis Thermal Design Considerations

2.3.4.1 Chassis Thermal Design Capabilities and Improvements

One of the critical parameters in thermal design is the local ambient temperature assumption of the processor. Keeping the external chassis temperature fixed, internal chassis temperature rise is the only component that can affect the processor local ambient temperature. Every degree gained at the local ambient temperature directly translates into a degree relief in the processor case temperature.

Given the thermal targets for the processor, it is extremely important to optimize the chassis design to minimize the air temperature rise upstream to the processor (T_{rise}), hence minimizing the processor local ambient temperature. Please refer to *T_{RISE} Reduction Guidelines for Rack Servers and Workstations* for more details.

The heat generated by components within the chassis must be removed to provide an adequate operating environment for both the processor and other system components. Moving air through the chassis brings in air from the external ambient environment and transports the heat generated by the processor and other system components out of the system. The number, size and relative position of fans, vents and other heat generating components determine the chassis thermal performance, and the resulting ambient temperature around the processor. The size and type (passive or active) of the thermal solution and the amount of system airflow can be traded off against each other to meet specific system design constraints. Additional constraints are board layout, spacing, component placement, and structural considerations that limit the thermal solution size.

In addition to passive heatsinks, fan heatsinks and system fans, other solutions exist for cooling integrated circuit devices. For example, ducted blowers, heat pipes and liquid cooling are all capable of dissipating additional heat. Due to their varying attributes, each of these solutions may be appropriate for a particular system implementation.

To develop a reliable, cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of fans that can be used in a particular design.

2.4 Thermal/Mechanical Reference Design Considerations

2.4.1 Heatsink Solutions

2.4.1.1 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- **The area of the surface on which the heat transfer takes place** – Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is by attaching a heatsink to the IHS. A heatsink

can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.

- **The conduction path from the heat source to the heatsink fins –** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it. Refer to Section 2.4.2 for further information on the TIM between the IHS and the heatsink base.
- **The heat transfer conditions on the surface on which heat transfer takes place –** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA}, and the local air velocity over the surface. The higher the air velocity over the surface, the resulting cooling is more efficient. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface required to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases: it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

2.4.2 Thermal Interface Material

TIM application between the processor IHS and the heatsink base is generally required to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier and allow direct heatsink attach, without the need for a separate TIM dispense or attach process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures the entire processor IHS area is covered. It is important to compensate for heatsink-to-processor attach positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective application tape over it. This tape must be removed prior to heatsink installation.

The TIM performance is susceptible to degradation (that is, grease breakdown) during the useful life of the processor due to the temperature cycling phenomena. For this reason, the measured T_{CASE} value of a given processor can decrease over time depending on the type of TIM material.

Refer to Section 2.4.7.2 for information on the TIM used in the Intel reference heatsink solution.

2.4.3 Summary

In summary, considerations in heatsink design include:

- The local ambient temperature T_{LA} at the heatsink, airflow (CFM), the power being dissipated by the processor, and the corresponding maximum T_{CASE}. These parameters are usually combined in a single lump cooling performance parameter, Ψ_{CA} (case to air thermal characterization parameter). More information on the definition and the use of Ψ_{CA} is given in Section 2.4 and Section 2.3.3.
- Heatsink interface (to IHS) surface characteristics, including flatness and roughness.
- The performance of the TIM used between the heatsink and the IHS.
- Surface area of the heatsink.
- Heatsink material and technology.
- Development of airflow entering and within the heatsink area.
- Physical volumetric constraints placed by the system.
- Integrated package/socket stack-up height information is provided in the *LGA771 Socket Mechanical Design Guide*.

2.4.4 Assembly Overview of the Intel Reference Thermal Mechanical Design

The reference design heatsinks that meet the Dual-Core Intel Xeon Processor 5000 Series thermal performance targets are called the Common Enabling Kit (CEK) heatsinks, and are available in 1U, 2U, & 2U+ form factors. Each CEK consists of the following components:

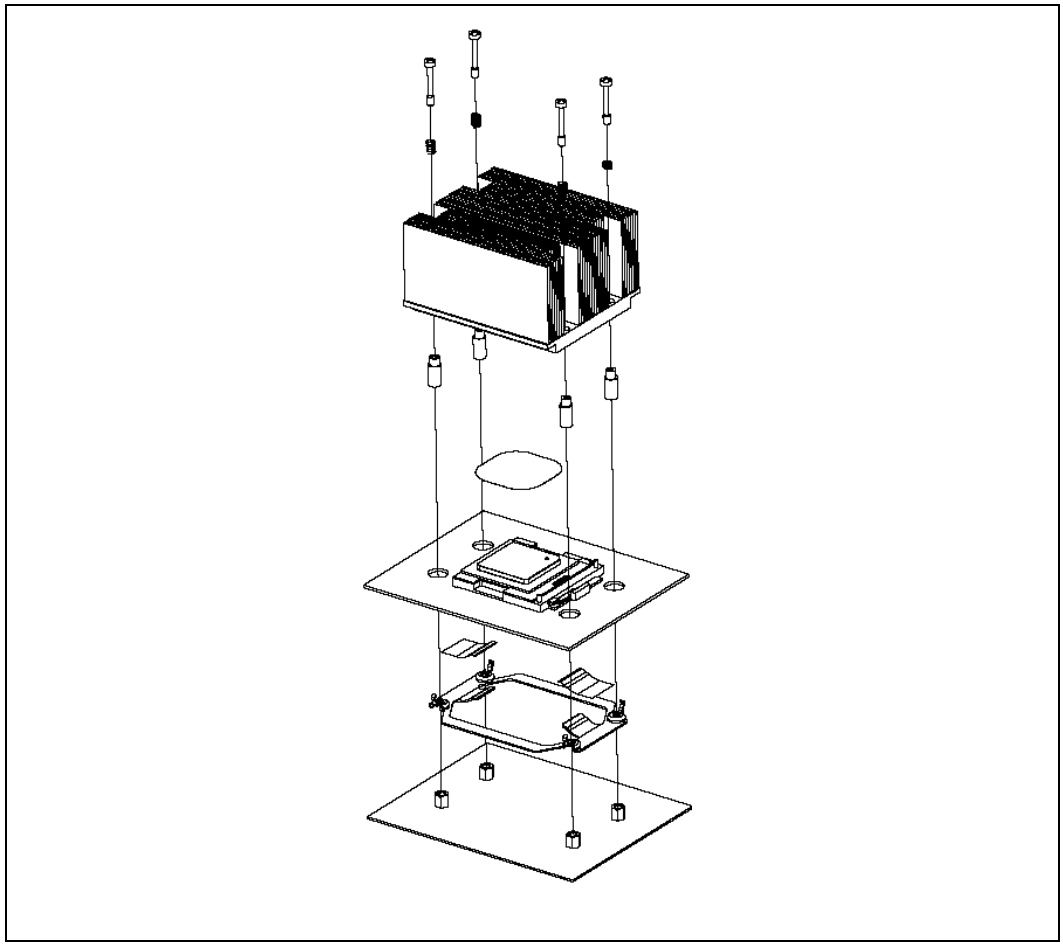
- Heatsink (with captive standoff and screws)
- Thermal Interface Material (TIM)
- CEK Spring

2.4.4.1 Geometric Envelope

The baseboard keepout zones on the primary and secondary sides and height restrictions under the enabling component region are shown in detail in Appendix A. The overall volumetric keep in zone encapsulates the processor, socket, and the entire thermal/mechanical enabling solution.

2.4.4.2 Assembly Drawing

Figure 2-15. Exploded View of CEK Thermal Solution Components



The CEK reference thermal solution is designed to extend air-cooling capability through the use of larger heatsinks with minimal airflow blockage and bypass. CEK retention solution can allow the use of much heavier heatsink masses compared to the legacy limits by using a load path directly attached to the chassis pan. The CEK spring on the secondary side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heatsink are transferred to the chassis pan via the stiff captive screws and standoffs. This reduces the risk of package pullout and solder-joint failures.

Using the CEK reference thermal solution, Intel recommends that the maximum outside diameter dimension of the chassis pan standoffs, regardless of shape, that interfaces with the CEK spring and captive screws to attach the heatsink to the chassis pan should be no larger than 7.112 mm [0.28 in.]. For example, circular standoffs should be no larger than 7.112 mm [0.28 in.] in diameter. Hexagonal standoffs should be no larger than 7.112 mm [0.28 in.] point-to-point.

The baseboard mounting holes for the CEK solution are at the same location as the hole locations used for previous Intel Xeon processor thermal solution. However, CEK assembly requires 10.16 mm [0.400 in.] large diameter holes to compensate for the CEK spring embosses.

The CEK solution is designed and optimized for a baseboard thickness range of 1.57 – 2.31 mm [0.062-0.093 in]. While the same CEK spring can be used for this board thickness range, the heatsink standoff height is different for a 1.57 mm [0.062 in] thick board than it is for a 2.31 mm [0.093 in] thick board. In the heatsink assembly, the standoff protrusion from the base of the heatsink needs to be 0.6 mm [0.024 in] longer for a 2.31 mm [0.093 in] thick board, compared to a 1.57 mm [0.062 in] thick board. If this solution is intended to be used on baseboards that fall outside of this range, then some aspects of the design, including but not limited to the CEK spring design and the standoff heights, may need to change. Therefore, system designers need to evaluate the thermal performance and mechanical behavior of the CEK design on baseboards with different thicknesses.

Refer to Appendix A for drawings of the heatsinks and CEK spring. The screws and standoffs are standard components that are made captive to the heatsink for ease of handling and assembly.

Contact your Intel field sales representative for an electronic version of mechanical and thermal models of the CEK (Pro/Engineer*, IGES and Icepak*, Flotherm* formats). Pro/Engineer*, Icepak* and Flotherm* models are available on Intel Business Link (IBL).

Note: Intel reserves the right to make changes and modifications to the design as necessary.

Note: The thermal mechanical reference design for the Dual-Core Intel Xeon Processor 5000 Series was verified according to the Intel validation criteria given in Appendix D.1. Any thermal mechanical design using some of the reference components in combination with any other thermal mechanical solution needs to be fully validated according to the customer criteria. Also, if customer thermal mechanical validation criteria differ from the Intel criteria, the reference solution should be validated against the customer criteria.

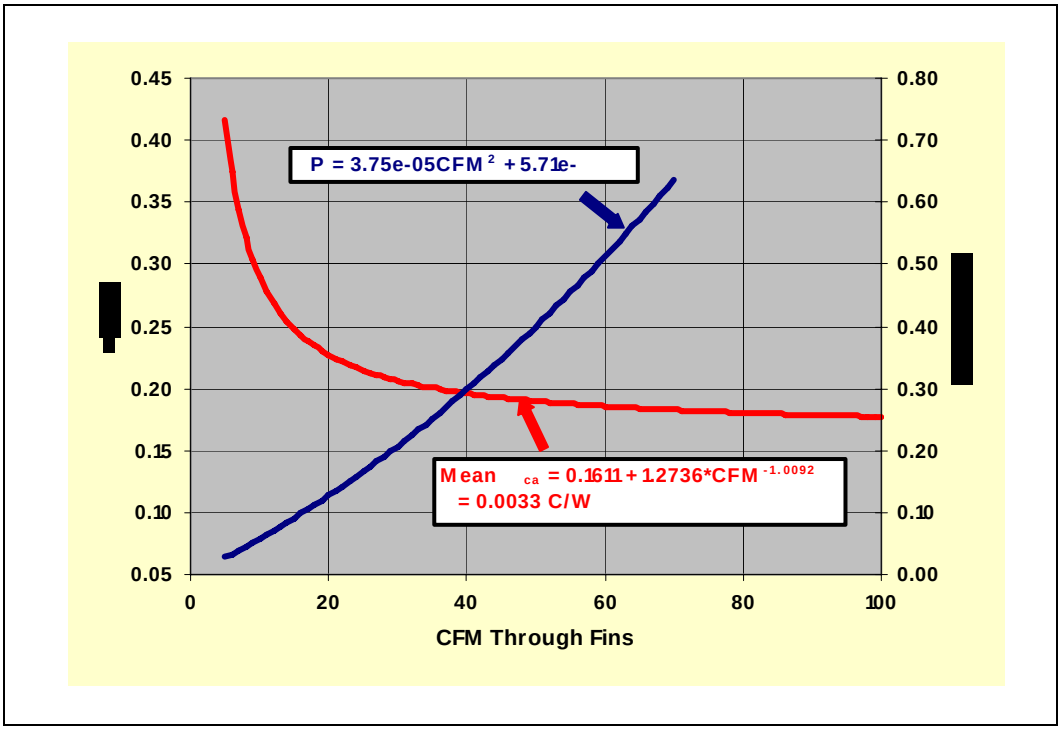
2.4.4.3 Structural Considerations of CEK

As Intel explores methods of keeping thermal solutions within the air-cooling space, the mass of the thermal solutions is increasing. Due to the flexible nature (and associated large deformation) of baseboard-only attachments, Intel reference solutions, such as CEK, are now commonly using direct chassis attach (DCA) as the mechanical retention design. The mass of the new thermal solutions is large enough to require consideration for structural support and stiffening on the chassis. Intel has published a best know method (BKM) document that provides specific structural guidance for designing DCA thermal solutions. The document is titled *Chassis Strength and Stiffness Measurement and Improvement Guidelines for Direct Chassis Attach Solutions*.

2.4.5 Thermal Solution Performance Characteristics

Figure 2-16 and Figure 2-17 show the performance of the 2U+ and 1U passive heatsinks, respectively. These figures show the thermal performance and the pressure drop through fins of the heatsink versus the airflow provided. The best-fit equations for these curves are also provided to make it easier for users to determine the desired value without any error associated with reading the graph.

Figure 2-16. 2U+ CEK Heatsink Thermal Performance



If other custom heatsinks are intended for use with the Dual-Core Intel Xeon Processor 5000 Series processors, they must support the following interface control requirements to be compatible with the reference mechanical components:

- **Requirement 1:** Heatsink assembly must stay within the volumetric keep-in.
- **Requirement 2:** Maximum mass and center of gravity.

Current maximum heatsink mass is 1000 grams [2.2 lbs] and the maximum center of gravity 3.81 cm [1.5 in.] above the bottom of the heatsink base.

- **Requirement 3:** Maximum and minimum compressive load.

Any custom thermal solution design must meet the loading specification as documented within this document, and should refer to the *Dual-Core Intel® Xeon® Processor 5000 Series Electrical, Mechanical, and Thermal Specifications* and *LGA771 Socket Mechanical Design Guide* and for specific details on package/socket loading specifications.

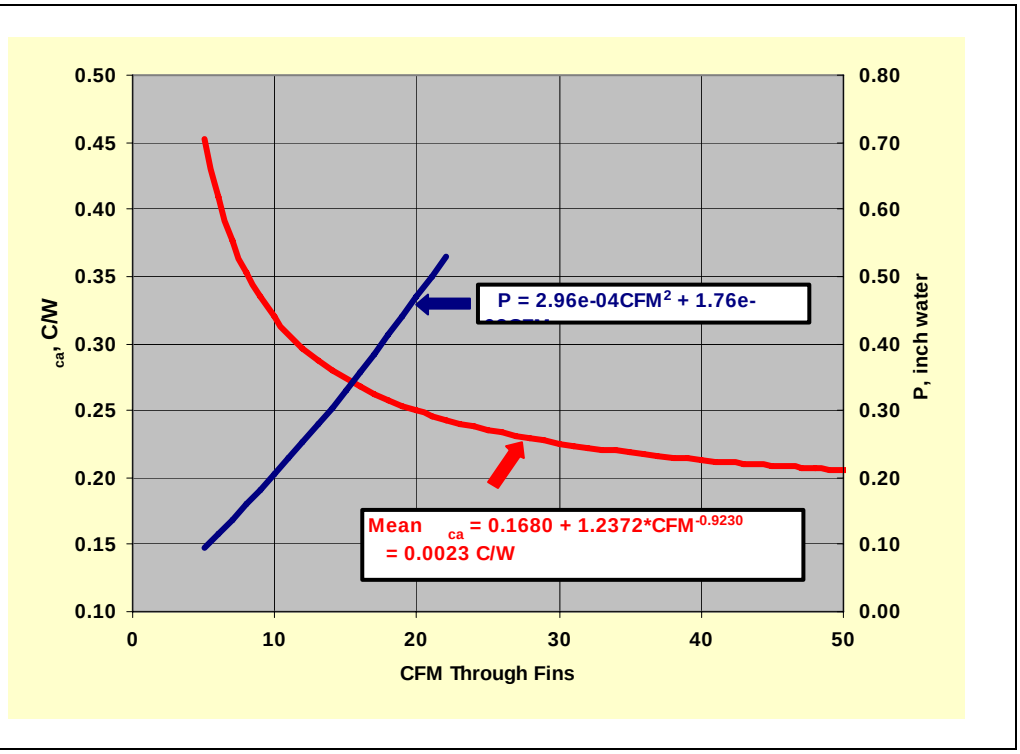


Figure 2-17. 1U CEK Heatsink Thermal Performance

2.4.6 Thermal Profile Adherence

The 2U+ CEK Intel reference thermal solution is designed to meet the Thermal Profile A for the Dual-Core Intel Xeon Processor 5080. From Table 2-8, the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.217°C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

Equation 2-9.y = 0.217x + 40

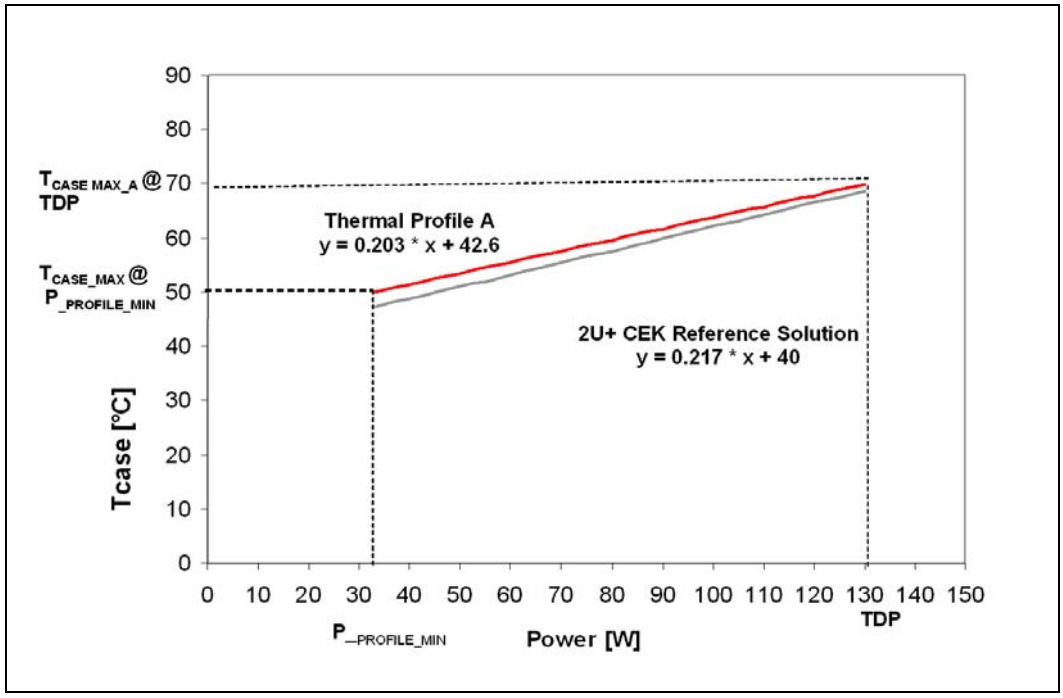
where,

y = Processor T_{CASE} value (°C)

x = Processor power value (W)

Figure 2-18 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon Processor 5080 Thermal Profile A specification. The 2U+ CEK solution meets the Thermal Profile A with a 2.1°C margin at the lower end ($P_{\_PROFILE\_MIN}$) and 0.8°C margin at the upper end (TDP). By designing to Thermal Profile A, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

Figure 2-18. 2U+CEK Thermal Adherence to Dual-Core Intel® Xeon® Processor 5080 Thermal Profile A



The 1U CEK Intel reference thermal solution is designed to meet the Thermal Profile B for the Dual-Core Intel Xeon Processor 5080. From Table 2-8 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.276°C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

Equation 2-10.y = 0.276x + 40

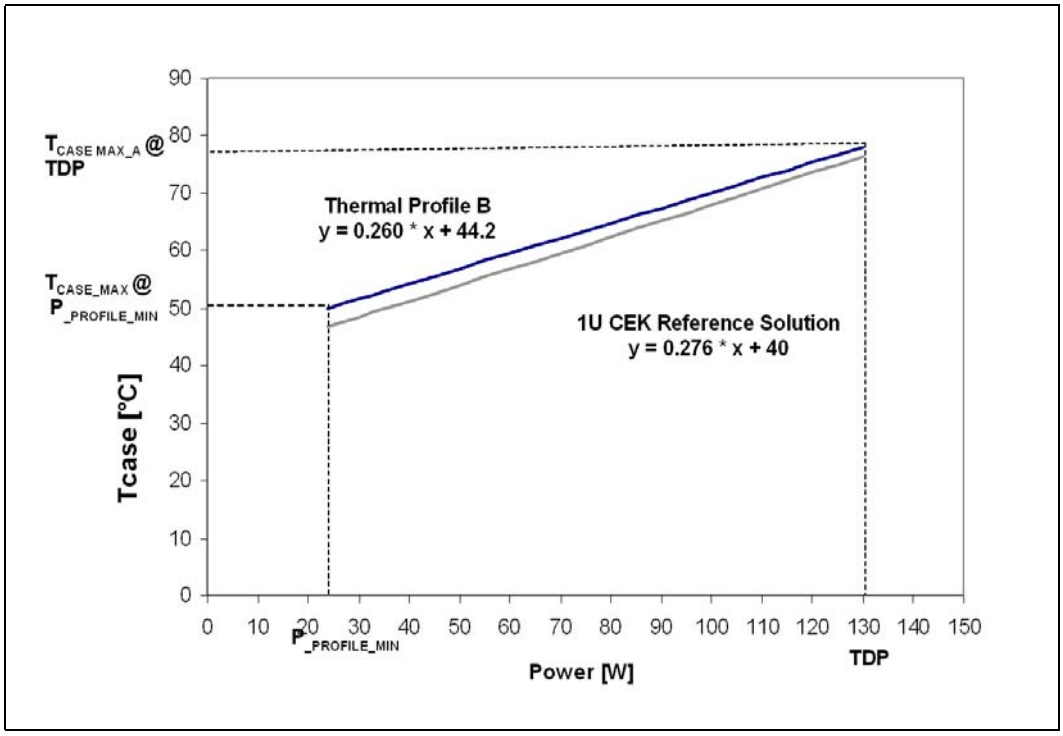
where,

y = Processor T_{CASE} value (°C)

x = Processor power value (W)

Figure 2-19 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon Processor 5080 Thermal Profile B specification. The 1U CEK solution meets the Thermal Profile B with 3.8°C margin at the lower end ($P_{\_PROFILE\_MIN}$) and 2.1°C margin at the upper end (TDP). However, as explained in Section 2.2.5, designing to Thermal Profile B results in increased TCC activation and measurable performance loss for the processor.

Figure 2-19. 1U CEK Thermal Adherence to Dual-Core Intel® Xeon® Processor 5080 Thermal Profile B



The 2U+ CEK Intel reference thermal solution is designed to meet the Thermal Profile A for the Dual-Core Intel Xeon Processor 5050. From Table 2-8, the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.217°C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

Equation 2-11.y = 0.217x + 40

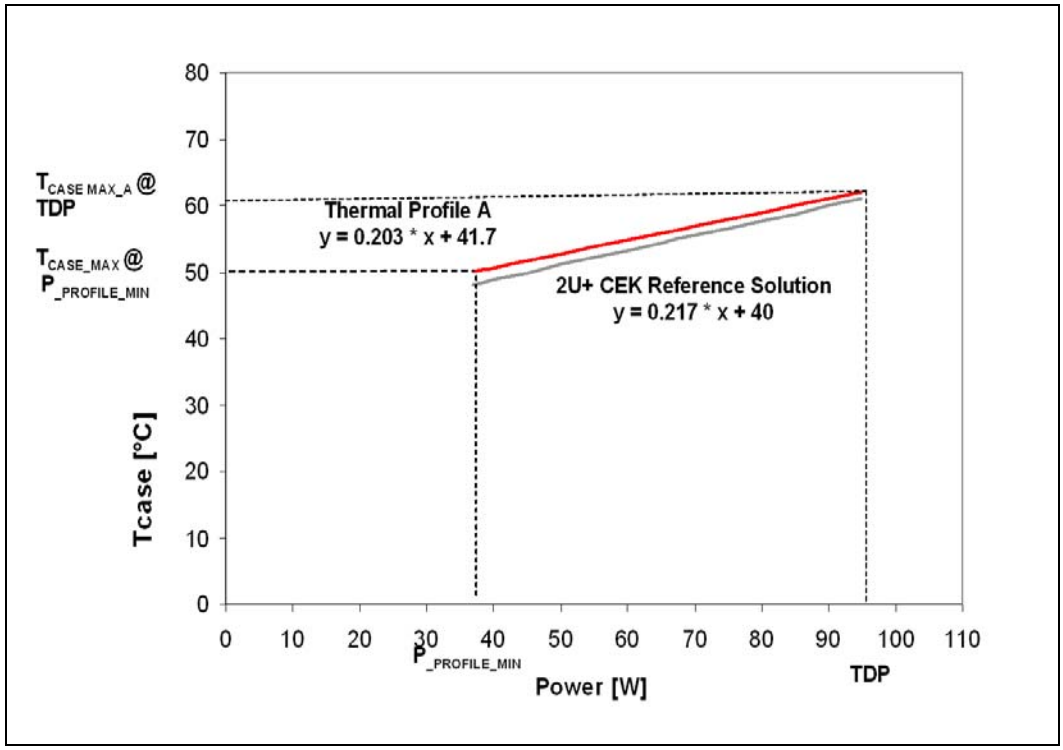
where,

y = Processor T_{CASE} value (°C)

x = Processor power value (W)

Figure 2-20 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon Processor 5050 Thermal Profile A specification. The 2U+ CEK solution meets the Thermal Profile A with a 1.1°C margin at the lower end ($P_{\_PROFILE\_MIN}$) and 0.4°C margin at the upper end (TDP). By designing to Thermal Profile A, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

Figure 2-20. 2U+CEK Thermal Adherence to Dual-Core Intel® Xeon® Processor 5050 Thermal Profile A



The 1U CEK Intel reference thermal solution is designed to meet the Thermal Profile B for the Dual-Core Intel Xeon Processor 5050. From Table 2-8 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.276°C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

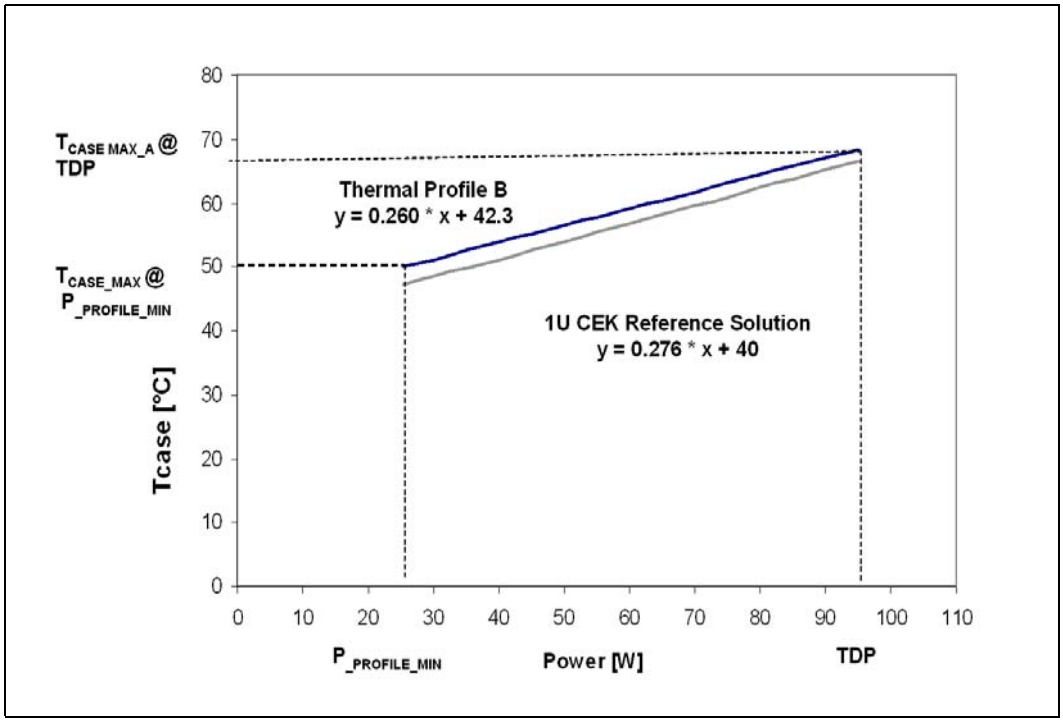
Equation 2-12.y = 0.276x + 40

where,

y = Processor T_{CASE} value (°C)
x = Processor power value (W)

Figure 2-21 below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon Processor 5050 Thermal Profile B specification. The 1U CEK solution meets the Thermal Profile B with 1.8°C margin at the lower end ($P_{\_PROFILE\_MIN}$) and 0.8°C margin at the upper end (TDP). However, as explained in Section 2.2.5, designing to Thermal Profile B results in increased TCC activation and measurable performance loss for the processor.

Figure 2-21. 1U CEK Thermal Adherence to Dual-Core Intel® Xeon® Processor 5050 Thermal Profile B



The 1U CEK Intel reference thermal solution is designed to meet the Thermal Profile for the Dual-Core Intel Xeon Processor 5063 (MV). From Table 2-8 the three-sigma (mean+3sigma) performance of the thermal solution is computed to be 0.276°C/W and the processor local ambient temperature (T_{LA}) for this thermal solution is 40°C. Hence, the Thermal Profile equation for this thermal solution is calculated as:

Equation 2-13.y = 0.276x + 40

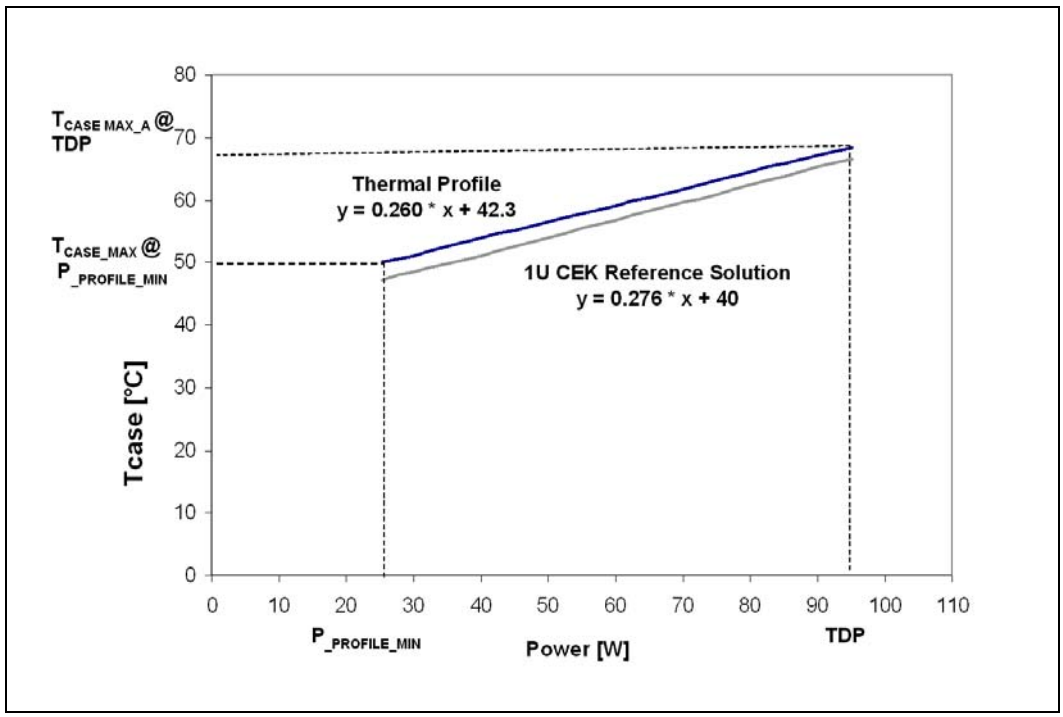
where,

y = Processor T_{CASE} value (°C)

x = Processor power value (W)

below shows the comparison of this reference thermal solution's Thermal Profile to the Dual-Core Intel Xeon Processor 5063 (MV) Thermal Profile B specification. The 1U CEK solution meets the Thermal Profile B with 1.8°C margin at the lower end ($P_{\_PROFILE\_MIN}$) and 0.8°C margin at the upper end (TDP). By designing to Thermal Profile A, it is ensured that no measurable performance loss due to TCC activation is observed under the given environmental conditions.

Figure 2-22. 1U CEK Thermal Adherence to Dual-Core Intel® Xeon® Processor 5063 (MV) Thermal Profile

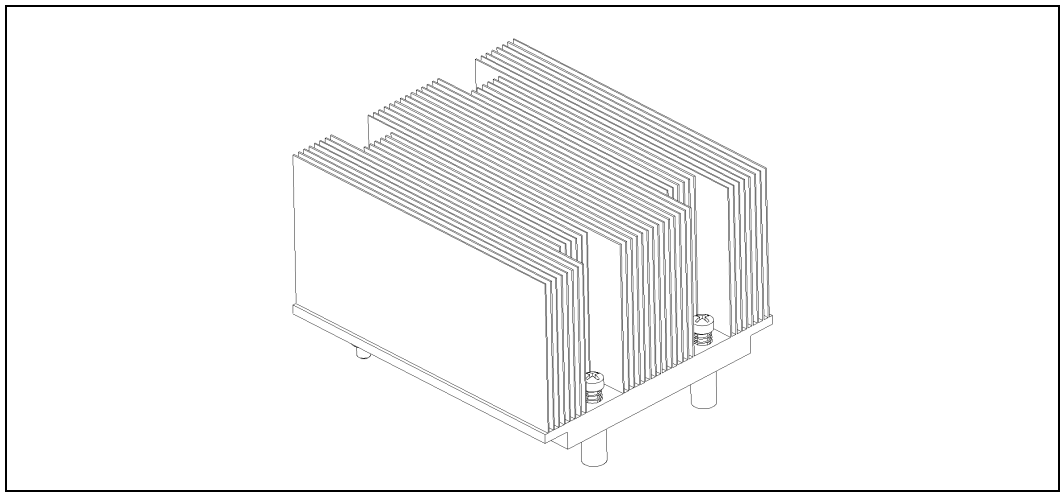


2.4.7 Components Overview

2.4.7.1 Heatsink with Captive Screws and Standoffs

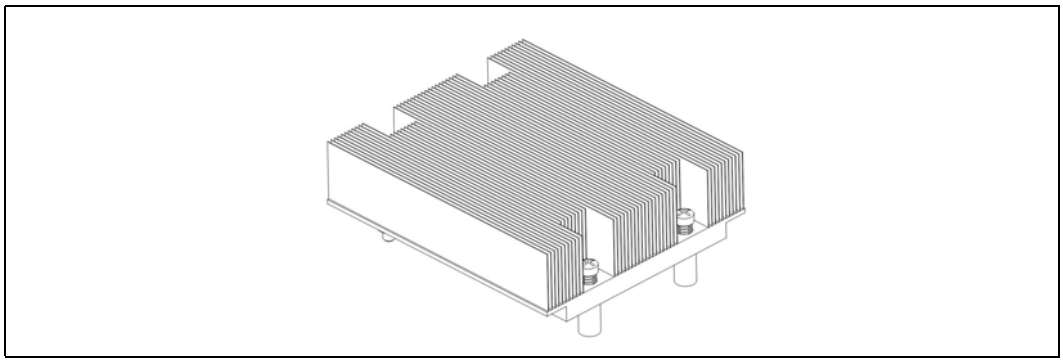
The CEK reference heatsink uses snapped-fin technology for its design. It consists of a copper base and copper fins with Shin-Etsu* G751 thermal grease as the TIM. The mounting screws and standoffs are also made captive to the heatsink base for ease of handling and assembly as shown in Figure 2-23 and Figure 2-24 for the 2U+ and 1U heatsinks, respectively.

Figure 2-23. Isometric View of the 2U+ CEK Heatsink



Note: Refer to Appendix A for more detailed mechanical drawings of the heatsink.

Figure 2-24. Isometric View of the 1U CEK Heatsink



Note: Refer to Appendix A for more detailed mechanical drawings of the heatsink.

The function of the standoffs is to provide a bridge between the chassis and the heatsink for attaching and load carrying. When assembled, the heatsink is rigid against the top of the standoff, and the standoff is rigid to a chassis standoff with the CEK spring firmly sandwiched between the two. In dynamic loading situations the standoff carries much of the heatsink load, especially in lateral conditions, when compared to the amount of load transmitted to the processor package. As such, it is comprised of steel. The distance from the bottom of the heatsink to the bottom of the standoff is 8.79 mm [0.346 in.] for a board thickness of 1.57 mm [0.062 in]. The standoff will need to be modified for use in applications with a different board thickness, as defined in Section 2.4.4.2.

The function of the screw is to provide a rigid attach method to sandwich the entire CEK assembly together, activating the CEK spring under the baseboard, and thus providing the TIM preload. A screw is an inexpensive, low profile solution that does not negatively impact the thermal performance of the heatsink due to air blockage. Any fastener (that is, head configuration) can be used as long as it is of steel construction; the head does not interfere with the heatsink fins, and is of the correct length of 20.64 mm [0.8125 in.].

Although the CEK heatsink fits into the legacy volumetric keep-in, it has a larger footprint due to the elimination of retention mechanism and clips used in the older enabled thermal/mechanical components. This allows the heatsink to grow its base and fin dimensions, further improving the thermal performance. A drawback of this enlarged size and use of copper for both the base and fins is the increased weight of the heatsink. The retention scheme employed by CEK is designed to support heavy heatsinks (approximately up to 1000 grams) in cases of shock, vibration and installation as explained in Appendix D. Some of the thermal and mechanical characteristics of the CEK heatsinks are shown in Table 2-8.

Table 2-8. CEK Heatsink Thermal Mechanical Characteristics

Size	Height	Weight	Target Airflow Through Fins	Mean Ψ_{ca}	Standard Deviation Ψ_{ca}	Pressure Drop
	(mm) [in.]	(kg) [lbs]	(m^3/hr) [CFM]	(°C/W)	(°C/W)	(Pa) [in H_2O]
2U+	50.08 [2.00]	1.0 [2.2]	45.9 [27]	0.207	0.0033	45.3 [0.182]
1U	20.64 [1.04]	0.53 [1.2]	25.5 [15]	0.270	0.0023	82.4 [0.331]

2.4.7.2 Thermal Interface Material (TIM)

A TIM must be applied between the package and the heatsink to ensure thermal conduction. The CEK reference design uses Shin-Etsu* G751 thermal grease.

The recommended grease dispense weight to ensure full coverage of the processor IHS is given below. For an alternate TIM, full coverage of the entire processor IHS is recommended.

Table 2-9. Recommended Thermal Grease Dispense Weight

Processor	Minimum	Maximum	Units	Notes
TIM Dispense weight		400	mg	Shin-Etsu* G751. Dispense weight is an approximate target.
Static compressive TIM loading provided by CEK	18 80	30 133	lbf N	Generated by the CEK reference solution. See Table Note below.

Note: For further information, refer to the LGA771 Socket Mechanical Design Guide for socket loading specifications.

It is recommended that you use thermally conductive grease. Thermally conductive grease requires special handling and dispense guidelines. The following guidelines apply to Shin-Etsu G751 thermal grease. For guidance with your specific application, please contact the vendor. Vendor information is provided in Appendix E. The use of a semi-automatic dispensing system is recommended for high volume assembly to ensure an accurate amount of grease is dispensed on top of the IHS prior to assembly of the heatsink. A typical dispense system consists of an air pressure and timing controller, a hand held output dispenser, and an actuation foot switch. Thermal grease in cartridge form is required for dispense system compatibility. A precision scale with an accuracy of ±5 mg is recommended to measure the correct dispense weight and set the corresponding air pressure and duration. The IHS surface should be free of foreign materials prior to grease dispense.

Additional recommendations include recalibrating the dispense controller settings after any two hour pause in grease dispense. The grease should be dispensed just prior to heatsink assembly to prevent any degradation in material performance. Finally, the thermal grease should be verified to be within its recommended shelf life before use.

The CEK reference solution is designed to apply a compressive load of up to 133 N [30 lbf] on the TIM to improve the thermal performance.

2.4.7.3 CEK Spring

The CEK spring, which is attached on the secondary side of the baseboard, is made from 0.80 mm [0.0315 in.] thick 301 stainless steel half hard. Any future versions of the spring will be made from a similar material. The CEK spring has four embosses which, when assembled, rest on the top of the chassis standoffs. The CEK spring is located between the chassis standoffs and the heatsink standoffs. The purpose of the CEK spring is to provide compressive preload at the TIM interface when the baseboard is pushed down upon it. This spring does not function as a clip of any kind. The two tabs on the spring are used to provide the necessary compressive preload for the TIM when the whole solution is assembled. The tabs make contact on the secondary side of the baseboard. In order to avoid damage to the contact locations on the baseboard, the tabs are insulated with a 0.127 mm [0.005 in.] thick Kapton* tape (or equivalent). Figure 2-25 shows an isometric view of the CEK spring design.

Figure 2-25. CEK Spring Isometric View

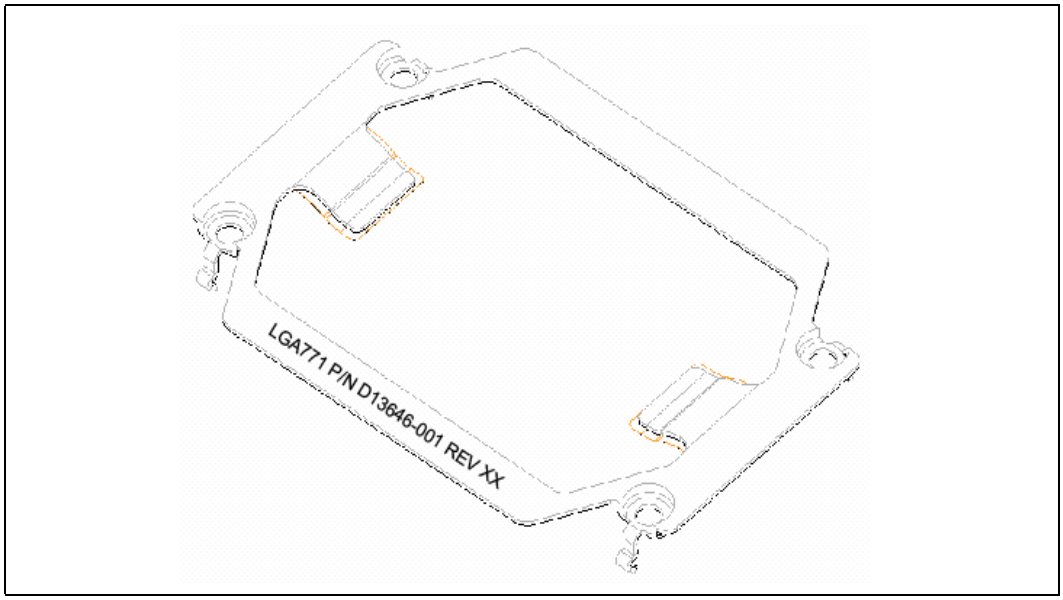
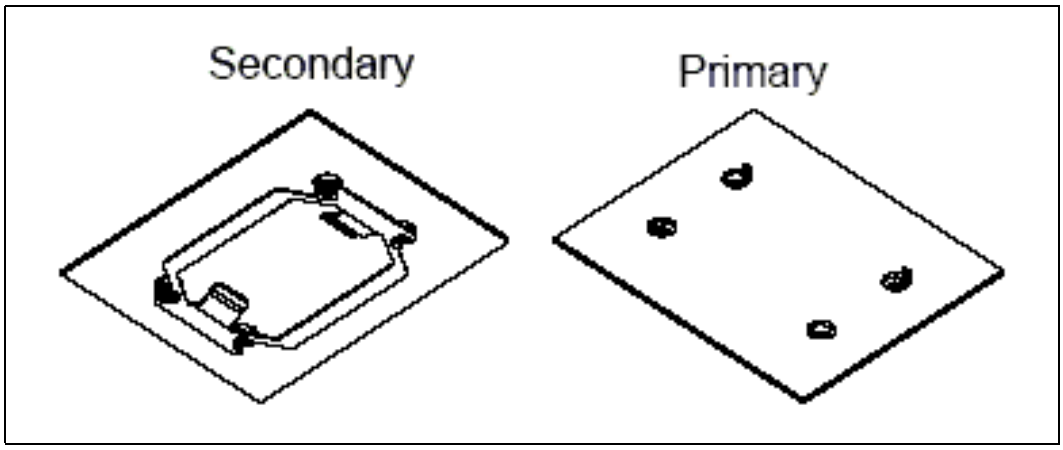


Figure 2-26. Isometric View of CEK Spring Attachment to the Base Board



Please refer to Appendix A for more detailed mechanical drawings of the CEK spring. Also, the baseboard keepout requirements shown in Appendix A must be met to use this CEK spring design.

2.4.8 Boxed Active Thermal Solution for the Dual-Core Intel® Xeon® Processor 5000 Series Processors

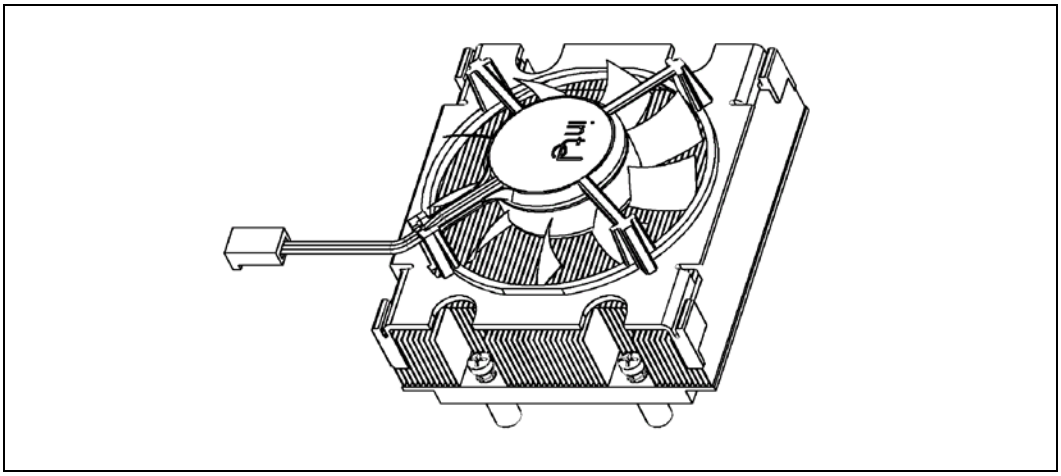
In addition to the 1U and 2U passive CEK heatsinks, Intel is developing an active heatsink solution. This heatsink solution is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present and side directional airflow is not an issue. All three heatsinks will be offered as part of boxed Dual-Core Intel Xeon Processor 5000 Series products. These solutions are intended for system integrators who build systems from components available through distribution channels. The retention solution used for these products is called the CEK. The CEK base is compatible with all three heatsink solutions.

Figure 2-27 provides a representation of the active CEK solution. This design is based on a 4-pin PWM/T-diode controlled active fan heatsink solution. PWM (Pulse Width Modulation also synonymous with Pulse Duration Modulation PDM) is a modulation in which the duration of pulse is varied in accordance with some characteristic of the modulating signal. This new solution is being offered to help provide better control over pedestal chassis acoustics. This is achieved though accurate measurement of processor temperature through the processor's temperature diode (T-diode). Fan RPM is modulated through the use an ASIC (Application Specific Integrated Circuit) located on the serverboard, that sends out a PWM control signal to the fourth pin of the connector labeled as **Control**. Detail information about 4-wire PWM fan implementation can be found in the *4-Wire Pulse Width Modulation (PWM) Controlled Fan Specification* from *www.formfactors.org.*

This heatsink solution also requires a constant +12 V supplied to pin 2 and does not support variable voltage control or 3-pin PWM control. If no PWM signal is detected on the fourth pin this heatsink solution will revert back to thermistor control mode, supporting both the 4-wire PWM and standard 3-wire ambient air control methods.

The solution is still under development at this time. Intel may make changes to specification and product descriptions at any time, without notice. The active heatsink solution will not exceed a mass of approximately 1050 grams. Note that this is per processor, so a dual processor system will have up to approximately 2100 grams total mass in the heatsinks. This large mass will require a minimum chassis stiffness to be met in order to withstand force during shock and vibration.

Figure 2-27. Boxed Active CEK Heatsink Solutions with PWM/T-diode Control (Representation Only)



Clearance is required around the heatsink to ensure unimpeded airflow for proper cooling. The physical baseboard keepout requirements for the active solution are the same as the passive CEK solution shown in Appendix A. Refer to Figure A-18 through Figure A-20 for additional details on the active CEK thermal solution volumetrics.

2.4.8.1 Fan Power Supply

The active heatsink includes a fan, which requires a +12 V power supply. Platforms must provide a matched fan power header to support the boxed processor. Table 2-10 contains specifications for the input and output signals at the heatsink fan connector.

The fan outputs a SENSE signal, an open-collector output, which pulses at a rate of two pulses per fan revolution. A baseboard pull-up resistor provides VCC to match the baseboard-mounted fan speed monitor requirements, if applicable. Use of the SENSE signal is optional. If the SENSE signal is not used, pin 3 of the connector should be tied to GND.

It is recommended that a 4-pin fan header be used on the baseboard, in addition to, a control ASIC that can send a PWM signal to the active fan heatsink solution on the fourth pin, at a nominal 25 KHz frequency. If a 3-pin CPU fan header is used instead, the active fan heatsink solution will revert back to an automatic ambient air temperature control mode.

The fan power header on the baseboard must be positioned to allow the fan heatsink power cable to reach it. The fan power header identification and location must be documented in the supplier's platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 177.8 mm [7 in.] from the center of the processor socket.

Table 2-10. Fan Specifications (Boxed 4-wire PWM/T-diode Heatsink Solution)

Description	Min	Typ Steady	Max Steady	Max Startup	Unit	Notes
+12V: 12 Volt Fan Power Supply	10.8	12	12	13.2	V	
IC: Fan Current Draw	N/A	1.25	1.25	1.7	A	
SENSE: SENSE Frequency	2	2	2	2	Pulses per fan revolution	1

Note: System board should pull this pin up to V_{CC} with a resistor.

Figure 2-28. Fan Cable Connection (Active CEK)

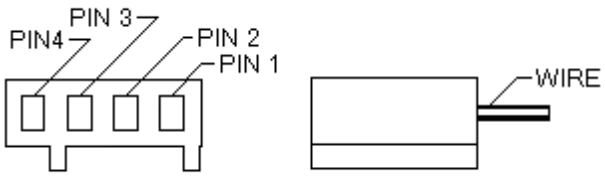


Table 2-11. Fan Cable Connector Pin Out (Active CEK)

Pin Number	Signal	Color
1	Ground (Constant)	Black
2	Power (+12V)	Yellow
3	Signal: 2 pulses per revolution	Green
4	Control	Blue

2.4.8.2 Systems Considerations Associated with the Active CEK

This heatsink was designed to help pedestal chassis users to meet the processor thermal requirements without the use of chassis ducting. It may be necessary to implement some form of chassis air guide or air duct to meet the T_{LA} temperature of 40°C depending on the pedestal chassis layout. Also, while the active heatsink solution is designed to mechanically fit into a 2U chassis, it may require additional space at the top of the heatsink to allow sufficient airflow into the heatsink fan. Therefore, additional

design criteria may need to be considered if this heatsink is used in a 2U rack mount chassis, or in a chassis that has drive bay obstructions above the inlet to the fan heatsink.

Thermal Profile A should be used to help determine the thermal performance of the platform. The primary recommended control method for this solution is using pulse width modulation control. This control method requires the motherboard provide the correct PWM duty cycle to the active fan heatsink solution to properly follow the thermal profile. If no PWM signal is detected the active heatsink solution will default back to a thermistor controlled mode and the fan will automatically adjust fan RPM to meet the thermal profile.

It is critical to supply a constant +12 V to the fan header so that the active CEK heatsink solution can operate properly. If a system board has a jumper setting to select either a constant +12 V power to the fan header or a variable voltage, it is strongly recommended that the jumper be set by default to the constant +12 V setting.

It is recommended that the ambient air temperature outside of the chassis be kept at or below 35°C. The air passing directly over the processor heatsink should not be preheated by other system components. Meeting the processor's temperature specification is the responsibility of the system integrator.

2.4.8.3 Boxed Processor Contents

A direct chassis attach method must be used to avoid problems related to shock and vibration, due to the weight of the heatsink required to cool the processor. The board must not bend beyond specification in order to avoid damage. The boxed processor contains the components necessary to solve both issues. The boxed processor will include the following items:

- Dual-Core Intel Xeon Processor 5000 Series processor
- Unattached heatsink solution
- Four screws, four springs, and four heatsink standoffs (all captive to the heatsink)
- Thermal Interface Material (pre-applied on heatsink)
- Installation Manual
- Intel Inside® logo

The other items listed in Figure 2-15 that are required to complete this solution will be shipped with either the chassis or boards. They are as follows:

- CEK Spring (supplied by baseboard vendors)
- Heatsink standoffs (supplied by chassis vendors)

§

A Mechanical Drawings

The mechanical drawings included in this appendix refer to the thermal mechanical enabling components for the Dual-Core Intel Xeon Processor 5000 Series.

Note: Intel reserves the right to make changes and modifications to the design as necessary.

Table A-1. Mechanical Drawing List

Drawing Description	Figure Number
"2U CEK Heatsink (Sheet 1 of 4)"	Figure A-1
"2U CEK Heatsink (Sheet 2 of 4)"	Figure A-2
"2U CEK Heatsink (Sheet 3 of 4)"	Figure A-3
"2U CEK Heatsink (Sheet 4 of 4)"	Figure A-4
"CEK Spring (Sheet 1 of 3)"	Figure A-5
"CEK Spring (Sheet 2 of 3)"	Figure A-6
"CEK Spring (Sheet 3 of 3)"	Figure A-7
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)"	Figure A-8
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)"	Figure A-9
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)"	Figure A-10
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)"	Figure A-11
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)"	Figure A-12
"Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)"	Figure A-13
"1U CEK Heatsink (Sheet 1 of 4)"	Figure A-14
"1U CEK Heatsink (Sheet 2 of 4)"	Figure A-15
"1U CEK Heatsink (Sheet 3 of 4)"	Figure A-16
"1U CEK Heatsink (Sheet 4 of 4)"	Figure A-17
"Active CEK Thermal Solution Volumetric (Sheet 1 of 3)"	Figure A-18
"Active CEK Thermal Solution Volumetric (Sheet 2 of 3)"	Figure A-19
"Active CEK Thermal Solution Volumetric (Sheet 3 of 3)"	Figure A-20

Figure A-1. 2U CEK Heatsink (Sheet 1 of 4)

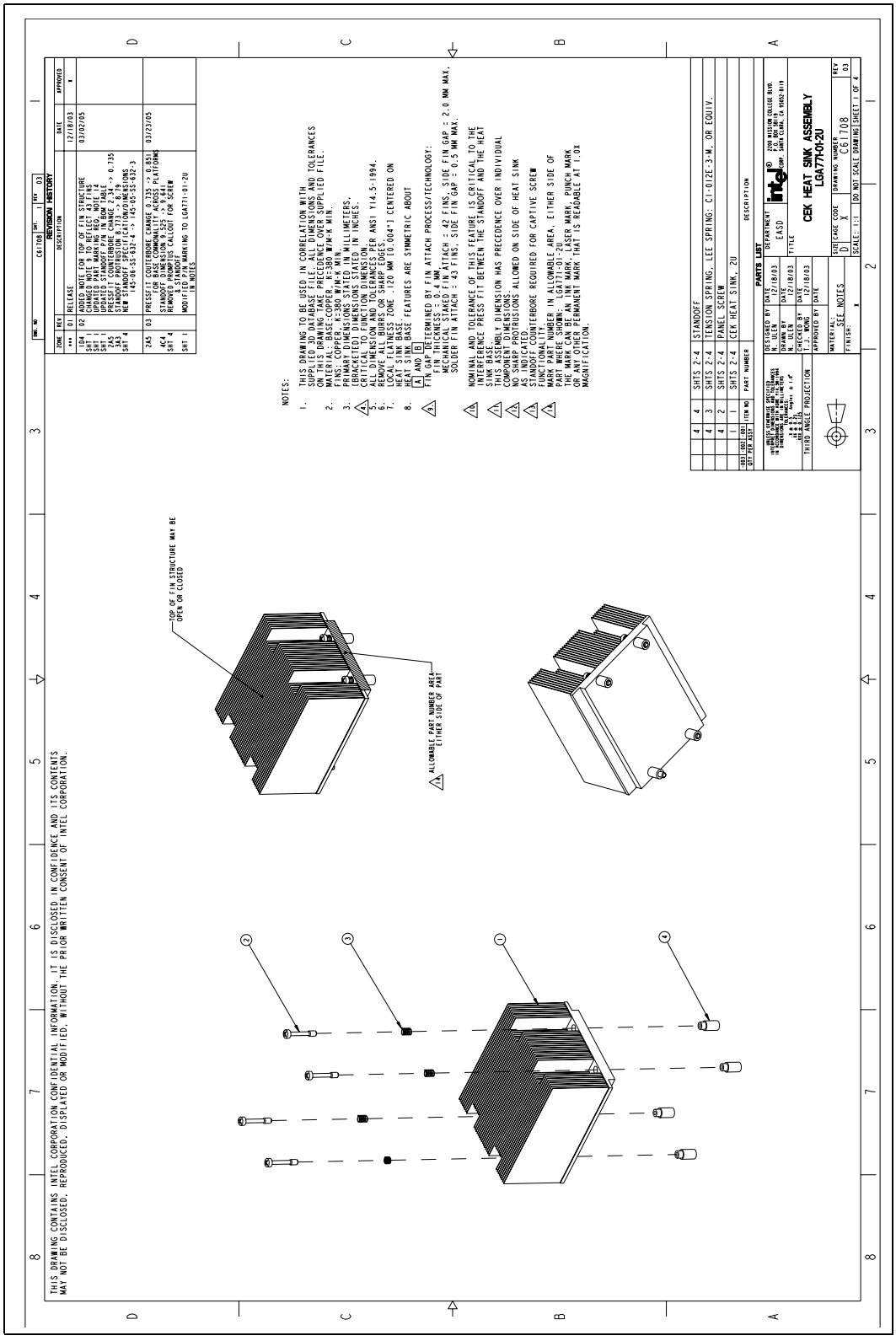


Figure A-2. 2U CEK Heatsink (Sheet 2 of 4)

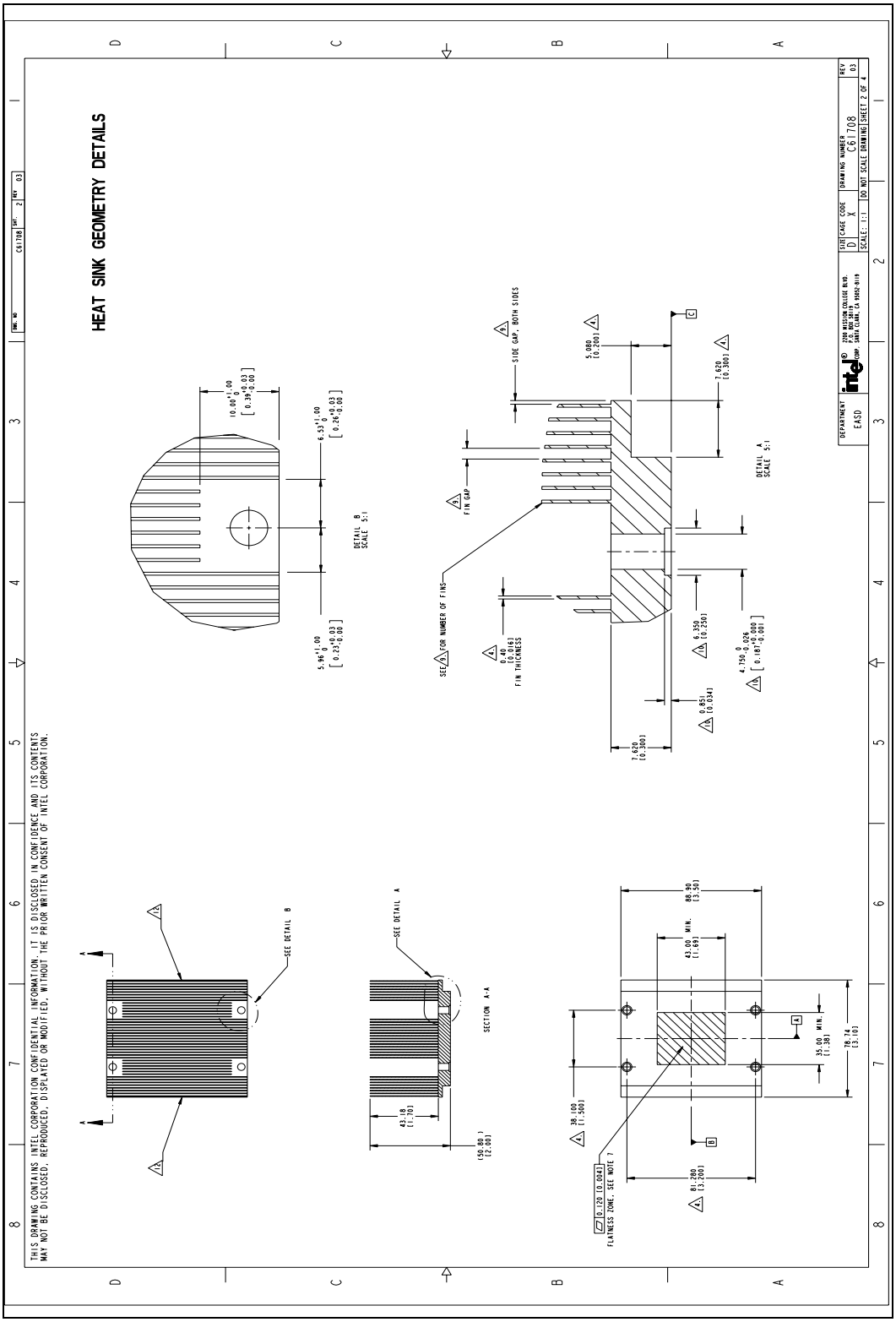


Figure A-3. 2U CEK Heatsink (Sheet 3 of 4)

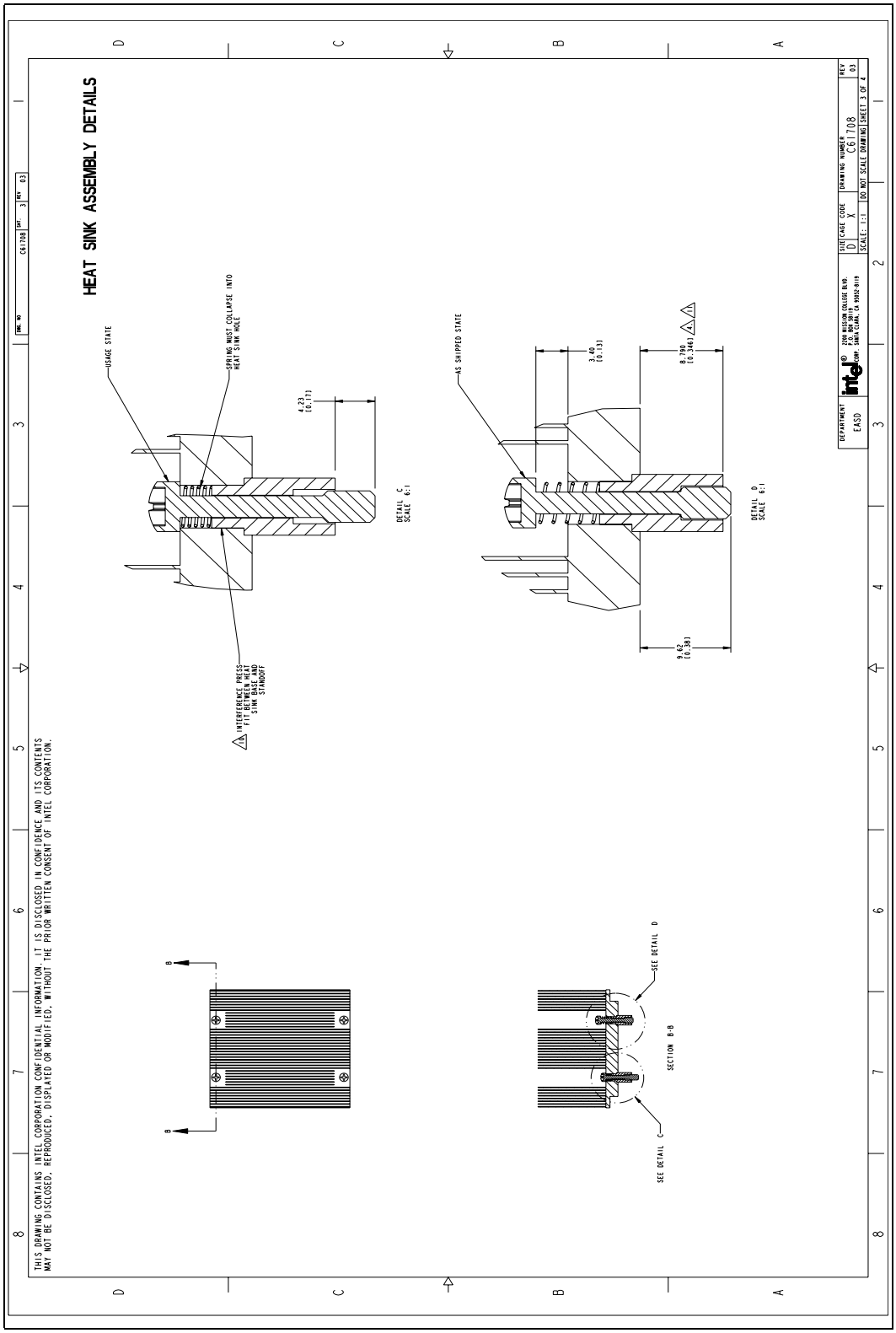


Figure A-4. 2U CEK Heatsink (Sheet 4 of 4)

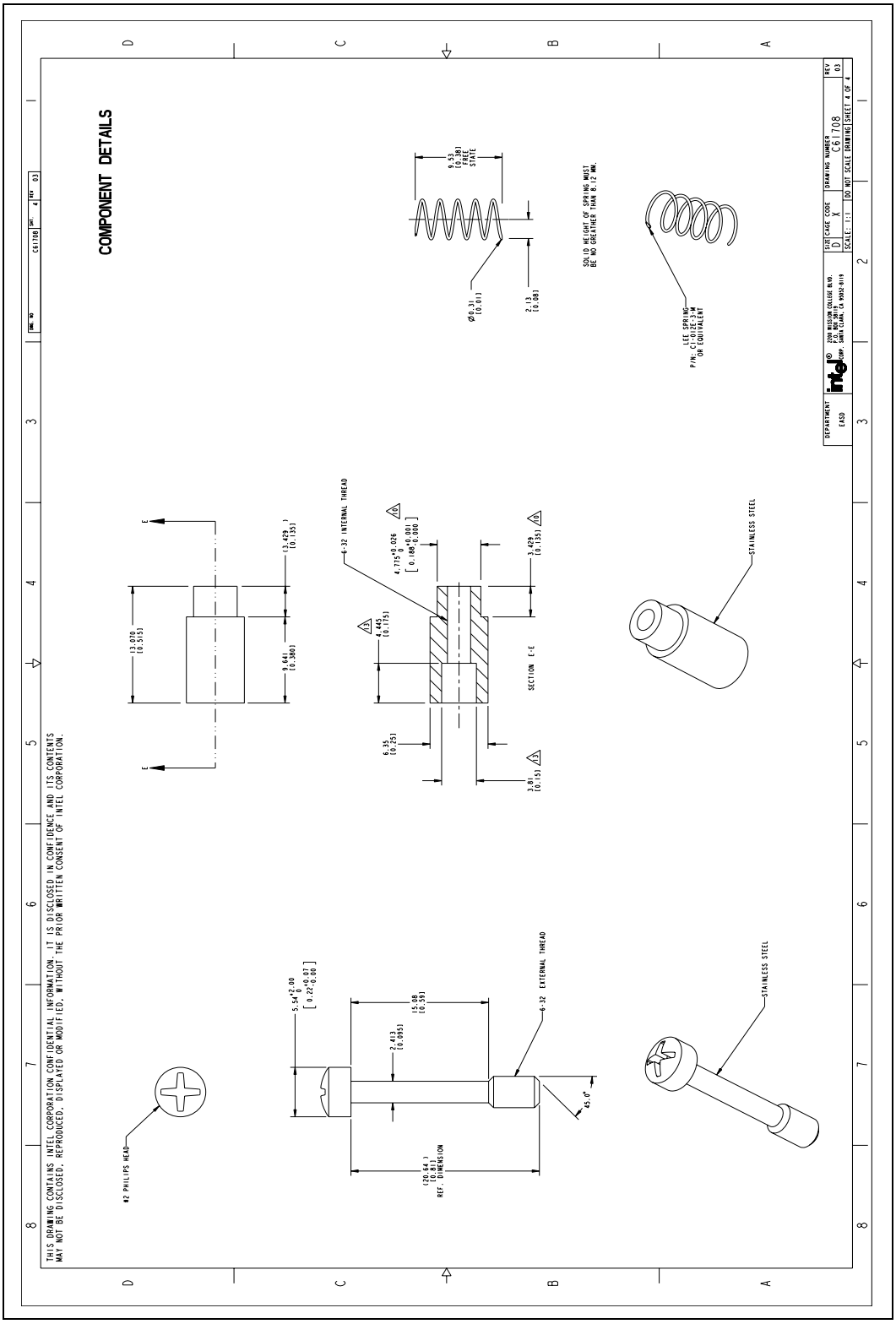


Figure A-5. CEK Spring (Sheet 1 of 3)

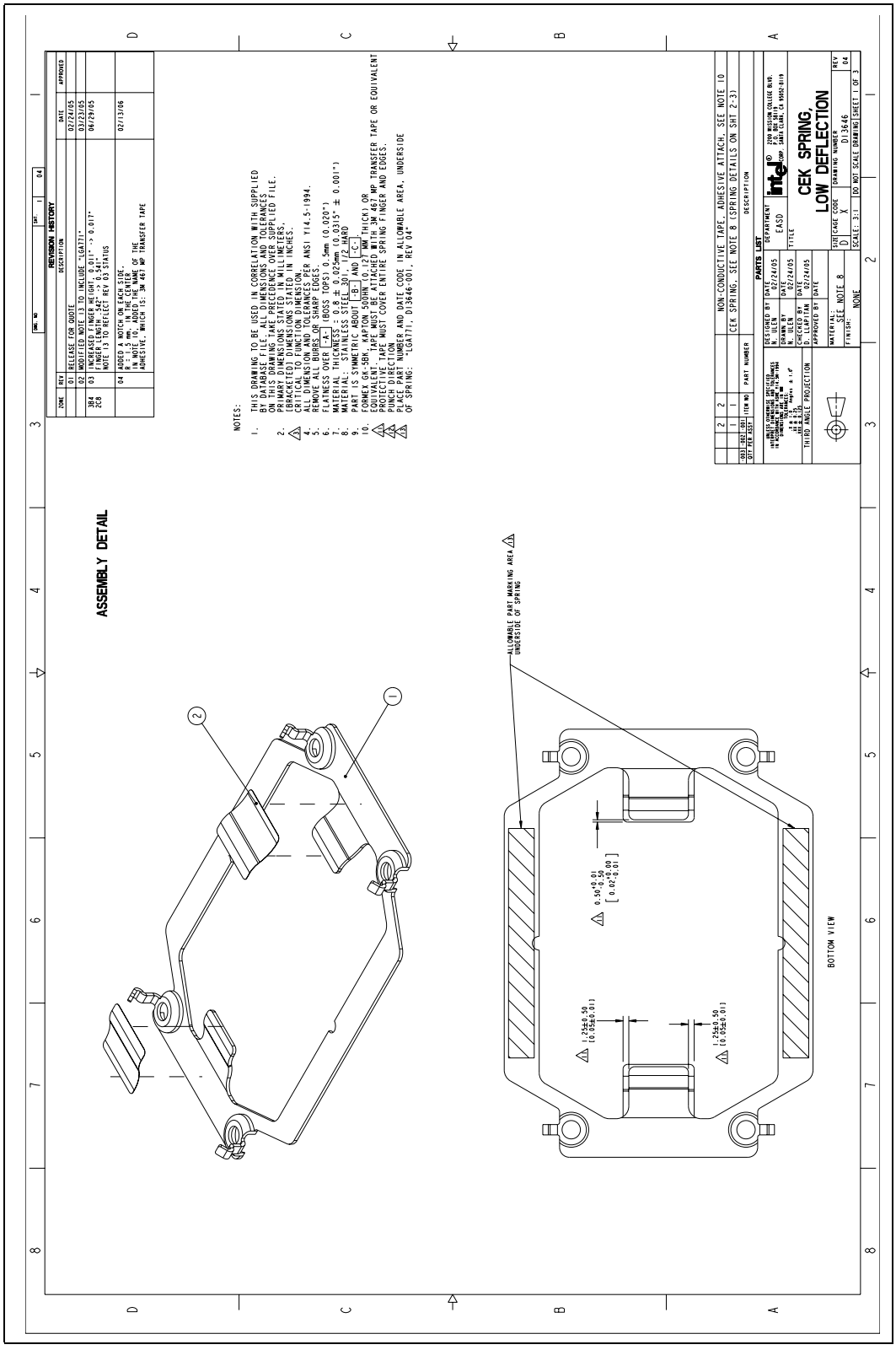
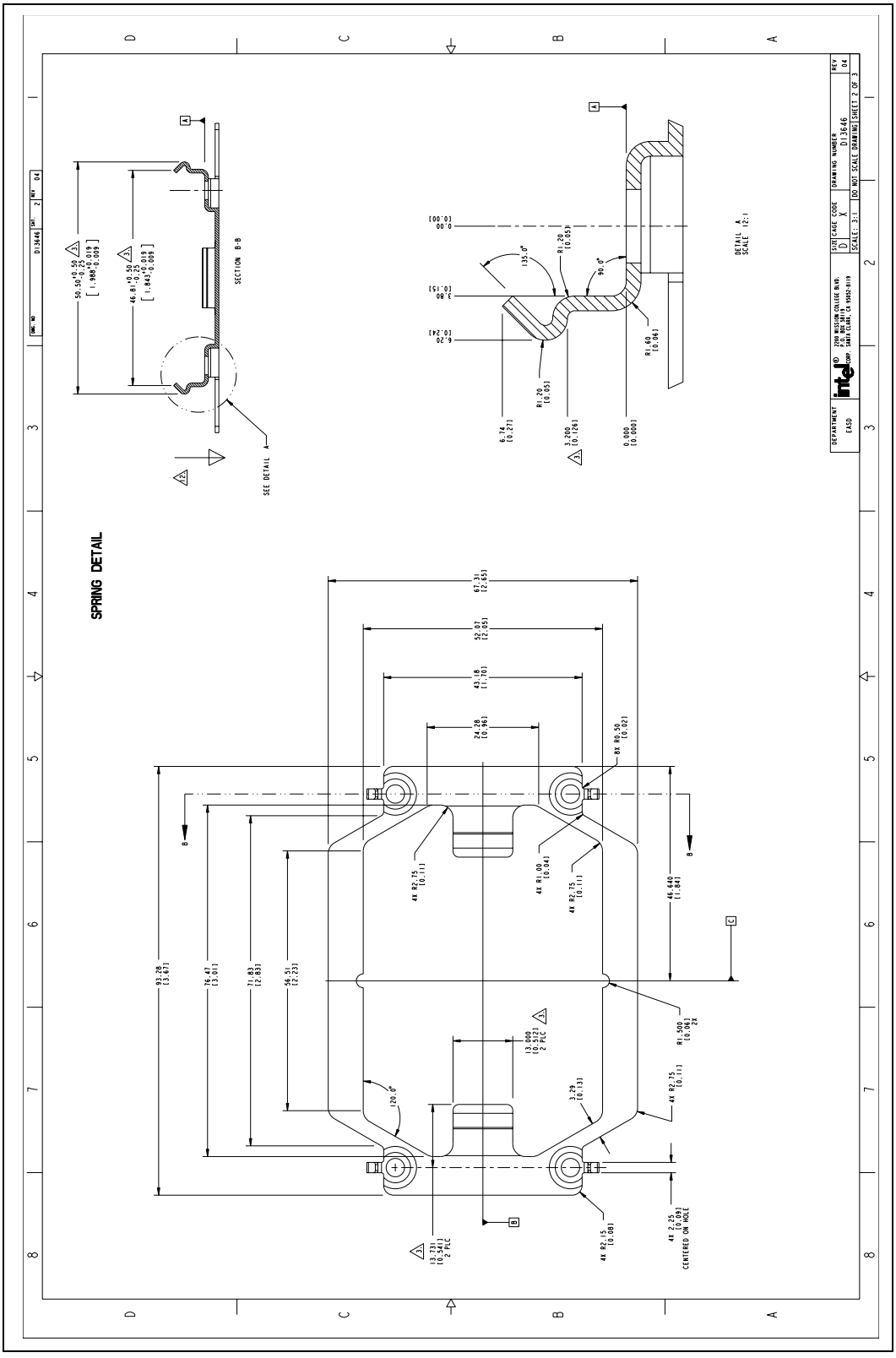


Figure A-6. CEK Spring (Sheet 2 of 3)



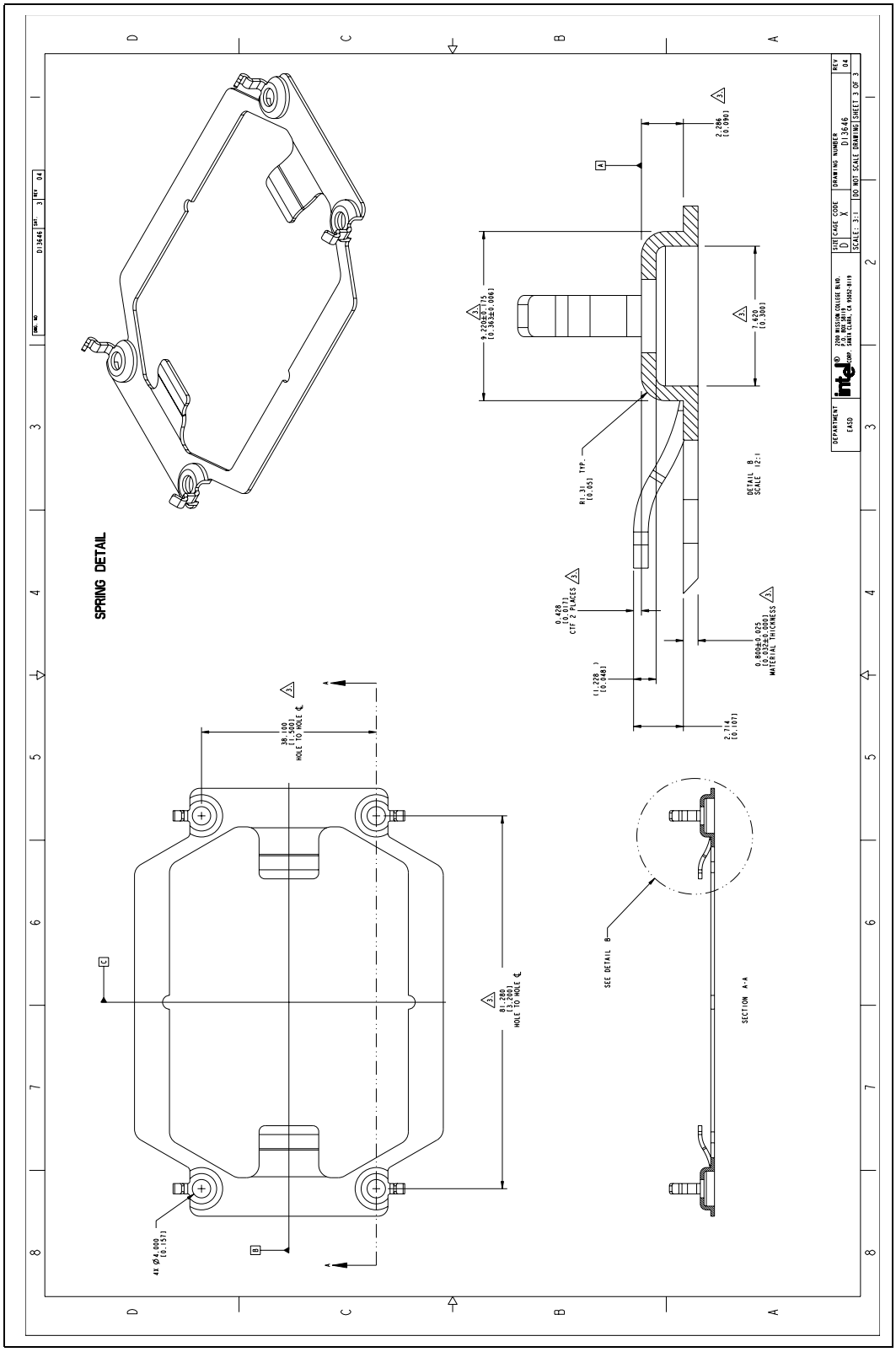


Figure A-7. CEK Spring (Sheet 3 of 3)

Figure A-8. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 1 of 6)

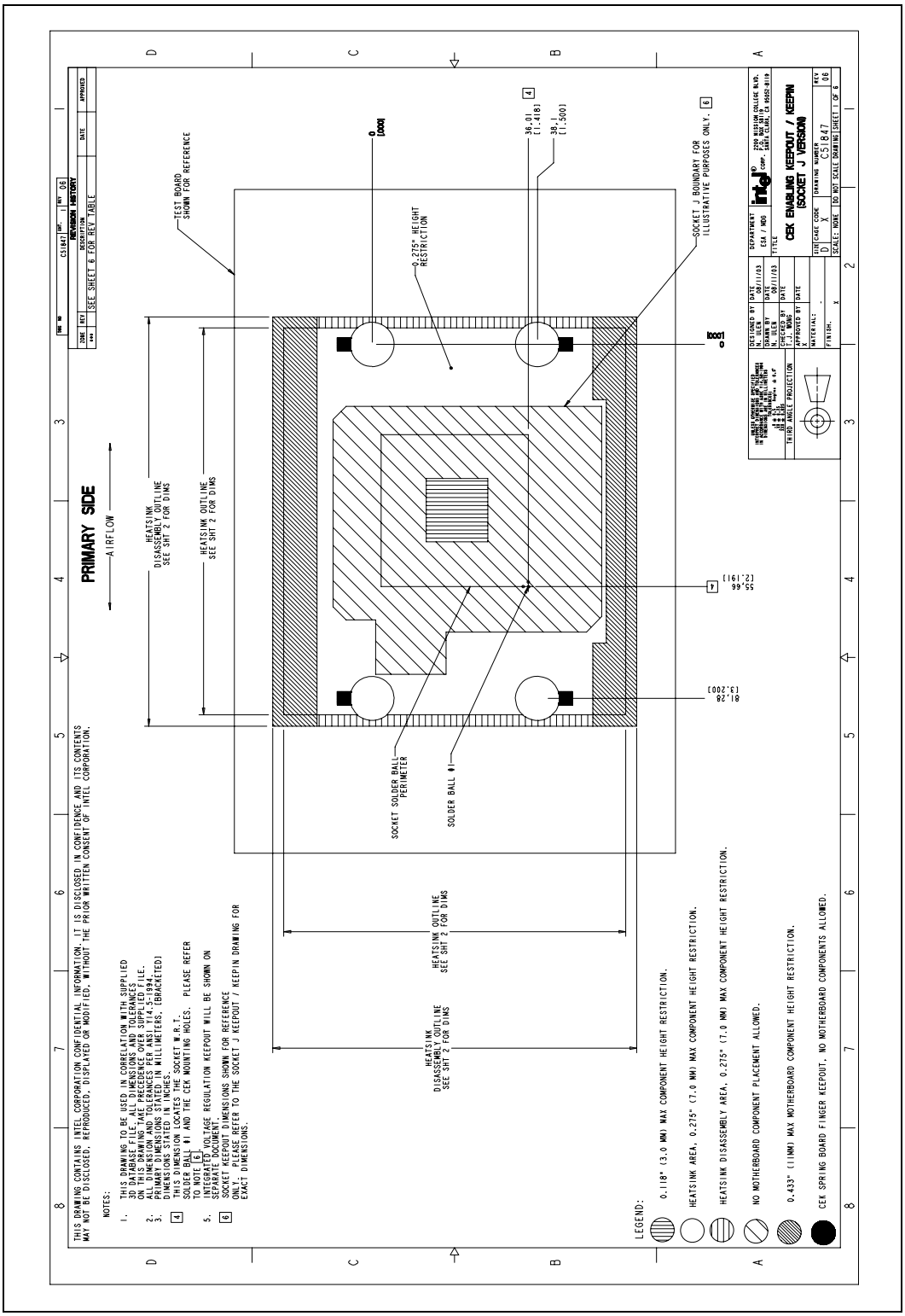


Figure A-9. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 2 of 6)

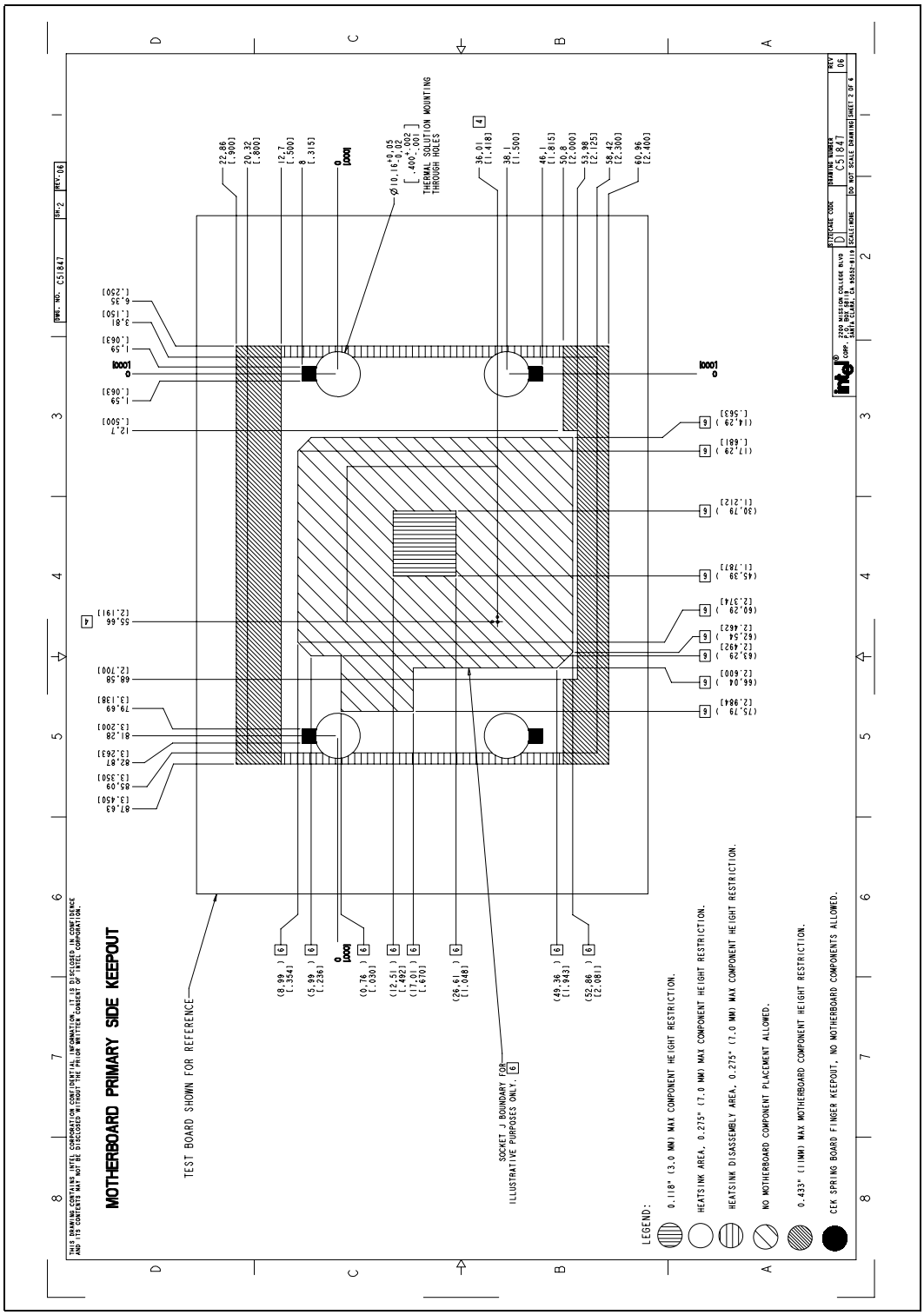


Figure A-10. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 3 of 6)

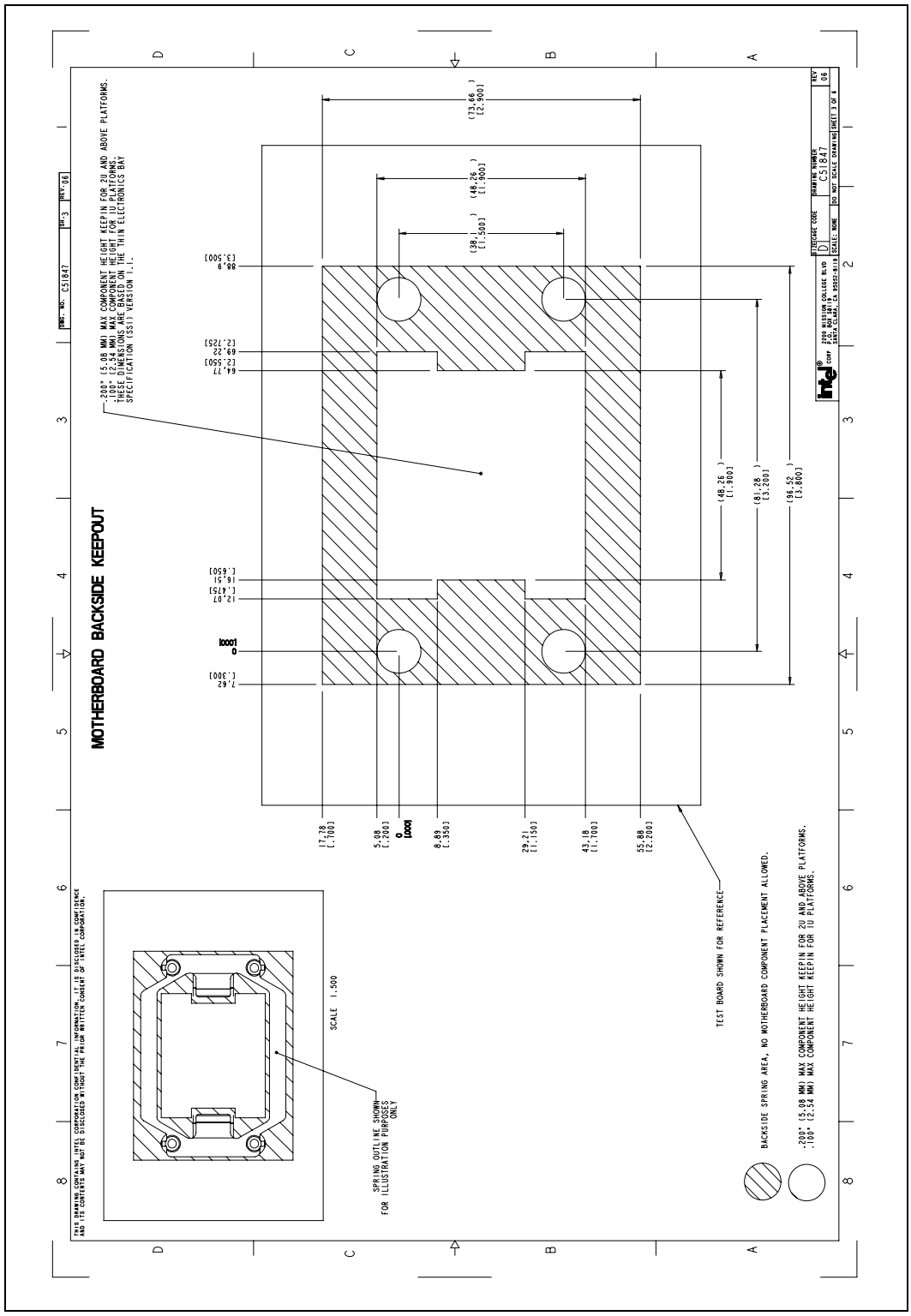


Figure A-11. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 4 of 6)

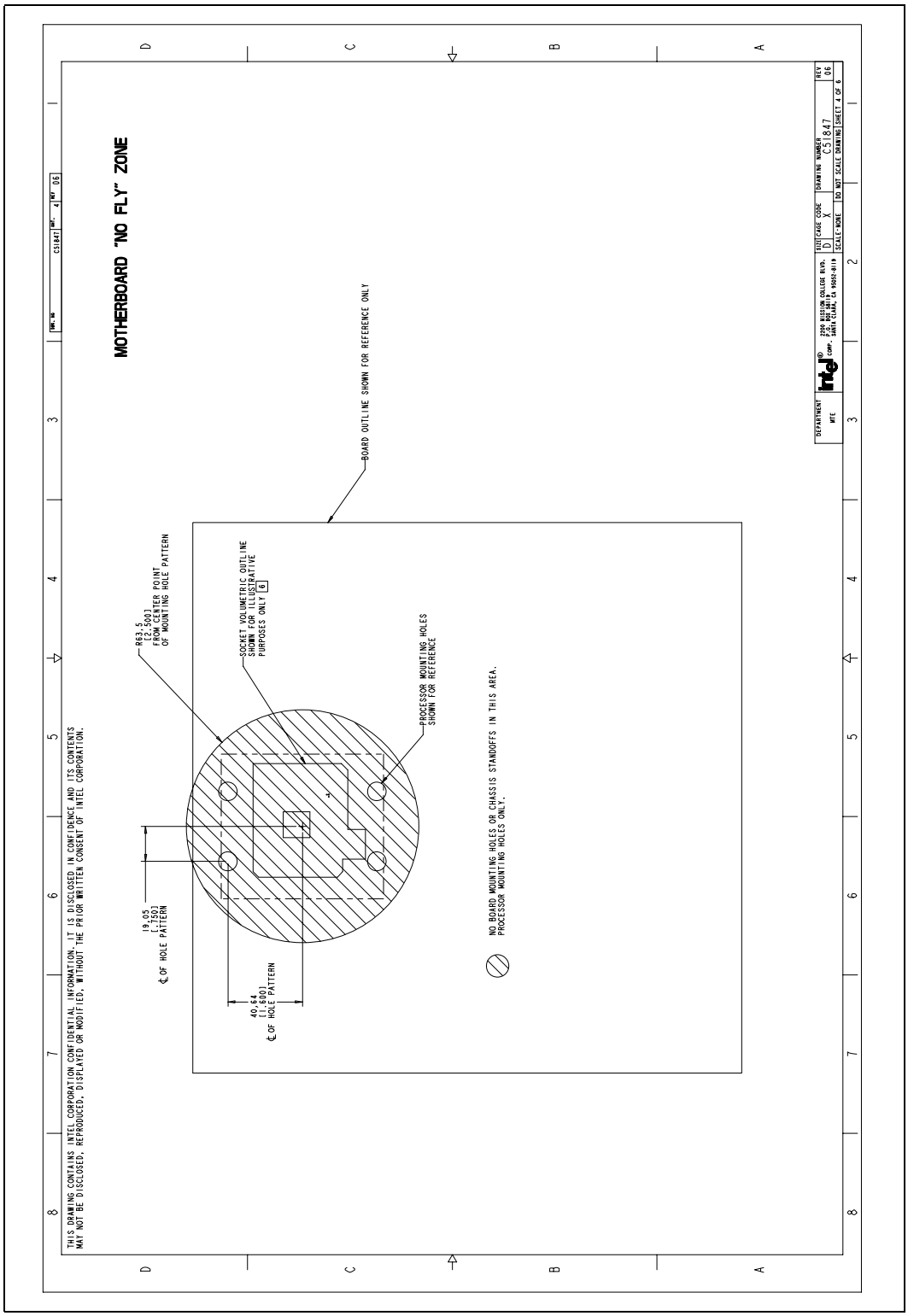


Figure A-12. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 5 of 6)

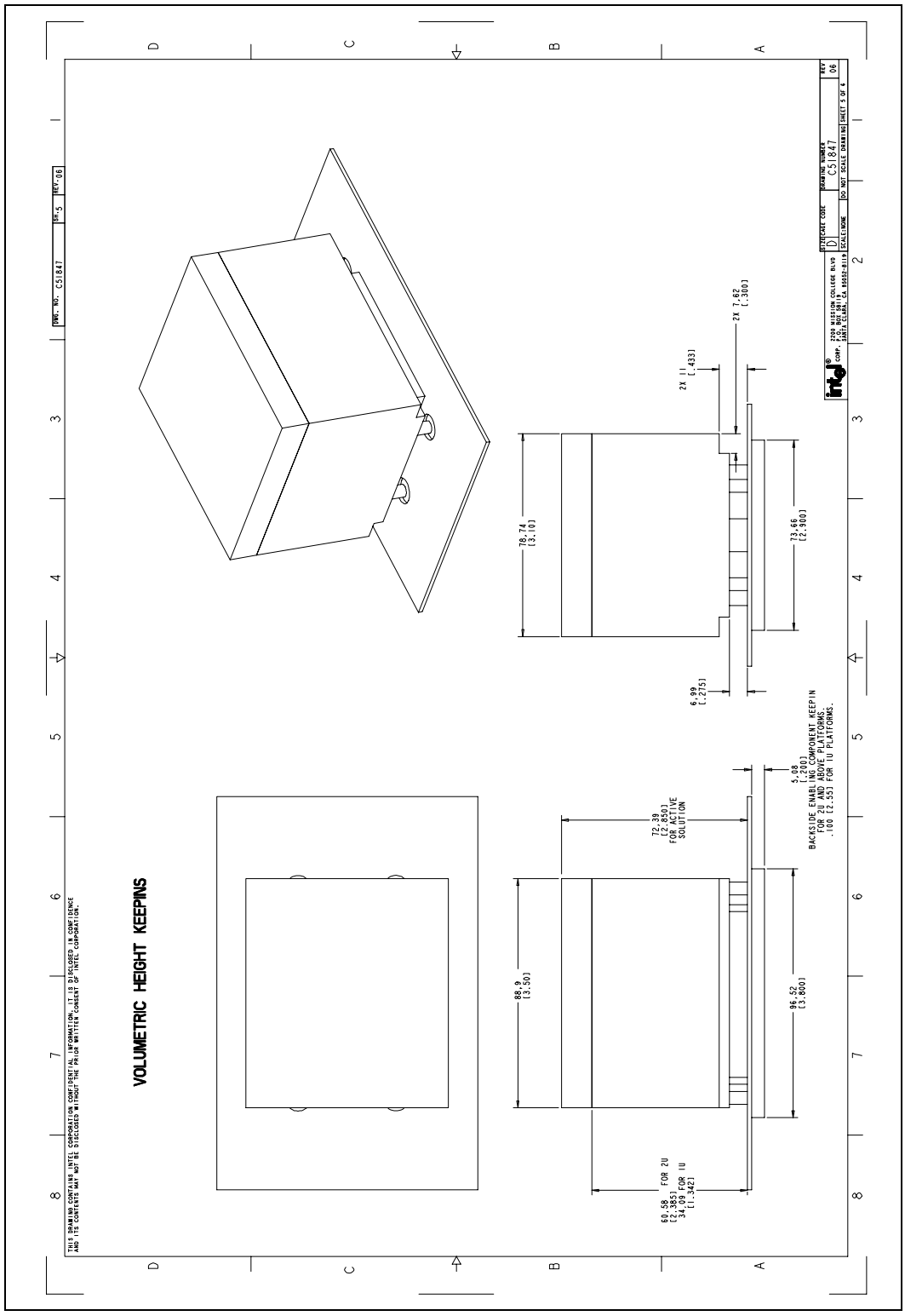


Figure A-13. Baseboard Keepout Footprint Definition and Height Restrictions for Enabling Components (Sheet 6 of 6)

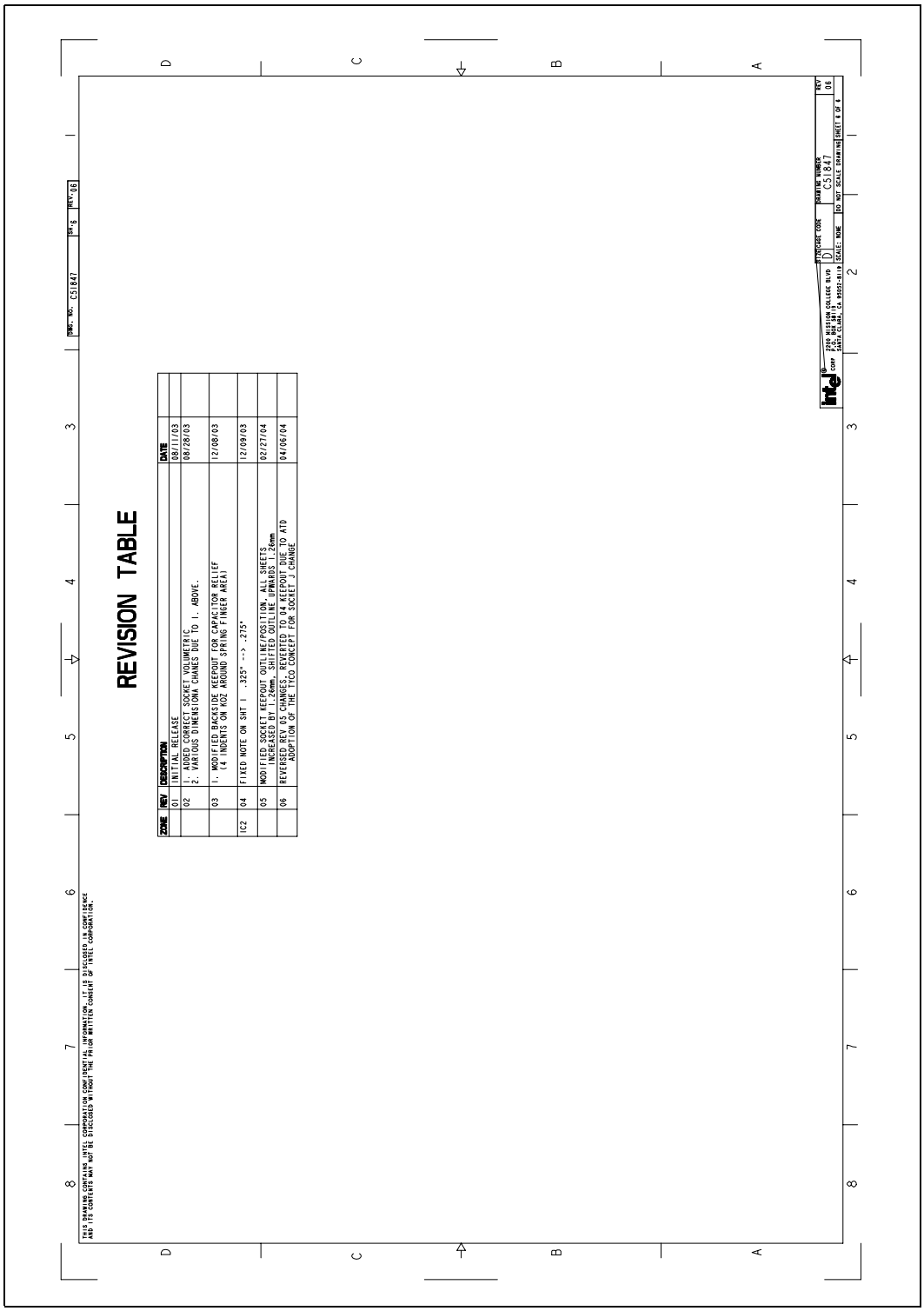
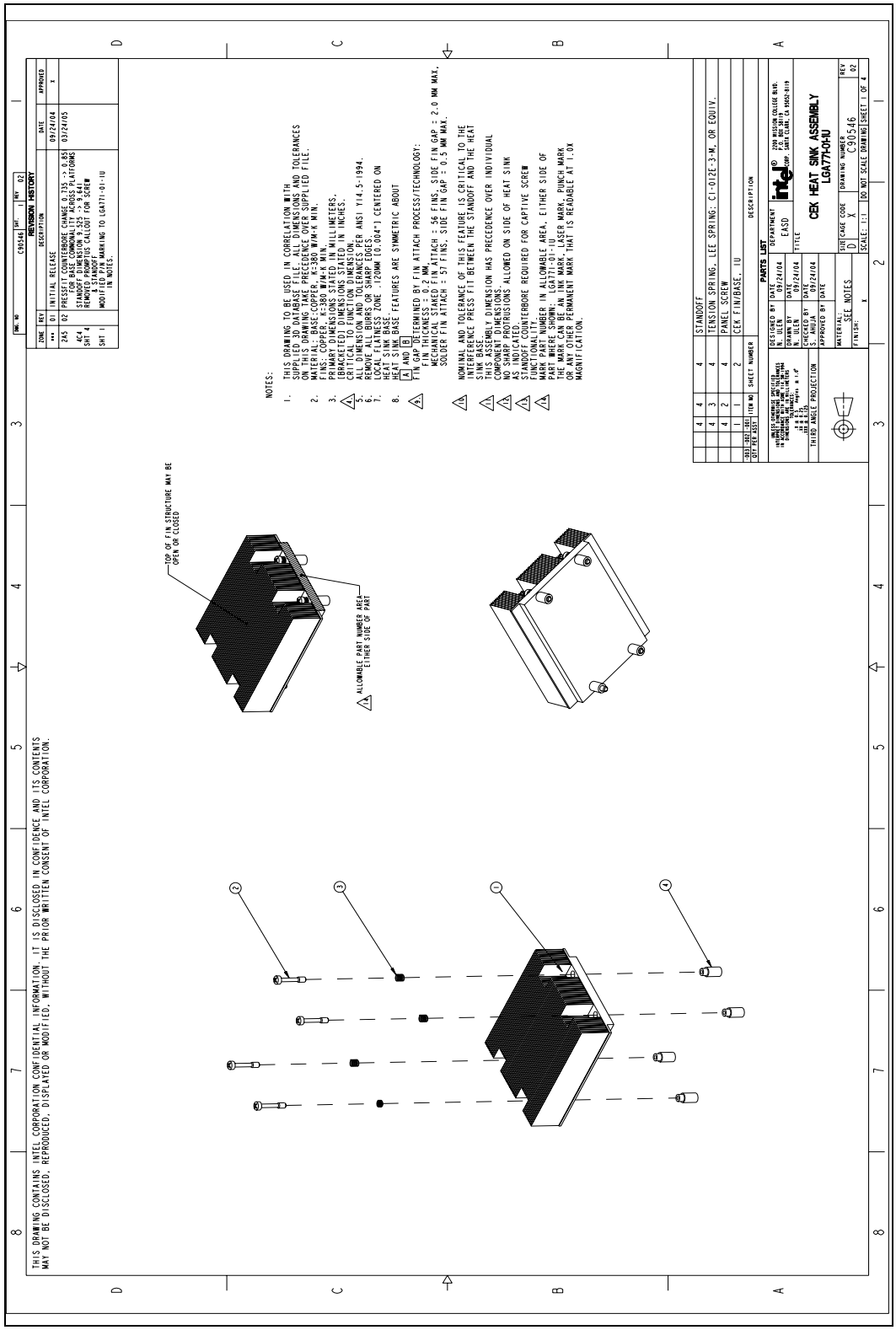


Figure A-14. 1U CEK Heatsink (Sheet 1 of 4)



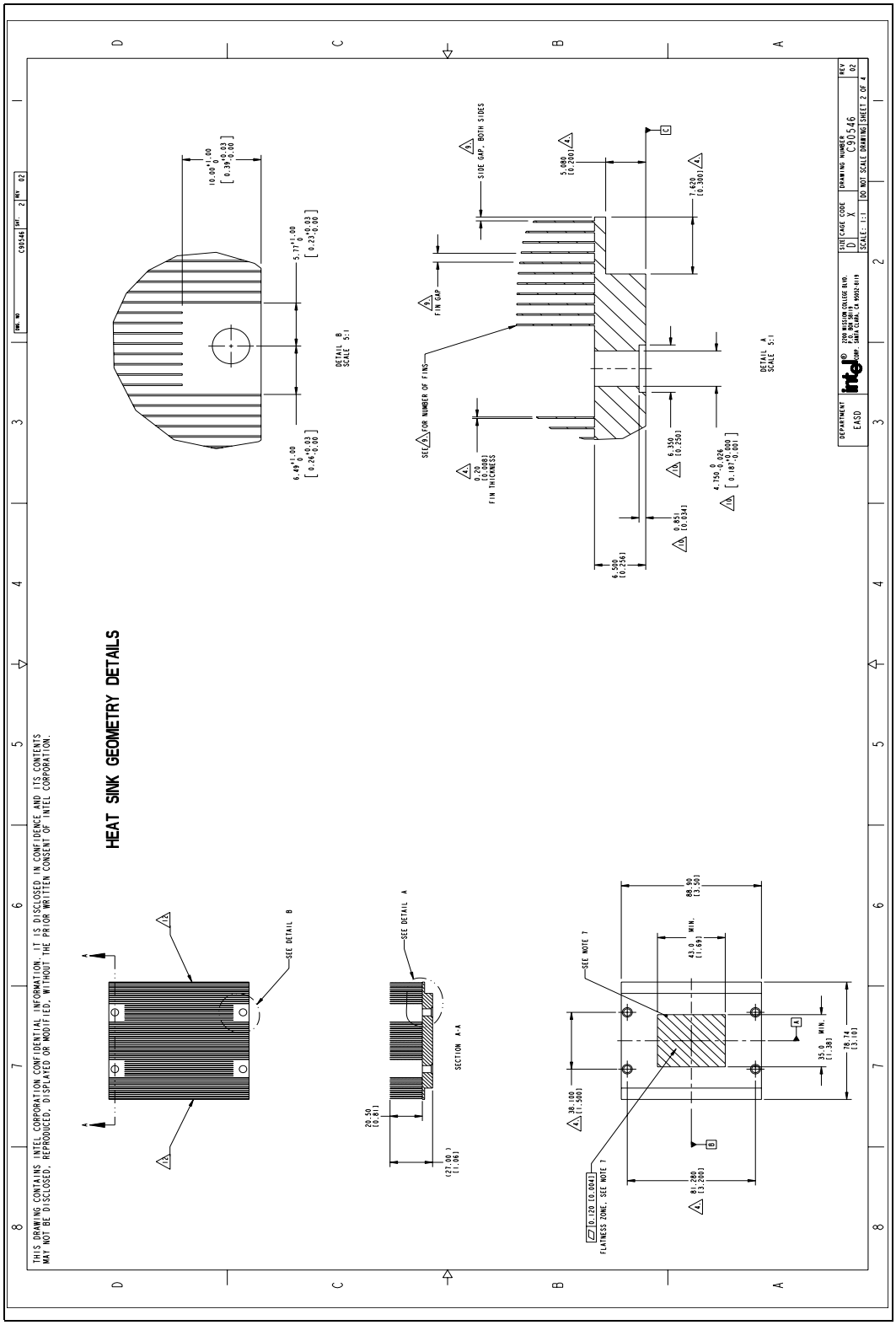

HEAT SINK GEOMETRY DETAILS
THIS DRAWING CONTAINS INTEL CORPORATION CONFIDENTIAL INFORMATION. IT IS DISCLOSED IN CONFIDENCE AND ITS CONTENTS MAY NOT BE DISCLOSED, REPRODUCED, DISPLAYED OR MODIFIED, WITHOUT THE PRIOR WRITTEN CONSENT OF INTEL CORPORATION.
DETAIL B SCALE 5:1
DETAIL A SCALE 5:1
SIDE GAP, BOTH SIDES
FIN GAP
SEE FOR NUMBER OF FINS
FIN THICKNESS
SEE DETAIL B
SEE DETAIL A
SECTION A-A
SEE NOTE 7
FLATNESS ZONE, SEE NOTE 7
DRAWING NUMBER
REV
SHEET 2 OF 4
DO NOT SCALE DRAWING
DEPARTMENT
EASD

Figure A-16. 1U CEK Heatsink (Sheet 3 of 4)

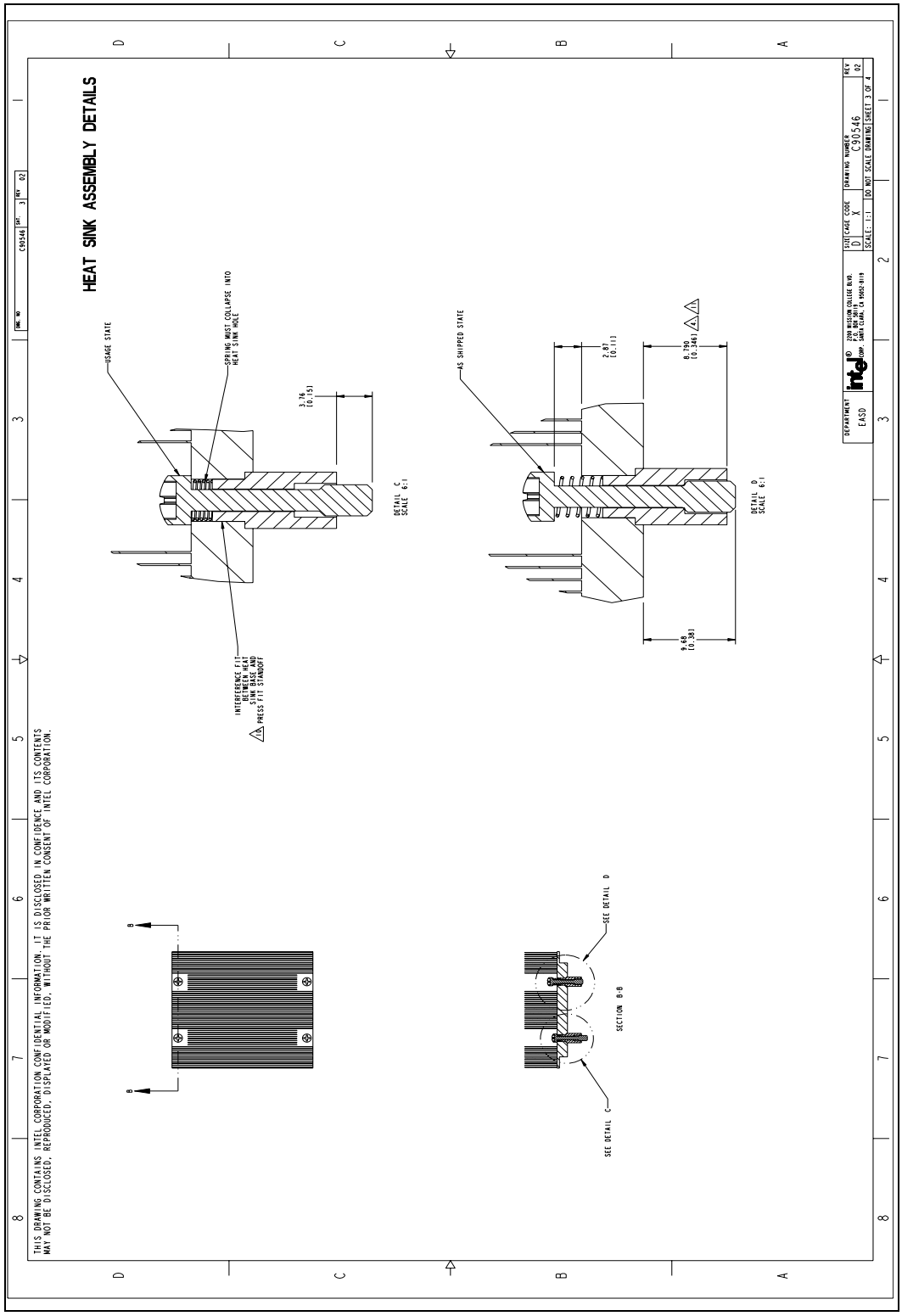


Figure A-17. 1U CEK Heatsink (Sheet 4 of 4)

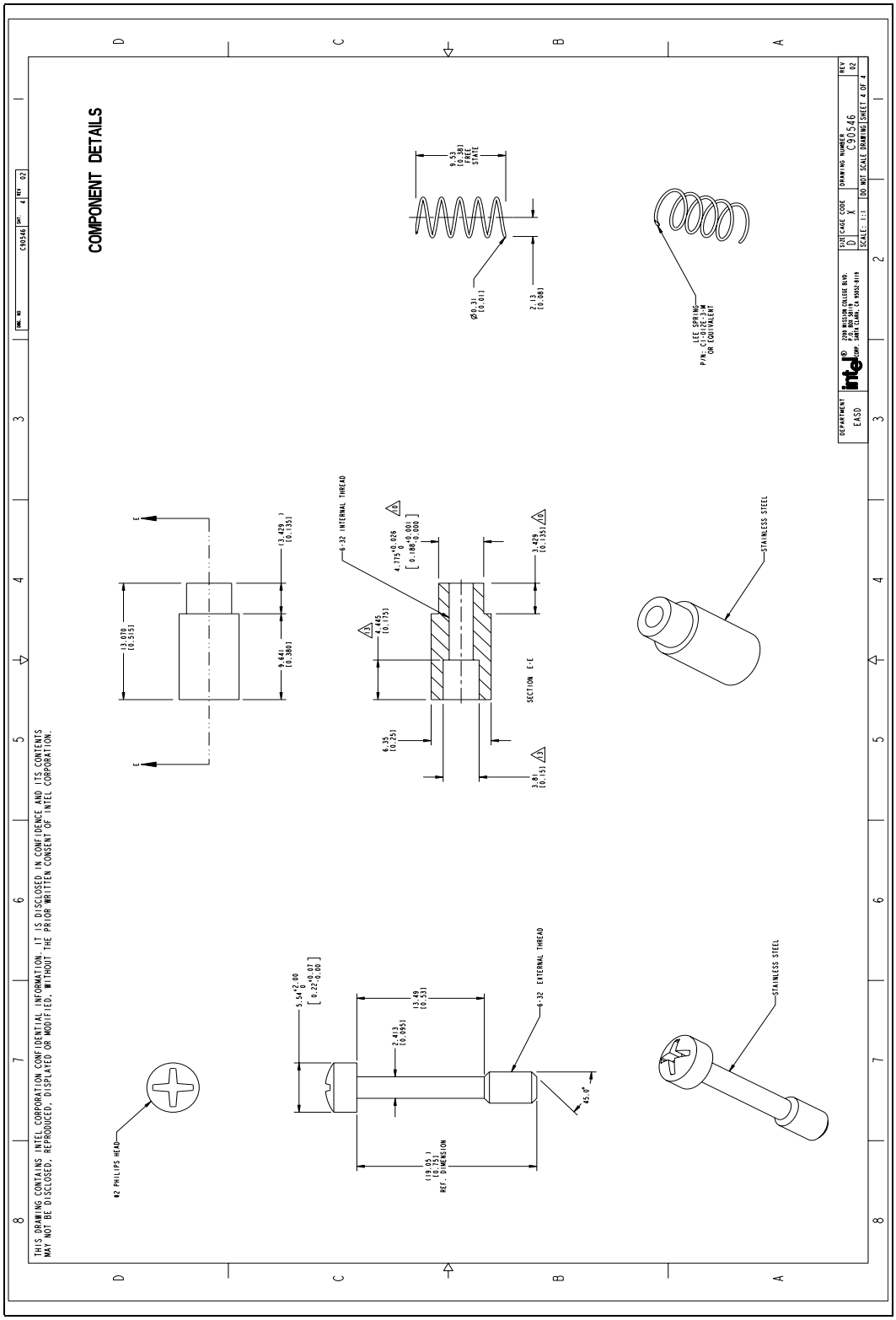


Figure A-18. Active CEK Thermal Solution Volumetric (Sheet 1 of 3)

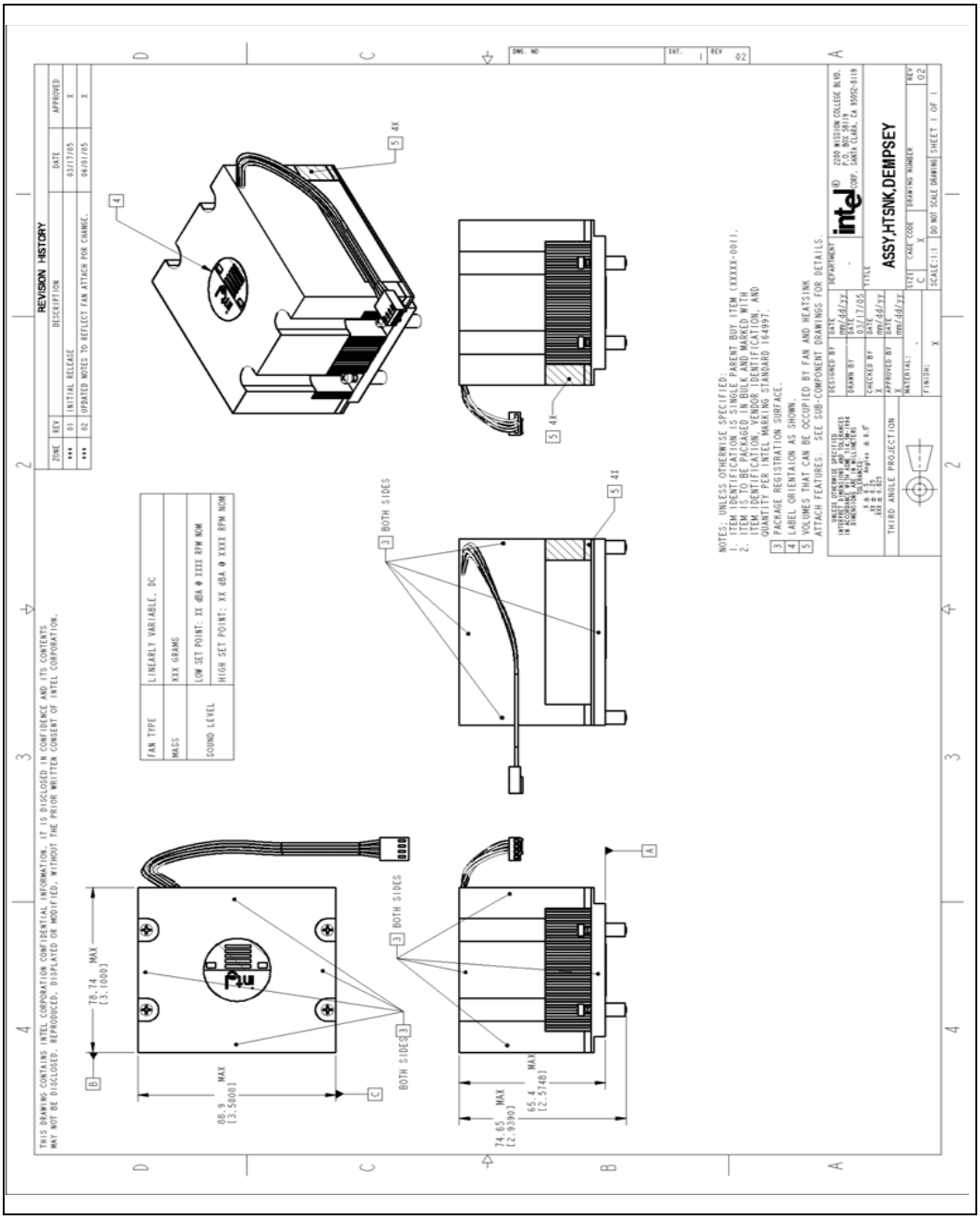


Figure A-19. Active CEK Thermal Solution Volumetric (Sheet 2 of 3)

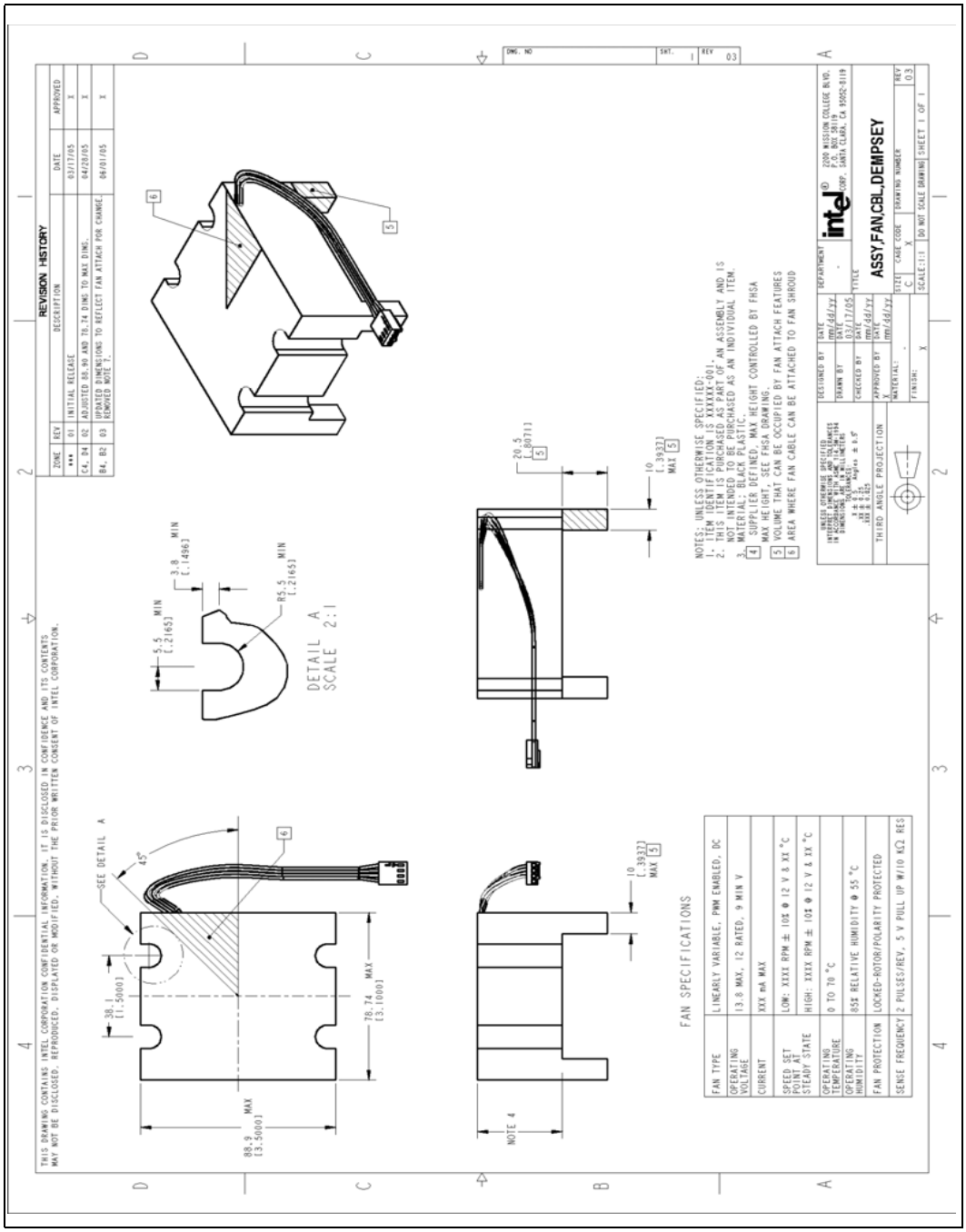
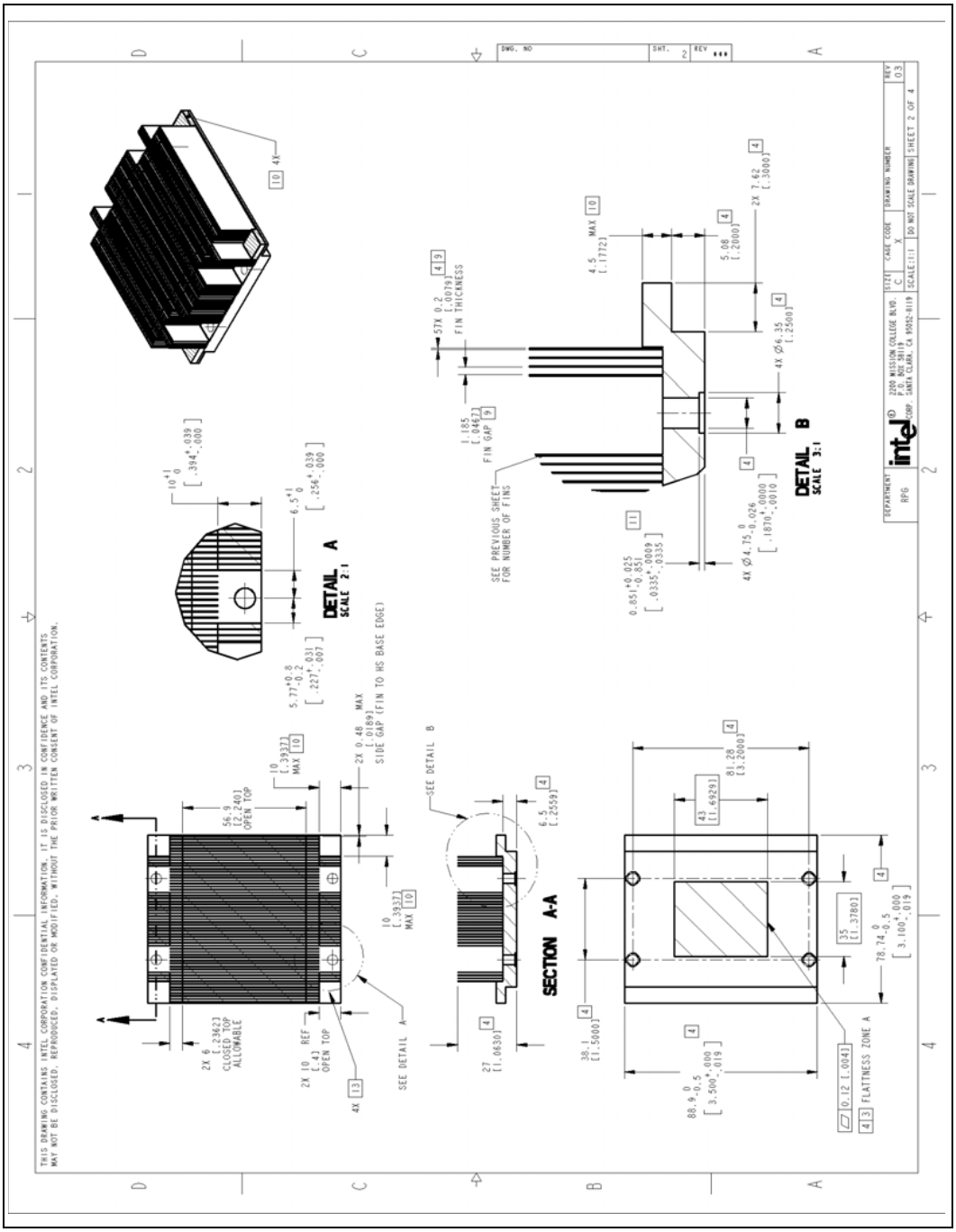


Figure A-20. Active CEK Thermal Solution Volumetric (Sheet 3 of 3)



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B Heatsink Clip Load Methodology

B.1 Overview

This section describes a procedure for measuring the load applied by the heatsink/clip/fastener assembly on a processor package.

This procedure is recommended to verify the preload is within the design target range for a design, and in different situations. For example:

- Heatsink preload for the LGA771 socket.
- Quantify preload degradation under bake conditions.

Note: This document reflects the current metrology used by Intel. Intel is continuously exploring new ways to improve metrology. Updates will be provided later as this document is revised as appropriate.

B.2 Test Preparation

B.2.1 Heatsink Preparation

Three load cells are assembled into the base of the heatsink under test, in the area interfacing with the processor Integrated Heat Spreader (IHS), using load cells equivalent to those listed in Section B.2.2.

To install the load cells, machine a pocket in the heatsink base, as shown in Figure B-1 and Figure B-2. The load cells should be distributed evenly, as close as possible to the pocket walls. Apply wax around the circumference of each load cell and the surface of the pocket around each cell to maintain the load cells in place during the heatsink installation on the processor and motherboard.

The depth of the pocket depends on the height of the load cell used for the test. It is necessary that the load cells protrude out of the heatsink base. However, this protrusion should be kept minimal, as it will create an additional load offset since the heatsink base is artificially raised. The measurement load offset depends on the whole assembly stiffness (that is, motherboard, clip, fastener, and so on). For example, the Dual-Core Intel Xeon Processor 5000 Series CEK Reference Heatsink Design clip and fasteners assembly have a stiffness of around 160 N/mm [915 lb/in]. If the resulting protrusion is 0.038 mm [0.0015”], then a extra load of 6.08 N [1.37 lb] will be created, and will need to be subtracted from the measured load. Figure B-3 shows an example using the Dual-Core Intel Xeon Processor 5000 Series CEK Reference Heatsink designed for the Dual-Core Intel Xeon Processor 5000 Series in the 771–land LGA package.

Note: When optimizing the heatsink pocket depth, the variation of the load cell height should also be taken into account to make sure that all load cells protrude equally from the heatsink base. It may be useful to screen the load cells prior to installation to minimize variation.

Alternate Heatsink Sample Preparation

As just mentioned, making sure that the load cells have minimum protrusion out of the heatsink base is paramount to meaningful results. An alternate method to make sure that the test setup will measure loads representative of the non-modified design is:

- Machine the pocket in the heatsink base to a depth such that the tips of the load cells are just flush with the heatsink base.
- Then machine back the heatsink base by around 0.25 mm [0.01”], so that the load cell tips protrude beyond the base.

Proceeding this way, the original stack height of the heatsink assembly should be preserved. This should not affect the stiffness of the heatsink significantly.

Figure B-1. Load Cell Installation in Machined Heatsink Base Pocket – Bottom View

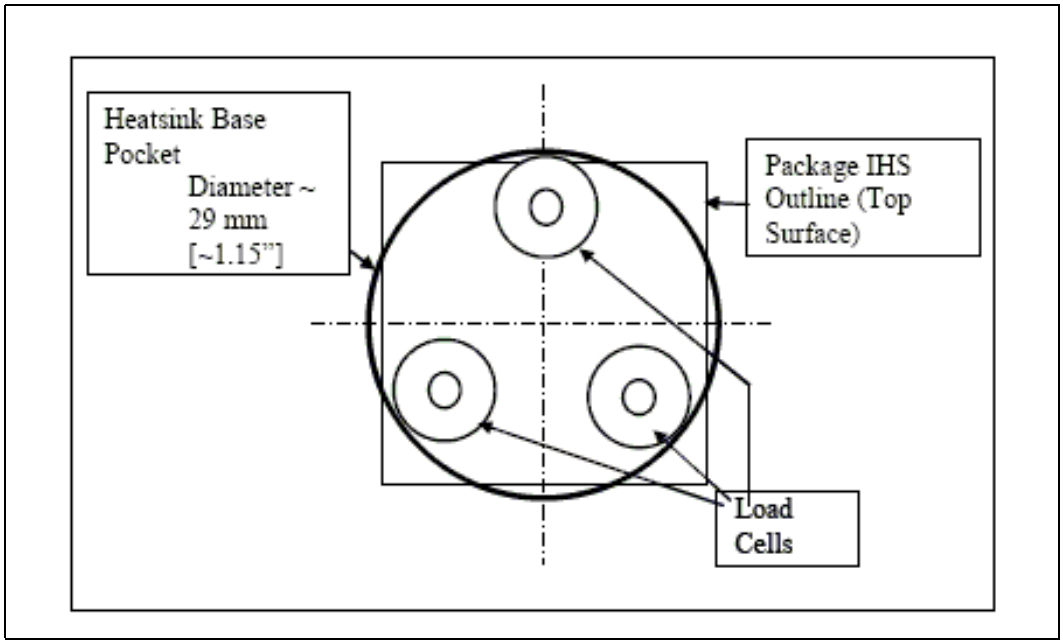


Figure B-2. Load Cell Installation in Machined Heatsink Base Pocket – Side View

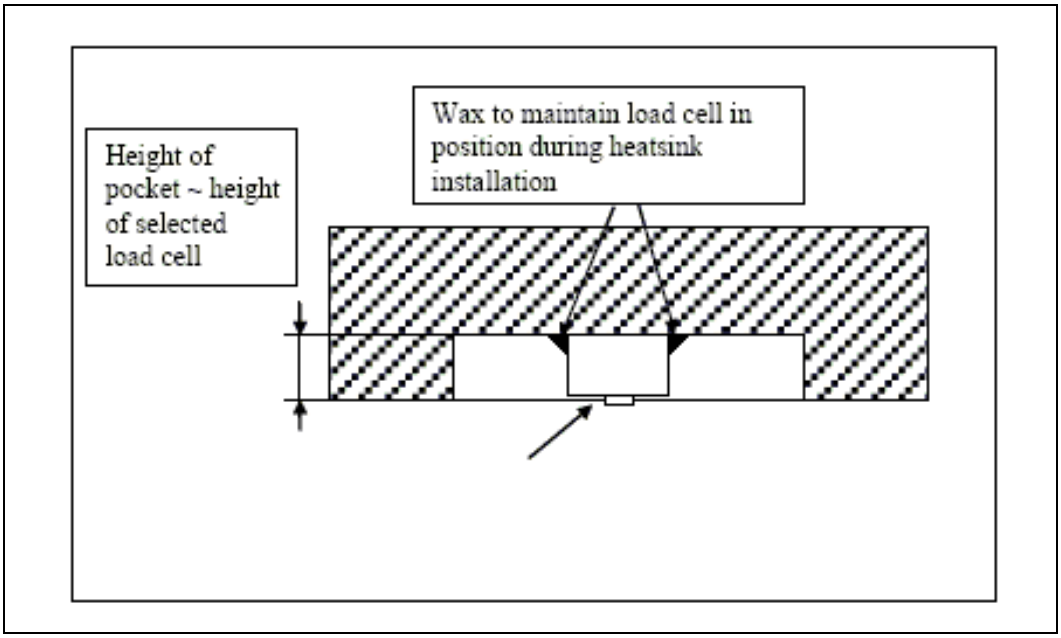
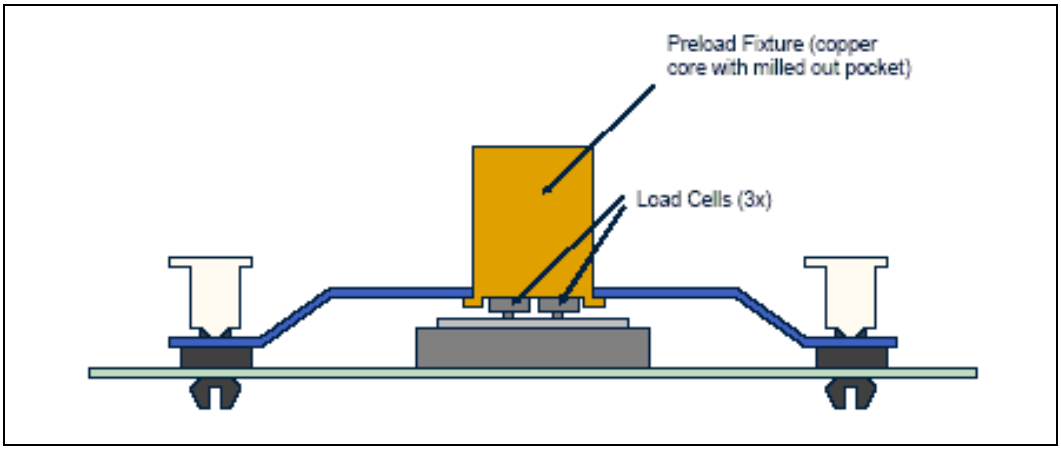


Figure B-3. Preload Test Configuration



B.2.2 Typical Test Equipment

For the heatsink clip load measurement, use equivalent test equipment to the one listed Table B-1.

Table B-1. Typical Test Equipment

Item	Description	Part Number (Model)
Load cell Notes: 1, 5	Honeywell*-Sensotec* Model 13 subminiature load cells, compression only Select a load range depending on load level being tested. www.sensotec.com	AL322BL
Data Logger (or scanner) Notes: 2, 3, 4	Vishay* Measurements Group Model 6100 scanner with a 6010A strain card (one card required per channel).	Model 6100

Notes:
1. Select load range depending on expected load level. It is usually better, whenever possible, to operate in the high end of the load cell capability. Check with your load cell vendor for further information.
2. Since the load cells are calibrated in terms of mV/V, a data logger or scanner is required to supply 5 volts DC excitation and read the mV response. An automated model will take the sensitivity calibration of the load cells and convert the mV output into pounds.
3. With the test equipment listed above, it is possible to automate data recording and control with a 6101-PCI card (GPIB) added to the scanner, allowing it to be connected to a PC running LabVIEW* or Vishay's StrainSmart* software.
4. **IMPORTANT**: In addition to just a zeroing of the force reading at no applied load, it is important to calibrate the load cells against known loads. Load cells tend to drift. Contact your load cell vendor for calibration tools and procedure information.
5. When measuring loads under thermal stress (bake for example), load cell thermal capability must be checked, and the test setup must integrate any hardware used along with the load cell. For example, the Model 13 load cells are temperature compensated up to 71°C, as long as the compensation package (spliced into the load cell's wiring) is also placed in the temperature chamber. The load cells can handle up to 121°C (operating), but their uncertainty increases according to 0.02% rdg/°F.

B.2.3 Test Procedure Examples

The following sections give two examples of load measurement. However, this is not meant to be used in mechanical shock and vibration testing.

Any mechanical device used along with the heatsink attach mechanism will need to be included in the test setup (that is, back plate, attach to chassis, and so on).

Prior to any test, make sure that the load cell has been calibrated against known loads, following load cell vendor's instructions.

B.2.4 Time-Zero, Room Temperature Preload Measurement

1. Pre-assemble mechanical components on the board as needed prior to mounting the motherboard on an appropriate support fixture that replicate the board attach to a target chassis.

   For example: If the attach mechanism includes fixtures on the back side of the board, those must be included, as the goal of the test is to measure the load provided by the actual heatsink mechanism.
2. Install the test vehicle in the socket.
3. Assemble the heatsink reworked with the load cells to motherboard as shown for the Dual-Core Intel Xeon Processor 5000 Series CEK-reference heatsink example in Figure B-3, and actuate attach mechanism.
4. Collect continuous load cell data at 1 Hz for the duration of the test. A minimum time to allow the load cell to settle is generally specified by the load cell vendors

(often on the order of 3 minutes). The time zero reading should be taken at the end of this settling time.

5. Record the preload measurement (total from all three load cells) at the target time and average the values over 10 seconds around this target time as well, that is, in the interval for example over [target time – 5 seconds; target time + 5 seconds].

B.2.5 Preload Degradation under Bake Conditions

This section describes an example of testing for potential clip load degradation under bake conditions.

1. Preheat thermal chamber to target temperature (45 ºC or 85 ºC for example).
2. Repeat time-zero, room temperature preload measurement.
3. Place unit into preheated thermal chamber for specified time.
4. Record continuous load cell data as follows:
   Sample rate = 0.1 Hz for first 3 hrs
   Sample rate = 0.01 Hz for the remainder of the bake test
5. Remove assembly from thermal chamber and set into room temperature conditions
6. Record continuous load cell data for next 30 minutes at sample rate of 1 Hz.

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C Safety Requirements

Heatsink and attachment assemblies shall be consistent with the manufacture of units that meet the safety standards:

1. UL Recognition-approved for flammability at the system level. All mechanical and thermal enabling components must be a minimum UL94V-2 approved.
2. CSA Certification. All mechanical and thermal enabling components must have CSA certification.
3. Heatsink fins must meet the test requirements of UL1439 for sharp edges.

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D Quality and Reliability Requirements

D.1 Intel Verification Criteria for the Reference Designs

D.1.1 Reference Heatsink Thermal Verification

The Intel reference heatsinks will be verified within specific boundary conditions using a TTV and the methodology described in the *Intel® Xeon® Processor Family Thermal Test Vehicle User's Guide*.

The test results, for a number of samples, are reported in terms of a worst-case mean + 3σ value for thermal characterization parameter using real processors (based on the TTV correction offset).

D.1.2 Environmental Reliability Testing

D.1.2.1 Structural Reliability Testing

The Intel reference heatsinks will be tested in an assembled condition, along with the LGA771 Socket. Details of the Environmental Requirements, and associated stress tests, can be found in the *LGA771 Socket Mechanical Design Guide*.

The use condition environment definitions provided in Appendix D-1are based on speculative use condition assumptions, and are provided as examples only.

Table D-1. Use Conditions Environment

Use Environment	Speculative Stress Condition		Example Use Condition	Example 7-Yr Stress Equiv.	Example 10-Yr Stress Equiv.
Shipping and Handling	Mechanical Shock • System-level • Unpackaged • Trapezoidal • 25 g • velocity change is based on packaged weight		Total of 12 drops per system: • 2 drops per axis • ± direction	n/a	n/a
	Product Weight (lbs)	Non-palletized Product Velocity Change† (in/sec)			
	< 20 lbs	250			
	20 to > 40	225			
	40 to > 80	205			
	80 to < 100	175			
	100 to < 120	145			
	≥120	125			
	†Change in velocity is based upon a 0.5 coefficient of restitution.				
Shipping and Handling	Random Vibration • System Level • Unpackaged • 5 Hz to 500 Hz • 2.20 g RMS random • 5 Hz @ .001 g^2/Hz to 20 Hz @ 0.01 g^2/Hz (slope up) • 20 Hz to 500 Hz @ 0.01 g^2/Hz (flat) • Random control limit tolerance is ± 3 dB		Total per system: • 10 minutes per axis • 3 axes	n/a	n/a

Note: In case of a discrepancy, information in the most recent *LGA771 Socket Mechanical Design Guidelines* supersedes that in the Table D-1 above.

D.1.2.2 Recommended Test Sequence

Each test sequence should start with components (that is, baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly, and BIOS/Processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/Processor/memory test.

D.1.2.3 Post-Test Pass Criteria

The post-test pass criteria are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flatly against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.

3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

D.1.2.4 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard.
- Processor and memory.
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. *Intel PC Diags* is an example of software that can be utilized for this test.

D.1.3 Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (e.g. polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Material used shall not have deformation or degradation in a temperature life test.

Any plastic component exceeding 25 grams should be recyclable per the European Blue Angel recycling standards.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

Lead-free and Pb-free: Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

RoHS compliant: Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/ pending exemption applies.

Note: RoHS implementing details are not fully defined and may change.

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E Enabled Suppliers Information

E.1 Supplier Information

E.1.1 Intel Enabled Suppliers

The Intel reference enabling solution for the Dual-Core Intel Xeon Processor 5000 Series solutions has been verified to meet the criteria outlined in Appendix D, "Quality and Reliability Requirements." Customers can purchase the Intel reference thermal solution components from the suppliers listed in Table E-1.

For additional details, please refer to the Dual-Core Intel Xeon Processor 5000 Series thermal mechanical enabling components drawings in Appendix A, "Mechanical Drawings."

Table E-1. Suppliers for the Dual-Core Intel Xeon Processor 5000 Series Reference Solution (Sheet 1 of 2)

Assembly	Component	Description	Development Suppliers	Supplier Contact Info
CEK771-01-2U (for 2U, 2U+)	CEK Heatsinks Intel Reference Heatsink p/n C61708 rev03 - or - Intel Boxed Heatsink p/n D36871	Copper Fin, Copper Base includes PCM45F TIM+cover	Fujikura CNDA 1242012 (stacked fin)	Fujikura America Ash Ooe a_ooe@fujikura.com 408-748-6991 Fujikura Taiwan Branch Yao-Hsien Huang yeohsien@fujikuratw.com.tw 886(2)8788-4959
	CEK Heatsink Intel Boxed Heatsink p/n D36871	Copper Fin, Copper Base includes PCM45F TIM+cover	Furukawa CNDA 65755 (Crimped fin)	Furukawa America Timothy Yu yu@FurukawaAmerica.com 408-345-1528 Furukawa Taiwan Branch Johnson Tseng Johnson@tfe.com.tw (02)2563-8148x15
	Thermal Interface Material	Grease	Shin-Etsu G751 CNDA 75610	Donna Hartigan (480) 893-8898
	CEK Spring for CEK771 Intel p/n D13646 rev04	Stainless Steel 301, Kapton* Tape on Reinforced Spring Fingers	AVC CNDA 2085011	David Chao 886-2-22996390 x619 david_chao@avc.com.tw

Table E-1. Suppliers for the Dual-Core Intel Xeon Processor 5000 Series Reference Solution (Sheet 2 of 2)

CEK771-01-1U (for 1U)	CEK Heatsink Intel p/n C90546 rev02	Copper Fin, Copper Base	Fujikura CNDA 1242012 (stacked fin)	Fujikura America Ash Ooe a_ooe@fujikura.com 408-748-6991 Fujikura Taiwan Branch Yao-Hsien Huang yeohsien@fujikuratw.com.tw 886(2)8788-4959
	Thermal Interface Material	See CEK771-2U-01		
	CEK Spring for CEK771	See CEK771-2U-01		

E.1.2 Additional Enabled Suppliers

The Intel enabled solutions for the Dual-Core Intel Xeon Processor 5000 Series have been verified to meet the criteria outlined in Appendix D, "Quality and Reliability Requirements." Customers can purchase the Intel enabled thermal solution components from the suppliers listed in Table E-1.

For additional details, please refer to the Dual-Core Intel Xeon Processor 5000 Series thermal mechanical enabling components drawings in Appendix A, "Mechanical Drawings.".

Table E-2. Suppliers of Alternative Thermal Solutions for the Dual-Core Intel Xeon Processor 5000 Series

Assembly	Component	Description	Development Suppliers	Supplier Contact Info
2U Heatsink	Alternative CEK Heatsink	Copper Fin, Copper Base	AVC CNDA AP5281 (stacked fin)	David Chao david_chao@avc.com.tw 886-2022996930x7619 Jeff Brown (North America) jb@avcamerica.com 310-783-5442
			Aavid Thermalloy CNDA #2525071	David Huang huang@aavid.com 603-223-1724 Frank Hsue frank.hsu@aavid.com.tw 886-2-26989888 x306
			CCI (Chaun-Choung Technology Co. Ltd. CNDA #8747572	Monica Chih monica_chih@ccic.com.tw 886-2-29952666 EXT 292 Hary Lin 714-739-5797 ackinc@aol.com
			Auras CNDA #5779699	Stephen Lee stephen_lee@auras.com.tw +886-937-183-194

Table E-2. Suppliers of Alternative Thermal Solutions for the Dual-Core Intel Xeon Processor 5000 Series

Assembly	Component	Description	Development Suppliers	Supplier Contact Info
1U Heatsink	Alternative CEK Heatsink	Copper Fin, Copper Base	AVC CNDA AP5281	David Chao david_chao@avc.com.tw 886-2022996930x7619 Jeff Brown (North America) jb@avcamerica.com 310-783-5442
			ADDA CNDA AP1249	Jomei jomei@adda.com.tw 886-2-82212252x209
			CCI CNDA 8747572	Monica Chih monica_chih@ccic.com.tw 886-2-29952666 EXT 292 Hary Lin 714-739-5797 ackinc@aol.com
			Auras CNDA #5779699	Stephen Lee stephen_lee@auras.com.tw +886-937-183-194
			CoolerMaster CNDA #7425225	Helen Wen helena_wan@coolermaster.com.tw +886 (2) 3234-0050 x235
			ThermalTake CNDA #7429482	Vic Chan vic@thermaltake.com +866 (2) 2662-6501 x213

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