Customer Success
Thales: Wireless

If a picture is worth a thousand words, an executable model is worth a thousand pictures

PROBLEM STATEMENT:

When faced with developing a high data-rate 802.16 modem, Thales needed to design a system to easily handle wireless interfaces with frequencies up to 10 GHz. To best support the new standard, Thales needed to determine the architecture that provided the best performance. With a focus on minimizing development costs, the goal was to reuse elements from previous designs where applicable. Thales turned to Intel® CoFluent™ Studio to capitalize on their internal know-how and existing software. Intel® CoFluent™ Studio enabled them to move design exploration to a higher level of abstraction and explore the impact of architectural changes on performance early in the design cycle.

Thales

Thales (www.thalesgroup.com), established in France more than a century ago, is a leading international group, addressing defense, aerospace, and security markets worldwide. Thales' expertise in its core markets spans the entire value chain, providing all the capabilities its customers require, from equipment and systems to comprehensive support services, and including prime contracting on large-scale programs.

Thales' leading-edge technology is supported by 22,000 R&D engineers who offer a capability unmatched in Europe to develop and deploy field-proven mission-critical information systems. To this end, the group's civil and military businesses develop in parallel and share a common base of technologies to serve a single objective: the security of people, property, and nations.

New developments in digital technologies, mobile communications, and integrated services, combined with the explosive growth of the internet, are creating exciting new business opportunities while completely changing the face of telecommunications. Thales, a driving force in the market, already includes many of the newly defined functions and features in the company's product offerings. Thales is set to consolidate its worldwide leadership position in the communication systems sector.

Wireless Modem Architecture

In the context of the ITEA MARTES (Model-based Approach to Real-Time Embedded Systems) European research project (www.martes-itea. org), Thales used Intel® CoFluent™ Studio to model a high-data-rate 802.16 wireless modem. The modem uses the orthogonal frequency division multiplexing (OFDM) modulation techniques to identify adaptations that improve the robustness of the links and/or the output data rate. The modem contains an existing piece of software originally written in C++. It is modular code and uses three freeware libraries and an internal matrix library.

Modem Architecture Modeling and Performance Analysis

The modeled system is composed of a transmitter and a receiver. The test bench consists of two radio channel simulators, a data source, a data sink, and a comparator to check received data against the data originally sent. Similarly, the receiver subsystem shows two receiver heads for simulating spatial diversity reception. The transmitter is composed of a series of functional modules: convolutive coder, puncture function, interleave function, reshape function, modulator, IFFT, prefix appending function. The receiver presents the inverse structure compared to the transmitter. All communications between modules are modeled using FIFOs.

In order to study the performance of the system, the identified physical architecture was described. This executive structure is composed of two processing units: one software unit for functions having relatively high activation periods, and a hardware unit to support the high-frequency activated functions.

The chosen hardware platform for the test case is dedicated to simulation and validation purposes in the analysis and design phases of the high data-rate modem. It consists of a general purpose processor (GPP) and a digital signal processor (DSP), which is to be selected later.

The created model has multiple possibilities for data paths, which can be individually selected to experiment with various possible hardware choices. Three alternatives are considered:

- High-level and radio interfaces on the bus

- Radio interface on the bus, high-level interface on dedicated FIFOs

- Radio interface via dedicated FIFOs

Ten different architectural models were designed. The architectures were compared to analyze their pros and cons.

The design team then utilized Intel® CoFluent™ Studio, along with a Thales proprietary C++ library, external source files, and subroutines for OFDM, modulation, and puncture algorithms, to simulate the implementation of the modem in a two-processor hardware architecture loosely derived from the TI OMAP 5910-5912. Previously recorded performance data was used to refine the simulation results and evaluate the architecture alternatives.

Architectural Exploration Benefits

By varying the parameters of the model, and changing between different block dispatching and data path possibilities, the executable model created with Intel® CoFluent™ Studio helped determine both hardware/software implementation and module distribution between processors. The tool compared hardware/software tradeoffs as well as board versus SoC design options. The level of confidence achieved is dependent on the quality of the user-provided performance data. Intel® CoFluent™ Studio in itself allows a large range of possibilities to define the performance data.

Optimizing the Architecture to Boost Performance in Wireless Designs

Several models of the high-data-rate 802.16 modem are created at different abstraction levels, according to the Intel® CoFluent™ Studio methodology. The modem function is then mapped onto the execution platform, and the functions are distributed between the DSP and GPP. The mapping is varied for each of the three architectures under consideration.

1. Radio and high-level interfaces on the bus

The data source, destination, and radio interface are projected on the bus address space for this model. This option leads to less hardware and more possibilities for the data exchanges, going either to DSP or GGP by programming. This model's drawback is an increased risk of contention on the bus and the connecting elements, since all must be aware of the frame-level timing.
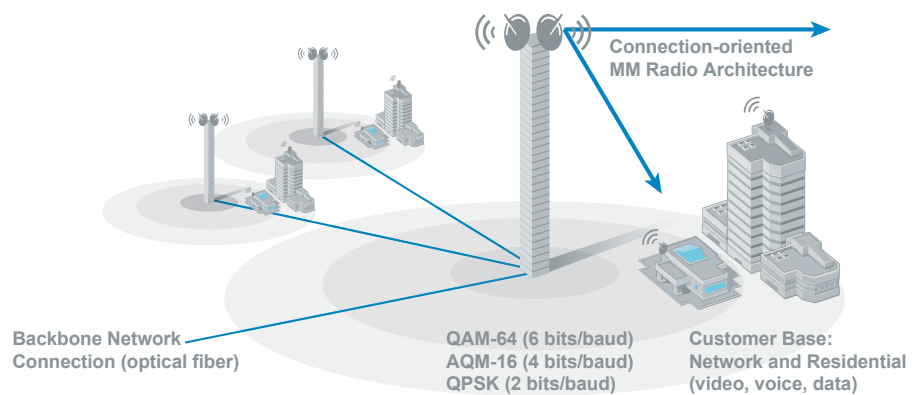
2. Radio interface on the bus, high-level interface on dedicated FIFOs

The circulation of data frames inside the GPP or DSP is not hardware-modeled: It is done by passing a memory pointer from one software module to another, and requires no time. This architecture represents a radio interface that consists of a port projected on the bus, and the radio part implementing a hardware FIFO to put the data on the air. The FIFOs on the high-level end alleviate the real-time burden on the data generator and receiver, which need only to ensure a known average throughput.

3. Radio interface via dedicated FIFOs

This configuration utilizes additional dedicated FIFOs on the low-level radio interface. There, data transfers between processors do not create radio interface. The FIFOs can be implemented in hardware on the modem or in software on the processors via a serial interface. This simplifies the radio hardware, which can receive the data with a clock and no timing to control. While this implementation is more efficient, it is more difficult to modify.

Connection-oriented MM Radio Architecture

Backbone Network Connection (optical fiber)

QAM-64 (6 bits/baud)
AQM-16 (4 bits/baud)
QPSK (2 bits/baud)

Customer Base: Network and Residential (video, voice, data)

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