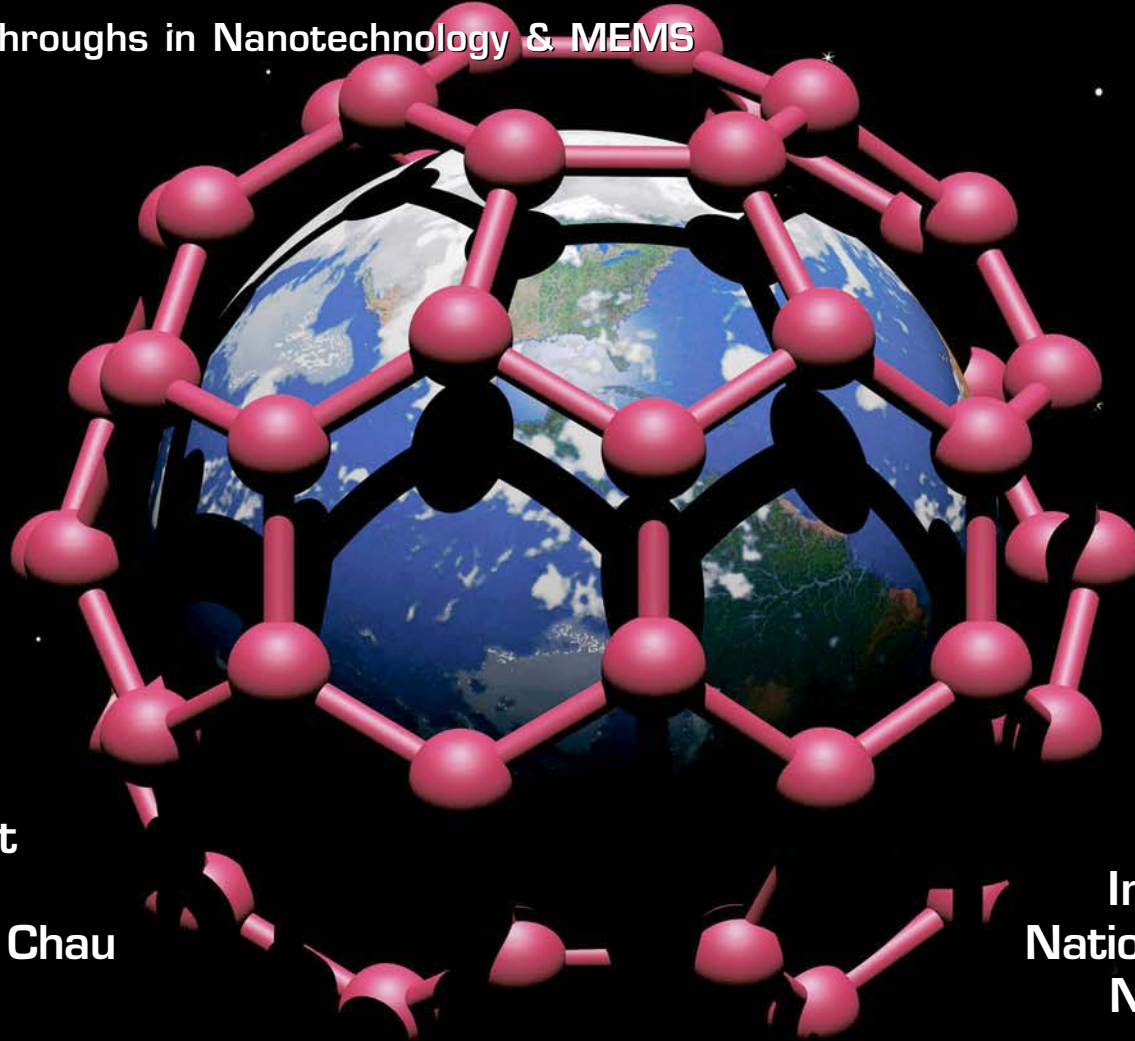


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**Maintaining a
Livable Planet:
Nanotech and
the Environment**

**Meet Robert S. Chau
of Intel**

**Nano 2005
Show Preview**

**Inside Canada's
National Institute of
Nanotechnology**



Robert S. Chau

Intel Fellow, Technology and Manufacturing Group, and
Director, Transistor Research and Nanotechnology, Intel Corp.

Robert Chau is responsible for directing research and development at Intel in advanced transistors and gate dielectrics for microprocessor applications. He is also responsible for leading research efforts in advanced silicon and non-silicon nanotechnologies for future device and process applications.

Chau joined Intel in 1989 and has developed seven generations of Intel gate dielectrics along with many CMOS transistor innovations used in various Intel manufacturing processes and logic products. He has received six Intel Individual Achievement Awards and 13 Intel Logic Technology Development Division Recognition Awards, and currently holds 57 U.S. patents. Chau is an IEEE Fellow.

Nanotech Briefs: What is the history of nanotechnology research at Intel?

Robert Chau: Intel entered the nanotechnology era in 2000 when it began volume manufacturing of microprocessors whose transistor gate lengths became sub-100 nm. Of course, research into this process technology began many years earlier — it takes a long time for a new process to go from the

research lab to commercialization. For instance, today we are doing research into technologies that are not expected to be in our production fabs until well into the next decade. These include emerging devices like carbon nanotubes, semiconductor nanowires, and III-V nanoelectronics.

NB: How does nanotechnology affect Moore's Law?

Chau: Moore's Law states simply that the number of transistors on a chip doubles every two years. If you look at Intel's track record, you can see that we have been maintaining this pace since the invention of the microprocessor in the early 1970s. We crossed the nanotechnology barrier in 2000 (with the 0.13- μm technology node, which has transistor physical gate length of about 70 nm), and are getting ever deeper into nanotechnology space. A very good example of nanotechnology used in our current 90-nm technology node (in production starting 2003) is the gate oxide, which has physical thickness of only 1.2 nm, about four atomic-layers thick.

NB: Why is nanotechnology necessary for the development of ever more powerful microprocessors?

Chau: Nanotechnology allows an exponential growth in transistor count, as well as higher performance and lower power per transistor. More high-performance transistors allow more features, more capabilities, and higher performance, all at lower cost per function and higher energy efficiency. This in turn will enable many new applications. For instance, an increased transistor budget enables the integration of specialized engines such as graphics processors and network co-processors. In the future, specialized processors to enable tasks such as pattern recognition and natural language translation also may be possible.

NB: What are the benefits/drawbacks of nanotech in relation to chip manufacturing?

Chau: The primary benefit is the higher computing capabilities and reduced costs per function that are offered as Moore's Law advances. There

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are no real drawbacks, although there are challenges in terms of new materials, new device structures, new integration schemes, and new manufacturing techniques.

NB: What specific areas of nanotechnology is Intel addressing?

Chau: Intel is looking at making smaller, faster, and more power-efficient transistors as well as higher speed, higher bandwidth interconnects. As feature sizes get smaller and circuits operate at higher speeds, active power and off-state leakage tend to increase. Intel has implemented several measures to address the power/leakage problem, and is doing a great deal of research in this area. The recent high-K/metal-gate breakthrough is an example. High-K/metal gates can be used to replace the conventional SiO₂/polySi gate stack in CMOS transistors for enhancing device performance and for controlling gate oxide leakage.

Some of Intel's research work is more long-term. For example, Intel is looking at the use of III-V materials, carbon nanotubes, and semiconductor nanowires as high-mobility materials for future high-speed and low-power transistor applications, as well as looking at the use of carbon nanotubes for future interconnect applications. To gauge real research progress, we have also developed and implemented a benchmarking methodology to benchmark emerging nanoelectronic devices against state-of-the-art silicon devices. This will al-

Nanotechnology allows an exponential growth in transistor count, as well as higher performance and lower power per transistor.

low the potential merits and drawbacks of these new emerging devices to be evaluated and addressed at an accelerated pace.

NB: What are some of the recent nanotech breakthroughs made at Intel?

Chau: Intel has developed and implemented a 1.2-nm gate oxide for its 90-nm technology node. The 1.2-nm gate oxide is the thinnest gate oxide ever put into volume production. Intel has also developed strained silicon and is using it in volume production to increase the performance of its microprocessors and/or to reduce their power consumption. Intel is using it in its 90-nm logic node, and plans to use a second-generation version of strained silicon technology (which provides even more performance/power benefits) in its 65-nm technology node. Intel has also disclosed that it has made significant breakthroughs in high-K/metal gates for enhancing transistor perform-

ance and controlling gate oxide leakage, and in a non-planar 3-D device called the Tri-gate transistor to improve short channel performance. The high-K/metal-gate and Tri-gate CMOS technologies are important technology options being evaluated for future technology nodes beyond the 65-nm node.

NB: What is the ultimate goal of Intel's nanotech research?

Chau: The ultimate goal is to continue the pace of Moore's Law. This allows Intel to deliver ever more functionality to end users at exponentially decreasing cost. This is the force that has been driving the semiconductor industry and has led to the electronic revolution that we are all experiencing.

If you have questions for Robert S. Chau, please contact him at robert.s.chau@intel.com. For more information about Intel's nanotechnology research, visit www.intel.com/research/silicon. ^{NE}