Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications

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***Abstract*—Recently there has been tremendous progress made in the research of novel nanotechnology for future nanoelectronic applications. In particular, several emerging nanoelectronic devices such as carbon-nanotube field-effect transistors (FETs), Si nanowire FETs, and planar III–V compound semiconductor (e.g., InSb, InAs) FETs, all hold promise as potential device candidates to be integrated onto the silicon platform for enhancing circuit functionality and also for extending Moore's Law. For high-performance and low-power logic transistor applications, it is important that these research devices are frequently benchmarked against the existing Si logic transistor data in order to gauge the progress of research. In this paper, we use four key device metrics to compare these emerging nanoelectronic devices to the state-of-the-art planar and nonplanar Si logic transistors. These four metrics include: 1) CV/I or intrinsic gate delay versus physical gate length L_g; 2) energy-delay product versus L_g; 3) subthreshold slope versus L_g; and 4) CV/I versus on-to-off-state current ratio I_{ON}/I_{OFF}. The results of this benchmarking exercise indicate that while these novel nanoelectronic devices show promise and opportunities for future logic applications, there still remain shortcomings in the device characteristics and electrostatics that need to be overcome. We believe that *benchmarking* is a key element in accelerating the progress of nanotechnology research for logic transistor applications.**

***Index Terms*—Nanotechnology, semiconductor devices.**

I. Introduction

Moore's Law states that the number of transistors per integrated circuit doubles every 24 months, and it has been the guiding principle for the semiconductor industry for over 30 years. The sustaining of Moore's Law requires transistor scaling, as illustrated in Fig. 1. The physical gate length (L_g) of Si transistors used in our current 90-nm generation node is $\sim$50 nm. It is projected that the size of the transistor will reach $\sim$10 nm in 2011. Through technology innovations, such as strained-Si channels [1], [2], metal–gate/high-κ stacks [3], [4], and the nonplanar fully depleted Tri-gate CMOS transistor architecture [5], [6], Moore's Law will continue at least through early next decade. By combining silicon innovations with other novel nanotechnologies on the same silicon platform, we expect Moore's Law to extend well into the next decade. Recently, there has been tremendous progress made and excitement generated in the research of novel nanotechnology for future nanoelectronics applications. To gauge the progress of nanotechnology research for high-performance and low-power logic applications, it is important that these new devices be benchmarked against the best Si MOSFET data using a set of appropriate device metrics. In this paper, we compare several novel nanoelectronic devices, including a carbon-nanotube (CNT) field-effect transistors (FETs) [7]–[16], Si nanowire FETs [17]–[19], and planar III–V compound semiconductor (e.g., InSb, InAs) FETs [20]–[22] to the state-of-the-art planar and nonplanar Si devices (both Tri-gate and double-gate FinFET transistors [6], [25]) in terms of four key metrics, which are: 1) intrinsic speed (CV/I) versus L_g; 2) energy-delay product $(CV/I \cdot CV^2)$ versus L_g; 3) transistor subthreshold slope versus L_g; and 4) CV/I versus I_{ON}/I_{OFF} ratio. These four metrics capture the four fundamental device parameters for logic applications, namely: 1) speed; 2) switching energy; 3) scalability; and 4) off-state leakage. Fig. 2 shows the transmission electron microscope (TEM) and scanning electron microscope (SEM) images of the various nanoelectronic devices along with the planar and nonplanar Si MOSFETs used for this benchmarking study. The results of this benchmarking exercise will allow us to identify the various device-related strengths, as well as limitations of these novel devices, and focus on solving these device related problems in order to accelerate the research progress. It is

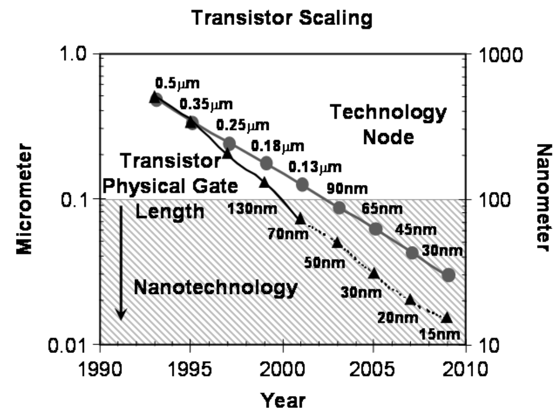

Fig. 1. Scaling of transistor size (physical gate length) with technology node to sustain Moore's Law. Nodes with feature size less than 100 nm can be referred to as nanotechnology. By 2011, the gate length is expected to be at or below 10 nm. Transistor scaling will be enabled by integration of emerging nanotechnology options on to the Si platform.

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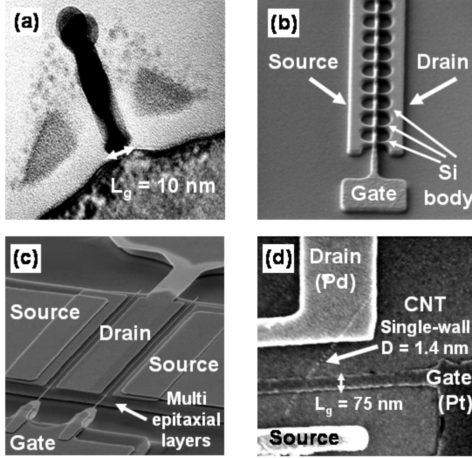

Fig. 2. TEM cross section and SEM images of: (a) a planar Si MOSFET with physical gate length $L_g = 10$ nm, (b) a nonplanar Tri-gate transistor with multiple Si fins, (c) a III–V quantum-well FET on a multilayered epitaxial substrate, and (d) a top-gated CNT FET.

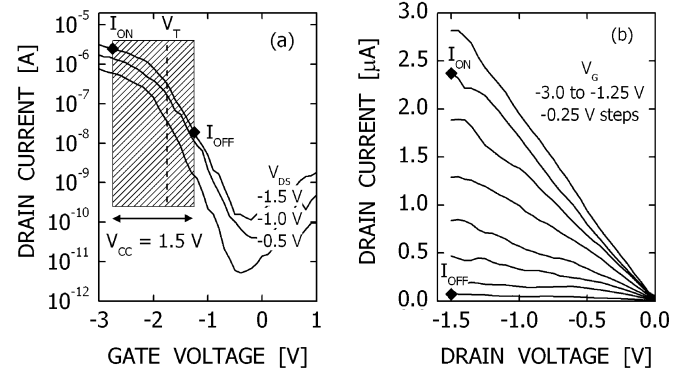

Fig. 3. Example (a) I_D–V_G and (b) I_D–V_{DS} characteristics of a CNT FET illustrating our benchmarking procedure. The V_{CC} choice is made by selecting the highest available V_{DS}, which, in this example, is 1.5 V. The shaded box in (a) is anchored around $V_G = V_T$, as discussed in the text. The width of the box denotes the V_G swing of 1.5 V, which is consistent with the V_{CC} choice. The values of I_{ON} and I_{OFF} are shown as black diamonds in both (a) and (b).

to be noted that this study specifically addresses the device performance aspects of the emerging technologies, and does not address the materials aspects such as the chirality of CNTs, the positioning of nanotubes and nanowires, and the integration of III–V-based devices onto the Si platform.

II. Benchmarking Methodology

Nanoelectronic devices from literature and from our own research, as shown in Fig. 2, were used in this benchmarking exercise. In order to compute the four metrics, we need to determine the gate capacitance value, voltage of operation, on-state current, and corresponding off-state current from these devices.

The gate capacitance for the planar and nonplanar Si CMOS and the III–V devices was experimentally measured. However, in the case of nanotube and nanowire devices, due to the very small gate area, the gate capacitance could not be measured directly and was computed based on the geometry of the device structure, as well as the gate dielectric thickness and material used. For example, the total gate capacitance per unit length $C_{\rm TOTAL}$ of the CNT and nanowire devices with metal gate (assuming no poly-Si depletion effect) is determined using the equation

$$C_{\rm TOTAL}^{-1} = C_{\rm OX}^{-1} + C_{\rm QM}^{-1} \quad (1)$$

where $C_{\rm OX}$ is the gate dielectric capacitance per unit length and is calculated using the equation

$$C_{\rm OX} = 2\pi\varepsilon_0\varepsilon_r/\ln(2h/R) \quad (2)$$

where ε_r is the dielectric constant of the gate dielectric, $(h-R)$ is the thickness of the gate dielectric, and R is the radius of the nanotube or nanowire. Equation (2) assumes the gate electrode is an infinite metal plane over a cylindrical wire or tube. $C_{\rm QM}$ is the capacitance per unit length related to quantum mechanical effects and is equal to ~4 pF/cm in the case of CNTs [23].

Applying the four device metrics to benchmark emerging nanoelectronic devices with nontargeted threshold voltage V_T and nonoptimized I–V characteristics requires careful evaluation of the supply voltage of operation $V_{\rm CC}$, on-state current $I_{\rm ON}$, and off-state current $I_{\rm OFF}$. In the case of optimized Si devices, the supply voltage $V_{\rm CC}$ is applied between the drain and source, i.e., $V_{\rm DS} = V_{\rm CC}$. A gate voltage swing of V_G from 0 V to $V_{\rm CC}$ is applied between the gate and source for transistor operation, i.e., V_G goes from 0 V to $V_{\rm CC}$. $I_{\rm ON}$ is determined at $V_G = V_{\rm DS} = V_{\rm CC}$, while $I_{\rm OFF}$ is determined at $V_G = 0$ V and $V_{\rm DS} = V_{\rm CC}$. Historically, in optimized Si devices, V_T is roughly 1/3 of $V_{\rm CC}$ such that 2/3 of the V_G swing above V_T is used for obtaining the on-state current $I_{\rm ON}$, while 1/3 of the V_G swing below V_T is used for obtaining the off-state current $I_{\rm OFF}$. Finally, in the computation of CV/I, $V = V_{\rm CC}$ and $I = I_{\rm ON}$.

In the case of emerging nanoelectronic devices where V_T is not targeted and the I–V characteristics are not optimized, the choice of $V_{\rm CC}$ and on-state current for the evaluation of the CV/I metric becomes arbitrary and often leads to erroneous interpretation during benchmarking. In our benchmarking process, we select the voltage of operation $V_{\rm CC}$ for the nanoelectronic device after analyzing its drain current versus drain–source voltage (I_D–$V_{\rm DS}$) and drain current versus gate voltage (I_D–V_G) characteristics. We select the power supply voltage $V_{\rm CC}$ based on the highest available $V_{\rm DS}$ value from the I_D–V_G plot. For example, Fig. 3 shows the I_D–$V_{\rm DS}$ and I_D–V_G characteristics of a CNTFET from which we choose a $V_{\rm CC}$ value of 1.5 V, i.e., $|V_{\rm DS}| = V_{\rm CC} = 1.5$ V. Care has been taken to use a $V_{\rm CC}$ value that is no higher than that of a standard Si device of comparable L_g and gate–oxide thickness.

The on-state current $I_{\rm ON}$ and off-state current $I_{\rm OFF}$ are then determined by anchoring the V_G swing (of magnitude equal to $V_{\rm CC}$) around V_T on the I_D–V_G curve at $|V_{\rm DS}| = V_{\rm CC}$ with 2/3 of the V_G swing above V_T for determining $I_{\rm ON}$ and 1/3 of the V_G swing below V_T for determining $I_{\rm OFF}$, as shown by the shaded box in Fig. 3(a). This choice of anchoring the V_G swing [i.e., the location of the shaded box in Fig. 3(a)] around V_T is based on historical Si device data that shows a similar 70% and 30% division in the V_G swing from V_T between the on and off states, respectively. In our CNT transistor example in Fig. 3(a), $V_T = -1.75$ V (V_T is extracted using the standard peak transconductance method [27]) and, therefore, $I_{\rm ON}$ is determined at $V_G = -2.75$ V and $I_{\rm OFF}$ at $V_G = -1.25$ V for

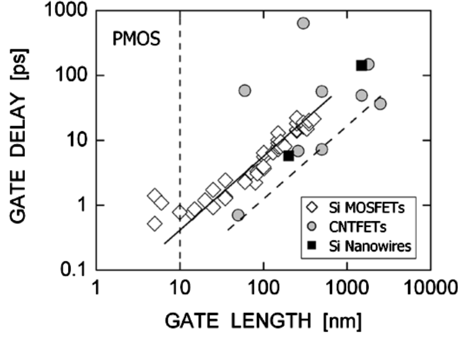

Fig. 4. Gate delay (intrinsic device speed CV/I) versus transistor physical gate length of PMOS devices.

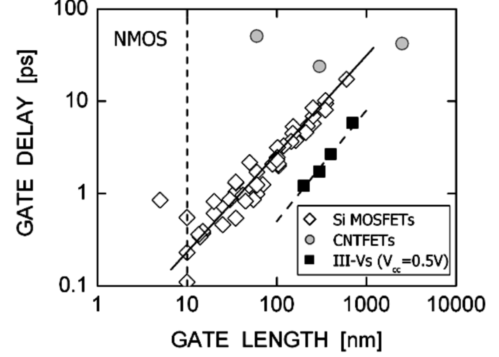

Fig. 5. Gate delay (intrinsic device speed, CV/I) versus transistor physical gate length of NMOS devices.

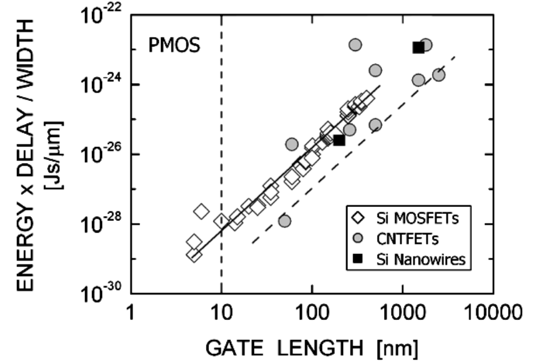

Fig. 6. Energy-delay product per device width versus transistor physical gate length of PMOS transistors.

the total V_G swing of $V_{\rm CC} = 1.5$ V. The same $I_{\rm ON}$ and $I_{\rm OFF}$ values selected from the I_D–V_G characteristics are indicated on the I_D–$V_{\rm DS}$ family of curves in Fig. 3(b).

The intrinsic gate delay (CV/I) and energy-delay product $(CV/I \cdot CV^2)$ per unit device width can now be computed from the determined gate capacitance $V_{\rm CC}$ and $I_{\rm ON}$ values. In the computation of $CV/I, V = V_{\rm CC}$ and $I = I_{\rm ON}$. The total device width for CNTs and Si nanowires is assumed to be equal to $2\pi R$, where R is the radius of the nanotube and nanowire. In the case of nonplanar Si double-gate transistors (FinFETs), the device width is $2T_{\rm Si}$, where $T_{\rm Si}$ is the height of the silicon fin [25]. In the case of nonplanar Si Tri-gate transistors, the device width is $(2T_{\rm Si} + W_{\rm Si})$ [6], [25], where $W_{\rm Si}$ is the width of the silicon body. As we go to novel devices, the small diameter (i.e., small device width) associated with nanotubes and nanowires makes the energy-delay product unfairly low compared to standard planar devices. Therefore, the energy-delay product needs to be normalized to the device width for meaningful comparison.

Since CV/I and energy-delay product metrics do not comprehend the importance of the transistor off-state leakage $I_{\rm OFF}$, one needs to ensure that the choice of $I_{\rm ON}$ does not embellish the intrinsic gate delay (CV/I) at the expense of $I_{\rm OFF}$. Recently, Antoniadis and Lundstrom proposed a CV/I versus $I_{\rm ON}/I_{\rm OFF}$ metric to evaluate novel devices with nonoptimized V_T [24]. In this metric, a $V_{\rm CC}$ window, such as the one shown schematically in Fig. 3(a), is rigidly moved along the V_G axis of the I_D–V_G curve with $V_{\rm DS} = V_{\rm CC}$, thus generating a pair of data points (CV/I and $I_{\rm ON}/I_{\rm OFF}$) for each V_G step. This metric allows one to evaluate the tradeoff between intrinsic gate delay and $I_{\rm ON}/I_{\rm OFF}$ ratio for emerging nanoelectronic devices with a nonoptimized V_T target.

III. Benchmarking Results

The intrinsic device speed (CV/I) of the CNT PMOS FET and the planar and nonplanar Si PMOS FET with respect to the transistor physical gate length L_g is shown in Fig. 4. Also included in this figure is the Si nanowire transistor data. The data shows that the very best CNTs, reported to date, exhibit significant CV/I improvement over the Si devices. This improvement is primarily due to the mobility enhancement in CNTs. Based on the data, it is estimated that the effective device mobility of CNTs is at least 20 times higher than that of Si; presumably, this effective mobility improvement will even be higher if the contact resistance of the CNT devices can be further lowered. The CV/I characteristics of the Si nanowire transistors is similar to that of Si planar and nonplanar transistors at this time, indicating no significant improvement in mobility with Si nanowire. In both cases, the scalability of CNT and Si nanowire transistors to below 50 nm L_g remains to be demonstrated.

Fig. 5 compares the CV/I of CNT NMOS FETs and the planar and nonplanar Si NMOS FETs. Obviously, the CNT NMOS FETs are not as well established as the CNT PMOS FETs. This issue is discussed later in Section IV. Included in the plot are planar III–V devices in which the channel is made of a high mobility compound semiconductor material such as InSb or InAs [20]–[22]. The III-V devices exhibit approximately 50 times higher effective channel mobility as obtained from Hall measurements and, hence, significant improvement in CV/I compared to the Si MOSFETs. The other important factor contributing to the CV/I improvement is that these III–V devices were operated at a very low supply voltage of only 0.5 V without significant drive current reduction due to high mobility. Despite the significant enhancement in CV/I, the scalability of these III–V devices to shorter L_g still remains to be demonstrated.

Figs. 6 and 7 show the energy-delay product per unit device width of the PMOS and NMOS devices, respectively. The improvement of the CNT FETs over the Si devices in PMOS energy-delay product is due to the higher effective mobility of the

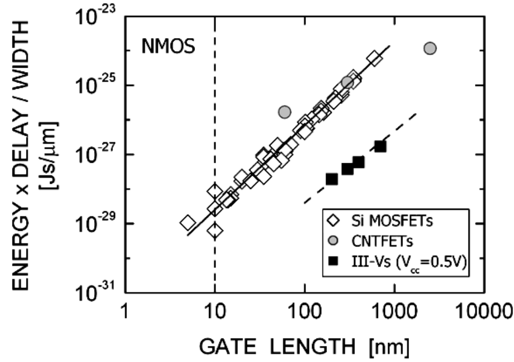

Fig. 7. Energy-delay product per device width versus transistor physical gate length of NMOS transistors.

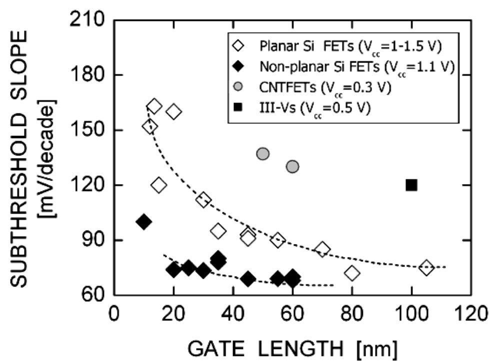

Fig. 8. Subthreshold slope versus transistor physical gate length. The planar and nonplanar Si FETs as well as the III–V planar devices are n-channel transistors, while the CNT FETs are p-channel transistors.

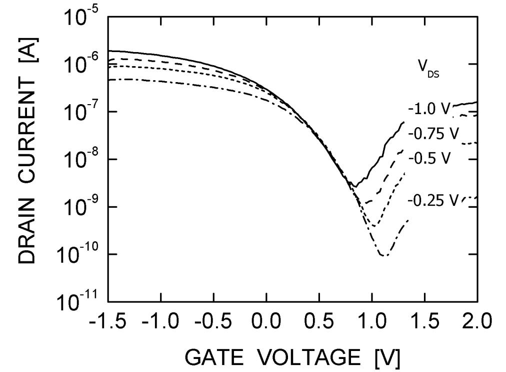

Fig. 9. I_D–V_G characteristics of an Si nanowire PMOS transistor with metal source–drain at different drain biases $V_{\rm DS}$, illustrating ambipolar conduction.

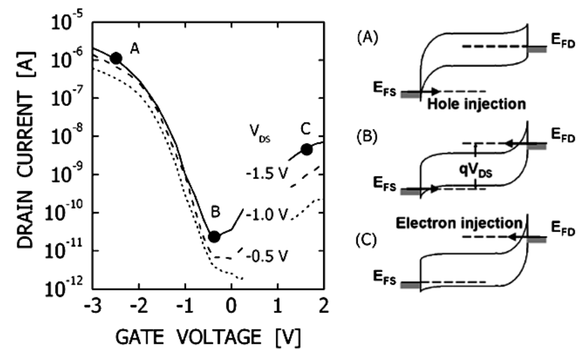

Fig. 10. I_D–V_G characteristics of a CNT PMOS transistor with Pd metal source–drain at different drain biases $V_{\rm DS}$, illustrating ambipolar conduction. Pd has a p-type work function with respect to nanotubes. The energy band diagrams exhibit: (A) dominant hole injection in the on state, (B) equal hole and electron injection at the minimum current point, and (C) dominant electron injection in the ambipolar branch.

CNT FETs. The significant improvement of the III–V devices over the Si devices in NMOS energy-delay product is due to the lower supply voltage (0.5 V) and higher effective mobility of the III–V devices.

The next two metrics, subthreshold slope versus L_g and CV/I versus $I_{\rm ON}/I_{\rm OFF}$ will be discussed in Section IV.

IV. Challenges and Opportunities

All of the existing novel nanoelectronic devices to date have relatively long transistor gate length L_g of longer than 50 nm. It is important that these devices exhibit good short channel performance and be scalable below 50 nm and beyond. One meaningful device parameter related to electrostatics and device scalability is the subthreshold slope, measured under high drain bias conditions $V_{\rm DS} = V_{\rm CC}$. Fig. 8 shows the subthreshold slope of planar Si FETs, nonplanar Si FETs (e.g., Tri-gate transistors [5], [6]), CNT FETs, and planar III–V devices. It can be seen that the subthreshold slope and, hence, short channel performance of the planar Si devices degrades on reducing L_g, and that the use of nonplanar architecture, such as, the Tri-gate transistors [5], [6] improves the electrostatics significantly. The subthreshold slopes of the CNT devices are much degraded compared to the Si devices even at relatively long L_g. The reasons for the degraded subthreshold slope are the use of relatively thick gate–oxide and metal source–drain contacts in the current CNT devices. The subthreshold slope of the planar III–V devices is also degraded compared to the Si devices even at relatively long L_g. This is due to the relatively large gate to channel separation in these III–V devices.

One of the technical challenges is to make conventional implanted or diffused P–N junctions in CNT (and also nanowire) devices. The current CNT technology uses metal-CNT contacts to form the source and drain of the transistor, which gives rise to the problems of degraded subthreshold slope and ambipolar conduction. Figs. 9 and 10 show the I_D–V_G characteristics, measured at different drain biases, of the Si nanowire FET and CNT FET, respectively. In both cases, metal source–drain contacts are used (as opposed to conventional implanted source–drain junctions). The data shows the signature of ambipolar conduction in both cases, as shown in Figs. 9 and 10. The energy band diagrams included in Fig. 10 illustrate the mechanism of ambipolar conduction. The energy band diagrams are drawn for an intrinsic CNT with metal source–drain that have p-type work functions.

Results in Section III show that while p-channel CNT devices show significant improvement in intrinsic gate delay over p-channel Si devices, the n-channel CNT devices are not as well established. One of the reasons is that there has been lack of demonstration of a suitable metal with n-type workfunction that forms a stable interface with the CNT. It is expected that upon

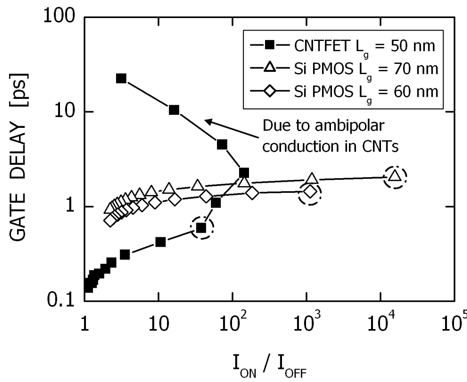

Fig. 11. Gate delay (intrinsic device speed, CV/I) versus on-to-off state current ratio $I_{\rm ON}/I_{\rm OFF}$ of Si PMOS transistors with $L_g = 60$ nm and 70 nm at $V_{\rm CC} = 1.3$ V, and a CNT PMOS transistor with $L_g = 50$ nm and $V_{\rm CC} = 0.3$ V [15]. The three circled points were used in the PMOS CV/I versus L_g plot in Fig. 4, where the V_G swing is anchored around $V_G = V_T$.

solving this problem, a high-performance n-channel CNT FET can be realized due to the symmetry of the conduction and valence band structure of CNT [26].

Fig. 11 shows the gate delay CV/I versus $I_{\rm ON}/I_{\rm OFF}$ ratio for Si PMOS FETs with $L_g = 60$ and 70 nm at $V_{\rm CC} = 1.3$ V, and for a CNT PMOS FET with $L_g = 50$ nm at $V_{\rm CC} = 0.3$ V [15]. The data shows that, in general, CV/I improves with reducing the $I_{\rm ON}/I_{\rm OFF}$ ratio due to the increase in the on-state current from high overdrive, but at the expense of significant increase in $I_{\rm OFF}$. This is true for both the Si devices and CNT. The results show that the p-channel CNTFET has significantly better CV/I over the Si devices for a given $I_{\rm ON}/I_{\rm OFF}$ less than 100 due to the higher effective mobility and lower $V_{\rm CC}$ used for the CNT. The highest $I_{\rm ON}/I_{\rm OFF}$ ratio in the case of CNTFETs is limited by ambipolar conduction, beyond which $I_{\rm OFF}$ will significantly increase while $I_{\rm ON}$ will continue to decrease. This, in turn, causes a loss in gate delay and a reduction in $I_{\rm ON}/I_{\rm OFF}$ simultaneously. This highlights the need for a P–N junction technology for CNTFETs such that the metal source–drain contacts can be replaced with doped semiconducting contacts. It is expected that the subthreshold slope and, hence, the scalability of CNTs, will greatly improve once the metal source–drain contacts can be replaced by a self-aligned P–N junction technology.

We have used dotted circles in Fig. 11 to indicate the CV/I points that were used in the p-channel CV/I versus L_g plot in Fig. 4. These three circled data points represent the CV/I values that were determined with the V_G swing anchored around $V_G = V_T$ (i.e., 2/3 of the $V_{\rm CC}$ swing above V_T to obtain $I_{\rm ON}$ and 1/3 of the $V_{\rm CC}$ swing below V_T to obtain $I_{\rm OFF}$). The significance of these data points are that the CV/I values in this case are not arbitrarily enhanced by employing significant gate overdrive, which results in poor $I_{\rm ON}/I_{\rm OFF}$ ratio.

V. Conclusion

We have benchmarked several important emerging nanoelectronic devices (CNT, Si nanowire, and planar III–V compound semiconductor devices) versus the state-of-the-art planar and nonplanar Si devices in terms of four key device metrics, which are: 1) CV/I versus L_g; 2) energy-delay product versus L_g; 3) sub-threshold slope versus L_g; and 4) CV/I versus $I_{\rm ON}/I_{\rm OFF}$ ratio. The benchmarking results show that while these novel devices hold promise and opportunities for future logic transistor applications, their performance and electrostatics require further improvement and their scalability still needs to be demonstrated. For example, one key area to focus on in CNTs and semiconductor nanowires is to replace the metal source–drain junctions with conventional P–N junctions in order to eliminate ambipolar conduction, improve subthreshold slope, and further enhance the effective channel mobility. This paper emphasizes the importance of *benchmarking* to identify the strengths, as well as the areas of improvement for these emerging nanoelectronic devices, and accelerate the progress in nanotechnology research.

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