

SATA PHY Interface Specification (SAPIS)

Draft – Rev 0.90

February 8, 2002

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Revision History

Rev 0.2, released May 23, 2001

Rev 0.7, released June 28, 2001

Changes in Rev 0.7:

1. Figure 1 updated to show RBC(0:1) instead of a single RBC signal
2. Figure 1 updated to show a single connection for REF_CK on the PHY, as opposed to two occurrences in the previous version.
3. Table 1 updated to describe RBC(0:1) functionality
4. New "Signal Timing" section added in this revision, describing in detail the TX and RX clock architectures and their timing specifications.

Rev 0.71, released October 24, 2001

Changes in Rev 0.71:

1. Require REF_CK to be 25MHz or 100MHz, and provide an input to the PHY to indicate which frequency is present
2. Require the PHY to generate an ASIC_CK clock output at either 150MHz or 300MHz. The output frequency is derived from REF_CK using a PLL. A control line called ASIC_CK_RATE_SELECT determines which clock frequency is produced.
3. Require the ASIC_CK to transition between speeds (when ASIC_CK_RATE_SELECT is changed) without ever producing a high or low level shorter than allowed for 300MHz operation. This means that the ASIC can expect a useable clock even during speed changes.
4. Require the RBC(0:1) clocking scheme to be the same for Gen 1 and Gen 2. The dual clocking approach currently described for Gen 2 will now be used for both speeds.
5. Support 25 Mhz REF_CK input? Decision was made to make 25Mhz an option, but to leave 100Mhz as a requirement
6. Ck behavior in partial/slumber? Decision was made to have the ASIC_CK output remain active in PARTIAL, but to have it be inactive in SLUMBER. Note that internal clocks in the PHY will continue to run in order to support OOB signal detection
7. 300MHz ASIC_CK output required? Decision was made to require GEN2 capable PHY's to provide 150 and 300MHz, but that "GEN1 only" PHY's are only required to provide 150MHz
8. Merge Tx and Rx rate? Decision was made to merge these 2 control lines into a single line called DATA_RATE
9. Must PHY work with SSC on REF_CK? Decision was made that a PHY must support a spread-spectrum REF_CK. A PHY may create SSC from a non-spread REF_CK as a vendor specific feature

Rev 0.72, released November 28, 2001

Changes in Rev 0.71:

1. Added signaling specifications (SSTL_2, PECL)
2. Revised timing specifications

Rev 0.90, released February 8, 2002

Changes in Rev 0.90:

1. Cosmetic changes only

Scope

SAPIS (**S**ATA **P**HY **I**nterface **S**pecification) is intended to enable the development of functionally equivalent SATA PHY's. Such PHY's can be delivered as discrete IC's or as macrocells for inclusion in ASIC designs. The specification defines a set of PHY functions which must be incorporated in a SAPIS compliant PHY, and it defines a standard interface between such a PHY and a link layer ASIC. It is not the intent of this specification to define the internal architecture or design of a compliant PHY chip or macrocell; the SAPIS specification is defined so as to allow various approaches to be used. Where possible the SAPIS specification references the SATA specification rather than repeating its content. SAPIS requires PHY's to support Gen 1 signaling; support of Gen 2 is optional.

Overview of SAPIS PHY Functionality

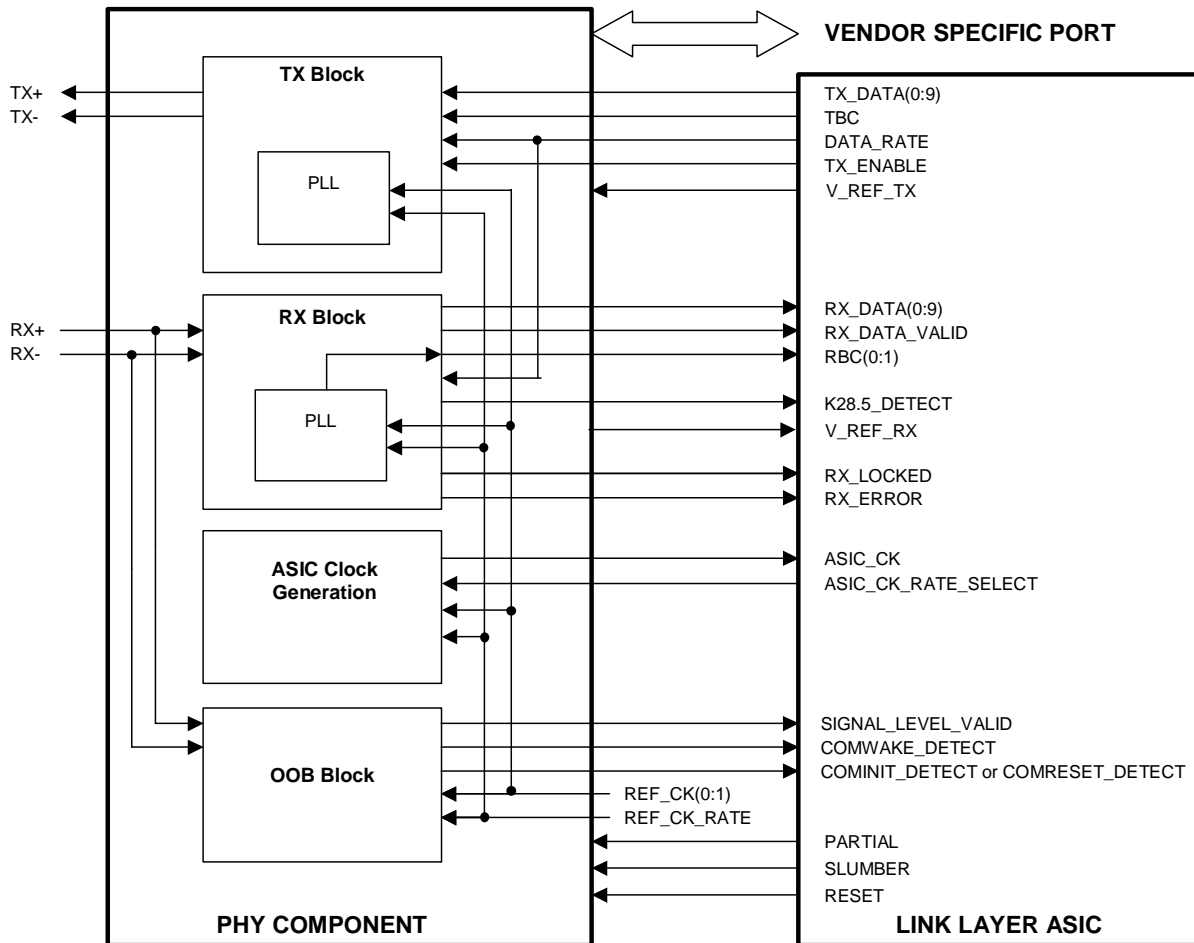


Figure 1 - SAPIS PHY Signals

The PHY input and output signals are described in Table 1. Note that Input/Output is defined from the perspective of a SAPIs compliant PHY component. Thus a signal described as an “Output” is driven by the PHY and a signal described as an “Input” is received by the PHY.

RX Block Signals		
RX+, RX-	Input: SATA	The differential inputs to the PHY. They may be DC or AC coupled to the SATA cable as defined in the SATA specification.
REF_CK(0:1)	Input: PECL	REF_CK(0:1) is the differential reference clock. REF_CK1 is the positive signal component, and REF_CK0 is the negative signal component. Thus a “rising edge” of REF_CK occurs when REF_CK1 rises and REF_CK0 falls. This clock is used by the PLL of tracking receivers or by the DLL of oversampling receivers. REF_CK is also used to generate the TX serial clock and the ASIC_CK signal. Its nominal frequency is either 100MHz or 25MHz. A SAPIs compliant PHY must be able to accept a 100MHz REF_CK, and may optionally accept a 25MHz REF_CK. The applied REF_CK signal is subject to the accuracy, SSC, and jitter behaviors governed by the SATA specification. REF_CK is additionally used for filtering the OOB signaling. Thus COMWAKE_DETECT, COMINIT_DETECT, and COMRESET_DETECT are not useable in the absence of REF_CK.
REF_CK_RATE	Input: SSTL_2	REF_CK_RATE indicates to the PHY whether the REF_CK is 25MHz or 100MHz. A low level indicates 25MHz, and a high indicates 100MHz. A PHY which does not support 25MHz will not have this input.
RBC(0:1)	Output: SSTL_2	RBC(0:1) are the clocks used by the PHY to transfer recovered data to the link layer ASIC. For an oversampling receiver, RBC(0:1) will be frequency locked to the REF_CK signal, although the phase is not specified. For a tracking receiver, RBC(0:1) are phase locked to the incoming data stream and use REF_CK as a reference clock source.
RX_DATA_VALID	Output: SSTL_2	RX_DATA_VALID signal is used for flow control. A high indicates that the concurrent RX_DATA outputs are valid; a low indicates that they should be ignored. RX_DATA_VALID is primarily used by oversampling receivers which can experience RX data underruns (such as occur when an RX block is receiving data from a transmitter whose REF_CK is slower than its own). For tracking receivers, the signal will generally be held high.
RX_DATA(0:9)	Output: SSTL_2	This 10 bit bus delivers the recovered 10b data. The RX block byte aligns the data. Note that RX_DATA bit 0 is the earliest bit received at the RX inputs, and bit 9 is the latest received.

DATA_RATE	Input: SSTL_2	DATA_RATE selects the SATA signaling data rate. A low level selects Gen 1 and a high selects Gen 2 as defined by the SATA specification. A SAPIS PHY is required to support Gen 1 signaling, and may optionally support Gen 2 signaling. A PHY which does not support Gen 2 signaling will not have this input.
K28.5_DETECT	Output: SSTL_2	K28.5_DETECT goes high while the K28.5 control character is present (with either disparity) on the RX_DATA pins. Note that the RX block is allowed to drop any instance of the Align character (as long as it is dropped in its four byte entirety). Oversampling designs will commonly do this as part of their elasticity functionality. Dropping bytes may be accomplished by omitting them at the RX_DATA pins, or by marking them as invalid with the RX_DATA_VALID line. If a K28.5 character is omitted at the RX_DATA pins, K28.5_DETECT goes high during the next byte, even if that byte is marked as invalid.
RX_LOCKED	Output: SSTL_2	RX_LOCKED goes high while three conditions are met: <ol style="list-style-type: none"> 1. The differential input signal exceeds the Squelch Detector threshold as defined by the SATA specification 2. The receiver is locked to the incoming signal 3. The RX byte alignment is correctly established
RX_ERROR	Output: SSTL_2	A high on RX_ERROR indicates that a data reception error has occurred. A PHY vendor is required to document the types of errors indicated by this signal. Examples of possible errors include elasticity buffer overrun and underrun.
V_REF_RX	Output: Reference	V_REF_RX is the reference voltage for the SSTL_2 signals driven by the PHY
TX Block Signals		
TX+, TX-	Output: SATA	The differential outputs from the PHY. They may be DC or AC coupled to the SATA cable, as defined in the SATA specification.
TBC	Input: SSTL_2	TBC is the transmit byte clock used to clock data into the PHY on the TX_DATA bus. TX data transitions occur concurrently with both edges of TBC. Thus TBC will nominally operate at 75MHz for Gen 1, and 150 MHz for Gen2 signaling. TBC is required to be frequency locked to REF_CK and to track its phase (in the presence of SSC, jitter, etc.) The exact timing relationship between TBC and REF_CK is not tightly specified, however.
TX_DATA(0:9)	Input: SSTL_2	The transmitter accepts 10 bit data words as inputs to the serializer on the TX_DATA(0:9) inputs. Note that TX_DATA bit 0 is transmitted first, and bit 9 is transmitted last.

TX_ENABLE	Input: SSTL_2	TX_ENABLE enables the SATA cable drivers in the transmitter portion of the PHY. When this signal is high, the drivers generate normal drive levels. When low, the PHY outputs are idle and maintain common mode bias as specified in the SATA specification.
V_REF_TX	Input: Reference	V_REF_TX is the reference voltage for the SSTL_2 signals driven by the Link Layer ASIC
OOB Block		
SIGNAL_LEVEL_VALID	Output: SSTL_2	SIGNAL_LEVEL_VALID output from the PHY indicates that the differential input signal exceeds the squelch detector threshold. In a situation in which the REF_CK is not being applied to the PHY, this output remains functional. Thus SIGNAL_LEVEL_VALID can be used as a means to awaken a link layer ASIC and/or clock source from a suspended state.
COMWAKE_DETECT	Output: SSTL_2	This output goes high while the criteria for detecting COM_WAKE are met.
COMINIT_DETECT and/or COMRESET_DETECT	Output: SSTL_2	This output goes high while the criteria for detecting COMINIT_DETECT and/or COMRESET_DETECT have been met.
Control Signals		
PARTIAL	Input: SSTL_2	When driven high, PARTIAL places the PHY in its Partial power state as defined by the SATA specification. The ASIC_CK output from the PHY is required to be active in PARTIAL.
SLUMBER	Input: SSTL_2	When driven high, SLUMBER places the PHY in its Slumber power state as defined by the SATA specification. The ASIC_CK output from the PHY is required to be inactive in SLUMBER. Note that the PHY's internal clocks must continue to operate, however, in order to support OOB Signal detection.
RESET	Input: SSTL_2	When driven High, RESET resets all internal state information in the PHY to its default condition. An exception is that state conditions set via the Vendor Specific Port need not be cleared by RESET. Such state conditions must be cleared, however, by power cycling the chip.

ASIC Clock Generation Signals		
ASIC_CK	Output: SSTL_2	ASIC_CK is a signal generated by the PHY for the purpose of clocking the Link Layer ASIC. ASIC_CK is required to be 150MHz for PHY's which only support Gen 1 signaling. It is required to operate at both 150MHz and 300MHz for Gen 2 capable PHY's. ASIC_CK is required to transition between speeds (when ASIC_CK_RATE_SELECT is changed) without ever producing a high or low level shorter than allowed for 300MHz operation. This means that the ASIC can expect a useable clock even during speed changes.
ASIC_CK_RATE_SELECT	Input: SSTL_2	ASIC_CK_RATE_SELECT determines which clock frequency is produced on the ASIC_CK output. A low level produces 150MHz, and a high level produces 300MHz. A PHY which does not support Gen 2 signaling will not have this input.

Table 1 – PHY Input/Output Signals

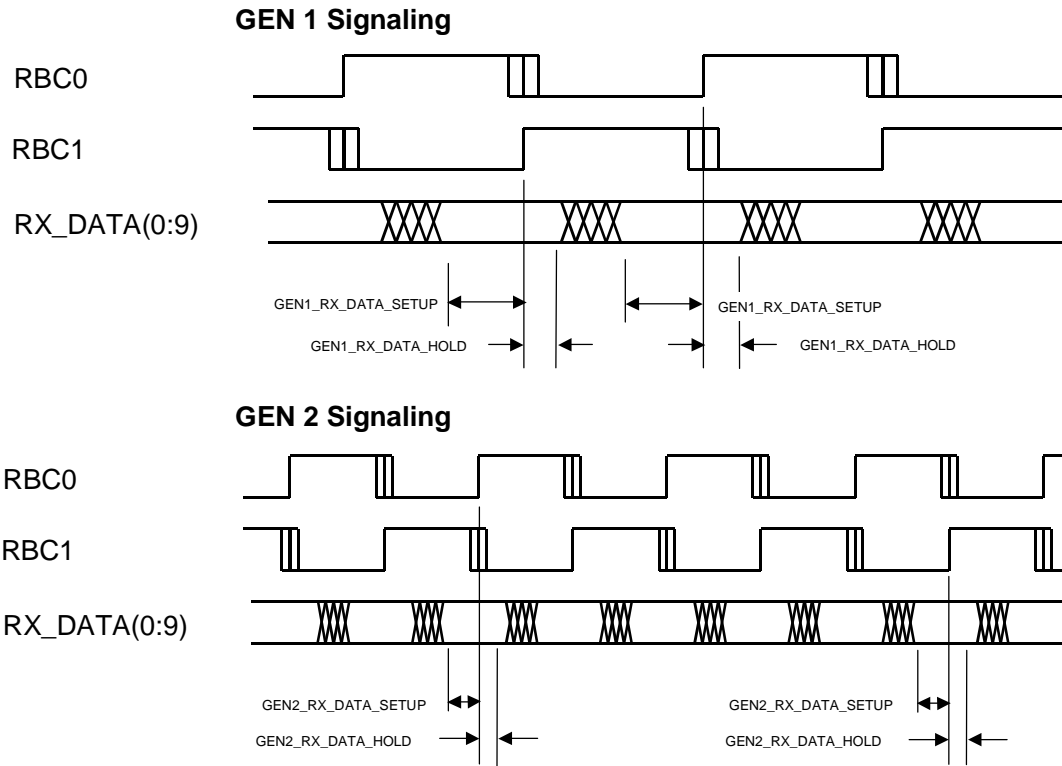
Vendor Specific Port

A PHY vendor may optionally add a Vendor Specific Port (VSP) to a PHY component. Such a port allows access to a superset of the PHY functionality required by SAPIS. Such access may include, but is not limited to, features for testability, internal signal visibility, compliance testing, system debug, and component characterization. If a VSP is incorporated, it must conform to the following requirements:

1. All VSP pins must be internally pulled high or low to a default condition.
2. Leaving VSP pins in their open, default condition must cause the PHY to operate as if there was no VSP.
3. There must be no vendor-defined control sequences required at the VSP to enable the chip to operate correctly.
4. State conditions established via the VSP must be reset to default values when the component is power cycled.
5. State conditions established via the VSP need not be reset when the PHY RESET pin is driven high.

Signal Timing

Receive Timing



Receive Timing (PHY delivers data to link layer ASIC)

Figure 2 - Receive Timing

When RX data is being delivered from the PHY to the link layer ASIC, RBC0 and RBC1 are used to clock data into the Link Layer ASIC as shown in Figure 2.

Note: The RBC clock(s) are not generally synchronous to the ASIC_CK signal, so the link layer ASIC must incorporate the required elasticity buffering.

Table 2 specifies the timing with which data must be delivered by the PHY. These timing relationships are depicted in Figure 2.

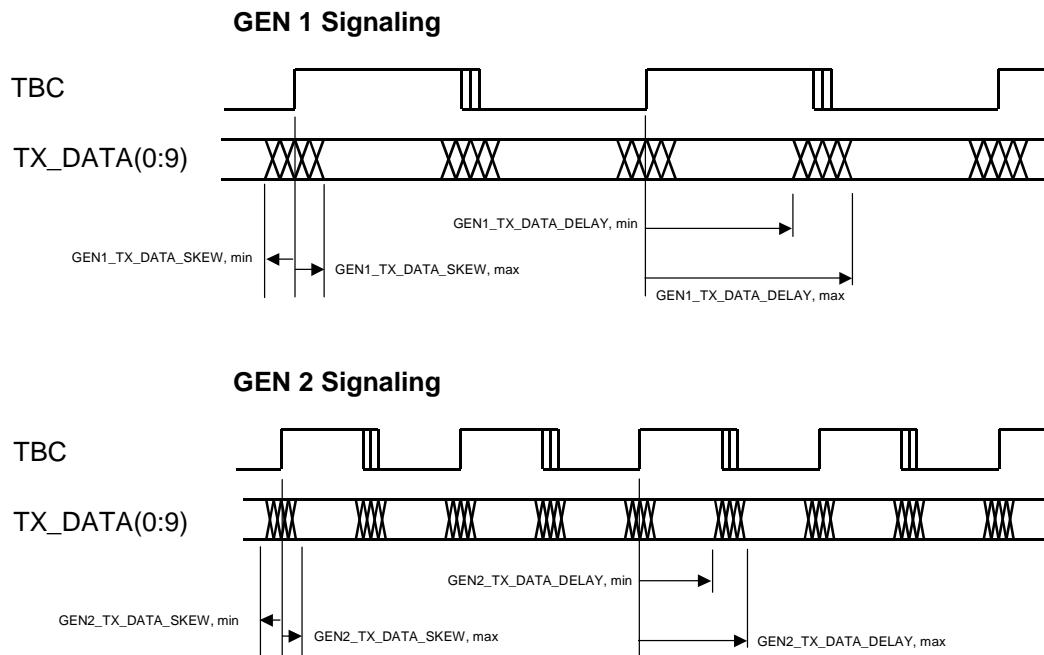
PHY Output Timing			
	Min	Max	Units
GEN1_RX_DATA_SETUP	3.0	-	ns
GEN1_RX_DATA_HOLD	0.3	-	ns
GEN2_RX_DATA_SETUP	1.8	-	ns
GEN2_RX_DATA_HOLD	0.3	-	ns

Note 1: Setup and Hold specifications must be met relative to rising edges on both RBC0 and RBC1

Table 2 – PHY Output Timing

Transmit Timing

When TX data is being delivered from the link layer ASIC to the PHY, TBC is provided as a clock reference (rather than as a true clock) by the Link Layer ASIC. The PHY uses the TBC clock reference for receiving TX data as shown in Figure 3. Because the TBC signal transitions occur concurrently with the transmit data, and because the TBC signal operates at “half speed”, it is straightforward for the link layer ASIC to generate TBC with the same output structures as the data signals, thereby minimizing timing skew.



Transmit Timing (Link layer ASIC delivers data to PHY)

Figure 3 – Transmit Timing

A SATA PHY may incorporate a PLL to generate the clock for sampling the TX data at the specified times. It is required that such a PLL use only the rising edges of TBC for controlling the times at which the TX data is sampled.

It is strongly recommended that a SATA PHY use REF_CK (rather than TBC) as the clock reference for the transmit PLL which generates the serial data clock.

Table 3 specifies the required timing for the link layer ASIC outputs to the PHY. These timing relationships are depicted in Figure 3. A link layer ASIC which only supports Gen 1 data rates is required to meet the Gen1 timing specifications. A link layer ASIC which supports Gen 1 and Gen 2 data rates is required to meet the timing specifications for the speed at which it is operating.

Link Layer ASIC Output Timing			
	Min	Max	Units
GEN1_TX_DATA_SKEW	- 1.500	+ 1.500	ns
GEN1_TX_DATA_DELAY	5 Gen 1 bit times – 1.500ns	5 Gen 1 bit times + 1.500ns	
GEN2_TX_DATA_SKEW	- 0.750	+ 0.750	ns
GEN2_TX_DATA_DELAY	5 Gen 2 bit times – 0.750ns	5 Gen 2 bit times + 0.750ns	

Note 2: GEN1_TX_DATA_SKEW and GEN2_TX_DATA_SKEW limits apply to the data transitions that occur concurrently with rising edges of TBC.

Note 3: GEN1_TX_DATA_DELAY and GEN2_TX_DATA_DELAY limits apply to the data transitions that occur concurrently with the falling edges of TBC.

Table 3– Link Layer ASIC Output Timing

System Design Notes

A system which utilizes a SAPIS PHY must implement certain functions:

Receive path requirements:

1. The Link Layer ASIC must receive data synchronous to the RBC clock signal.
2. The receive portion of the Link Layer ASIC must incorporate an elastic buffer of sufficient depth to accomplish rate matching between the PHY and the Link Layer ASIC. While some PHY's may make this unnecessary, PHY's which utilize tracking architectures will require it. The elastic buffer must be able to recognize and drop align characters as needed to prevent overruns.
3. The Link Layer ASIC must accept the RX_DATA_VALID signal from the PHY as an input, and must correctly implement flow control by ignoring invalid bytes.

Transmit path requirements:

1. The Link Layer ASIC must deliver TX data synchronous to the TBC clock signal
2. The TBC clock from the ASIC must maintain a fixed phase relationship to the REF_CK signal even in the presence of SSC, jitter, etc.
3. Because the TX Block drives serial data with a clock derived from REF_CK, REF_CK must be a suitable reference for meeting all SATA jitter and timing specifications. For example, the Gaussian jitter of REF_CK (expressed as a percentage of a single 150MHz period) should be no more than the percentage allowed on the wire for the actual signaling UI.

Out of Band Detection:

1. Because a SAPIS PHY uses REF_CK to measure OOB signal timing, REF_CK must be present to detect OOB signaling. If a design shuts down REF_CK for power management, the SIGNAL_LEVEL_VALID output should be used to start REF_CK.

K28.5_DETECT signal usage:

Because the second, third, and fourth bytes of an ALIGN Character are indistinguishable from data, the SAPIS spec requires that if any byte of an ALIGN is dropped, the entire ALIGN must be dropped. Dropping a byte is accomplished by either omitting the byte entirely at the RX_DATA pins, or by marking the byte as invalid by holding the RX_DATA_VALID signal low while the byte is on the RX_DATA pins. A SAPIS PHY may use any combination of these two techniques within an ALIGN character that's being dropped.

So, given the pin behaviors currently specified, here's how a Link Layer ASIC should react to a K28.5_DETECT so as to get Byte 0 alignment:

1. When K28.5_DETECT goes high, the Link Layer ASIC must test whether the current byte (whether valid or not) is a K28.5.
2. If yes and valid, the Link Layer ASIC knows that the current byte and the next three valid bytes are an ALIGN. Thus the next valid byte after that is either Byte 0 or another ALIGN.
3. If yes and not valid, the Link Layer ASIC knows that an ALIGN is detected by the PHY but that it will be dropped in its entirety. Thus the next valid byte is either Byte 0 or another ALIGN.

4. If not K28.5, the Link Layer ASIC knows that an ALIGN is detected by the PHY but that it will be dropped in its entirety. Thus the next valid byte (which could potentially be the current one) is either Byte 0 or another ALIGN.