

System Architectures for High-rate Ultra-wideband Communication Systems: A Review of Recent Developments

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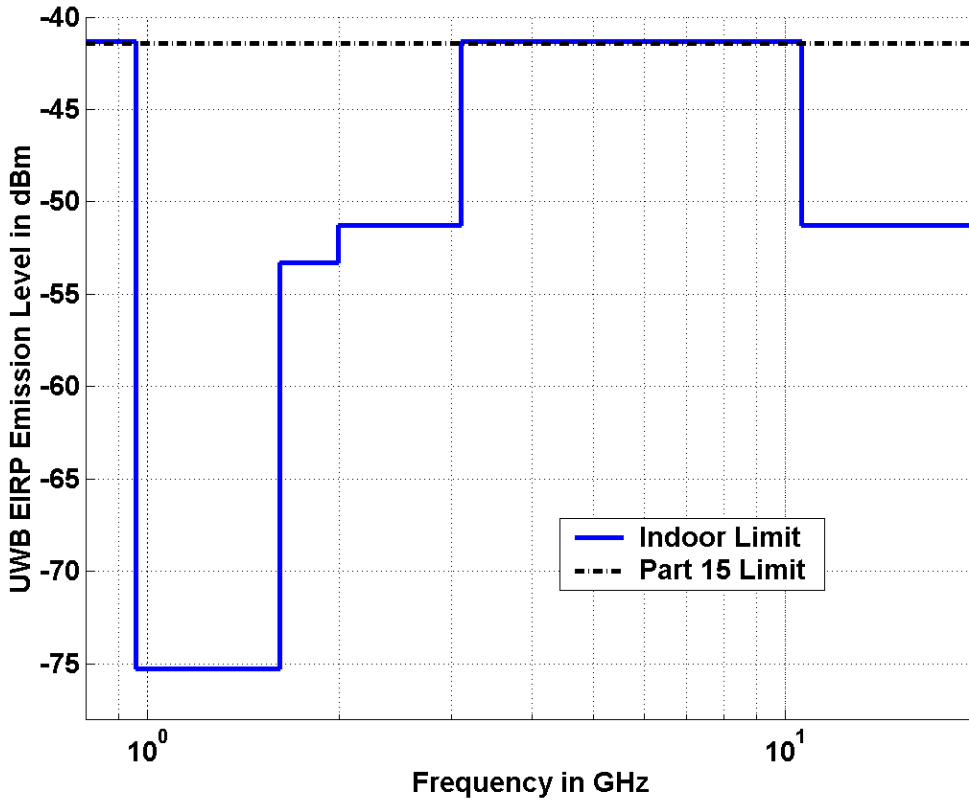
I. INTRODUCTION

Ultra-Wideband (UWB) was approved by the Federal Communications Commission (FCC) in Mar. 2002 for unlicensed operation in the 3.1-10.6 GHz band subject to modified Part 15 rules. The rule limits the emitted *power spectral density* (*p.s.d*) from a UWB source measured in a 1 MHz bandwidth at the output of an isotropic transmit antenna at a reference distance to that shown in Figure 1. Further, the transmitted signal must instantaneously occupy either i) a fractional bandwidth in excess of 20% of the center frequency or ii) in excess of 500 MHz of absolute bandwidth to be classified as a UWB signal. The maximum allowable p.s.d for UWB transmission of -41.3 dBm/MHz corresponds to approximately 0.5 mW of average transmit power when the entire 3.1-10.6 GHz band is used, effectively limiting UWB links to short ranges. Nevertheless, the potential for exploiting such low power UWB links for *high data rate* wireless PAN connectivity (in excess of 100 Mbps) at ranges up to 10 m particularly for in-home networking applications has led to considerable recent interest in this technology.

The combination of the ultra-wide bandwidths and low average transmitted power presents unique challenges for UWB radio design. Such large bandwidths imply highly frequency selective multipath channels, with a large number (order of hundreds) of resolved multipath components¹. Due to stringent limitations on average and peak transmit power, power efficient modulation schemes such as binary pulse (amplitude and/or position) modulation are typically used for UWB signaling; to increase data rate therefore requires scaling of the PRF which in turn leads to increased inter-symbol interference in a strong multipath environment that necessitates costly equalization and/or coding to meet performance specifications. An alternative for higher data rates is to employ power efficient M-ary orthogonal signaling schemes although they require higher bit SNR at the receiver input.

¹ Pursuant to the IEEE standards process, the 15.3a created standard multipath channel models and specified minimum receiver performance requirements (desired packet error rates for rate/range combinations) as part of selection criteria for a basis for comparison of different proposals.

Figure 1: UWB Spectral Mask Per FCC (Modified) Part 15 Rules



UWB devices are expected to organize in typical clusters that may overlap due to close proximity of multiple clusters. This points to a need for effective multiple accessing techniques to manage co-existence of simultaneous piconets. Further, due to mobility of client UWB enabled devices, some form of ad-hoc networking mechanism is desired to support topology changes (i.e. leaving and joining by devices in a cluster). Finally, since it is inevitable that UWB transmission will overlay legacy narrowband services, possibly in very close proximity – for example, a laptop/PDA in the future may have integrated 802.11 and UWB transceivers at separations of few inches. Thus UWB system design must also allow for narrowband interference (NBI) mitigation to preserve link integrity.

This paper presents an overview of the system architecture aspects of high data rate UWB link layer design and provides a brief synopsis of recent candidate proposals to the IEEE 802.15.3a standards task group. Emphasis is placed on the circuit design and implementation issues and their inter-relation with important link design objectives such as system BER performance, power dissipation and silicon complexity/cost. The paper is organized as follows – Sec. II provides an overview of the main design considerations for a successful UWB system. Sec. III then summarizes the salient aspects of representative proposals based on both impulse and carrier based approaches that impact system realization and performance.

II. OVERVIEW OF UWB SYSTEM ARCHITECTURE CONSIDERATIONS

To meet the size, cost, and power consumption demands of consumer applications, a single-chip UWB transceiver architecture with few external components is desired. This level of integration has been achieved in systems like Bluetooth although this is not an easy design to realize and there are performance penalties. While there are a number of different fabrication options for UWB, CMOS is particularly compelling due to its low cost and low power consumption. Poor passive components and the lower operating voltages associated with process scaling pose significant problems for the radio architect and designer.

The relatively low breakdown voltages of CMOS transistors limit both peak transmit RF power and receiver dynamic range. This fits UWB well since parallel or magnetic coupled structures are not required to meet the sub-milliwatt average transmit power. However since peak power is also limited, the peak to average power ratios (PAPR) of the proposals is an important consideration. Since the envisioned UWB systems operate over a relatively short range, the receiver requires only ~40dB dynamic range to process UWB signals. However the anticipated presence of strong narrow band interferers (NBI) within the receiver passband could be as much as 60dB above the UWB signal. Most of the proposed standards provide methods to mitigate NBI but they all rely on linear processing in the receiver front end. The linearity and dynamic range requirements imposed by NBI is one of the more difficult challenges of UWB receiver architecture.

All but the lowest performance radio receivers use some form of filtering to select the desired frequency range and UWB is no exception. However its large fractional bandwidth can provide some headroom to mitigate variations of fabrication process, operating voltage and temperature (PVT). For example a 1 percent variation in center frequency of a filter could render a narrow band receiver whose fractional bandwidth is 1% useless whereas a UWB receiver would only be degraded by $\frac{1}{\beta}$ where β is the (percent) fractional BW of the UWB receiver (thus for $\beta = 25$, the degradation is 4%). Due to the high cost of external filters, realization of these filters on-chip is essential.

On-chip noise or interference can potentially be more difficult for UWB compared to narrow-band systems. Digital clocks can produce significant EM radiation which can be difficult to isolate and their fundamental or harmonic frequencies are likely to fall within the bandwidth of the RF and baseband circuits. Thus tricks such as shifting the clock frequency so its harmonics fall out of band or spreading the spectrum of a clock have a lower probability of success in UWB architectures. On-chip isolation requirements are not addressed by the current proposals and will require further research.

Beyond single-chip UWB transceiver design is the issue of integration with other needed functionalities to make a complete user device on one chip. Such an overall device would host primarily digital circuits and use digital-only CMOS processes which have very limited support for analog circuit elements such as resistors, capacitors and low noise or high dynamic range amplifiers. If we are ever to achieve this level of integration it is clear that a single chip CMOS radio is the place to start. In solving the on-chip interference problems of the single-chip UWB transceiver, we will be better prepared to address the more challenging interference issues of single-chip devices.

As Moore's law predicts, the shrinking of CMOS feature sizes will continue to reduce the cost and power consumption of digital circuits. However shrinking of feature sizes (scaling) is often a problem for analog circuits. Capacitors and inductors do not scale with process because their physical size is a function of the required reactance and the materials used. Also, lower operating voltage associated with scaling makes high dynamic range circuits more difficult to realize. For these reasons UWB architectures that rely more heavily on digital processing have the potential to cost less and use less power in coming years. For these reductions to be meaningful, however, careful attention must be paid to power consumption and die area of the analog circuits as these can easily swamp any savings in the digital domain. UWB systems and radio architectures that rely heavily on digital processing and have the lowest possible power consumption and die area in the analog domain have a distinct advantage.

Due to the low transmit RF power, most of the concern about power consumption in UWB transceivers is in receive mode. This is especially important in portable devices where energy use in receive and stand-by modes is usually the dominant factor in battery life. In receive mode, the architectures under review burn most of their analog power in the ADC, LNA and baseband filters in that order.

Analog-Digital-Converter (ADC) power consumption

Flash ADC architecture is the rule-of-thumb choice [9] for the sample rates and resolution required for the proposed UWB architectures. These converters use a preamplifier to drive an array of 2^n comparators which can quantize the sample with n bits of resolution. Estimating the power consumption of these converters depends on many variables but it has been shown [9] that, in general, for each additional bit of resolution, the power consumed by the comparators grows by a factor of two where the power used in the preamplifier grows by a factor of four. Also, due to the gate capacitance of the comparator array, the preamplifier consumes more power in order to meet the settling time requirements of higher sample rates and input bandwidth. So to keep power consumption to a minimum the architect can choose either a high sample rate (GHz) or high resolution (5+ bits) but not both. The effect of this trade space can be seen in the choices made in the proposals as summarized in table 1.

Table 1. Analog Digital Converters required by the proposals

System	Qty	Rate	Resolution
PPM	1 (real)	20GHz	1-bit
DSSS	2 (IQ)	1GHz	1-bit
ODFM	2 (IQ)	528MHz	4-bit
MB	2 (IQ)	333MHz	5-bit

LNA and filters

The primary factors in choosing an LNA scheme are noise figure, dynamic range, linearity and power consumption. All of the proposals reviewed in this paper allocate ~7dB to the overall system noise figure. This calls for an LNA scheme with a noise figure of ~3dB which can be difficult to achieve in CMOS given the bandwidth. The common practice of using narrow band impedance matching circuits to optimize the noise figure is not an option. To meet the dynamic range requirements of NBI cases the LNA circuits must operate at relatively high voltages, employ distributed architectures or reduce the NBI signal power at input with notch filters. One approach is to use the off-chip band selection filter to reject expected NBI sources such as 5GHz WLAN. But in addition to distorting a part of the UWB spectrum, such *fixed* schemes do not protect against potential new NBI sources that will eventually appear; this points to the need for *adaptive* notch filtering. These filters are very difficult to realize on-chip, however, due to the relatively poor passive components available in CMOS. Also through possible spurious EM coupling, the effect of the filter can be negated unless it is well isolated. This can lead to a physically large on-chip filter structure.

UWB Transmitter Design Issues

Many UWB modulation schemes are based on some form of (im)-pulse modulation where the pulse shape and duration is used to control the bandwidth occupancy of the transmitted signal and repetition frequency (PRF) essentially determines the information rate. Needless to say, choice and generation of an appropriate pulse shape that potentially spans 500 MHz- several GHz subject to the FCC's spectral mask is a considerable challenge. As has already been indicated, the pulse shape design must meet the sometimes conflicting requirements – a) efficiently filling the FCC spectrum mask for maximum allowable transmit power while b) minimizing anticipated inter-symbol (and in the case of DS-UWB, inter-chip) interference and c) provide spectral flexibility as a method to coexist with other radio systems that may be present.

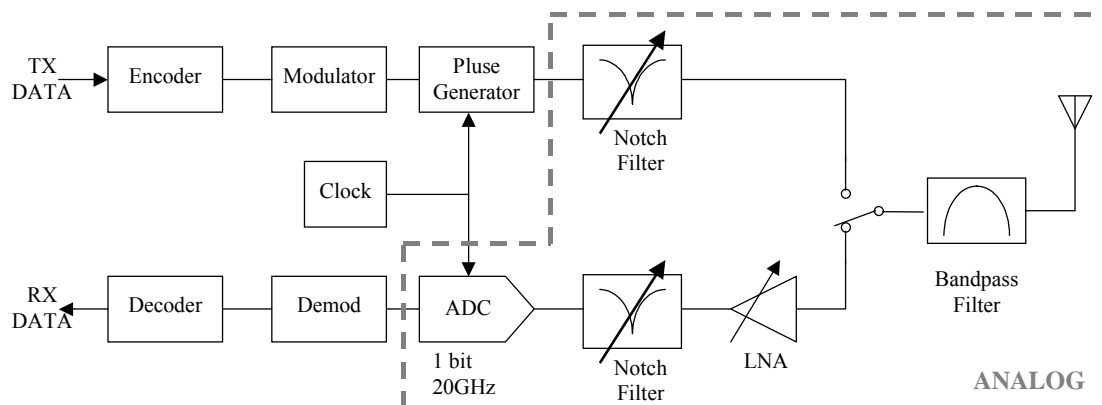
Typical impulse based systems use transition generators with edge rates designed to occupy 3 GHz of bandwidth or more. While others systems use various forms of gated frequency generators where the edge rates are selected to spread the energy around the fundamental frequency of the generator.

III. PROPOSED SYSTEM ARCHITECTURES

Pulse Position Modulation

An impulse based system proposed by Didier Héjal, et all, [7] uses pulse position and polarity to create a bi-orthogonal modulation scheme capable of sending up to three bits per pulse. As shown in Figure 2, the receiver architecture uses direct RF sampler operating at 20GHz followed by 1280 parallel digital matched filters. During preamble reception, the training sequence is used to estimate the channel response with 50ps resolution. Since the sampler is a single bit, the channel estimates can be updated with a simple increment or decrement operation. Once trained, the matched filters capture energy from the channel like an infinite rake. Since the RAKE architecture is an *adaptive* matched filter, the transmitted pulse can be shaped as needed to create holes in the spectrum which can be used for coexistence or regulatory issues.

Figure 2. Proposed PPM Transceiver Architecture



To achieve the required 110Mb/s effective throughput, pulses are modulated using 2PPM + polarity at a rate of 156MHz. This two bit per symbol mode combined with rate 1/3 convolutional code yields 123Mb/s delivered to the MAC layer. This system is predicted to deliver 110Mb/s @ 10 meters with a combined link and implementation margin of 6.8dB. Due to the parallel architecture, most of the digital circuits operate at a relatively low clock rate of $1/PRF = 15.6\text{MHz}$. Due to its estimated 175K gates, however, the channel estimator is the dominant power consumer. To reduce power consumption, enhancements are proposed to the MAC protocol such that the duty cycle of these circuits can be held to 10 percent. In this mode the average power consumption of the complete receiver is estimated at 200mW. Die area for the transmitter and receiver is estimated to be less than 5mm^2 in $0.13\mu\text{CMOS}$.

Direct Sequence Spread Spectrum

Fujita, et all, [5] proposed a direct sequence spread system architecture, shown in Figure 3, using $\pi/2$ BPSK modulation with a chip rate of 1GHz. Alternating 2ns pulses on

I and Q channels yields a signal with a constant envelope easing CMOS implementation. The emission bandwidth is 2GHz and can be used with center frequencies of 4, 7 & 9GHz. This frequency plan is designed to enable future expansion as CMOS technology improves and to reduce energy put into the collective worldwide 5GHz WLAN bands. Date rate adaptation is accomplished by varying spreading factors as show in table 2.

Figure 3. Proposed Direct Sequence – UWB System Architecture

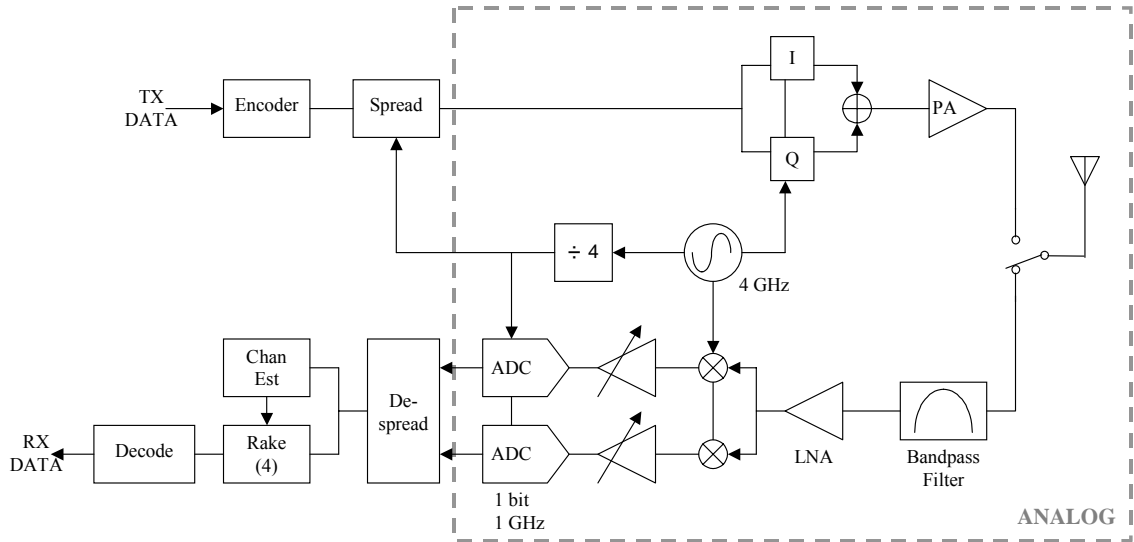


Table 2. DSSS Rate adaption

Spreading factor (N _{ss})	Raw data rate
8	125Mb/s
5	200Mb/s
2	500Mb/s
1 (no spreading)	1Gb/s

A flexible FEC scheme uses Convolutional ($r=1/2$, $K=7$) and Reed Solomon (240, 224, 16) codes either individually or concatenated. Under high SNR conditions power consumption can be reduced since the Viterbi decoder is not required. The receiver evaluated performs preamble acquisition and channel estimation concurrently which is facilitated by 4x oversampling rate (4GHz). Four parallel digital despanders reduce search time and increase SNR of the preamble by coherently adding preamble segments. These same despanders are later used as four rake fingers to collect energy dispersed by the channel.

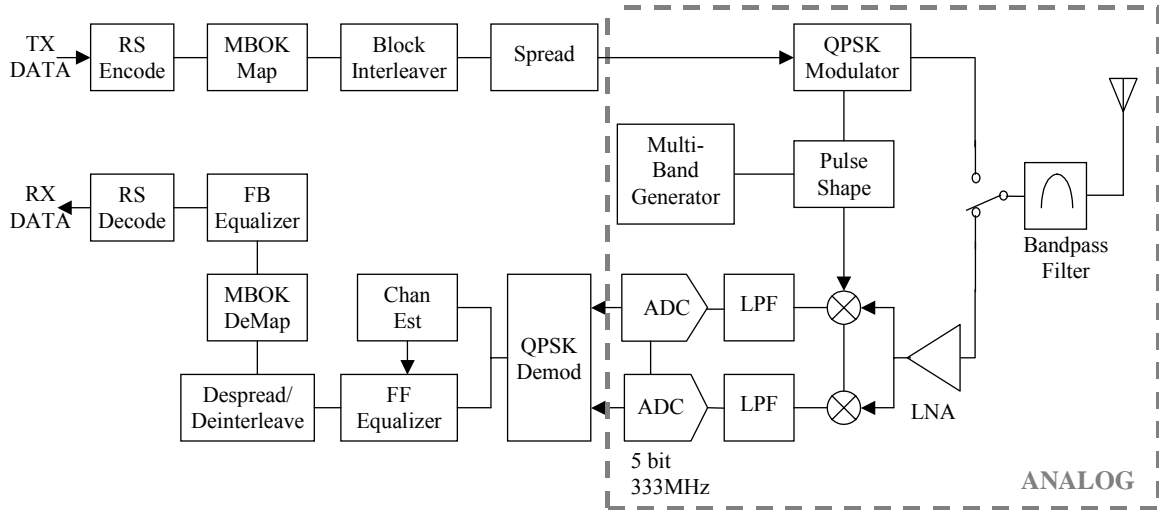
As the path loss is lowest at 4GHz, initial CMOS implementations are envisioned to use this channel due to the relaxed noise figure and phase noise requirements. Combined link and implementation margin is predicted to be 7.7dB when delivering

115Mb/s @ 10 meters range. More coding gain or lower noise circuits may be needed for the 7 & 9GHz channels, as the margin drops to 2.8dB and 0.7dB respectively. Receiver power consumption is estimated at 150mW for 115Mb/s and die area is estimated at 5-6mm² in 0.18u CMOS.

Multiband Architectures

There were a number of proposals submitted which we classify as multiband since this is their primary method to achieve performance scaling, multiple access & coexistence. Here the UWB band is sub-divided into multiple (N) sub-bands each of which exceed 500 MHz to meet the FCC requirements. Individual pulses are transmitted sequentially in time over these sub-bands yielding a band-hopping modulation scheme, where the pulse repetition frequency in each sub-band is $\frac{1}{N}$ of a comparable single-band system. The lower PRF mitigates the performance requirements on the equalizer while the time-sequencing of pulse transmission avoids the high peak-to-average ratio (PAR) problem encountered in multi-carrier systems such as OFDM where all sub-carriers are used simultaneously. Multiband systems propose to drop sub-bands as needed to address coexistence and world wide regulatory compliance issues.

Figure 4. Multi-band UWB System Architecture



Foerster, et al, [8] proposed a system that uses 13 sub-bands each 550MHz wide with the first band centered at 3.6GHz. The transceiver, as shown in Figure 4 forms symbols by emitting QPSK modulated pulses 3ns in duration. A -10dB bandwidth of ~700MHz for the pulse is achieved by applying a rectified cosine envelope to the pulse. Four symbols are emitted sequentially one band at a time according to a time-frequency coding scheme. This scheme enables the use a single RF conversion chain. To resolve the ISI caused by the close spacing of the symbols, an interleaved M-ary Binary Orthogonal Keying (MBOK) scheme is used such that the receiver can use a relatively simple decision

feedback equalizer. An outer Reed-Solomon (221, 255) code is added to correct for burst errors. Assuming a 7dB system noise figure, when operating in the lower set of seven sub-bands and the IEEE channel models, the system is predicted to deliver 108Mb/s @ 10 meters with a combined link plus implementation margin of 9.3dB.

OFDM Architecture

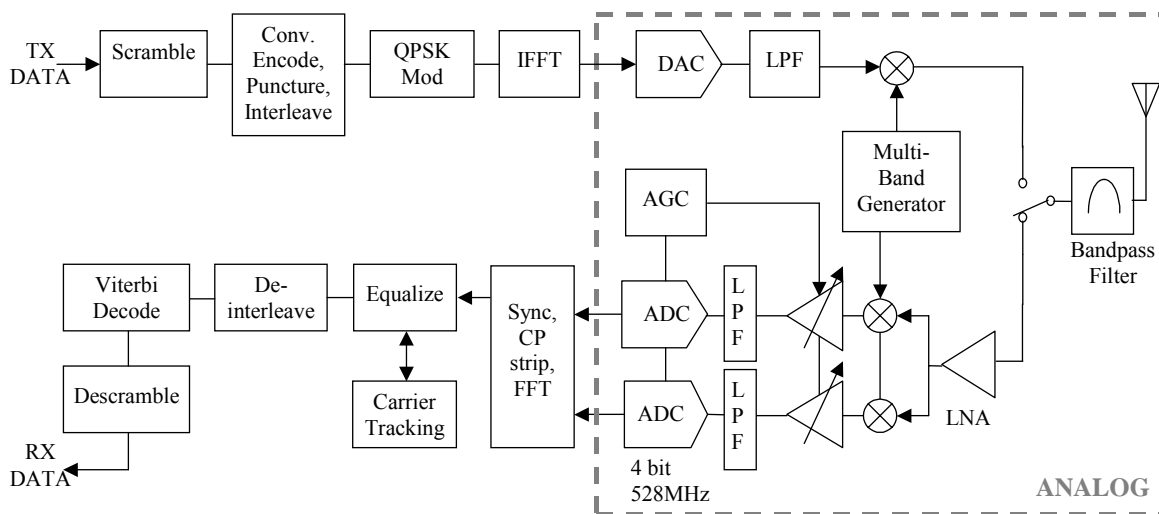
Batra, et al, [6] proposed a time-frequency interleaved OFDM architecture as shown in Figure 6. This system operates in the 3.1 to 4.6GHz section of UWB band. The 5GHz UNII band is not used and frequencies above this are reserved for later use. The operating band is divided into three sub-bands each 528MHz wide.

OFDM symbols are 312.5ns in duration and are emitted one sub-band at a time. A 9.5ns guard time is included to allow the transceivers to hop to the next frequency. The OFDM symbol has 128 tones (128 point FFT) each 4.125MHz wide for a symbol bandwidth of 528MHz. The tones are allocated as follows:

- 100 tones carry data using QPSK modulation (2bits per tone)
- 12 tones are pilots which can be used for phase tracking etc.
- 10 tones are user defined
- 6 remaining tones including DC are null

The DC tone is null to allow direct conversion receivers to block any DC caused by on-chip LO leakage. The other null tones are used to make holes in the spectrum for world wide regulatory compliance. User defined tones do not carry information but their presence can be used by the implementer in conjunction with the post DAC filter to meet the FCC minimum bandwidth and spectral mask rules. A raw data rate of 640Mb/s results from 100 data tones with two bits per tone sent at a symbol rate of 3.2Ms/s (312.5ns).

Fig. 6. OFDM-UWB System Architecture



Information bits are interleaved over all three sub-bands to provide frequency diversity and a $K=7$ convolutional code is added to extend range. The resulting data rates are summarized in Table 3.

Table 3. OFDM Data Rates

Information rate	code rate (K=7)	Spread rate	Information tones
110Mb/s	11/32	2	50
200Mb/s	5/8	2	50
480Mb/s	3/4	1	100

To combat multipath a cyclic prefix of 60.6ns is prepended to the OFDM symbol to maintain orthogonality in FFT processing. Simulation results in the proposal predict less than 0.1dB energy loss in collecting energy from the expected multipath channels. This in effect supplants the need for rake structures employed by other proposed architectures.

When normalized to a 7dB system noise figure, this system is predicted to deliver 110Mb/s @ 10 meters with 8.1dB combined link and implementation margin. For data rates up to 200Mb/s the OFDM transmitter does not need complex DAC which may be used to save power or die area in less demanding devices. For 110Mb/s operation implemented in 0.13u CMOS, power consumption is estimated at 117mW in transmit mode and 205mW in receive mode. Die area for the analog circuits is estimated at 3mm² and 3.8mm² for digital.

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