Intel® Core™ Microarchitecture

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Continuing From Last Fall’s IDF...

Let’s Take A Look Inside
Intel® Core™ Microarchitecture
The Energy Efficient Performance Leader

Core™ Microarchitecture: Higher Performance AND Lower Power

Platform Capabilities

Performance
Energy Consumption

Perf ↑
Energy ↓

Platform – Level
Energy Efficient
Performance

DP Performance Per Watt
Comparison with SPECint_rate
at the Platform Level

Woodcrest H2 ‘06
Dempsey MV H1 ‘06
Paxville DP H2 ‘05
Irwindale H1 ‘05

Source: Intel®
History

Microarchitecture and Architecture

- i486™ 1989
- Integrated FPU
- Pipelining
- Branch Prediction
- Superscalar
- Pentium® Pro 1995
- Out Of Order
- Register Renaming
- Speculative Execution
- Pentium® III 1999
- NetBurst™
- SSE
- SSE 2
- Pentium® 4 2000
- Hyper Threading
- Pentium® M 2003
- Xeon™ 2002
- Xeon® 2004
- Itanium® 2001
- Epic
- Power Management
- Micro Fusion

*Graphics not representative of actual die photo or relative size
Historical Driving Forces

- **Increased Performance via Increased Frequency**
  - Frequency (MHz)
  - Graph showing growth from 1970 to 2020

- **Shrinking Geometry**
  - Feature Size (μm)
  - Graph showing decrease from 1970 to 2020

- **1946**
  - 20 Numbers in Main Memory

- **1971**
  - I4004 Processor
  - 2300 Transistors

- **2005**
  - 65nm
  - 1B+ Transistors
The Challenges

Power Limitations

Supply Voltage (V)

Diminishing Voltage Scaling

Power = Capacitance x Voltage^2 x Frequency
also
Power ~ Voltage^3
Energy Efficient Performance – High End

**NASA Columbia**
- 2 MWatt
- 60 TFlops goal
- 10,240 cpus – Itanium II
- $50M
- 30,720 Flops/Watt
- 1,288 Flops/Dollar

**ASC Purple**
- 6 MWatt
- 100 TFlops goal
- 12K+ cpus – Power5
- $230M
- 17,066 Flops/Watt
- 467 Flops/Dollar

Source: NASA
Source: LLNL
A New Era...

**THE OLD**
- Performance Equals Frequency
- Unconstrained Power
- Voltage Scaling

**THE NEW**
- Performance Equals IPC
- Multi-Core
- Power Efficiency
- Microarchitecture Advancements
Intel® Core™ Microarchitecture

Low Power

- Intel® Wide Dynamic Execution
- Intel® Intelligent Power Capability
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Advanced Digital Media Boost

High Performance

- Server Optimized
- Desktop Optimized
- Mobile Optimized

Scalable

- Woodcrest
- Conroe
- Merom

65nm

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### Intel® Wide Dynamic Execution

#### EACH CORE

- **Efficient**
  - 14 Stage Pipeline
- **Deeper Buffers**
- **4 Wide - Decode to Execute**
- **4 Wide - Micro-op Execute**
- Micro and Macro Fusion
- **Enhanced ALUs**

#### CORE 1

1. Instruction Fetch and Pre-decode
2. Instruction Queue
3. Decode
4. Rename / Alloc
5. Retirement Unit (Reorder Buffer)
6. Schedulers
7. Execute

#### CORE 2

1. Instruction Fetch and Pre-decode
2. Instruction Queue
3. Decode
4. Rename / Alloc
5. Retirement Unit (Reorder Buffer)
6. Schedulers
7. Execute

### ADVANTAGE

- 33% Wider Execution over Previous Gen
- Comprehensive Advancements
- Enabled In Each Core
Intel® Wide Dynamic Execution
Micro and Macro Fusion

**MACRO FUSION EXAMPLE**
**CMP+JMP IN 1 CLOCK**

**WITH MACRO FUSION**
- INSTRUCTION 3
- INSTRUCTION 2
- INSTRUCTION 1
- DECODE
- COMBINED INST 2 & 3
- INTERNAL INST 1
- EXECUTE
- COMPLETED INST 3
- COMPLETED INST 2
- COMPLETED INST 1

**WITHOUT MACRO FUSION**
- INSTRUCTION 3
- INSTRUCTION 2
- INSTRUCTION 1
- DECODE
- INTERNAL INST 3
- INTERNAL INST 2
- INTERNAL INST 1
- EXECUTE
- COMPLETED INST 3
- COMPLETED INST 2
- COMPLETED INST 1

**ADVANTAGE**
- Instruction Load Reduced ~ 15%**
- Micro-Ops Reduced ~ 10%**

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** Workload dependant
Intel® Intelligent Power Capability

- **Process**
  - 65nm
  - Strained Silicon
  - Low-K Dielectric
  - More Metal Layers

- **Coarse Grained**
  - Aggressive Clock Gating
  - Enhanced Speed-Step

- **Ultra Fine Grained**
  - Low VCC Arrays
  - Blocks Controlled Via Sleep Transistors

- **Transistor**
  - Low Leakage Transistors
  - Sleep Transistors

**ADVANTAGE**
- Mobile-Level Power Management
- Energy Efficient Performance

*Graphics not representative of actual die photo or relative size*
Intel® Advanced Smart Cache
Dynamic L2 Cache Usage

- Higher Cache Hit Rate
- Reduced BUS Traffic
- Lower Latency to Data

*Graphics not representative of actual die photo or relative size
Intel® Smart Memory Access
Hardware-based Memory Disambiguation

Core™ Microarchitecture

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"
- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

DECODE/SCHEDULE

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

EXECUTE

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

OUT OF ORDER

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

INST 2 MUSST

Wait For

Inst. 1 "STORE [X]"

OUT

IN ORDER

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

DECODE/SCHEDULE

- INST 2 "LOAD [Y]"
- INST 1 "STORE [X]"

STALL

Inst. 2 Must Wait For Inst. 1 "Store" To Complete

HARDWARE Mem. Dis. Predictor

Inst. 2 “Load” Can Occur Before Inst. 1 “Store”

ADVANTAGE

- Higher Utilization of Pipeline
- Masks latency to data access
- Higher Performance

Perf

Energy

Higher Performance

• Higher Utilization of Pipeline
• Masks latency to data access
• Higher Performance
**Intel® Advanced Digital Media Boost**

**Single Cycle SSE**

**In Each Core**
- Fusion Support
- Single Cycle SSE
- DECODE
- EXECUTE

**SSE Operation**
(SSE/SSE2/SSE3)
- SOURCE
- SSE/2/3 OP
- DEST
- X4 X3 X2 X1
- Y4 Y3 Y2 Y1

**Core™ µarch**
- CLOCK CYCLE 1
  - X4opY4 X3opY3 X2opY2 X1opY1

**Previous**
- CLOCK CYCLE 1
  - X2opY2 X1opY1
- CLOCK CYCLE 2
  - X4opY4 X3opY3

**ADVANTAGE**
- Increased Performance
- 128 bit Single Cycle in each core
- Improved Energy Efficiency

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Next Generation Platforms

Energy  Efficient  Performance

Intel® Core™ Microarchitecture

- Intel® Wide Dynamic Execution
- Intel® Intelligent Power Capability
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Advanced Digital Media Boost

Server Optimized

- 80W Target TDP
- 40W LV Target TDP
- 2 Execution Cores
- 4MB L2 Cache
- Server Platform *Ts
- DP Configurations

Bensley

Desktop Optimized

- 65W Mainstream TDP
- 2 Execution Cores
- 2MB & 4MB L2 Cache
- Desktop Platform *Ts

Averill Bridge Creek

Mobile Optimized

- Mobile TDP
- 2 Execution Cores
- 2MB & 4MB L2 Cache
- Mobile Power Optimizations
- Mobile Platform *Ts

Napa refresh

Intel Developer FORUM
Comprehensive Platform Architecture

Memory Controller Considerations

Rapid Adoption Of Technology Transitions

Market Segments Require Different Technologies

MOBILE DESKTOP SERVER

Business + Technical

- RELIABILITY
- PERFORMANCE
- POWER MANAGEMENT
- COHERENCY LATENCY REDUCTION
- MEMORY ACCESS REDUCTION
- PROCESS SCALING RATES
- PLATFORM-LEVEL ENHANCEMENTS
Comprehensive Platform Architecture

MEMORY CONTROLLER CONSIDERATIONS

Memory Controller in Chipset

- Extended RAS for Servers
- Memory Closer to Integrated GFX, Smart Cache and Smart Memory Access
- Centralized Coherency Control
- CPU Power States w/ Memory Alive
- MC vs Processor Device Scaling
- IO Acceleration Technology

Technical

- RELIABILITY
- PERFORMANCE
- MEMORY ACCESS REDUCTION
- COHERENCY LATENCY REDUCTION
- POWER MANAGEMENT
- PROCESS SCALING RATES
- PLATFORM-LEVEL ENHANCEMENTS
DP Server Architecture

- FSB Scaling
  - 800MHz
  - 1067MHz
  - 1333MHz
- Large Shared Caches
- Central Coherency Resolution
- Local and Remote Memory Latencies Consistent
- Platform Performance: It’s all about Bandwidth & Latency
- Point to Point Interconnect
- Easy Capacity Expansion
- Sustained & Balanced Throughput
- Blackford
- Bensley Platform
- 64 GB
- 17 GB/s

Consistently analyzing the requirements, the technologies, and the tradeoffs.

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Developing for the Intel® Core™ Microarchitecture

- Program for Multicore
- Utilize SSE Enhancements
- Exploit Energy Efficient Performance
- Benefit from Power Efficiency
Further Insight Into Intel® Core™ Microarchitecture

- Core™ Microarchitecture White Paper at rear of auditorium
- Intel®'s Core™ Microarchitecture  
  (Session, MATS001)
- Intel® Multi-Core Architecture and Implementations  
  (Session, MATS002)
- Multi-Core and Core™ Microarchitecture  
  (Chalk Talk, MATC005)
- Shop Talk with Intel® Fellows tomorrow morning 8-9
- Technology Showcase
- Check out www.intel.com/multi-core