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# Intel® Core™ Microarchitecture

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Mobility Group

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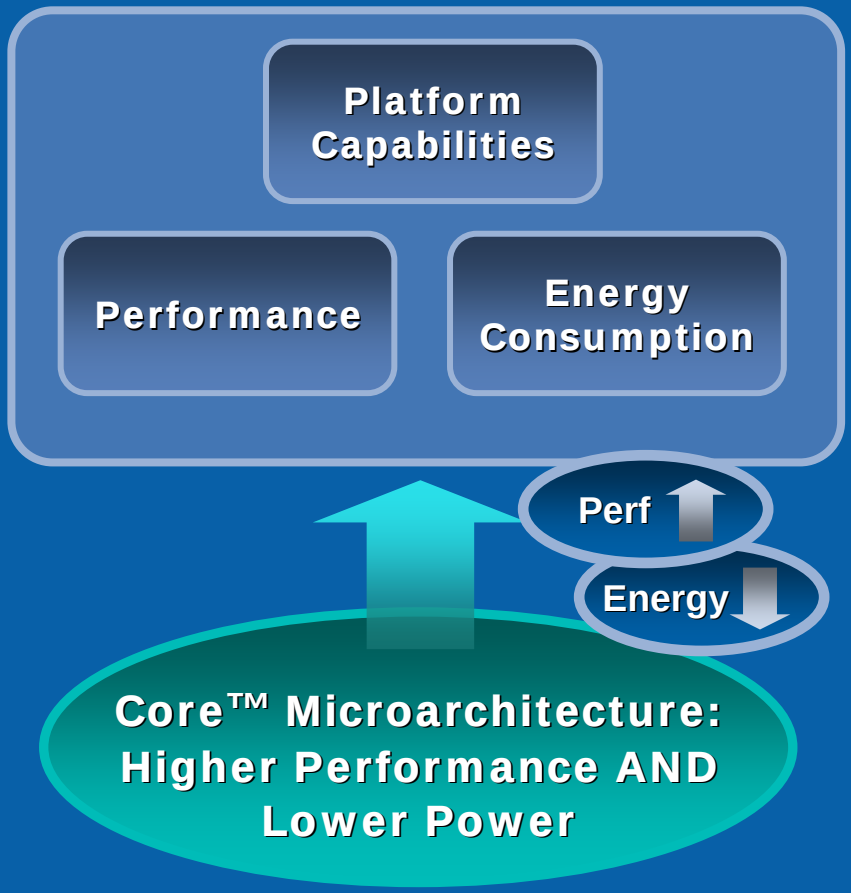
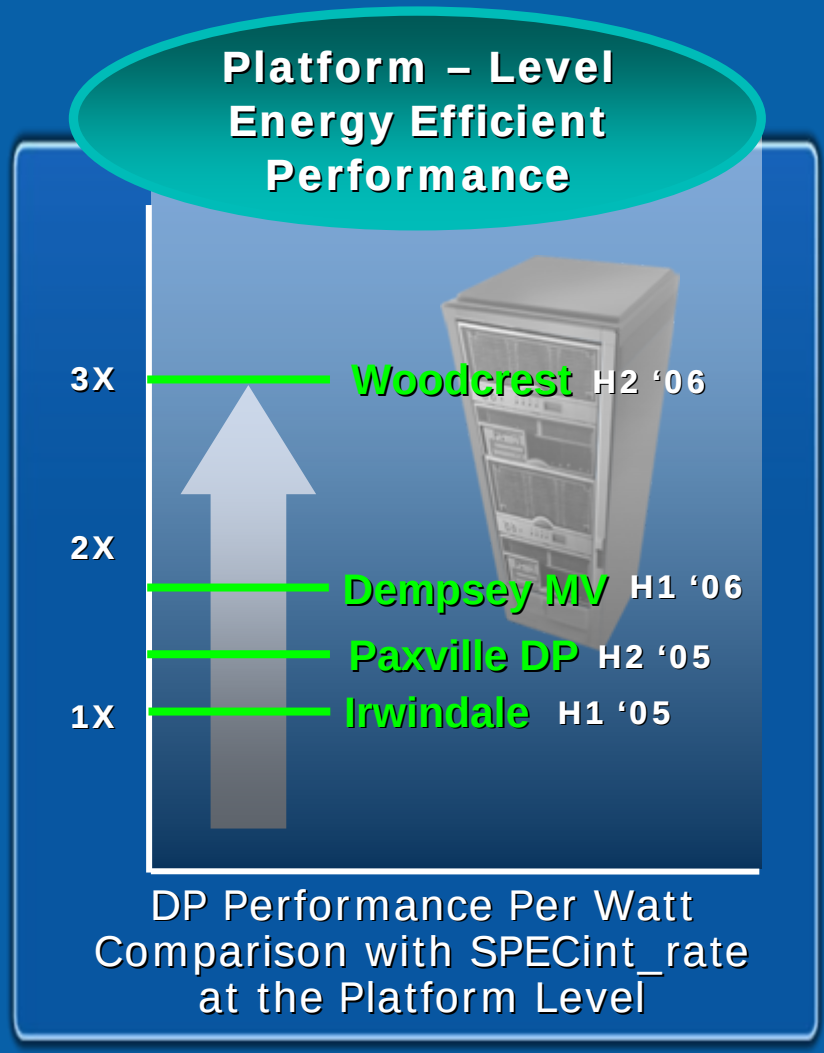
# Continuing From Last Fall's IDF…




**Let's Take A Look Inside**

# Intel® Core™ Microarchitecture
## The Energy Efficient Performance Leader




Source: Intel®

# History

**Microarchitecture and Architecture**

i486™ 1989

Integrated FPU

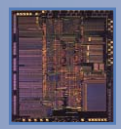
Pipelining

PENTIUM® 1993

Branch Prediction

Superscalar

PENTIUM® Pro 1995

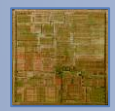


Out Of Order

Register Renaming

Speculative Execution

PENTIUM® III 1999



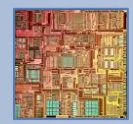
SSE

PENTIUM® 4 2000

NetBurst™

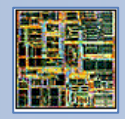
SSE 2

ITANIUM® 2001



EPIC

XEON™ 2002



Hyper Threading

PENTIUM® M 2003

Power Management

Micro Fusion

XEON® 2004

EM64T

PERFORMANCE

POWER EFFICIENT PERFORMANCE

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*Graphics not representative of actual die photo or relative size

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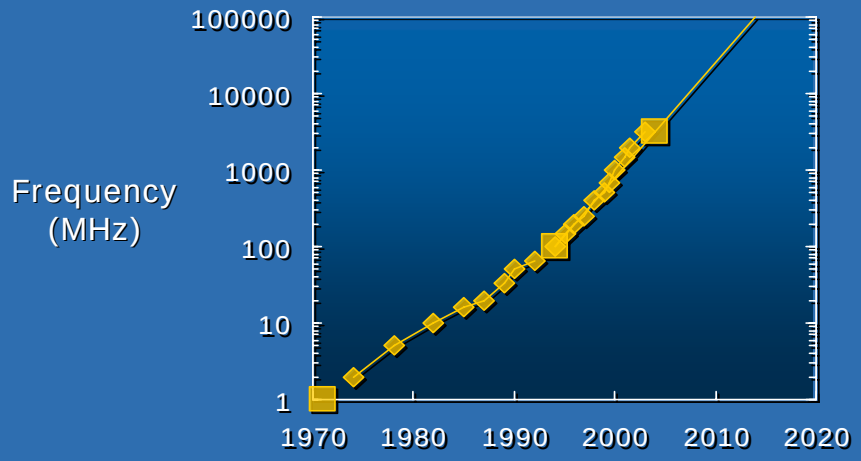
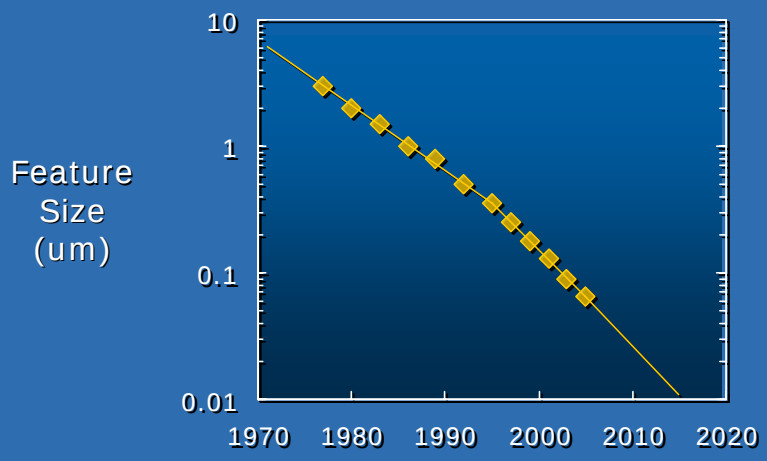
# Historical Driving Forces

## Increased Performance via Increased Frequency

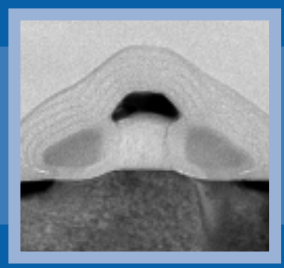



## Shrinking Geometry




**1946**
20 Numbers
in Main Memory

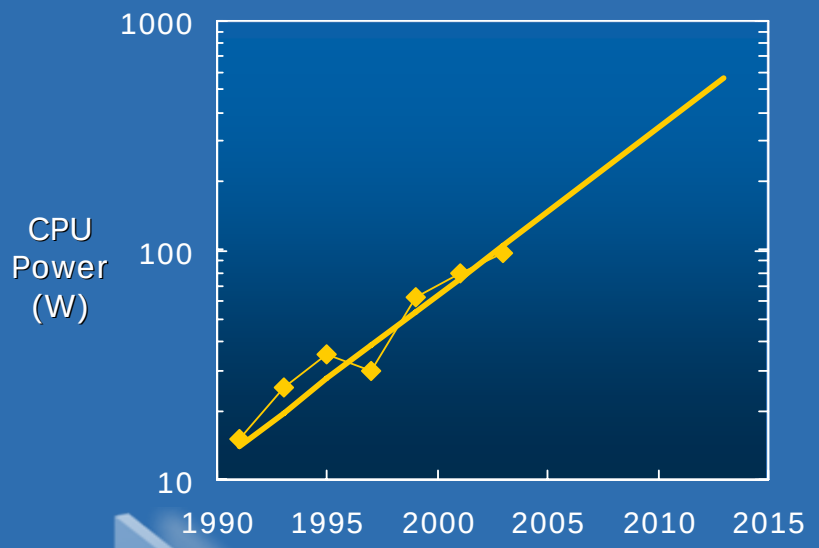
**1971**
I4004 Processor
2300 Transistors



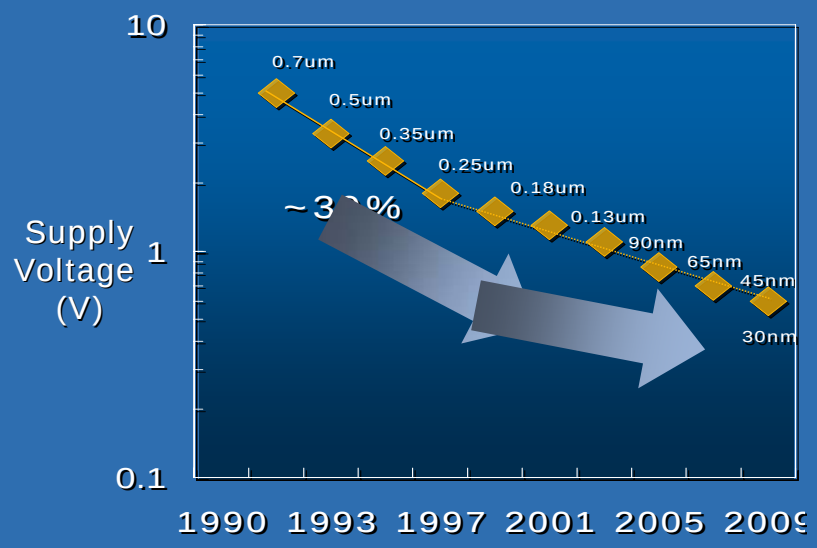
**2005**
65nm
1B+ Transistors

# The Challenges

## Power Limitations



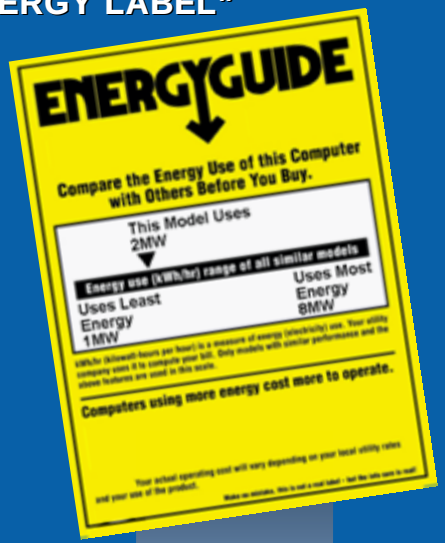

## Diminishing Voltage Scaling

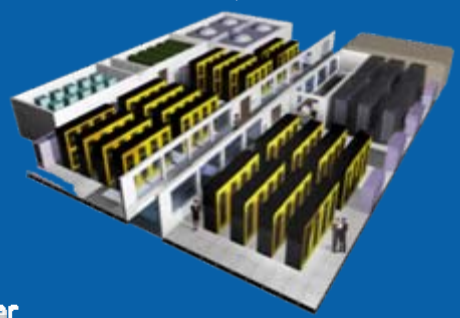


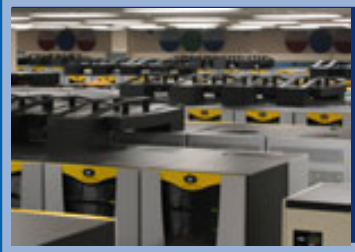

**Power = Capacitance x Voltage² x Frequency**
**also**
**Power ~ Voltage³**

# Energy Efficient Performance – High End

**DATACENTER "ENERGY LABEL"**





***NASA Columbia***
2 MWatt
60 TFlops goal
10,240 cpus – Itanium II
**$50M**

Source: NASA

30,720 Flops/Watt
1,288 Flops/Dollar

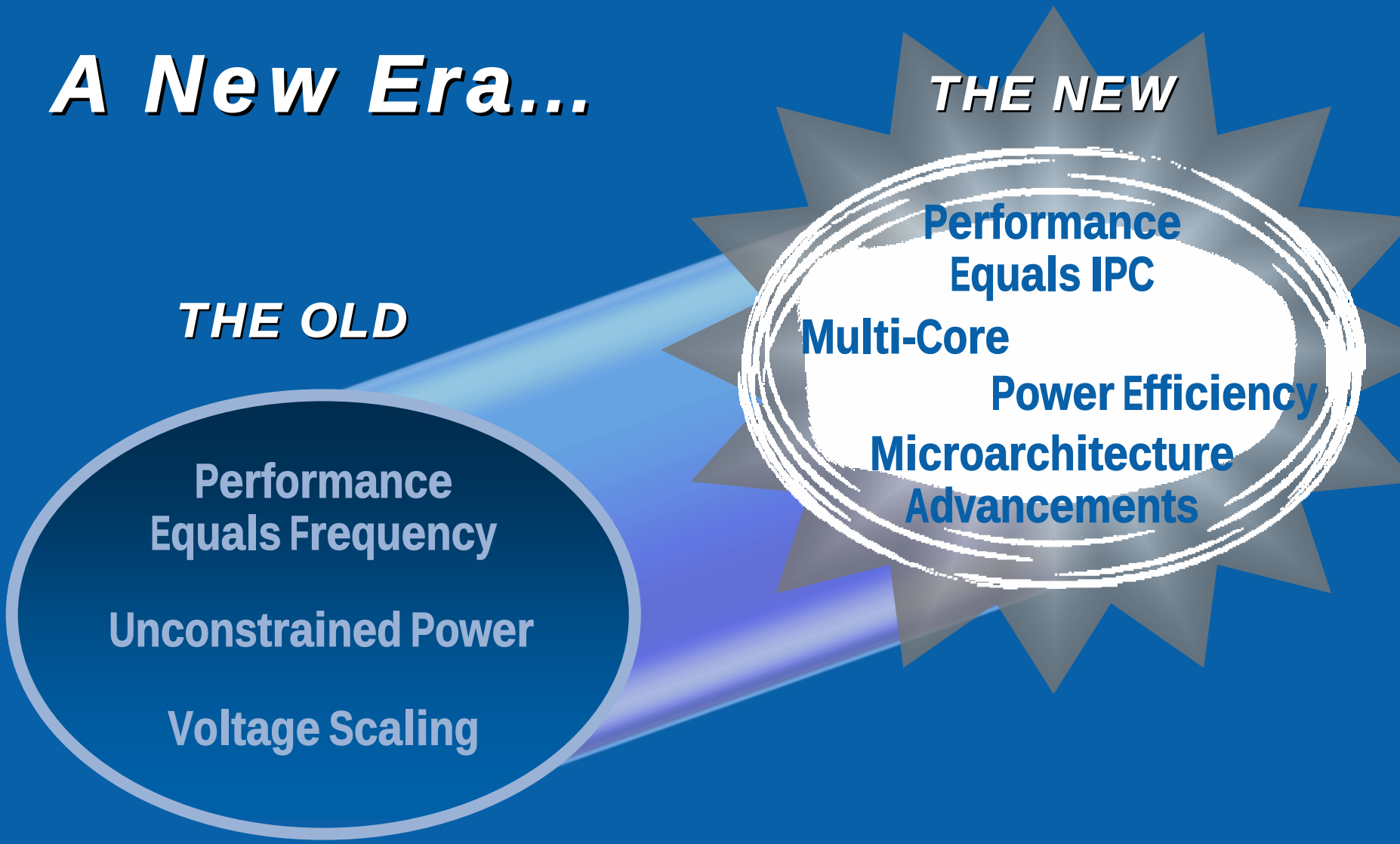
**Computational Efficiency**

17,066 Flops/Watt
467 Flops/Dollar

***ASC Purple***
6 MWatt
100 TFlops goal
12K+ cpus – Power5
**$230M**

Source: LLNL

# A New Era...

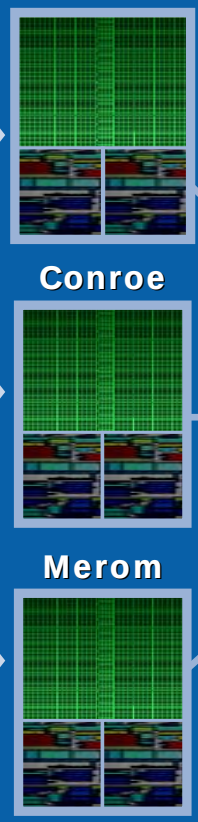

THE OLD
Performance
Equals Frequency
Unconstrained Power
Voltage Scaling
THE NEW
Performance
Equals IPC
Multi-Core
Power Efficiency
Microarchitecture
Advancements

# Intel® Core™ Microarchitecture

Low Power | High Performance | Scalable

- Intel® Wide Dynamic Execution
- Intel® Intelligent Power Capability
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Advanced Digital Media Boost

- Server Optimized
- Desktop Optimized
- Mobile Optimized




65nm

*Graphics not representative of actual die photo or relative size

# Intel® Wide Dynamic Execution

## EACH CORE

*EFFICIENT 14 STAGE PIPELINE*

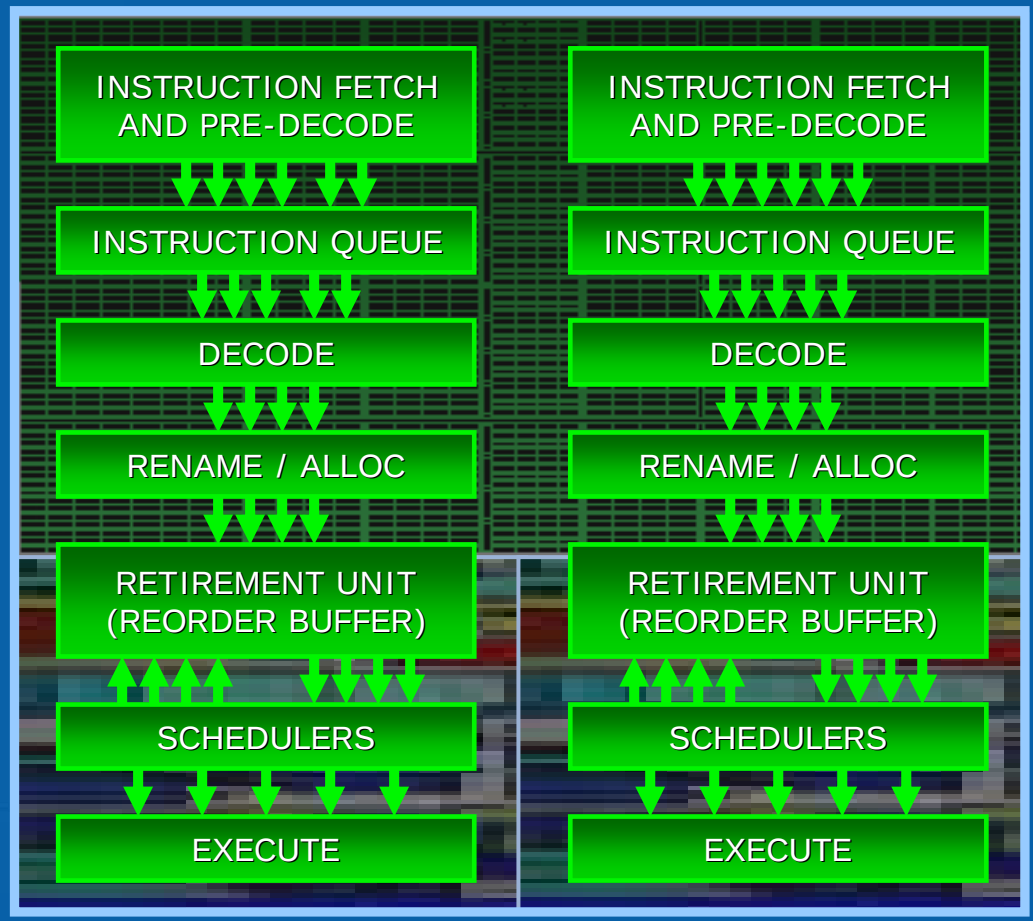
*DEEPER BUFFERS*

*4 WIDE - DECODE TO EXECUTE*

*4 WIDE - MICRO-OP EXECUTE*

*MICRO and MACRO FUSION*

*ENHANCED ALUs*




Perf

Energy

**ADVANTAGE**

- 33% Wider Execution over Previous Gen
- Comprehensive Advancements
- Enabled In Each Core

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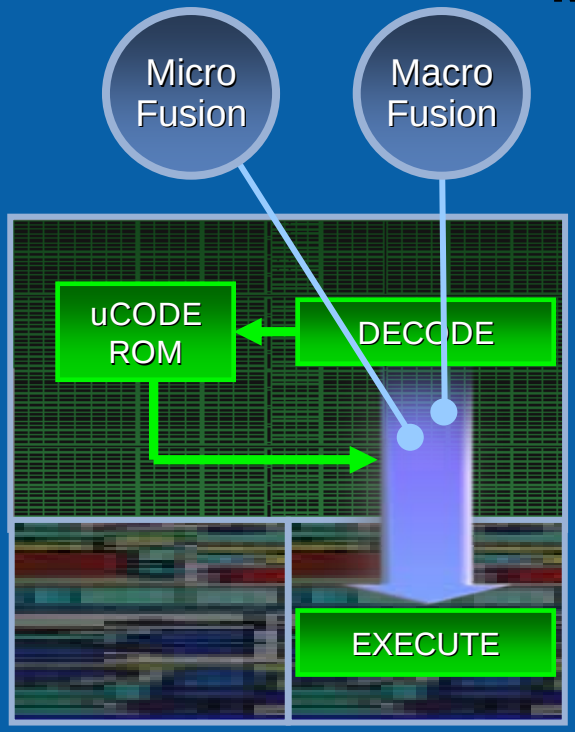
# Intel® Wide Dynamic Execution

## Micro and Macro Fusion




**MACRO FUSION EXAMPLE**

**CMP+JMP IN 1 CLOCK**

| WITH MACRO FUSION | WITHOUT MACRO FUSION |
|---|---|
| INSTRUCTION 3 | INSTRUCTION 3 |
| INSTRUCTION 2 | INSTRUCTION 2 |
| INSTRUCTION 1 | INSTRUCTION 1 |
| DECODE | DECODE |
| COMBINED INST 2 & 3 | INTERNAL INST 3 |
| INTERNAL INST 1 | INTERNAL INST 2 |
| EXECUTE | INTERNAL INST 1 |
| COMPLETED INST 3 | EXECUTE |
| COMPLETED INST 2 | COMPLETED INST 3 |
| COMPLETED INST 1 | COMPLETED INST 2 |
| | COMPLETED INST 1 |

Perf ↑

Energy ↓

**ADVANTAGE**

- Instruction Load Reduced ~ 15%**
- Micro-Ops Reduced ~ 10%**

*Graphics not representative of actual die photo or relative size

** Workload dependant

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# Intel® Intelligent Power Capability


| Process | Coarse Grained | Ultra Fine Grained | Transistor |
|---|---|---|---|
| • 65nm<br>• Strained Silicon<br>• Low-K Dielectric<br>• More Metal Layers | • Aggressive Clock Gating<br>• Enhanced Speed-Step | • Low VCC Arrays<br>• Blocks Controlled Via Sleep Transistors | • Low Leakage Transistors<br>• Sleep Transistors |

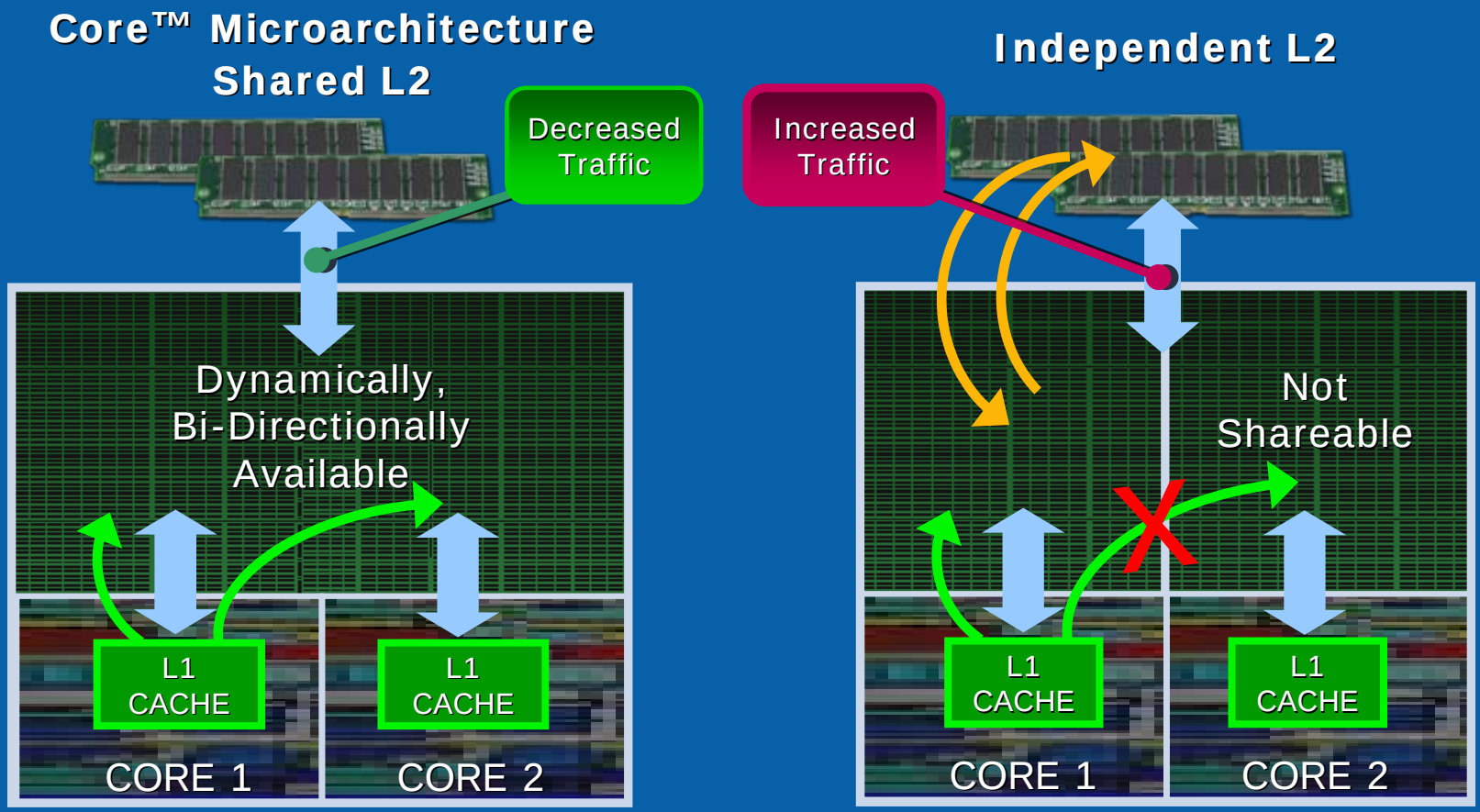
Energy **ADVANTAGE**

- Mobile-Level Power Management
- Energy Efficient Performance

*Graphics not representative of actual die photo or relative size

# Intel® Advanced Smart Cache

## Dynamic L2 Cache Usage




**Perf** ↑

**Energy** ↓

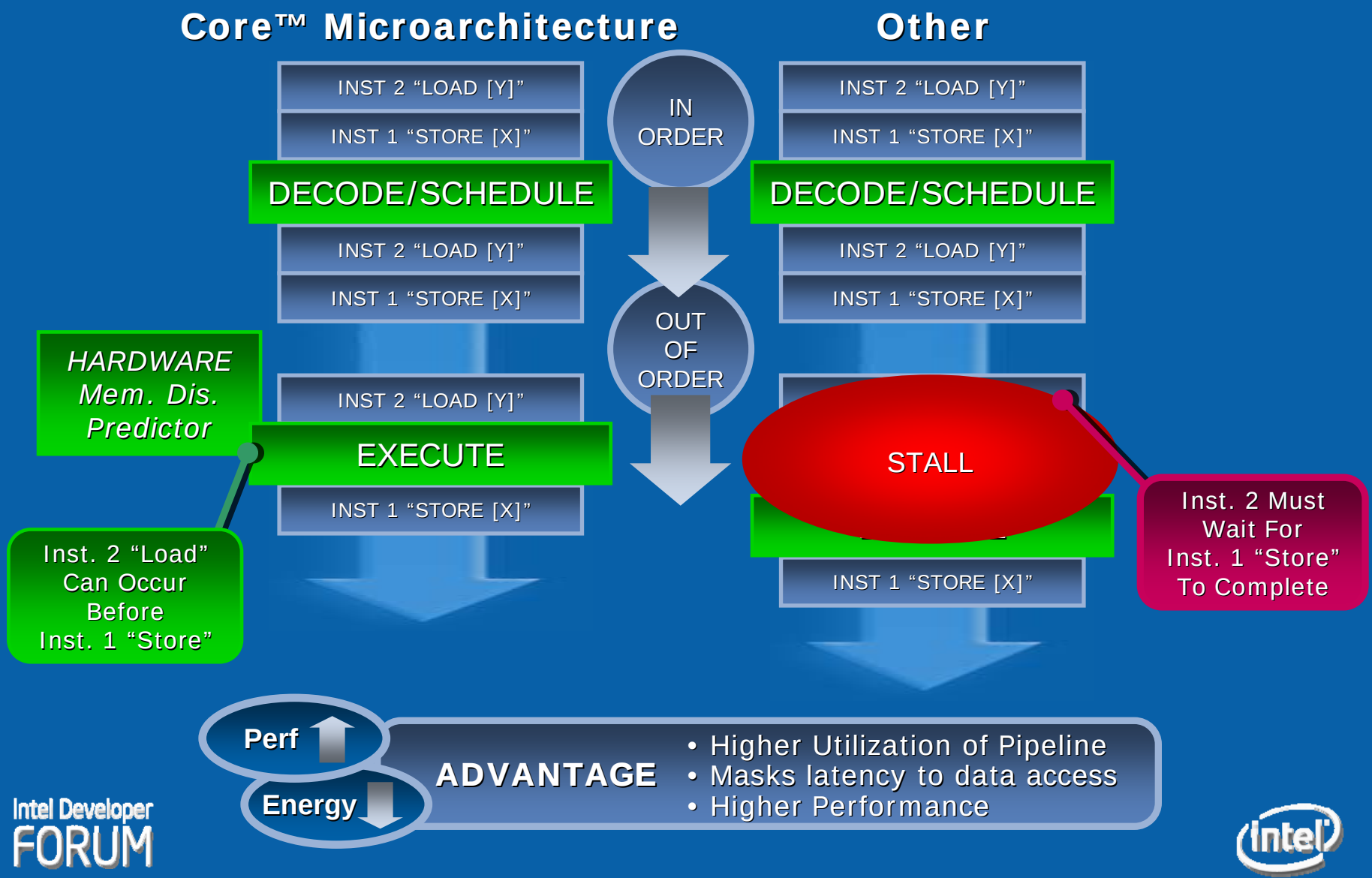
**ADVANTAGE**

- Higher Cache Hit Rate
- Reduced BUS Traffic
- Lower Latency to Data

*Graphics not representative of actual die photo or relative size

# Intel® Smart Memory Access

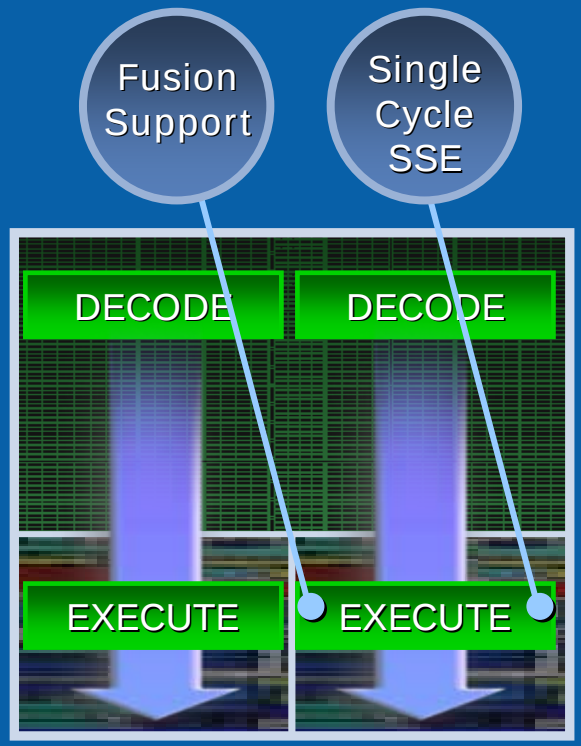
## Hardware-based Memory Disambiguation



# Intel® Advanced Digital Media Boost

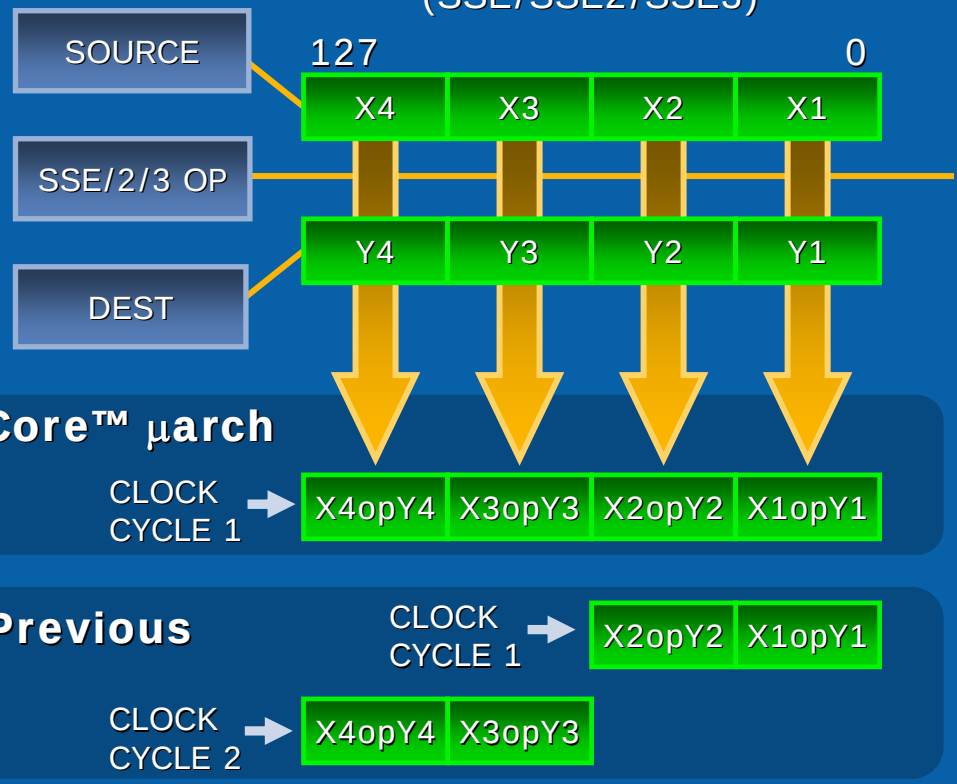
## Single Cycle SSE

### In Each Core




### SSE Operation

(SSE/SSE2/SSE3)





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# Next Generation Platforms

## Energy Efficient Performance

**Intel® Core™ Microarchitecture**

- Intel® Wide Dynamic Execution
- Intel® Intelligent Power Capability
- Intel® Advanced Smart Cache
- Intel® Smart Memory Access
- Intel® Advanced Digital Media Boost

**Server Optimized**

Bensley

- 80W Target TDP
- 40W LV Target TDP
- 2 Execution Cores
- 4MB L2 Cache
- Server Platform *Ts
- DP Configurations

**Desktop Optimized**

Averill Bridge Creek

- 65W Mainstream TDP
- 2 Execution Cores
- 2MB & 4MB L2 Cache
- Desktop Platform *Ts

**Mobile Optimized**

Napa refresh

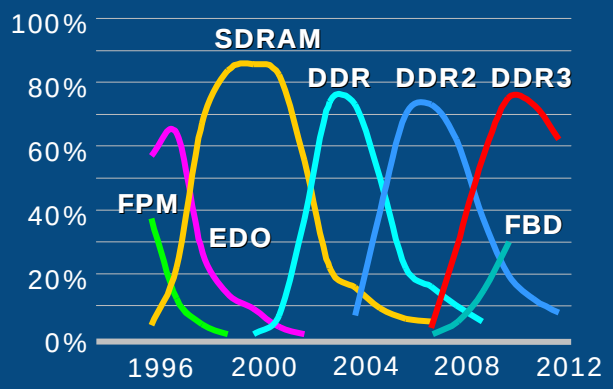
- Mobile TDP
- 2 Execution Cores
- 2MB & 4MB L2 Cache
- Mobile Power Optimizations
- Mobile Platform *Ts

# Comprehensive Platform Architecture

## *Memory Controller Considerations*

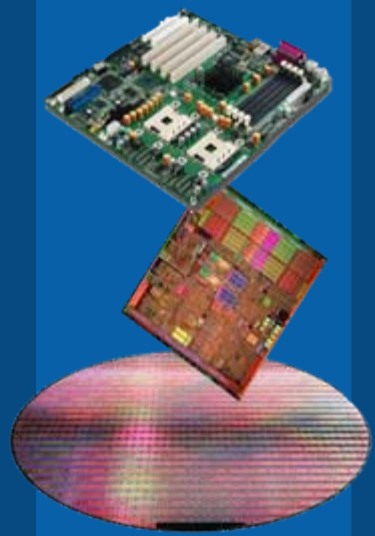
**Business** + **Technical**

Rapid Adoption Of Technology Transitions




Market Segments Require Different Technologies

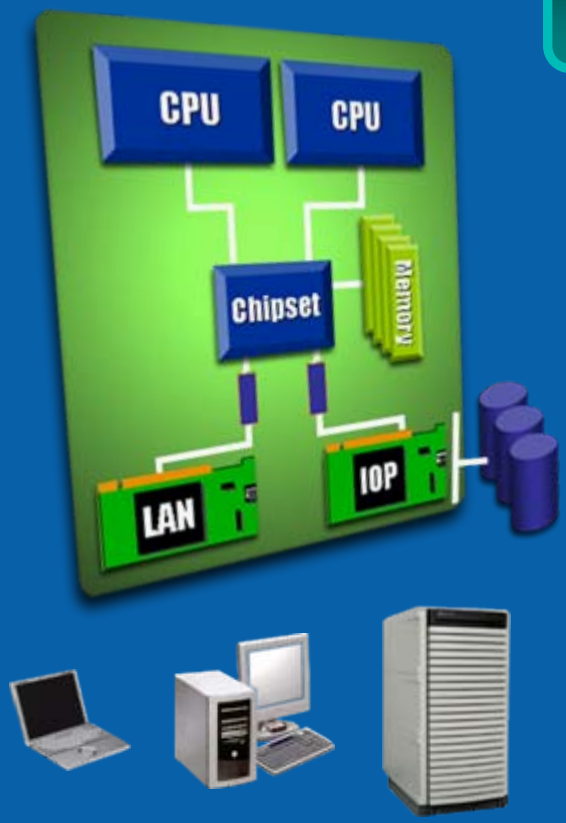
***MOBILE DESKTOP SERVER***



- RELIABILITY
- PERFORMANCE
- POWER MANAGEMENT
- COHERENCY LATENCY REDUCTION
- MEMORY ACCESS REDUCTION
- PROCESS SCALING RATES
- PLATFORM-LEVEL ENHANCEMENTS

# Comprehensive Platform Architecture

## *MEMORY CONTROLLER CONSIDERATIONS*




**Memory Controller in Chipset**

**Technical**

| Memory Controller in Chipset | Technical |
|---|---|
| Extended RAS for Servers | RELIABILITY |
| Memory Closer to Integrated GFX, Smart Cache and Smart Memory Access | PERFORMANCE |
| | MEMORY ACCESS REDUCTION |
| Centralized Coherency Control | COHERENCY LATENCY REDUCTION |
| CPU Power States w/ Memory Alive | POWER MANAGEMENT |
| MC vs Processor Device Scaling | PROCESS SCALING RATES |
| IO Acceleration Technology | PLATFORM-LEVEL ENHANCEMENTS |

# DP Server Architecture

FSB Scaling
800MHz
1067MHz
1333MHz

Large
Shared Caches

Central Coherency
Resolution

Local and Remote
Memory Latencies
Consistent

Bensley Platform

*Platform Performance: It's all about* ***Bandwidth*** *&* ***Latency***

Point to Point
Interconnect

Easy Capacity
Expansion

Sustained &
Balanced
Throughput

64 GB

17 GB/s

Blackford

Perf ↑

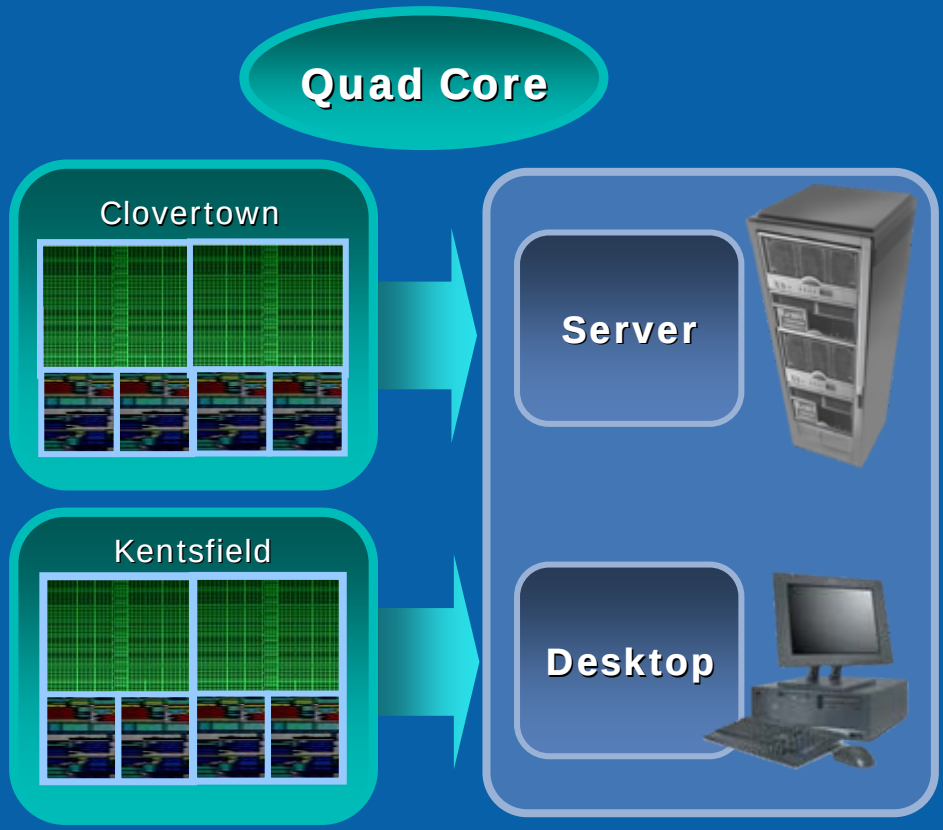
Energy ↓

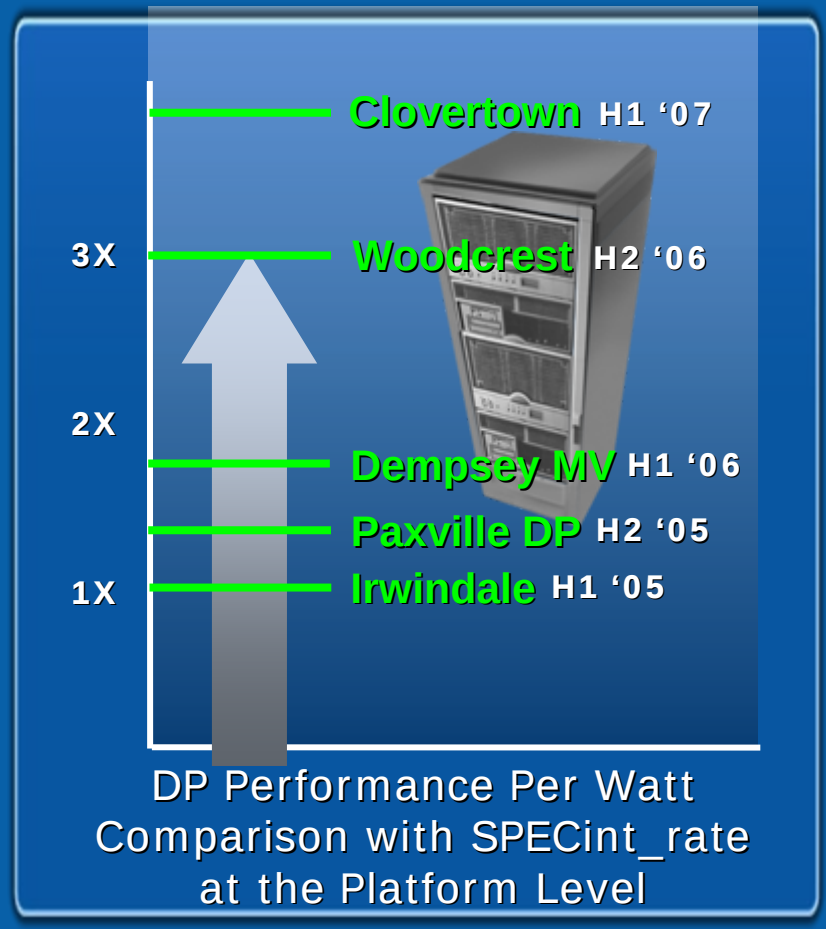
**CONSTANTLY ANALYZING THE REQUIREMENTS, THE TECHNOLOGIES, AND THE TRADEOFFS**

*Graphics not representative of actual die photo or relative size

# Core™ Microarchitecture Advances With Quad Core

**Energy Efficient Performance**




Source: Intel®

*Graphics not representative of actual die photo or relative size

# Developing for the Intel® Core™ Microarchitecture

# Further Insight Into Intel® Core™ Microarchitecture

- Core™ Microarchitecture White Paper at rear of auditorium
- Intel®'s Core™ Microarchitecture

  (Session, MATS001)
- Intel® Multi-Core Architecture and Implementations

  (Session, MATS002)
- Multi-Core and Core™ Microarchitecture

  (Chalk Talk, MATC005)
- Shop Talk with Intel® Fellows tomorrow morning 8-9
- Technology Showcase
- Check out www.intel.com/multi-core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