Backgrounder

GETTING THE LEAD OUT: THE TECHNICAL CHALLENGE

May 22, 2007 -- Intel Corporation today announced that it is going lead-free[1] beginning with its entire family of 45 nanometer (nm) high-k metal gate (Hi-k) processors, including the next-generation Intel® Core™ 2 Duo, Core 2 Quad and Xeon® processor families. Intel will begin 45nm Hi-k production in the second half of this year.

• ***A Phased Approach*** -- Because of customer demand and technology complexity, Intel took a phased approach to remove the lead in its products, starting first with its flash products. Since then, Intel moved up the demand/technology curve and consistently developed lead-free or reduced-lead technologies for the other, more complex market segments.

1999 Intel forms an internal team to focus on lead-free technologies
2002 Intel produced its first lead-free 130nm flash memory products
2004 Availability of initial 95 percent lead-free[2] 90nm second level interconnect flip-chip ball grid array products
2007 Intel announces lead-free 45nm flip-chip processors beginning with its forthcoming 45nm Hi-k family of processors, set to begin production in 2H'07

• ***Removing the Lead*** -- Since early 2005, Intel has shipped more than 1 billion microprocessor, chip chipset and flash components with more than 95 percent[2] of the lead eliminated in the packaging. With its 45nm Hi-k silicon technology, Intel has achieved the final and most challenging milestone to eliminate the small amount of lead still remaining in its CPU products.

• ***Packaging Basics*** – Lead is used today in a variety of micro-electronic "packages" and the "bumps" that attach an Intel chip to the packages. Packages wrap around the chip and ultimately connect it to the motherboard. Different types of packages are used for processors targeted at specific market segments, including mobile, desktop and server. There are three key types of packaging for micro-electronics: pin grid array (PGA), ball grid array (BGA) and land grid array (LGA).

• ***Flip Chip Overview*** -- "Flip chip" is an industry term used to describe the electrical connection of face-down processor die onto the package by means of conductive bumps (the round bumps in the illustration below) on the chip bond pads. Flip chip assembly replaced older wire bonding, which used face-up chips with a wire connection to each pad.

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1 - 45nm product is manufactured on a Lead Free process. Lead-free per EU RoHS directive July, 2006 (2002/95/EC, Annex A). Some EU RoHS exemptions may apply to other components used in the product package.

2 - Percentage based on weight. Some RoHS exemptions may apply to other components used in the product package

"Flip Chip" Ball Grid Array (FC-BGA) example:

- ***Removing the Last 5 Percent of Lead – Why Is It So Hard?*** – The remaining lead was found in the first level interconnect: the solder joint connecting the silicon die to the package substrate. Lead has been used in electronics for decades. The silicon and packaging technology was developed around its electrical and mechanical properties. The new material (tin/silver/copper solder) used to replace the lead had to be similar, plugging in to the manufacturing processes and designs, and ideally offering a performance benefit as well.

- ***The Engineering Challenge*** -- A great deal of engineering work was required to integrate a new tin/silver/copper solder alloy system with the complex interconnect structure of Intel's advanced silicon technologies. This had to be done, too, while still demonstrating the high level of quality and reliability expected of Intel components. New innovative solutions had to be developed to manage the increased stresses caused by the new materials. The new lead-free first level interconnect architecture is a winner on several fronts; it can carry more current and enable higher performance microprocessors, it is more reliable, and it is better for the environment since it is lead-free.

- ***Selecting the Right Materials*** –The team had a wide variety of solders to sort through before finding the right combination. Intel selected the tin/silver copper solder because of its ability to form reliable connections, carry large amounts of current for many years, and its resistance to fatigue, among other attributes. Solders with lower melting points, which would have reduced the stress problems as the parts changed temperatures, did not meet some of the other critical criteria.

- ***Designing a New Lead Free Architecture that Also Improves Performance*** – The new solder alloy uses copper and a new copper column die bump that together, dramatically increase the current carrying capability of the electrical connection. Copper is a better conductor than the previously used lead/tin solder and it can connect to massive metal layers inside the die. An increased challenge exists when using copper, though. Copper is a stiffer material and the new tin/silver/copper solder is stiffer than the traditional leaded solder. The tin/silver solder does not wet the copper surface as well as the lead/tin solder did in the past, presenting another challenge for Intel engineers.

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• ***Managing the Stress*** – The use of a lead-free tin/silver/copper solder alloy results in increased stress on the silicon due to the higher solder melting point. To manage the increased stress and survive the higher process temperatures, Intel reengineered many aspects of the technology including:

- The protector for the silicon, called "passivation" (a material that seals the die surface and protects the underlying microcircuits). Intel engineers did this to meet the product performance and stress-management requirements posed by the latest micro-architecture and new 45nm process, as well as the increased stress from the lead-free solder process.

- Developing a flip chip joint with good integrity and that would form a consistent solder bond required a new flux, the material that provides a tackiness to hold the die in place (precariously placed atop the substrate pre-solder) until the solder melts and the joints are formed. This process provides an acid cleaning action to facilitate a good electrical connection between the die and substrate.

- Preventing bump to bump bridging required precise control of both solder volumes and the reflow process to control the solder joint formation without decomposing the flux.

- Scanning Acoustic Microscopes, using sound waves to penetrate inside the chips where light cannot reach, were used to evaluate the quality and reliability of the devices together with Scanning Electron Microscopes, which can magnify images tens of thousands of times.

- Lastly, engineers had to reformulate the die "underfill," an epoxy that is drawn under the die by means of capillary action, to have the proper adhesion characteristics to the new bump metallurgy and die passivation.

• ***Hours of Engineering Results in Lead-Free Chips*** – Long hours of work were expended and tens of thousands of test vehicles were built by teams of Intel engineers collaborating across Intel sites in Chandler, Ariz., Hillsboro, Ore. and around the world to solve the challenges of removing the remaining lead found in Intel flip chip packages.

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