

## ***NEWS RELEASE***

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### **Oasys Design Systems Closes Series B Funding With Investments From Intel Capital, Xilinx**

*Capital to be Used to Expand R&D, Support*

**SANTA CLARA, CALIF. — April 10, 2012 —** [Oasys Design Systems](#), a provider of chip design software, today announced it has closed Series B Funding with investments from Intel Capital, Intel’s global investment organization, and [Xilinx](#), a leading provider of programmable platforms. Funding will be used as working capital to expand Oasys’ research and development team, as well as for further expansion of its worldwide support structure.

Chip Synthesis is a fundamental shift in how synthesis is applied to the design and implementation of integrated circuits (ICs). Traditional block-level synthesis tools do a poor job of handling chip-level issues. Oasys’ RealTime Designer is the first design tool for physical register transfer level (RTL) synthesis of 100-million gate designs and produces better results in a fraction of the time needed by traditional logic synthesis products. It features a unique RTL placement approach that eliminates unending design closure iterations between synthesis and layout.

“Xilinx has licensed Oasys technology and achieved excellent results across a wide range of designs” says Salil Raje, Vice President of Software Product Development

at Xilinx. “We have a long-standing and productive working relationship with the Oasys team and we are pleased to extend our support through this investment.”

“Oasys’ technology has the potential to positively impact the design flow for VLSI chip implementation,” adds Shishpal Rawat, Director, Business Enabling Programs at Design Technology Solutions Group, Intel. “This is a new way of thinking for next-generation chip design implementation. We are pleased to invest in Oasys.”

“We are excited to have the venture capital arm of the number one semiconductor company and the number one programmable platforms vendor as investors in Oasys,” remarks Paul van Besouw, Oasys’ president and chief executive officer (CEO). “With tapeouts at 45 and 28nm process nodes, Realtime Designer is the proven synthesis solution offering substantial runtime and capacity advantages for some of the world’s most complex designs. Intel Capital and Xilinx have given us strategic support, and their investment will enable us to scale commercially and to continue to advance our technology.”

Previously, Oasys announced that several top U.S. semiconductor companies, such as Texas Instruments, Qualcomm and Xilinx, are already using RealTime Designer™. In 2011, Oasys enhanced its Chip Synthesis™ platform by adding design for test (DFT) capabilities and support for chip-level power design, further extending the fast speed and high capacity of RealTime Designer. These additional features completed the fully integrated Chip Synthesis design flow.

### **About Oasys Design Systems**

[Oasys Design Systems](#) is a privately funded electronic design automation (EDA) software supplier with a revolutionary new platform called Chip Synthesis™, a

fundamental shift in how synthesis is used to design and implement ICs larger than 20-million gates. It has attracted the support of legendary EDA leaders and its RealTime Designer™ product is in use at leading-edge semiconductor and systems companies worldwide. Corporate Headquarters is located at 3250 Olcott Street, Suite 120, Santa Clara, Calif. 95054. Telephone: (408) 855-8531. Facsimile: (408) 855-8537. Email: [info@oasys-ds.com](mailto:info@oasys-ds.com). For more information, visit: [www.oasys-ds.com](http://www.oasys-ds.com).

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