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News Fact Sheet

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INTEL DISCLOSURES AT 2007 INTERNATIONAL ELECTRON DEVICES MEETING

Dec. 7, 2007: Intel Corporation is presenting three technical papers at the International Electron Devices Meeting (IEDM) taking place Dec. 10-12 in Washington, D.C. Below are summaries of each Intel paper at the conference, all of which will be presented on Dec. 11.

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Paper 10.2: "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free¹ Packaging"

Session 10: Integrated Circuits and Manufacturing - Advanced CMOS Logic and SoC Platforms

This paper will describe Intel's breakthrough 45nm processing technology, the world's first with high-k metal gate transistors. The new gate stack is combined with enhanced third-generation strained silicon to produce n-type metal oxide semiconductor (NMOS) and p-type metal oxide semiconductor (PMOS) transistors with the highest drive currents reported to date. Logic gate delay will be reported to improve by more than 20 percent compared to 65nm. The technology has produced multiple functional microprocessors and is already in high-volume manufacturing. Intel recently launched its first 45nm processors based on its high-k metal gate transistor technology.

- The paper will highlight another first for the technology: the use of trench (rectangular) contacts to replace square contacts, providing improved performance and local routing capability for improved layout density.
- In addition, the paper will discuss key design rules to achieve density scaling. The technology features the smallest transistor pitch reported at the 45nm generation, providing better transistor packing density as well as a small static random access memory (SRAM) cell size of 0.346µm². High transistor performance at a small transistor pitch shows that no fundamental conflict exists between performance and density as some others have suggested.
- The process features nine copper interconnect layers with extensive use of low-k interlayer dielectrics for improved power and performance integrated with lead-free¹ packaging
- For the first time, the process integrates a very thick copper power redistribution interconnect layer using a polymer inter layer dielectric (ILD).

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Paper 18.2: “Reducing Variation in Advanced Logic Technologies Approaches to Process and Design Manufacturability of Nanoscale CMOS”

Session 18: CMOS Devices - Device/Design Interaction

Process variation is not a barrier to Moore’s Law: Although device dimensions continue to shrink each generation in accordance with Moore’s Law, Intel is able to co-optimize layout regularity, design innovation and other design-for-manufacturing (DFM) techniques with process improvements and disruptive inventions to maintain (or improve) process variation across generations.

- This paper will highlight variation data for Intel’s 45nm high-k metal gate process, illustrating that Intel has been able to maintain or improve many aspects of process variation in 45nm relative to past generations.
- In addition, this paper discusses a variety of detailed process variation mechanisms (including random dopant fluctuation, poly patterning and interconnect variation) and presents scaling data from 130nm to 45nm illustrating that both random and systematic variation have largely remained constant across these process generations.
- This paper will also describe how random variation in transistor threshold voltage due to random dopant fluctuation is the one exception that has shown an increasing trend with generational scaling. Even this mode, however, shows improvement in Intel’s 45nm process technology due to the implementation of the company’s high-k metal gate transistors.



Paper 23.5: “Heterogeneous Integration of Enhancement Mode In_{0.7}Ga_{0.3}As Quantum Well Transistor on Silicon Substrate using Thin (≤ 2 nm) Composite Buffer Architecture for High-Speed and Low-Voltage (0.5V) Logic Applications”

Session 23: Quantum, Power, and Compound Semiconductor Devices - III-V FETs for Microwave, Millimeter Wave and Digital Applications

Intel continues its leadership in silicon advancement with research and development of innovations for future device scaling. This paper will provide a technical view into the company’s latest achievement. It will describe the successful fabrication of high performance quantum well field effect transistors (QWFETs) using a new material called Indium Gallium Arsenide (InGaAs) that is made up of elements found in the III and V columns of the periodic table. The QWFETs were developed using a thin buffer layer on silicon substrate with an 80nm gate. The paper will describe how this will change some of the technologies being explored for future transistor advancement in the middle of the next-decade timeframe.

- III-V QWFETs are promising device candidates for future high-speed, low-power digital logic applications because they offer very high performance at significantly reduced operating voltage.
- Successful fabrication of these devices on silicon wafers would allow seamless integration with more conventional silicon devices and circumvents the development of inefficient large-diameter III-V substrates.
- These devices operate at high performance at only 0.5V and deliver greater than 10 times the power reduction compared with the equivalent silicon device.



Intel engineers will also participate in two short courses offered at IEDM 2007:

Short Course: Emerging Nanotechnology and Nanoelectronics

Sunday, Dec. 9

Introduction provided by course organizer Robert Chau, Intel Senior Fellow, Technology and Manufacturing Group director, Transistor Research and Nanotechnology, Intel Corporation.

Intel Fellow Valluri “Bob” Rao will co-instruct the session titled “Emerging Nanotechnology for Nanoelectronic Applications.”

Short Course: Performance Boosters for Advanced CMOS Devices

Sunday, Dec. 9

Intel engineer Paul Packan will instruct a session titled “Device / Circuit Interactions.”

Additional information and a complete agenda can be found at

www.his.com/~iedm/program/07advprg.pdf.

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¹ 45nm product is manufactured on a lead-free process. Lead-free per EU RoHS directive July 2006. Some E.U. RoHS exemptions may apply to other components used in the product package.