Intel Labs ISSCC 2014 Highlights
Energy Efficiency Research

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Wen-Hann Wang, VP and Managing Director, Intel Labs

• Led hardware and software research and product development groups in 22-years at Intel.

• Prior to becoming Director of the Labs, I led the Circuits and Systems Research Lab.

• Intel Labs continues to deliver innovative technologies that significantly impact Intel’s products including Intel® Quark processor and Intel® Edison processor.
INTEL LABS
Deliver breakthrough innovations to fuel Intel’s growth and technology leadership

COLLABORATE FOR RESULTS
- UNIVERSITIES
- GOVERNMENTS
- INDUSTRY

KEY RESEARCH FOCUS AREAS
- USER EXPERIENCE
- ARCHITECTURE AND DESIGN
- SYSTEMS AND SOFTWARE
- SECURITY AND PRIVACY
- INTEGRATED COMPUTING

ADDITIONAL ORGANIZATIONS
- INTEL LABS EUROPE Sustainable Intelligent Systems
- INTEL LABS CHINA China Tech Ecosystem
- STRATEGY, PLANNING and COLLABORATION
Energy Efficiency Research

• Intel Research helps contribute fundamental new technologies to improve platform efficiency and overall battery life

• 20x idle power reduction in Haswell\(^1\)

• More than 10 hours of battery life and three weeks of standby in Bay Trail SoC\(^2\)

• Research introduced at ISSCC serves as the foundation

• Next generation of efficiency gains will come from innovative circuits, architecture, and I/O that operate at lower voltage and adaptively scale performance

\(^1\) Intel Developer forum 2011 Keynote presentation

\(^2\) Intel BayTrail SoC factsheet
Low Power Circuit Innovations
- NTV operation and Vmin reduction
- Guardband reduction through resilient and adaptive circuit solutions
- Reducing leakage energy

Platform Power Management
- Shift from OS to hardware management of platform
- Collect and align system and device activity, low power device states
- Highly efficient new system states

Efficient I/O and Memory
- eDRAM and memory interface circuits
- Energy efficient interconnects
- Circuit and system for low cost I/O

Technologies for the efficient future
1. **Efficient Computing Research:** Boost GFLOPS/Watt of 3D graphics execution core via adaptive circuits & power management techniques

2. **Security Circuits Research:** Physically Unclonable Function (PUF) SoC building block for advanced hardware security features

3. **Many-Core Interconnect Circuits Research:** Efficient network-on-chip circuits scalable to 100’s of compute nodes

4. **Platform Interconnect Circuits Research:** Efficient serial link and memory interface for scalable platform performance
Energy-Efficient Graphics Execution Core
(5.7) A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep

- Adaptive clocking mitigates impact of fast voltage droops
- Selective boosting allows low-voltage operation of embedded register file and ROM arrays
- State-retention capability shows 10X leakage savings\(^1\)
- Near-Threshold Voltage (NTV) operation boosts GFLOPS/Watt by 2.7X compared to nominal voltage\(^1\)
- 1.4X higher peak GFLOPS/Watt\(^1\)

Invited by ISSCC for demo

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\(^1\) All measurements from research testchip published in paper 5.7 at International Solid-State Circuits Conference 2014.
Physically Unclonable Function (PUF)

(16.2) A 0.19pJ/bit PVT Variation-tolerant Hybrid Physically Unclonable Function Circuit for 100% Stable Secure Key Generation in 22nm CMOS

- Demonstrates high performance PUF circuits for more stable and more secure unique key generation
- Resistant to tampering/probing attacks -- repeatable, externally-invisible key without fuses
- Leverages process variations to generate key at power-up
- 27X higher throughput vs. best previous reported
- Industry-leading 0.19pJ/bit energy efficiency
- High-density 4.6mm² bit-cell in 22nm tri-gate CMOS

1 All measurements from research testchip published in paper 16.2 at International Solid-State Circuits Conference 2014.
256-Node Efficient Network-on-Chip (16.1) A 340mV-to-0.9V 20.2Tb/s Source-Synchronous Hybrid Packet/Circuit-Switched 16×16 Network-on-Chip in 22nm Tri-Gate CMOS

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- Targeted for on-chip interconnect fabric of future many-core processors
- Demonstrates industry-leading 20.2Tb/s inter-core communication bandwidth\(^1\)
- 18.3Tbps/Watt energy efficiency at 430mV NTV\(^1\)
- Low voltage operation at 340mV – 9X lower power than nominal voltage\(^1\)
- Source-synchronous operation for PVT variation tolerance and scalable, modular design

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\(^1\) All measurements from research testchip published in paper 16.1 at International Solid-State Circuits Conference 2014.
Scalable & Wide-Range Platform IO

(26.2) A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS

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- Lowest power link in its class (25-32Gb/s)$^1$
- Demonstrates scalable efficiency down to 1pJ/b for lightly loaded conditions (4Gb/s)$^1$
- Bidirectional capability to maximize performance for asymmetric applications such as displays and storage
- Cooperative clock recovery enables low power
- Circuit and system optimized for low cost applications

$^1$All measurements from research testchip published in paper 26.2 at International Solid-State Circuits Conference 2014.
Scalable & Configurable Memory Interface

(26.4) A 25.6Gb/s Differential and DDR4/GDDR5 Dual-Mode Transmitter with Digital Clock Calibration in 22nm CMOS

- Enables high speed memory link with backward compatibility to legacy standards
- Dual-mode differential/single-ended transceiver
- Up to 25.6Gb/s differential data rate over -24dB loss channel
- All-active DDR driver and configurable circuits minimize area overhead

1 All measurements from research testchip published in paper 26.4 at International Solid-State Circuits Conference 2014.
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Q&A
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Demand could be different from Intel's expectations due to factors including changes in business and economic conditions; customer acceptance of Intel's and competitors' products; supply constraints and other disruptions affecting customers; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers.

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