SAN FRANCISCO, Feb. 9, 2013 – Intel is delivering myriad presentations, panel discussions and demonstrations at this year’s IEEE International Solid-State Circuits Conference (ISSCC). Topics include fundamental research advances in energy-efficient graphics execution core, efficient network-on-chips, scalable I/O, high-performance and scalable memory interfaces, and last but not the least, building block innovations to enable advanced security features in future SoCs. Below are highlights covering Intel’s scheduled presence at the event.

**Sunday, Feb. 9**

- **Forum F2: “Scaling the Memory Wall with 3D-IC: A System Perspective,” 9:20 AM**
  Three-dimensional (3D) stacking integration offers many product benefits for SoC and memory: performance enhancements, product miniaturization and cost reduction. Image sensors featuring 3D stacking of a specialized image sensor layer on top of a deep submicron digital CMOS have just come to the market. The objective of this forum is to present applications and details of process integration, device techniques, circuits and systems featuring 3D stacking integration. Shih-Lien Lu, an Intel principal engineer, will speak in this forum and provide a system perspective on scaling the memory wall with 3D-IC.

- **Evening Session:**
  - **ES2: “Today’s Big (data) Is Small,” 8:00 PM**
  With the rise of cloud computing and Big Data, data centers pose an important counterpoint to rapid growth in the mobile market. Building cost-effective, efficient computing infrastructures is a challenge that starts with processors, I/O, memory and many other system technologies, but also encompasses system and customer-centric issues such as cooling, power delivery, and total cost of ownership. In this session, Steve Pawlowski, Intel Senior Fellow, will provide an outlook on the future of data centers.
Monday, Feb. 10
Session 5: Processors

- Session 5.4 – “Ivytown: A 22nm 15-Core Enterprise Xeon® Processor Family,” 2:30 PM
  In this paper Intel will discuss new details of the next generation Intel Xeon processor E7v2 product family codenamed “Ivytown”. The new product family is aimed at real-time advanced data analytics workloads and is based on 22nm process technology. It offers significant improvements in memory support, core count and performance compared to previous generations. The paper focuses on architecture and technology innovations that led to reduction in power consumption.

- Session 5.7 – “A Graphics Execution Core in 22nm CMOS Featuring Adaptive Clocking, Selective Boosting and State-Retentive Sleep,” 4:00 PM
  The demand for high-performance graphics capability even in extremely power-constrained platforms such as smartphones and tablets requires circuit techniques that scale from efficient operation at low voltage to high performance when needed. In this Intel Labs paper, a 22nm graphics execution core research test-chip is discussed that demonstrates Near Threshold Voltage operation that boosts GFLOPS/Watt by 2.7X. Also, the chip’s built-in state retention capability shows 10X leakage savings. The overall peak energy efficiency improves by 40 percent, enabled by the advanced circuit and design techniques. This research was, in part, funded by the U.S. Government. Also there is a live demonstration of the test-chip in Golden Gate Hall on Monday, Feb 10, from 4:00PM to 7PM.

- Session 5.7 – “Haswell: A Family of IA 22nm Processors,” 4:45 PM
  Consumer demands for better user experience continue to drive market requirements for thinner, lighter and more responsive devices. Traditional personal computing platforms are evolving to deliver against these demands. This paper highlights a broad range of innovations delivered by the 4th Generation Intel® Core™ Processor family (codename ‘Haswell’) to meet the challenge across an increasingly diverse set of PC form-factor constraints, from fan-less Ultrabooks™ and 2-in-1 devices to traditional and All-in-One desktop systems. Technical solutions are discussed, and topics of interest include: power efficiency and power management; cache hierarchy and memory management; graphics and media; as well as processor core enhancements and system-level considerations.

Tuesday, Feb. 11
Session 13: Advanced Embedded Memory

- Session 13.1 – “A 1Gb 2GHz Embedded DRAM in 22nm Tri-Gate CMOS Technology,” 1:30 PM
  Conventional VLSI systems often rely on on-die SRAMs to address the performance gap between CPU and main DRAM memory. However, with the rapid growth in capacity needs for high-performance memory, SRAM is not always sufficient to meet the demands of bandwidth intense applications. Embedded – i.e. on-die -- DRAM (eDRAM) has been explored as an alternative to satisfy the high-performance and density needs in memory. In this paper, a high-performance eDRAM based on a 22nm tri-gate CMOS technology is introduced. This eDRAM technology enables the integration of an eDRAM cell into the logic technology platform. By leveraging the high-performance and low-voltage tri-gate transistor at 22nm generation, the
eDRAM achieves a wide range in operating voltage, from 1.05V (2GHz) down to 0.7V (1GHz), and the 128Mb Array Macro achieves 17.5Mbit/mm2 array density.

Session 16: SoC Building Blocks

- Session 16.1 – “A 340mV-to-0.9V 20.2Tb/s Source-Synchronous Hybrid Packet/Circuit-Switched 16x16 Network-on-Chip in 22nm Tri-Gate CMOS,” 3:15 PM
  Energy-efficient networks-on-chip (NoCs) are key enablers for exascale computation as they make it possible to shift the power budget from communication toward computation. As core counts scale into the 100s, on-chip interconnect fabrics must support increasing heterogeneity and voltage/clock domains. In this paper, Intel Labs presents a source-synchronous 256-node NoC on 22nm Tri-Gate CMOS with industry-leading energy efficiency that mitigates these penalties. The NoC utilizes hybrid packet/circuit switching to parallelize operations for 20.2 Tb/s network utilization at 0.9V. The NoC is also the first reported to operate at near-threshold and ultra-low-voltages, this reducing power by 9x to 363µW at 340mV. This research was, in part, funded by the U.S. Government. Also there is a live demonstration of the Network-on-Chip testchip in Golden Gate Hall on Monday, Feb 10, from 4:00PM to 7PM.

- Session 16.2 – “A 0.19pJ/b PVT-Variation-Tolerant Hybrid Physically Unclonable Function Circuit for 100% Stable Secure Key Generation in 22nm CMOS,” 3:45 PM
  Physically Unclonable Function (PUF) circuits are low-cost cryptographic primitives used for generation of unique, stable and secure keys for device authentication and data security in high performance microprocessors. The volatile nature of PUFs provides a high level of security and tamper resistance against invasive probing attacks compared to conventional fuse-based key storage technologies. In this paper, Intel Labs presents high-performance PUF circuits for 100 percent stable and unique secure key generation that leverages process variations to generate key at system power up. This PUF circuit demonstrates industry-leading 0.19pJ/bit energy efficient and provides 27X higher throughput compared to the state of the art.

Wednesday, Feb. 12
Session 26: Energy Efficient Dense Interconnect

- Session 26.2 – “A 205mW 32Gb/s 3-Tap FFE/6-Tap DFE Bidirectional Serial Link in 22nm CMOS,” 3:45 PM
  Peripheral I/O data rates for PC and mobile computing platforms continue scaling to meet high-bandwidth applications comprising high-resolution displays and large-capacity external storage. The bandwidth requirements will soon exceed the data rates of current standards such as PCI Express and USB. A low-power, low-cost, high-speed serial link is needed for the next generation peripheral interface that can scale to at least 32Gb/s per channel. Although such throughputs have been previously demonstrated, the circuit power and channel characteristics of those technologies were not suitable for mainstream PC and mobile markets. In response, Intel Labs developed the best in class bidirectional serial link that consumes the least power when compared to the state of the art solutions and demonstrates scalable efficiency down to 1pj/b targeting low cost applications. In this Intel Labs’ paper, a low-profile connector and cable assembly prototype is presented that can address the manufacturing challenges while at the same
time optimizing the serial link architecture and design. Also there is a live demonstration of the Serial Link in Golden Gate Hall on Monday, Feb 10, from 4:00PM to 7PM.

  A wide range of memory configurations exist in today’s high-speed digital systems to meet platform-specific bandwidth, power, capacity, and cost constraints. In the near term, DDR4 and GDDR5 are expected to meet the needs of server, client, graphics and mobile platforms. Differential signaling with high-speed serial I/O enhancements will potentially continue I/O performance scaling for post-DDR4 and future buffered memory solutions. A unified memory interface that can meet the signaling requirements of all these memory standards offers several benefits: reduced cost and design time, greater platform design flexibility, and a smoother transition from DDR4/GDDR5 to a high-speed differential memory interface. In this paper Intel Labs presents the industry’s first unified memory interface, a dual-mode TX that supports single-ended 1.2V-DDR4/1.5V-GDDR5 as well as high-speed differential signaling which is implemented using only thin-gate-oxide devices in 22nm CMOS.

Thursday, Feb. 13
- Forum F3: “Process Technology Variation Characteristics and Trends,” 8:30 AM
  As the industry continues the pursuit of Moore’s Law, one key challenge is the management of process technology variation. Continued improvements in process technology and transistor architecture have enabled the development of advanced technologies with both scaled transistor area and improved device variation to support lower voltage operation. In this presentation, Intel Principal Engineer, Martin Giles will consider the characteristics and trends of device variation sources across technology generations, some circuit implications of different kinds of variation, the variation impact of device reliability degradation, and the challenges and outlook for the future.

- Forum F3: “Design of Adaptive and Resilient Circuits for Power-Delivery Solutions,” 1:00PM
  In this talk, Intel engineer, Ramnarayanan Muthukaruppan, will focus on variation in deep-submicron technologies, exploring sources of variation including aging, systematic and random sources and the impact on the performance of the circuit. The talk will also describe circuit techniques such as tunable replica circuits and error detection sequential to make IP block sub-systems intelligent and to measure the margin to failure. The second half of the talk focuses on the techniques that can be used to modulate the clock frequency or the supply voltage, with focus on supply voltage modulation. In terms of supply voltage modulation the presentation will revolve around various integrated architectures like switched capacitor VRs, buck regulators and linear regulators and power gating solutions.

- Forum F6: “Ultra-Efficient Mobile I/O,” 1:20 PM
  System power consumption will drive the architecture of future computing systems. From cloud-connected smart phones to the first exaFLOP supercomputers, systems that are the best at managing and minimizing power consumption will hold a key competitive advantage. At the same time, wireline communication bandwidth requirements within these systems will continue to grow exponentially, driving per-lane data rates beyond 25Gb/s and aggregate bandwidth past 1Tb/s. The objective of this Forum is to provide an overview of ultra-efficient parallel and serial
interfaces, advanced memory applications, dense and high-speed optical communication, and platform-driven wired I/O for mobile. In this forum, Intel Labs Research Scientist, James Jaussi will explore how to design serial I/O specifically for mobile products, including low-power equalization and clocking and low-latency standby state.

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