Technology Insight:
Intel® Next Generation Microarchitecture
Codename Ivy Bridge

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SPCS005
Agenda

• Introduction to: Intel® Next Generation Microarchitecture Codename Ivy Bridge
• Innovation in the Processor Core
• Innovation in Processor Graphics

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Intel® Next Generation Microarchitecture
Codename Ivy Bridge

Introduction
Innovation in the Processor Core

Varghese George, Sr. Principal Engineer
Ivy Bridge – What is the Same...

- Continue the 2-chip platform partition (CPU + PCH)
- Fully integrated on silicon:
  - IA Cores, Processor Graphics
  - Media, Display engine
  - Memory Controller, PCI Express* controller
  - Modular on-die Ring Interconnect
  - Shared LLC
- Supports similar product offerings
- Backwards compatible socket (with 2nd Generation Intel® Core processor codename Sandy Bridge)
Ivy Bridge – What is New...

**Entire chip moves to 22nm**
- Higher performance/Lower power

**Graphics/Media**
- Higher 3D performance with next generation microarchitecture and support for Microsoft* DirectX*11
- Significant improvements in media features and performance

**IA Core/ISA**
- IPC improvements in Core, LLC, Memory controller
- Enhancements to ISA for SSE, strings performance
Ivy Bridge – What is New...

**Security**
- Digital Random Number Generator
- Supervisory Mode Execution Protection

**Power Management**
- Features for improved battery life
- Scalability features: Configurable TDP, Low Power Mode

**Memory/Display**
- DDR3L support, improved overclocking
- 3 independent displays
Key ISA Visible Changes

- Digital Random Number Generator instruction
- Supervisor Mode Execution Protection (SMEP)
- REP MOVSB/STOSB performance improvements
  - More consistent performance across string lengths
- Fast access of FS & GS base registers
  - Useful for user level thread storage by providing 4 new instructions for ring-3 access of FS & GS base registers
- Float16 format conversion instructions
  - Conversion between a 16-bit (compressed) floating point memory format and 32-bit single precision (256-bit AVX and 128-bit SSE versions)
Ivy Bridge introduces a high quality/high performance DRNG

The DRNG is designed to be Standards compliant
- ANSI X9.82, NIST SP 800-90 and NIST FIPS 140-2/3 Level 2 certifiable entropy source

New instruction: RDRAND - Available at all privilege levels/operating modes
- Instruction will return a random number (16, 32 or 64-bit) to the destination register

RDRAND is enumerated via CPUID.1.ECX[30]
Supervisory Mode Execute Protection (SMEP)

- Ivy Bridge introduces SMEP to help prevent Escalation of Privilege (EoP) security attacks
  - Prevents execution out of untrusted application memory while operating at a more privileged level
  - If CR4.SMEP set to 1 and in supervisor mode (CPL<3), instructions may not be executed from a linear address for which the user mode flag is 1
  - Available in both 32- and 64-bit operating modes
  - SMEP is enumerated via CPUID.7.0.EBX[7]
Power Management Improvements

- **DDR I/O embedded power gating**
  - Power off DDR I/O when in deep C states (idle)

- **Configurable TDP / Low power mode**

- **Design optimizations to reduce S3 power**

- **Lower choices for System Agent operating voltages**
  - Allows power optimize low power SKUs further

- **Power Aware Interrupt Routing (PAIR)**
  - Chooses ‘best core’ to service interrupts based on optimization mode (power vs. performance)

- **Optimized voltage choice for all operating frequency points**
  - Best power efficiency across full range of operation
Configurable TDP/Low Power Mode

- Configurable TDP allows multiple TDP levels within the same part
  - Greater dynamic range of power/performance
  - Dynamically transition based on runtime triggers
- Low power mode defines lowest active operating point for the part
  - Further optimizations for lower power
- Intel offers software driver implementing both features
- Allow OEMs more flexibility to build more scalable systems
Memory and Overclocking Features

• **DDR3L support**
  – Low voltage DDR3 (DDR3L) support in mobile SKUs

• **Power optimizations**
  – DRAM ODT optimization in mobile to reduce active power

• **CPU / Graphics Overclocking**
  – Increased max ratio support (ratio 57 => 63)
  – Dynamic overclocking: Allows ratio change without a reboot

• **DDR Overclocking:**
  – Support for up to 2800 MT/s (up from 2133)
  – Finer grain steps in adjusting frequency – Added 200 MHz
Intel® Next Generation Microarchitecture Codename Ivy Bridge

Innovation in Processor Graphics

Tom Piazza, Intel Fellow
Hong Jiang, Senior Principal Engineer
Ivy Bridge represents a Significant Graphics and Media (”tick+”) evolution for Intel® HD Graphics with key changes focused on:

- Architectural features
- μArchitectural improvements
- Power
Ivy Bridge Graphics and Media Microarchitecture Overview

- **Next generation Intel® Core™ microprocessor on the latest 22-nm process**
- **Improved Game Playability**
  - More 3D performance
  - Microsoft® DirectX®11 Support
- **Significant Media Performance**
  - Higher performing Intel® Quick Sync Video
- **Three Native Display Support**
Ivy Bridge HD Graphics: µArchitecture

µArchitecture Changes

Scalable Architecture partitioned into 5 domains:
1. Global Assets: Includes Geometry Front-end up to Setup
2. Slice Common: Includes Rasterizer, L3$ and Pixel Back-end
3. Slice: Shaders (EUs), IC$, Samplers, Addr$ Gen
4. CODEX and media
5. Displays

Sets the stage for further scale-up opportunities
Ivy Bridge HD Graphics: Architecture

Addrs Significant 3D Enhancements

Microsoft* DirectX* 11

Hardware Tessellation
• Adds two programmable stages (HS and DS) and one fixed function Tessellator

New Compressed Texture Format Support (BC6H/7)
Ivy Bridge HD Graphics: Architecture

More Key Changes

Compute Shader Support

- Data Parallelism
- UAVs, Atomics, Barriers, etc for compute shader ops
- Shared Local Memory aka Thread Group Local Memory for Direct Compute* Shaders
- Scatter gather

Shader Array adds support for Shader Model 5.0 (New DX11 Instructions)
Ivy Bridge HD Graphics: µArchitecture

µArchitecture Changes

Improved Geometry Performance
- Faster GS and H/w Stream-out
- Faster Clip/Setup

Fast Clear of Render Target
Increase in Hi-Z Performance

Sampler throughput
- Improved Anisotropic Quality

Increased compute throughput (peak GFLOPs)
- Increased # of threads/registers to cover latency and support complex shaders
- “Enhanced” coissue

L3$ lowers BW need from Ring Architecture

Media Applications benefit from infrastructure changes in EU/L3$ / etc
Ivy Bridge HD Graphics: µArchitecture

**Significant Media Performance**
- Higher performing Intel® Quick Sync Video

**µArchitecture Changes**
- Enhanced Performance for Multi-Format CODEC
- Increased Media Sampler Throughput and performance for scaling and other filters
- Pixel Back end has Image Color and Contrast Enhancement capabilities
Power Optimizations

• **µArchitecture plus 22nm offers:**
  – Up to ~½ power at same performance
  • ~Double the performance / watt

• **Co-issue:**
  – Extended Co-issue on EU to many more operations
  – More IPC per unit area – therefore less power to leakage

• **L3$:**
  – Less BW need from LL$ = Less Energy spent
Summary

• Intel® Next Generation Microarchitecture, Codename Ivy Bridge, is the 1\textsuperscript{st} product on 22 nm process technology

• Another big leap in Performance/Power efficiency in both IA core and Graphics/Media

• Features for improved Security, better Battery life, new Memory technology (DDR3L), better Overclocking support

• Next generation Graphics microarchitecture is a Significant Graphics and Media ("tick+") evolution for Intel® HD Graphics

It’s Just The Beginning
Additional Sources of Information on This Topic:

More web based info on Tri-Gate:

www.intel.com/technology/architecture-silicon/22nm/

Other Session:

SPCS002 - 22 nm Tri-Gate Transistors for Industry-Leading Low Power Capabilities

Download the video recording next week – check out intel.com/idf for links
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