



T1/E1/J1, N+1 Redundancy With Analog Switches and Intel[®] LXT38x Line Interface Units

Preliminary Application Note

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Revision History

Revision Number: 002 Revision Date: July 03, 2003	
Page Number	Description
5	Changed power consumption for relay in Table 1 from 140 μ W to 140 mW.

Revision Number: 001 Revision Date: June 20, 2003	
Page Number	Description
	Initial release.

1.0 Introduction

Modern communications systems with multi-port T1/E1/J1 line cards employ redundancy protection to achieve the high-availability requirements telecom networks demand. Traditionally, these systems have used relays to implement N+1 redundancy switching. As the number of T1/E1/J1 ports per line card and the number of line cards per system increases, relays become impractical both because of board space and power consumption considerations. Therefore, more and more designers seek a solution using analog switches as a replacement for relays. The advantages of analog switches over relays are numerous.

Intel® LXT38x Line Interface Units (LIUs) directly provide 1+1 redundancy with Intel® Hitless Protection Switching (HPS).

Note: This application note applies to N + 1 redundancy. For 1+1 redundancy see the Application Note "1+1 Protection without Relays using Intel® LXT380/1/4/6/8 Hitless Protection Switching" available on the Intel Web site.

Table 1 summarizes the most important advantages for this application.

Table 1. Analog Switches vs. Relays

	Relay	Analog Switch
Board Space	100 mm ²	15 mm ²
Power Consumption	140 mW	5 μW
Switching Speed	4 ms	30 ns
Reliability	Mechanical Operation	No Moving Parts

2.0 Redundancy Architecture

Figure 1, "Receive Interface" on page 7 through Figure 3, "Transmit Interface, T1 Mode" on page 9 show the recommended redundancy architecture with analog switches. The transmit and receive interfaces are shown in separate figures. Transmit and receive interfaces reside on the same board for each T1/E1 port.

In both cases, there is a protection bus running in the backplane where the input or output signals can routed through the analog switches. The protection bus connects directly to a backup (protection) line card.

3.0 Receive Interface Circuit

Figure 1, "Receive Interface" on page 7 shows the recommended receive configuration. The resistors R_r provide the appropriate receive termination. The recommended value depends on the cable impedance as outlined in Table 2, "Receive Termination Resistor" on page 6 (also see the applicable Intel® LXT38x datasheet).

Table 2. Receive Termination Resistor

Operation Mode	R _r
E1 Twisted Pair Cable – 120 Ω	15.0 Ω
E1 Coaxial Cable – 75 Ω	9.31 Ω
T1 Twisted Pair – 100 Ω	12.4 Ω

The 150 Ω series resistors protect both the LIU and the analog switches from residual surge currents coupled through the transformer and line side protection. In order to optimize the receiver performance and return loss, the Maxim* MAX4717 offers the right balance of low R_{on} and low capacitance. It offers 3 Ω typical R_{on}, and very low capacitance (C_{ON} = 15 pF typical and C_{OFF} = 9 pF typical).

4.0 Transmit Interface Circuit

Figure 2, “Transmit Interface, E1 Mode” on page 8 and Figure 3, “Transmit Interface, T1 Mode” on page 9 show the recommended transmit interface circuits for E1 and T1. Both circuits assume the LXT38x transmitters are powered by a 3.3 V power supply. With this approach, it is possible to design a common board for both T1 and E1 operation just by setting different “stuffing options.”

In E1 mode, the recommended transmit resistors are 10.5 Ω (instead of the 11 Ω per the LXT38x datasheets). This effectively compensates for the 0.6 Ω typical on-resistance (R_{on}) in the analog switch.

In T1 applications (Figure 3), the transmit resistors are replaced with a small ferrite bead (Lt), such as the LI0603G800R-00 from Steward* (<http://www.steward.com>). The parallel capacitor is increased to 1500 pF. This circuit ensures good pulse template performance in T1 mode.

Surge protection is provided by a Transient Voltage Suppressor (TVS) in the line side of the transformer and by clamping diodes in the chip-side (such as the BAT54S). Please refer to the Intel application notes and reference designs for additional information regarding surge protection.

The extremely low R_{on} in the MAX4714/36 is critical to ensure that the pulse amplitude remains within specifications over temperature and power supply variations. Furthermore, the 0.1 Ω R_{on} flatness of the switch ensures that the output pulse is not distorted. Low capacitance is also important to ensure good pulse template and return loss performance. The MAX4714/36 features very low capacitance (C_{ON} = 65 pF typical and C_{OFF} = 30 pF typical) which results in very good performance in this application as demonstrated in Section 5.0, “Test Results” on page 10.

Figure 1. Receive Interface

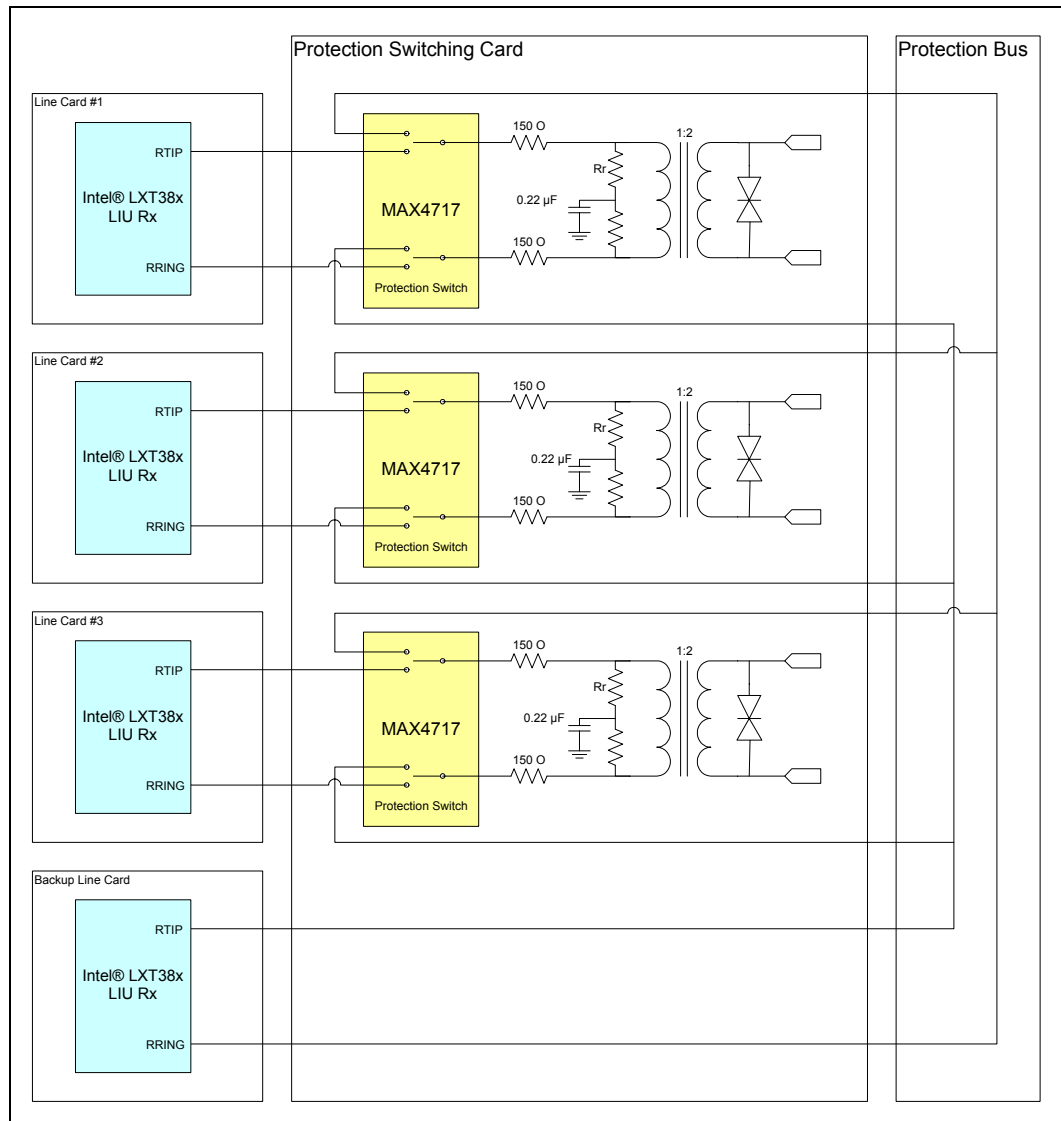


Figure 2. Transmit Interface, E1 Mode

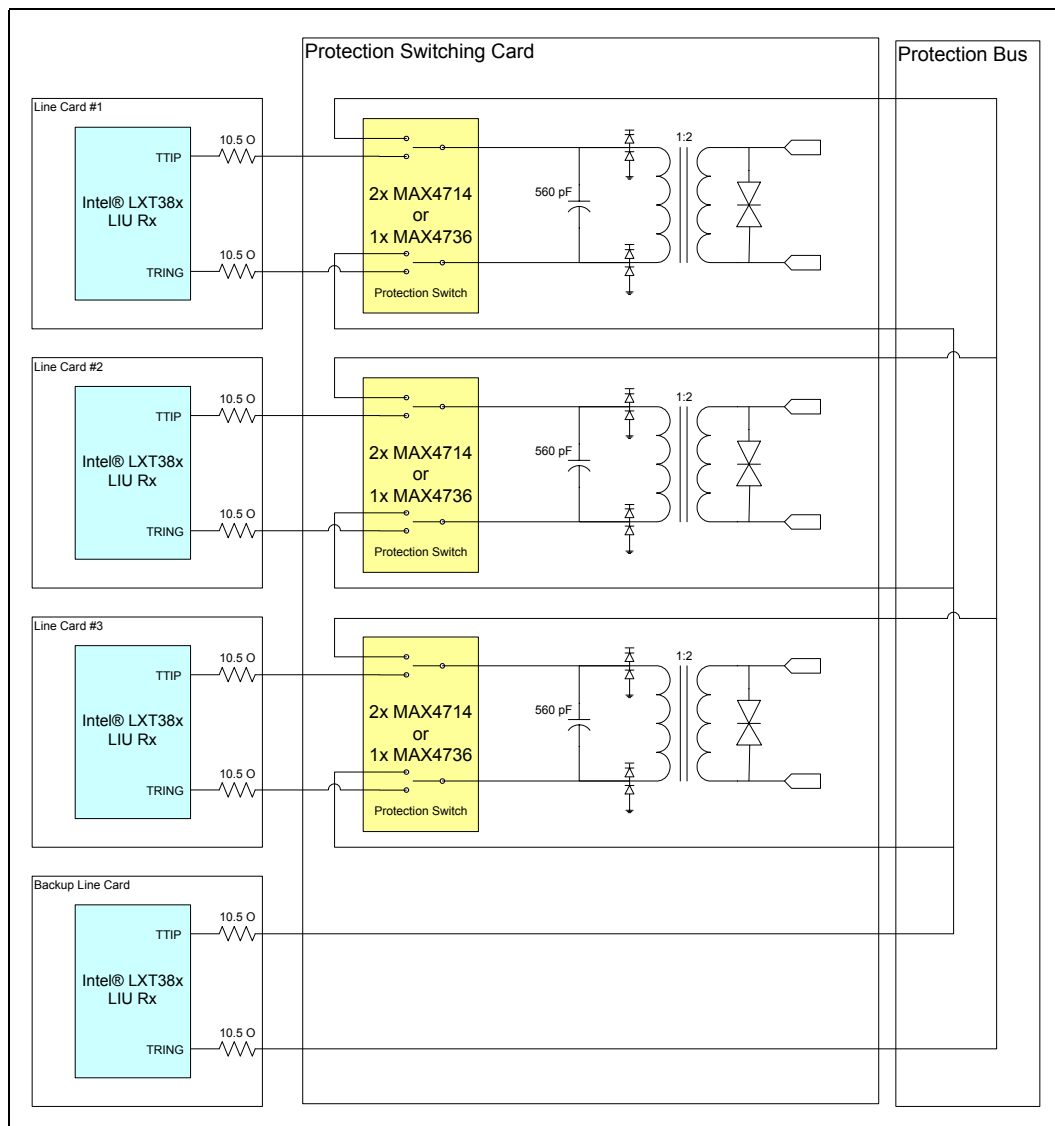
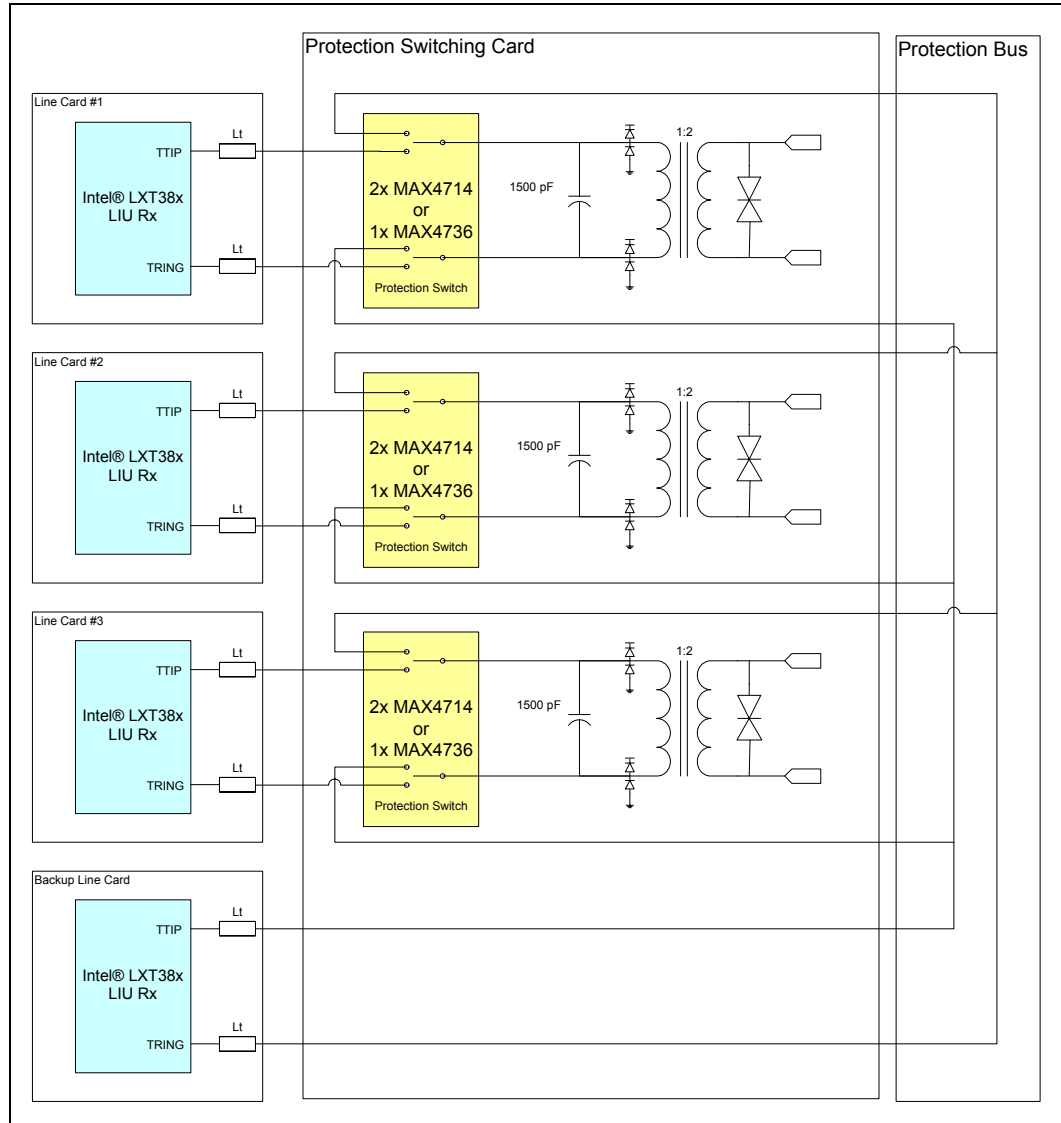


Figure 3. Transmit Interface, T1 Mode



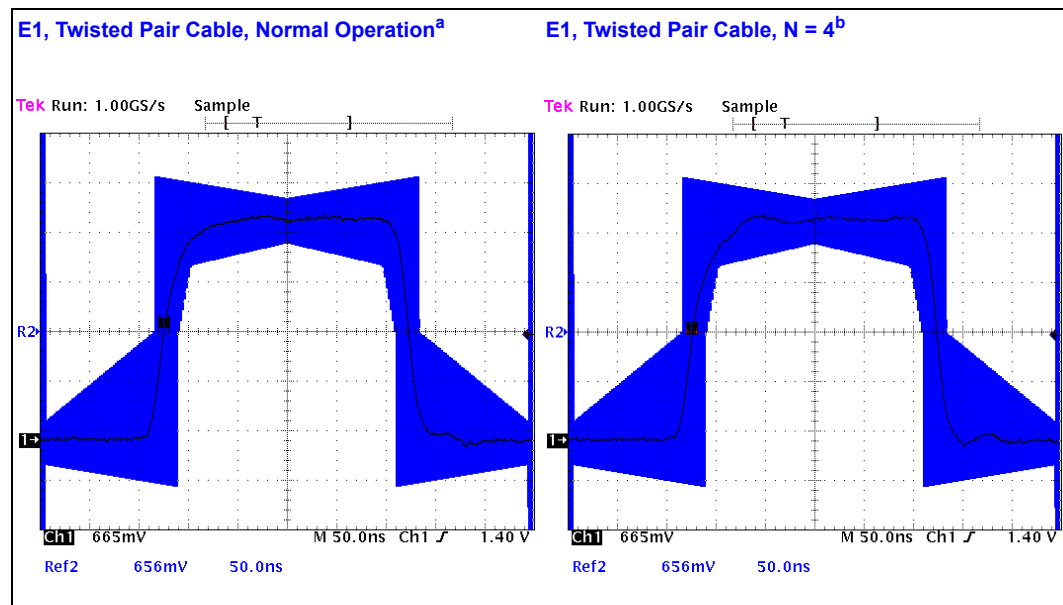
5.0 Test Results

Figure 1, “Receive Interface” on page 7 through Figure 3, “Transmit Interface, T1 Mode” on page 9 illustrates that as the number of boards N in an $N+1$ redundancy implementation increases, so does the maximum parallel off-capacitance that the backup board LIU observes. This parallel capacitance has some effect on the output pulse shape and in the return loss performance. However, in normal operation (backup board inactive), the switch on-capacitance is the predominant capacitance the LIU sees and this (smaller) capacitance is easily handled.

For good performance with the worst case capacitive loading condition (backup board active), Intel recommends that the number N does not exceed 8 (1:8 redundancy protection).

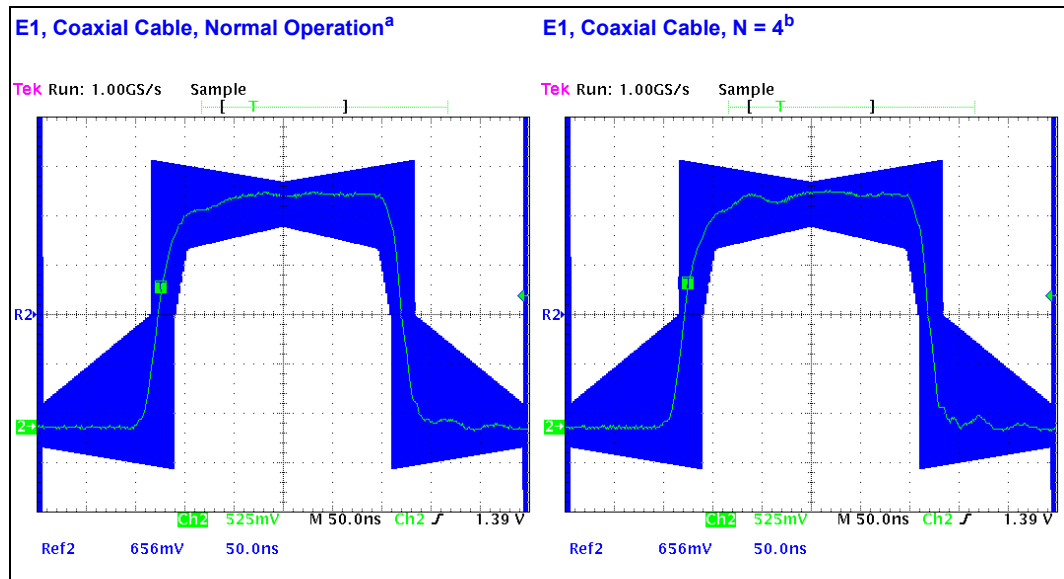
Figure 4, “Output Pulses, E1 Twisted Pair” on page 10 through Figure 6, “Output Pulses, T1 Mode” on page 11 show the measured T1/E1 output pulses using the MAX4717 and the MAX4714 analog switches and an LXT384 LIU.

Figure 4. Output Pulses, E1 Twisted Pair



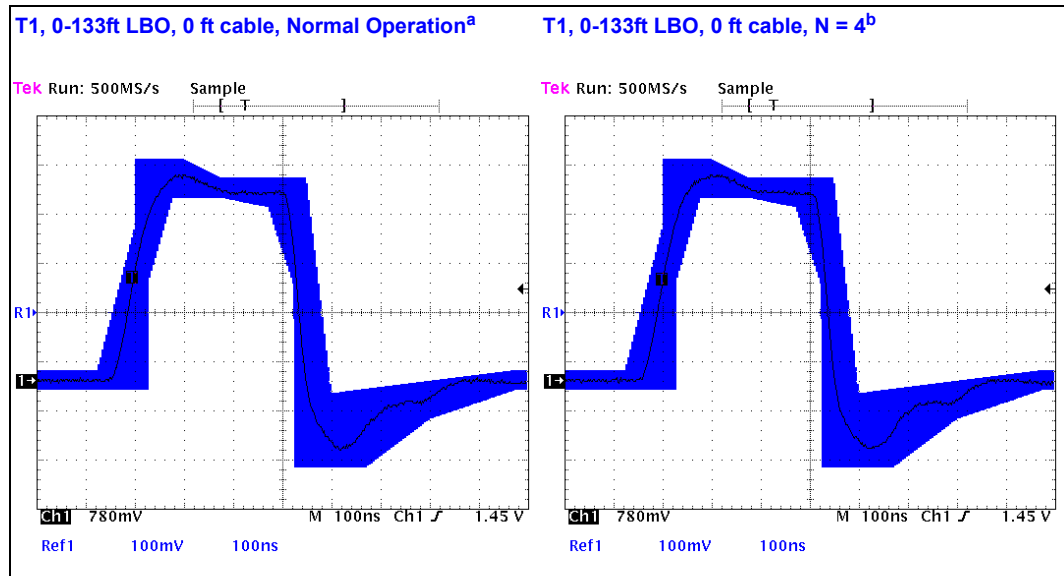
- a. Output pulse through two series switches in the transmit path
- b. Output pulse from backup board with 4+1 configuration.

Figure 5. Output Pulses, E1 Coaxial Cable



- a. Output pulse through two series switches in the transmit path
- b. Output pulse from backup board with 4+1 configuration.

Figure 6. Output Pulses, T1 Mode



- a. Output pulse through two series switches in the transmit path
- b. Output pulse from backup board with 4+1 configuration.

