

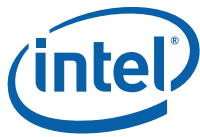
Intel[®] 413808 and 413812 SAS/SATA I/O Controllers

Specification Update

| *July 2008*

Notice: The Intel[®] 413808 and 413812 SAS/SATA I/O controllers may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

| Order Number: 315043-007US



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Revision History

Date	Version	Description
July 2008	007	<ul style="list-style-type: none">• Added Document Change 2.• Added Specification Clarification 6.• Revised Errata 25 - 26.
December 2007	006	<ul style="list-style-type: none">• Revised Table 1 and Table 2.
October 2007	005	<ul style="list-style-type: none">• Revised Errata 22 - 24.• Added Specification Changes 1 and 2.• Added Specification Clarification 5.• Added Document Change 1.
March 2007	004	<ul style="list-style-type: none">• Revised Errata C1 column with appropriate “x” steppings.
March 2007	003	<ul style="list-style-type: none">• Revised Errata C1 column with appropriate “x” steppings.• Revised Specification Clarification C1 column with appropriate “x” steppings.
February 2007	002	<ul style="list-style-type: none">• Added Errata 19 - 22.• Updated Table 1, “Die Details” on page 10.• Updated Errata 7 and 18.• Updated Specification Clarification 1 and 2• Removed Errata 1, 2, 8, 9, 12, 16, and 17 from the previous version of this document. They do not apply to this product.• Removed previous Specification Clarification 4.
September 2006	001	Launch Release.



Preface

This document is an update to the specifications contained in the *Affected Documents/Related Documents* table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel® 81348 I/O Processor Developer's Manual	315036
Intel® 413808 and 413812 SAS/SATA I/O Controllers Datasheet	315040

Nomenclature

Errata are design defects or errors. These may cause Intel® 413808 and 413812 behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 413808 and 413812 product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X: Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.

(No mark)
or (Blank box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page): Page location of item in this document.

Status

Doc: Document change or update will be implemented.

Fixed: This erratum has been previously fixed.

NoFix: There are no plans to fix this erratum.

Plan Fix: This erratum may be fixed in a future stepping of the product.

Row

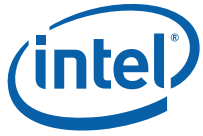


Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.



Errata

No.	Steppings					Page	Status	ERRATA
	A0	A1	B0	C0	C1			
1								Removed
2								Removed
3	X	X	X	X	X	12	No Fix	GNT# to FRAME# timing violation by one clock in ATUX
4	X	X	X	X	X	12	No Fix	ATUE ATUCR[4] functionality has been defeatured
5	X	X	X	X	X	12	No Fix	Spurious DMA0 End-Of-Transfer Interrupt
6	X	X	X	X	X	13	No Fix	Data parity errors occurring on an inbound write transactions are not to be logged by South Internal Bus (IB) to North IB bridge (XBG)
7	X	X	X	X	X	13	No Fix	PCI outputs might not float within 40ns after P_RST# asserts
8								Removed
9								Removed
10	X	X	X	X	X	14	No Fix	With default drive strengths, the General Purpose output pads may fail to meet the min VOH1 specification (2.6V) at max IOH (-10mA)
11	X	X	X	X	X	14	No Fix	There is an internal timing violation through PMMRBAR
13	X	X	X	X	X	14	No Fix	ATUE maximum allowable lane skew of 20 ns is not being met
14	X	X	X	X		14	Fixed	Potential Transmit Buffer and Receive Buffer Over-runs/Under-runs may occur when the SRAM Controller loses its request before the memory transaction is acknowledged by the SRAM Controller
15	X	X	X	X	X	15	No Fix	Following the de-assertion of WARM_RST#, the ATU-E can lock up, which can only be exited with a full reset (assertion of P_RST#)
16								Removed
17								Removed
18	X	X	X	X	X	15	No Fix	The PCI memory window is not retained following preemptive resets
19	X	X	X	X		15	Fixed	Potential Transmit Buffer and Receive Buffer Over-runs/Under-runs occur when the SRAM Controller loses its request before the memory transaction is acknowledged by the SRAM Controller
20	X	X	X	X	X	16	No Fix	Hot-Swap Next Item Pointer (HS_NXTP) Register does not reset
21	X	X	X	X	X	16	No Fix	PBI read data gets corrupted when reading PBI MMRs while there is actual PBI read activity on the bus
22	X	X	X	X	X	17	No Fix	8034x does not support Spread Spectrum Clock (SSC) For SATA drives
23	X	X	X	X	X	17	No Fix	The SMBus reads are not supported
24	X	X	X	X	X	17	No Fix	The SMBus unit (SMU) implements the Packet Error Check (PEC) incorrectly
25	X	X	X	X	X	17	No Fix	The MSI-X Capability ID is incorrect for 413808 and 413812
26	X	X	X	X	X	18	No Fix	Inbound MSI gets lost when core is simultaneously writing to IMIPRx to clear a previous interrupt





Specification Changes

No.	Steppings		Page	Status	SPECIFICATION CHANGES
	B0	#			
1	X		19	Doc	The Maximum Specification for the REFCLK Rise Time and Fall Time changed from 350ps to 700ps to match the PCI Express Specification
2	X		19	Doc	The VIH max level is changing from 1.8V to 2.0V for the p_mode2 and p_clkin pins

Specification Clarifications

No.	Steppings					Page	Status	SPECIFICATION CLARIFICATIONS
	A0	A1	B0	C0	C1			
1	X	X	X	X	X	20	No Fix	ATUe and ATU-X Outbound Memory Windows overlap at power-on
2	X	X	X	X	X	21	No Fix	Adequate delay required when programming some Memory-Mapped Registers (MMR)
3	X	X	X	X	X	22	No Fix	During power-up, it is normal to see a current and voltage fluctuations on the 3.3 V, 1.8 V and 1.2 V power supplies
4								Removed
5	X	X	X	X	X	22	Doc	Clarification on the initialization procedure for the circular queues
6	X	X	X	X	X	23	Doc	CPLD bus keepers must be turned off during compilation

Documentation Changes

No.	Document Revision	Page	Status	DOCUMENTATION CHANGES
1	315046	24	Doc	The "Note" in the section on supported Flash is wrong
2	315046	25	Doc	The VCCPLL Pin Requirements section of the Datasheet have changed



Identification Information

Die Details

Table 1. Die Details

Stepping	Part Number	QDF (Q)/ Specification Number (SL)	Processor Speed (MHz)	Notes
A0	HP413808	Q077	800/400	Pb Alpha Samples Single Interface – 8 Port
A0	HP413808	Q137	800/400	Pb Alpha Samples Single Interface – 8 Port
A1	HP413808	Q265	800/400	Pb Alpha Samples Single Interface – 8 Port
B0	WP413812	Q535	1200/400	Pb-free Samples Single Interface – 8 Port
B0	WP413808	Q536	800/400	Pb-free Samples Single Interface – 8 Port
C0	WP413812	Q617	1200/400	Pb-free Samples Single Interface – 8 Port
C0	WP413808	Q618	800/400	Pb-free Samples Single Interface – 8 Port
C1	WP413812	Q824	1200/400	Pb-free Samples Single Interface – 8 Port
C1	WP413808	Q825	800/400	Pb-free Samples Single Interface – 8 Port
C1	WP413812	SL9XV	1200/400	Pb-free Production Single Interface – 8 Port
C1	WP413808	SL9XW	800/400	Pb-free Production Single Interface – 8 Port
C1	WP413812	SLAMU	1200/400	Pb-free Production Single Interface – 8 Port
C1	WP413808	SLAMV	800/400	Pb-free Production Single Interface – 8 Port

Note: SLAMU replaces SL9XV and SLAMV replaces SL9XW.



Table 2. Device ID Registers

Device and Stepping	Processor Device ID (CP15, Register 0 - opcode_2=0)	ATU Revision ID	JTAG Device ID
1200/800 MHz cores, 8-port, Single-interface (PCIe or PCI-X) ATUe (TPMI) Device ID: 0x3363 with Transport FW running 0x3362 without Transport FW running ATUX (TPMI) Device ID: 0x336B with Transport FW running 0x336A without Transport FW running			
A0	0x69056010	0x0	0x01203013
A1	0x69056011	0x1	0x11203013
B0	0x69056014	0x4	0x41203013
C0	0x69056818	0x8	0x81203013
C1	0x69056819	0x9	0x91203013
C1	0x69056819	0x9	0x91205013

Note: 0x91203013 applies to SL9XV/SL9XW and 0x91205013 applies to SLAMU/SLAMV.



Errata

1. Removed

2. Removed

3. GNT# to FRAME# timing violation by one clock in ATUX

Problem: The GNT# to FRAME timing is in violation of the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0. This violation can occur only when the ATU-X masters back-to-back requests. When there is another PCI device that wants the bus, GNT# rotates away from 413808 and 413812. So, in a system with balanced bus traffic this violation is less likely to occur.

Implication: Although this is a violation of *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0, it is for a performance issue which other PCI devices tolerate. 413808 and 413812 taking an extra clock to assert FRAME# is not a functional problem.

Workaround: No workaround.

Status: No Fix. See the [Table](#) , "Summary Table of Changes" on page 6.

4. ATUE ATUCR[4] functionality has been defeated

Problem: The "Inbound Minimum Completion Size" feature of the ATUCR (bit 4) has been defeated in the ATUE.

Implication: The "Inbound Minimum Completion Size" feature of the ATUCR (bit 4) cannot be enabled. ATUCR[4] needs to remain at the default value of '0'.

Workaround: No workaround.

Status: No Fix. See the [Table](#) , "Summary Table of Changes" on page 6.

5. Spurious DMA0 End-Of-Transfer Interrupt

Problem: When the interrupt controller goes from having no interrupts asserted to 1 or more asserted, there is a 1 clock cycle window in which the IINTVEC (IRQ Interrupt Vector register: CP6, Page 2, Register 3) or FINTVEC (FIQ Interrupt Vector register: CP6, Page 2, Register 4) may report the value of the INTBASE register (Interrupt Base register: CP6, Page 2, Register 0), which is the vector address for interrupt 0, DMA0 End-of-Transfer.

This condition can occur even when the DMA0 EOT interrupt is masked, INTCTL0.0 = 0.

Implication: No negative impact expected. When the interrupt service routine that reads the IINTVEC/FINTVEC qualifies the return value against IINTSRC0.0/FINTSRC0.0, it either sees there is nothing to do or it validly calls the DMA0 End-of-Transfer handler.

Workaround: When IINTVEC/FINTVEC equals INTBASE, then re-read the IINTVEC/FINTVEC register.

Status: No Fix. See the [Table](#) , "Summary Table of Changes" on page 6.



6. Data parity errors occurring on an inbound write transactions are not to be logged by South Internal Bus (IB) to North IB bridge (XBG)

Problem: During inbound transactions (transactions flowing from the South IB to the North IB), when the inbound request to XBG is corrupted with data parity error, it is not being logged. The bug is exercised by writes which would cross a 16B boundary and result in two XSI data phases with a parity error in the 1st phase (for example, 32B writes.) Aligned DWORD (4B) writes, QWORD (8B) writes and OWORD (16B) writes are all unaffected, but anything larger could trigger the erratum. It affects only parity errors in the 1st data phase of a two data phase inbound write (for example, bytes 0 through 15 of a 32B write.) It does NOT affect completions.

Implication: When a data parity error occurs during inbound write requests to the XBG, it should be logged. Because the data parity error is not logged an XBG error interrupt does not occur.

Workaround: No workaround.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

7. PCI outputs might not float within 40ns after P_RST# asserts

Problem: Per the *PCI-X Addendum to the PCI Local Bus Specification*, Revision 2.0, when P_RST# asserts, PCI outputs must be floated within 40ns. PCI outputs might not float within 40ns after P_RST# asserts.

The issue is, that the divider codes to the PCI-X PLL can change after P_RST# assertion, but BEFORE the PLL has been disabled (the divider codes are changing on-the-fly). This can mess with pp_clk, which 413808 and 413812 is relying on to provide clocks for the pad OE flops, so that the PCI-X pads float within the required time after P_RST# asserts.

If the MCU is enabled there is even less of a chance of this happening since the powerfail sequence must complete before internal reset, and during the powerfail sequence the PCI output buffers have plenty of time to become disabled. Even with the MCU disabled, there is very little likelihood, and maybe none, of triggering an issue. This has never been seen in any post silicon validation or testing and therefore, unlikely to ever occur.

Implication: The danger is not only the violation of the 40ns float time in the specification, but the possibility of not turning off the OE signals. This would cause contention with the Central Resource and result in it not being able to configure the device properly (contention could occur on the initialization pattern signals, for example).

Workaround: If this problem surfaces, force the ATU-X off of the PCI bus before asserting P_RST# (turn off bus master enable, turn off memory enable). This guarantees the PCI-X output enables are OFF when P_RST# asserts.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

8. Removed

9. Removed



10. **With default drive strengths, the General Purpose output pads may fail to meet the min VOH1 specification (2.6V) at max IOH (-10mA)**

Problem: With default drive strengths, the General Purpose output pads may fail to meet the min VOH1 specification (2.6V) at max IOH (-10mA).

Implication: In high current source application, e.g. sourcing current to an LED, the General Purpose output pads (all pads except for PCI and analog PHYs) may not meet the VOH1 2.6V spec. They are however capable of driving to 2.4V at -10 mA. Also, there is no problem with the VOL1 spec when sinking IOL (+10 mA), so driving LEDs in an open-drain manner is acceptable.

Workaround: No workaround.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

11. **There is an internal timing violation through PMMRBAR**

Problem: There is an internal timing violation through PMMRBAR.

Implication: May have to use the default values of the PMMRBAR.

Workaround: Use either of the two possible workarounds for this erratum.

1. Do not write to this register, just use the default value.
2. Ensure that both the North and South Internal Bus are completely inactive for 20 bus clocks following any update to this register.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

12. **Removed**

13. **ATUE maximum allowable lane skew of 20 ns is not being met**

Problem: The maximum allowable lane skew of 20 ns is not being met. The PCIe electrical specification, Version 1.1, Section 5.3.5: "Lane-to-Lane Skew", defines the allowable Interconnect Lane-to-Lane Skew as 1.6 ns. The most lane-to-lane skew seen externally is 1.6 ns + 1.3 ns (Ltx=500+2UIps) = 2.9 ns.

The maximum lane-to-lane skew the device can tolerate is ~15.76 ns.

Implication: Although this is a specification violation, the impact is negligible as the expected maximum lane skew is on order of ~2.9 ns which leaves ~12.9 ns of margin.

Workaround: No workaround.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

14. **Potential Transmit Buffer and Receive Buffer Over-runs/Under-runs may occur when the SRAM Controller loses its request before the memory transaction is acknowledged by the SRAM Controller**

Problem: Under certain conditions (abnormal or error) the protocol engine may violate protocol to the SRAM Controller by removing its request before the memory transaction is acknowledged by the SRAM Controller - essentially it is trying to abort the request.

Implication: This can result in Transmit Buffer over-runs/under-runs and Receive Buffer over-runs/under-runs - all of which can result in retried I/Os. Either case is a very rare occurrence

Workaround: No workaround.

Status: Fixed in C1. See the Table , "Summary Table of Changes" on page 6.



15. Following the de-assertion of WARM_RST#, the ATU-E can lock up, which can only be exited with a full reset (assertion of P_RST#)

Problem: Following the de-assertion of WARM_RST#, the ATU-E can lock up, which can only be exited with a full reset (assertion of P_RST#).

Implication: The PCI-E link is completely unusable since no traffic passes through the ATU-E.

Workaround: When using WARM_RST#, the maximum reset duration should not exceed 24 ms time.

Other workarounds:

1. When in Endpoint Mode, set LK_DN_RST_BYPASS# to "0". Following WARM_RST# deassertion, issue a Hot Reset to the controller. Setting the LK_DN_RST_BYPASS# strap to '0' prevents a full-chip reset as a result of the hot reset message.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

16. Removed

17. Removed

18. The PCI memory window is not retained following preemptive resets

Problem: The PCI memory window is not retained following preemptive resets.

PCI configuration space should be preserved during an Internal Bus (IB) Reset.

The IALR (limit register) and the IATVR0/IAUTVR0 (translate value registers) are implemented in control register space (not in configuration space) so these get reset on an IB reset.

Implication: Because the limit register is AND'ed into the BAR, the resetting of the limit register causes the BAR to also get reset (indirectly).

This causes the BAR to go back to its default of 16 MB. This can cause overlapping BARs (if the BAR had been previously reduced to some size less than 16 MB) and potentially a system crash.

Workaround: Always use the default 16 MB limit register value.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

19. Potential Transmit Buffer and Receive Buffer Over-runs/Under-runs occur when the SRAM Controller loses its request before the memory transaction is acknowledged by the SRAM Controller

Problem: Under certain conditions (abnormal or error) the protocol engine violate protocol to the SRAM Controller by removing its request before the memory transaction is acknowledged by the SRAM Controller - essentially it is trying to abort the request.

Implication: This results in Transmit Buffer over-runs/under-runs and Receive Buffer over-runs/under-runs - all of which results in retried I/Os. Either case is a very rare occurrence.

Workaround: No workaround.

Status: Fixed in C1. See the Table , "Summary Table of Changes" on page 6.



20. Hot-Swap Next Item Pointer (HS_NXTP) Register does not reset

Problem: The Hot-Swap Next Item Pointer register normally resets to 0 (to indicate that it is the final capability in the capabilities list). Instead, it resets to 0xE8.

The Developer's Manual is inconsistent. The "Default" column clearly states 0xE8, but the "Description" column clearly states 0x00. The RTL implements the "Default" column.

Implication: This only impacts applications that use the PCI-X bus in endpoint mode. When the HS_NXTP resets to 0xE8 as the default, it points to the Hot-swap capability, thereby creating a possible infinite loop in enumeration S/W.

The other thing to point out that when cores are held in reset and Configuration Retry is disabled, then there is still exposure to a possible lock-up in the enumeration BIOS. The two scenarios impacted by this are FRU and Flashless boots.

Workaround: Firmware is already given the option to program the register to 0x90 (to link in the VPD capability). Therefore, we recommend that F/W always programs the register; either to 0x00 (no VPD) or to 0x90.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

21. PBI read data gets corrupted when reading PBI MMRs while there is actual PBI read activity on the bus

Problem: PBI read data gets corrupted when reading PBI MMRs while there is PBI read activity on the bus and while there is long latency bus activity on the South XSI bus (XSI bus activity other than PBI reads and MMR reads). The XSI activity is the component of this issue that holds data in the PBI completion buffer making it susceptible to being overwritten by a subsequent PBI read while reading a PBI MMR. This occurrence is limited to reads of the following MMRs: PBCR, PBISR, PBBAR0, PBLR0, PBBAR1, PBLR1.

Implication: PBI read data can get corrupted.

Workaround: Occurrence of this issue is very unlikely, but observe the following precautions:

- Read the MMRs listed above only during initialization and prior to any large transactions occurring on the South XSI bus.
- During normal operating mode, avoid reads of these MMRs. When a PBI MMR read is required, ensure that there are no PBI bus reads occurring.
- The only affected PBI register that a user normally considers reading after initialization is the PBI Status Register (PBISR). However, since there is only one interrupt source for the PBI bus, when the Interrupt Pending Register1 indicates a PBI Interrupt, it is redundant to read PBISR to determine the interrupt cause.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.



22. 8034x does not support Spread Spectrum Clock (SSC) For SATA drives

Problem: 8034x does not support Spread Spectrum Clock (SSC) for SATA drives.

Implication: Although some drives appear to function correctly with SSC enabled, extended duration testing results in various signal integrity issues.

Workaround: Do not enable SSC on any SATA drives.

Status: **No Fix.** See the [Table](#) , “[Summary Table of Changes](#)” on page 6.

23. The SMBus reads are not supported

Problem: Writes corrupt SMBus read data which renders SMBus reads non-functional.

Implication: SMBus reads are not supported. No problem has been found with SMBus writes.

Workaround:

1. Use I²C Master to send outbound messages/responses (requires slave capability on the customer end of SMBus).

HW Changes to implement this workaround:

- I2C0 SCL -> SMBus SCL
- I2C0 SDA -> SMBus SDA
- I2C0 GND -> SMBus GND

On most boards there are three pins per each I²C: clock, data, and ground. The external I²C master connects to a ground, but this is just a common ground, so it is just two wires (clock and data) on the board and with no need to worry about the GND pin.

2. Use GPIOs to emulate an I²C Master (requires slave capability on the customer end of SMBus).

Status: **No Fix.** See the [Table](#) , “[Summary Table of Changes](#)” on page 6.

24. The SMBus unit (SMU) implements the Packet Error Check (PEC) incorrectly

Problem: The SMU slave is calculating the PEC incorrectly. The slave address is incorrectly being added to the start of the byte stream. For example, in a 4 byte block write sequence the PEC needs to be the CRC-8 of the 7 bytes from Address to D3 as follows:

PEC = CRC-8 (Address, CommandCode, ByteCount, D0, D1, D2, D3)

The SMBus unit is calculating the PEC as follows:

PEC = CRC-8 (SA, Address, CommandCode, ByteCount, D0, D1, D2, D3) where SA = the SlaveAddress programmed into the slave.

Implication: The PEC calculation will be incorrect.

Workaround: No workaround. PEC is an optional feature for SMBus and has been de-featured.

Status: **No Fix.** See the [Table](#) , “[Summary Table of Changes](#)” on page 6.

25. The MSI-X Capability ID is incorrect for 413808 and 413812

Problem: The MSI-X Capability ID is incorrect for the 413808 and 413812; MSI-X Capability ID is 0x11 on the PCI Specification while the 413808 and 413812 is 0x0D.

Implication: The 413808 and 413812 do not support MSI-X.

Workaround: A change in firmware is needed to ***hide*** MSI-X capabilities from the OS.

Status: **No Fix.** See the [Table](#) , “[Summary Table of Changes](#)” on page 6.



26. Inbound MSI gets lost when core is simultaneously writing to IMIPRx to clear a previous interrupt

Problem: Inbound MSI gets lost when core is simultaneously writing to IMIPRx to clear a previous interrupt.

1. Intel XScale® microarchitecture writes to IMIPRx to clear the interrupt bit for the first MSI.
2. In the same clock cycle, the MU is trying to set a bit in the same IMIPRx for the second MSI.

When these two conditions occur in the same clock cycle to the same IMIPRx, the "set" operation for the second interrupt fails to set the bit.

Implication: Inbound MSI gets lost when core is simultaneously writing to IMIPRx to clear a previous interrupt.

Workaround: Use no more than one bit in each IMIPRx giving a total of only four possible inbound MSIs, in other words, one bit in each of IMIPR0, IMIPR1, IMIPR2, IMIPR3.

Status: No Fix. See the [Table](#) , "Summary Table of Changes" on [page 6](#).



Specification Changes

1. The Maximum Specification for the REFCLK Rise Time and Fall Time changed from 350ps to 700ps to match the PCI Express Specification

Problem: The Maximum Specification for REFCLK Rise Time and Fall Time in "Table 21, PCI Express Clock Timing", in the 4138xx Datasheet, has changed from 350ps to 700ps to match the PCI Express Specification.

Affected Docs: Intel® 413808 and 413812 I/O Controllers Datasheet

2. The VIH max level is changing from 1.8V to 2.0V for the p_mode2 and p_clkin pins

Issue: The VIH max level is changing from 1.8V to 2.0V for the p_mode2 and p_clkin pins.

Affected Docs: Intel® 413808 and 413812 I/O Controllers Datasheet



Specification Clarifications

1. **ATUe and ATU-X Outbound Memory Windows overlap at power-on**

Issue: The Outbound Memory Windows (OUMBARs) for the ATUe and ATU-X are enabled and overlap by default when the 413808 and 413812 are powered on. This causes internal bus conflict when writing to the Outbound Window since each ATU tries to claim that address. The simplest fix is to only enable OUMBAR0 for ATU-X and OUMBAR1 for ATUe. The enable bit must be cleared in the other OUMBAR (Bit 31) to disable them.

Affected Docs: Intel® 81348 I/O Processor Developer's Manual

Status: No Fix. See the [Table](#) , "Summary Table of Changes" on page 6.



2. Adequate delay required when programming some Memory-Mapped Registers (MMR)

Issue: Most peripheral units must be initialized/programmed by firmware using their respective memory-mapped registers (MMRs) before they can be used. Some examples of these registers are:

- Base Address Registers
- Limit Registers
- Size Registers

In addition, some of the peripheral units provide registers that are used as Address/Data Ports and for testing purposes. Firmware must ensure that any change made to these types of memory-mapped registers have successfully taken effect before further action is taken on that peripheral unit.

The registers which are written will not be updated immediately, so a subsequent transaction that relies on the register being updated may fail. When writing a value to an MMR that can change the operating mode or configuration of the system, the programmer must ensure that the register has been properly updated before subsequent transactions that are dependent on the written data begin execution. To do this, perform a read of the MMR after writing it and also create a data dependency on the read completing before subsequent instructions can execute.

One example where a register update must be in place before continuing, is the DLLRCVER register auto-calibration routine. In this example, the DLLRCVER register must be updated before a memory location can be read and then the memory operation must be complete before the DLLRCVER register can be read. Therefore, the DLLRCVER register is written, read-back, and then a register dependency is placed on the register for the read data, which means the read data must be returned before the read from DDR takes place. Then memory is read and a dependency is placed on the memory read to ensure data has returned before the DLLRCVER register is sampled.

```
#define MCU_DLLRCVER ((volatile unsigned int*)0xFFD82030)

/* Write DLLRCVER Register */
*MCU_DLLRCVER = data;

/* Read register back to push the value to the register */
val = *MCU_DLLRCVER;

/* Put a register dependency on the data being read back to make the core stall until
read data returns, which ensures the write has occurred*/
asm volatile("mov %0, %0" : : "r" (val));

/* Read a DDR SDRAM Memory Location, this memory read causes the auto calibration
circuit to sample the DQS signal */
val = *ddr_mem_addr;

/* Put a register dependency on the data being read back to ensure that the read from
memory has taken place */
asm volatile("mov %0, %0" : : "r" (val));

/* Read DLLRCVER register bit 24 to get DQS sample */
val = *MCU_DLLRCVER & (1<<24);

/* The comparison creates a dependency to ensure the data has returned from the
register */
return (val == 0 ? val : 1);
```

Affected Docs: Intel® 81348 I/O Processor Developer's Manual.

Status: **No Fix** in B0 See the [Table](#) , "Summary Table of Changes" on page 6.



3. During power-up, it is normal to see a current and voltage fluctuations on the 3.3 V, 1.8 V and 1.2 V power supplies

Issue: The following may be observed during initial device power-up.

1. During initial power-up, it is normal to see a current drop on supplies that were powered up earlier as subsequent supplies power up. This is due to internal leakage paths being disabled.
2. When the 3.3 V supplies are powered up first it is normal to see the 1.2 V rail come part way up. This is due to internal paths between the two supplies that get isolated after the 1.2 V rail powers up.
3. During device power-on, it is normal to see a current drop on the 3.3 V supplies after the 1.2 V supplies powers up. The 3.3 V I/Os are disabled until all power rails are up and running. Once the other power rails are up and running the 3.3 V I/Os are enabled and this is the reason for the current drop.
4. Vcc1p8e voltage goes up to ~750 mV when the Vcc1p2e power rails go up. It stays at ~750 mV until it is powered up and then it goes to 1.8 V.

Affected Docs: Intel® 413808 and 413812 SAS/SATA I/O Controllers Datasheet.

Status: No Fix. See the Table , "Summary Table of Changes" on page 6.

4. Removed

5. Clarification on the initialization procedure for the circular queues

Issue: Do not let Host write to outbound post queue.

The circular queues must be initialized starting with the HEAD first and then the tail, or the queue is considered full and a write is continuously retried, causing a hang condition.

Figure 1. Required Initialization Order for Circular Queues

```

IN_FREE_HEAD_REG = IN_FREE_BOTTOM
IN_FREE_TAIL_REG = IN_FREE_BOTTOM
IN_POST_HEAD_REG = IN_POST_BOTTOM
IN_POST_TAIL_REG = IN_POST_BOTTOM
OUT_FREE_HEAD_REG = OUT_FREE_BOTTOM
OUT_FREE_TAIL_REG = OUT_FREE_BOTTOM
OUT_POST_HEAD_REG = OUT_POST_BOTTOM
OUT_POST_TAIL_REG = OUT_POST_BOTTOM

```

The MU is now a device on the Internal Bus (IB) and it can claim any transaction on the South IB, which hits its MUBAR/MUUBAR. This includes for example, using the ADMA for initial DDR memory scrub. Note that core access to memory does not conflict with the MU since the core comes in from the North IB and is isolated via the internal bridge. In situations where South IB access conflicts with the MU region, use the core to access that region of DDR.

Because the MU is now movable on the IB, the inbound translation value register, for the appropriate inbound BAR, is programmed to match the MU base, to assure inbound traffic translates as expected.

Status: Doc. See the Table , "Summary Table of Changes" on page 6.



6. CPLD bus keepers must be turned off during compilation

Issue: CPLD bus keepers must be turned off during compilation.

The bus keepers in the CPLD take the Flash bus width selection during power on to an indeterminate level (~1-1.2V) when the supply voltage is 3.6 V. By turning off the bus keepers for the CPLD this does not occur.

Status: Doc. See the [Table](#) , “[Summary Table of Changes](#)” on page 6.



Documentation Changes

1. The “Note” in the section on supported Flash is wrong

Problem: The “Note” in the section on supported Flash in the “Design Notes” section of the 81341/81342 Design Review Checklist is wrong.

The “Note” in the section on supported Flash in the “Design Notes” section of the 81341/81342 Design Review Checklist should read:

“Note: Flash device that support **CFI Cmd set 1 (CFI1).**”

Affected Docs: Intel® 413808 and 413812 I/O Controllers Design Review Checklist

Status: Doc. See the [Table](#) , “Summary Table of Changes” on page 6.



2. The VCCPLL Pin Requirements section of the Datasheet have changed

Problem: The VCCPLL Pin Requirements section of the Datasheet have changed. See below for the updates in Section 4.1 and Figure 8 in the Datasheet.

Implication:

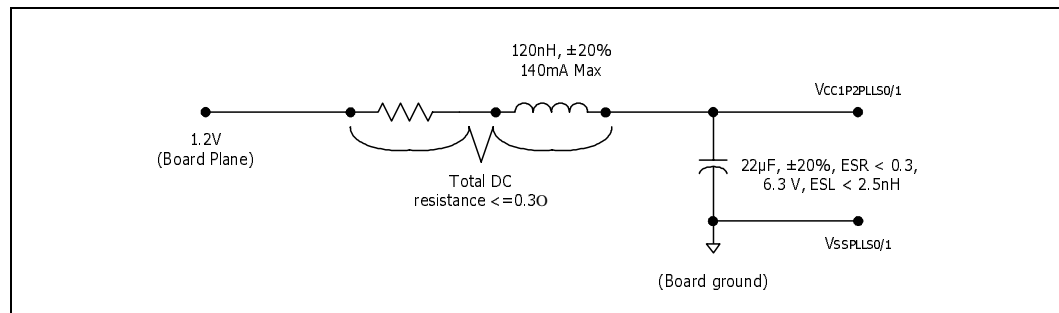
New wording for Section 4.1 - VCCPLL Pin Requirements (last two paragraphs):

This paragraph pertains to the VCC1P2PLLS0, VCC1P2PLLS1 filters. The recommended filter for the PLL supplies is shown in Figure 8. The purpose of this filter is to achieve at least 10 dB rejection of frequencies between 1 and 20 MHz. The board supply distribution system must ensure that the minimum voltage into the PLL ball is equal to or greater than 1.164 V. The current draw for the IC is 95 mA typical less than 140 mA maximum. The filter components are selected to achieve a corner frequency of 100 KHz. The series resistance keeps the Q of this resonant circuit safely below unity for all component variations. The total DC resistance of the resistor and the inductor must be equal to or less than 0.3 Ohms.

The bypass capacitor must be placed as close to the supply pins as possible. The series impedances to both the supply pin and the PCB analog ground plane must be an order of magnitude lower than the ESR and ESL specified for the capacitor. The S0/S1 PLLs have dedicated internal supplies, so the VSSPLLS0/S1 pins must be soldered directly to the analog ground plane of the PCB.

New Figure 8:

Figure 8. VCC1P2PLLS0, VCC1P2PLLS1 Low-Pass Filter



Affected Docs: Intel® 413808 and 413812 I/O Controllers Design Review Checklist

Status: Doc. See the Table , "Summary Table of Changes" on page 6.