White Paper
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Dynamic Power Gating Implementation

on Intel® Embedded Media and Graphics Driver (Intel® EMGD)

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Executive Summary

The Intel® Atom™ Processor E6xx series is designed with optimized power utilization to support a low-power embedded system usage model. To reduce overall power leakage and consumption, power gating capability is available on the Intel Atom Processor E6xx series. Power Gating allows modules that are not being used to be turned off.

Power gating is designed to reduce power leakage during system standby and idle modes. Most power leakage happens during transistor switching, so even during system idle, power leakage still happens. Power gating can be accomplished either by software or hardware methods.

Power gating turns off the power to various modules in the processor to reduce power leakage in the silicon.

Intel Atom Processor E6xx series features Hardware Video Encode, Hardware Video Decode, Graphic and Display modules in the integrated graphics adapter. Intel® Embedded and Media Graphic Drivers (Intel® EMGD) provides an embedded, focused graphic solution for the Intel Atom Processor E6xx.

The goal of power gating is to put the system into its lowest power state whenever possible. Intel EMGD implements the power gate option for Video Decode (VDX), Video Encode (VED), Graphics (GFX), and Display (DSP) modules. Intel EMGD dynamically power gates non-operational modules in runtime.

This paper focuses on dynamic power gating solution in Intel Atom Processor E6xx for Microsoft Windows* XP with Intel® EMGD.

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Background

This paper covers techniques to allow customers to enable or disable power gating. It is intended for:

- Customers who would like to write their own drivers with power gating, or
- Customers with headless systems (i.e., with no graphics output) who would like to power gate certain graphics modules.

The Intel® Atom™ processor enables embedded systems to incorporate rich media and graphics features that were synonymous with "PC-like" systems. Rich media allows the system to decode high definition video playback and run 3D applications. The challenge for embedded systems using the Intel Atom processor is to incorporate rich multimedia capabilities while maintaining a relatively low operating power.

One of the solutions to reduce the power consumption of the Intel Atom Processor E6xx series is to enable dynamic power gating for integrated graphics adapter. Intel Embedded Media and Graphics Driver (EMGD) will toggle the power gating state of the individual graphics components based on application that is being executed by the operating system. For example, if the system is not playing video, power gating to the hardware video decode is enabled. When the system starts to play video, EMGD turns off the power gate to the hardware video decode. Power gating is toggled during runtime, therefore the system does not need to be rebooted. The power gate switching is also transparent to the operating system and user, therefore the user does not need to run additional steps to enable power gating.

Note: This paper uses the term "power gating enable" to mean that power to the module is turned off.

There are four graphics modules on Atom E6xx that have power gating functionality: Video Decode Engine (VDX), Video Encode Engine (VED), Graphics Engine (GFX), and Display Controller (DSP), which are described in the next sections.

Video Decode Engine (VDX)

The Intel Atom Processor E6xx has a dedicated video decode engine that is used to accelerate decoding a video stream in hardware. VDX is a multi-standard high definition video decoder that is fully reinitialized on startup of the video subsystem. EMGD enabled hardware accelerated video decode that offers faster video decoding. VDX receives the elementary stream and decodes it to produce a final picture without requiring any processing from the CPU other than framebuffer management and housekeeping.

Video Encode Engine (VED)

Intel Atom Processor E6xx also has a dedicated hardware module for video encode that can accelerate encoding a video stream in hardware. VED is a compact multi-standard elementary stream level encoder. With the hardware accelerated video encoder as coprocessor, the CPU only needs to deal with higher level control code functions such as providing image to encode and process video elementary stream. It provides hardware acceleration to encode/compress the incoming raw video stream.

Graphics Engine (GFX)

The Intel Atom Processor E6xx uses an integrated 2D/3D graphics engine to accelerate 2D and 3D operations. It is designed to process pixel data, vertex data, video data, and general purpose processing concurrently.

Display Controller (DSP)

The display engine's main duty is to integrate various post-processed components in the graphics adapter and streams the data out to display devices (such as an LCD monitor). It supports two independent displays via LVDS and SDVO ports.

All the above modules are initialized during system boot up. Each of these modules consumes a certain amount of power, which has been addressed as future challenge. To reduce overall power consumption, it is highly desirable to add a technique to turn off modules that are not being used. This technique is called *power gating*.

Requirements

Power gating registers are available on the Intel Atom Processor E6xx for the different modules in the integrated graphics adapter. The system needs to be running using Intel Embedded Media and Graphics Driver for Windows XP (Intel® EMGD) version 1.6 or later.

Intel Embedded Media and Graphics Driver dynamically power gates the graphics adapter modules based on the application running in the system. The power gating operation in the driver is transparent to the user and operating system. The power gating is also done in runtime; therefore rebooting the system is not required.

Dynamic power gating is currently supported in Microsoft Windows* XP on the Intel Atom Processor E6xx only.

EMGD Configuration for Power Gating

By default, after driver installation, the dynamic power gating feature is enabled in Intel Embedded Media and Graphics Driver (version 1.6 or later). No configuration is necessary to enable this feature.

Disabling Dynamic Power Gating

For debugging and analysis, a configuration registry is made available to disable dynamic power gating. An additional line needs to be added in the iegd.inf file before installing the driver.

Add the line below under the [iegd_SoftwareDeviceSettings_tnc] section in iegd.inf file to disable dynamic power gate in Microsoft Windows XP.

```
HKR, ALL\1\General , PowerGate, %REG_DWORD%, 0
```

Note: This configuration is not available in EMGD Configuration EDitor (CED), nor is it a runtime configuration.

Power Gating Registers

Intel Atom Processor E6xx has four modules in the integrated graphics adapter:

- Video Decode (VDX)
- Video Encode (VED)
- Graphics Engine (GFX)
- Display Controller (DSP)

Power gating is added to the driver as part of the power management module. On Intel Atom E6xx Processor all the integrated graphics adapter components can be power gated. The power gate functionality is in addition to the power management capabilities already available in the integrated graphics adapter. Power management is defined as the capability to set the device into low power modes such as ACPI D1 or ACPI D3.

A device in the power gate-enabled state consumes less power than any of the power management states. P-unit does the power gating of modules on the system. EMGD needs to program the p-unit register to toggle the power gating state for each of the modules. It requires explicit commands (by register programming) to be sent to P-unit which power gates requested module. EMGD will also handle the interrupt unmasking during power gate.

Power Gate registers are located in Active Power Management (APM) block. P-unit is responsible for decoding accesses to these registers based on Base Address stored in APM Base Address Register (APM_BLK). APM_BLK has addressability of 32 bytes. All APM registers are assumed to be 4 bytes (DWORD) long. EMGD accesses these registers over the Message Bus Interface.

Except for the display controller, EMGD uses Active Power Gate Control Register (PWRGT_CNT) and the Active Power Gate Status Register (PWRGT_STS) in the APM block to control power gating. Power gating state to the display controller is done through the OSPM register.

The PWRGT_CNT, PWRGT_STS and OSPM registers are defined in the Intel Atom E6xx Processor EAS.

Active Power Gate Control Register (PWRGT_CNT)

PWRGT_CNT indicates configuration of voltage islands for various blocks that P-unit controls. This register is updated by Intel EMGD to request power up/power down of Graphics Island, Video Decode Island, Video Encode Island and Display Island. Each island is controlled by a 2-bit field – Bit 1 for power up request and Bit 0 for power down request. At reset/power up, all Islands come up enabled (00) indicates driver is not requesting power up/power down. EMGD sets the register fields via the Message Bus Interface. Hardware clears the bits when the request is serviced.

Active Power Gate Status (PWRGT_STS)

PWRGT_STS indicates the status of voltage islands of various blocks that P-unit controls. This register is updated by hardware. two bits are used to indicate power up/ power down status of each island: Graphics Island, Video Decode Island, Video Encode Island and Display Island. This register is used to determine the power gating state of the individual power island. EMGD polls this register to ensure that power gating has been successful after setting the PWRGT_CNT register. Accessing a memory mapped register of a power gated module causes a system hang.

Operating System Power Management (OSPM) Registers

Display Controller Island is powered up/powered down by EMGD via OSPM registers.

Active Power Management Sequence

When EMGD writes to Active Power Gate Control Registers (PWRGT_CNT) or OSPM registers, P-unit will monitor these control bits in its main execution loop and then jump to the active power management routine. P-unit has compile time delay variables that define how long we wait during the power up or power down sequence.

The first thing P-unit does is pull reset to a particular power domain, followed by a delay and then it enables firewalls. After the firewall is enabled, P-unit de-asserts `clk_en` for that domain. After fixed amount of delay, P-unit disables Power Gate enables to the Power domain.

P-unit waits a fixed amount of time and sets the status bits to indicate the selected power domain has been powered off. If the interrupt enable is set, P-unit sends out an interrupt to the driver to inform it that the power domain has been powered off.

To power up a particular power domain, EMGD writes to the Active power gate control register. P-unit works in reverse order, first bringing up the power domain by driving power gate enable followed by `clk_en`, firewall, and reset.

Power Gate Implementation on Microsoft Windows XP

This section explains the dynamic power gating implementation in EMGD for Microsoft Windows XP. The steps below can be used as a reference to implement dynamic power gating for other operating systems.

Power Gating During Boot Up

When the system powers on, the firmware (system BIOS or EFI) disables power gate for all integrated graphics adapter modules as default. When firmware hands over operation to the driver during boot up, the integrated graphics adapter modules are powered up. It is up to the driver to enable power gate for modules that are not required.

The driver first initializes all the modules during boot up, such as mapping the device registers, initializing the hardware and enabling interrupts for the module. After that, the driver enables power gate to the video decode and encode. The process of enabling power gate also saves the state of the hardware as well as unmasking interrupts used by the modules. The driver initializes the modules during boot up to reduce latency when toggling the power gating state.

By default, Microsoft Windows XP does not provide an application programming interface (API) for hardware video encode. Therefore, power gate to the hardware video encode will always be enabled in Microsoft Windows XP.

When a user plays a video, the driver detects the need for hardware video decode and disables the power gating to the hardware video decode. The latency for the power gate to take effect after setting the register is negligible.

Note: During Windows XP boot up, power gate to the hardware video decode and hardware video encode is enabled in the display driver callback function `DrvEnablePDEV`.

Power Gating During ACPI Power Management

EMGD power gates all integrated graphics adapter modules during ACPI power management. This may seem redundant but power gating the device results in lesser power consumption compared to ACPI power management states. Power gating the device is an additional step on the ACPI power management sequence and is transparent to the user. EMGD handles the register save and restore for the integrated display adapter.

Table 1: EMGD Power Gating Timing for Microsoft Windows* XP

Modules	When to Power Gate
VDX	Power gate enable during system boot up and when there is no active decode sessions. Power gate enable during S3 Power gate disable during D0
VED	Power gate enable during system boot up* Power gated enable during S3 and D0 NOTE: This feature is not currently supported, so EMGD does not handle power gating in the case where encode is active vs. non active. In the future when encode is officially supported, power gate module for encode needs to be implemented to handle this module. EMGD will enable power gate when there is no active encode session and disable it when encode is active.
GFX	Power gate enable during S3 Power gate disable during D0
DSP	Power gate enable during S3 Power gate disable during D0

Note: *No current support for video encode API on EMGD for Microsoft Windows XP.

Power Gating When Playing Video

There are three major software components to enable hardware accelerated video decode. They are:

- Video playback applications such as Microsoft Windows Media Player* or CyberLink* Power DVD
- Video Codec that provides filters to decode the video frame. Microsoft Windows XP uses DXVA framework for video decode support.
- Driver to provide hardware accelerated interface to the codec.

The video playback application uses the available codec to decode the video frame. The codec queries the driver to determine whether hardware accelerated video decode is available for particular the video playback.

EMGD disables power gate to the hardware video decode module when a call to create DXVA context is made from XP's DXVA runtime library. EMGD enables VDX power gating when a call to destroy DXVA context causing outstanding active contexts becomes zero.

In the case where multiple videos are playing, the driver will keep count of the number of video playbacks. After the last video has stopped playing, power gating will be enabled for the hardware video decode module.

Limitations

Dynamic power gating in EMGD is implemented in the Intel Atom Processor E6xx on Microsoft Windows XP only. This feature is available in all Intel Atom processor E6xx SKUs.

Power gating implementation in EMGD depends on the System BIOS revision, which allows the driver to control power gating.

Conclusion

Data collection on power consumption before and after power gating shows that there is ~10.37% power saved when power gating to the hardware video decode and hardware video encode is enabled while the system is running on idle.

In ACPI power management standby (S1) state, data showed that dynamic power gating saved ~4.35% of power consumption. Power gate to all integrated graphics adapter is enabled in ACPI power management.

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Acronyms

ACPI	Advanced Configuration and Power Interface
API	Application Programming Interface
CED	Configuration EDitor
DSP	Display Controller
DXVA	DirectX Video Acceleration
EMGD	Intel Embedded Media and Graphics Driver
GFX	Graphics engine
P-unit	Power management unit (controller that is in charge of power gating and clock gating the media block)
VDX	Hardware Video Decode Engine
VED	Hardware Video Encode Engine

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