AHCI 1.0

Errata 001

AHCI 1_0 Errata_001.doc

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1 PxCI bits may only be set when PxCMD.ST = ‘1’

1.1 Description of Technical Flaw

If a Register FIS, due to device power-up, is received before PxCMD.ST is set to ‘1’ the HBA may clear PxTFD.BSY and PxTFD.DRQ. This action causes the HBA to clear the PxCI bit that corresponds to the current command slot. If host software has set the PxCI bit for a command slot prior to setting PxCMD.ST to ‘1’, the HBA may inadvertently clear the PxCI bit as part of receiving the power-up Register FIS from the device.

To avoid accidentally clearing a PxCI bit, host software shall only set bits in the PxCI register when PxCMD.ST is set to ‘1’.

1.2 Description of Correction to Specification

3.3.14 Offset 138h: P0CI – Port 0 Command Issue

Bit	Type	Reset	Description
31:0	R/W1	0	**Commands Issued (CI):** This field is set by software to indicate to the HBA that a command has been built in system memory for a command slot and may be sent to the device. When the HBA receives a FIS which clears the BSY, DRQ, and ERR bits for the command, it clears the corresponding bit in this register for that command slot. Bits in this field shall only be set to ‘1’ by software when PxCMD.ST is set to ‘1’. This field is also cleared when PxCMD.ST is written from a ‘1’ to a ‘0’ by software.

2 PhyRdy Dropping Outside of a FIS

2.1 Description of Technical Flaw

If the PhyRdy signal drops outside of a FIS boundary intermittently, no command is affected by the condition. To avoid signaling error conditions to software that do not affect outstanding commands, this condition shall not be signaled to software via PxIS.IFS nor PxIS.INFS. If software is concerned about this condition, it may consult the PxSERR.DIAG.N bit.

2.2 Description of Correction to Specification

Within section 6.1.2, make the following changes to the "PhyRdy Dropping Unexpectedly" bullet:

- **PhyRdy Dropping Unexpectedly:** When this occurs, the HBA returns to idle. If the PhyRdy signal dropped during the middle of a command, the HBA may have to be restarted. If the PhyRdy signal dropped outside of a FIS, neither the PxIS.IFS nor the PxIS.INFS bits shall be set.

3 Errors that Cause Controller to Stop

3.1 Description of Technical Flaw

Section 6.1.2 of the AHCI specification defines which errors cause the controller to stop and require a re-start before continuing. The PxSERR.ERR register contains a statement that is inconsistent with the material in section 6.1.2 by causing the controller to stop for a more extensive list of errors. In order to fix this inconsistency, the statement in the PxSERR.ERR register is stricken to avoid stopping the controller more often than necessary.

3.2 Description of Correction to Specification

The PxSERR.ERR register in section 3.3.12 is modified as follows:

3.3.12 Offset 130h: P0SERR – Port 0 Serial ATA Error (SCR1: SError)

<table>
<tr><th>Bit</th><th>Type</th><th>Reset</th><th>Description</th></tr>
<tr><td>15:00</td><td>RWC</td><td>0000h</td><td>
Error (ERR): The ERR field contains error information for use by host software in determining the appropriate response to the error condition.

~~If one or more of bits 11:8 of this register are set, the controller shall stop the current transfer.~~

<table>
<tr><td>15:12</td><td>Reserved</td></tr>
<tr><td>11</td><td>Internal Error (E): The SATA controller failed due to a master or target abort when attempting to access system memory.</td></tr>
<tr><td>10</td><td>Protocol Error (P): A violation of the Serial ATA protocol was detected.</td></tr>
<tr><td>9</td><td>Persistent Communication or Data Integrity Error (C): A communication error that was not recovered occurred that is expected to be persistent. Persistent communications errors may arise from faulty interconnect with the device, from a device that has been removed or has failed, or a number of other causes.</td></tr>
<tr><td>8</td><td>Transient Data Integrity Error (T): A data integrity error occurred that was not recovered by the interface.</td></tr>
<tr><td>7:2</td><td>Reserved</td></tr>
<tr><td>1</td><td>Recovered Communications Error (M): Communications between the device and host was temporarily lost but was re-established. This can arise from a device temporarily being removed, from a temporary loss of Phy synchronization, or from other causes and may be derived from the PhyNRdy signal between the Phy and Link layers.</td></tr>
<tr><td>0</td><td>Recovered Data Integrity Error (I): A data integrity error occurred that was recovered by the interface through a retry operation or other recovery action.</td></tr>
</table>
</td></tr>
</table>

4 Software must wait for CLO='0' before setting PxCMD.ST

4.1 Description of Technical Flaw

Software must ensure that the operations associated with command list override are carried out before proceeding. The HBA may be in the middle of receiving a FIS at the time PxCMD.CLO is set, thus the operation may be slightly delayed. Software must ensure that PxCMD.CLO = '0' before proceeding.

4.2 Description of Correction to Specification

03	RW	0	**Command List Override (CLO):** Setting this bit to '1' causes PxTFD.STS.BSY and PxTFD.STS.DRQ to be cleared to '0'. This allows a software reset to be transmitted to the device regardless of whether the BSY and DRQ bits are still set in the PxTFD.STS register. The HBA sets this bit to '0' when PxTFD.STS.BSY and PxTFD.STS.DRQ have been cleared to '0'. A write to this register with a value of '0' shall have no effect. This bit shall only be set to '1' immediately prior to setting the PxCMD.ST bit to '1' from a previous value of '0'. Setting this bit to '1' at any other time is not supported and will result in indeterminate behavior. Software must wait for CLO to be cleared to '0' before setting PxCMD.ST to '1'.

5 Prefetch bit shall not be set for NCQ commands

5.1 Description of Technical Flaw

Section 5.4.2 on system software rules specifies that CH(z).P (prefetchable) shall not be set by software if the commands in the list are native queuing commands. In section 4.2.2, where the prefetchable bit is defined, this is not a requirement but only a recommendation. This errata fixes section 4.2.2 such that it is always a requirement for the prefetchable bit to be '0' when issuing native queuing commands.

5.2 Description of Correction to Specification

Modify the definition of Prefetchable in Figure 8 of section 4.2.2 as follows:

07	**Prefetchable (P):** This bit is only valid if the PRDTL field is non-zero. When set and PRDTL is non-zero, the HBA may prefetch PRDs in anticipation of performing a data transfer. System software ~~should~~ shall not set this bit when using native command queuing commands. **Note:** The HBA may prefetch the ATAPI command, PRD entries, and data regardless of the state of this bit. However, it is recommended that the HBA use this information from software to avoid prefetching needlessly.

6 IPMS may be set during Port Multiplier enumeration

6.1 Description of Technical Flaw

When enumerating devices on a Port Multiplier, it is possible to receive Register FISes from ports other than the currently selected port. When the PxSERR.DIAG.X bit is cleared for a particular Port Multiplier device port, that device will send a Register FIS to the host. At that point in time, the currently selected port will be the control port (port Fh). This results in the PxIS.IPMS bit becoming set.

Host software should only use PxIS.IPMS after enumeration on the Port Multiplier is complete in order to avoid counting expected operation during the enumeration process as errors.

6.2 Description of Correction to Specification

Modify the definition of Incorrect Port Multiplier Status in section 3.3.5 as follows:

23	RWC	0	**Incorrect Port Multiplier Status (IPMS):** Indicates that the HBA received a FIS from a device whose Port Multiplier field did not match what was expected. The IPMS bit may be set during enumeration of devices on a Port Multiplier due to the normal Port Multiplier enumeration process. It is recommended that IPMS only be used after enumeration is complete on the Port Multiplier.