AHCI 1.0

Erratum 004

AHCI 1_0 Erratum_004.doc

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1 State machine Command FIS retries do not work

1.1 Description of Technical Flaw

When transmission of a command FIS fails due to XRDY/XRDY collision, an R_ERR response, or some other failure condition, the command FIS should be retried at a later time. H:Idle is the state where command retries are started by taking arc 3 or arc 6 (depending on whether the command is a reset). Both arc 3 and arc 6 are overconstrained such that they will never be taken again after an initial attempt to transmit the command FIS. This errata removes some of the unnecessary constraints to ensure that command FISes are retried.

1.2 Description of Correction to Specification

Make the following changes in section 5.2.2.7:

5.2.2.7 H:Idle

H:Idle	HBA sets PxCMD.CR to '1'.		
	1. PxSSTS.DET != 3h	→	H:NotRunning
	2. PxCI != 0h and hbaIssueTag = 32	→	H:SelectCmd
	3. ~~PxCI.CI(hbaIssueTag) = '1' and~~ hbaCmdToIssue = '1' and CTBA(hbaIssueTag)[R] is set to '1' and hbaDmaXferCnt = '0' ~~and PxTFD.STS.BSY = '0' and PxTFD.STS.DRQ = '0'~~	→	CFIS:SyncEscape
	4. Data FIS received	→	DR:Entry
	5. Non-Data FIS received	→	NDR:Entry
	6. ~~PxCI.CI(hbaIssueTag) = '1' and~~ hbaCmdToIssue = '1' and hbaDmaXferCnt = '0' ~~and PxTFD.STS.BSY = '0' and PxTFD.STS.DRQ = '0'~~	→	CFIS:Xmit
	7. Else	→	H:Idle

The H:Idle state is entered when in normal operation to determine the next thing to do.

2 COMRESET Transmission Behavior

2.1 Description of Technical Flaw

Serial ATA defines three different behaviors for how COMRESET may be transmitted when PxSCTL.DET=1h. This errata clarifies that all behaviors are permitted to be used.

2.2 Description of Correction to Specification

Make the following changes to the DET field in the P0SCTL register in section 3.3.11:

03:00	RW	0h	**Device Detection Initialization (DET):** Controls the HBA's device detection and interface initialization. 0h No device detection or initialization action requested 1h Perform interface communication initialization sequence to establish communication. This is functionally equivalent to a hard reset and results in the interface being reset and communications reinitialized. While this field is 1h, COMRESET is ~~continuously~~ transmitted on the interface. Software should leave the DET field set to 1h for a minimum of 1 millisecond to ensure that a COMRESET is sent on the interface. 4h Disable the Serial ATA interface and put Phy in offline mode. All other values reserved This field may only be modified when P0CMD.ST is '0'. Changing this field while the P0CMD.ST bit is set to '1' results in undefined behavior. When P0CMD.ST is set to '1', this field should have a value of 0h. Note: It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

Make the following changes to state H:StartComm in section 5.2.2.10:

5.2.2.10 H:StartComm

H:StartComm	The HBA tells link layer to start communication, which involves sending COMRESET[2] to device. The HBA resets PxTFD to 7Fh, and sets hbaUpdateSig to '1'.

	1. PxSCTL.DET = 1h	→	H:StartComm
	2. Unconditional	→	H:NotRunning

NOTE:
1. Hardware polling to determine if a device is present is an implementation specific detail. A polling strategy is not specified in AHCI.
2. It is permissible to implement any of the Serial ATA defined behaviors for transmission of COMRESET when DET=1h.

The H:StartComm state is entered to start communication with the device by issuing a COMRESET.

3 H:Init updates to show undocumented actions

3.1 Description of Technical Flaw

On power-up or after an HBA reset, the H:Init state is entered. If PxCMD.SUD=1 (i.e. no staggered spin-up support), the HBA shall transmit a COMRESET to the device. H:Init will also cause PxTFD.STS and hbaUpdateSig to be updated as in the H:StartComm state. This errata updates the H:Init state to show those actions.

3.2 Description of Correction to Specification

Make the following changes to the H:Init state in section 5.2.2.1:

5.2.2.1 H:Init

H:Init	The HBA performs the following actions: 1. Resets state machine variables to their reset values, as specified in section 5.2.1 2. Resets GHC.AE, GHC.IE, and the IS register to their reset values. 3. Resets all port specific register fields except those fields marked as HwInit and the PxFB/PxFBU/PxCLB/PxCLBU registers. 4. HBA resets PxTFD.STS to 7Fh and sets hbaUpdateSig to '1'. 5. Transmits COMRESET to the device if PxCMD.SUD='1'.

	1. GHC.HR is set to '1'	→	H:Init
	2. Else	→	H:NotRunning
	NOTE: This state is entered asynchronously when GHC.HR is set to '1' from a previous value of '0'.		

The H:Init state is entered to initialize or reset a port. This state is only entered when the HBA powers up or an entire HBA reset is performed. If cold presence detect is supported as specified in PxCMD.CPD, the power to each port is off by default and remains off in this state until software enables power to the port.

4 Remove variable hbaFatal from state machine

4.1 Description of Technical Flaw

There is a state machine variable in section 5.2.1 called hbaFatal that is never used or referred to in the state machine. This errata removes the extraneous variable from section 5.2.1.

4.2 Description of Correction to Specification

Remove hbaFatal from the table in section 5.2.1:

~~**hbaFatal**~~	~~The hbaFatal variable is set whenever the HBA has detected a fatal error. When this variable is set, no new commands shall be issued. On power-up or reset of the HBA port, hbaFatal is cleared to 0.~~

5 hbaPioIBit needs to be set in state machine

5.1 Description of Technical Flaw

There state machine variable hbaPioIBit should be set to ‘1’ in the PIO:Entry field if the I bit is set to ‘1’ in the PIO Setup FIS. The state machine currently does not show this bit being set.

5.2 Description of Correction to Specification

Make the following changes in section 5.2.8.1:

5.2.8.1 PIO:Entry

PIO:Entry	HBA performs the following actions in order: 1. Copies the PIO Setup FIS to system memory at PxFB[PSFIS]. 2. Sets hbaPioXfer to ‘1’ 3. Sets hbaPioESts to E_Status field of the FIS 4. Sets hbaPioErr to Error field of the FIS 5. Sets hbaPioIBit to value of I bit in the FIS 6. Sets hbaDmaXferCnt to Transfer Count field of the FIS 7. Sets PxTFD.STS register to Status field of the FIS

1.	PxTFD.STS.ERR = ‘1’	→	ERR:Fatal
2.	D bit in the FIS is cleared to 0 and hbaXferAtapi is set to 0 (Data FIS should be transmitted)	→	DX:Entry
3.	D bit in the FIS is cleared to 0 and hbaXferAtapi is set to 1 (ATAPI command should be transmitted)	→	ATAPI:Entry
4.	Else (Data FIS will be received from device)	→	H:Idle

This state receives a PIO Setup FIS and updates the appropriate state based on the PIO Setup FIS.

6 Remove unnecessary arc in SDB:Entry

6.1 Description of Technical Flaw

Arc 3 in SDB:Entry is unnecessary since there is no definition in Serial ATA for sending a Set Device Bits FIS with the SActive field cleared to 0h and the Interrupt 'I' bit set to '0'. This errata removes the unnecessary arc.

6.2 Description of Correction to Specification

Make the following changes in section 5.2.12.1:

5.2.12.1 SDB:Entry

SDB:Entry	HBA performs the following actions: 1. Copies Set Device Bits FIS to system memory at offset PxFB[SDFIS] 2. Updates PxTFD.STS with non-reserved bits in Status field of FIS 3. Updates PxTFD.ERR with Error field of FIS 4. Clears bits in PxSACT that have corresponding bits set in the SActive field of the SDB FIS. Sets hbaSActive to value of SActive field in received FIS. 5. Clears hbaDmaXferCnt to '0'

1. PxTFD.STS.ERR = '1'	→	ERR:Fatal
2. I bit is set in the SDB FIS	→	SDB:SetIntr
~~3. hbaSActive = '0'~~	~~→~~	~~H:Idle~~
3. Else	→	AggrPM:Entry

7 Specify when hbaPrdIntr is set to ‘0’ to avoid error issues

7.1 Description of Technical Flaw

When an error occurs in a data transfer state, the hbaPrdIntr variable may remain set. This errata ensures that when another data transfer occurs, this variable is cleared to avoid inadvertently signaling an interrupt from a previous error condition.

7.2 Description of Correction to Specification

Make the following changes in section 5.2.9.1:

5.2.9.1 DX:Entry

DX:Entry	The HBA constructs a Data FIS for command list entry hbaDataTag. The PMP field of the Data FIS is set to the value in PxCLB[CH(hbaDataTag)][PMP]. The HBA fetches PRDs and data from locations specified in the hbaDataTag command list entry. The HBA clears hbaPrdIntr to ‘0’.		
1.	No data to transmit and hbaPioXfer = ‘1’	→	PIO:Update
2.	No data to transmit and hbaPioXfer = ‘0’	→	H:Idle
3.	Else	→	DX:Start

This state starts to construct a Data FIS to transmit to the device. This state is entered after a PIO Setup, DMA Activate, or DMA Setup FIS is received.

Make the following changes in section 5.2.10.1:

5.2.10.1 DR:Entry

DR:Entry	Clear hbaPrdIntr to ‘0’.		
1.	PMP field in the Data FIS does not equal hbaPMP	→	ERR:Non-fatal
2.	Else	→	DR:Receive

This state is entered when a Data FIS is received. This state checks to make sure the Port Multiplier Port field is valid.

8 Specify that Command FIS may be prefetched in H:FetchCmd

8.1 Description of Technical Flaw

The H:FetchCmd state selects the next command for transmission. A host should be allowed to fetch the command FIS from this state. This errata specifies that the host has that capability.

8.2 Description of Correction to Specification

Make the following changes in section 5.2.2.9:

5.2.2.9 H:FetchCmd

H:FetchCmd	The HBA performs the following actions in the order specified: 1. HBA fetches command header from PxCLB[CHz] 2. HBA sets hbaIssueTag = z 3. HBA sets PxCMD.CCS = z 4. HBA sets hbaCmdToIssue = '1' 5. HBA may prefetch the command FIS from memory		
	1. CTBA(hbaIssueTag).A (ATAPI) = '1' and CTBA(hbaIssueTag).P[1] (Prefetchable) = '1'	→	CFIS:PrefetchACMD
	2. CTBA(hbaIssueTag).P[1] (Prefetchable) = '1'	→	CFIS:PrefetchPRD
	3. Unconditional	→	H:Idle
	NOTE: 1. The P bit may be ignored by hardware although it is recommended to be observed to avoid prefetching unnecessary data. 2. An HBA implementation may choose to ignore arcs 1 and 2 if it is not desireable to prefetch after the command FIS is fetched from memory.		

The H:FetchCmd state is entered to fetch the command header for the next command to issue from memory. Note that when a command is selected to be transferred next, an implementation may choose to set PxTFD.STS.BSY. The requirement is that PxTFD.STS.BSY must be set before the command is issued to the device.

9 Prefetchable bit clarification

9.1 Description of Technical Flaw

The Prefetchable bit may be set for ATAPI commands that do not have an associated data transfer. In this case, the HBA may prefetch the ATAPI command itself. This errata clarifies that this behavior is allowed.

9.2 Description of Correction to Specification

Make the following change to the definition of Prefetchable in Figure 8 in section 4.2.2:

07	**Prefetchable (P):** This bit is only valid if the PRDTL field is non-zero or the ATAPI 'A' bit is set in the command header. When set and PRDTL is non-zero, the HBA may prefetch PRDs in anticipation of performing a data transfer. When set and the ATAPI 'A' bit is set in the command header, the HBA may prefetch the ATAPI command. System software shall not set this bit when using native command queuing commands or when using FIS-based switching with a Port Multiplier. **Note:** The HBA may prefetch the ATAPI command, PRD entries, and data regardless of the state of this bit. However, it is recommended that the HBA use this information from software to avoid prefetching needlessly.

10 Register FIS reception when PxCMD.ST=0

10.1 Description of Technical Flaw

When a Register FIS is received while PxCMD.ST=0, the HBA must ensure that the FIS is dropped if BSY or DRQ are cleared. This errata ensures that when PxCMD.ST=0, this condition is checked for.

10.2 Description of Correction to Specification

Make the following change to sections 5.2.2.3, 5.2.4.1 and 5.2.4.2:

5.2.2.3 H:RegFisUpdate

H:RegFisUpdate	HBA performs the following actions: ~~1. HBA accepts the FIS with a status of R_OK.~~ 1. HBA updates PxSIG with appropriate fields from D2H Register FIS as outlined in 3.3.9, and clears hbaUpdateSig to '0'.

1.	PxCMD.FRE = '1'	→	H:RegFisPostToMem
2.	Else	→	H:NotRunning

The H:RegFisUpdate state is entered to update the PxSIG registers when a D2H Register FIS is received while the PxCMD.ST bit is cleared to '0'.

5.2.4.1 NDR:Entry

NDR:Entry	Receive up to 64 bytes of FIS into internal FIFO.

1.	Reception error (FIS reception failed)	→	ERR:Non-fatal
2.	FIS is longer than 64 bytes	→	ERR:Fatal
~~3.~~	~~FIS Type is D2H Register and PxCMD.ST=0~~	~~→~~	~~H:RegFisUpdate~~
3.	Else	→	NDR:Accept

This state is entered when the HBA has received a non-Data FIS.

5.2.4.2 NDR:Accept

NDR:Accept	HBA accepts the FIS with a status of R_OK.

1.	FIS type is D2H Register FIS or PIO Setup FIS and (PxTFD.STS.BSY = '0' and PxTFD.STS.DRQ = '0')	→	H:Idle
2.	FIS Type is D2H Register and PxCMD.ST=0	→	H:RegFisUpdate
3.	FIS Type is D2H Register	→	RegFIS:Entry
4.	FIS Type is Set Device Bits	→	SDB:Entry
5.	FIS Type is DMA Activate	→	DX:Entry
6.	FIS Type is DMA Setup	→	DmaSet:Entry
7.	FIS Type is BIST Activate and far-end loopback is enabled in the FIS	→	BIST:FarEndLoopback
8.	FIS Type is BIST Activate and far-end loopback is not enabled in the FIS	→	BIST:TestOngoing
9.	FIS Type is PIO Setup	→	PIO:Entry
10.	Else (FIS type is unknown)	→	UFIS:Entry

In this state, the non-Data FIS received has been verified to be valid. If the FIS is a Register FIS or PIO Setup FIS and PxTFD.STS.BSY and PxTFD.STS.DRQ are cleared, the HBA accepts the FIS with R_OK but does not perform any updates based on it; see section 6.1.2.

11 ATAPI command transfer state clarification

11.1 Description of Technical Flaw

An ATAPI command is transferred to the device as part of a PIO Setup operation. After transferring the ATAPI command successfully, the host should update the taskfile registers based on the PIO Setup FIS received that requested transmission of the ATAPI command. This errata ensures that the update occurs rather than proceeding directly to H:Idle.

11.2 Description of Correction to Specification

Make the following change to section 5.2.6.1:

5.2.6.1 ATAPI:Entry

ATAPI:Entry	The HBA constructs a Data FIS with the minimum of hbaDmaXferCnt bytes or 16 bytes of data fetched from CTBA(hbaDataTag)[ACMD] as necessary. The PMP field of the Data FIS is set to the value in PxCLB[CH(hbaDataTag)][PMP]. HBA transmits the Data FIS to the device. HBA clears hbaXferAtapi to 0.

1.	Error occurred on transmission	→	ERR:Fatal
2.	Else (transmission successful, R_OK received)	→	~~H:Idle~~ PIO:Update

This state is entered to transmit the ATAPI command to the device.