AHCI 1.0

Erratum 005

AHCI 1_0 Errata_005.doc

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1 Global interrupt enable behavior

1.1 Description of Technical Issue

The behavior when GHC.IE is cleared to '0' does not clearly state that Interrupt Status bits in the IS register are set regardless of this bit. Additionally, the behavior mis-states that "the HBA may generate interrupts" when GHC.IE = '0'.

1.2 Description of Correction to Specification

Make the following changes in section 10.6.1.1:

10.6.1.1 First Tier (IS Register)

The first tier is identified by the GHC and IS registers.

GHC.IE register enables interrupts for the entire HBA. This is the 'master enable. Until this bit is set, the HBA shall not generate any interrupts. When it is cleared, the HBA may ~~generate interrupts~~ set Interrupt Status bits in the IS register but no interrupt is asserted on the controller. This bit is only a mask, and does not affect the setting of any of the interrupt status bits in any of the ports. These bits are set regardless of whether or not interrupts are enabled.

The 32-bit IS register reports whether a port has an interrupt pending. This is a bit-mapped register indicating a bit for each of the 32 ports allowed in AHCI. Each bit location can be thought of as reporting a '1' if the virtual "interrupt line" for that port is indicating it wishes to generate an interrupt. That is, if a port has one or more interrupt status bit set, and the enables for those status bits are set, then this bit shall as set. The bits in this register are read/write clear. It is set by the level of the virtual interrupt line being a set, and cleared by a write of '1' from the software.

This register allows software to perform a quick glance of the HBA to see which ports are reporting interrupts. By being read/write clear, it also allows for the implementation of message signaled interrupts.