AHCI 1.3

Errata 008 Draft

AHCI 1_3 Errata_008.doc

Please send comments to James Boyd
james.a.boyd@intel.com

Table of Contents

1 Correction of State Machine NDR:Accept

1.1 Description of Technical Issue

NDR:Accept never returns to FB:Idle if FIS Based Switching is enabled. It only returns to P:Idle. The state machine should be updated to correct this.

1.2 Description of Correction to Specification

Update section 5.3.5.3 as indicated in red

5.3.5.3 NDR:Accept

NDR:Accept	HBA accepts the FIS with a status of R_OK.		
	1. FIS type is D2H Register FIS or PIO Setup FIS and (pBsy[pPmpCur] = '0' and pDrq[pPmpCur] = '0') and PxFBS.EN = '1'	→	FB:Idle
	2. FIS type is D2H Register FIS or PIO Setup FIS and (pBsy[pPmpCur] = '0' and pDrq[pPmpCur] = '0')	→	P:Idle
	3. FIS Type is D2H Register and PxCMD.ST=0	→	P:RegFisUpdate
	4. PxCMD.FRE=0	→	P:NotRunning[1]
	5. FIS Type is D2H Register	→	RegFIS:Entry
	6. FIS Type is Set Device Bits and 'N' bit is set to '1' and PxFBS.EN = '0' and PM Port field does not match the port currently being accessed.	→	SDB:Notification
	7. FIS Type is Set Device Bits	→	SDB:Entry
	8. FIS Type is DMA Activate	→	DX:Entry
	9. FIS Type is DMA Setup	→	DmaSet:Entry
	10. FIS Type is BIST Activate and far-end loopback is enabled in the FIS	→	BIST:FarEndLoopback[2]
	11. FIS Type is BIST Activate and far-end loopback is not enabled in the FIS	→	BIST:TestOngoing[2]
	12. FIS Type is PIO Setup	→	PIO:Entry
	13. Else (FIS type is unknown)	→	UFIS:Entry
	NOTE: 1. Software shall set PxCMD.FRE to '1' prior to setting PxCMD.ST to '1'. Setting PxCMD.ST to '1' when PxCMD.FRE is cleared to '0' will cause indeterminate results. 2. Handling of the BIST Activate FIS when using FIS-based switching is vendor specific. It is recommended that BIST procedures with a connected Port Multiplier be performed with command-based switching. Note that BIST support is not standardized for Port Multipliers.		

2 Correction of Typo in 5.3.1 Variables

2.1 Description of Technical Issue

pDrq[16] incorrectly states that pBsy[0] is reflected in PxTFD.STS when PxFBS.EN = '0'. It should be pDrq[0] that is reflected in PxTFD.STS.

2.2 Description of Correction to Specification

Update section 5.3.1 as indicated in red

5.3.1 Variables

pUpdateSig This variable is set whenever the HBA needs to update the PxSIG register due to a hard or software reset. It is cleared when the D2H Register FIS which updates the signature is received. On power-up or reset of the HBA port, pUpdateSig is set to '1'.

pBsy[16] The pBsy array contains the value of the BSY bit in the Shadow Status register for each device. On power-up or reset of the HBA port, the pBsy array is cleared to 0h. In the case where FIS-based switching is not enabled (PxFBS.EN = '0'), only pBsy[0] is valid and is directly reflected in PxTFD.STS.BSY.

pDevIssue This variable is set to the device to issue the next command to. On power-up or reset of the HBA port, pDevIssue is cleared to 0h.

pDrq[16] The pDrq array contains the value of the DRQ bit in the Shadow Status register for each device. On power-up or reset of the HBA port, the pDrq array is cleared to 0h. In the case where FIS-based switching is not enabled (PxFBS.EN = '0'), only pDrq[0] is valid and is directly reflected in PxTFD.STS.DRQ.

pPmpCur The value of the Port Multiplier Port (PMP) field in the last FIS received. On power-up or reset of the HBA port, pPmpCur is set to 0h.

pIssueSlot[16] The pIssueSlot variable contains the command slot location of the last command issued to each of the devices. On power-up or reset of the HBA port, all pIssueSlot variables are set to 32. When FIS-based switching is not enabled, only the first value in the array is used.

pDataSlot[16] Each pDataSlot element contains the command slot location of the command to transfer data for the corresponding device. On power-up or reset of the HBA port, all pDataSlot variables are cleared to 0h. When FIS-based switching is not enabled, only the first value in the array is used.

pPMP The pPMP variable contains the value in the PMP field of the command table of the last command FIS transferred to the device. On power-up or reset of the HBA port, pPMP is cleared to 0h.

pXferAtapi[16] The pXferAtapi variable is set to '1' when a command is issued that had the A bit set for a particular transfer. The pXferAtapi variable is cleared to '0' when a Data FIS is transferred to the device that contains the ATAPI command from the command list. On power-up or reset of the HBA port, pXferAtapi is cleared to '0'.

pPioXfer[16] The pPioXfer[x] variable is set to '1' when a PIO Setup FIS is received with a PMP value of x. This variable is used after a data transfer occurs in order to update the Status register appropriately. When FIS-based switching is not enabled, only the first value in the array is used.

pPioESts[16] The pPioESts variable is set to the E_Status field of the PIO Setup FIS to be stored until the data for the DRQ block is transferred. On power-up or reset of the HBA port, all pPioESts variables are cleared to '0'. When FIS-based switching is not enabled, only the first value in the array is used.

pPioErr[16] The pPioErr variable is set to the Error field of the PIO Setup FIS to be stored until the data for the DRQ block is transferred. On power-up or reset of the HBA port, all pPioErr variables are cleared to '0'. When FIS-based switching is not enabled, only the first value in the array is used.

pPioIbit[16] The pPioIbit variable is set to the I bit of the PIO Setup FIS to be stored until the data for the DRQ block is transferred. On power-up or reset of the HBA port, all pPioIbit variables are cleared to '0'. When FIS-based switching is not enabled, only the first value in the array is used.

pDmaXferCnt[16] The pDmaXferCnt variable is set to the DMA transfer count for a particular DMA transfer. The DMA transfer may consist of multiple Data FISes. The pDmaXferCnt variable is decremented by the size of a Data FIS on each successful reception of a Data FIS. On power-up or reset of the HBA port, pDmaXferCnt is cleared to 0h. An pDmaXferCnt = 0h signals that there was no DMA Setup FIS or PIO Setup FIS corresponding to the data transfer and that the transfer lengths should be constructed based on the PRD table entries only. When FIS-based switching is not enabled, only the first value in the array is used.

pCmdToIssue This variable is set whenever the currently fetched command still needs to be transmitted to the device. It is used by the state machine to ensure the command is actually transmitted to the device, especially after a command transmission failure. On power-up or reset of the HBA port, pCmdToIssue is cleared to 0h.

pPrdIntr[16] This pPrdIntr[x] variable is set whenever the HBA completes a PRD in either the data transmission or data reception states for the device with a PMP value of x. It is used to generate a PRD interrupt at the end of a successful data FIS. On power-up or reset of the HBA port, all pPrdIntr variables are cleared to 0h. When FIS-based switching is not enabled, only the first value in the array is used.

pSActive This variable is set to the value of the SActive field in a received Set Device Bits FIS. On power-up or reset of the HBA port, pSActive is cleared to 0h.

pSlotLoc This variable is used to track the command slot location the HBA will issue a command from next if one is available in that slot for issue. On power-up or reset of the HBA port, pSlotLoc is cleared to 0h.

3 Correction of pDmaXferCnt

3.1 Description of Technical Issue

pDmaXfer is an array and the state machines should reflect which members are updated according to the current state the HBA is in.

3.2 Description of Correction to Specification

Update sections as indicated in red

5.3.2.11 P:Idle

P:Idle	HBA sets PxCMD.CR to '1'.		
1.	PxSSTS.DET != 3h	→	P:NotRunning
2.	PxCI != 0h and pIssueSlot[0] = 32	→	P:SelectCmd
3.	pCmdToIssue = '1' and CTBA(pIssueSlot[0])[R] is set to '1' and pDmaXferCnt[0] = '0'	→	CFIS:SyncEscape
4.	Data FIS received	→	DR:Entry
5.	Non-Data FIS received	→	NDR:Entry
6.	pCmdToIssue = '1' and pDmaXferCnt[0] = '0'	→	CFIS:Xmit
7.	Link layer has negotiated to low power state based on device power management request	→	PM:LowPower
8.	PxCMD.ICC written	→	PM:ICC
9.	Else	→	P:Idle

5.3.3.1 FB:Idle

FB:Idle	HBA sets PxCMD.CR to '1'.		
1.	PxSSTS.DET != 3h	→	P:NotRunning
2.	pCmdToIssue = '0' and there is a device that a command pending in the command list can be issued to[1]	→	FB:SelectDevice
3.	Data FIS received	→	DR:Entry
4.	Non-Data FIS received	→	NDR:Entry
5.	pCmdToIssue = '1' and pDmaXferCnt[pDevIssue] = '0'	→	CFIS:Xmit
6.	Link layer has negotiated to low power state based on device power management request	→	PM:LowPower
7.	PxCMD.ICC written	→	PM:ICC
8.	Else	→	FB:Idle
NOTE: 1. The HBA shall only issue a command to a device if the corresponding pDmXferCnt, pBsy, and pDrq variables are zero.			

5.3.7.1 ATAPI:Entry

ATAPI:Entry	The HBA constructs a Data FIS with the minimum of pDmaXferCnt[pPmpCur] bytes or 16 bytes of data fetched from CTBA(pDataSlot[pPmpCur])[ACMD] as necessary. The PMP field of the Data FIS is set to the value in PxCLB[CH(pDataSlot[pPmpCur])][PMP]. HBA transmits the Data FIS to the device. HBA clears pXferAtapi[pPmpCur] to '0'.		
1.	Error occurred on transmission	→	ERR:Fatal
2.	Else (transmission successful, R_OK received)	→	PIO:Update

5.3.10.2 DX:Transmit

DX:Transmit	HBA transmits the Data FIS to the device. Continue to fetch PRDs and data as necessary to complete the Data FIS until pDmaXferCnt[pPmpCur] bytes or 8KB has been transferred. For each PRD entry processed, if R_OK is received for all the FISes containing the data for that PRD entry and the 'I' bit is set in the PRD entry, then set pPrdIntr[pPmpCur] to '1'.

1. SYNC escape received for Data FIS	→	ERR:SyncEscapeRecv
2. R_ERR received for FIS and PxFBS.EN = '1'	→	ERR:Non-fatal
3. Transmission failed	→	ERR:Fatal
4. pDmaXferCnt[pPmpCur] bytes have been transferred, end of PRD table reached, or maximum Data FIS length of 8KB has been transferred.	→	DX:UpdateByteCount

NOTE:
1. If the DMAT primitive is received from the device, it is recommended that this primitive be ignored and data transmission be continued.

4 Correction of PIO:Entry

4.1 Description of Technical Issue

PIO: Entry may transition to the ERR: FatalTaskFile state if PxTFD.STS.ERR = '1'. However, upon entering PIO: Entry the HBA is not updating this value with the value in pPioErr[pPmpCur].

4.2 Description of Correction to Specification

Update sections as indicated in red

5.3.9.1 PIO: Entry

PIO:Entry	HBA performs the following actions in order: 1. Copies the PIO Setup FIS to system memory at PxFB[(pPmpCur * 256) + PSFIS]. 2. Sets pPioXfer[pPmpCur] to '1' 3. Sets pPioESts[pPmpCur] to E_Status field of the FIS 4. Sets pPioErr[pPmpCur] to Error field of the FIS 5. Sets pPioIbit[pPmpCur] to value of I bit in the FIS 6. Sets pDmaXferCnt[pPmpCur] to Transfer Count field of the FIS 7. Sets PxTFD.STS register to Status field of the FIS 8. Updates PxTFD.STS.ERR with pPioErr[pPmpCur] 9. Sets pBsy[pPmpCur] and pDrq[pPmpCur] according to Status field of the FIS.

1. PxTFD.STS.ERR = '1'	→	ERR:FatalTaskfile
2. D bit in the FIS is cleared to '0' and pXferAtapi[pPmpCur] is cleared to '0' (Data FIS should be transmitted)	→	DX:Entry
3. D bit in the FIS is cleared to '0' and pXferAtapi[pPmpCur] is set to '1' (ATAPI command should be transmitted)	→	ATAPI:Entry
4. PxFBS.EN = '1' (Data FIS will be received from device)	→	FB:Idle
5. Else (Data FIS will be received from device)	→	P:Idle

5 Removal of State Machine jump

5.1 Description of Technical Issue

ERR:Fatal state shows a transition to FB:SingleDeviceError when PxFBS.EN=1, but according to Figure18: HBA Error Handling Behavior, there is no Fatal type error/transition that would also be SingleDeviceError. The Transition to FB:SingleDeviceError transition has been removed.

5.2 Description of Correction to Specification

Update sections as indicated in red

ERR:Fatal	HBA performs the following actions in the order specified: 1. Sets PxIS.IFS to '1'.		
	~~1. PxFBS.EN = '1' and error was a single device error~~	→	~~FB:SingleDeviceError~~
	1. Unconditional	→	ERR:WaitForClear

6 Correction of State Machine typos

6.1 Description of Technical Issue

There are several state machine names that are incorrect (typos).

6.2 Description of Correction to Specification

Update sections as indicated in red

5.3.16.3 ERR:SyncEscapeFbNd

ERR:SyncEscapeFbNd	HBA performs the following actions in the order specified: 1. Sets PxIS.INFS to '1'.		
	1. Unconditional	→	FB:SingleDeviceError

5.3.16.4 ERR:FatalTaskfile

ERR:FatalTaskfile	HBA performs the following actions in the order specified: 1. Sets PxIS.TFES to '1'.		
	1. PxFBS.EN = '1'	→	FB:SingleDeviceError
	2. Else	→	ERR:WaitForClear

5.3.10.4 DX:PrdSetIntr

DX:PrdSetIntr	HBA sets PxIS.DPS to '1'. HBA clears pPrdIntr[pPmpCur] to '0'.		
	1. PxIE.DPE = '1'	→	DX:PrdSetIS
	2. pPioXfer[pPmpCur] = '1'	→	PIO:Update
	3. PxFBS.EN = '1'	→	FB:Idle
	4. Else	→	P:idle