

AHCI 1.3

Errata 006 Draft



AHCI 1_3 Errata_006.doc

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1 Clarification of Interface Speed Support

1.1 Description of Technical Issue

Section 10.5 describes the various combinations of CAP.ISS and PxSCTL.SPD, and the resulting Maximum Speed Negotiated. This table needs to be updated to include the various combinations for HBAs supporting 6 Gbps.

1.2 Description of Correction to Specification

Update section 10.5 as indicated in red

10.5 Interface Speed Support

The HBA indicates the maximum speed it can support via the CAP.ISS register. Software can further limit the speed of a port by manipulating each port's PxSCTL.SPD field to a lower value. If software writes a value that is greater than the value in CAP.ISS, the actual speed negotiated will be limited by CAP.ISS, as shown in the following table:

CAP.ISS	PxSCTL.SPD	Maximum Speed Negotiated
1h	0h	1.5 Gbps
1h	1h	1.5 Gbps
1h	2h	1.5 Gbps
1h	3h	1.5 Gbps
2h	0h	3 Gbps
2h	1h	1.5 Gbps
2h	2h	3 Gbps
2h	3h	3 Gbps
3h	0h	6.0 Gbps
3h	1h	1.5 Gbps
3h	2h	3 Gbps
3h	3h	6 Gbps

If PxSCTL.SPD is set to a non-zero value when system software loads, platform BIOS (or expansion ROM) decided that the current port required speed limitation. Speed limitation may be set by the platform BIOS to avoid an inordinate number of errors on a port; e.g. a laptop swapbay connector that goes through several intermediate connectors may need to speed limitation for robust operation. If PxSCTL.SPD is set to a non-zero value when system software loads, system software should preserve this setting, including across power management state transitions. It is recommended that platform BIOS (or expansion ROM) not specify a speed limitation unless it is necessary for robust operation. If system software encounters errors and speed could be limited further, system software is allowed to restrict the speed negotiated to a slower rate.