AHCI 1.2

Errata 002

AHCI 1_2 Errata_002.doc

Please send comments to Amber Huffman
amber.huffman@intel.com

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1 BOHC register and HBA reset

1.1 Description of Technical Issue

It is unclear whether HBA reset affects the values in the BIOS/OS Handoff Control and Status register. This erratum clarifies that HBA reset does not affect this register.

1.2 Description of Correction to Specification

Modify section 3.1.11 as shown below:

3.1.11 Offset 28h: BOHC – BIOS/OS Handoff Control and Status

This register controls various global actions of the HBA. This register is not affected by an HBA reset.

Bit	Type	Reset	Description
31:05	*RO*	*0h*	*Reserved*
04	RW	0	**BIOS Busy (BB):** This bit is used by the BIOS to indicate that it is busy cleaning up for ownership change.
03	RWC	0	**OS Ownership Change (OOC):** This bit is set to '1' when the OOS bit transitions from '0' to '1'. This bit is cleared by writing a '1' to it. Writing '0' has no effect on it.
02	RW	0	**SMI on OS Ownership Change Enable (SOOE):** This bit, when set to '1', enables an SMI when the OOC bit has been set to '1'.
01	RW	0	**OS Owned Semaphore (OOS):** The system software sets this bit to request ownership of the HBA controller. Ownership is obtained when this bit reads '1' and the BOS bit reads '0'. ~~This bit is not affected by an HBA reset.~~
00	RW	0	**BIOS Owned Semaphore (BOS):** The BIOS sets this bit to establish ownership of the HBA controller. BIOS will clear this bit in response to a request for ownership of the HBA by system software via OOS. ~~This bit is not affected by an HBA reset.~~

2 AHCI Enable clarification

2.1 Description of Technical Issue

It is not clear whether software is allowed to clear the AHCI Enable bit and set the HBA Reset bit at the same time. This erratum clarifies that clearing the AHCI Enable bit shall not be combined with other operations.

2.2 Description of Correction to Specification

The definition of the AHCI Enable bit in the Global HBA Control register in section 3.1.2 shall be modified as shown below:

Bit	Type	Reset	Description
31	RW/RO	Impl Spec	**AHCI Enable (AE):** When set, indicates that communication to the HBA shall be via AHCI mechanisms. This can be used by an HBA that supports both legacy mechanisms (such as SFF-8038i) and AHCI to know when the HBA is running under an AHCI driver. When set, software shall only communicate with the HBA using AHCI. When cleared, software shall only communicate with the HBA using legacy mechanisms. When cleared FISes are not posted to memory and no commands are sent via AHCI mechanisms. Software shall set this bit to '1' before accessing other AHCI registers. When software clears this bit to '0' from a previous value of '1', it shall set no other bit in the GHC register as part of that operation (i.e., clearing the AE bit requires software to write 00000000h to the register). The implementation of this bit is dependent upon the value of the CAP.SAM bit. If CAP.SAM is '0', then GHC.AE shall be read-write and shall have a reset value of '0'. If CAP.SAM is '1', then AE shall be read-only and shall have a reset value of '1'.