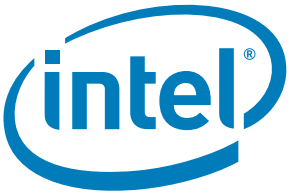
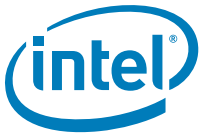


Measuring TX_TCLK Jitter on Intel® Ethernet Controllers

September 2009

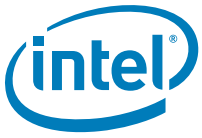
321222-002
Revision 1.1



Revision History

Date	Revision	Description
September 2009	1.1	Fixed two typos.
December 2008	1.0	Initial public release.

Note: This page intentionally left blank.



1.0 Introduction

Self certification for IEEE standards can be a difficult undertaking. Companies such as Tektronix and Agilent offer test suites to provide early compliance reports for Ethernet designs. One test, outlined in Clause 40.6.1.2.5 of IEEE 802.3, requires that designers inspect an internal clock (TX_TCLK) for jitter content. This application note describes an alternative method for measuring this clock for Intel Ethernet controllers that do not make this clock externally available for inspection.

2.0 Scope

This document outlines why Intel does not make the TX_TCLK available on most of its Ethernet controllers, where to find documentation regarding an approved alternative method of measuring the jitter of this clock, and provide the reader with the location of further IEEE 802.3 testing documentation available from the University of New Hampshire.

3.0 Why is TX_TCLK Not Available on Certain Intel Ethernet Controllers?

TX_TCLK is often not found externally available on Intel Ethernet controllers.

Since this is the internal clock that is used to drive MDI signals, it is by design a clean clock. When designers take this clean, internal clock and try and expose it to the rest of the world, there is the additional cost and complexity associated with adding a low-jitter driver for the test clock. Also, bringing this clock out to the ball or lead of a package can also change the characteristic of the original clock as well as the measured clock.

4.0 What is the Alternative Method for Measuring TX_TCLK?

See Appendix 40.B Transmitter Timing Jitter, No TX_TCLK Access: ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL40_PMA/PMA_Test_Suite_v2.5.pdf.

The appendix indirectly measures the jitter of the 125 MHz clock. The premise is the TM2/TM3 jitter signal is driven by TX_TCLK. Note that TX_TCLK jitter is included in the measurement. If the TM2/TM3 signal jitter passes, which includes TX_TCLK jitter as well as any jitter that is added by the Analog Front End (AFE) or coupled in from the system, then the TX_TCLK indirectly passes the jitter test.

5.0 Is TX_CLK the Same Clock as TX_TCLK?

No, TX_CLK is different clock in a different clock domain than TX_TCLK. TX_CLK is the clock found between the Media Access Controller (MAC) and the PHY used over the GMII interface. TX_TCLK is the 125 MHz clock that drives the internal transmitters, BI_DA, BI_DB, BI_DC, and BI_DD, that generate the five-level PAM signal that drives the signal out to the magnetics.

6.0 Where Can I Find More Information?

The University of New Hampshire maintains the Interoperability Labs (IOL) for the gigabit Ethernet standard.