14 nm Process Technology: Opening New Horizons

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Logic Technology Development

SPCS010
Agenda

• Introduction
• 2\textsuperscript{nd} Generation Tri-gate Transistor
• Logic Area Scaling
• Cost per Transistor
• Product Benefits
• SoC Feature Menu
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Intel Technology Roadmap

22 nm  |  14 nm  |  10 nm  |  7 nm

Manufacturing  |  Development  |  Research
Intel Technology Roadmap

>500 million chips using 22 nm Tri-gate (FinFET) transistors shipped to date
Industry's first 14 nm technology is now in volume manufacturing.
Intel Scaling Trend

Scaled transistors provide:

- Higher performance
- Lower power
- Lower cost per transistor

Moore’s Law continues!
How Small is 14 nm?
How Small is 14 nm?

- Mark: 1.66 m
- Fly: 7 mm
- Mite: 300 um
- Blood Cell: 7 um
- Virus: 100 nm
- Silicon Atom: 0.24 nm

<table>
<thead>
<tr>
<th>meter</th>
<th>millimeter</th>
<th>micrometer</th>
<th>nanometer</th>
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How Small is 14 nm?

Mark 1.66 m
Fly 7 mm
Mite 300 um
Blood Cell 7 um
Virus 100 nm
Silicon Atom 0.24 nm

14 nm Process

meter | millimeter | micrometer | nanometer
14 nm Tri-gate Transistor Fins

8 nm Fin Width

42 nm Fin Pitch

Si Substrate

Gate
14 nm Intel® Core™ M Processor

1.3 billion transistors

82 mm² die size

Industry’s first 14 nm processor now in volume production
Agenda

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**Minimum Feature Size**

<table>
<thead>
<tr>
<th></th>
<th>22 nm</th>
<th>14 nm</th>
<th>Scale</th>
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<td>Transistor Gate Pitch</td>
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<td>70</td>
<td>.78x</td>
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<tr>
<td>Interconnect Pitch</td>
<td>80</td>
<td>52</td>
<td>.65x</td>
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*Intel has developed a true 14 nm technology with good dimensional scaling*
Transistor Fin Optimization

![Diagram showing comparison of 22 nm and 14 nm processes with Si Substrate, 60 nm pitch, and 34 nm height.](image)
Transistor Fin Optimization

Tighter fin pitch for improved density
Transistor Fin Optimization

Taller and thinner fins for improved performance
Transistor Fin Optimization

*Reduced number of fins for improved density and lower capacitance*
Transistor Fin Optimization

1st generation Tri-gate

22 nm Process

14 nm Process

2nd generation Tri-gate
Transistor Fin Optimization

22 nm Process

1\textsuperscript{st} generation Tri-gate

14 nm Process

2\textsuperscript{nd} generation Tri-gate
Interconnects

22 nm Process

14 nm Process

80 nm minimum pitch

52 nm (0.65x) minimum pitch

52 nm interconnect pitch provides better than normal interconnect scaling
SRAM Memory Cells

22 nm Process

.108 um²
(Used on CPU products)

14 nm Process

.0588 um²
(0.54x)

14 nm design rules + 2nd generation Tri-gate provides industry-leading SRAM density
Agenda

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Transistor Gate Pitch Scaling

Gate pitch scaling ~0.8x for good balance of performance, density and low leakage
Metal Interconnect Pitch Scaling

14 nm interconnects scaling faster than normal for improved density
Logic Area Scaling Metric

\[ \text{Logic area scaling} \approx \text{gate pitch} \times \text{metal pitch} \]
Logic Area Scaling

Logic area continues to scale ~0.53x per generation
Logic Area Scaling

In the past, others tended to have better density, but came later than Intel

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p.129
Logic Area Scaling

Intel continues scaling at 14 nm while other pause to develop FinFETs

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14
20nm: H. Shang (IBM alliance), 2012 VLSI, p. 129
Logic Area Scaling

Intel is shipping its 2nd generation FINFETs before others ship their 1st generation

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14
Intel 14 nm is both denser and earlier than what others call “16nm” or “14nm”

45nm: K-I. Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
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Cost per Transistor

$ / mm^2
(normalized)

Wafer cost is increasing due to added masking steps
Cost per Transistor

$ / \text{mm}^2$
(normalized)

\begin{itemize}
  \item 130 nm
  \item 90 nm
  \item 65 nm
  \item 45 nm
  \item 32 nm
  \item 22 nm
  \item 14 nm
  \item 10 nm
\end{itemize}

\begin{itemize}
  \item 1
  \item 0.1
  \item 0.01
\end{itemize}

14 nm achieves better than normal area scaling
Cost per Transistor

*Intel 14 nm continues to deliver lower cost per transistor*
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Transistor Performance vs. Leakage

14 nm transistors provide improved performance and leakage...
Transistor Performance vs. Leakage

Higher Transistor Performance (switching speed)

... to support a wide range of products
New technology generations provide improved performance and/or reduced power, but the key benefit is improved performance per watt.
Product Benefits

14 nm Intel® Core™ M processor delivers >2x improvement in performance per watt

- 2nd generation Tri-gate transistors with improved low voltage performance and lower leakage
- Better than normal area scaling
- Extensive design-process co-optimization
- Microarchitecture optimizations for active power reduction

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Intel® Core™ M Processor

- **Real Performance**
  - Up to 50% faster CPU performance vs. previous generation\(^1\)
  - Up to 40% faster graphics performance vs. previous generation\(^2\)
- **Longer Battery Life**
  - Power sipping 4.5W processor
- **No Fan**
  - 60% reduction in thermal design point (TDP)\(^3\)
- **A Conflict-Free Choice**
  - Intel® Core™ M is a “conflict-free” product\(^4\)

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\(^1\) Source: Intel: Based on SPECfp_rate_base2006. System configurations in backup.

\(^2\) Source: Intel: 3DMark® IceStorm Unlimited v 1.2. System configurations in backup.

\(^3\) Intel has reduced our thermal design power from 18W in 2010 to 11.5W in 2013 to 4.5W with the new Intel Core M processor. That’s a 4X reduction over 4 years and a 60% reduction year over year.

\(^4\) “Conflict-free” means “DRC conflict-free”, which is defined by the Securities and Exchange Commission rules to mean products that do not contain conflict minerals (tin, tantalum, tungsten and/or gold) that directly or indirectly finance or benefit armed groups in the Democratic Republic of the Congo (DRC) or adjoining countries.

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Intel® Core™ M Processor Die Area Scaling

- Dense 14 nm process features provide good die area scaling compared to 22 nm processor
- 0.51x feature-neutral die area scaling
- 0.63x die area scaling with added design features

82 mm²
14 nm Manufacturing

- Process yield is now in healthy range with further improvements coming
- 14 nm process and lead product are qualified and in volume production
- 14 nm manufacturing fabs are located in:
  - Oregon (2014)
  - Arizona (2014)
  - Ireland (2015)
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• SoC Feature Menu
Multiple transistor options to support products from high performance to low power
Interconnect Stacks

- Low Cost
- Dense
- High Performance

Multiple interconnect stack offerings to optimize for cost, density, or performance
SoC Device Features

14 nm technology provides a full menu of SoC device options
Summary

• Intel has developed a true 14 nm technology with industry-leading performance, power, density and cost per transistor

• The 14 nm technology and the lead processor product are now qualified and in volume production

• A full menu of SoC transistor and interconnect features are provided

• Intel’s 14 nm technology will be used to manufacture a wide range of products, from high performance to low power

Moore’s Law continues!
Intel Technology Roadmap

22 nm 14 nm 10 nm 7 nm

Manufacturing Development Research

10 nm coming next, with further improvements in performance, power and cost
Additional Sources of Information

• A PDF of this presentation is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.

• “Leading at the Edge of Moore’s Law with Intel Custom Foundry” SPCS011, 4:00-5:00pm, room 2004

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Systems Configurations
