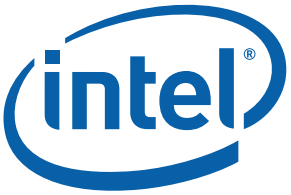

Intel® Scalable Memory Interconnect 2 438-Pin Edge Connector

Specification

February 2014

Reference Number: 329989-001

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Revision History

Document Number	Revision Number	Description	Date
329989	001	• Initial Release	February 2014

§

1 Introduction

1.1 Purpose and Scope

This document provides specifications for Intel® Scalable Memory Interconnect 2 (Intel® SMI2) connector that would interface with a riser card supporting two Intel® SMI2 channels with transfer rate as high as 3.2 Gbps. It contains mechanical, electrical and environmental requirements of the connector accepting 2.36 mm (0.093”) nominal thickness add-in card. Intent of this document is to enable connector, system designers and manufacturers to build, qualify, and use the Intel® SMI2 connectors as the standard interface between the Intel® SMI2 riser card and the Intel server platform.

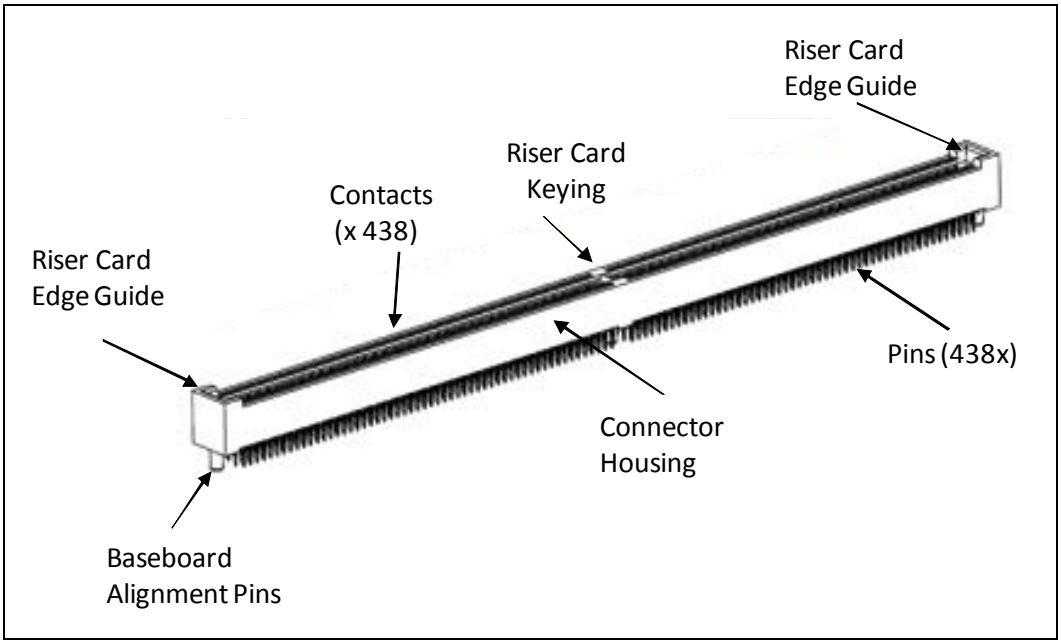
In this document the terms ‘*connector*’ refers to the Intel® SMI2 438-Pin edge connector, the term ‘baseboard’ is used in reference to the motherboard (MB) or system board the connector is mounted onto, and the term ‘riser card’ is used in reference to the ‘Intel® SMI2 Riser Card’, whose gold finger edge is inserted vertically into the connector.

1.2 Connector Overview

Intel® SMI2 connector is a single piece 438 pin vertical press fit connector with 0.7 mm staggered contact pitch. It is defined for applications where a riser card vertically enters the connector, perpendicular to the system board with 2.36 mm (0.093”) nominal thickness.

The connector requires the use of mechanical alignment/insertion/retention/extraction mechanisms (see Appendix E, “Riser Card Installation” for more details).

Figure 1-1. Intel® Scalable Memory Interconnect 2 438-Pin Edge Connector



1.3 Terms and Definitions

Term	Description
Baseboard	Also known as motherboard (MB) or system board
dB	Given in dB-volts, that is, 20log10(V2/V1)
DUT	Device Under Test
EIA	Electronic Industry Alliance
EOL	End of Life
Gap	Space between two traces
Gbps	Gigabytes per second
Intel® SMI2	Intel® Scalable Memory Interconnect 2
LLCR	Low Level Contact Resistance
Module	Refers to Intel® SMI2 Riser card also known as riser card
PCB	Printed Circuit Board
Riser Card	Refers to Intel SMI2 riser card also known as module
SMA	SubMiniature version A
Staggered Contact Pitch	Refers to diagonal position of contacts with respect to one another.
System Board	Printed circuit board on which the Intel® SMI2 438-Pin edge connector is mounted
TDR	Time Domain Reflectometry
TDT	Time Domain Transmission
Tie Bar	A physical part near the gold finger to allow electroplating of Ni and Au after etching
TRL	Through, Reflection, and Line
TW	Trace Width
Vertical Connector	A connector that accepts a module perpendicular to the system board
VNA	Vector Network Analyzer

1.4 References

Seven Year life cycle testing is applied to mechanical requirement and environmental requirement per EIA 364-1000. This specification requires references to other documents.

- EIA-364-1000: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Business Office Applications. www.eia.org
- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-13:Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23C - Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets

- EIA-364-29: Contact Retention Test Procedure for Electrical Connectors
- EIA 364-70B - Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- Agilent Application Note, “Agilent Network Analysis Applying the 8510 TRL Calibration for Non-Coaxial Measurements”, Product Note 8510-8A

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2 Signal Description and Pin Assignment

This section describes the signals included in the Intel® SMI2 connector, as well as the connector and the riser card pin assignments.

2.1 Signal Description

Intel SMI2 connector signal groups, names, and number of assigned pins are provided in Table 2-1.

Table 2-1. Intel® Scalable Memory Interconnect 2 (Intel® SMI2) Connector and Module Signal Descriptions

Signal Group	Signal Name	Pin Count	Notes
Command Clock	VCK0p	1	Cmd clock, Use to be VMSE0_CLK_P
	VCK0n	1	Cmd clock, Use to be VMSE0_CLK_N
	VCK1p	1	Cmd clock, Use to be VMSE1_CLK_P
	VCK1n	1	Cmd clock, Use to be VMSE1_CLK_N
Reference Clock	RefCLK0p	1	Reference clock of 100MHz
	RefCLK0n	1	Reference clock of 100MHz
	RefCLK1p	1	Reference clock of 100MHz
	RefCLK1n	1	Reference clock of 100MHz
CMD signal	VMSE0_CMD#[0-16]	17	Command bits on Channel 0
	VMSE1_CMD#[0-16]	17	Command bits on Channel 1
DQ signal	VMSE0_DQ[0-63]	64	Data bits on Channel 0
	VMSE1_DQ[0-63]	64	Data bits on Channel 1
Check Bits	VMSE0_ECC[0-7]	8	Check bits/ error correction bits on Channel 0
	VMSE1_ECC[0-7]	8	Check bits/ error correction bits on Channel 1
Strobe signals	VMSE0_DQSp[0-8]	9	
	VMSE0_DQSn[0-8]	9	
	VMSE1_DQSp[0-8]	9	
	VMSE1_DQSn[0-8]	9	
CMD_error signal	VMSE0_ERR_N	1	Error signal for Channel 0, active low
	VMSE1_ERR_N	1	Error signal for Channel 1, active low
Signal Ref Pin	VSS	214	
Misc	RFU	0	
Total		438	

2.2 Pin Assignments

Intel SMI2 Connectors pin assignment is listed in Table 2-2. Figure 3-3 and Figure 3-8 respectively illustrate pin 1 location on the connector and the riser card.

Table 2-2. Intel SMI2 Connector and Modules Pin Assignment (Sheet 1 of 5)

Pin Number	Signal			Signal		Pin Number
1	VMSE0_DQ[59]			VMSE0_DQ[51]		220
2		VSS			VSS	221
3	VMSE0_DQ[62]			VMSE0_DQ[54]		222
4		VSS			VSS	223
5	VMSE0_DQ[58]			VMSE0_DQ[50]		224
6		VSS			VSS	225
7	VMSE0_DQ[63]			VMSE0_DQ[55]		226
8		VSS			VSS	227
9	VMSE0_DQSp[7]			VMSE0_DQSn[6]		228
10		VMSE0_DQSn[7]			VMSE0_DQSp[6]	229
11	VSS			VSS		230
12		VMSE0_DQ[57]			VMSE0_DQ[49]	231
13	VSS			VSS		232
14		VMSE0_DQ[60]			VMSE0_DQ[52]	233
15	VSS			VSS		234
16		VMSE0_DQ[61]			VMSE0_DQ[53]	235
17	VSS			VSS		236
18		VMSE0_DQ[56]			VMSE0_DQ[48]	237
19	VSS			VSS		238
20		VMSE0_DQ[43]			VMSE0_DQ[35]	239
21	VSS			VSS		240
22		VMSE0_DQ[46]			VMSE0_DQ[39]	241
23	VSS			VSS		242
24		VMSE0_DQ[42]			VMSE0_DQ[34]	243
25	VSS			VSS		244
26		VMSE0_DQ[47]			VMSE0_DQ[38]	245
27	VSS			VSS		246
28		VMSE0_DQSp[5]			VMSE0_DQSp[4]	247
29	VMSE0_DQSn[5]			VMSE0_DQSn[4]		248
30		VSS			VSS	249
31	VMSE0_DQ[41]			VMSE0_DQ[33]		250
32		VSS			VSS	251
33	VMSE0_DQ[44]			VMSE0_DQ[36]		252
34		VSS			VSS	253
35	VMSE0_DQ[45]			VMSE0_DQ[37]		254
36		VSS			VSS	255
37	VMSE0_DQ[40]			VMSE0_DQ[32]		256
38		VSS			VSS	257
39	VSS			VMSE0_ECC[3]		258
40		VMSE0_CMD#[0]			VSS	259
41	VSS			VMSE0_ECC[6]		260
42		VMSE0_CMD#[1]			VSS	261
43	VSS			VMSE0_ECC[2]		262
44		VMSE0_CMD#[2]			VSS	263
45	VSS			VMSE0_ECC[7]		264
46		VMSE0_CMD#[3]			VSS	265
47	VSS			VMSE0_DQSn[8]		266
48		VMSE0_CMD#[4]			VMSE0_DQSp[8]	267
49	VSS			VSS		268
50		VMSE0_CMD#[5]			VMSE0_ECC[1]	269
51	VSS			VSS		270
52		VMSE0_CMD#[6]			VMSE0_ECC[4]	271
53	VSS			VSS		272
54		VMSE0_CMD#[7]			VMSE0_ECC[5]	273

Table 2-2. Intel SMI2 Connector and Modules Pin Assignment (Sheet 2 of 5)

Pin Number	Signal			Signal		Pin Number
55	VSS			VSS		274
56		VCK0p			VMSE0_ECC[0]	275
57	VCK0n			VSS		276
58		VSS			VSS	277
59	VMSE0_CMD#[8]					278
60		VSS				279
61	VMSE0_CMD#[9]			VSS		280
62		VSS			VSS	281
63	VMSE0_CMD#[11]			VMSE0_CMD#[10]		282
64		VSS			VSS	283
65	VMSE0_CMD#[13]			VMSE0_CMD#[12]		284
66		VSS			VSS	285
67	VMSE0_CMD#[15]			VMSE0_CMD#[14]		286
68		VSS			VSS	287
69	VMSE0_Err_N			VMSE0_CMD#[16]		288
70		VSS			VSS	289
71	VSS			VSS		290
72		VMSE0_DQ[27]			VMSE0_DQ[19]	291
73	VSS			VSS		292
74		VMSE0_DQ[30]			VMSE0_DQ[22]	293
75	VSS			VSS		294
76		VMSE0_DQ[26]			VMSE0_DQ[18]	295
77	VSS			VSS		296
78		VMSE0_DQ[31]			VMSE0_DQ[23]	297
79	VSS			VSS		298
80		VMSE0_DQSp[3]			VMSE0_DQSp[2]	299
81	VMSE0_DQSn[3]			VMSE0_DQSn[2]		300
82		VSS			VSS	301
83	VMSE0_DQ[25]			VMSE0_DQ[17]		302
84		VSS			VSS	303
85	VMSE0_DQ[28]			VMSE0_DQ[20]		304
86		VSS			VSS	305
87	VMSE0_DQ[29]			VMSE0_DQ[21]		306
88		VSS			VSS	307
89	VMSE0_DQ[24]			VMSE0_DQ[16]		308
90		VSS			VSS	309
91	VMSE0_DQ[11]			VMSE0_DQ[3]		310
92		VSS			VSS	311
93	VMSE0_DQ[14]			VMSE0_DQ[6]		312
94		VSS			VSS	313
95	VMSE0_DQ[10]			VMSE0_DQ[2]		314
96		VSS			VSS	315
97	VMSE0_DQ[15]			VMSE0_DQ[7]		316
98		VSS			VSS	317
99	VMSE0_DQSp[1]			VMSE0_DQSn[0]		318
100		VMSE0_DQSn[1]			VMSE0_DQSp[0]	319
101	VSS			VSS		320
102		VMSE0_DQ[9]			VMSE0_DQ[1]	321
103	VSS			VSS		322
104		VMSE0_DQ[12]			VMSE0_DQ[4]	323
105	VSS			VSS		324
106		VMSE0_DQ[13]			VMSE0_DQ[5]	325
107	VSS			VSS		326
108		VMSE0_DQ[8]			VMSE0_DQ[0]	327
109	VSS			VSS		328

Table 2-2. Intel SMI2 Connector and Modules Pin Assignment (Sheet 3 of 5)

Pin Number	Signal			Signal		Pin Number
110		VSS			VSS	329
111	VMSE1_DQ[59]			VMSE1_DQ[51]		330
112		VSS			VSS	331
113	VMSE1_DQ[62]			VMSE1_DQ[54]		332
114		VSS			VSS	333
115	VMSE1_DQ[58]			VMSE1_DQ[50]		334
116		VSS			VSS	335
117	VMSE1_DQ[63]			VMSE1_DQ[55]		336
Key						
118		VSS			VSS	337
119	VMSE1_DQSp[7]			VMSE1_DQSn[6]		338
120		VMSE1_DQSn[7]			VMSE1_DQSp[6]	339
121	VSS			VSS		340
122		VMSE1_DQ[57]			VMSE1_DQ[49]	341
123	VSS			VSS		342
124		VMSE1_DQ[60]			VMSE1_DQ[52]	343
125	VSS			VSS		344
126		VMSE1_DQ[61]			VMSE1_DQ[53]	345
127	VSS			VSS		346
128		VMSE1_DQ[56]			VMSE1_DQ[48]	347
129	VSS			VSS		348
130		VMSE1_DQ[43]			VMSE1_DQ[35]	349
131	VSS			VSS		350
132		VMSE1_DQ[46]			VMSE1_DQ[38]	351
133	VSS			VSS		352
134		VMSE1_DQ[42]			VMSE1_DQ[34]	353
135	VSS			VSS		354
136		VMSE1_DQ[47]			VMSE1_DQ[39]	355
137	VSS			VSS		356
138		VMSE1_DQSp[5]			VMSE1_DQSp[4]	357
139	VMSE1_DQSn[5]			VMSE1_DQSn[4]		358
140		VSS			VSS	359
141	VMSE1_DQ[41]			VMSE1_DQ[33]		360
142		VSS			VSS	361
143	VMSE1_DQ[44]			VMSE1_DQ[36]		362
144		VSS			VSS	363
145	VMSE1_DQ[45]			VMSE1_DQ[37]		364
146		VSS			VSS	365
147	VMSE1_DQ[40]			VMSE1_DQ[32]		366
148		VSS			VSS	367
149	VSS			VMSE1_ECC[3]		368
150		VMSE1_CMD#[0]			VSS	369
151	VSS			VMSE1_ECC[6]		370
152		VMSE1_CMD#[1]			VSS	371
153	VSS			VMSE1_ECC[2]		372
154		VMSE1_CMD#[2]			VSS	373
155	VSS			VMSE1_ECC[7]		374
156		VMSE1_CMD#[3]			VSS	375
157	VSS			VMSE1_DQSn[8]		376
158		VMSE1_CMD#[4]			VMSE1_DQSp[8]	377
159	VSS			VSS		378
160		VMSE1_CMD#[5]			VMSE1_ECC[1]	379
161	VSS			VSS		380
162		VMSE1_CMD#[6]			VMSE1_ECC[4]	381
163	VSS			VSS		382

Table 2-2. Intel SMI2 Connector and Modules Pin Assignment (Sheet 4 of 5)

Pin Number	Signal			Signal		Pin Number
164		VMSE1_CMD#[7]			VMSE1_ECC[5]	383
165	VSS			VSS		384
166		VCK1p			VMSE1_ECC[0]	385
167	VCK1n			VSS		386
168		VSS			VSS	387
169	VMSE1_CMD#[8]					388
170		VSS				389
171	VMSE1_CMD#[9]			VSS		390
172		VSS			VSS	391
173	VMSE1_CMD#[11]			VMSE1_CMD#[10]		392
174		VSS			VSS	393
175	VMSE1_CMD#[13]			VMSE1_CMD#[12]		394
176		VSS			VSS	395
177	VMSE1_CMD#[15]			VMSE1_CMD#[14]		396
178		VSS			VSS	397
179	VMSE1_Err_N			VMSE1_CMD#[16]		398
180		VSS			VSS	399
181	VSS			VSS		400
182		VMSE1_DQ[27]			VMSE1_DQ[19]	401
183	VSS			VSS		402
184		VMSE1_DQ[30]			VMSE1_DQ[22]	403
185	VSS			VSS		404
186		VMSE1_DQ[26]			VMSE1_DQ[18]	405
187	VSS			VSS		406
188		VMSE1_DQ[31]			VMSE1_DQ[23]	407
189	VSS			VSS		408
190		VMSE1_DQSp[3]			VMSE1_DQSp[2]	409
191	VMSE1_DQSn[3]			VMSE1_DQSn[2]		410
192		VSS			VSS	411
193	VMSE1_DQ[25]			VMSE1_DQ[17]		412
194		VSS			VSS	413
195	VMSE1_DQ[28]			VMSE1_DQ[20]		414
196		VSS			VSS	415
197	VMSE1_DQ[29]			VMSE1_DQ[21]		416
198		VSS			VSS	417
199	VMSE1_DQ[24]			VMSE1_DQ[16]		418
200		VSS			VSS	419
201	VMSE1_DQ[11]			VMSE1_DQ[3]		420
202		VSS			VSS	421
203	VMSE1_DQ[14]			VMSE1_DQ[6]		422
204		VSS			VSS	423
205	VMSE1_DQ[10]			VMSE1_DQ[2]		424
206		VSS			VSS	425
207	VMSE1_DQ[15]			VMSE1_DQ[7]		426
208		VSS			VSS	427
209	VMSE1_DQSp[1]			VMSE1_DQSn[0]		428
210		VMSE1_DQSn[1]			VMSE1_DQSp[0]	429
211	VSS			VSS		430
212		VMSE1_DQ[9]			VMSE1_DQ[1]	431
213	VSS			VSS		432
214		VMSE1_DQ[12]			VMSE1_DQ[4]	433
215	VSS			VSS		434
216		VMSE1_DQ[13]			VMSE1_DQ[5]	435

Table 2-2. Intel SMI2 Connector and Modules Pin Assignment (Sheet 5 of 5)

Pin Number	Signal			Signal		Pin Number
217	VSS			VSS		436
218		VMSE1_DQ[8]			VMSE1_DQ[0]	437
219	VSS			VSS		438

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3 Connector Interface Definitions

This section defines the Intel® SMI2 connector and riser card mechanical interfaces to ensure form, fit and function.

3.1 Design Essentials

The following notes apply for all drawings in this section:

1. Dimensions and tolerances conform to ASME Y14.5-2009.
2. All dimensions are in millimeters (mm) unless identified otherwise.
3. All dimensions tolerances are ±0.15 unless specified otherwise.
4. Critical dimensions and tolerances are identified with the symbol Ⓒ, and are required to meet Cpk ≥1.00.

3.2 Intel® SMI2 Connector Dimensions

Intel SMI2 connector is defined mainly for applications that require a vertical entry of a riser card into the connector. Figure 3-1 illustrates a 3-dimensional image of such a connector. Figure 3-2 shows connector outline.

Figure 3-1. Intel® SMI2 Connector and Riser Card

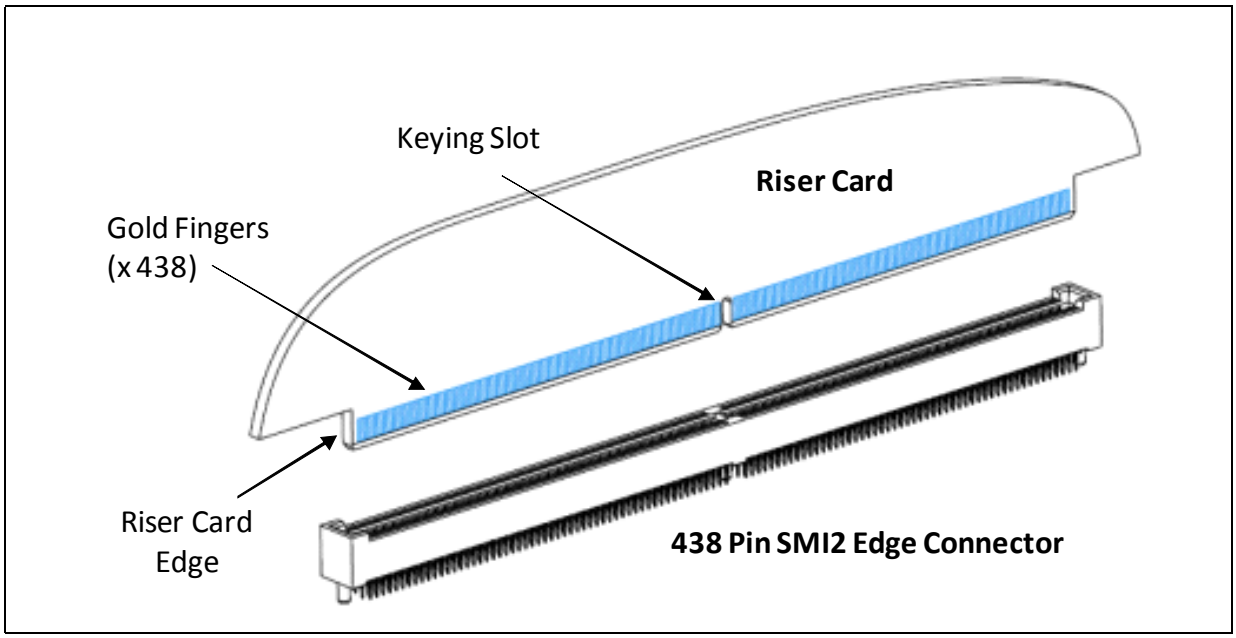
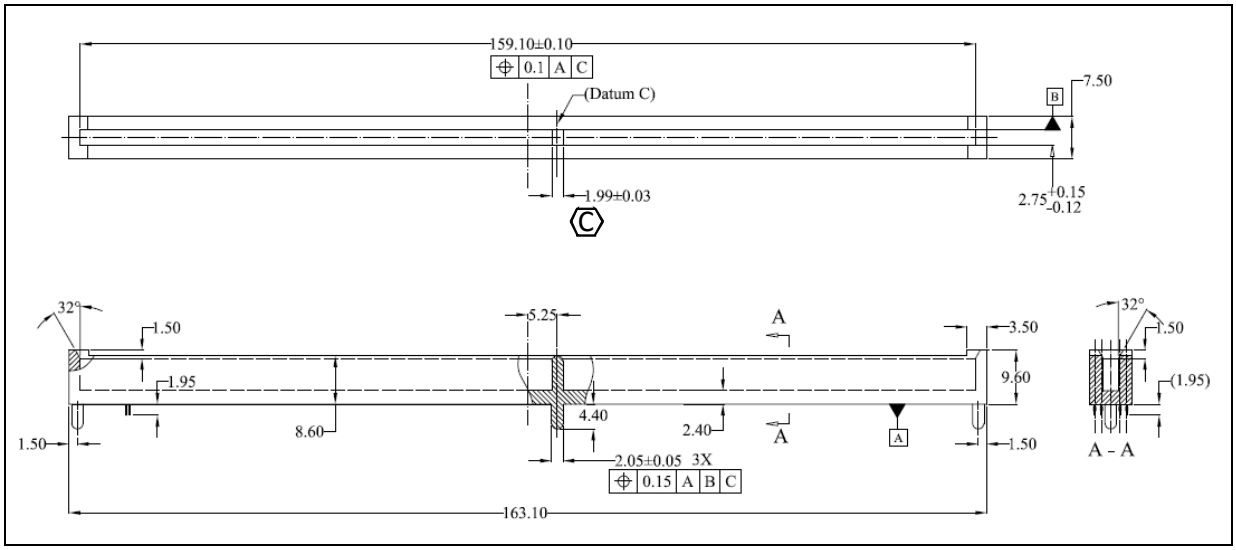


Figure 3-2. Intel SMI2 Connector Dimensions



The outer locus of the Intel® SMI2 connector contact at interface with riser card should be ≤ 0.38 mm to prevent any shorts during the riser card insertion into the connector. Contact outer locus at the riser card interface is the maximum zone where contact could locate, which is controlled by housing cavity size, pin size and housing cavity position tolerance referenced to datum key.

3.3 Intel SMI2 Connector - Baseboard Footprint

As a press-fit type connector, Intel SMI2 connector relies on a mechanical interference fit between the pin on the connector and the plated through hole (PTH) in the board to ensure electrical connection between the connector and board is made. Board finish can effect both mechanical and electrical performance of the connector.

Connector footprint and board holes details are shown in Figure 3-3. Additional board space is needed for the connector installation and removal tool. The recommended baseboard keep-out zones are shown in Figure 3-4 and Figure 3-5.

Figure 3-3. Intel SMI2 Connector Footprint (Top View)

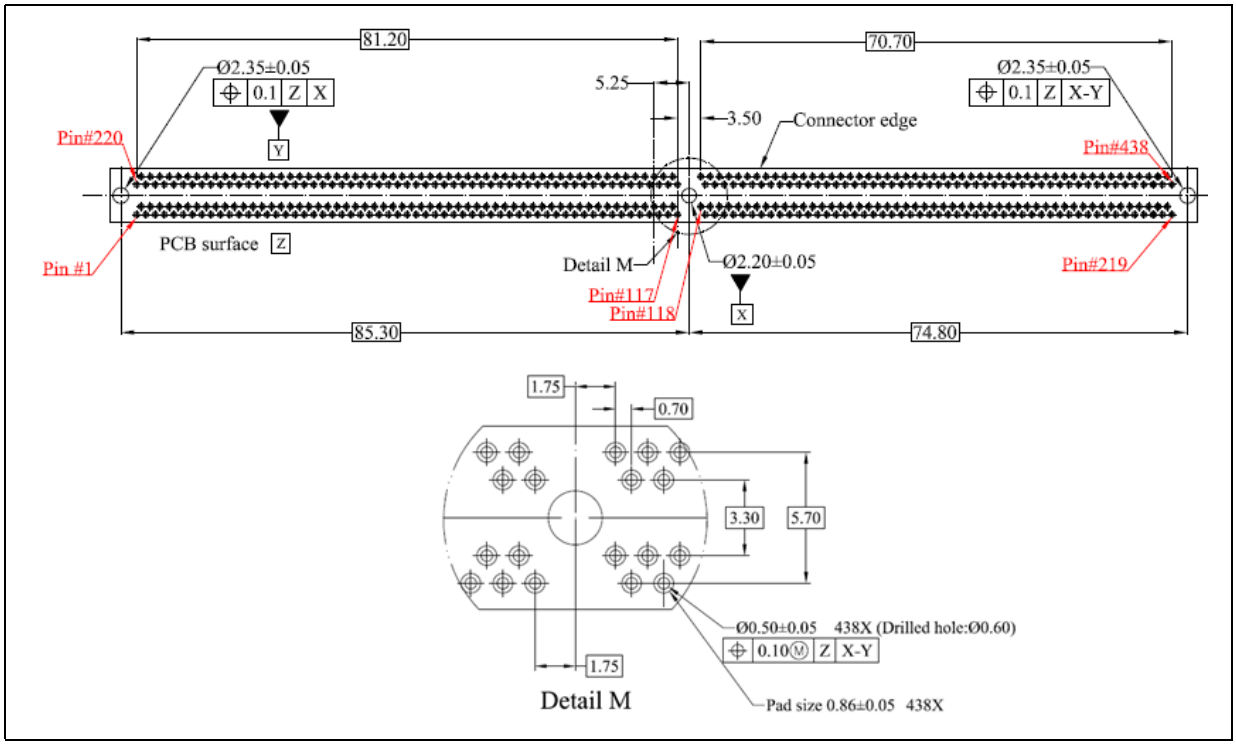


Figure 3-4. System Board Keep-out Zone for Assembly

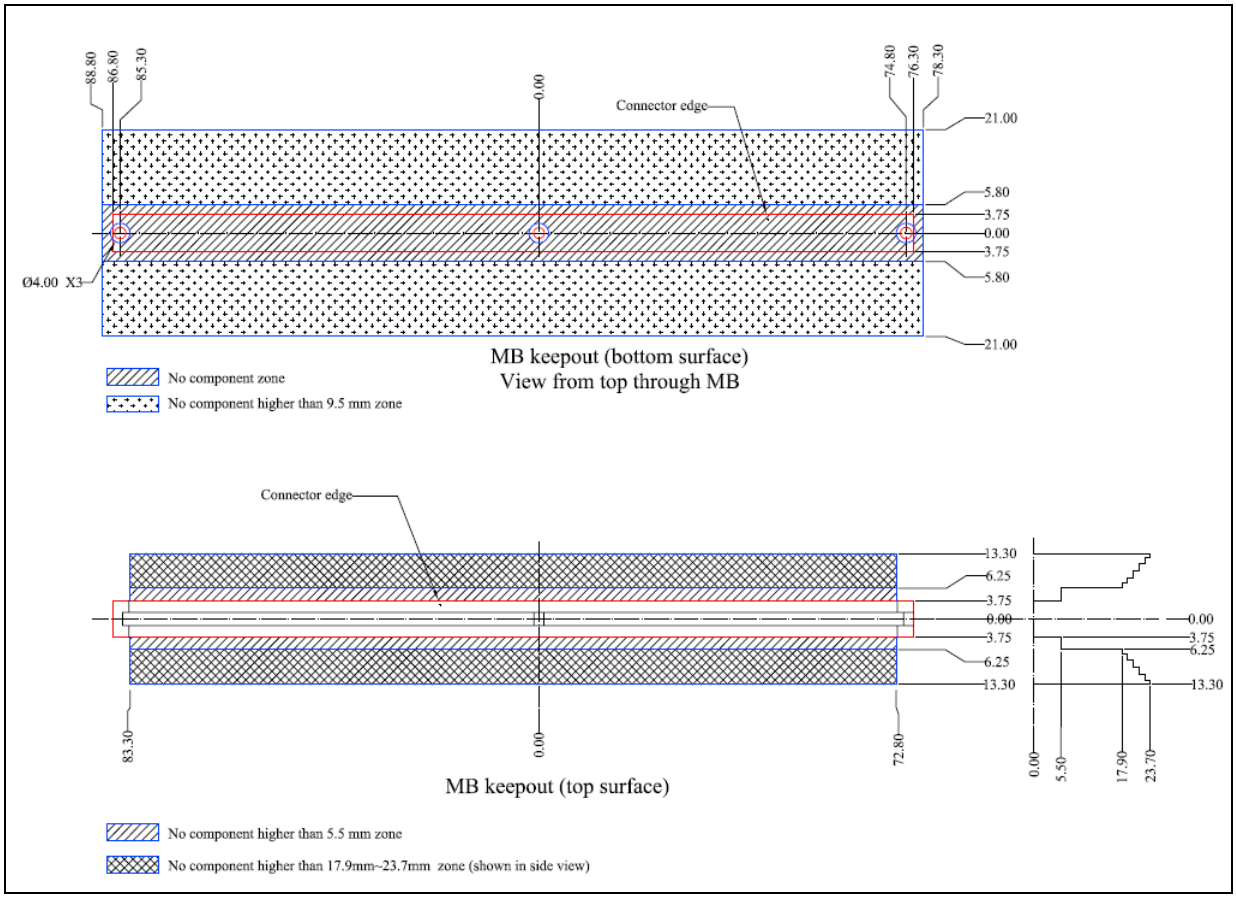
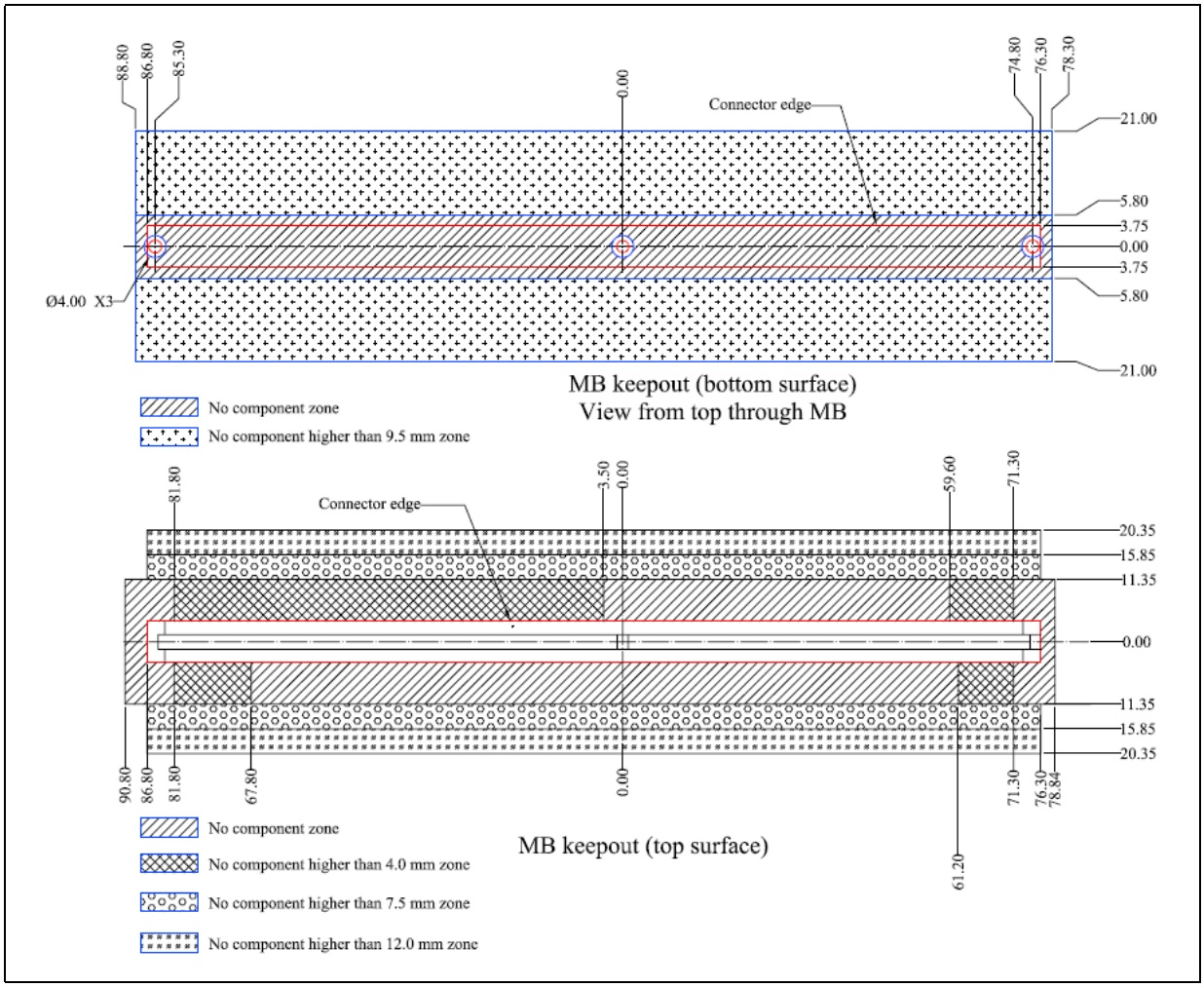
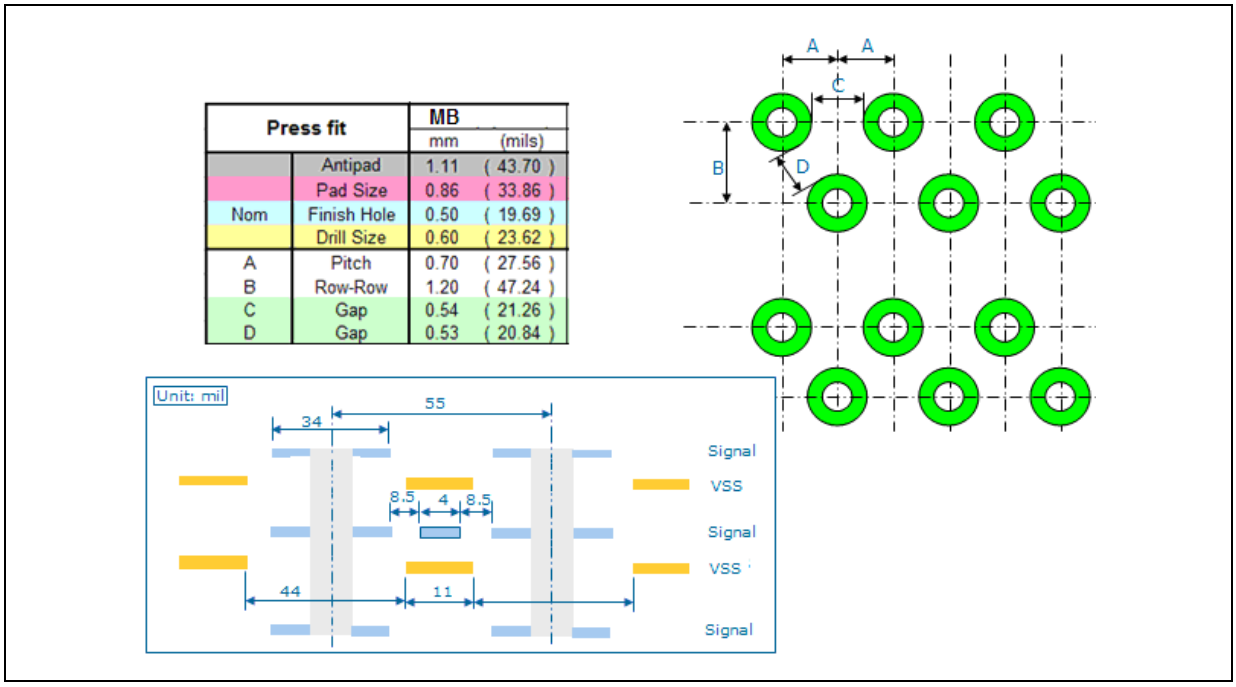


Figure 3-5. System Board Keep-out Zone for Rework



The recommended system board stack-up and via size are shown in Figure 3-6.

Figure 3-6. System Board Stack-up and Via Dimensions

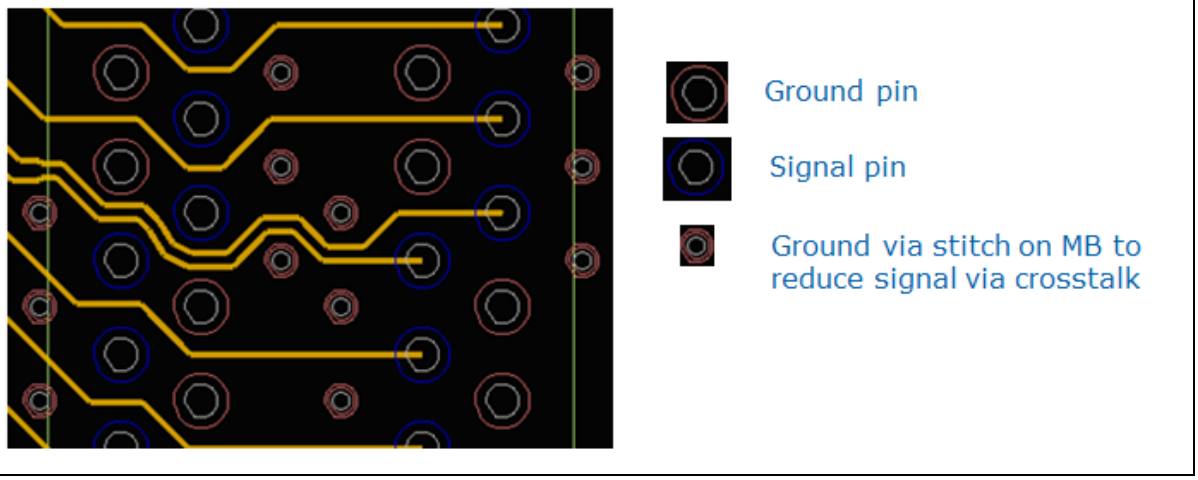


Intel SMI2 connector rely on specific pad sizes and plating types to achieve reliable solder joints between the connector and the baseboard. See manufacturers drawings for specific through hole drill/pad/anti-pad sizes and board finish types.

An example of the Intel® SMI2 connector field routing is shown in Figure 3-7.

- CLK/DQs: 4 mil (gap) — 4.5 mil (TW) — 4.5 mil (gap) — 4.5 mil (TW) — 4 mil (gap)
- DQ/CMD: 8 mil (gap) — 4.5 mil (TW) — 8 mil (gap)

Figure 3-7. Intel® SMI2 Connector Field Routing Example



3.4 Intel SMI2 Riser Card Dimensions

The gold finger positional tolerance is identified as a critical riser card dimension. Gold finger position in relation to riser card edges is critical to ensure connector contacts are properly lined up with the each gold finger. The Intel® SMI2 riser card mechanical dimensions are shown in the Figure 3-8 thru Figure 3-10. The detailed explanation of the gold finger positional tolerance is provided in Appendix D.

External tie bar will be needed on riser card top/bottom layer, inner tie bar is not allowed for gold plating.

Minimum required gold finger plating is 30 micro-inches of gold over 100 micro-inches of nickel. Connector and riser card are to be tested per industry standard EIA 364-1000.

Figure 3-8. Intel® SMI2 Riser Card Dimensions

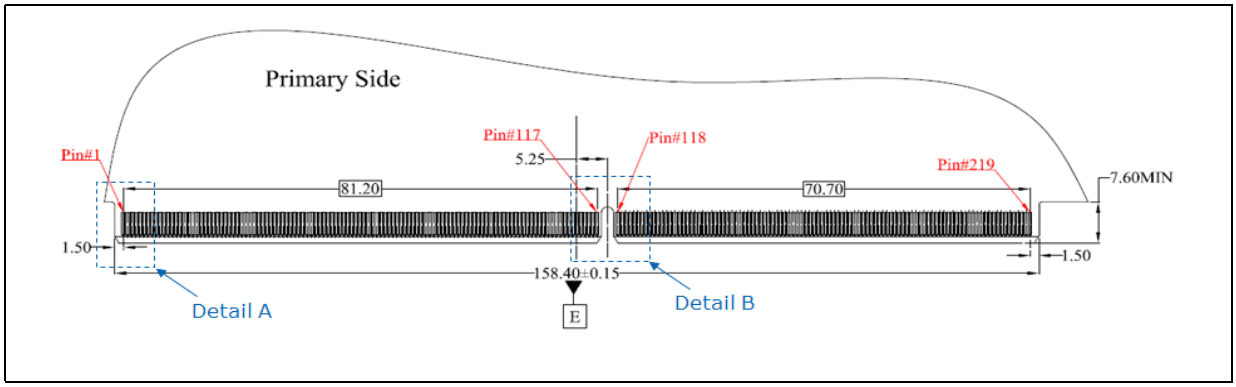


Figure 3-9. Intel SMI2 Riser Card Dimensions (Detail A)

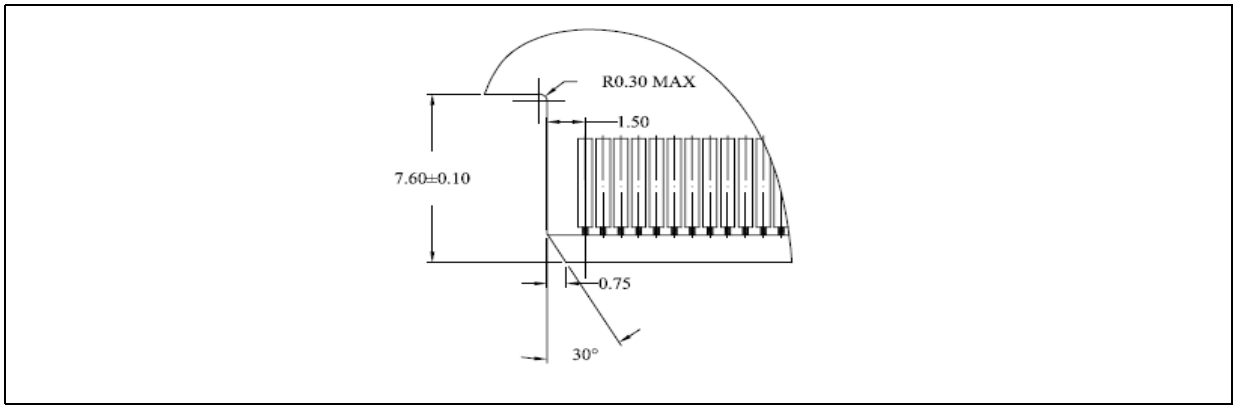
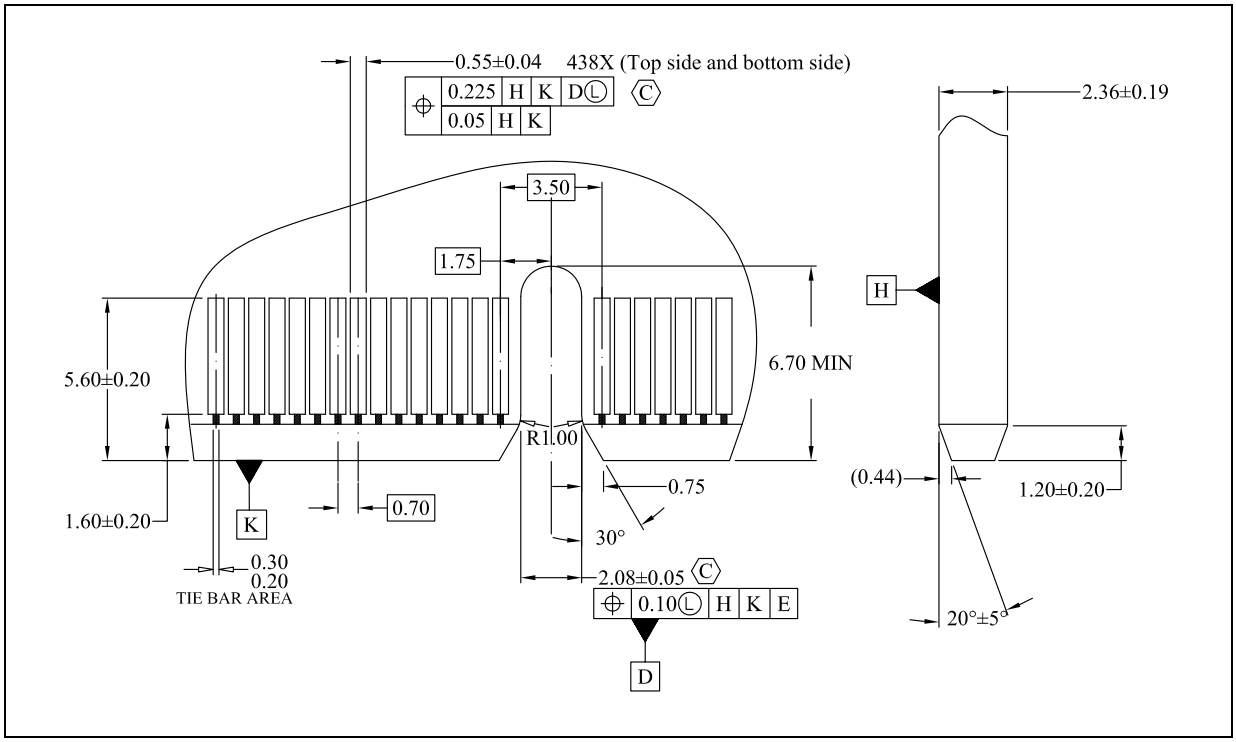


Figure 3-10. Intel SMI2 Riser Card Dimensions (Detail B)



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4 Electrical Specification

This section specifies the Intel SMI2 connector electrical requirements including connector impedance, contact resistance, current carrying capacity, and the parasitic requirements.

The following table outlines Intel SMI2 connector DC electrical requirements.

Table 4-1. DC Electrical Requirements

Parameter	Requirements	Procedure
Impedance	34.5 Ohms min 48.5 Ohms max TDR rise time = 100 ps (10%-90%)	See Appendix A for measurement
Contact Resistance (Low Level Contact Resistance- LLCR)	Initial: 20 milli-Ohms max for a mated connector Delta (after stress): 10 milli-Ohms max The resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading, shall not exceed 10 milli-ohms.	EIA 364- 23 Subject mated contacts assembled in housing to 20 mV max open circuit at 100 mA max (see Appendix B for measurement)
Current rating	0.50 A per contact minimum. The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C.	EIA 364-70 method 2 Test the mated connector: 1. The sample size is a minimum of three mated connectors. 2. The sample shall be press-fit on a PC board with the appropriate footprint. 3. Wire all the power and all the ground pins in a series circuit. 4. A thermocouple of 30 AWG or less shall be placed as close to the mating contact as possible. 5. Conduct a temperature rise versus current test.
Withstand Voltage	500 V min	EIA364-20
Insulation Resistance	1 M-Ohm min	EIA364-21
Intra pair skew (between any two adjacent pins)	10 ps max	Measurement to be obtained from simulation model @ 50% point on the waveform.

4.1 AC Requirements

The following table lists the Intel® SMI2 connector S parameter requirements. For measurement methodology see Appendix C.

Table 4-2. Connector Single-ended S-parameter Values (Sheet 1 of 2)

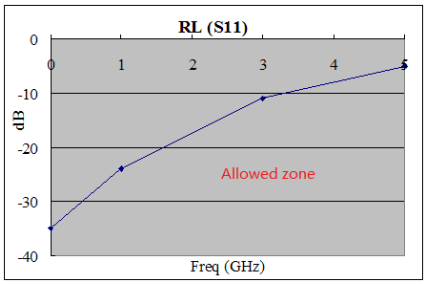
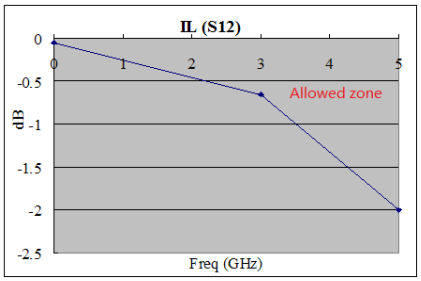
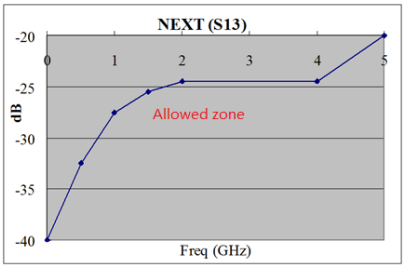
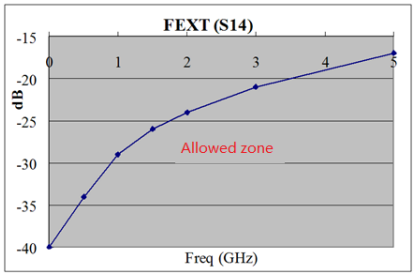
S-Parameter	Target Value	Profile
S11 (Return Loss) ***Note:*** Effects of the baseboard thru-hole via and riser card gold edge finger are included. Specification of Return Loss presumes the data is normalized to 40 Ohms	< 11*f -35 dB (f ≤ 1 GHz) < 6.5*f - 30.5 dB (1 GHz < f ≤ 3 GHz) < 3*f - 20 dB (3 GHz < f ≤ 5 GHz)	 Decision points: (0,-35); (1,-24); (3,-11);(5,-5)
S21 (Insertion Loss) ***Note:*** Effects of the baseboard thru-hole via and riser card gold edge finger are included. Specification of Insertion Loss presumes the data is normalized to 40 Ohms	> -0.2*f - 0.05 dB (0 GHz < f ≤ 3 GHz) > -0.675*f+1.375 dB (3 GHz < f ≤ 5 GHz)	 Decision points: (0,-0.05); (3,-0.65); (5,-2)
NEXT S13 (Near End X-Talk) ***Note:*** Effects of the baseboard thru-hole via and riser card gold edge finger are included. Specification of Near-End X-Talk presumes the data is normalized to 40 Ohms	< 15*f - 40 dB (f ≤ 0.5 GHz) < 10*f – 37.5 dB (0.5 GHz < f ≤ 1 GHz) < 4*f – 31.5 dB (1 GHz < f ≤ 1.5 GHz) < 2*f – 28.5 dB (1.5 GHz < f ≤ 2 GHz) < -24.5 dB (2 GHz < f ≤ 4 GHz) < 4.5*f – 42.5 dB (4 GHz < f ≤ 5 GHz)	 Decision points: (0,-40); (0.5,-32.5); (1,-27.5); (1.5,-25.5); (4,-24.5);(5,-20)

Table 4-2. Connector Single-ended S-parameter Values (Sheet 2 of 2)

S-Parameter	Target Value	Profile
FEXT S14 (Far End X-Talk) ***Note:*** Effects of the baseboard thru-hole via and riser card gold edge finger are included. Specification of Far End X-Talk presumes the data is normalized to 40 Ohms	< 12*f – 40 dB (f ≤ 0.5 GHz) < 10*f – 39 dB (0.5 GHz < f ≤ 1 GHz) < 6*f – 35 dB (1 GHz < f ≤ 1.5 GHz) < 4*f – 32 dB (1.5 GHz < f ≤ 2 GHz) < 3*f – 30 dB (2 GHz < f ≤ 3 GHz) < 2.25*f – 27.75 dB (3 GHz < f ≤ 5 GHz)	 Decision points: (0,-40); (0.5,-34); (1,-29); (1.5,-26); (2,-24);(3,-21); (5,-17)

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5 Mechanical, Environmental, and Reliability Specification

This section specifies the connector mechanical and environmental requirements. Seven year life cycle testing is applied for both mechanical requirement and environmental requirement per EIA 364-1000.

5.1 Mechanical Specifications

Intel SMI2 connector mechanical requirements include the riser card mating force and durability. Intel SMI2 connector must comply with the mechanical requirements listed in Table 5-1. Note that the sample size shall follow Section 2.2.1 of EIA-364-1000.

Table 5-1. Mechanical Specifications

Parameter	Value	Notes
Volumetric and Mechanical Dimensions	For mechanical dimensions see Section 3 and drawings.	Visual and dimensional inspection, Procedure EIA364-18 visual, dimensional per applicable quality inspection plan, Requirement: meets drawing
Insertion Force (Riser card to Connector)	30 Kgf max	Test per EIA 364-13 Measure the force necessary to mate the connector assemblies at a maximum rate of 2.54 cm per minute Riser card gage thickness 2.58 mm ± 0.02
Normal force per contact	50 gf min (EOL)	Test per EIA 364-04
Retention Force – Terminal Pin	300 gf min per pin	Test per EIA 364-29 No movement of contact greater than 0.38 mm
Unmate Force (riser card removal from connector)	2 Kgf (~min)	Test per EIA 364-13 Measure the force necessary to un-mate the connector assemblies at a maximum rate of 2.54 cm/minute
Durability	30 cycles over connector life time	Use one riser card and one connector

Additionally, Intel SMI2 connector must meet the material requirements listed in Table 5-2 to ensure compliance with industry standards and regulations.

Table 5-2. Material Requirements

Parameter	Requirement	Notes
Marking	Connector marking must contain: • Manufacturer's insignia • Part Number • Date Code All markings must withstand typical environmental, mechanical, and reliability tests. All markings must be visible after mounting.	
Flammability	UL 94 V-0	Material certification or certification of compliance is required with each lot to satisfy the Underwriters Laboratories follow-up service requirements
RoHS Compliant	RoHS compliant per IEC 62474	RoHS Directive (2011/65/EU)
Low Halogen	1000 ppm max Cl when used in a flame retardant 1000 ppm max Br when used in a flame retardant Per JS-709A Standard - Clause 4	Sample combustion followed by ion chromatography as specified by: British Standard Methods BS EN 14582:2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste)

5.2 Environmental Requirements

Connector environmental tests shall follow EIA-364-1000, Groups 1 thru 6 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications. The test groups/sequences and durations shall be derived from the following application requirements:

- Field temperatures of 65°C
- Field life of 7 years
- Operating Temperature -55° C to +85°C
- Non-operating Life -55°C to +85°C

Both the plating thickness and the baseboard thickness shall be recorded in the environmental test report.

5.3 Reliability Requirement

Intel SMI2 connector reliability test conditions requires completion of ANSI/EIA-364-1000 test groups 1 thru 6. Reliability test conditions are described in Table 5-3. After reliability testing, the connector under test must meet electrical, mechanical and environmental criteria.

Table 5-3. Reliability Test Conditions

Test Description	Test Condition	Notes
Durability	Test per ANSI/EIA-364-09 precondition 20 plug/unplug cycles	No evidence of physical damage
Temperature Life	ANSI/EIA-364-17, Method A (without electrical load) Test: 105 °C, 72 hrs precondition: 105C, 72 hrs perform in mated condition	
Low Level Contact Resistance (LLCR)	ANSI/EIA-364-23	Termination of connector to board carrier shall be included in the measurement
Physical Shock	ANSI/EIA-364-27, Test Condition A, Half Sine, duration 11 ms, 100 mA load, 3 drops each axis normal and reversed directions, perform in mated condition.	
Vibration	ANSI/EIA-364-28 Test Condition D 5 Hz @ 0.02 g^2/Hz to 20 Hz @ 0.02 g^2/Hz (slope up) 20 Hz to 500 Hz @ 0.02 g^2/HZ (flat) Input acceleration is 3.10 g RMS. Both halves rigidly fixed. 15 Minutes per axis on all 3 axes (X, Y, Z). Random control limit tolerance is ±1.5 dB. Continuity check: Electrical load 100 milliamperes for all contacts.	No discontinuities of ≥ 1 microsecond
Cyclic Temperature & Humidity	ANSI/EIA-364-31B, Method III without conditioning, initial measurements, cold shock and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 10 cycles in mated condition	
Thermal Shock	ANSI/EIA-364-32, Method A, Table2, Test Condition 1, -55°C to 85°C, perform 5 cycles in mated condition	
Thermal Disturbance	ANSI/EIA-364-1000 Cycle the connector between 15° ±3°C and 85° ±3°C, as measured on the part. Ramps should be a minimum of 2°C/minute. Dwell times should insure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled, perform 10 cycles in mated condition.	
Thermal Cycle	ANSI/EIA-364-1000 Cycle the connector between 15° ±3°C and 85° ±3°C, as measured on the part. Ramps should be a minimum of 2°C/minute. And dwell times should insure that the contact s reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled, perform 500 cycles in mated condition.	
Mixed Flowing Gas	ANSI/EIA-364-65, class IIA, Option 4, perform in mated condition, duration 7 days	
Dust	ANSI/EIA-364-91 Condition: Unmated Dust Composition: #1 Test Duration: 1 hr 15 minutes Test per group D (LLCR)	This test applies to connectors having lubricated contacts. Use testing of non-lubricated connectors as control mechanism.

5.4 Riser Card Mechanical Requirements

The connector will not provide structural support for the riser card or cards that plug into the riser card. The system/chassis must provide structural support.

Table 5-4. Riser Card Mechanical Requirements

Description	Requirement	Test Procedure
Riser card insertion/ extraction/retention	Must be used in any use condition. Chassis/system must provide general alignment of riser card to connector, but riser slot to connector key interface must be allowed to provide final riser card position reference.	EIA 364-27, EIA364-28 Appropriate conditions to model use condition and system configuration.
Riser card mass limit	1.32 kg [2.9 lb] max	Card and all components, including thermal solutions.
Riser card keepouts	Meet applicable inspection plan.	EIA 364-18 Visual, dimensional per applicable quality inspection plan.

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6 Supplier Contact Information

6.1 Supplier Contact and Part Number Information

Third-party supplier has been enabled to ensure that the Intel® SMI2 connector is available.

Notes:

1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of the connector.
2. All "Part Numbers" listed are subject to change.
3. Supplier information provided in the table was deemed accurate at the time of release of this document.
4. Customers planning on using the Intel® SMI2 connector should contact the supplier for the latest information on their product(s).
5. Customers must evaluate the connector performance against their own product requirements.

Table 6-1. Connector Part Number and Supplier Contact Information

Component	Part Number		
	Description	Lotes	Intel
Connector	30 u" min Gold, with Lube, Metal Key	AAA-EDG-003-Y06	G25700-003
	30 u" min Gold, Metal Key	AAA-EDG-003-Y04	G25700-002
	30 u" min Gold, Plastic Key	AAA-EDG-003-Y02	G25700-001
Assembly Tool	Lotes part number:	G02-001-765	
Rework Tool	Lotes part number:	G02-001-766	

Note: Connector contact gold plating thickness, use of the metal key vs Plastic key, and applying lubrication to the contacts have shown to improve mechanical reliability of the connector. It is at the discretion of the customer to identify, select, and verify which version of the connector is Best suited for use in their application.

Supplier Contact:

Cathy Yang

Address: No. 526 North of Jinling Road, Nansha District, Guangzhou
Guangdong Province, China 511458

Phone: 86-20-84686519

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A TDR Measurements

A.1 Reference Equipment

Time Domain Reflectometer (TDR): Agilent Infinium DCA-J 86100C Digital Communications Analyzer, Agilent 86100C Infinium DCA-J Mainframe, or equivalent

Agilent TDR Cal KIT or equivalent

Southwest Microwave SMA connector: Model 292-11A-5

Seekonk SL-6 Torque Screwdriver, McMaster-Carr part number 5699A11, 1/16” Allen screw adaptor, Pronto 4770-1/16”, to tighten 1-72 screws of SMA connector to board to 2.0 inch-pounds

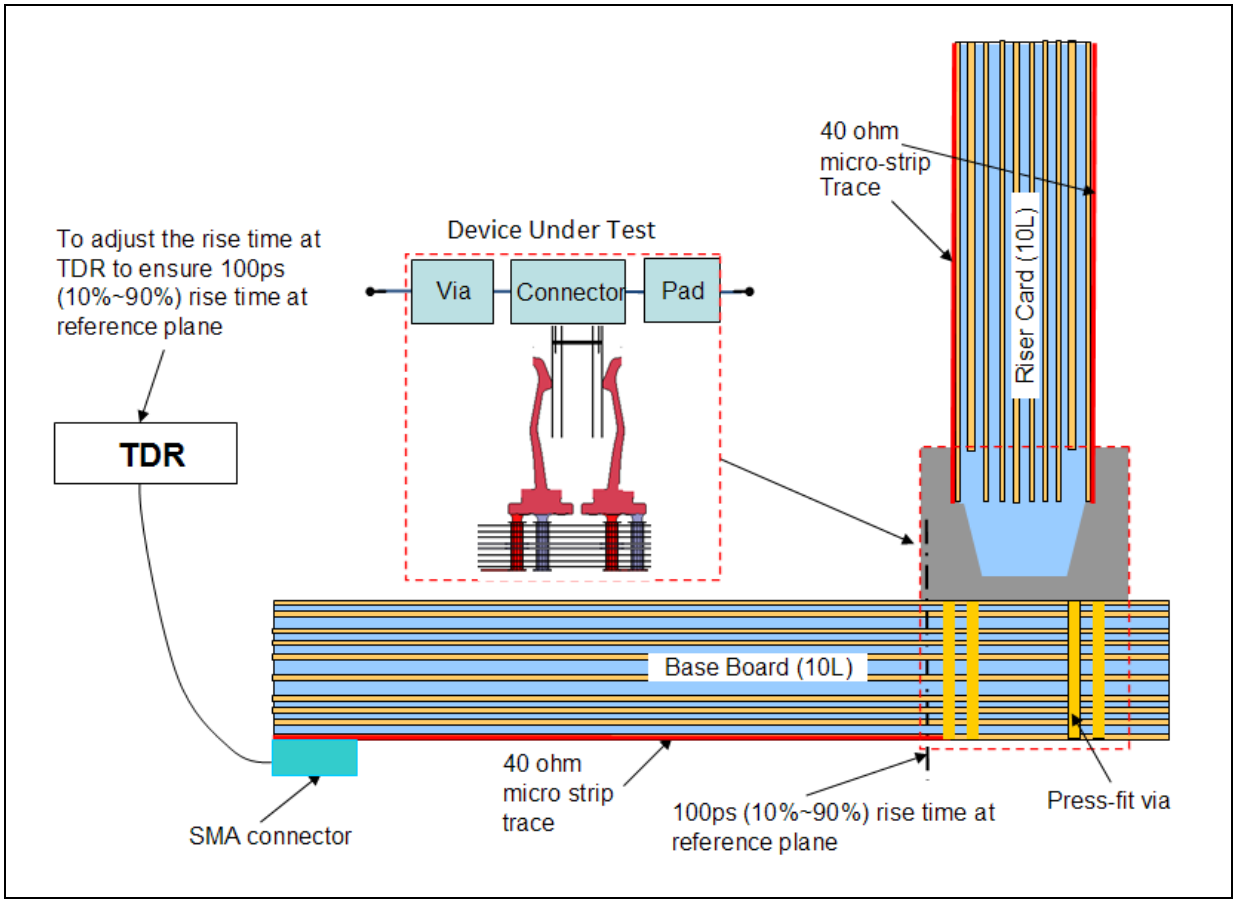
Half through trace on calibration card (shown in Figure C-4) to capture the 100 ps rise time at the reference plane of connector

A.2 TDR Setup

Apply TDT on half through trace on calibration card to adjust the rise time launched at SMA to ensure 100 ps (10%-90%) at reference plane, measure connector impedance using TDR with the adjusted rise time.

Make a rise time measurement prior to mounting the DUT connector to confirm adequate rise time. Standard 40-Ohms calibration is used to take the reference plane to the end of the cables before the test fixture. Make sure you de-skew both the input and output cables. The recommended accuracy of de-skew is less than 1 ps. Cables that are tightly phase matched with low-losses provide the best de-skew accuracy.

Figure A-1. TDR Measurements Setup



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B LLCR Measurements

B.1 Reference Equipment

Micro-ohmmeter (such as Keithly 580; Agilent 4338B)

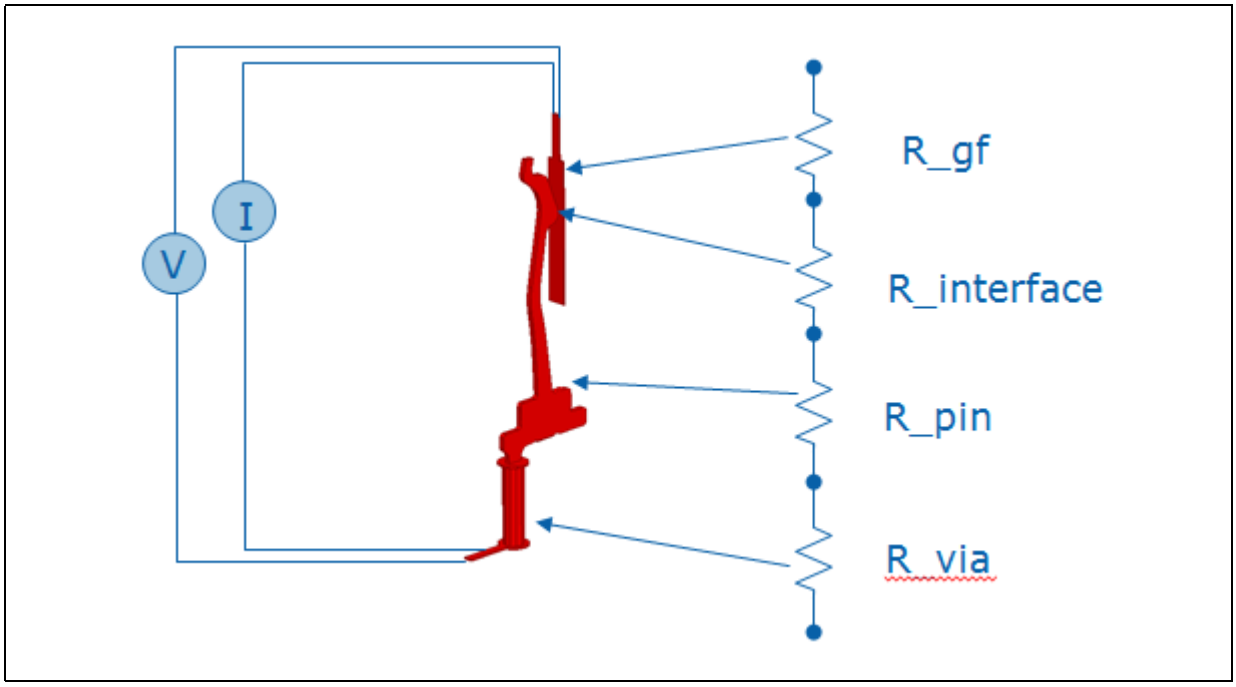
Cable with clamper or pogo pins

B.2 Test Fixture

Figure B-1 illustrates LLCR measurement using 4-terminal technique. The contact bulk resistance, including:

- Gold finger resistance
- Resistance at interface between pin and gold finger, the value is sensitive to interface condition, such as normal force, contamination, etc.
- Contact pin resistance
- Via resistance

Figure B-1. LLCR Measurements Using 4-terminal Technique



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C Frequency Domain Measurements

C.1 Reference Equipment

- Vector Network Analyzer (VNA) System –Agilent E8364B PNA Series Network Analyzer
- Agilent N5203A, Anritsu MS4640A Series, Rhode and Schwartz ZVB 20, or equivalent
- SMA's- Southwest Microwave 292-11A-5
- Calibration Standard - TRL standards are part of test board panel. The following calibration standards are provided: Open, Short, Zero length Thru, and Lines.
- Two 50 Ω high frequency, low loss phase-matched cables. Recommend cables offered by Micro Coax (part number UFB197C) or equivalent. The cables are used to connect the SMA's to the measurement ports on the Vector Network Analyzer (VNA).

C.2 Test Fixture and Samples

The test fixture for connector S-parameter measurement should be designed and built to the following specifications:

- The test fixture shall be a PCB of the micro-strip structure. The test fixture PCB thickness shall be 2.36 mm (0.93"), and the test add-in card should be a break-out card fabricated in the same PCB panel for the fixture.

Note: By making the test add-in card as a break out from the test fixture PCB, it ensures boards characteristics are identical.

- The measurement signals shall be send to the connector from the bottom of the test fixture, capturing the worse case through-hole cross talk effect. The connector reference planes are set 50 mils away from gold finger and PTH via pad. The traces between the connector reference plane and measurement ports (SMA) should be uncoupled. The trace lengths between the connector reference plane and measurement port (SMA) on the baseboard and riser card are equal.
- All of the traces on the baseboard and riser card must be held to a characteristic impedance of 40 Ω with a tolerance of ±5%. The ground plane immediately underneath the edge finger pads must be removed. The press-fit hole of the baseboard shall have the stack-up shown in Figure C-4.
- The SMA launch structure shall be designed to minimize the impedance discontinuity from SMA.
- The baseboard and riser card stack-up are shown in Figure C-1. For better impedance control, core was used between layer 1 [E1] and layer 2 [E2], layer 9 [E9] and layer 10 [E10]. The rest dielectric materials were used accordingly.

Figure C-1. Connector and Riser Card Test Boards Stack-up

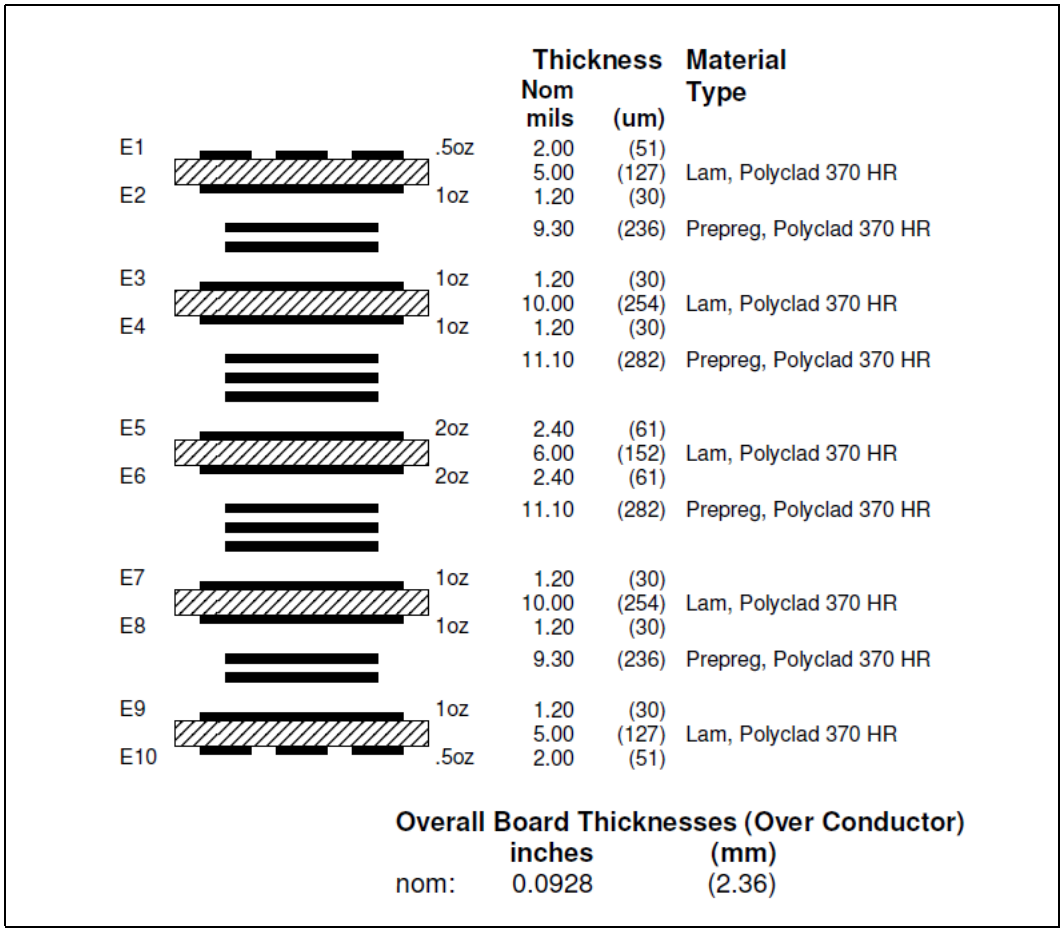
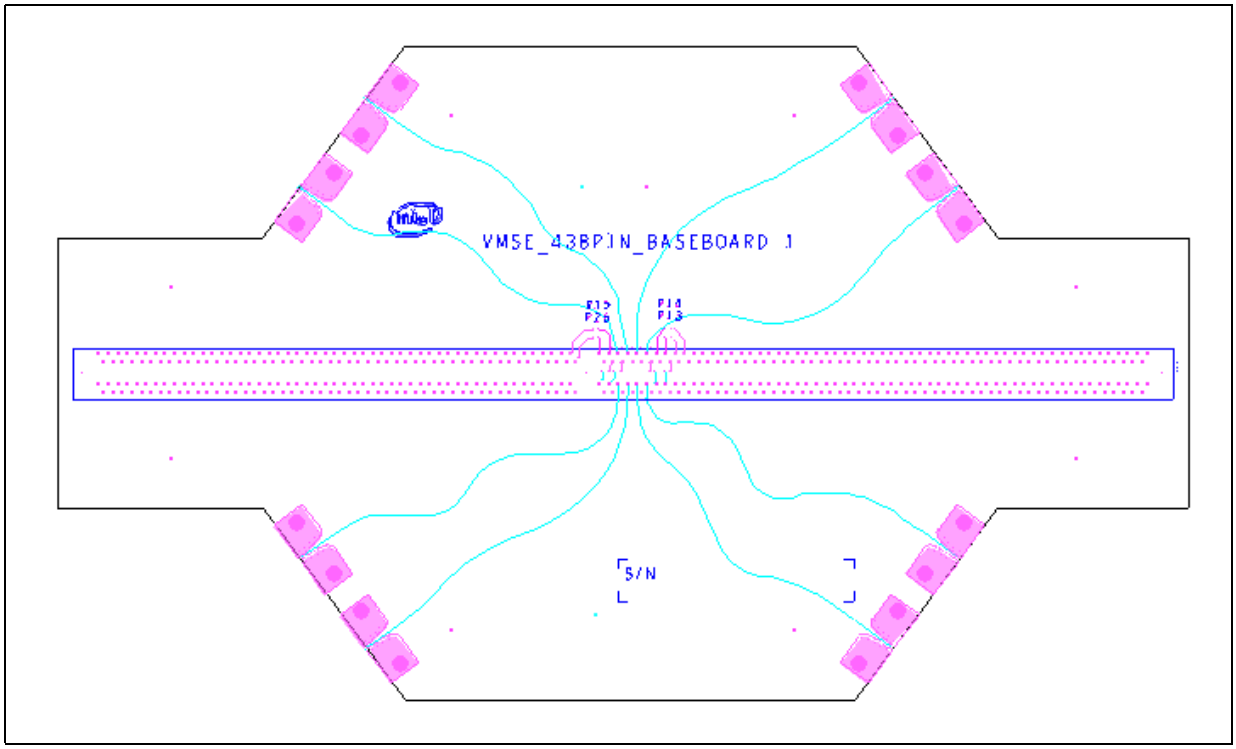


Figure C-2 and Figure C-3 illustrate the footprint of the baseboard and riser card test boards used in taking electrical measurements.

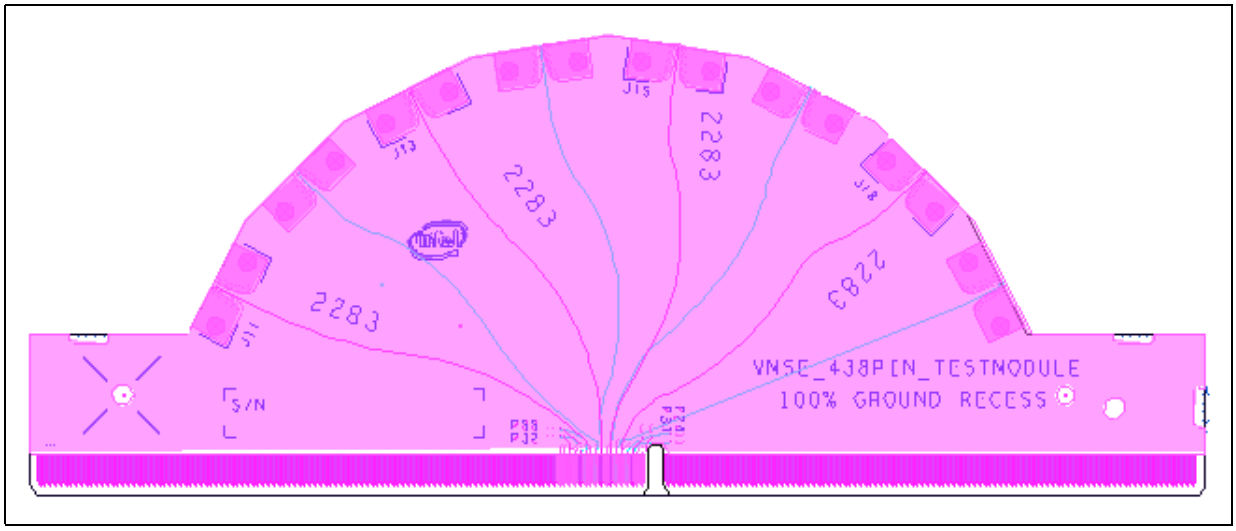
Measurements shall be taken from 200 MHz to 14.2 GHz, using a VNA. For maximum accuracy, the impact of the trace between the SMA connectors and the connector will be removed by TRL calibration.

Figure C-2. 438-Pin Connector Test Board



All measurements must be made at room temperature, and humidity condition not to exceed 65% RH (non-condensing).

Figure C-3. Riser Card Test Board



C.3 Calibration

To properly characterize the performance of the connector in the test fixture, the VNA must be calibrated and traced to a known standard. The intent of the calibration is to eliminate systematic errors in the measurement and to improve measurement

accuracy. The precise geometric location at which a vector network analyzer measurement is made is called the reference plane. There are sometimes two different reference planes involved in a connector measurement. If a commercial coaxial calibration kit is used, it will typically establish a reference plane near the end of the test cables. In this case, a second step, called de-embedding, is needed to remove the influence of the test fixture and move the reference plane closer to the connector. The connector reference planes are set 50 mils away from gold finger and PTH via pad.

TRL is the recommended method for calibration, the trace lengths on calibration card are shown in Table C-1. TRL has the advantage that it can be easily tailored to impedances other than 50 ohms and can eliminate the need for de-embedding the test fixture. The calibration card is shown in Figure C-4.

Table C-1. Calibration Traces Length

	Length Offset (cm)	Length Offset (mil)	Min. Freq. (GHz)	Max. Freq. (GHz)	Time Delay (ps)
LINE 1	7.795	3068.9	0.200	0.829	488.0
LINE 2	1.882	740.8	0.829	3.433	117.8
LINE 3	0.454	178.8	3.433	14.221	28.4
Trace Length	cm	mil			
Ref. plane to SMA	5.52323	2174.5			
SHORT	5.52323	2174.5			
OPEN	5.52323	2174.5			
LOAD	5.52323	2174.5			
THROUGH	11.04646	4349.0			
LINE 1	18.842	7417.9			
LINE 2	12.928	5089.8			
LINE 3	11.501	4527.8			

Figure C-4. TRL Calibration Card

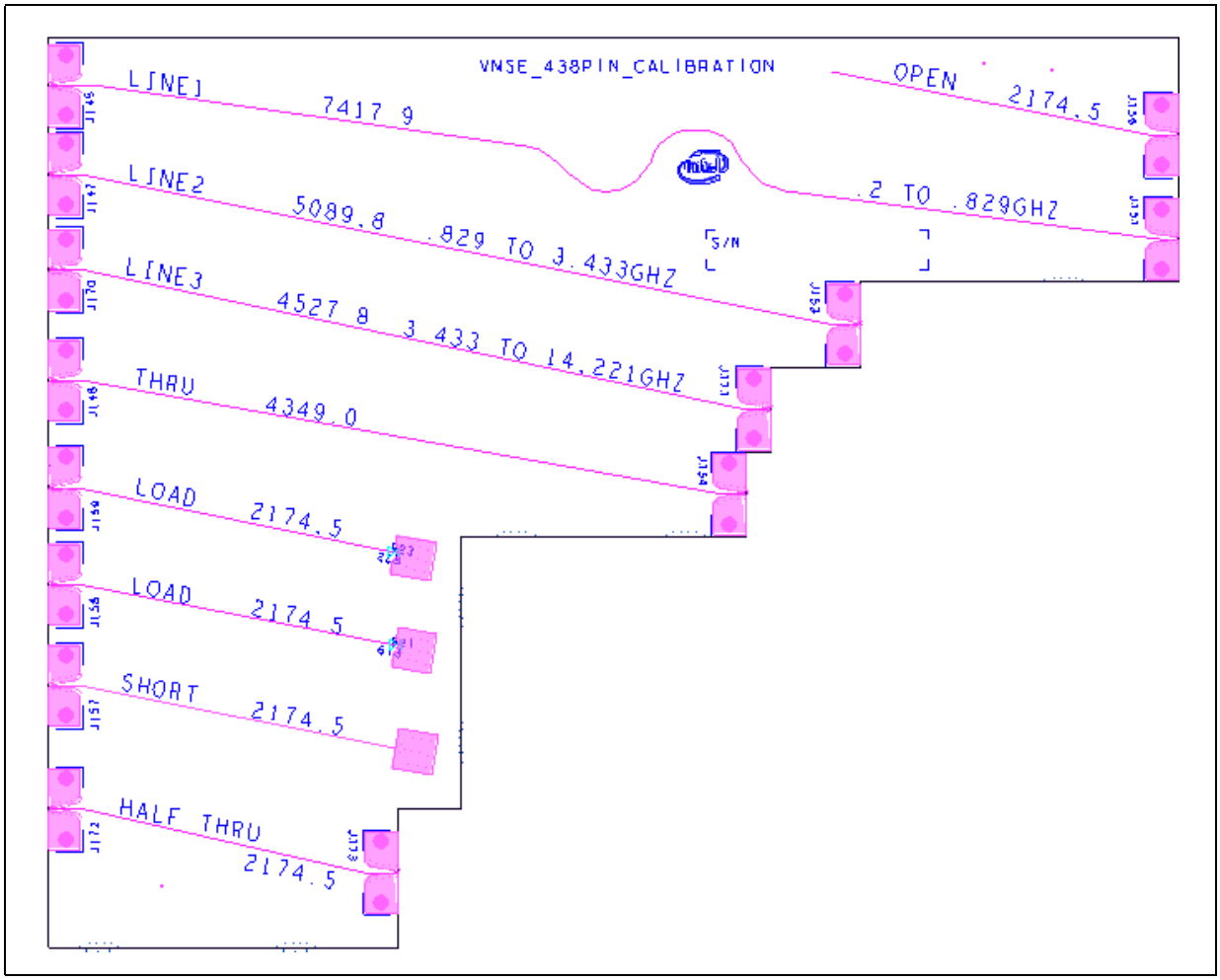
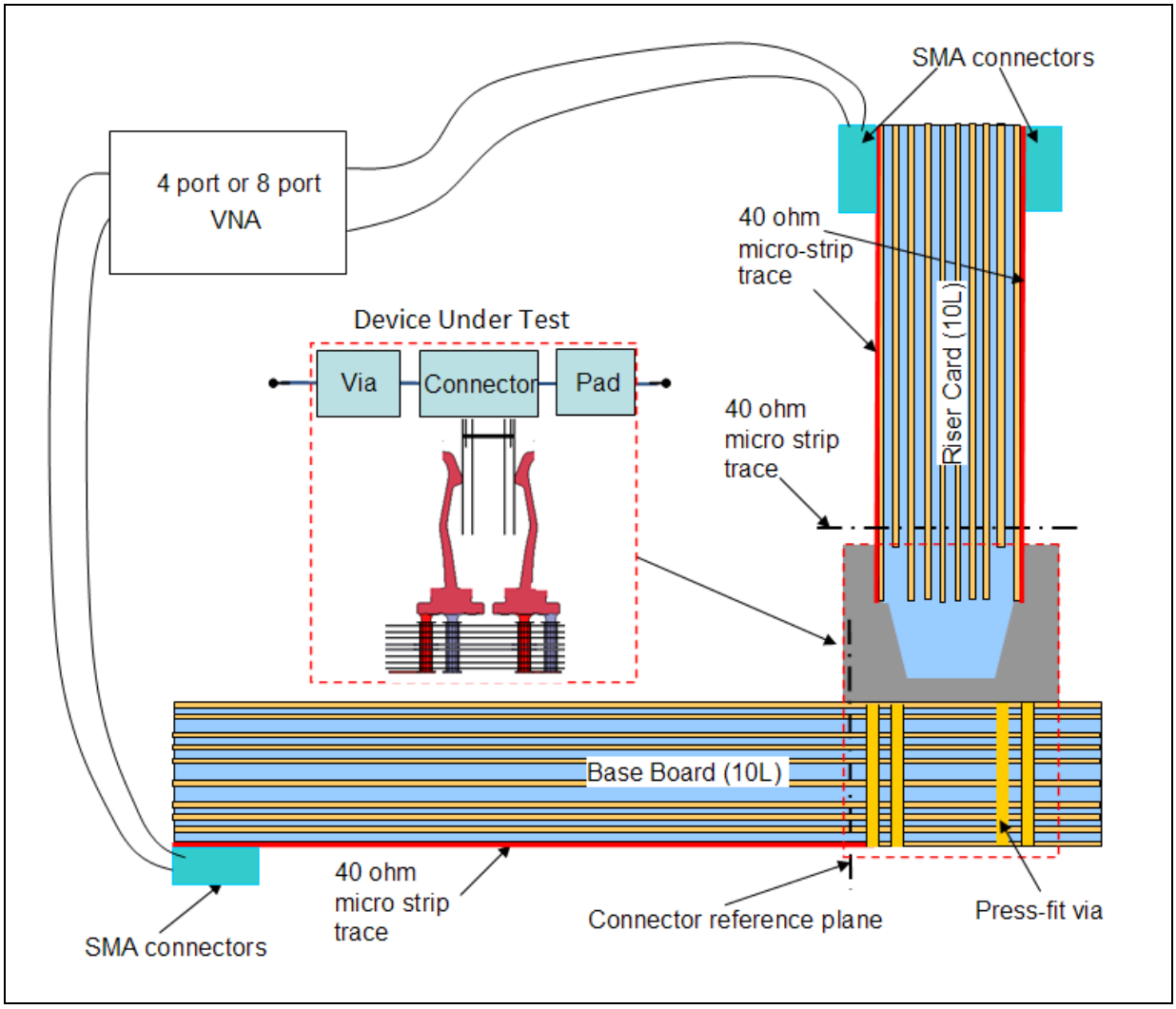


Figure C-5. Reference Plane Location on System Board and Riser Card



C.4 Sample Preparation

The baseboard and riser card test boards shall be used for electrical test only. Align the connector pins with the corresponding through press-fit hole of the baseboard. Firmly press the connector into the board with uniform pressure across the connector body until all of the connector standoff points are flush with the baseboard surface. The gap between the baseboard and the connector standoff must be less than 0.05 mm to be considered a good sample.

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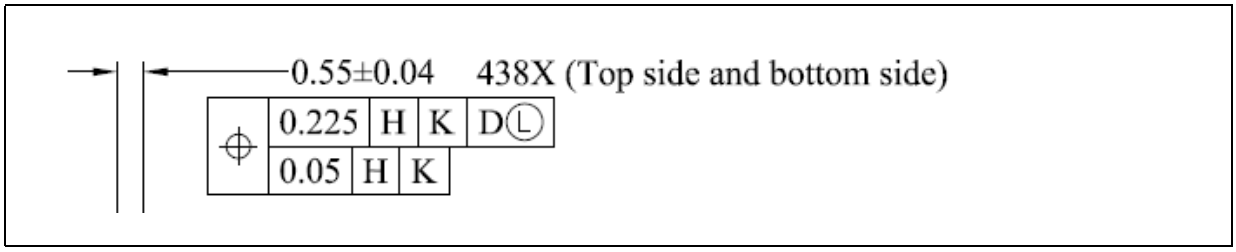
D Riser Card Gold Finger Positional Tolerance

Dimensions of the Intel® SMI2 riser card edge are provided in Section 3.4. Detailed gold finger positional tolerance is shown in Figure D-1 and Figure D-2. Least material condition (LMC) is applied to Datum D which will introduce bonus tolerance on gold finger positional tolerance. The dimensioning is for use only as reference by the board manufacturers since it is not in compliance with geometric dimensioning and tolerances (GD&T).

In a case which the riser card notch is at least material condition where the notch width is 2.13 mm, the allowed gold finger positional tolerance is 0.225 mm (or ±0.113 mm). When the riser card notch is at nominal dimension, 2.08 mm, the allowed positional tolerance is 0.275 mm (or ±0.137mm). In a case which the riser card notch is at maximum material condition where the notch width is 2.03 mm, and the allowed positional tolerance is 0.325 mm (or ±0.162 mm). As a reference, Table D-1 lists the allowed gold finger positional tolerances (B) with respect to the riser card notch width dimension (A).

Figure D-1. Gold Finger Size and Positional Tolerance



Where:

Datum H is riser card surface

Datum K is riser card bottom edge

Datum D is riser card notch center line

Figure D-2. Gold Finger Location Tolerance

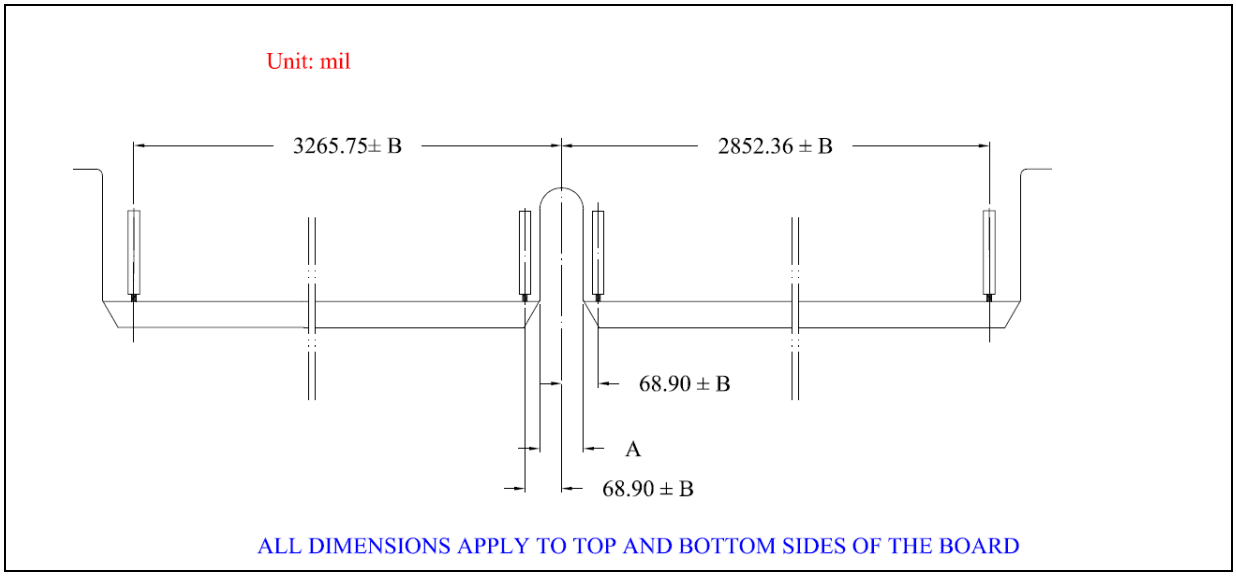


Table D-1. Allowed Gold Finger Positional Tolerance

Notch width (A)		Allowed B		Note
mil	mm	mil	mm	
83.86	2.13	4.43	0.113	Maximum notch width
83.66	2.13	4.53	0.115	
83.46	2.12	4.63	0.118	
83.27	2.12	4.72	0.120	
83.07	2.11	4.82	0.123	
82.87	2.11	4.92	0.125	
82.68	2.10	5.02	0.128	
82.48	2.10	5.12	0.130	
82.28	2.09	5.22	0.133	
82.09	2.09	5.31	0.135	
81.89	2.08	5.41	0.137	Nonimal notch width
81.69	2.08	5.51	0.140	
81.50	2.07	5.61	0.142	
81.30	2.07	5.71	0.145	
81.10	2.06	5.81	0.147	
80.91	2.06	5.91	0.150	
80.71	2.05	6.00	0.152	
80.51	2.05	6.10	0.155	
80.31	2.04	6.20	0.157	
80.12	2.04	6.30	0.160	
79.92	2.03	6.40	0.162	Minimum notch width

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E Riser Card Installation

E.1 Riser Card Installation Guide

There are different alignment orders to guide the riser card into Intel® SMI2 connector, and to support the riser card during the shock and vibration conditions.

Note: Blind mating of riser card to the connector requires alignment features.

1. Chassis will have to provide the first order of guidance for the riser card to ensure it is properly oriented and aligned to the connector.
2. The second order of guidance is provided by the connector end towers with riser card edge chamfers. Chassis guides and insertion features must allow the riser card to freely move into its correct position with respect to connector open slot.
3. Connector key to riser card slot provide the final, 3rd order, guidance. Once the riser card notch locates to the key, the center of the riser card should be properly aligned with the center of the connector. This is considered the "SET" position before fully engagement as shown in Figure E-2. This step is very critical and need additional caution by the installer to ensure proper engagement is made before load is applied.
4. Apply uniform load to fully engage the riser card to connector.
5. Secure riser card assembly in final fully seated position

E.2 Riser Card Pre-alignment Mechanism

Guide features are required for the riser card to align card slot to the connector keying feature before insertion load is applied.

Dimensions and tolerances of the chassis guide features must be such that at the worst case condition the offset between the board slot in middle of the riser card and the center of connector key is less than 1.5 mm as shown in Figure E-1. Any offset > 1.5 mm will require the position of the rise card adjusted manually to align with the connector before applying insertion load. All allowed positions of card guide must enable the slot on the riser card and connector key to fully align without interference (over-constraint).

Figure E-1. Riser Card Notch to Connector Keying Alignment

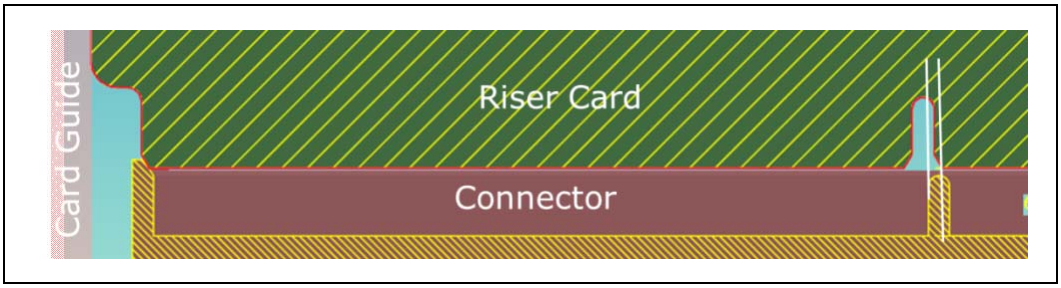
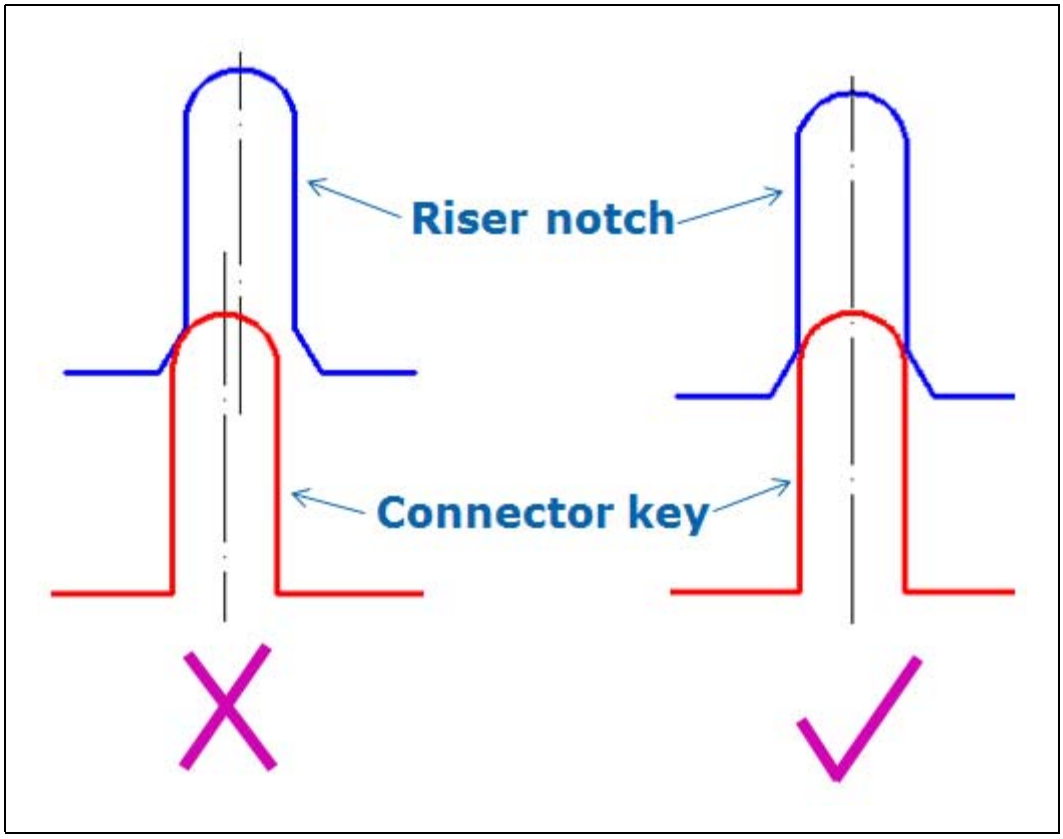


Figure E-2. Proper Alignment Between Riser card Notch and Connector Keying



E.3 Insertion/Extraction Mechanism

Because of the connector high pin count, the insertion/extraction forces exceed the ergonomic limits for a manual installation operation. Additionally manual insertion/ extraction has high possibility of rocking the riser card which may damage the connector contacts, gold fingers, and possibly cause misalignment risk.

A mechanically assisted insertion/extraction mechanism is recommended in all use conditions. The mechanism should provide mechanical advantage to bring loads within the required ergonomic limits. The mechanism should also be designed such that it does not introduce lateral force onto connector.

Additional caution is required to ensure the riser card is uniformly inserted into the connector during insertion/extraction such that all connector contact simultaneously engage with gold finger.

E.4 Retention Mechanism

Retention mechanism from the chassis (system) is required to provide the riser card with mechanical structural support. The retention mechanism will reduce the shock and vibration risks by securing the riser card to the chassis.

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F Shock and Vibration Test Methodology

This section describes the applied physical shock and vibration (S&V) test methodology to applied to verify the connector compliance with its environmental specification.

F.1 Test Equipment

1. Vibration Machine
2. S&V Test Fixture
3. Riser Test board with appropriate dimensions and mass representing the riser card mechanical specifications. Figure F-2 illustrates a block of aluminum attached to the a PCB representing a typical mass of component on the riser card.

   Riser test board dimensions:

   Length: 225 mm

   width: 160 mm

   Riser test board Mass: 1.32 kg
4. Connector Test Board with a connector

F.2 Test Environment

Temperature: Room temperature (21 to 24 °C)

Relative Humidity: 60-65% RH (recommended)

F.3 Test Conditions

See connector Physical Shock and Vibration testing requirements specified in the reliability requirement section of this document and ANSI/EIA-364 test procedures.

F.4 Test Fixture

A test fixture is required to support and constrain the riser card movement with respect to the connector mounted on a base board. The fixture shall mimic the riser card support structure and tolerances. Figure F-1 illustrates a fully constrained riser card movement in X, Y, and Z axis. A gap of approximately 1mm is provided in the PCB slot to ensure the riser card is fully seated in the connector.

Figure F-1. Riser Test Card Allowable Movement in Z-Axis

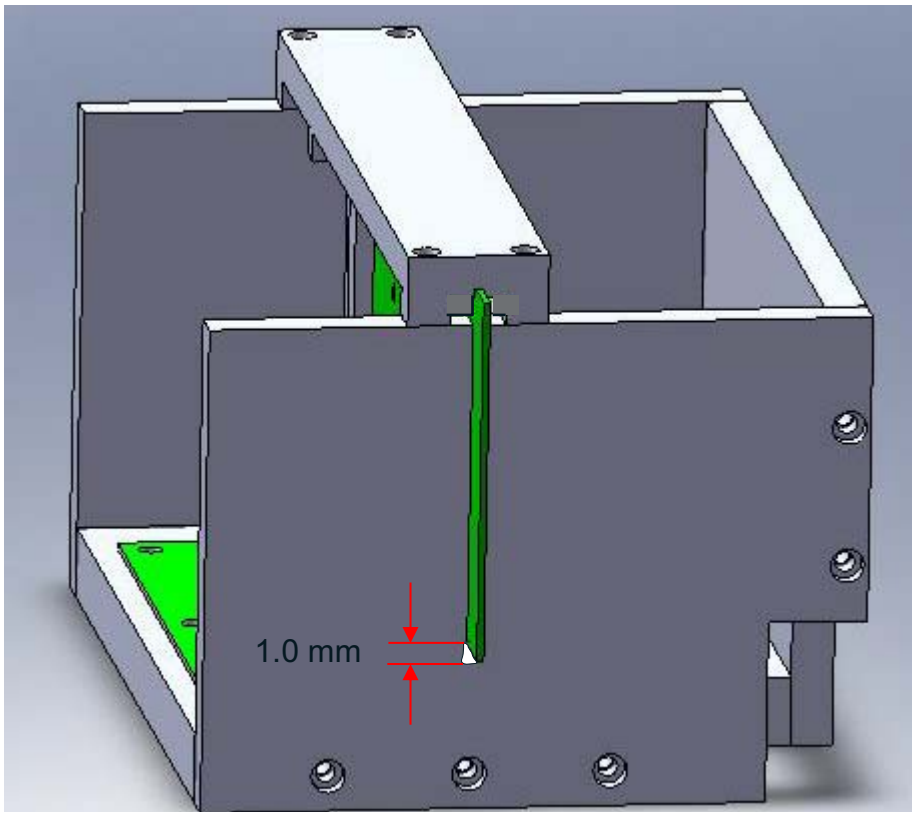
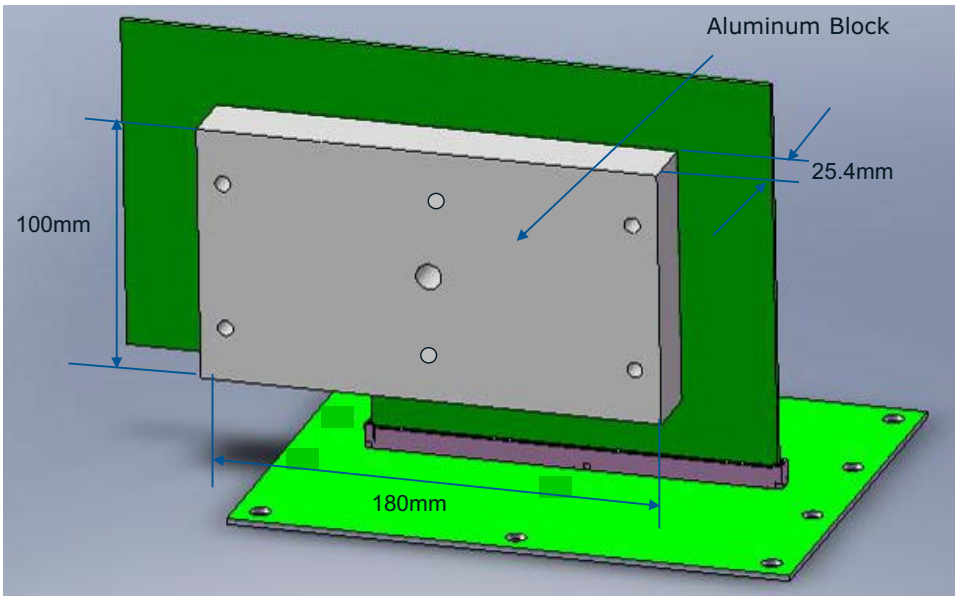


Figure F-2. Riser Test Card Mass



F.5 Post Test Verification

Post shock and vibration tests inspect the riser test board and the connector for physical wear and damages. Inspection shall include but not limited to the riser card gold fingers.

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G Assembly/Rework Guidance

G.1 Press Tool Loading

1. **Press System Requirements**

- The press tool should have the capability to slow to 1.27± 0.25 mm/sec while applying the appropriate force.
- The majority of qualification, testing, and characterization of the final product to be performed at the final insertion rate of 1.27 mm/sec.
- Intel® SMI2 Connector requires maximum force of up to 1.63 Kgf/pin to be fully seat into the baseboard. NOTE: To prevent damaging the baseboard or the connector, do not exceed the maximum allowable connector pin insertion force.
- The press tool should have Z axis control capability to within 0.125 mm.
- Press tool should have a press bed flatness adequate to ensure the application tooling properly engages the connector pressing surfaces. The face of the application press should be parallel with the PCB surface to within 0.125 mm, and should have a Z-axis stroke of 25 mm or greater.
- Pressing mechanism must restrict side-to-side movement during press cycle.

2. **Alignment of the PCB and Connector**

- The application tool (insertion head) can be manually placed on the mating side of the connector or attached to the press ram. The alignment of the PCB in the press is such that the press ram is approximately (within a diameter of 12.7 mm) centered above the insertion head.

3. **Press**

The application tool (insertion head) is designed to conform to the mating end geometry of the connector. Ensure the connector is properly pre-loaded, place the PCB into the press, and place the insertion head on the connector as shown in Figure G-1.

Figure G-1. Connector Assembly

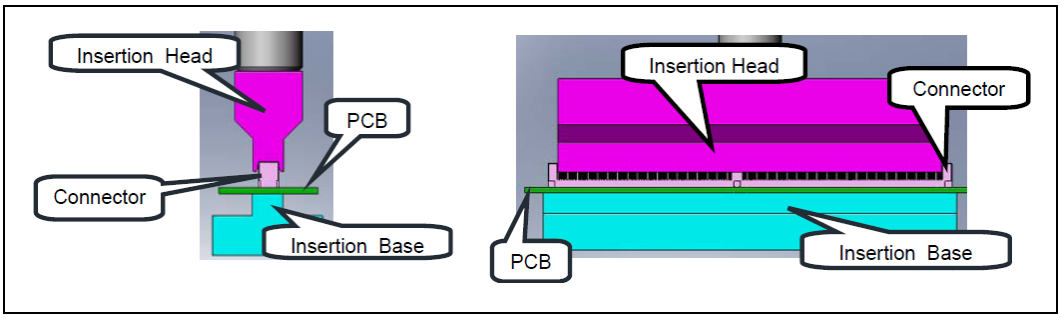


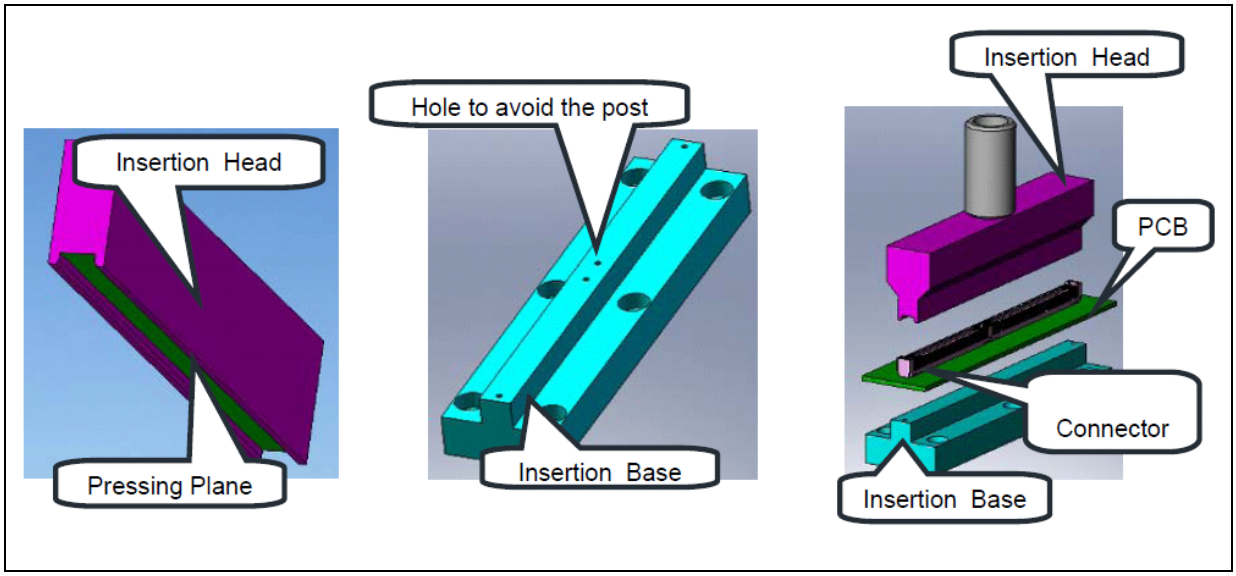
Table G-1. Connector Pin Insertion Force

Press Force	Value	Notes
Pre-load Force	0.125 kgf/pin	Force adequate to insert the connector pin the baseboard holes. This is an approximation value.
Pre-seating Force	0.25 kgf/pin	Force adequate to ensure the connector does not become dislodged This is an approximation value.
Insertion Force	1.63 kgf/pin max	Force necessary to fully insert the connector pins into baseboard holes.

G.2 Assembly

A press tool is required to aid in inserting the connector pins into the baseboard. The press tooling consists of insertion head and insertion base, as show in Figure G-2. Following steps provide general instructions on using the tool to complete the connector installation onto a baseboard.

Figure G-2. Connector Insertion Tool



Step 1: Inspect the connector pin tips for bents or damages

- Use approved pin gauge to inspect the connector pin positions. This step is to ensure pin tip positional accuracy was not compromised during packaging, shipping, or handling prior to installation. An out of position pin could result in bent and/or folded pins and severe board damage.

Step 2: Inspect the plated through hole on PCB

- Inspect all connector holes in the baseboard for damaged, blocked, or obstruction prior to performing the pressing operation. This can be done using optical or mechanical inspection tools. During any mechanical or inspection operation requiring physical contact with the baseboard, use caution to prevent damaging the inside of the PTHs.

Step 3: Align the baseboard and the connector to the press tool

- Ensure the entire assembly is aligned and located in reference to the press and the base tool, baseboard, and the connector orientation.

Step 4: Partially insert the connector pins into the baseboard holes

1. Under pre-load insert the connector pins into the baseboard hole pattern.
2. Ensure the connector in properly orientated, else the connector will not function properly from a mechanical or electrical standpoint. See Customer Drawings for the position of "Pin A1" reference location.
3. Ensure all pins are aligned with their respective PTHs and the tip of all connector to baseboard keying pins are below the top surface plane of the PCB.
4. Apply a pre-seating force adequate to ensure the connector does not become dislodged during any slight board movement.
5. Visually inspect each connector before actuating the press to ensure all pins have remained properly positioned inside the PTH.

Step 5: Press in the connector

- Lower the press head until it reaches the top surface (riser card side) of the connector. Continue lowering the press until the connector is seated flush on the PCB surface.

Step 6: Inspection

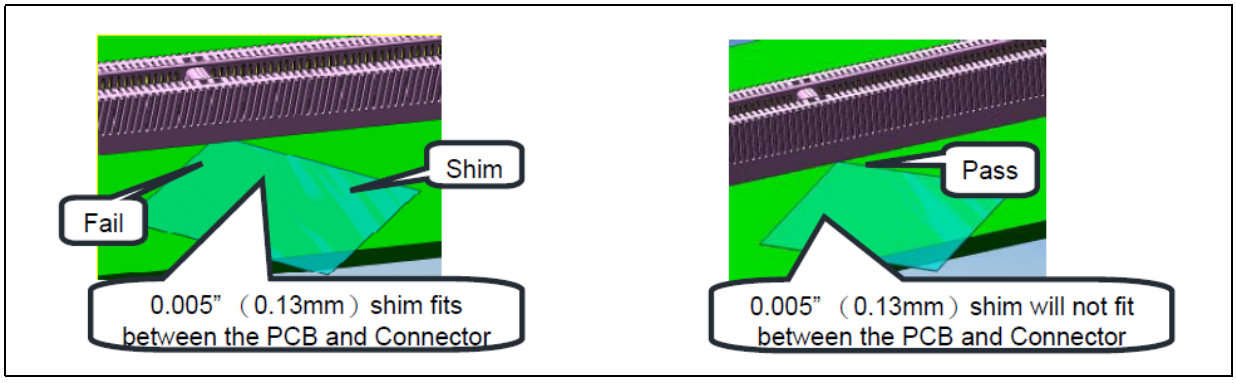
1. **Connector Position:**

- Verify the Connector is seating flush on the baseboard. The gap between the connector and the baseboard must be less than 0.13mm (0.005"). A gap of 0.13 mm (0.005") or greater between the PCB and connector is NOT acceptable.
- Verify the final seating depth of the connector using a 0.13 mm (0.005") shim. The shim should not fit between the surface of the PCB and the plastic insulator on the connector, as shown in Figure G-3.

2. **Quality:**

- Verify there are no cracks or deformities in the connector plastic. If possible view all pins from the backside of the board. Pin's end must be visible and pressed-in to the same height.

Figure G-3. Quality Inspection After Assembly



G.3 Rework

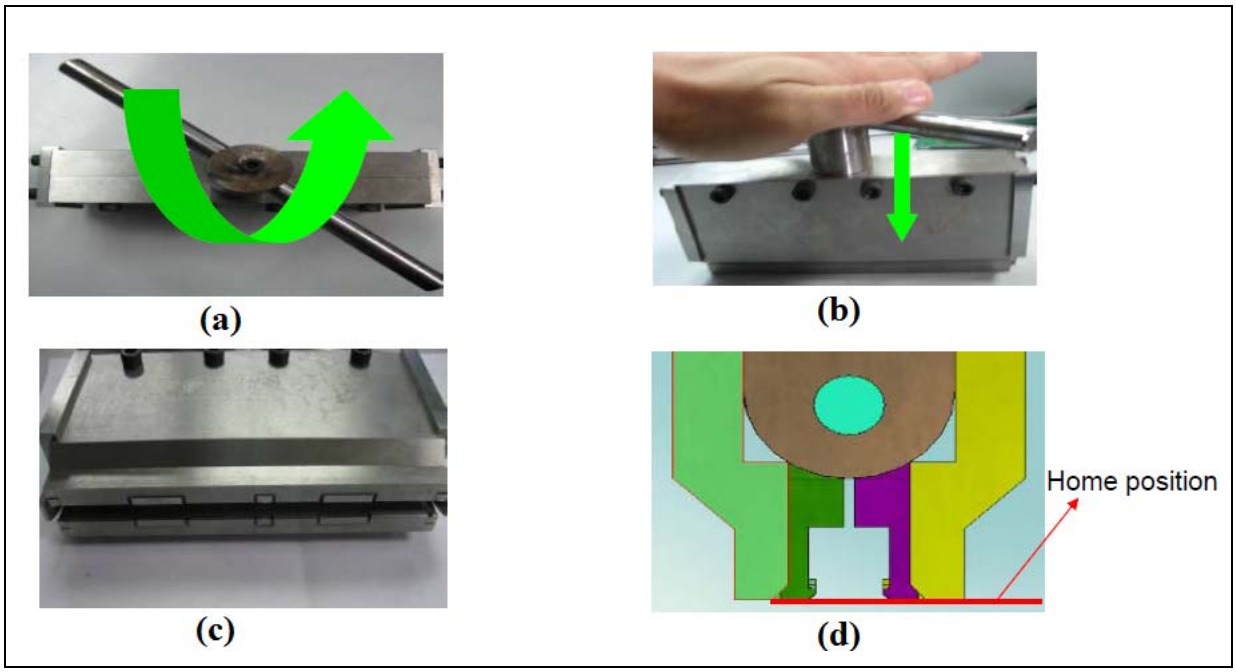
The connector rework tooling is used to remove the connector from baseboard. It consist of handle, shaft, left support, right support, screw, pulling, left clamp, right clamp, front guide, and back guide.

Following steps provide general instructions on using the rework tool to complete the connector removal from the baseboard.

Step 1: Verify the removal tool is at home position

- Open the removal tool by turning the handle counterclockwise as shown in picture (a), see Figure G-4. At the same time push the handle downwards as shown in picture (b) until the moveable parts are in the home position as shown in pictures (c) and (d).

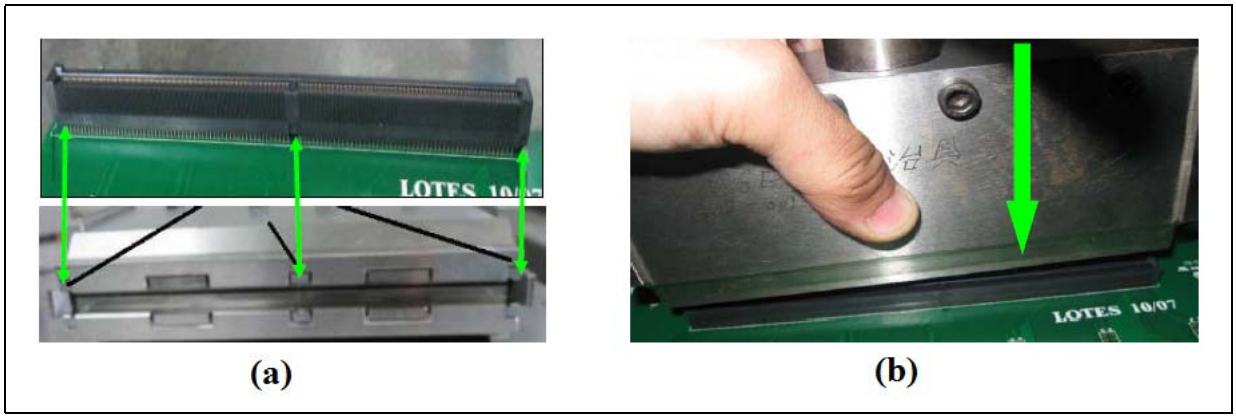
Figure G-4. Rework Tool Home Position



Step 2: Place the rework tool over the connector

1. Locate the defective connector which needs to be removed from the board.
2. Align and position the hook of the tool next to the notch of the connector as shown in (a) of Figure G-5.
3. Place the removal tool flat on the surface of the board and align with the defective connector as shown in (b) of Figure G-5.

Figure G-5. Rework Tool Placement



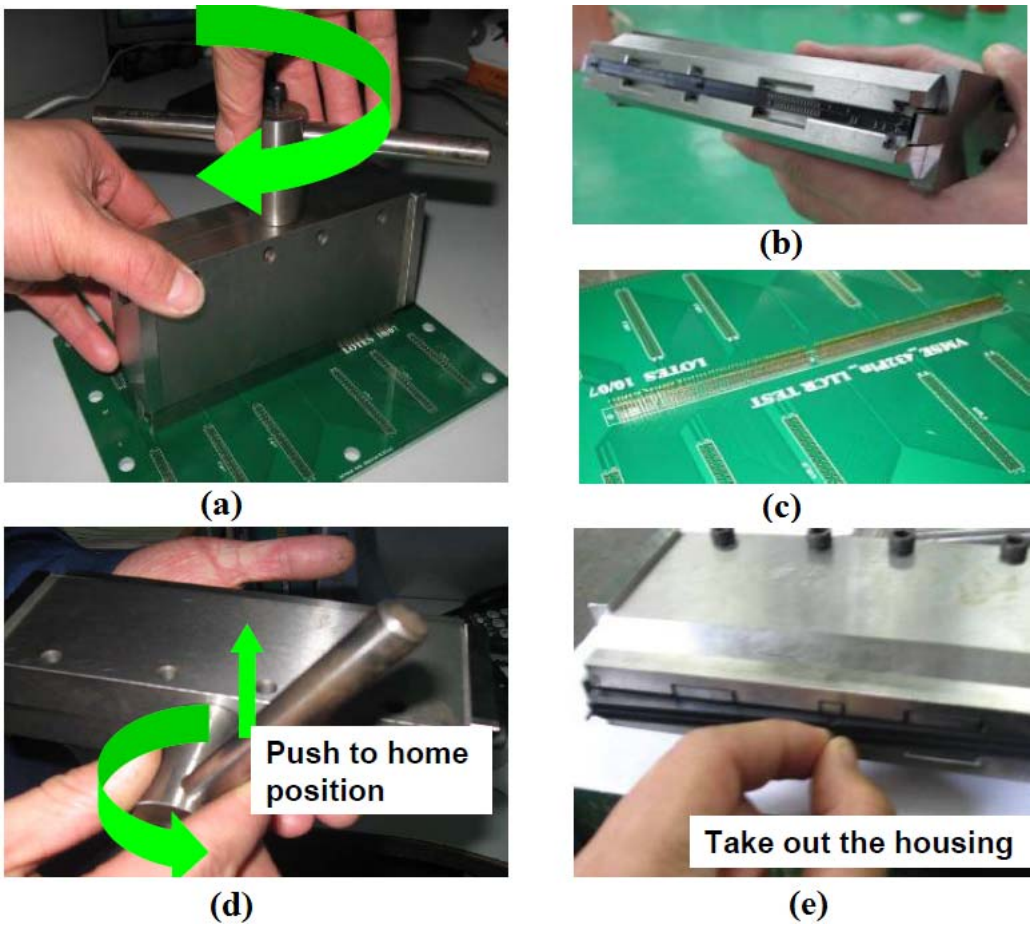
Step 3: Remove the connector plastic housing using the removal tool

Table G-2. Connector Pin Removal Force

Press Force	Value	Notes
Removal force	0.49 kgf/pin min	Force necessary to remove the connector pins from baseboard holes.

1. Hold the removal tool down tightly against the surface of the board with one hand. Slowly turn the handle clockwise with the other hand until the handle start to tighten and the connector housing begins to lift out of the board, see picture (a) in Figure G-6).
2. Continue to turn the handle until connector housing is completely removed from the board.
3. Lift the removal tool and the connector plastic housing away from the board.
4. Remove the connector plastic housing from the tool by turning the handle counter-clockwise, and push the moveable part to return to its home position as shown in picture (d) of Figure G-6.
5. Take out the housing as shown in picture (e) of Figure G-6.

Figure G-6. Removing Connector Housing



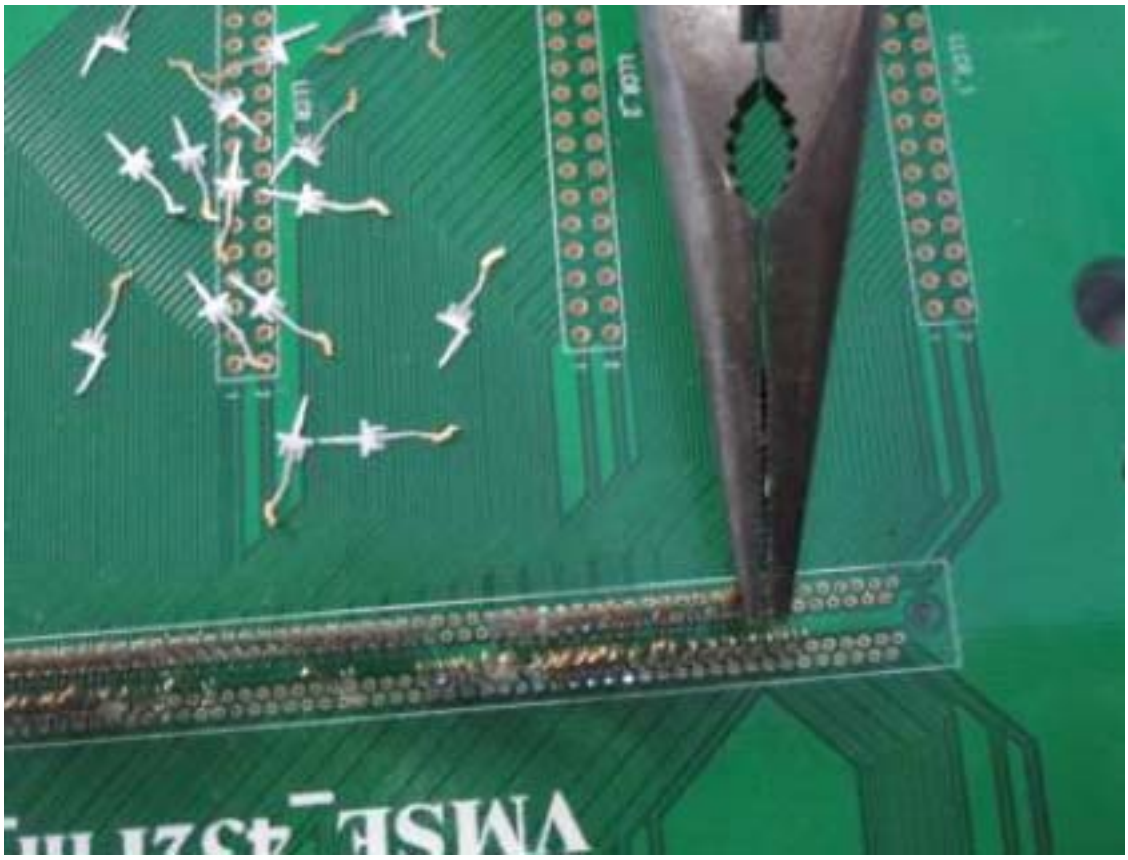
Step 4: Manually remove the remaining connector pins

- Some pins may remain in the board after the plastic housing and plastic insert are removed. These pins must be manually removed with needle nose pliers to complete the removal process.
- Use a pair of fine tipped needle nose pliers to extract the remaining pins one at a time.

Caution: Do not attempt to remove more than one pin at a time to prevent damaging the baseboard.

- Grasp the pin firmly and pull straight up as shown in Figure G-7. Check the pin and plated through hole to ensure the pin is fully removed, and the hole is clear.

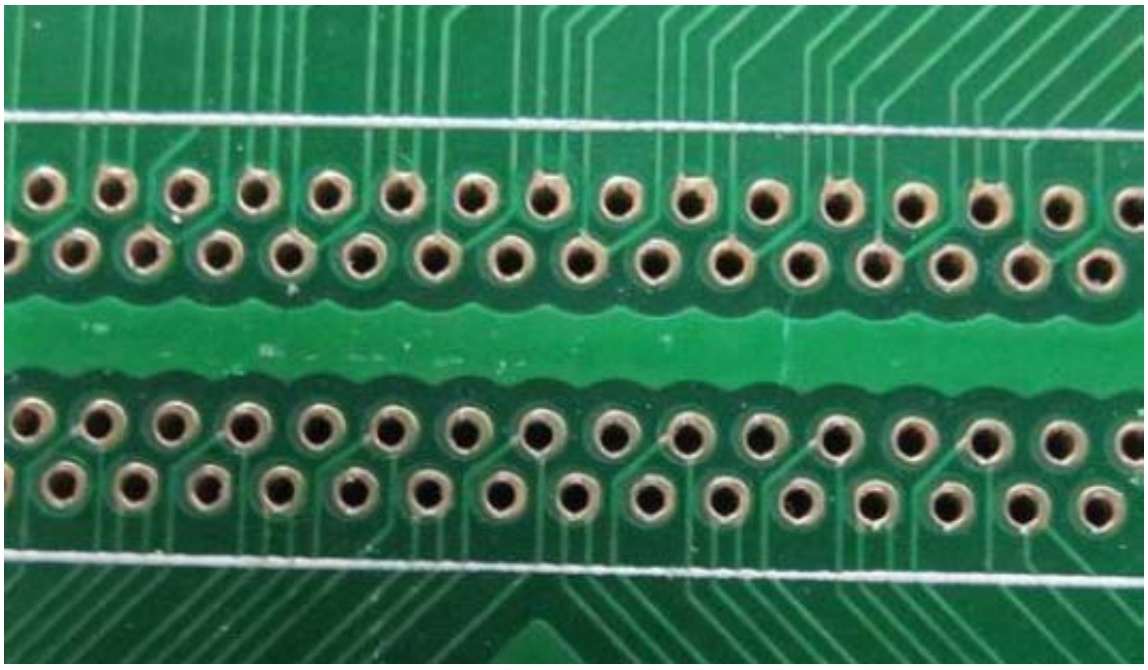
Figure G-7. Manual Pin Removal



Step 5: Final inspection

- After removing all pins using an optical magnifier visually inspect the plated through holes for damages and/or material left behind from the extraction process as shown in Figure G-8.

Figure G-8. Board Inspection Post Connector Removal Process



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