



Intel® IXDPG425 Network Gateway Reference Platform

Specification Update

July 2007



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Revision History

| Date | Revision | Description |
|-----------|----------|---------------------------------|
| July 2007 | 001 | Initial release of the document |

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1.0 Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation changes, and specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

This document may contain information that was not previously published.

1.1 Affected Documents/Related Documents

This document contains updates to the Intel® IXDPG425 Network Gateway Reference Platform and related documentation.

Refer to *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update* and *Intel® IXP400 Software Version 1.x Software Specification Update* for any updates related to the following documents:

- *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet*
- *Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual*
- *Intel® IXP400 Software Programmer's Guide*

| Title | Document Number |
|--|-----------------|
| <i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet</i> | 252479 |
| <i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual</i> | 252480 |
| <i>Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Specification Update</i> | 252702 |
| <i>Intel® IXP400 Software Programmer's Guide</i> | 252539 |
| <i>Intel® IXP400 Software Version 1.x Software Specification Update</i> | 273795 |

1.2 Nomenclature

Changes are design defects or errors. These may cause the Intel® IXDPG425 Network Gateway Reference Platform behavior to deviate from published specifications. Hardware and software designed to be used with any given board revision must assume that all changes documented for that board revision are present on all devices.

Specification Changes are modifications to the currently published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the currently published specifications. These will be incorporated in any new release of the specification.

Note: Changes remain in the specification update throughout the product's life cycle, or until a particular revision is no longer commercially available. Under these circumstances,



changes removed from the specification update are archived and available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (quick start guide, users' guides, and so on.).

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2.0 Summary Table of Changes

The following table indicates the changes, specification changes, specification clarifications, or documentation changes that apply to the Intel® IXDPG425 Network Gateway Reference Platform. Intel may fix some of the changes in a future revision of the component and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

2.1 Codes Used in Summary Table

2.1.1 Revision

X: Changes exists in the revision indicated. Specification Change or Clarification that applies to this revision.
 (No mark)
 or (Blank box): This erratum is fixed in listed revision or specification change does not apply to listed revision.

2.1.2 Page

(Page): Page location of item in this document.

2.1.3 Status

Doc: Document change or update will be implemented.
 Plan fix: This erratum may be fixed in a future revision of the component.
 Fixed: This erratum has been previously fixed.
 NoFix: There are no plans to fix this erratum.

2.1.4 Row

A change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

2.2 Changes

| Changes No. | Revision K1XDPG425A D/BD/.LF | Page | Status | Changes Detail |
|-------------|------------------------------------|------|--------|---|
| | B1 | | | |
| 1 | X | 9 | Fixed | HSS TX/RX Output Clock Jitter and Error Characterization Data |
| 2 | X | 9 | Fixed | Incorrect Reference Clock |

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3.0 Identification Information

3.1 Part Numbers

Table 1. Part Numbers

| Device | Part # | MM # |
|--|--------------|--------|
| Intel® IXDPG425 Network Gateway Reference Platform | KIXDPG425.LF | 885412 |

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4.0 Changes

1. HSS TX/RX Output Clock Jitter and Error Characterization Data

Problem: The High-speed serial (HSS) ports on the Intel® IXP4XX Product Line of Network Processors can be configured to generate an output clock on the HSS_TXCLK and HSS_RXCLK pins. The output clock generated by the HSS ports is based on the internal, 133.32 MHz AHB bus. This frequency does not divide down easily. Consequently, jitter and error may be introduced into the resultant HSS output clock causing inaccuracies.

Implication: If developers are clocking a framer, DAA, or other device with a sensitive input PLL, or time-critical application (for example, fax transmission), the inaccurate HSS clock can affect functioning of the time-sensitive application either partially or completely.

Workaround: External clocks can provide more stability and better accuracy than the HSS output clock and is recommended for time-critical applications. To implement the external clock, perform the following actions on Intel® IXDPG425 Network Gateway Reference Platform:

1. Add an external 2.048 MHz 50 ppm oscillator to OSC1
2. Add a 2-pin HEADER connector to connect pin1 and pin2 of CON5

Note: Software configuration of external/ internal clock must be changed according to the hardware implementation.

Status: Fixed.

2. Incorrect Reference Clock

Problem: Incorrect 33 MHz 50 ppm reference clock used on the Intel® IXDPG425 Network Gateway Reference Platform. The Intel® IXP4XX Product Line of Network Processors require a reference clock of 33.33 MHz 50 ppm instead of 33 MHz 50 ppm.

Implication: Depending on customer's application, using a reference clock with a frequency other than 33.33 MHz may lead to the following - internal peripheral (for example, expansion bus or PCI bus) clock may not generate the desired clock frequency, and affect functioning of the connected devices either partially or completely.

Workaround: None.

Status: Fixed.

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