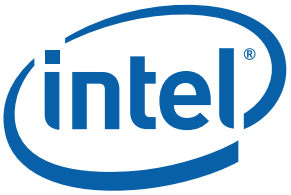


Intel® C102/C104 and C112/C114 Scalable Memory Buffer

Specification Update

April 2017

Notice: The Intel® C102/C104 and C112/C114 Scalable Memory Buffer may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are available upon request.

Reference Number: 332445-002

Contents

Revision History

Version	Description	Date
001	Initial Release	June 2015
002	Added erratum 6	April 2017

Preface

This document is an update to the specifications contained in the Affected Documents table below. This document is a compilation of device errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Affected Documents

Document Title	Document Number
Intel® C102/C104 Scalable Memory Buffer Datasheet	330032-001
Intel® C112/C114 Scalable Memory Buffer Datasheet	332444-001

Nomenclature

S-Spec Number is a five-digit code used to identify products as described in the Intel® C102/C104 and C112/C114 Scalable Memory Buffers identification information table. Read all notes associated with each S-Spec number.

Errata are design defects or errors. These may cause the Intel® C102/C104 and C112/C114 Scalable Memory Buffers to deviate from published specifications. Hardware and Software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the products lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specifications or user documentation (datasheets, manuals and so forth).

Identification Information

Component Identification via Programming Interface

The Intel® C102/C104 Scalable Memory Buffer stepping can be identified by the following table of register contents.

Stepping	Features	Vendor ID	Device ID	Revision ID
C1	Production	8086h	0883h	21h

The Intel® C112/C114 Scalable Memory Buffer stepping can be identified by the following table of register contents.

Stepping	Features	Vendor ID	Device ID	Revision ID
D1	Production	8086h	0883h	31h

Component Marking Information

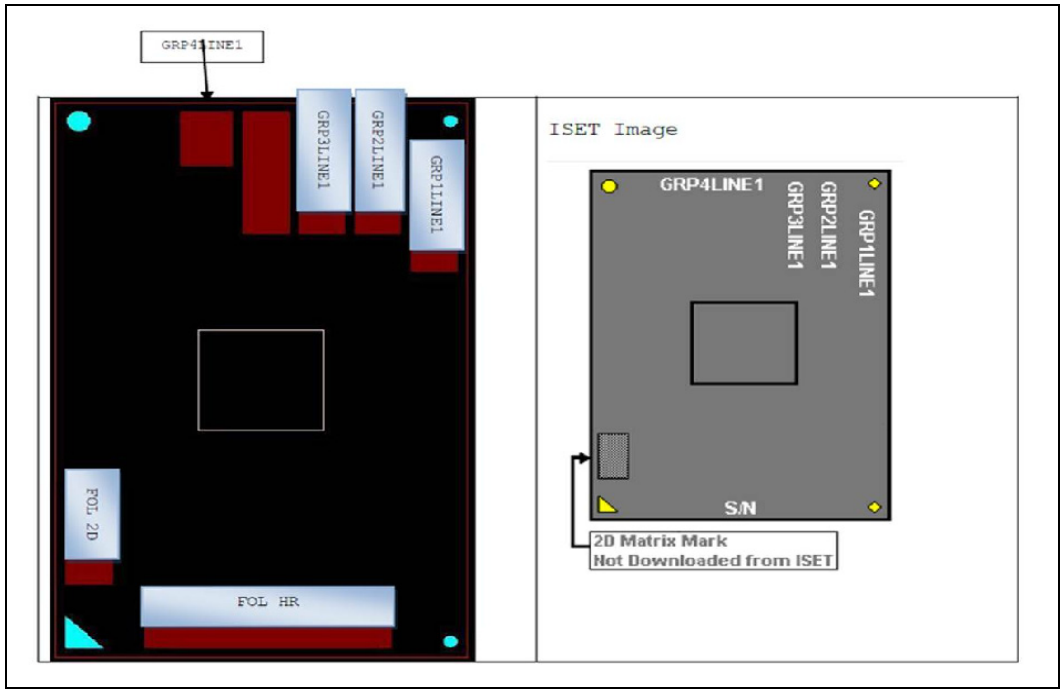
The Intel® C102/C104 Scalable Memory Buffer stepping can be identified by the following table of component markings.

SKU	GRP1LINE1	GRP2LINE1	GRP3LINE1	GRP4LINE1
Intel® C102	date code in the form of i{M}{C}YY	FPO	SLK4Q	{eX}
Intel® C104	date code in the form of i{M}{C}YY	FPO	SLK4P	{eX}

The Intel® C112/C114 Scalable Memory Buffer stepping can be identified by the following table of component markings.

SKU	GRP1LINE1	GRP2LINE1	GRP3LINE1	GRP4LINE1
Intel® C112	date code in the form of i{M}{C}YY	FPO	SLKHU	{eX}
Intel® C114	date code in the form of i{M}{C}YY	FPO	SLKHV	{eX}

Figure 1. Intel® C102/C104 and C112/C114 Scalable Memory Buffer Markings



Note:
1. Pin 1 orientation is in the lower left corner.

Summary Table of Changes

The table indicates the errata that apply to the Intel® C102/C104 and C112/C114 Scalable Memory Buffers. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted.

Definitions are listed below for terminology used in the Errata Summary.

Affected Stepping Column

X: Erratum exists in the stepping indicated.

Blank: This sighting is fixed, or does not exist, in the listed stepping.

Status Column

No Fix: There are no plans to fix the erratum.

Plan Fix: The erratum may be fixed in a future stepping of the product.

Fixed: The erratum has been previously fixed.

Doc: Documentation change or update will be implemented.

Non-Si: This issue is not due to a erratum in the Intel® C102/C104 or C112/C114 Scalable Memory Buffers.

Change Bar

Change bar on outside margins indicates this erratum is either new or modified from a previous version of the document.

Errata Summary

Errata Table

Number	Stepping		Status	Description
	C-1	D-1		
1	X	X	No Fix	LAI trigger sequence is not working as expected for TRIG[2:1].
2	X	X	No Fix	EVENTCNT field does not log the occurrence of a event correctly.
3	X	X	No fix	At power up, voltage leakage may be observed on VCCADDRDLL (1.5V) and VCCAVMSEIO (1.35V) rail.
4	X		No Fix C-1 Fixed D-1	A single bit flip in least significant bit of the spare device may not be detected when using lockstep with x4 DRAMs
5		X	N/A C-1 No Fix D-1	Southbound CRC Errors may cause ECC errors for DIMMs in slot B
6		X	N/A C-1 No Fix D-1	Command Address Parity errors may not get injected on the Intel® Xeon® Processor E7 v4 Product Family

Specification Changes - Summary

Specification Changes

Number	Doc Revision				Description
	1.0				
NA					

Specification Clarification - Summary

Specification Changes

Number	Doc Revision				Description
	1.0				
NA					

Documentation Changes - Summary

Specification Changes

Number	Doc Revision				Description
	1.0				
NA					

Errata

1. LAI trigger sequence is not working as expected for TRIG[2:1].

Problem: Four level trigger sequencer is not functioning for TRIG[2:1].

Implication: Support for four level trigger sequencer is limited to TRIG[0] only. Up to 3 level trigger sequencer is supported on TRIG[1] and up to two level trigger sequencer is supported on TRIG[2].

Workaround: None identified.

Status: No Fix. For the steppings affected, see the Errata Summary.

2. EVENTCNT field does not log the occurrence of a event correctly.

Problem: EVNETCNT field (bit 16) in EVENT[3:0] CSR (offset 47Ch, 478h, 474h, 470h) is expected to be set when a programmable number of event(s) (offset 4EA, 4E8h) have occurred. Due to the errata, the EVNETCNT field is set upon the occurrence of the first event and not when the programmed number of events have occurred.

Implication: The issue impacts the ability to log the occurrence of the event. It does not impact the ability to trigger the LAI upon the occurrence of programmable number of events.

Workaround: None identified.

Status: No Fix. For the steppings affected, see the Errata Summary.

3. At power up, voltage leakage may be observed on VCCADDRDLL (1.5V) and VCCAVMSEIO (1.35V) rail.

Problem: When the VCCDCORE_1P0 (1V) rail powers up a voltage leakage of about 700 mV may be observed on 1.5V rail and about 125 mV on 1.35V rail.

Implication: The observed leakage levels are not expected to cause any functional issues.

Workaround: None.

Status: No fix. For the steppings affected, see the Errata Summary.

4. A single bit flip in least significant bit of the spare device may not be detected when using lockstep with x4 DRAMs

Problem: When Intel® C102/C104 Scalable Memory Buffer is using lockstep with x4 DRAMS, the least significant bit of the unused spare device data on the Intel® Scalable Memory Interconnect (Intel® SMI) 2 or DDR interfaces is not correctly used for error detection.

Implication: When using lockstep with x4 DRAMS (DDDC mode), errors (either transient or hard errors) on the least significant bit of the unused spare device data on Intel® SMI2 or DDR interfaces will not be detected and logged by Intel® C102/C104 Scalable Memory Buffer. Southbound Intel® SMI2 link errors affecting only this specific bit will get stored in DRAM. However, a successful read of the data will result in correction by the processor memory controller. An error on this particular bit will appear to be a Intel® SMI2 northbound error regardless of origin. If another error affects the same cache line before the cache line is scrubbed by patrol scrub, an uncorrectable error may occur. The occurrence of this sequence of events is expected to be rare.

Workaround: None.

Status: For the steppings affected, see the Errata Summary.

5. Southbound CRC Errors may cause ECC errors for DIMMs in slot B

Problem: When running in 2:1 mode at 3200MT/s, southbound CRC errors may cause the slot B DIMMs to experience ECC errors

Implication: For error injection testing, the injection rate will have to be limited

Workaround: Limiting southbound error injection to a rate of 1/second eliminates this issue

Status: No Fix. For the steppings affected, see the Errata Summary.

6. Command Address Parity errors may not get injected on the Intel® Xeon® Processor E7 v4 Product Family

Problem: With DDR4 DIMMs in 3DPC configuration, Command Address Parity errors may not be injected correctly on the Intel® Xeon® Processor E7 v4 Product Family platforms.

Implication: Command Address Parity error injection cannot be tested in 3DPC configuration. Command Address Parity error detection and correction can be tested successfully on 2DPC or 1DPC configuration in this case.

Workaround: None.

Status: No Fix. For the steppings affected, see the Errata Summary.

Specification Changes

This section documents changes to the Intel® C102/C104 and C112/C114 Scalable Memory Buffer datasheets.

Specification Clarifications

This section documents clarifications to the Intel® C102/C104 and C112/C114 Scalable Memory Buffer datasheets.

Documentation Changes

This section documents any potential changes that will be made to the next revision of the Intel® C102/C104 and C112/C114 Scalable Memory Buffer datasheets.

§