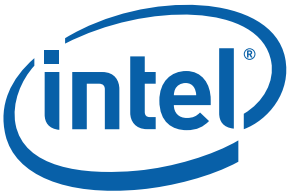

Intel® 7510/7512 Scalable Memory Buffer

Specification Update

June 2013

Document Number: 325123-002

Notice: This document contains information on products in the design phase of development. The information here is subject to change without notice. Do not finalize a design with this information.

Contents

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Revision History

Document number	Revision number	Description	Date
325123	001	Initial release of the document.	April 2011
325123	002	Added erratum 5.	June 2013

Preface

This document is an update to the specifications listed in the *Affected documents* table below. This document is a compilation of device and documentation errata, specification clarifications, and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in *Nomenclature* are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected documents

Document title	Document number/location
Intel® 7500/7510/7512 Scalable Memory Buffer Datasheet	322824 on *www.intel.com* *https://www-ssl.intel.com/content/dam/doc/datasheet/7500-7510-7512-scalable-memory-buffer-datasheet.pdf*

Related documents

Document title	Location
Advanced Memory Buffer -- Generation 2 FB-DIMM2 Circuit Architecture Specification	
Intel® FBD2 Host Interface Specification	
JESD79-3 DDR3 SDRAM Specification	JEDEC

Nomenclature

S-Spec Number. This is a five-digit code used to identify products. Products are differentiated by their unique characteristics (for example, core speed, L3 cache size, package type, etc.) as described in the processor identification information table. Read all notes associated with each S-Spec number.

Known Sample Issues. These are design defects or errors. These may cause the processor behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all Known Sample Issues documented for that stepping are present on all devices.

Sightings. These are anomalies seen during system and component validation. At this time, the cause of these anomalies may not be known. Please note that Sightings may not be Known Sample Issues.

Errata. These are design defects or errors. These may cause the Intel® 7510/7512 Scalable Memory Buffer's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification changes. These are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification clarifications. These describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation changes. These include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the Specification Update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and will be available upon request. Specification changes, specification clarifications, and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, and so forth).

Summary Table of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 7510/7512 Scalable Memory Buffer. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables use the following notations.

Codes used in summary tables

Stepping

X: An "X" in the stepping columns indicates the sighting exists in the stepping indicated. Specification change or clarification that applies to this stepping.

Blank: This sighting is fixed in listed stepping or specification change does not apply to the listed stepping.

Platform

X: An "X" in the processor columns indicates the sighting exists in this platform. Refer to the table footnotes for specific processor families.

Blank: This sighting does not apply to the platform.

Status

Doc: Document change or update will be implemented.

Plan Fix: This sighting may be fixed in a future stepping of the product. Plan Fix (HW) indicates that the fix will be implemented in silicon.

Fixed: This sighting has been fixed.

No Fix: There are no plans to fix this sighting.

Spec Change: Root caused to a specification error that will be updated.

Under Investigation: The disposition of this sighting has not been determined. An "Under Investigation" status will be updated in a future release of this document.

Not Reproducible: The sighting could not be reproduced after it was reported.

Third Party: Root caused to a board, software, driver, BIOS, or third-party silicon issue.

Change Bar

A change bar in the margin indicates a sighting that is either new or modified from the previous version of the document.

Errata Summary

Table 1. Errata summary table

#	Stepping		Status	Processor		Errata
	A0	A1		Note [1]	Note [2]	
1.	X	X	No Fix		X	*On Intel® 7510/7512 Scalable Memory Buffer, JTAG - BScan EXTEST is noncompliant to 1149.1 specification (uses wrong clock edge).*
2.	X	X	No Fix		X	*During an Intel® SMI Disable_b event, SMBus transactions underway between bus Master and another device on the bus other than Intel® 7510/7512 Scalable Memory Buffer may be affected.*
3.	X	X	No Fix		X	*Broken trace to either the P or the N lane of the Intel® SMI forwarded clock differential pair may result in loss of forwarded clock but not always lead to clock lane failover.*
4.	X	X	No Fix		X	*Under cold operating conditions, manufacturing stress tests reveal issues with Intel® 7510 Scalable Memory Buffer (standard SKU; maxTDP=8.7W) S-Spec parts.*
5.	X	X	No Fix		X	*BIOS Command clock training algorithm may fail to find a failing window when populated in a minimum memory configuration with one DDR channel unpopulated.*

1. Intel® Itanium® processor 9300 series-based platform.
2. Intel® Xeon® processor E7-8800/4800/2800 product families.

Identification Information

Component identification via programming interface

The **Intel® 7510/7512 Scalable Memory Buffer** stepping can be identified by the following register contents:

Stepping	Features	Vendor ID	Device ID	Revision number
A1	Engineering Sample 2	8086h	0881h	01h

Component marking information

The **Intel® 7510 Scalable Memory Buffer** stepping can be identified by the following component markings:

Stepping	Top marking	Notes
A1	BD82030M2	MM#: 908098
A1	BD7510	MM#: 910394

The **Intel® 7512 Scalable Memory Buffer** stepping can be identified by the following component markings:

Stepping	Top marking	Notes
A1	BD82029M2	MM#: 908099
A1	BD7512	MM#: 910395

Errata

1. On Intel® 7510/7512 Scalable Memory Buffer, JTAG - BScan EXTEST is noncompliant to 1149.1 specification (uses wrong clock edge).

Problem: As per the JTAG 1149.1 specification, "test data registers enabled to drive data off-chip shall be designed such that component outputs change only on the **falling** edge of TCK after entry to the Update-DR, Update-IR, Run-Test/Idle, or Test-Logic-Reset controller state as a result of signals applied to TCK and TMS". Intel® 7510/7512 Scalable Memory Buffer is in violation of this specification.

Implication: On Intel® 7510/7512 Scalable Memory Buffer, while performing DFx Boundary Scan (EXTEST), system pins (including DDR, Intel® Scalable Memory Interconnect (Intel® SMI), and miscellaneous IOs) are transmitted on the **rising** TCK edge (instead of falling TCK edge).

Workaround: If using automated test equipment to sample the output data when executing EXTEST, the test must wait for the rising edge of TCK before sampling the values being driven on the Intel® 7510/7512 Scalable Memory Buffer output pins.

Status: No Fix.

2. During an Intel® SMI Disable_b event, SMBus transactions underway between bus Master and another device on the bus other than Intel® 7510/7512 Scalable Memory Buffer may be affected.

Problem: Intel® 7510/7512 Scalable Memory Buffer EDS (rev 1.9) states that SMBus transactions to the memory buffer that are underway during an Intel® SMI Disable_b event may not complete normally. In addition, SMBus transactions under way to devices other than Intel® 7510/7512 Scalable Memory Buffer may also be affected. For example, a transaction under way to a DIMM Thermal Sensor (TS) during a Disable_b event may result in Intel® 7510/7512 Scalable Memory Buffer interpreting the SMBus transaction as targeting that memory buffer. If this occurs, Intel® 7510/7512 Scalable Memory Buffer can mistakenly drive the SMBus, even though it is not the target device.

Implication: Disable_b events can occur as a result of a CRC error handling routine, or as part of the Intel® SMI link-down memory self-refresh power saving mode. Under this specific error event, Intel® 7510/7512 Scalable Memory Buffer can drive SMBus for one or more clocks, resulting in corruption of the transaction in progress. If the transaction results in data corruption and has Parity Error Checker (PEC) enabled, the error will be detected by the master or slave, and then the transaction can be retried. If PEC is not enabled, then some other mechanism will be needed to ensure integrity of the transaction. It is also possible that the transaction request will time out.

Workaround: At Intel, this sighting was observed when continuously polling the DIMM Thermal Sensor (TS) as part of fan speed control mechanism. The observed failure rate was very low for this specific usage model. In this case, as a workaround, a modified algorithm can perform multiple reads and filter "outlier values" before consuming the data. On usage models that involve SMBus writes, a read-after-write from the same target address would be needed to confirm the integrity of the write data. We do not recommend Block Read/Write transactions (for example, to DIMM SPD for error logging) since large data transfers create a probability that a specific pattern could occur which matches Intel® 7510/7512 Scalable Memory Buffer's target address followed by a write command, and could be consumed by Intel® 7510/7512 Scalable Memory Buffer. We have not observed this at Intel, but it is a theoretical possibility. Limiting SMBus transfers to less than 8 bytes between Start/Stop bits, eliminates this possibility. (DIMM Thermal Sensor polling is a 5-byte SMBus transaction.)

Workarounds are dependent on customer-specific usage models. Customers will likely want to test their own transaction corruption rate. Customers should work with Intel to implement workarounds for other usage models.

Status: No fix.

3. Broken trace to either the P or the N lane of the Intel® SMI forwarded clock differential pair may result in loss of forwarded clock but not always lead to clock lane failover.

Problem: If either only the P or the N lane of the Intel® SMI forwarded clock is broken, then Intel® 7510/7512 Scalable Memory Buffer is capable of detecting minimum differential swing on the clock lane, thus resulting in the memory buffer to assume that the forwarded clock still exists. Consequently, Intel® 7510/7512 Scalable Memory Buffer will proceed to the Intel® SMI link training phase.

Implication: If Intel® 7510/7512 Scalable Memory Buffer proceeds to the link training phase, then based on observations, it is possible that the Intel® SMI link may fail to train even after seven retry attempts and continue to remain in RESET state; or, if the link successfully reached L0 state, then the link may be unstable and shortly return to Disable_a state. However, if the P and N lanes of the forwarded clock differential pair are both broken due to board trace issues, then the clock failover mechanism on Intel® SMI channel has been found to operate successfully as expected.

Workaround: None exists at the moment.

Status: No Fix.

4. Under cold operating conditions, manufacturing stress tests reveal issues with Intel® 7510 Scalable Memory Buffer (standard SKU; maxTDP=8.7W) S-Spec parts.

Problem: Under cold temperature (<10°C) and low Vcc1P1 (~1.087 V) settings during manufacturing testing, Intel® 7510 Scalable Memory Buffer S-Spec parts have been observed to cause system issues. Symptoms appear as northbound or southbound CRC errors while attempting to boot OS. Not all Intel® 7510 Scalable Memory Buffer S-Spec parts cause these system issues. Additionally, operating condition must include both cold temperature and low Vcc1P1.

Implication: Intel® 7510 Scalable Memory Buffer Qualification samples do not exhibit this problem. Additionally, it is not possible to identify which Intel® 7510 Scalable Memory Buffer S-Spec parts may cause this problem under cold operating and low Vc1P1 conditions. As a result, a system using Intel® 7510 Scalable Memory Buffer S-Spec parts is at risk of running into OS boot-up issues.

Workaround: To avoid running into the cold socket issue with production units, the workaround consists of two steps, both being required:

1. Minor change in the MRC, starting with RC1.9.
2. Raising by 10 mV the specification of the digital and analog 1.1 V rail inputs to the Intel® 7510 Scalable Memory Buffer.

Note: Intel® 7512 Scalable Memory Buffer (low power SKU; maxTDP = 6.5 W) is not exposed to this issue; hence there is no change to 1.1 V input specification for Low Power SKU.

Status: No silicon fix.

5. BIOS Command clock training algorithm may fail to find a failing window when populated in a minimum memory configuration with one DDR channel unpopulated.

Problem: When operating in a minimum memory configuration with one channel unpopulated in a 2 DIMM per channel design, some Intel® 7510/7512 Scalable Memory Buffer parts may fail to find a failing window during command clock training. This occurs when BIOS sweeps the clock during command training and no eye edge is found. Additional loading (as occurs when a second DIMM is added) is usually sufficient to create signal delays (for example, on CAS) so that the training algorithm can now identify an eye edge.

Implication: The memory will be mapped out and the system will not boot.

Workaround: Add memory to the second DDR channel.

Status: No Fix.

Documentation Changes/ Clarifications

1. Intel® 7510/7512 Scalable Memory Buffer behavior in the event of loss of southbound forwarded clock during Disable_a state.

Intel® 7510/7512 Scalable Memory Buffer cannot tell the difference between a southbound forwarded clock failure due to signal integrity issues, and the deliberate use of the Intel® SMI Disable_a state for power management by the host memory controller. After the SB forwarded clock is stopped by the host, Intel® 7510/7512 Scalable Memory Buffer will flag an error in FERR/NERR.SBFWDCLK, if EMASK.SBFWDCLK is set to 0. If the Intel® SMI Disable_a state is used for power management, it is up to the host to mask this error, clear this error, or ignore this error.

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