IDF14

14 nm Process Technology: Opening New Horizons

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Intel Senior Fellow
Logic Technology Development

SPCS010

intel

Agenda

- Introduction
- 2nd Generation Tri-gate Transistor
- Logic Area Scaling
- Cost per Transistor
- Product Benefits
- SoC Feature Menu

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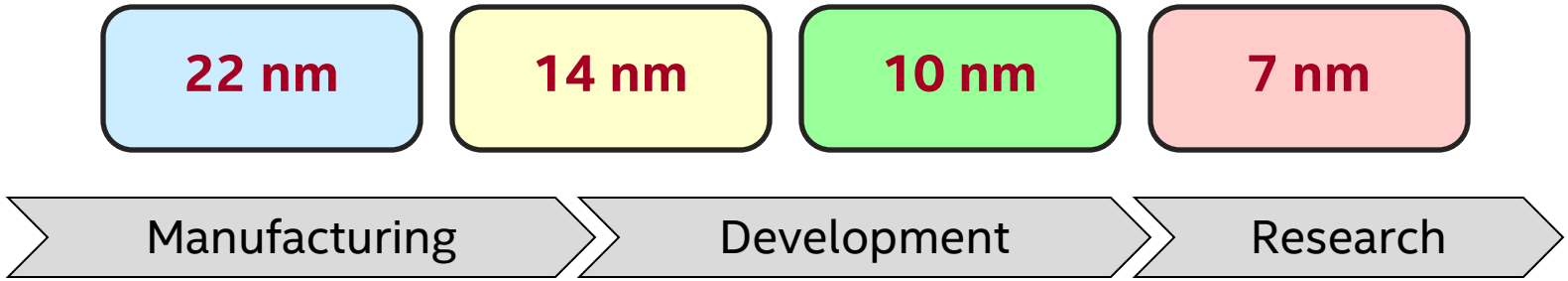
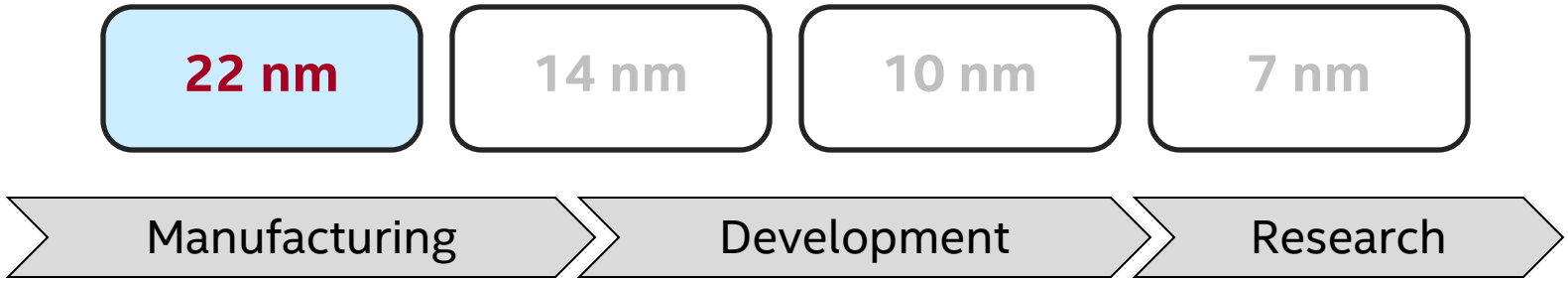
Intel Technology Roadmap

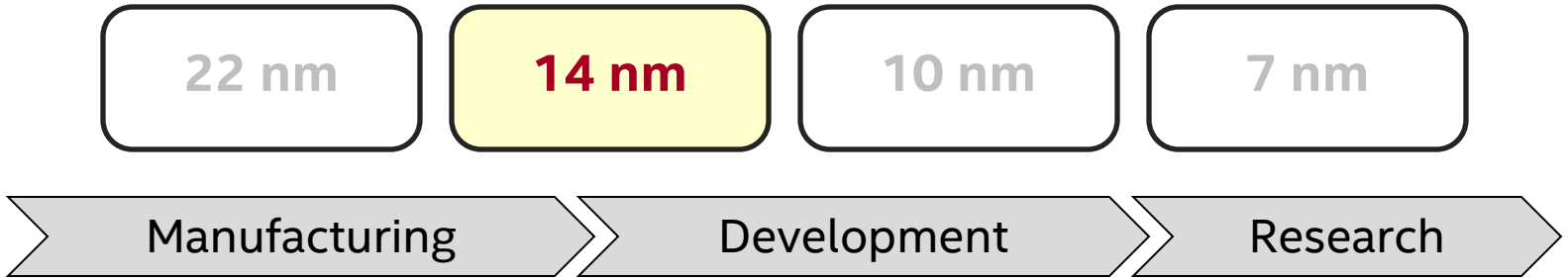


Intel Technology Roadmap



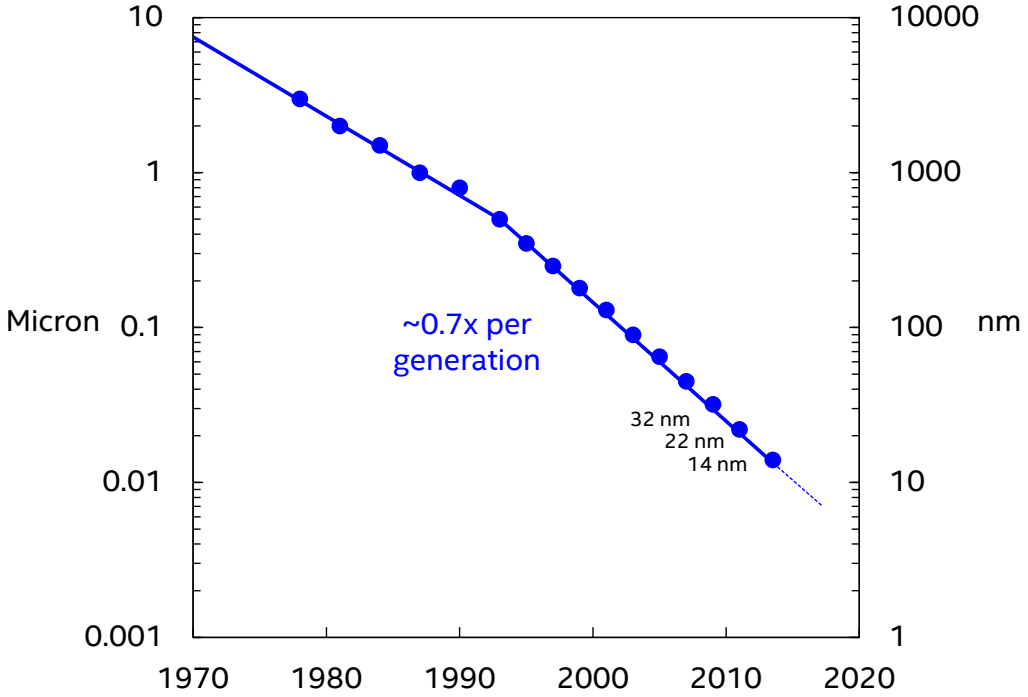
>500 million chips using 22 nm Tri-gate (FinFET) transistors shipped to date

Intel Technology Roadmap



Industry's first 14 nm technology is now in volume manufacturing

Intel Scaling Trend

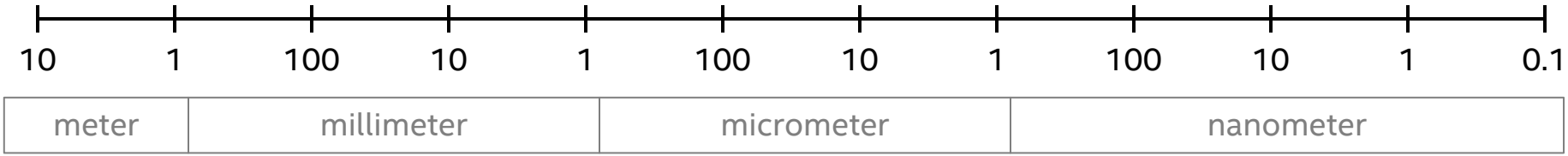


Scaled transistors provide:

- Higher performance
- Lower power
- Lower cost per transistor

Moore's Law continues!

How Small is 14 nm?



How Small is 14 nm?

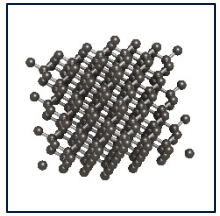
Mark
1.66 m

Fly
7 mm

Mite
300 um

Blood Cell
7 um

Virus
100 nm



Silicon Atom
0.24 nm

10 1 100 10 1 100 10 1 100 10 1 0.1

meter	millimeter	micrometer	nanometer

How Small is 14 nm?

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300 um

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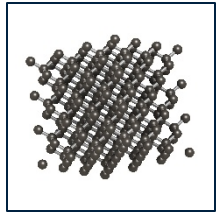
Virus
100 nm

14 nm
Process



Silicon Atom
0.24 nm

10 1 100 10 1 100 10 1 100 10 1 0.1

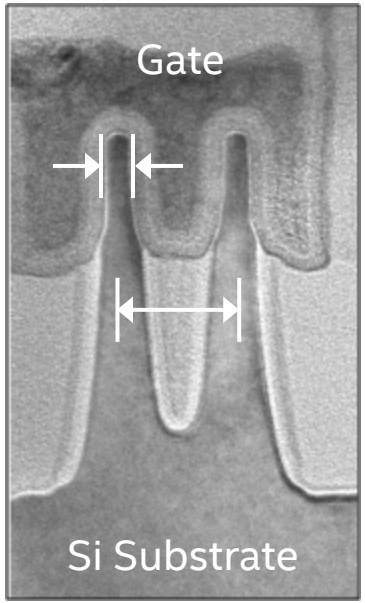
meter | millimeter | micrometer | nanometer

Very small

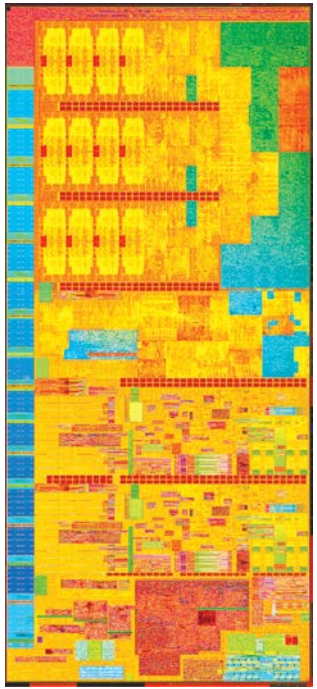
14 nm Tri-gate Transistor Fins

8 nm Fin Width

42 nm Fin Pitch



14 nm Intel® Core™ M Processor



1.3 billion transistors

82 mm^2 die size

Industry's first 14 nm processor now in volume production

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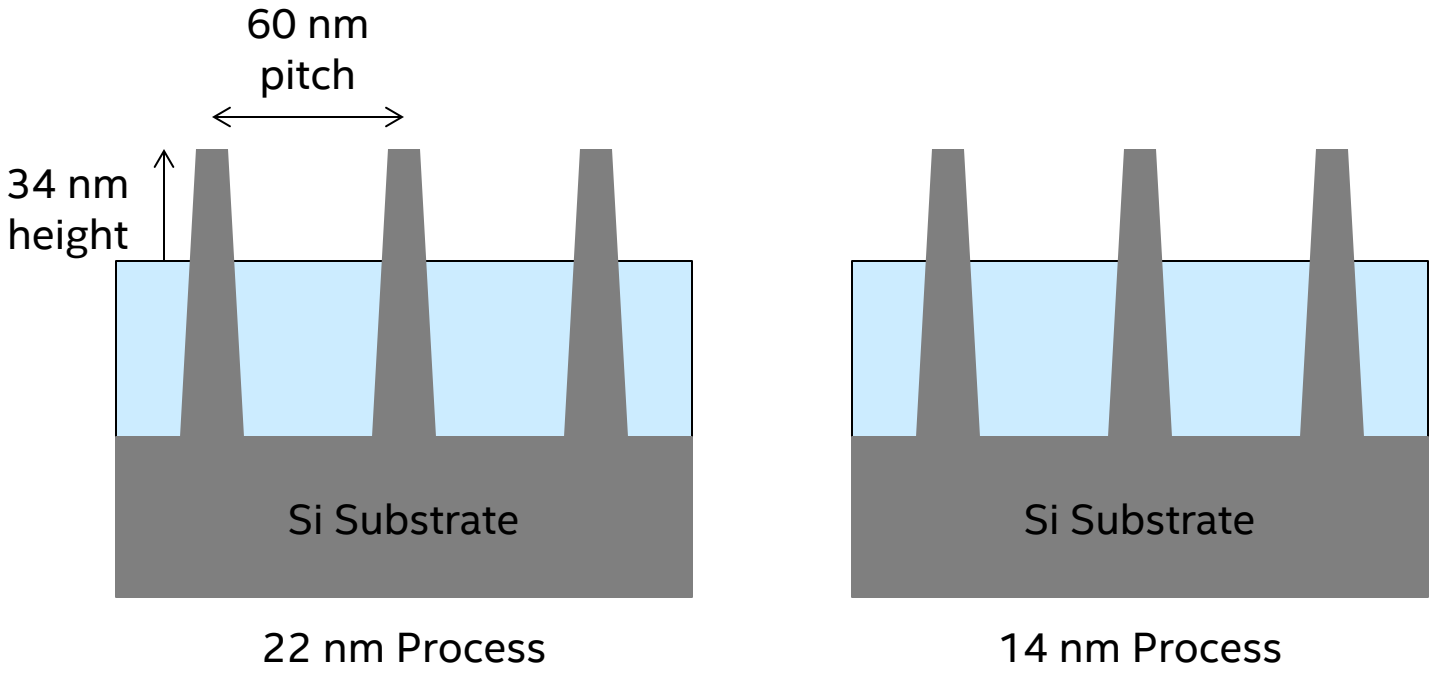
Minimum Feature Size

	22 nm	14 nm	Scale
Transistor Fin Pitch	60	42	.70x
Transistor Gate Pitch	90	70	.78x
Interconnect Pitch	80	52	.65x
	nm	nm	

Intel has developed a true 14 nm technology with good dimensional scaling

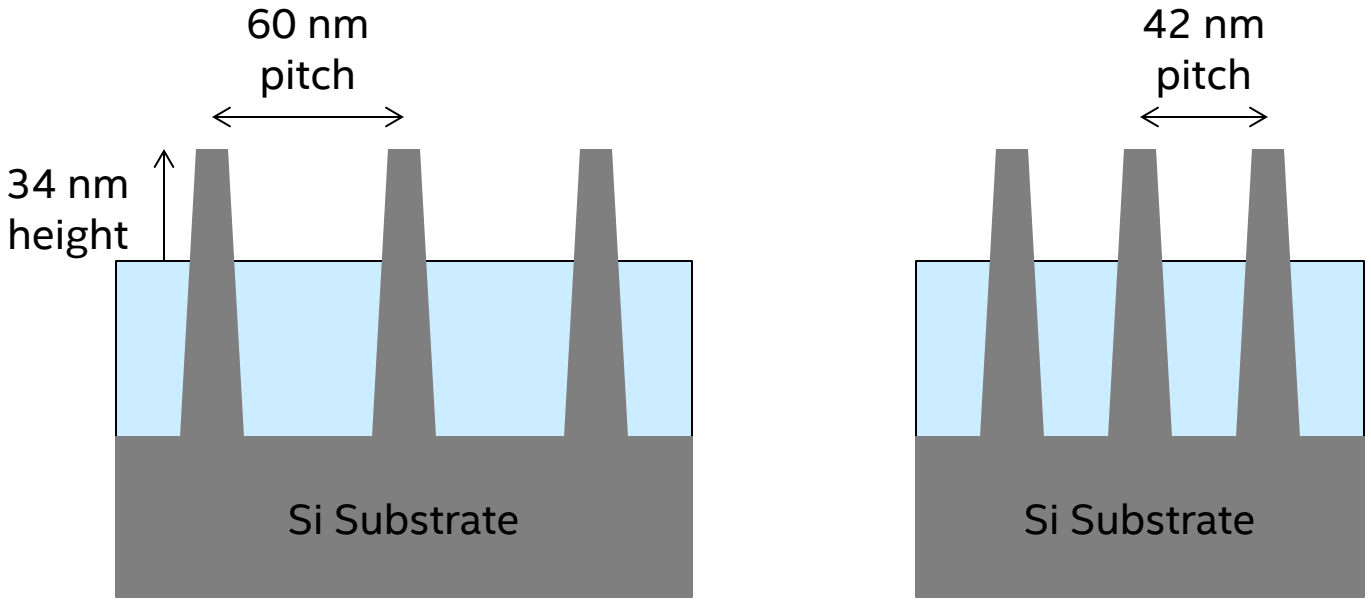
Transistor Fin Optimization



22 nm Process

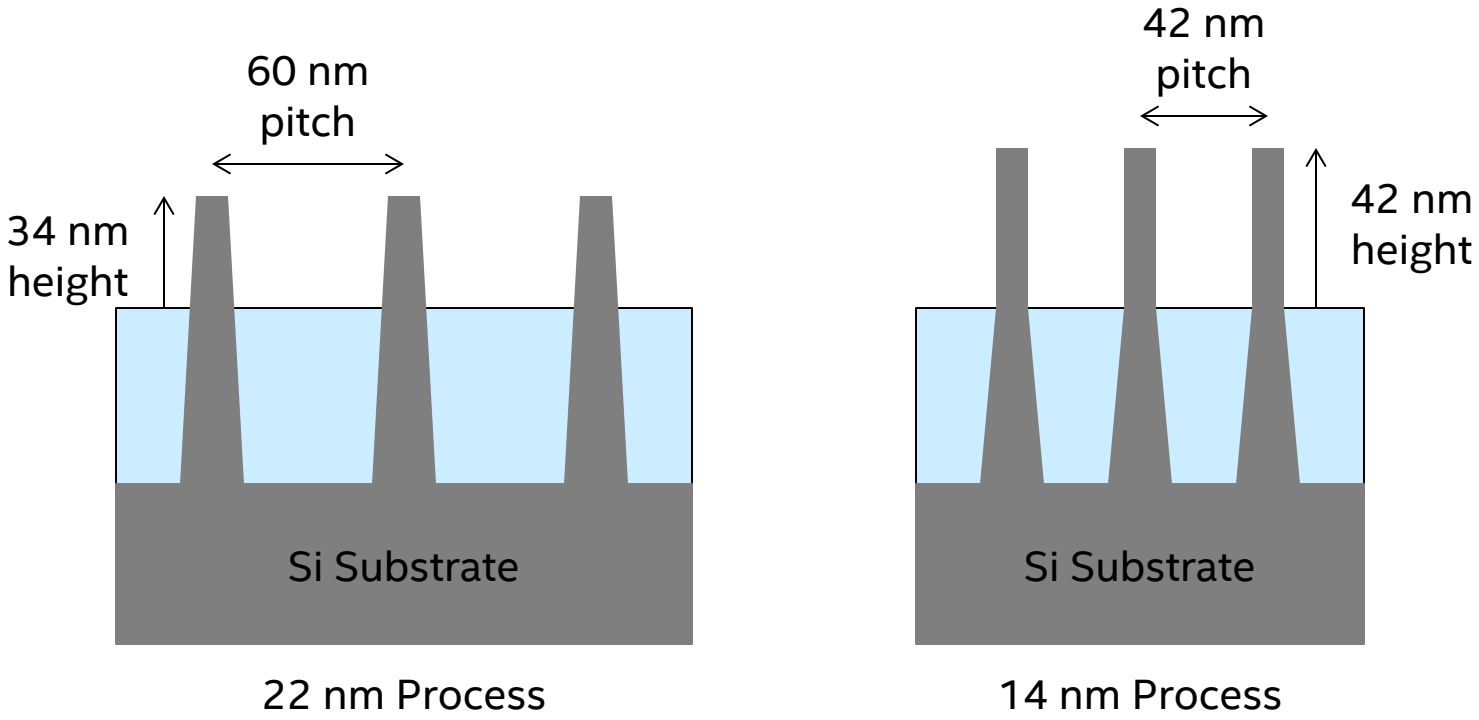
14 nm Process

Transistor Fin Optimization



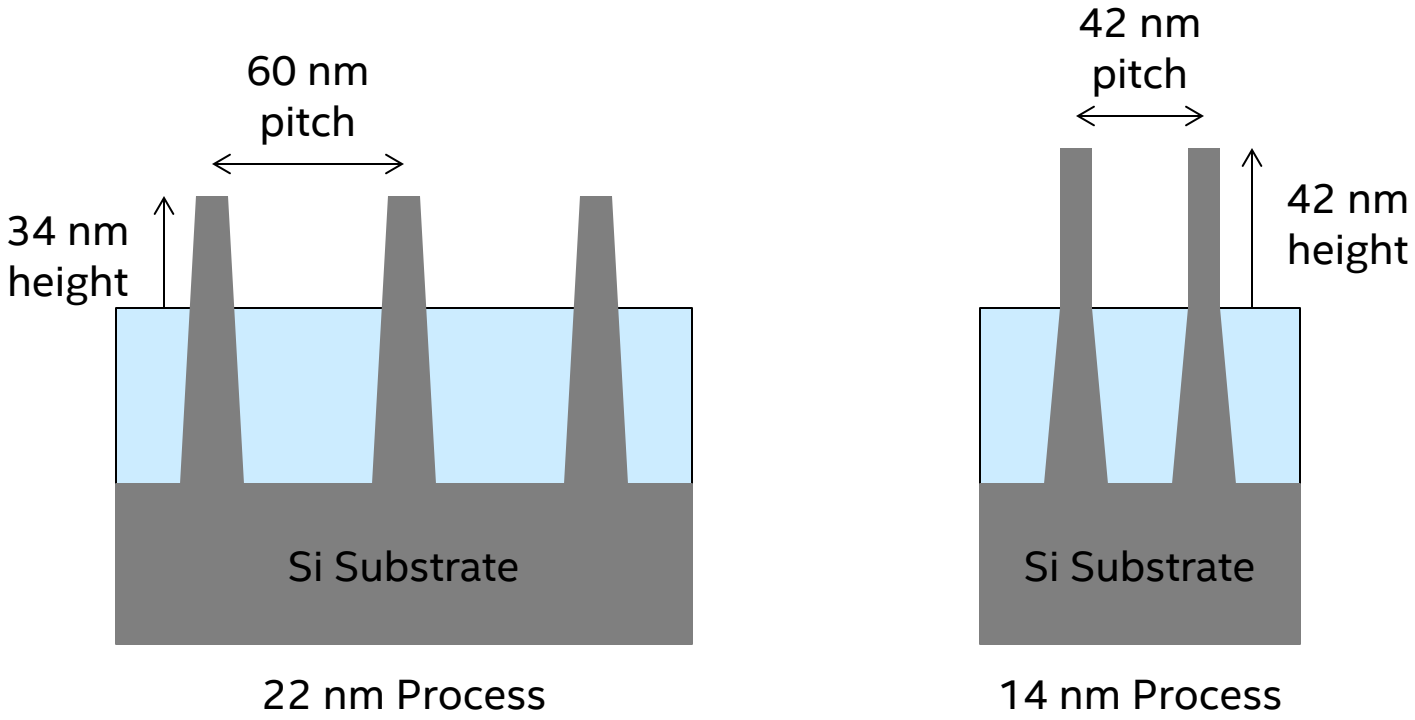
Tighter fin pitch for improved density

Transistor Fin Optimization



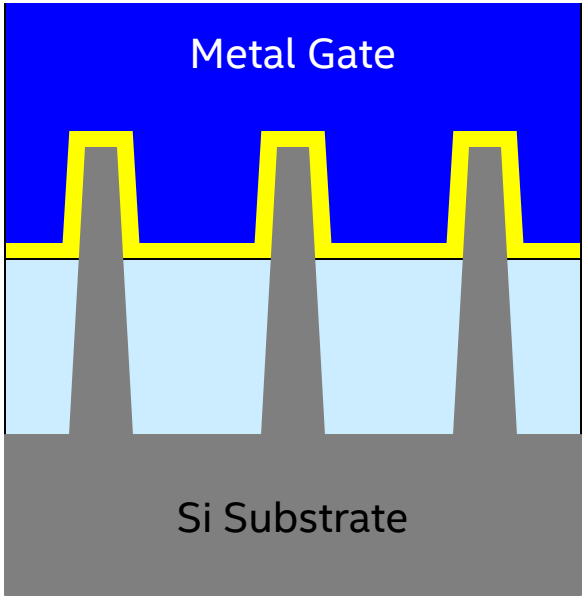
Taller and thinner fins for improved performance

Transistor Fin Optimization



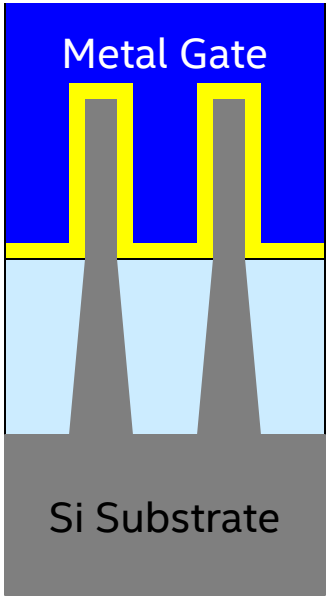
Reduced number of fins for improved density and lower capacitance

Transistor Fin Optimization



22 nm Process

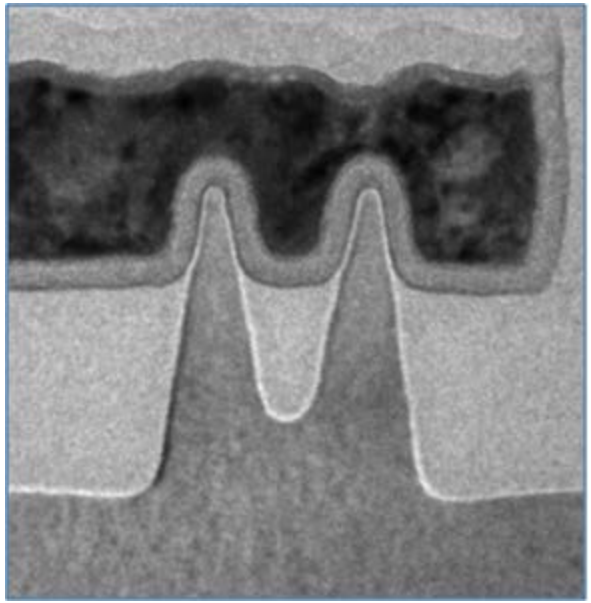
1st generation Tri-gate



14 nm Process

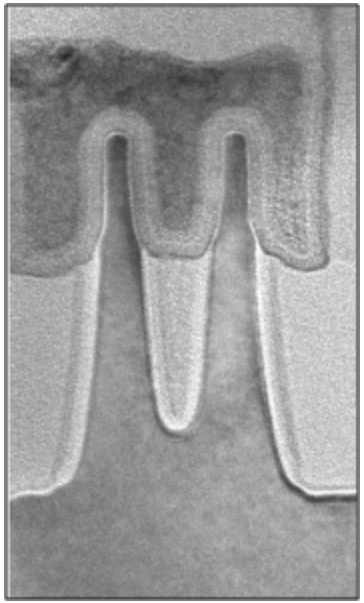
2nd generation Tri-gate

Transistor Fin Optimization



22 nm Process

1st generation Tri-gate

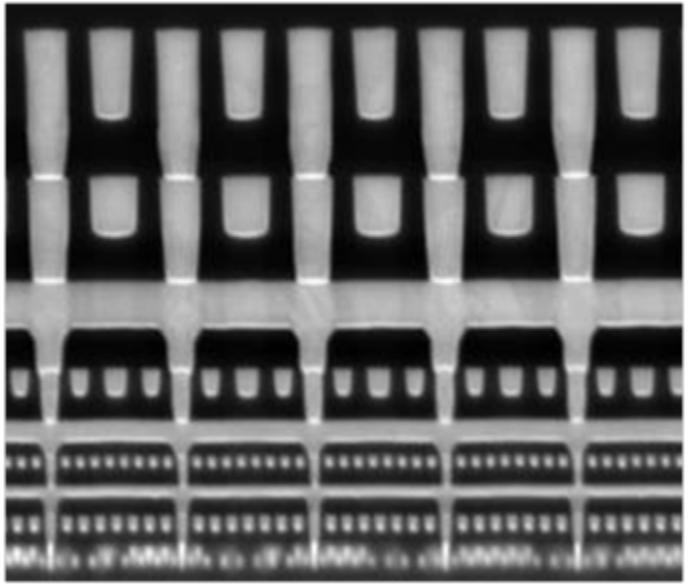


14 nm Process

2nd generation Tri-gate

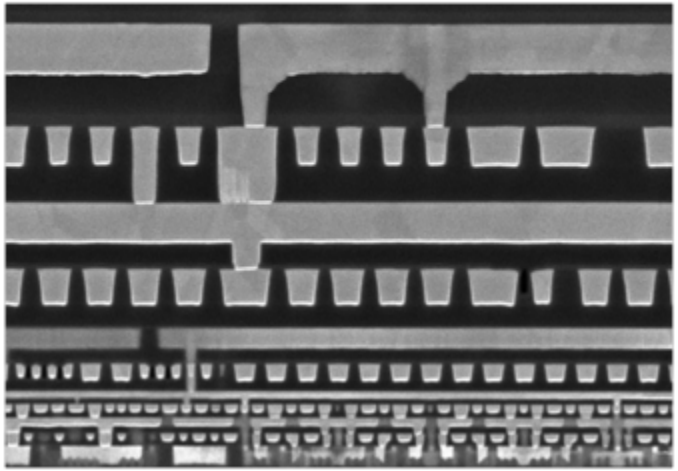
Interconnects

22 nm Process



80 nm minimum pitch

14 nm Process

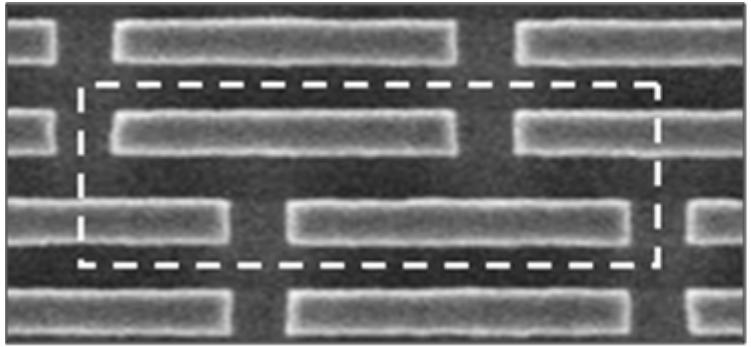


52 nm (0.65x) minimum pitch

52 nm interconnect pitch provides better than normal interconnect scaling

SRAM Memory Cells

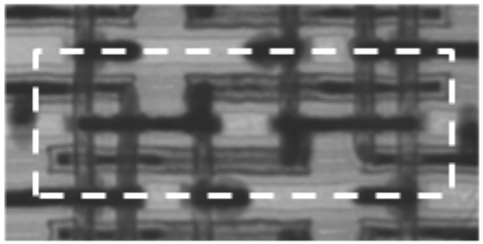
22 nm Process



.108 um^2

(Used on CPU products)

14 nm Process



.0588 um^2

(0.54x)

14 nm design rules + 2nd generation Tri-gate provides industry-leading SRAM density

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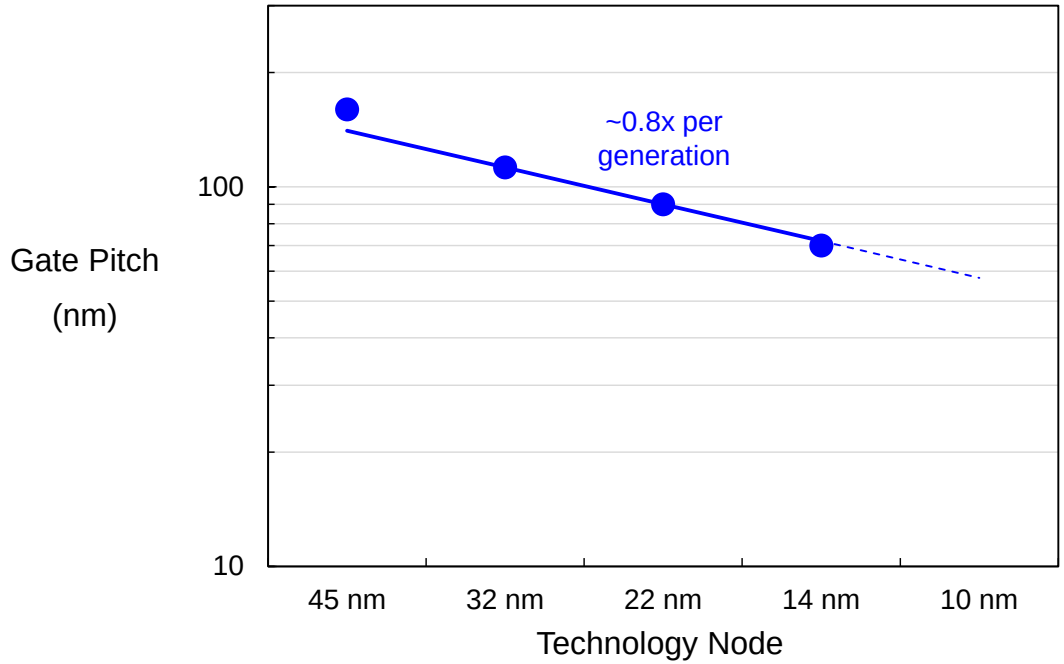
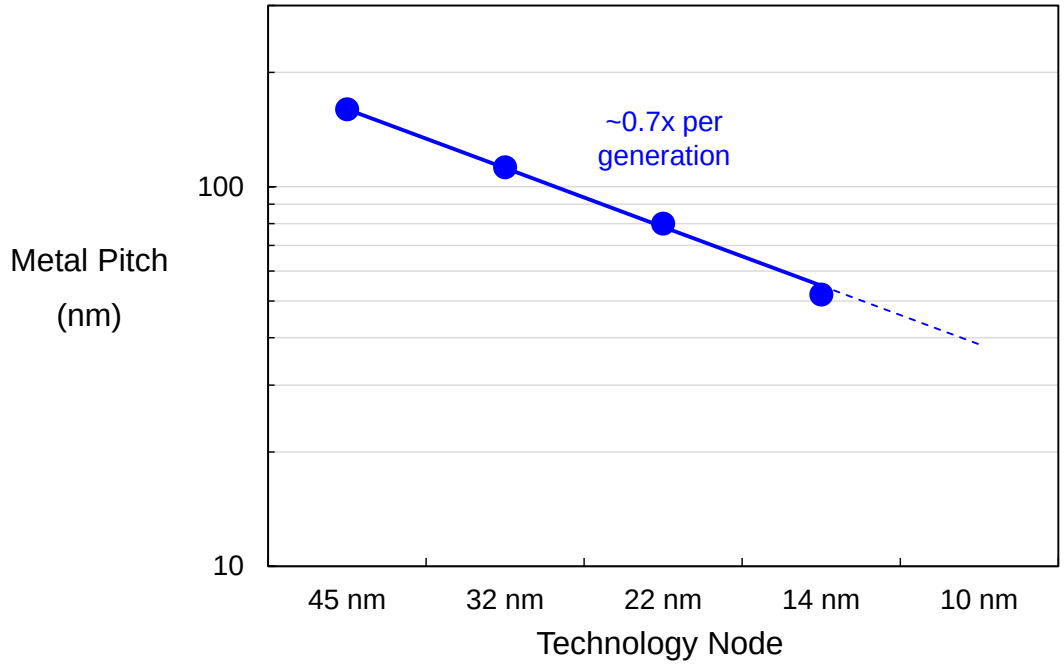
Transistor Gate Pitch Scaling



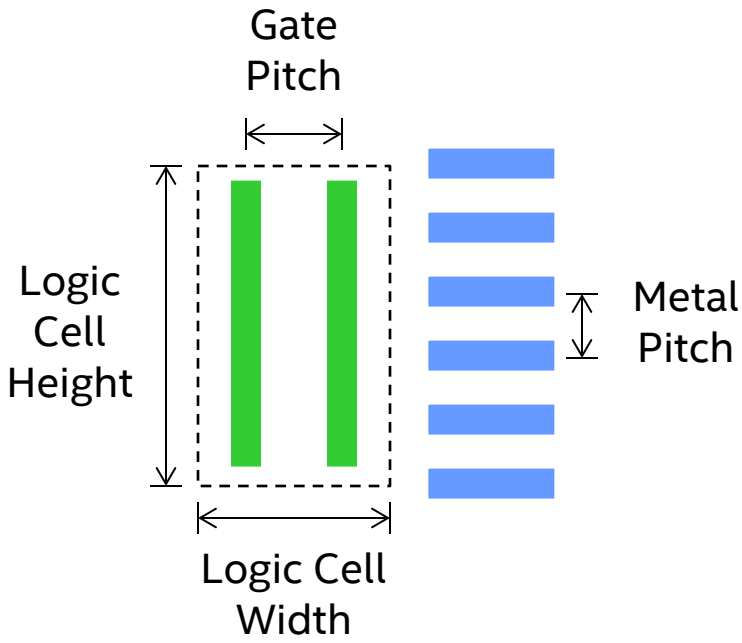
Gate pitch scaling ~0.8x for good balance of performance, density and low leakage

Metal Interconnect Pitch Scaling



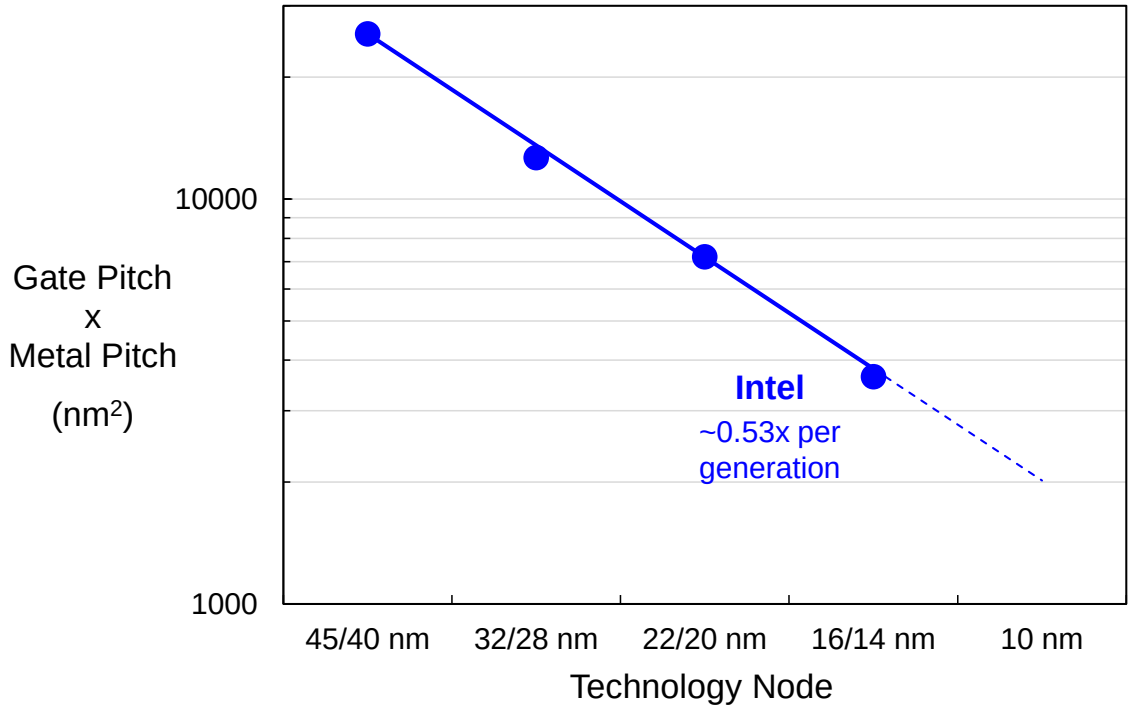
14 nm interconnects scaling faster than normal for improved density

Logic Area Scaling Metric



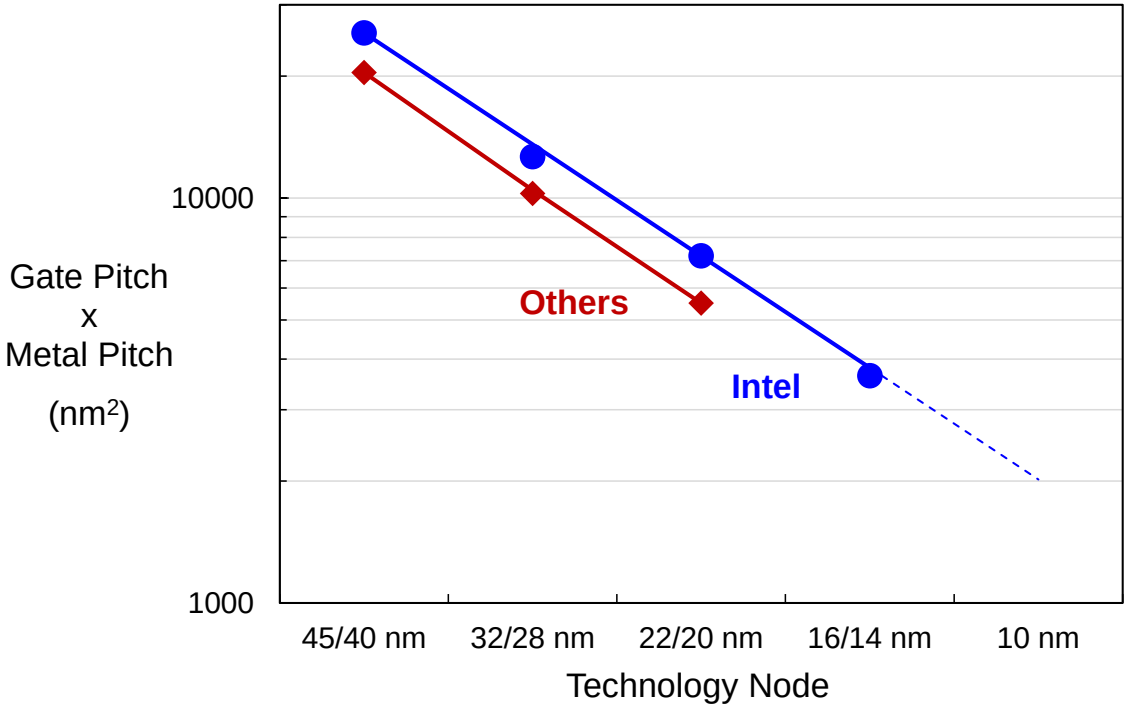
Logic area scaling ~ gate pitch x metal pitch

Logic Area Scaling



Logic area continues to scale ~0.53x per generation

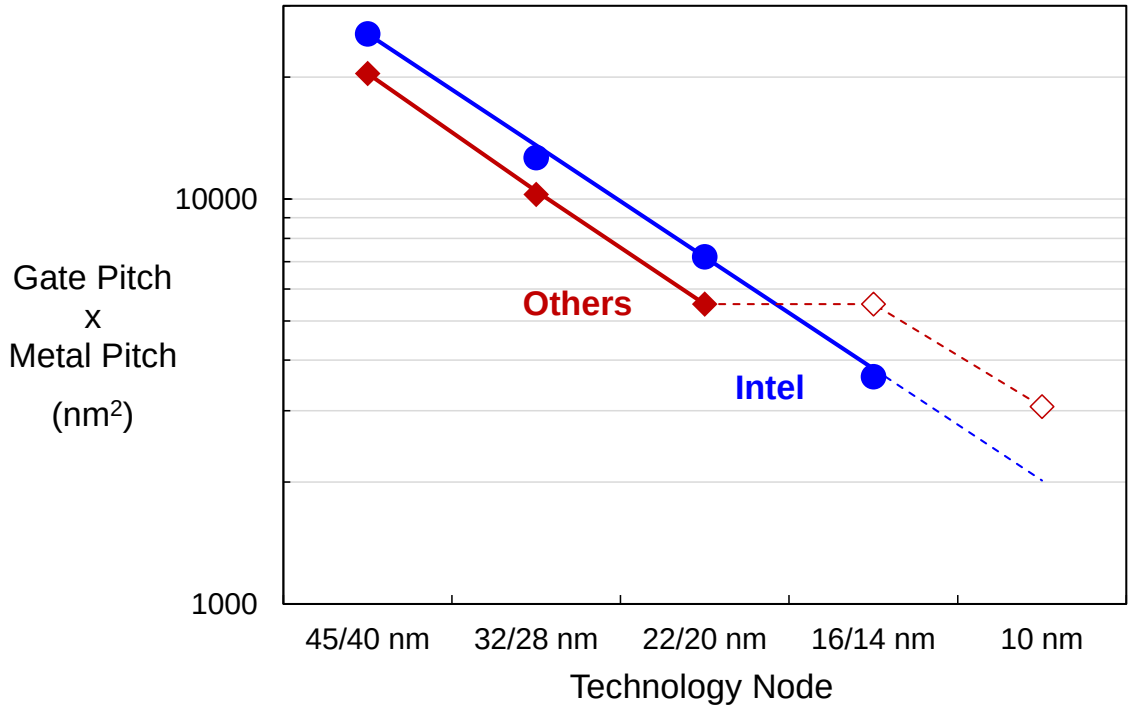
Logic Area Scaling



In the past, others tended to have better density, but came later than Intel

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p.129

Logic Area Scaling



Intel continues scaling at 14 nm while other pause to develop FinFETs

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
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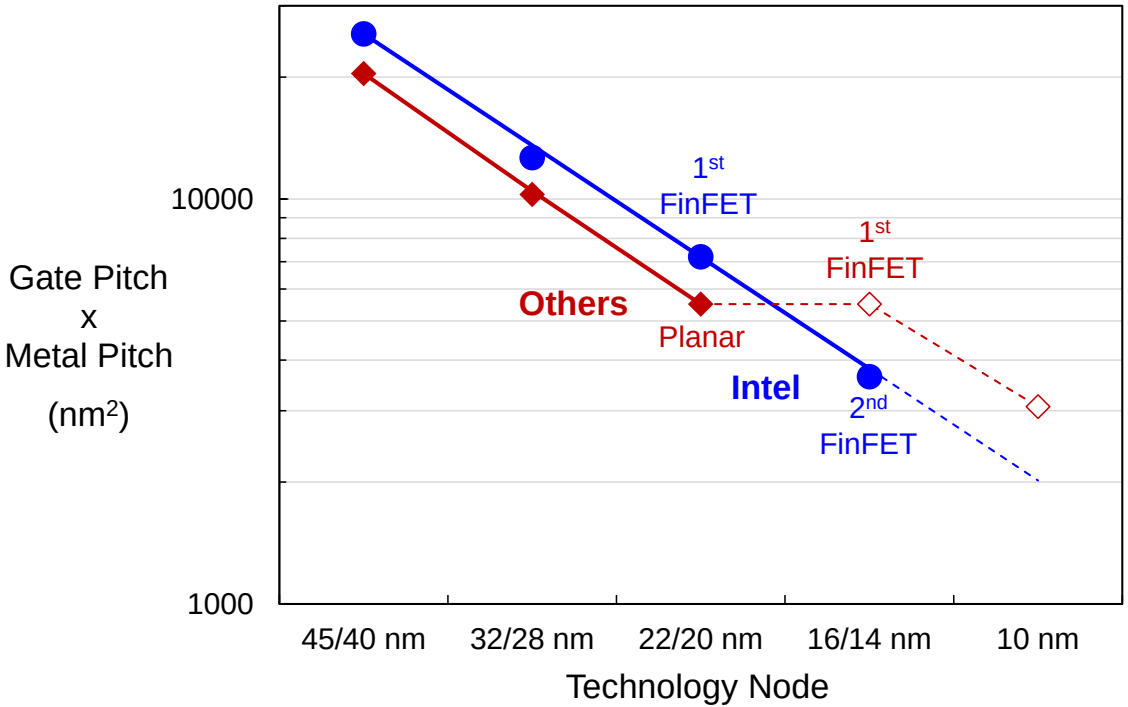
16nm: S. Wu (TSMC), 2013 IEDM, p. 224
10nm: K-I Seo (IBM alliance), 2014 VLSI, p. 14

Logic Area Scaling



Intel is shipping its 2nd generation FINFETs before others ship their 1st generation

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
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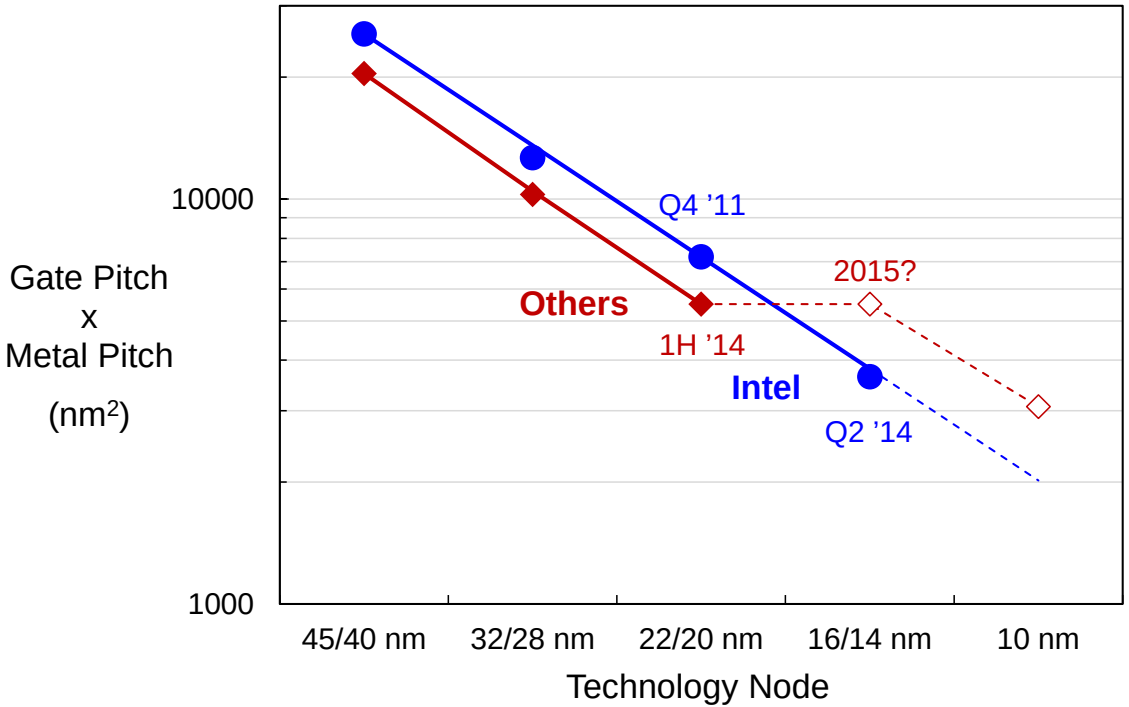
Logic Area Scaling



Intel 14 nm is both denser and earlier than what others call "16nm" or "14nm"

45nm: K-L Cheng (TSMC), 2007 IEDM, p. 243
28nm: F. Arnaud (IBM alliance), 2009 IEDM, p. 651
20nm: H. Shang (IBM alliance), 2012 VLSI, p.129
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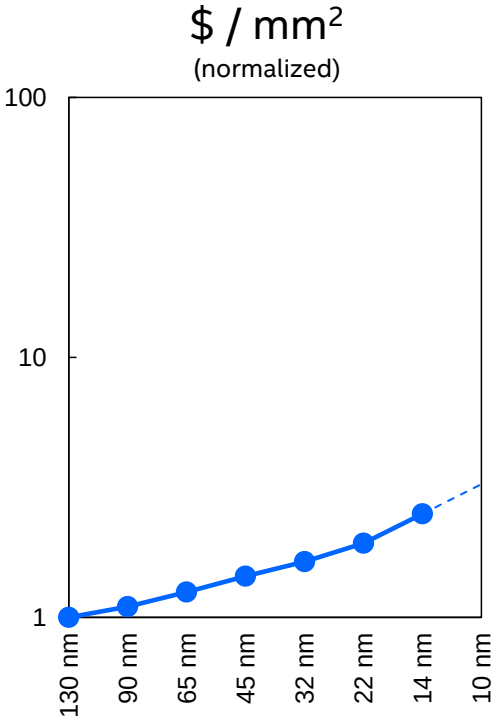
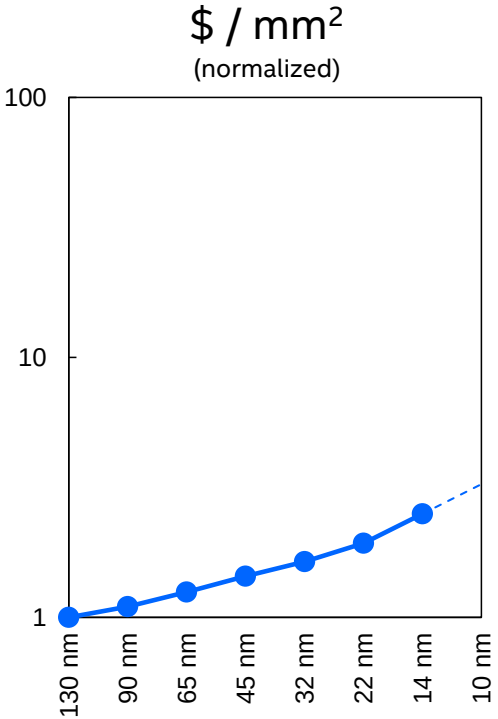
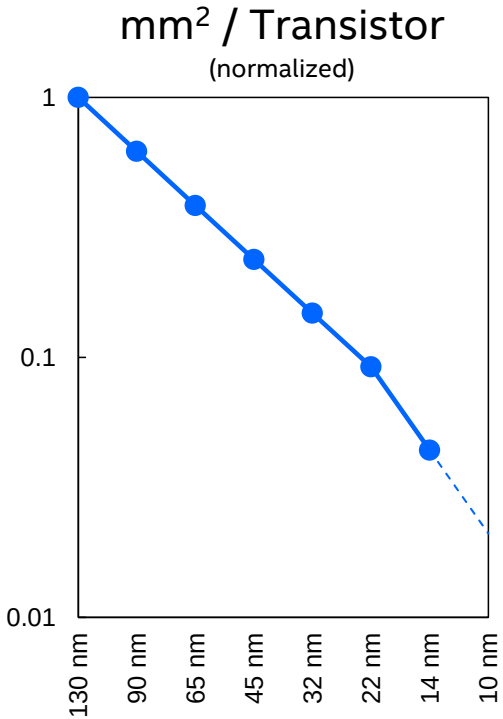
Cost per Transistor



Wafer cost is increasing due to added masking steps

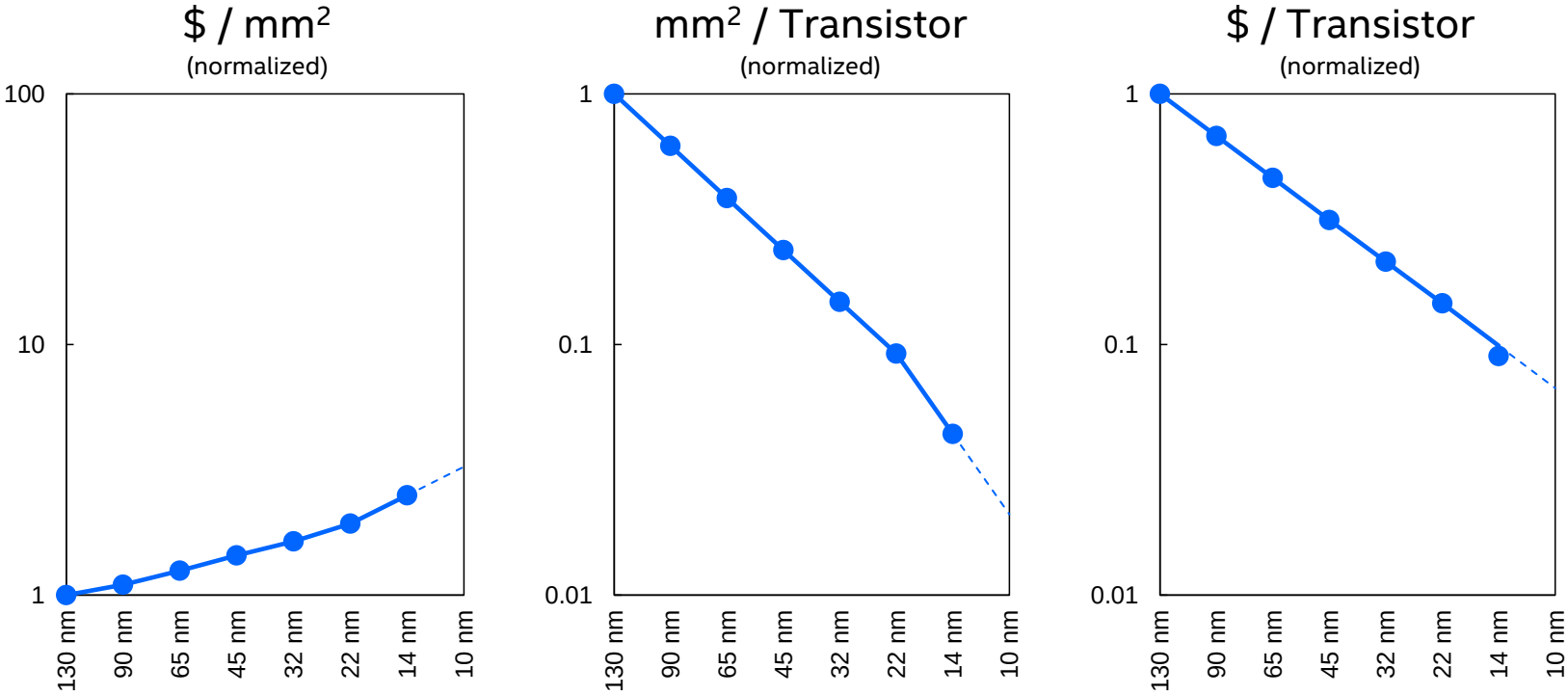
Cost per Transistor





14 nm achieves better than normal area scaling

Cost per Transistor



Intel 14 nm continues to deliver lower cost per transistor

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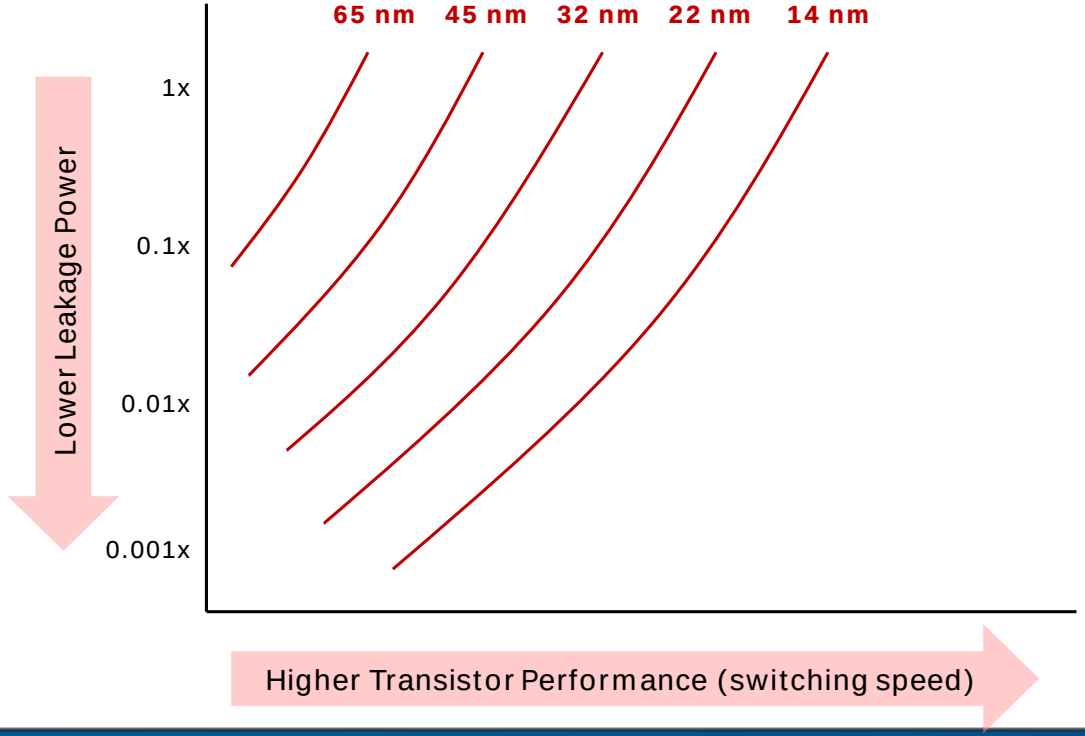
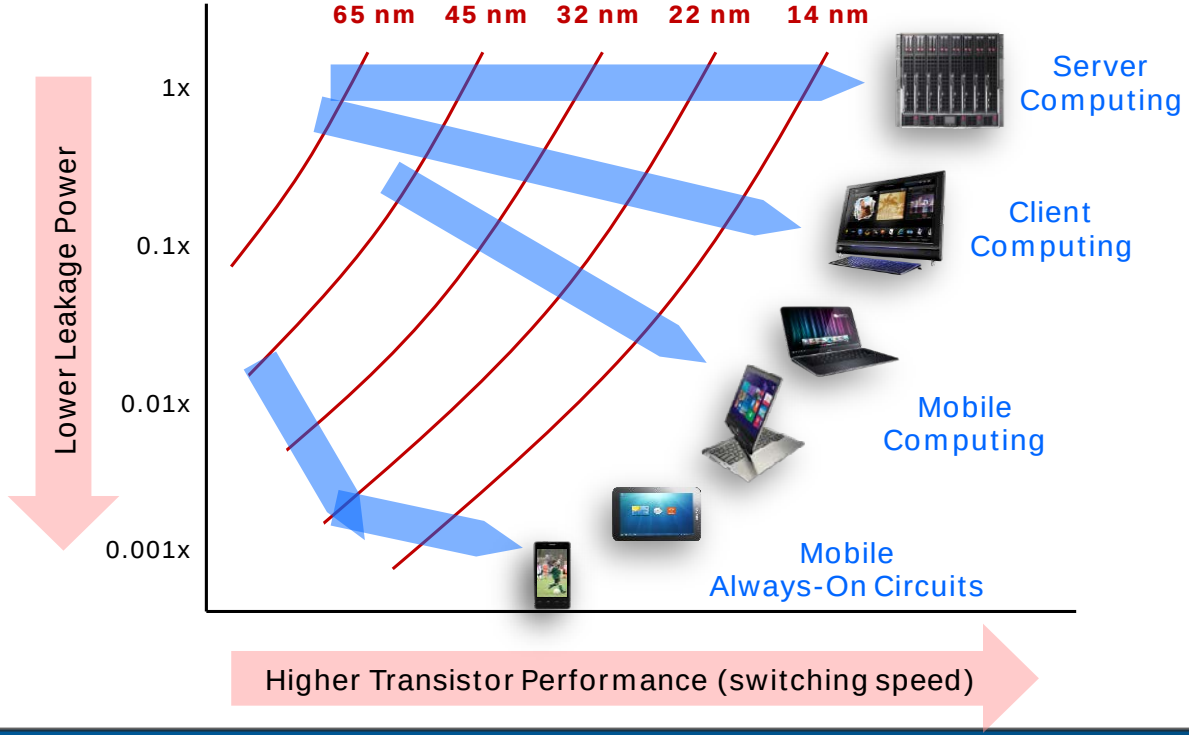
Transistor Performance vs. Leakage



14 nm transistors provide improved performance and leakage …

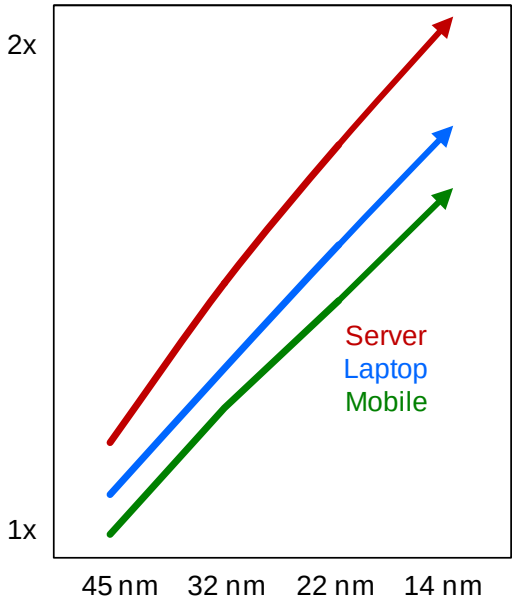
Transistor Performance vs. Leakage



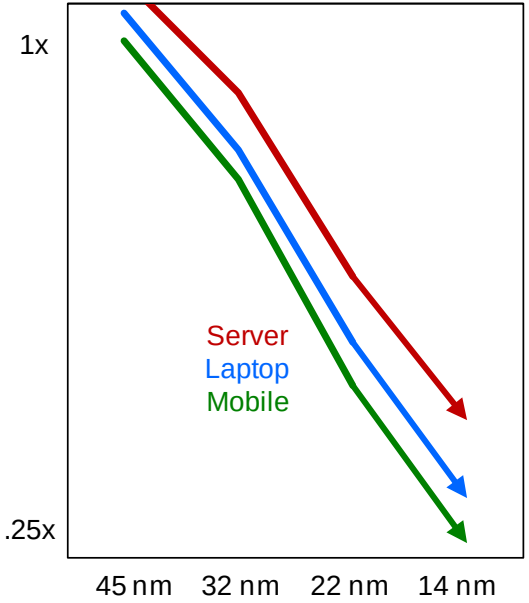
… to support a wide range of products

Product Benefits

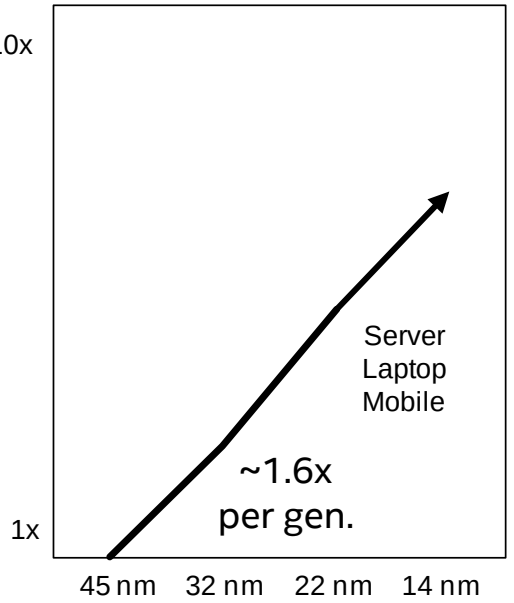
Performance



Active Power
(Includes performance increase)



Performance per Watt

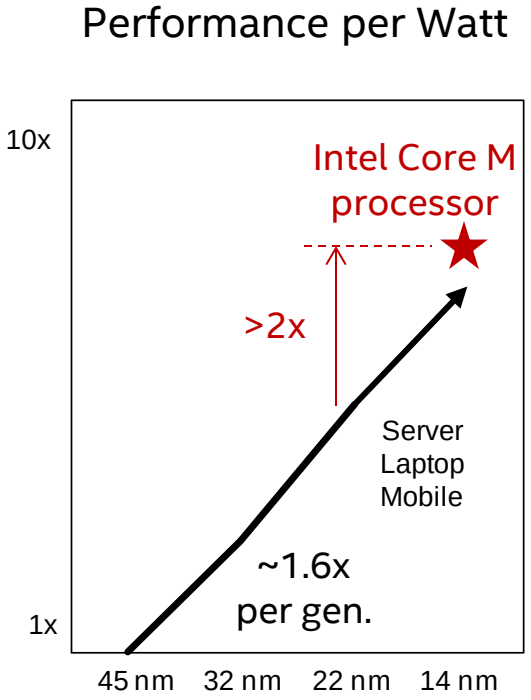


New technology generations provide improved performance and/or reduced power, but the key benefit is improved performance per watt

Product Benefits

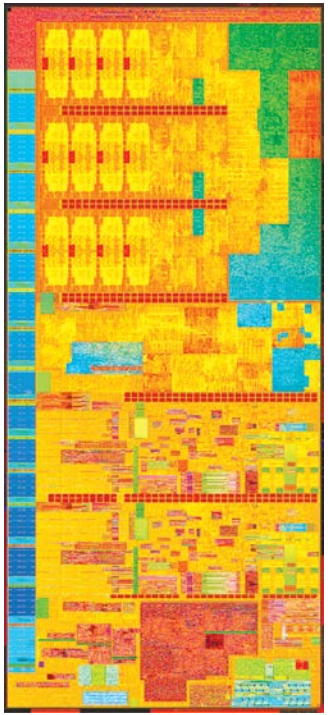
14 nm Intel® Core™ M processor delivers >2x improvement in performance per watt

- 2nd generation Tri-gate transistors with improved low voltage performance and lower leakage
- Better than normal area scaling
- Extensive design-process co-optimization
- Microarchitecture optimizations for active power reduction



Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark* and MobileMark*, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more information go to http://www.intel.com/performance.

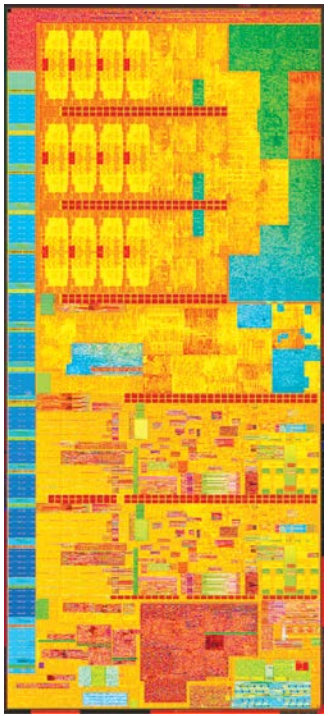
Intel® Core™ M Processor



- Real Performance
  - Up to 50% faster CPU performance vs. previous generation[1]
  - Up to 40% faster graphics performance vs. previous generation[2]
- Longer Battery Life
  - Power sipping 4.5W processor
- No Fan
  - 60% reduction in thermal design point (TDP)[3]
- A Conflict-Free Choice
  - Intel® Core™ M is a "conflict-free" product[4]

[1] Source: Intel: Based on SPECfp_rate_base2006. System configurations in backup.
[2] Source: Intel: 3DMark* IceStorm Unlimited v 1.2. System configurations in backup.
[3] Intel has reduced our thermal design power from 18W in 2010 to 11.5W in 2013 to 4.5W with the new Intel Core M processor. That's a 4X reduction over 4 years and a 60% reduction year over year.
[4] "Conflict-free" means "DRC conflict-free", which is defined by the Securities and Exchange Commission rules to mean products that do not contain conflict minerals (tin, tantalum, tungsten and/or gold) that directly or indirectly finance or benefit armed groups in the Democratic Republic of the Congo (DRC) or adjoining countries

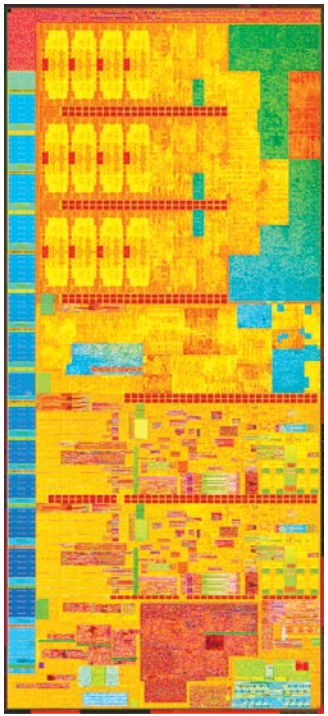
Intel® Core™ M Processor Die Area Scaling



82 mm^2

- Dense 14 nm process features provide good die area scaling compared to 22 nm processor
- 0.51x feature-neutral die area scaling
- 0.63x die area scaling with added design features

14 nm Manufacturing



- Process yield is now in healthy range with further improvements coming
- 14 nm process and lead product are qualified and in volume production
- 14 nm manufacturing fabs are located in:
  - Oregon (2014)
  - Arizona (2014)
  - Ireland (2015)

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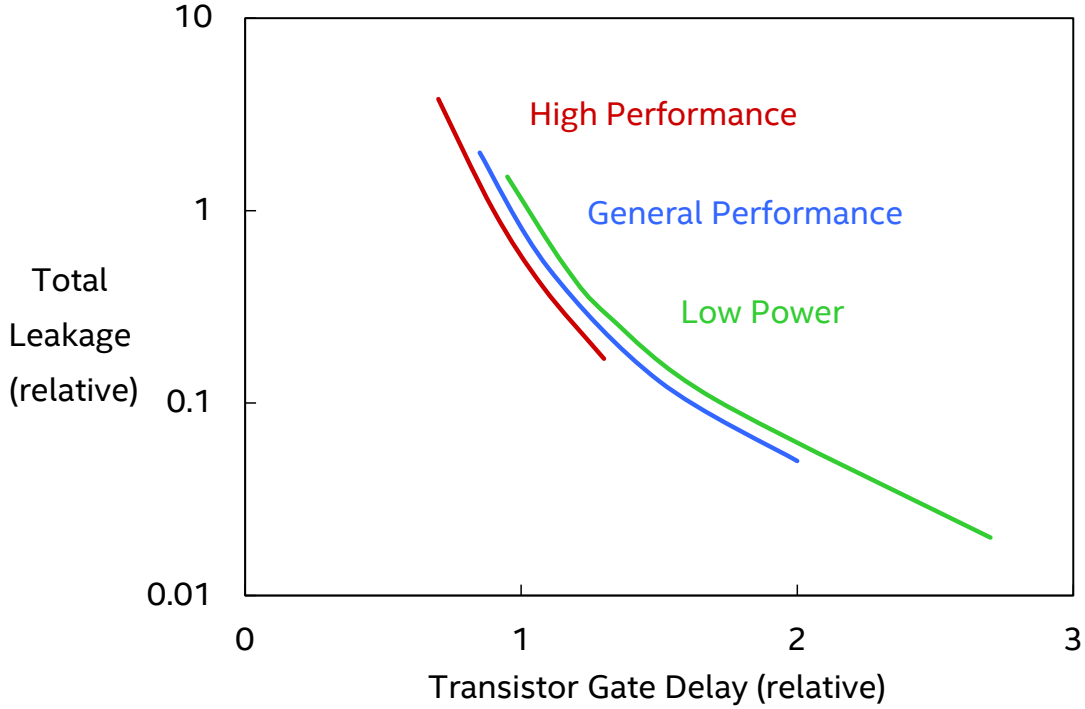
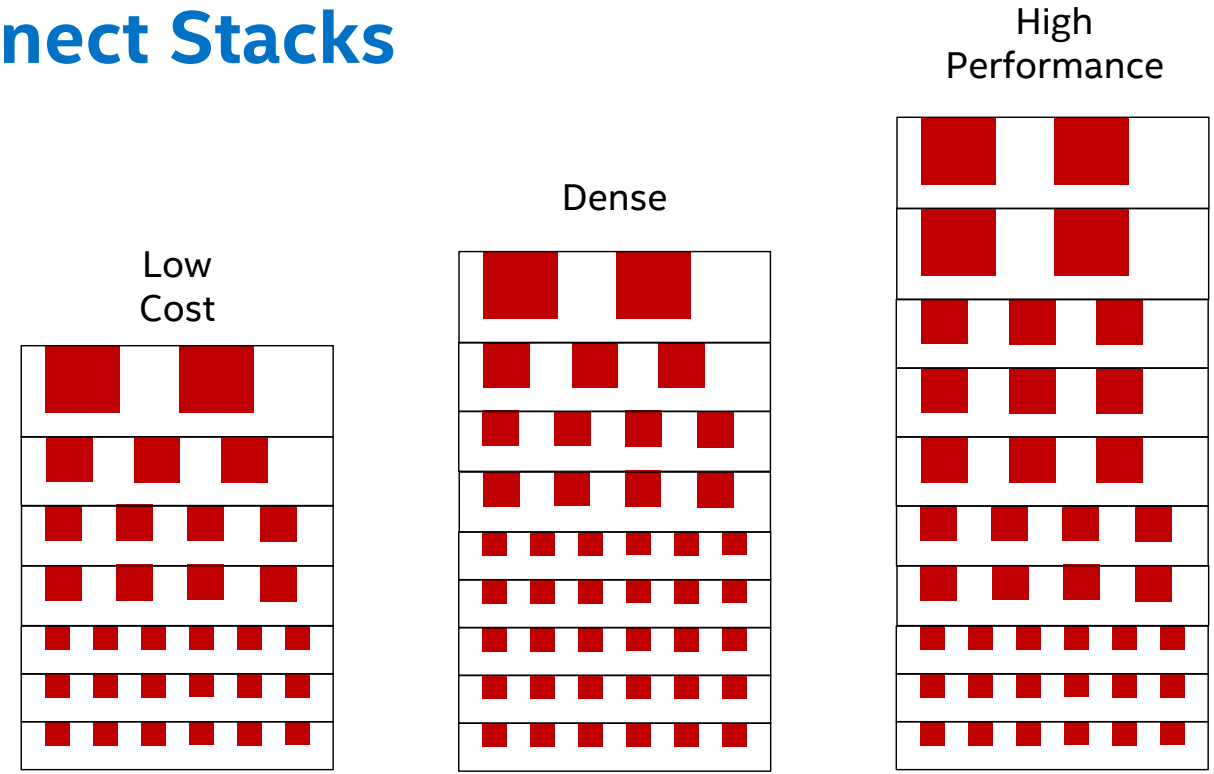


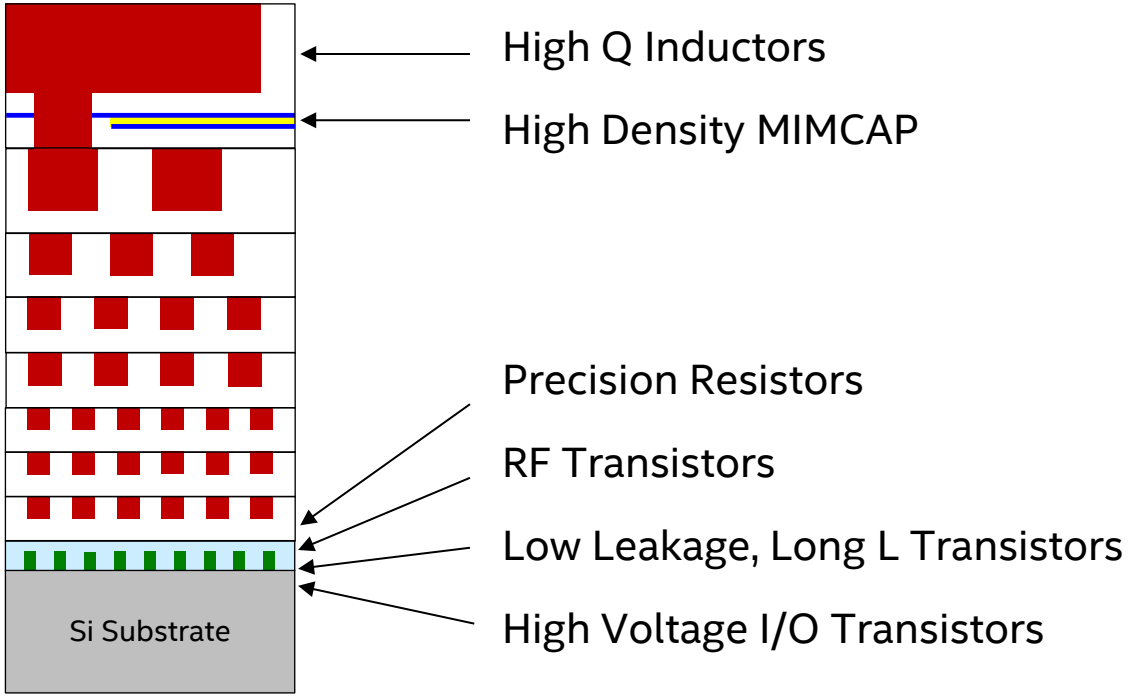
Multiple transistor options to support products from high performance to low power

Interconnect Stacks



Multiple interconnect stack offerings to optimize for cost, density, or performance

SoC Device Features



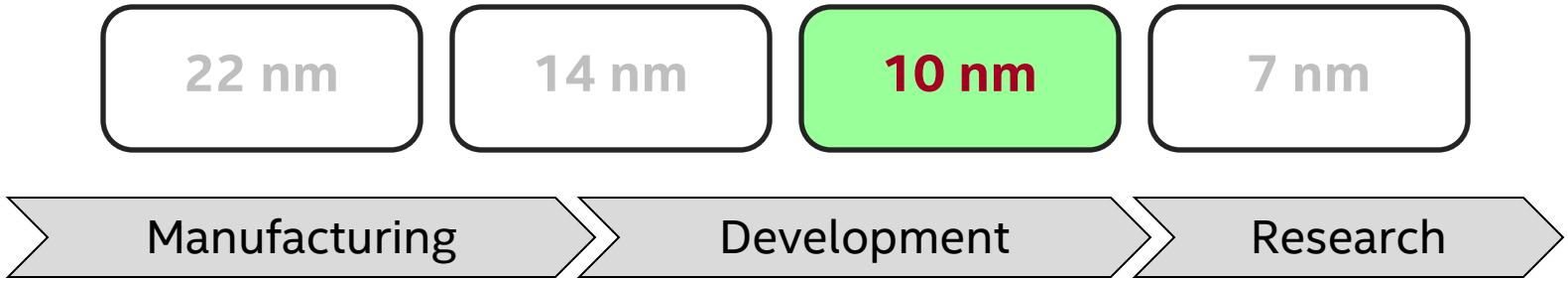
14 nm technology provides a full menu of SoC device options

Summary

- Intel has developed a true 14 nm technology with industry-leading performance, power, density and cost per transistor
- The 14 nm technology and the lead processor product are now qualified and in volume production
- A full menu of SoC transistor and interconnect features are provided
- Intel's 14 nm technology will be used to manufacture a wide range of products, from high performance to low power

Moore's Law continues!

Intel Technology Roadmap



10 nm coming next, with further improvements in performance, power and cost

Additional Sources of Information

- A PDF of this presentation is available is available from our Technical Session Catalog: www.intel.com/idfsessionsSF. This URL is also printed on the top of Session Agenda Pages in the Pocket Guide.
- "Leading at the Edge of Moore's Law with Intel Custom Foundry" SPCS011, 4:00-5:00pm, room 2004
- More web based info: http://newsroom.intel.com/community/intel_newsroom/blog/2014/08/11/intel-discloses-newest-microarchitecture-and-14-nanometer-manufacturing-process-technical-details

Legal Disclaimer

Risk Factors

The above statements and any others in this document that refer to plans and expectations for the second quarter, the year and the future are forward-looking statements that involve a number of risks and uncertainties. Words such as “anticipates,” “expects,” “intends,” “plans,” “believes,” “seeks,” “estimates,” “may,” “will,” “should” and their variations identify forward-looking statements. Statements that refer to or are based on projections, uncertain events or assumptions also identify forward-looking statements. Many factors could affect Intel’s actual results, and variances from Intel’s current expectations regarding such factors could cause actual results to differ materially from those expressed in these forward-looking statements. Intel presently considers the following to be important factors that could cause actual results to differ materially from the company’s expectations. Demand for Intel's products is highly variable and, in recent years, Intel has experienced declining orders in the traditional PC market segment. Demand could be different from Intel's expectations due to factors including changes in business and economic conditions; consumer confidence or income levels; customer acceptance of Intel’s and competitors’ products; competitive and pricing pressures, including actions taken by competitors; supply constraints and other disruptions affecting customers; changes in customer order patterns including order cancellations; and changes in the level of inventory at customers. Intel operates in highly competitive industries and its operations have high costs that are either fixed or difficult to reduce in the short term. Intel's gross margin percentage could vary significantly from expectations based on capacity utilization; variations in inventory valuation, including variations related to the timing of qualifying products for sale; changes in revenue levels; segment product mix; the timing and execution of the manufacturing ramp and associated costs; excess or obsolete inventory; changes in unit costs; defects or disruptions in the supply of materials or resources; and product manufacturing quality/yields. Variations in gross margin may also be caused by the timing of Intel product introductions and related expenses, including marketing expenses, and Intel's ability to respond quickly to technological developments and to introduce new products or incorporate new features into existing products, which may result in restructuring and asset impairment charges. Intel's results could be affected by adverse economic, social, political and physical/infrastructure conditions in countries where Intel, its customers or its suppliers operate, including military conflict and other security risks, natural disasters, infrastructure disruptions, health concerns and fluctuations in currency exchange rates. Intel’s results could be affected by the timing of closing of acquisitions, divestitures and other significant transactions. Intel's results could be affected by adverse effects associated with product defects and errata (deviations from published specifications), and by litigation or regulatory matters involving intellectual property, stockholder, consumer, antitrust, disclosure and other issues, such as the litigation and regulatory matters described in Intel's SEC filings. An unfavorable ruling could include monetary damages or an injunction prohibiting Intel from manufacturing or selling one or more products, precluding particular business practices, impacting Intel’s ability to design its products, or requiring other remedies such as compulsory licensing of intellectual property. A detailed discussion of these and other factors that could affect Intel’s results is included in Intel’s SEC filings, including the company’s most recent reports on Form 10-Q, Form 10-K and earnings release.

Rev. 4/15/14

Systems Configurations

- **Latest 2 in 1:** Intel® Core™ M-5Y70 Processor (up to 2.60GHz, 4T/2C, 4M Cache) On Intel Reference Platform. 4.5W Thermal Design Power. BIOS: v80.1 Graphics: Intel® HD Graphics (driver v. 15.36.3650) Memory: 4GB (2x2GB) Dual Channel LPDDR3-1600 SDD: Intel® 160GB OS: Windows* 8.1 Update RTM. System Power Management Policy: Balance Wireless: On and connected. Battery size assumption: 35WHr.
- **Prior generation:** Intel® Core™ i5-4302Y (up to 2.30GHz, 4T/2C, 3M Cache) on Intel Reference Platform. 4.5W Thermal Design Power. BIOS:WTM 137 Graphics : Intel® HD Graphics (driver v. 15.36.3650) Memory: 4 GB (2x2GB) Dual Channel LPDDR3-1600 SDD: Intel® 160GB OS: Windows* 8.1 Update RTM. System Power Management Policy: Balance Wireless: On and connected. Battery size assumption: 35WHr.