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CHAPTER 23
INTRODUCTION TO VIRTUAL-MACHINE EXTENSIONS

23.1 OVERVIEW

This chapter describes the basics of virtual machine architecture and an overview of the virtual-machine extensions (VMX) that support virtualization of processor hardware for multiple software environments.

Information about VMX instructions is provided in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*. Other aspects of VMX and system programming considerations are described in chapters of *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B*.

23.2 VIRTUAL MACHINE ARCHITECTURE

Virtual-machine extensions define processor-level support for virtual machines on IA-32 processors. Two principal classes of software are supported:

- **Virtual-machine monitors (VMM)** — A VMM acts as a host and has full control of the processor(s) and other platform hardware. A VMM presents guest software (see next paragraph) with an abstraction of a virtual processor and allows it to execute directly on a logical processor. A VMM is able to retain selective control of processor resources, physical memory, interrupt management, and I/O.

- **Guest software** — Each virtual machine (VM) is a guest software environment that supports a stack consisting of operating system (OS) and application software. Each operates independently of other virtual machines and uses on the same interface to processor(s), memory, storage, graphics, and I/O provided by a physical platform. The software stack acts as if it were running on a platform with no VMM. Software executing in a virtual machine must operate with reduced privilege so that the VMM can retain control of platform resources.

23.3 INTRODUCTION TO VMX OPERATION

Processor support for virtualization is provided by a form of processor operation called VMX operation. There are two kinds of VMX operation: VMX root operation and VMX non-root operation. In general, a VMM will run in VMX root operation and guest software will run in VMX non-root operation. Transitions between VMX root operation and VMX non-root operation are called VMX transitions. There are two kinds of VMX transitions. Transitions into VMX non-root operation are called VM entries. Transitions from VMX non-root operation to VMX root operation are called VM exits.

Processor behavior in VMX root operation is very much as it is outside VMX operation. The principal differences are that a set of new instructions (the VMX instructions) is available and that the values that can be loaded into certain control registers are limited (see Section 23.8).

Processor behavior in VMX non-root operation is restricted and modified to facilitate virtualization. Instead of their ordinary operation, certain instructions (including the new VMCALL instruction) and events cause VM exits to the VMM. Because these VM exits replace ordinary behavior, the functionality of software in VMX non-root operation is limited. It is this limitation that allows the VMM to retain control of processor resources.

There is no software-visible bit whose setting indicates whether a logical processor is in VMX non-root operation. This fact may allow a VMM to prevent guest software from determining that it is running in a virtual machine.

Because VMX operation places restrictions even on software running with current privilege level (CPL) 0, guest software can run at the privilege level for which it was originally designed. This capability may simplify the development of a VMM.
23.4 LIFE CYCLE OF VMM SOFTWARE

Figure 23-1 illustrates the life cycle of a VMM and its guest software as well as the interactions between them. The following items summarize that life cycle:

- Software enters VMX operation by executing a VMXON instruction.
- Using VM entries, a VMM can then enter guests into virtual machines (one at a time). The VMM effects a VM entry using instructions VMLAUNCH and VMRESUME; it regains control using VM exits.
- VM exits transfer control to an entry point specified by the VMM. The VMM can take action appropriate to the cause of the VM exit and can then return to the virtual machine using a VM entry.
- Eventually, the VMM may decide to shut itself down and leave VMX operation. It does so by executing the VMXOFF instruction.

23.5 VIRTUAL-MACHINE CONTROL STRUCTURE

VMX non-root operation and VMX transitions are controlled by a data structure called a virtual-machine control structure (VMCS).

Access to the VMCS is managed through a component of processor state called the VMCS pointer (one per logical processor). The value of the VMCS pointer is the 64-bit address of the VMCS. The VMCS pointer is read and written using the instructions VMPTRST and VMPTRLD. The VMM configures a VMCS using the VMREAD, VMWRITE, and VMCLEAR instructions.

A VMM could use a different VMCS for each virtual machine that it supports. For a virtual machine with multiple logical processors (virtual processors), the VMM could use a different VMCS for each virtual processor.

23.6 DISCOVERING SUPPORT FOR VMX

Before system software enters into VMX operation, it must discover the presence of VMX support in the processor. System software can determine whether a processor supports VMX operation using CPUID. If CPUID.1:ECX.VMX[bit 5] = 1, then VMX operation is supported. See Chapter 3, “Instruction Set Reference, A-M” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A.

The VMX architecture is designed to be extensible so that future processors in VMX operation can support additional features not present in first-generation implementations of the VMX architecture. The availability of extensible VMX features is reported to software using a set of VMX capability MSRs (see Appendix A, “VMX Capability Reporting Facility”).
23.7 ENABLING AND ENTERING VMX OPERATION

Before system software can enter VMX operation, it enables VMX by setting CR4.VMXE[bit 13] = 1. VMX operation is then entered by executing the VMXON instruction. VMXON causes an invalid-opcode exception (#UD) if executed with CR4.VMXE = 0. Once in VMX operation, it is not possible to clear CR4.VMXE (see Section 23.8). System software leaves VMX operation by executing the VMXOFF instruction. CR4.VMXE can be cleared outside of VMX operation after executing of VMXOFF.

VMXON is also controlled by the IA32_FEATURE_CONTROL MSR (MSR address 3AH). This MSR is cleared to zero when a logical processor is reset. The relevant bits of the MSR are:

- **Bit 0 is the lock bit.** If this bit is clear, VMXON causes a general-protection exception. If the lock bit is set, WRMSR to this MSR causes a general-protection exception; the MSR cannot be modified until a power-up reset condition. System BIOS can use this bit to provide a setup option for BIOS to disable support for VMX. To enable VMX support in a platform, BIOS must set bit 1, bit 2, or both (see below), as well as the lock bit.

- **Bit 1 enables VMXON in SMX operation.** If this bit is clear, execution of VMXON in SMX operation causes a general-protection exception. Attempts to set this bit on logical processors that do not support both VMX operation (see Section 23.6) and SMX operation (see Chapter 6, “Safer Mode Extensions Reference,” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*) cause general-protection exceptions.

- **Bit 2 enables VMXON outside SMX operation.** If this bit is clear, execution of VMXON outside SMX operation causes a general-protection exception. Attempts to set this bit on logical processors that do not support VMX operation (see Section 23.6) cause general-protection exceptions.

**NOTE**

A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*.

Before executing VMXON, software should allocate a naturally aligned 4-KByte region of memory that a logical processor may use to support VMX operation. This region is called the *VMXON region*. The address of the VMXON region (the VMXON pointer) is provided in an operand to VMXON. Section 24.11.5, “VMXON Region,” details how software should initialize and access the VMXON region.

23.8 RESTRICTIONS ON VMX OPERATION

VMX operation places restrictions on processor operation. These are detailed below:

- In VMX operation, processors may fix certain bits in CR0 and CR4 to specific values and not support other values. VMXON fails if any of these bits contains an unsupported value (see “VMXON—Enter VMX Operation” in Chapter 30). Any attempt to set one of these bits to an unsupported value while in VMX operation (including VMX root operation) using any of the CLTS, LMSW, or MOV CR instructions causes a general-protection exception. VM entry or VM exit cannot set any of these bits to an unsupported value. Software should consult the VMX capability MSRs IA32_VMX_CR0_FIXED0 and IA32_VMX_CR0_FIXED1 to determine how bits in CR0 are fixed. (see Appendix A.7). For CR4, software should consult the VMX capability MSRs IA32_VMX_CR4_FIXED0 and IA32_VMX_CR4_FIXED1 (see Appendix A.8).

**NOTES**

The first processors to support VMX operation require that the following bits be 1 in VMX operation: CR0.PE, CR0.NE, CR0.PG, and CR4.VMXE. The restrictions on CR0.PE and CR0.PG imply that VMX operation is supported only in paged protected mode (including IA-32e mode). Therefore, guest software cannot be run in unpaged protected mode or in real-address mode. See Section 31.2,

1. Future processors may require that a different amount of memory be reserved. If so, this fact is reported to software using the VMX capability-reporting mechanism.
“Supporting Processor Operating Modes in Guest Environments,” for a discussion of how a VMM might support guest software that expects to run in unpaged protected mode or in real-address mode.

Later processors support a VM-execution control called “unrestricted guest” (see Section 24.6.2). If this control is 1, CR0.PE and CR0.PG may be 0 in VMX non-root operation (even if the capability MSR IA32_VMX_CR0_FIXED0 reports otherwise). Such processors allow guest software to run in unpaged protected mode or in real-address mode.

- VMXON fails if a logical processor is in A20M mode (see “VMXON—Enter VMX Operation” in Chapter 30). Once the processor is in VMX operation, A20M interrupts are blocked. Thus, it is impossible to be in A20M mode in VMX operation.
- The INIT signal is blocked whenever a logical processor is in VMX root operation. It is not blocked in VMX non-root operation. Instead, INITs cause VM exits (see Section 25.2, "Other Causes of VM Exits").

---

1. “Unrestricted guest” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if the “unrestricted guest” VM-execution control were 0. See Section 24.6.2.
24.1 OVERVIEW

A logical processor uses virtual-machine control data structures (VMCSs) while it is in VMX operation. These manage transitions into and out of VMX non-root operation (VM entries and VM exits) as well as processor behavior in VMX non-root operation. This structure is manipulated by the new instructions VMCLEAR, VMPTRLD, VMREAD, and VMWRITE.

A VMM can use a different VMCS for each virtual machine that it supports. For a virtual machine with multiple logical processors (virtual processors), the VMM can use a different VMCS for each virtual processor.

A logical processor associates a region in memory with each VMCS. This region is called the VMCS region. Software references a specific VMCS using the 64-bit physical address of the region (a VMCS pointer). VMCS pointers must be aligned on a 4-KByte boundary (bits 11:0 must be zero). These pointers must not set bits beyond the processor’s physical-address width.

A logical processor may maintain a number of VMCSs that are active. The processor may optimize VMX operation by maintaining the state of an active VMCS in memory, on the processor, or both. At any given time, at most one of the active VMCSs is the current VMCS. (This document frequently uses the term “the VMCS” to refer to the current VMCS.) TheVMLAUNCH, VMREAD, VMRESUME, and VMWRITE instructions operate only on the current VMCS.

The following items describe how a logical processor determines which VMCSs are active and which is current:

- The memory operand of the VMPTRLD instruction is the address of a VMCS. After execution of the instruction, that VMCS is both active and current on the logical processor. Any other VMCS that had been active remains so, but no other VMCS is current.
- The VMCS link pointer field in the current VMCS (see Section 24.4.2) is itself the address of a VMCS. If VM entry is performed successfully with the 1-setting of the “VMCS shadowing” VM-execution control, the VMCS referenced by the VMCS link pointer field becomes active on the logical processor. The identity of the current VMCS does not change.
- The memory operand of the VMCLEAR instruction is also the address of a VMCS. After execution of the instruction, the launch state of that VMCS is “clear”. There are no other ways to modify the launch state of a VMCS (it cannot be modified using VMWRITE) and there is no direct way to discover it (it cannot be read using VMREAD).

1. The amount of memory required for a VMCS region is at most 4 KBytes. The exact size is implementation specific and can be determined by consulting the VMX capability MSR IA32_VMX_BASIC to determine the size of the VMCS region (see Appendix A.1).
2. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
3. If IA32_VMX_BASIC[48] is read as 1, these pointers must not set any bits in the range 63:32; see Appendix A.1.
VIRTUAL-MACHINE CONTROL STRUCTURES

Figure 24-1 illustrates the different states of a VMCS. It uses “X” to refer to the VMCS and “Y” to refer to any other VMCS. Thus: “VMPTRLD X” always makes X current and active; “VMPTRLD Y” always makes X not current (because it makes Y current); VMLAUNCH makes the launch state of X “launched” if X was current and its launch state was “clear”; and VMCLE AR X always makes X inactive and not current and makes its launch state “clear”.

The figure does not illustrate operations that do not modify the VMCS state relative to these parameters (e.g., execution of VMPTRLD X when X is already current). Note that VMCLEAR X makes X “inactive, not current, and clear,” even if X’s current state is not defined (e.g., even if X has not yet been initialized). See Section 24.11.3.

Figure 24-1. States of VMCS X

Because a shadow VMCS (see Section 24.10) cannot be used for VM entry, the launch state of a shadow VMCS is not meaningful. Figure 24-1 does not illustrate all the ways in which a shadow VMCS may be made active.

24.2 FORMAT OF THE VMCS REGION

A VMCS region comprises up to 4-KBytes. The format of a VMCS region is given in Table 24-1.

Table 24-1. Format of the VMCS Region

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Bits 30:0: VMCS revision identifier</td>
</tr>
<tr>
<td></td>
<td>Bit 31: shadow-VMCS indicator (see Section 24.10)</td>
</tr>
<tr>
<td>4</td>
<td>VMX-abort indicator</td>
</tr>
<tr>
<td>8</td>
<td>VMCS data (implementation-specific format)</td>
</tr>
</tbody>
</table>

The first 4 bytes of the VMCS region contain the VMCS revision identifier at bits 30:0. Processors that maintain VMCS data in different formats (see below) use different VMCS revision identifiers. These identifiers enable soft-

1. The exact size is implementation specific and can be determined by consulting the VMX capability MSR IA32_VMX_BASIC to determine the size of the VMCS region (see Appendix A.1).
ware to avoid using a VMCS region formatted for one processor on a processor that uses a different format.\(^1\) Bit 31 of this 4-byte region indicates whether the VMCS is a shadow VMCS (see Section 24.10).

Software should write the VMCS revision identifier to the VMCS region before using that region for a VMCS. The VMCS revision identifier is never written by the processor; VMPTRLD fails if its operand references a VMCS region whose VMCS revision identifier differs from that used by the processor. (VMPTRLD also fails if the shadow-VMCS indicator is 1 and the processor does not support the 1-setting of the “VMCS shadowing” VM-execution control; see Section 24.6.2.) Software can discover the VMCS revision identifier that a processor uses by reading the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).

Software should clear or set the shadow-VMCS indicator depending on whether the VMCS is to be an ordinary VMCS or a shadow VMCS (see Section 24.10). VMPTRLD fails if the shadow-VMCS indicator is set and the processor does not support the 1-setting of the “VMCS shadowing” VM-execution control. Software can discover support for this setting by reading the VMX capability MSR IA32_VMX_PROCBASED_CTLS2 (see Appendix A.3.3).

The next 4 bytes of the VMCS region are used for the **VMX-abort indicator**. The contents of these bits do not control processor operation in any way. A logical processor writes a non-zero value into these bits if a VMX abort occurs (see Section 27.7). Software may also write into this field.

The remainder of the VMCS region is used for **VMCS data** (those parts of the VMCS that control VMX non-root operation and the VMX transitions). The format of these data is implementation-specific. VMCS data are discussed in Section 24.3 through Section 24.9. To ensure proper behavior in VMX operation, software should maintain the VMCS region and related structures (enumerated in Section 24.11.4) in writeback cacheable memory. Future implementations may allow or require a different memory type\(^2\). Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).

### 24.3 ORGANIZATION OF VMCS DATA

The VMCS data are organized into six logical groups:

- **Guest-state area.** Processor state is saved into the guest-state area on VM exits and loaded from there on VM entries.
- **Host-state area.** Processor state is loaded from the host-state area on VM entries.
- **VM-execution control fields.** These fields control processor behavior in VMX non-root operation. They determine in part the causes of VM exits.
- **VM-exit control fields.** These fields control VM exits.
- **VM-entry control fields.** These fields control VM entries.
- **VM-exit information fields.** These fields receive information on VM exits and describe the cause and the nature of VM exits. On some processors, these fields are read-only.\(^3\)

The VM-execution control fields, the VM-exit control fields, and the VM-entry control fields are sometimes referred to collectively as VMX controls.

---

\(^1\) Logical processors that use the same VMCS revision identifier use the same size for VMCS regions.

\(^2\) Alternatively, software may map any of these regions or structures with the UC memory type. Doing so is strongly discouraged unless necessary as it will cause the performance of transitions using those structures to suffer significantly. In addition, the processor will continue to use the memory type reported in the VMX capability MSR IA32_VMX_BASIC with exceptions noted in Appendix A.1.

\(^3\) Software can discover whether these fields can be written by reading the VMX capability MSR IA32_VMX_MISC (see Appendix A.6).
24.4 GUEST-STATE AREA

This section describes fields contained in the guest-state area of the VMCS. As noted earlier, processor state is loaded from these fields on every VM entry (see Section 26.3.2) and stored into these fields on every VM exit (see Section 27.3).

24.4.1 Guest Register State

The following fields in the guest-state area correspond to processor registers:

- Control registers CR0, CR3, and CR4 (64 bits each; 32 bits on processors that do not support Intel 64 architecture).
- Debug register DR7 (64 bits; 32 bits on processors that do not support Intel 64 architecture).
- RSP, RIP, and RFLAGS (64 bits each; 32 bits on processors that do not support Intel 64 architecture).
- The following fields for each of the registers CS, SS, DS, ES, FS, GS, LDTR, and TR:
  - Selector (16 bits).
  - Base address (64 bits; 32 bits on processors that do not support Intel 64 architecture). The base-address fields for CS, SS, DS, and ES have only 32 architecturally-defined bits; nevertheless, the corresponding VMCS fields have 64 bits on processors that support Intel 64 architecture.
  - Segment limit (32 bits). The limit field is always a measure in bytes.
  - Access rights (32 bits). The format of this field is given in Table 24-2 and detailed as follows:
    - The low 16 bits correspond to bits 23:8 of the upper 32 bits of a 64-bit segment descriptor. While bits 19:16 of code-segment and data-segment descriptors correspond to the upper 4 bits of the segment limit, the corresponding bits (bits 11:8) are reserved in this VMCS field.
    - Bit 16 indicates an unusable segment. Attempts to use such a segment fault except in 64-bit mode. In general, a segment register is unusable if it has been loaded with a null selector.
    - Bits 31:17 are reserved.

Table 24-2. Format of Access Rights

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Segment type</td>
</tr>
<tr>
<td>4</td>
<td>S — Descriptor type (0 = system; 1 = code or data)</td>
</tr>
<tr>
<td>6:5</td>
<td>DPL — Descriptor privilege level</td>
</tr>
<tr>
<td>7</td>
<td>P — Segment present</td>
</tr>
<tr>
<td>11:8</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>AVL — Available for use by system software</td>
</tr>
</tbody>
</table>

1. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.). In a few places, notation such as EAX is used to refer specifically to lower 32 bits of the indicated register.

2. There are a few exceptions to this statement. For example, a segment with a non-null selector may be unusable following a task switch that fails after its commit point; see “Interrupt 10—Invalid TSS Exception (#TS)” in Section 6.14, “Exception and Interrupt Handling in 64-bit Mode,” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A. In contrast, the TR register is usable after processor reset despite having a null selector; see Table 10-1 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
The base address, segment limit, and access rights compose the “hidden” part (or “descriptor cache”) of each segment register. These data are included in the VMCS because it is possible for a segment register’s descriptor cache to be inconsistent with the segment descriptor in memory (in the GDT or the LDT) referenced by the segment register’s selector.

The value of the DPL field for SS is always equal to the logical processor’s current privilege level (CPL).\(^1\)

- The following fields for each of the registers GDTR and IDTR:
  - Base address (64 bits; 32 bits on processors that do not support Intel 64 architecture).
  - Limit (32 bits). The limit fields contain 32 bits even though these fields are specified as only 16 bits in the architecture.

- The following MSRs:
  - IA32_DEBUGCTL (64 bits)
  - IA32_SYSENTER_CS (32 bits)
  - IA32_SYSENTER_ESP and IA32_SYSENTER_EIP (64 bits; 32 bits on processors that do not support Intel 64 architecture)
  - IA32_PERF_GLOBAL_CTRL (64 bits). This field is supported only on processors that support the 1-setting of the “load IA32_PERF_GLOBAL_CTRL” VM-entry control.
  - IA32_PAT (64 bits). This field is supported only on processors that support either the 1-setting of the “load IA32_PAT” VM-entry control or that of the “save IA32_PAT” VM-exit control.
  - IA32_EFER (64 bits). This field is supported only on processors that support either the 1-setting of the “load IA32_EFER” VM-entry control or that of the “save IA32_EFER” VM-exit control.

- The register SMBASE (32 bits). This register contains the base address of the logical processor’s SMRAM image.

### 24.4.2 Guest Non-Register State

In addition to the register state described in Section 24.4.1, the guest-state area includes the following fields that characterize guest state but which do not correspond to processor registers:

- **Activity state** (32 bits). This field identifies the logical processor’s activity state. When a logical processor is executing instructions normally, it is in the **active state**. Execution of certain instructions and the occurrence of certain events may cause a logical processor to transition to an **inactive state** in which it ceases to execute instructions.
  
  The following activity states are defined:\(^2\)
  - 0: **Active**. The logical processor is executing instructions normally.

---

1. In protected mode, CPL is also associated with the RPL field in the CS selector. However, the RPL fields are not meaningful in real-address mode or in virtual-8086 mode.
2. Execution of the MWAIT instruction may put a logical processor into an inactive state. However, this VMCS field never reflects this state. See Section 27.1.
— 1: **HLT.** The logical processor is inactive because it executed the HLT instruction.

— 2: **Shutdown.** The logical processor is inactive because it incurred a **triple fault**\(^1\) or some other serious error.

— 3: **Wait-for-SIPI.** The logical processor is inactive because it is waiting for a startup-IPI (SIPI).

Future processors may include support for other activity states. Software should read the VMX capability MSR IA32_VMX_MISC (see Appendix A.6) to determine what activity states are supported.

**Interruptibility state** (32 bits). The IA-32 architecture includes features that permit certain events to be blocked for a period of time. This field contains information about such blocking. Details and the format of this field are given in Table 24-3.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Bit Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Blocking by STI</td>
<td>See the “STI—Set Interrupt Flag” section in Chapter 4 of the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual</em>, Volume 2B. Execution of STI with RFLAGS.IF = 0 blocks interrupts (and, optionally, other events) for one instruction after its execution. Setting this bit indicates that this blocking is in effect.</td>
</tr>
<tr>
<td>1</td>
<td>Blocking by MOV SS</td>
<td>See the “MOV—Move a Value from the Stack” from Chapter 3 of the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual</em>, Volume 2A, and “POP—Pop a Value from the Stack” from Chapter 4 of the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual</em>, Volume 2B, and Section 6.8.3 in the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual</em>, Volume 3A. Execution of a MOV to SS or a POP to SS blocks interrupts for one instruction after its execution. In addition, certain debug exceptions are inhibited between a MOV to SS or a POP to SS and a subsequent instruction. Setting this bit indicates that the blocking of all these events is in effect. This document uses the term “blocking by MOV SS,” but it applies equally to POP SS.</td>
</tr>
<tr>
<td>2</td>
<td>Blocking by SMI</td>
<td>See Section 34.2. System-management interrupts (SMIs) are disabled while the processor is in system-management mode (SMM). Setting this bit indicates that blocking of SMIs is in effect.</td>
</tr>
<tr>
<td>3</td>
<td>Blocking by NMI</td>
<td>See Section 6.7.1 in the <em>Intel® 64 and IA-32 Architectures Software Developer's Manual</em>, Volume 3A and Section 34.8. Delivery of a non-maskable interrupt (NMI) or a system-management interrupt (SMI) blocks subsequent NMIs until the next execution of IRET. See Section 25.3 for how this behavior of IRET may change in VMX non-root operation. Setting this bit indicates that blocking of NMIs is in effect. Clearing this bit does not imply that NMIs are not (temporarily) blocked for other reasons. If the “virtual NMIs” VM-execution control (see Section 24.6.1) is 1, this bit does not control the blocking of NMIs. Instead, it refers to “virtual-NMI blocking” (the fact that guest software is not ready for an NMI).</td>
</tr>
<tr>
<td>31:4</td>
<td>Reserved</td>
<td>VM entry will fail if these bits are not 0. See Section 26.3.1.5.</td>
</tr>
</tbody>
</table>

**Pending debug exceptions** (64 bits; 32 bits on processors that do not support Intel 64 architecture). IA-32 processors may recognize one or more debug exceptions without immediately delivering them.\(^2\) This field contains information about such exceptions. This field is described in Table 24-4.

---

1. A triple fault occurs when a logical processor encounters an exception while attempting to deliver a double fault.

2. For example, execution of a MOV to SS or a POP to SS may inhibit some debug exceptions for one instruction. See Section 6.8.3 of *Intel® 64 and IA-32 Architectures Software Developer's Manual*, Volume 3A. In addition, certain events incident to an instruction (for example, an INIT signal) may take priority over debug traps generated by that instruction. See Table 6-2 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual*, Volume 3A.
• **VMCS link pointer** (64 bits). If the "VMCS shadowing" VM-execution control is 1, the VMREAD and VMWRITE instructions access the VMCS referenced by this pointer (see Section 24.10). Otherwise, software should set this field to FFFFFFFF_FFFFFFFFH to avoid VM-entry failures (see Section 26.3.1.5).

• **VMX-preemption timer value** (32 bits). This field is supported only on processors that support the 1-setting of the "activate VMX-preemption timer" VM-execution control. This field contains the value that the VMX-preemption timer will use following the next VM entry with that setting. See Section 25.5.1 and Section 26.6.4.

• **Page-directory-pointer-table entries** (PDPTEs; 64 bits each). These four (4) fields (PDPTE0, PDPTE1, PDPTE2, and PDPTE3) are supported only on processors that support the 1-setting of the "enable EPT" VM-execution control. They correspond to the PDPTEs referenced by CR3 when PAE paging is in use (see Section 4.4 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*). They are used only if the "enable EPT" VM-execution control is 1.

• **Guest interrupt status** (16 bits). This field is supported only on processors that support the 1-setting of the "virtual-interrupt delivery" VM-execution control. It characterizes part of the guest's virtual-APIC state and does not correspond to any processor or APIC registers. It comprises two 8-bit subfields:
  
  — **Requesting virtual interrupt (RVI).** This is the low byte of the guest interrupt status. The processor treats this value as the vector of the highest priority virtual interrupt that is requesting service. (The value 0 implies that there is no such interrupt.)
  
  — **Servicing virtual interrupt (SVI).** This is the high byte of the guest interrupt status. The processor treats this value as the vector of the highest priority virtual interrupt that is in service. (The value 0 implies that there is no such interrupt.)

See Chapter 29 for more information on the use of this field.

• **PML index** (16 bits). This field is supported only on processors that support the 1-setting of the "enable PML" VM-execution control. It contains the logical index of the next entry in the page-modification log. Because the page-modification log comprises 512 entries, the PML index is typically a value in the range 0–511. Details of the page-modification log and use of the PML index are given in Section 28.2.5.

### Table 24-4. Format of Pending-Debug-Exceptions

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Bit Name</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>B3 – B0</td>
<td>When set, each of these bits indicates that the corresponding breakpoint condition was met. Any of these bits may be set even if the corresponding enabling bit in DR7 is not set.</td>
</tr>
<tr>
<td>11:4</td>
<td>Reserved</td>
<td>VM entry fails if these bits are not 0. See Section 26.3.1.5.</td>
</tr>
<tr>
<td>12</td>
<td>Enabled break</td>
<td>When set, this bit indicates that at least one data or I/O breakpoint was met and was enabled in DR7.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
<td>VM entry fails if this bit is not 0. See Section 26.3.1.5.</td>
</tr>
<tr>
<td>14</td>
<td>BS</td>
<td>When set, this bit indicates that a debug exception would have been triggered by single-step execution mode.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td>VM entry fails if this bit is not 0. See Section 26.3.1.5.</td>
</tr>
<tr>
<td>16</td>
<td>RTM</td>
<td>When set, this bit indicates that a debug exception (#DB) or a breakpoint exception (#BP) occurred inside an RTM region while advanced debugging of RTM transactional regions was enabled (see Section 15.3.7, “RTM-Enabled Debugger Support,” of <em>Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1</em>).</td>
</tr>
<tr>
<td>63:17</td>
<td>Reserved</td>
<td>VM entry fails if these bits are not 0. See Section 26.3.1.5. Bits 63:32 exist only on processors that support Intel 64 architecture.</td>
</tr>
</tbody>
</table>

**NOTES:**

1. In general, the format of this field matches that of DR6. However, DR6 clears bit 16 to indicate an RTM-related exception, while this field sets the bit to indicate that condition.

---

**NOTES:**

This format matches that of DR6. However, DR6 clears bit 16 to indicate an RTM-related exception, while this field sets the bit to indicate that condition.

---

**NOTES:**

1. In general, the format of this field matches that of DR6. However, DR6 clears bit 16 to indicate an RTM-related exception, while this field sets the bit to indicate that condition.
24.5 HOST-STATE AREA

This section describes fields contained in the host-state area of the VMCS. As noted earlier, processor state is loaded from these fields on every VM exit (see Section 27.5).

All fields in the host-state area correspond to processor registers:

- CR0, CR3, and CR4 (64 bits each; 32 bits on processors that do not support Intel 64 architecture).
- RSP and RIP (64 bits each; 32 bits on processors that do not support Intel 64 architecture).
- Selector fields (16 bits each) for the segment registers CS, SS, DS, ES, FS, GS, and TR. There is no field in the host-state area for the LDTR selector.
- Base-address fields for FS, GS, TR, GDTR, and IDTR (64 bits each; 32 bits on processors that do not support Intel 64 architecture).
- The following MSRs:
  - IA32_SYSENTER_CS (32 bits)
  - IA32_SYSENTER_ESP and IA32_SYSENTER_EIP (64 bits; 32 bits on processors that do not support Intel 64 architecture).
  - IA32_PERF_GLOBAL_CTRL (64 bits). This field is supported only on processors that support the 1-setting of the "load IA32_PERF_GLOBAL_CTRL" VM-exit control.
  - IA32_PAT (64 bits). This field is supported only on processors that support the 1-setting of the "load IA32_PAT" VM-exit control.
  - IA32_EFER (64 bits). This field is supported only on processors that support the 1-setting of the "load IA32_EFER" VM-exit control.

In addition to the state identified here, some processor state components are loaded with fixed values on every VM exit; there are no fields corresponding to these components in the host-state area. See Section 27.5 for details of how state is loaded on VM exits.

24.6 VM-EXECUTION CONTROL FIELDS

The VM-execution control fields govern VMX non-root operation. These are described in Section 24.6.1 through Section 24.6.8.

24.6.1 Pin-Based VM-Execution Controls

The pin-based VM-execution controls constitute a 32-bit vector that governs the handling of asynchronous events (for example: interrupts).\(^1\) Table 24-5 lists the controls. See Chapter 27 for how these controls affect processor behavior in VMX non-root operation.

---

1. Some asynchronous events cause VM exits regardless of the settings of the pin-based VM-execution controls (see Section 25.2).
All other bits in this field are reserved, some to 0 and some to 1. Software should consult the VMX capability MSRs IA32_VMX_PINBASED_CTLS and IA32_VMX_TRUE_PINBASED_CTLS (see Appendix A.3.1) to determine how to set reserved bits. Failure to set reserved bits properly causes subsequent VM entries to fail (see Section 26.2.1.1).

The first processors to support the virtual-machine extensions supported only the 1-settings of bits 1, 2, and 4. The VMX capability MSR IA32_VMX_PINBASED_CTLS will always report that these bits must be 1. Logical processors that support the 0-settings of any of these bits will support the VMX capability MSR IA32_VMX_TRUE_PINBASED_CTLS MSR, and software should consult this MSR to discover support for the 0-settings of these bits. Software that is not aware of the functionality of any one of these bits should set that bit to 1.

### 24.6.2 Processor-Based VM-Execution Controls

The processor-based VM-execution controls constitute two 32-bit vectors that govern the handling of synchronous events, mainly those caused by the execution of specific instructions. These are the primary processor-based VM-execution controls and the secondary processor-based VM-execution controls.

Table 24-6 lists the primary processor-based VM-execution controls. See Chapter 25 for more details of how these controls affect processor behavior in VMX non-root operation.

#### Table 24-6. Definitions of Primary Processor-Based VM-Execution Controls

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Interrupt-window exiting</td>
<td>If this control is 1, a VM exit occurs at the beginning of any instruction if RFLAGS.IF = 1 and there are no other blocking of interrupts (see Section 24.4.2).</td>
</tr>
<tr>
<td>3</td>
<td>Use TSC offsetting</td>
<td>This control determines whether executions of RDTSC, executions of RDTSCP, and executions of RDMSR that read from the IA32_TIME_STAMP_COUNTER MSR return a value modified by the TSC offset field (see Section 24.6.5 and Section 25.3).</td>
</tr>
<tr>
<td>7</td>
<td>HLT exiting</td>
<td>This control determines whether executions of HLT cause VM exits.</td>
</tr>
<tr>
<td>9</td>
<td>INVLPG exiting</td>
<td>This determines whether executions of INVLPG cause VM exits.</td>
</tr>
<tr>
<td>10</td>
<td>MWAIT exiting</td>
<td>This control determines whether executions of MWAIT cause VM exits.</td>
</tr>
<tr>
<td>11</td>
<td>RDPMC exiting</td>
<td>This control determines whether executions of RDPMC cause VM exits.</td>
</tr>
<tr>
<td>12</td>
<td>RDTSC exiting</td>
<td>This control determines whether executions of RDTSC and RDTSCP cause VM exits.</td>
</tr>
</tbody>
</table>

1. Some instructions cause VM exits regardless of the settings of the processor-based VM-execution controls (see Section 25.1.2), as do task switches (see Section 25.2).
Table 24-6. Definitions of Primary Processor-Based VM-Execution Controls (Contd.)

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CR3-load exiting</td>
<td>Whether executions of MOV to CR3 cause VM exits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The first processors to support the virtual-machine extensions supported the 1-setting of this control.</td>
</tr>
<tr>
<td>16</td>
<td>CR3-store exiting</td>
<td>Whether executions of MOV from CR3 cause VM exits.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The first processors to support the virtual-machine extensions supported the 1-setting of this control.</td>
</tr>
<tr>
<td>19</td>
<td>CR8-load exiting</td>
<td>Whether executions of MOV to CR8 cause VM exits.</td>
</tr>
<tr>
<td>20</td>
<td>CR8-store exiting</td>
<td>Whether executions of MOV from CR8 cause VM exits.</td>
</tr>
<tr>
<td>21</td>
<td>Use TPR shadow</td>
<td>Enables TPR virtualization and other APIC-virtualization features.</td>
</tr>
<tr>
<td>22</td>
<td>NMI-window exiting</td>
<td>Whether an NMI causes a VM exit.</td>
</tr>
<tr>
<td>23</td>
<td>MOV-DR exiting</td>
<td>Whether MOV DR causes VM exits.</td>
</tr>
<tr>
<td>24</td>
<td>Unconditional I/O exiting</td>
<td>Whether executions of I/O instructions (IN, INSB/INSD, OUT, and OUTS/OUTSB/OUTSW/OUTSD) cause VM exits.</td>
</tr>
<tr>
<td>25</td>
<td>Use I/O bitmaps</td>
<td>Whether I/O bitmaps are used to restrict executions of I/O instructions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The first processors to support the virtual-machine extensions supported the 1-setting of this control.</td>
</tr>
<tr>
<td>26</td>
<td>Move trap flag</td>
<td>If this control is 1, a VM exit occurs at the beginning of any instruction if there is no virtual-NMI blocking.</td>
</tr>
<tr>
<td>28</td>
<td>Use MSR bitmaps</td>
<td>Whether MSR bitmaps are used to control execution of the RDMSR and WRMSR instructions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The first processors to support the virtual-machine extensions supported the 1-setting of this control.</td>
</tr>
<tr>
<td>29</td>
<td>MONITOR exiting</td>
<td>Whether executions of MONITOR cause VM exits.</td>
</tr>
<tr>
<td>30</td>
<td>PAUSE exiting</td>
<td>Whether executions of PAUSE cause VM exits.</td>
</tr>
<tr>
<td>31</td>
<td>Activate secondary controls</td>
<td>Whether the secondary processor-based VM-execution controls are used. If this control is 0, the logical processor operates as if all the secondary processor-based VM-execution controls were also 0.</td>
</tr>
</tbody>
</table>

All other bits in this field are reserved, some to 0 and some to 1. Software should consult the VMX capability MSRs IA32_VMX_PROCBASED_CTLs and IA32_VMX_TRUE_PROCBASED_CTLs (see Appendix A.3.2) to determine how to set reserved bits. Failure to set reserved bits properly causes subsequent VM entries to fail (see Section 26.2.1.1).

The first processors to support the virtual-machine extensions supported only the 1-settings of bits 1, 4–6, 8, 13–16, and 26. The VMX capability MSR IA32_VMX_PROCBASED_CTLs will always report that these bits must be 1.

Logical processors that support the 0-settings of any of these bits will support the VMX capability MSR IA32_VMX_TRUE_PROCBASED_CTLs MSR, and software should consult this MSR to discover support for the 0-settings of these bits. Software that is not aware of the functionality of any one of these bits should set that bit to 1.

Bit 31 of the primary processor-based VM-execution controls determines whether the secondary processor-based VM-execution controls are used. If that bit is 0, VM entry and VMX non-root operation function as if all the secondary processor-based VM-execution controls were 0. Processors that support only the 0-setting of bit 31 of the primary processor-based VM-execution controls do not support the secondary processor-based VM-execution controls.
Table 24-7 lists the secondary processor-based VM-execution controls. See Chapter 25 for more details of how these controls affect processor behavior in VMX non-root operation.

### Table 24-7. Definitions of Secondary Processor-Based VM-Execution Controls

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Virtualize APIC accesses</td>
<td>If this control is 1, the logical processor treats specially accesses to the page with the APIC-access address. See Section 29.4.</td>
</tr>
<tr>
<td>1</td>
<td>Enable EPT</td>
<td>If this control is 1, extended page tables (EPT) are enabled. See Section 28.2.</td>
</tr>
<tr>
<td>2</td>
<td>Descriptor-table exiting</td>
<td>This control determines whether executions of LGDT, LIDT, LLDT, LTR, SGDT, SIDT, SLDT, and STR cause VM exits.</td>
</tr>
<tr>
<td>3</td>
<td>Enable RDTSCP</td>
<td>If this control is 0, any execution of RDTSCP causes an invalid-opcode exception (#UD).</td>
</tr>
<tr>
<td>4</td>
<td>Virtualize x2APIC mode</td>
<td>If this control is 1, the logical processor treats specially RDMSR and WRMSR to APIC MSRs (in the range 800H–8FFH). See Section 29.5.</td>
</tr>
<tr>
<td>5</td>
<td>Enable VPID</td>
<td>If this control is 1, cached translations of linear addresses are associated with a virtual-processor identifier (VPID). See Section 28.1.</td>
</tr>
<tr>
<td>6</td>
<td>WBINVD exiting</td>
<td>This control determines whether executions of WBINVD cause VM exits.</td>
</tr>
<tr>
<td>7</td>
<td>Unrestricted guest</td>
<td>This control determines whether guest software may run in unpaged protected mode or in real-address mode.</td>
</tr>
<tr>
<td>8</td>
<td>Virtualize APIC access</td>
<td>If this control is 1, the logical processor will virtualize certain APIC accesses. See Section 29.4 and Section 29.5.</td>
</tr>
<tr>
<td>9</td>
<td>Virtual-interrupt delivery</td>
<td>This control enables the evaluation and delivery of pending virtual interrupts as well as the emulation of writes to the APIC registers that control interrupt prioritization.</td>
</tr>
<tr>
<td>10</td>
<td>PAUSE-loop exiting</td>
<td>This control determines whether a series of executions of PAUSE can cause a VM exit (see Section 24.6.13 and Section 25.1.3).</td>
</tr>
<tr>
<td>11</td>
<td>RDRAND exiting</td>
<td>This control determines whether executions of RDRAND cause VM exits.</td>
</tr>
<tr>
<td>12</td>
<td>Enable INVPCID</td>
<td>If this control is 0, any execution of INVPCID causes a #UD.</td>
</tr>
<tr>
<td>13</td>
<td>Enable VM functions</td>
<td>Setting this control to 1 enables use of the VMFUNC instruction in VMX non-root operation. See Section 25.5.5.</td>
</tr>
<tr>
<td>14</td>
<td>VMCS shadowing</td>
<td>If this control is 1, executions of VMREAD and VMWRITE in VMX non-root operation may access a shadow VMCS (instead of causing VM exits). See Section 24.10 and Section 30.3.</td>
</tr>
<tr>
<td>16</td>
<td>RDSEED exiting</td>
<td>This control determines whether executions of RDSEED cause VM exits.</td>
</tr>
<tr>
<td>17</td>
<td>Enable PML</td>
<td>If this control is 1, an access to a guest-physical address that sets an EPT dirty bit first adds an entry to the page-modification log. See Section 28.2.5.</td>
</tr>
<tr>
<td>18</td>
<td>EPT-violation #VE</td>
<td>If this control is 1, EPT violations may cause virtualization exceptions (#VE) instead of VM exits. See Section 25.5.6.</td>
</tr>
<tr>
<td>20</td>
<td>Enable XSAVES/XRSTORS</td>
<td>If this control is 0, any execution of XSAVES or XRSTORS causes a #UD.</td>
</tr>
<tr>
<td>25</td>
<td>Use TSC scaling</td>
<td>This control determines whether executions of RDTS, executions of RDTSCP, and executions of RDMSR that read from the IA32_TIME_STAMP_COUNTER MSR return a value modified by the TSC multiplier field (see Section 24.6.5 and Section 25.3).</td>
</tr>
</tbody>
</table>

All other bits in this field are reserved to 0. Software should consult the VMX capability MSR IA32_VMX_PROCBASED_CTLS2 (see Appendix A.3.3) to determine which bits may be set to 1. Failure to clear reserved bits causes subsequent VM entries to fail (see Section 26.2.1.1).

### 24.6.3 Exception Bitmap

The **exception bitmap** is a 32-bit field that contains one bit for each exception. When an exception occurs, its vector is used to select a bit in this field. If the bit is 1, the exception causes a VM exit. If the bit is 0, the exception is delivered normally through the IDT, using the descriptor corresponding to the exception’s vector.

Whether a page fault (exception with vector 14) causes a VM exit is determined by bit 14 in the exception bitmap as well as the error code produced by the page fault and two 32-bit fields in the VMCS (the **page-fault error-code mask** and **page-fault error-code match**). See Section 25.2 for details.

### 24.6.4 I/O-Bitmap Addresses

The VM-execution control fields include the 64-bit physical addresses of **I/O bitmaps** A and B (each of which are 4 KBytes in size). I/O bitmap A contains one bit for each I/O port in the range 0000H through 7FFFH; I/O bitmap B contains bits for ports in the range 8000H through FFFFH.

A logical processor uses these bitmaps if and only if the “use I/O bitmaps” control is 1. If the bitmaps are used, execution of an I/O instruction causes a VM exit if any bit in the I/O bitmaps corresponding to a port it accesses is 1. See Section 25.1.3 for details. If the bitmaps are used, their addresses must be 4-KByte aligned.

### 24.6.5 Time-Stamp Counter Offset and Multiplier

The VM-execution control fields include a 64-bit **TSC-offset** field. If the “RDTSC exiting” control is 0 and the “use TSC offsetting” control is 1, this field controls executions of the RDTSC and RDTSCP instructions. It also controls executions of the RDMSR instruction that read from the IA32_TIME_STAMP_COUNTER MSR. For all of these, the value of the TSC offset is added to the value of the time-stamp counter, and the sum is returned to guest software in EDX:EAX.

Processors that support the 1-setting of the “use TSC scaling” control also support a 64-bit **TSC-multiplier** field. If this control is 1 (and the "RDTSC exiting" control is 0 and the "use TSC offsetting" control is 1), this field also affects the executions of the RDTSC, RDTSCP, and RDMSR instructions identified above. Specifically, the contents of the time-stamp counter is first multiplied by the TSC multiplier before adding the TSC offset.

See Chapter 27 for a detailed treatment of the behavior of RDTSC, RDTSCP, and RDMSR in VMX non-root operation.

### 24.6.6 Guest/Host Masks and Read Shadows for CR0 and CR4

VM-execution control fields include **guest/host masks** and **read shadows** for the CR0 and CR4 registers. These fields control executions of instructions that access those registers (including CLTS, LMSW, MOV CR, and SMSW). They are 64 bits on processors that support Intel 64 architecture and 32 bits on processors that do not.

In general, bits set to 1 in a guest/host mask correspond to bits “owned” by the host:

- Guest attempts to set them (using CLTS, LMSW, or MOV to CR) to values differing from the corresponding bits in the corresponding read shadow cause VM exits.
- Guest reads (using MOV from CR or SMSW) return values for these bits from the corresponding read shadow.

Bits cleared to 0 correspond to bits “owned” by the guest; guest attempts to modify them succeed and guest reads return values for these bits from the control register itself.

See Chapter 27 for details regarding how these fields affect VMX non-root operation.

### 24.6.7 CR3-Target Controls

The VM-execution control fields include a set of 4 **CR3-target values** and a **CR3-target count**. The CR3-target values each have 64 bits on processors that support Intel 64 architecture and 32 bits on processors that do not. The CR3-target count has 32 bits on all processors.

An execution of MOV to CR3 in VMX non-root operation does not cause a VM exit if its source operand matches one of these values. If the CR3-target count is \( n \), only the first \( n \) CR3-target values are considered; if the CR3-target count is 0, MOV to CR3 always causes a VM exit.

There are no limitations on the values that can be written for the CR3-target values. VM entry fails (see Section 26.2) if the CR3-target count is greater than 4.
Future processors may support a different number of CR3-target values. Software should read the VMX capability MSR IA32_VMX_MISC (see Appendix A.6) to determine the number of values supported.

24.6.8 Controls for APIC Virtualization

There are three mechanisms by which software accesses registers of the logical processor’s local APIC:

- If the local APIC is in xAPIC mode, it can perform memory-mapped accesses to addresses in the 4-KByte page referenced by the physical address in the IA32_APIC_BASE MSR (see Section 10.4.4, “Local APIC Status and Location” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A and Intel® 64 Architecture Processor Topology Enumeration).

- If the local APIC is in x2APIC mode, it can accesses the local APIC’s registers using the RDMSR and WRMSR instructions (see Intel® 64 Architecture Processor Topology Enumeration).

- In 64-bit mode, it can access the local APIC’s task-priority register (TPR) using the MOV CR8 instruction.

There are five processor-based VM-execution controls (see Section 24.6.2) that control such accesses. There are “use TPR shadow”, “virtualize APIC accesses”, “virtualize x2APIC mode”, “virtual-interrupt delivery”, and “APIC-register virtualization”. These controls interact with the following fields:

- **APIC-access address** (64 bits). This field contains the physical address of the 4-KByte APIC-access page. If the “virtualize APIC accesses” VM-execution control is 1, access to this page may cause VM exits or be virtualized by the processor. See Section 29.4.

  The APIC-access address exists only on processors that support the 1-setting of the “virtualize APIC accesses” VM-execution control.

- **Virtual-APIC address** (64 bits). This field contains the physical address of the 4-KByte virtual-APIC page. The processor uses the virtual-APIC page to virtualize certain accesses to APIC registers and to manage virtual interrupts; see Chapter 29.

  Depending on the setting of the controls indicated earlier, the virtual-APIC page may be accessed by the following operations:

  - The MOV CR8 instructions (see Section 29.3).
  - Accesses to the APIC-access page if, in addition, the “virtualize APIC accesses” VM-execution control is 1 (see Section 29.4).
  - The RDMSR and WRMSR instructions if, in addition, the value of ECX is in the range 800H–8FFH (indicating an APIC MSR) and the “virtualize x2APIC mode” VM-execution control is 1 (see Section 29.5).

  If the “use TPR shadow” VM-execution control is 1, VM entry ensures that the virtual-APIC address is 4-KByte aligned. The virtual-APIC address exists only on processors that support the 1-setting of the “use TPR shadow” VM-execution control.

- **TPR threshold** (32 bits). Bits 3:0 of this field determine the threshold below which bits 7:4 of VTPR (see Section 29.1.1) cannot fall. If the “virtual-interrupt delivery” VM-execution control is 0, a VM exit occurs after an operation (e.g., an execution of MOV to CR8) that reduces the value of those bits below the TPR threshold. See Section 29.1.2.

  The TPR threshold exists only on processors that support the 1-setting of the “use TPR shadow” VM-execution control.

- **EOI-exit bitmap** (4 fields; 64 bits each). These fields are supported only on processors that support the 1-setting of the “virtual-interrupt delivery” VM-execution control. They are used to determine which virtualized writes to the APIC’s EOI register cause VM exits:

  - EOI_EXIT0 contains bits for vectors from 0 (bit 0) to 63 (bit 63).
  - EOI_EXIT1 contains bits for vectors from 64 (bit 0) to 127 (bit 63).
  - EOI_EXIT2 contains bits for vectors from 128 (bit 0) to 191 (bit 63).
  - EOI_EXIT3 contains bits for vectors from 192 (bit 0) to 255 (bit 63).

  See Section 29.1.4 for more information on the use of this field.

  1. If the local APIC does not support x2APIC mode, it is always in xAPIC mode.
• **Posted-interrupt notification vector** (16 bits). This field is supported only on processors that support the 1-setting of the "process posted interrupts" VM-execution control. Its low 8 bits contain the interrupt vector that is used to notify a logical processor that virtual interrupts have been posted. See Section 29.6 for more information on the use of this field.

• **Posted-interrupt descriptor address** (64 bits). This field is supported only on processors that support the 1-setting of the "process posted interrupts" VM-execution control. It is the physical address of a 64-byte aligned posted interrupt descriptor. See Section 29.6 for more information on the use of this field.

### 24.6.9 MSR-Bitmap Address

On processors that support the 1-setting of the "use MSR bitmaps" VM-execution control, the VM-execution control fields include the 64-bit physical address of four contiguous **MSR bitmaps**, which are each 1-KByte in size. This field does not exist on processors that do not support the 1-setting of that control. The four bitmaps are:

• **Read bitmap for low MSRs** (located at the MSR-bitmap address). This contains one bit for each MSR address in the range 00000000H to 00001FFFH. The bit determines whether an execution of RDMSR applied to that MSR causes a VM exit.

• **Read bitmap for high MSRs** (located at the MSR-bitmap address plus 1024). This contains one bit for each MSR address in the range C0000000H to C0001FFFH. The bit determines whether an execution of RDMSR applied to that MSR causes a VM exit.

• **Write bitmap for low MSRs** (located at the MSR-bitmap address plus 2048). This contains one bit for each MSR address in the range 00000000H to 00001FFFH. The bit determines whether an execution of WRMSR applied to that MSR causes a VM exit.

• **Write bitmap for high MSRs** (located at the MSR-bitmap address plus 3072). This contains one bit for each MSR address in the range C0000000H to C0001FFFH. The bit determines whether an execution of WRMSR applied to that MSR causes a VM exit.

A logical processor uses these bitmaps if and only if the "use MSR bitmaps" control is 1. If the bitmaps are used, an execution of RDMSR or WRMSR causes a VM exit if the value of RCX is in neither of the ranges covered by the bitmaps or if the appropriate bit in the MSR bitmaps (corresponding to the instruction and the RCX value) is 1. See Section 25.1.3 for details. If the bitmaps are used, their address must be 4-KByte aligned.

### 24.6.10 Executive-VMCS Pointer

The executive-VMCS pointer is a 64-bit field used in the dual-monitor treatment of system-management interrupts (SMIs) and system-management mode (SMM). SMM VM exits save this field as described in Section 34.15.2. VM entries that return from SMM use this field as described in Section 34.15.4.

### 24.6.11 Extended-Page-Table Pointer (EPTP)

The **extended-page-table pointer** (EPTP) contains the address of the base of EPT PML4 table (see Section 28.2.2), as well as other EPT configuration information. The format of this field is shown in Table 24-8.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>EPT paging-structure memory type (see Section 28.2.6):</td>
</tr>
<tr>
<td></td>
<td>Other values are reserved.¹</td>
</tr>
<tr>
<td>5:3</td>
<td>This value is 1 less than the EPT page-walk length (see Section 28.2.2)</td>
</tr>
<tr>
<td>6</td>
<td>Setting this control to 1 enables accessed and dirty flags for EPT (see Section 28.2.4)²</td>
</tr>
</tbody>
</table>
24.6.12 Virtual-Processor Identifier (VPID)

The virtual-processor identifier (VPID) is a 16-bit field. It exists only on processors that support the 1-setting of the “enable VPID” VM-execution control. See Section 28.1 for details regarding the use of this field.

24.6.13 Controls for PAUSE-Loop Exiting

On processors that support the 1-setting of the “PAUSE-loop exiting” VM-execution control, the VM-execution control fields include the following 32-bit fields:

- **PLE_Gap.** Software can configure this field as an upper bound on the amount of time between two successive executions of PAUSE in a loop.
- **PLE_Window.** Software can configure this field as an upper bound on the amount of time a guest is allowed to execute a PAUSE loop.

These fields measure time based on a counter that runs at the same rate as the timestamp counter (TSC). See Section 25.1.3 for more details regarding PAUSE-loop exiting.

24.6.14 Control Field for Page-Modification Logging

The PML address is a 64-bit field. It is the 4-KByte aligned address of the page-modification log. The page-modification log consists of 512 64-bit entries. It is used for the page-modification logging feature. Details of the page-modification logging are given in Section 28.2.5.

If the "enable PML" VM-execution control is 1, VM entry ensures that the PML address is 4-KByte aligned. The PML address exists only on processors that support the 1-setting of the "enable PML" VM-execution control.

24.6.15 VM-Function Controls

The VM-function controls constitute a 64-bit vector that governs use of the VMFUNC instruction in VMX non-root operation. This field is supported only on processors that support the 1-settings of both the "activate secondary controls" primary processor-based VM-execution control and the "enable VM functions" secondary processor-based VM-execution control.
Table 24-9 lists the VM-function controls. See Section 25.5.5 for more details of how these controls affect processor behavior in VMX non-root operation.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EPTP switching</td>
<td>The EPTP-switching VM function changes the EPT pointer to a value chosen from the EPTP list. See Section 25.5.5.3.</td>
</tr>
</tbody>
</table>

All other bits in this field are reserved to 0. Software should consult the VMX capability MSR IA32_VMX_VMFUNC (see Appendix A.11) to determine which bits are reserved. Failure to clear reserved bits causes subsequent VM entries to fail (see Section 26.2.1.1).

Processors that support the 1-setting of the “EPTP switching” VM-function control also support a 64-bit field called the **EPTP-list address**. This field contains the physical address of the 4-KByte **EPTP list**. The EPTP list comprises 512 8-Byte entries (each an EPTP value) and is used by the EPTP-switching VM function (see Section 25.5.5.3).

### 24.6.16 VMCS Shadowing Bitmap Addresses

On processors that support the 1-setting of the “VMCS shadowing” VM-execution control, the VM-execution control fields include the 64-bit physical addresses of the **VMREAD bitmap** and the **VMWRITE bitmap**. Each bitmap is 4 KBytes in size and thus contains 32 KBits. The addresses are the **VMREAD-bitmap address** and the **VMWRITE-bitmap address**.

If the “VMCS shadowing” VM-execution control is 1, executions of VMREAD and VMWRITE may consult these bitmaps (see Section 24.10 and Section 30.3).

### 24.6.17 Controls for Virtualization Exceptions

On processors that support the 1-setting of the “EPT-violation #VE” VM-execution control, the VM-execution control fields include the following:

- **Virtualization-exception information address** (64 bits). This field contains the physical address of the virtualization-exception information area. When a logical processor encounters a virtualization exception, it saves virtualization-exception information at the virtualization-exception information address; see Section 25.5.6.2.

- **EPTP index** (16 bits). When an EPT violation causes a virtualization exception, the processor writes the value of this field to the virtualization-exception information area. The EPTP-switching VM function updates this field (see Section 25.5.5.3).

### 24.6.18 XSS-Exiting Bitmap

On processors that support the 1-setting of the “enable XSAVES/XRSTORS” VM-execution control, the VM-execution control fields include a 64-bit **XSS-exiting bitmap**. If the “enable XSAVES/XRSTORS” VM-execution control is 1, executions of XSAVES and XRSTORS may consult this bitmap (see Section 25.1.3 and Section 25.3).

### 24.7 VM-EXIT CONTROL FIELDS

The VM-exit control fields govern the behavior of VM exits. They are discussed in Section 24.7.1 and Section 24.7.2.

#### 24.7.1 VM-Exit Controls

The **VM-exit controls** constitute a 32-bit vector that governs the basic operation of VM exits. Table 24-10 lists the controls supported. See Chapter 27 for complete details of how these controls affect VM exits.
### Table 24-10. Definitions of VM-Exit Controls

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Save debug controls</td>
<td>This control determines whether DR7 and the IA32_DEBUGCTL MSR are saved on VM exit. The first processors to support the virtual-machine extensions supported only the 1-setting of this control.</td>
</tr>
<tr>
<td>9</td>
<td>Host address-space size</td>
<td>On processors that support Intel 64 architecture, this control determines whether a logical processor is in 64-bit mode after the next VM exit. Its value is loaded into CS.L, IA32_EFER.LME, and IA32_EFER.LMA on every VM exit. This control must be 0 on processors that do not support Intel 64 architecture.</td>
</tr>
<tr>
<td>12</td>
<td>Load IA32_PERF_GLOBAL_CTRL</td>
<td>This control determines whether the IA32_PERF_GLOBAL_CTRL MSR is loaded on VM exit.</td>
</tr>
<tr>
<td>15</td>
<td>Acknowledge interrupt on exit</td>
<td>This control affects VM exits due to external interrupts:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• If such a VM exit occurs and this control is 1, the logical processor acknowledges the interrupt controller, acquiring the interrupt's vector. The vector is stored in the VM-exit interruption-information field, which is marked valid.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• If such a VM exit occurs and this control is 0, the interrupt is not acknowledged and the VM-exit interruption-information field is marked invalid.</td>
</tr>
<tr>
<td>18</td>
<td>Save IA32_PAT</td>
<td>This control determines whether the IA32_PAT MSR is saved on VM exit.</td>
</tr>
<tr>
<td>19</td>
<td>Load IA32_PAT</td>
<td>This control determines whether the IA32_PAT MSR is loaded on VM exit.</td>
</tr>
<tr>
<td>20</td>
<td>Save IA32_EFER</td>
<td>This control determines whether the IA32_EFER MSR is saved on VM exit.</td>
</tr>
<tr>
<td>21</td>
<td>Load IA32_EFER</td>
<td>This control determines whether the IA32_EFER MSR is loaded on VM exit.</td>
</tr>
<tr>
<td>22</td>
<td>Save VMX-preemption timer value</td>
<td>This control determines whether the value of the VMX-preemption timer is saved on VM exit.</td>
</tr>
</tbody>
</table>

**NOTES:**

1. Since Intel 64 architecture specifies that IA32_EFER.LMA is always set to the logical-AND of CR0.PG and IA32_EFER.LME, and since CR0.PG is always 1 in VMX operation, IA32_EFER.LMA is always identical to IA32_EFER.LME in VMX operation.

All other bits in this field are reserved, some to 0 and some to 1. Software should consult the VMX capability MSRs IA32_VMX_EXIT_CTLS and IA32_VMX_TRUE_EXIT_CTLS (see Appendix A.4) to determine how it should set the reserved bits. Failure to set reserved bits properly causes subsequent VM entries to fail (see Section 26.2.1.2).

The first processors to support the virtual-machine extensions supported only the 1-settings of bits 0–8, 10, 11, 13, 14, 16, and 17. The VMX capability MSR IA32_VMX_EXIT_CTLS always reports that these bits must be 1. Logical processors that support the 0-settings of any of these bits will support the VMX capability MSR IA32_VMX_TRUE_EXIT_CTLS MSR, and software should consult this MSR to discover support for the 0-settings of these bits. Software that is not aware of the functionality of any one of these bits should set that bit to 1.

#### 24.7.2 VM-Exit Controls for MSRs

A VMM may specify lists of MSRs to be stored and loaded on VM exits. The following VM-exit control fields determine how MSRs are stored on VM exits:

- **VM-exit MSR-store count** (32 bits). This field specifies the number of MSRs to be stored on VM exit. It is recommended that this count not exceed 512 bytes. Otherwise, unpredictable processor behavior (including a machine check) may result during VM exit.
- **VM-exit MSR-store address** (64 bits). This field contains the physical address of the VM-exit MSR-store area. The area is a table of entries, 16 bytes per entry, where the number of entries is given by the VM-exit MSR-

---

1. Future implementations may allow more MSRs to be stored reliably. Software should consult the VMX capability MSR IA32_VMX_MISC to determine the number supported (see Appendix A.6).
store count. The format of each entry is given in Table 24-11. If the VM-exit MSR-store count is not zero, the address must be 16-byte aligned.

### Table 24-11. Format of an MSR Entry

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>MSR index</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved</td>
</tr>
<tr>
<td>127:64</td>
<td>MSR data</td>
</tr>
</tbody>
</table>

See Section 27.4 for how this area is used on VM exits.

The following VM-exit control fields determine how MSRs are loaded on VM exits:

- **VM-exit MSR-load count** (32 bits). This field contains the number of MSRs to be loaded on VM exit. It is recommended that this count not exceed 512 bytes. Otherwise, unpredictable processor behavior (including a machine check) may result during VM exit.1

- **VM-exit MSR-load address** (64 bits). This field contains the physical address of the VM-exit MSR-load area. The area is a table of entries, 16 bytes per entry, where the number of entries is given by the VM-exit MSR-load count (see Table 24-11). If the VM-exit MSR-load count is not zero, the address must be 16-byte aligned.

See Section 27.6 for how this area is used on VM exits.

## 24.8 VM-ENTRY CONTROL FIELDS

The VM-entry control fields govern the behavior of VM entries. They are discussed in Sections 24.8.1 through 24.8.3.

### 24.8.1 VM-Entry Controls

The **VM-entry controls** constitute a 32-bit vector that governs the basic operation of VM entries. Table 24-12 lists the controls supported. See Chapter 24 for how these controls affect VM entries.

### Table 24-12. Definitions of VM-Entry Controls

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Load debug controls</td>
<td>This control determines whether DR7 and the IA32_DEBUGCTL MSR are loaded on VM entry. The first processors to support the virtual-machine extensions supported only the 1-setting of this control.</td>
</tr>
<tr>
<td>9</td>
<td>IA-32e mode guest</td>
<td>On processors that support Intel 64 architecture, this control determines whether the logical processor is in IA-32e mode after VM entry. Its value is loaded into IA32_EFER.LMA as part of VM entry. This control must be 0 on processors that do not support Intel 64 architecture.</td>
</tr>
<tr>
<td>10</td>
<td>Entry to SMM</td>
<td>This control determines whether the logical processor is in system-management mode (SMM) after VM entry. This control must be 0 for any VM entry from outside SMM.</td>
</tr>
<tr>
<td>11</td>
<td>Deactivate dual-monitor treatment</td>
<td>If set to 1, the default treatment of SMIs and SMM is in effect after the VM entry (see Section 34.15.7). This control must be 0 for any VM entry from outside SMM.</td>
</tr>
</tbody>
</table>

---

1. Future implementations may allow more MSRs to be loaded reliably. Software should consult the VMX capability MSR IA32_VMX_MISC to determine the number supported (see Appendix A.6).
All other bits in this field are reserved, some to 0 and some to 1. Software should consult the VMX capability MSRs IA32_VMX_ENTRY_CTLS and IA32_VMX_TRUE_ENTRY_CTLS (see Appendix A.5) to determine how it should set the reserved bits. Failure to set reserved bits properly causes subsequent VM entries to fail (see Section 26.2.1.3).

The first processors to support the virtual-machine extensions supported only the 1-settings of bits 0–8 and 12. The VMX capability MSR IA32_VMX_ENTRY_CTLS always reports that these bits must be 1. Logical processors that support the 0-settings of any of these bits will support the VMX capability MSR IA32_VMX_TRUE_ENTRY_CTLS MSR, and software should consult this MSR to discover support for the 0-settings of these bits. Software that is not aware of the functionality of any one of these bits should set that bit to 1.

### 24.8.2 VM-Entry Controls for MSRs

A VMM may specify a list of MSRs to be loaded on VM entries. The following VM-entry control fields manage this functionality:

- **VM-entry MSR-load count** (32 bits). This field contains the number of MSRs to be loaded on VM entry. It is recommended that this count not exceed 512 bytes. Otherwise, unpredictable processor behavior (including a machine check) may result during VM entry.¹

- **VM-entry MSR-load address** (64 bits). This field contains the physical address of the VM-entry MSR-load area. The area is a table of entries, 16 bytes per entry, where the number of entries is given by the VM-entry MSR-load count. The format of entries is described in Table 24-11. If the VM-entry MSR-load count is not zero, the address must be 16-byte aligned.

See Section 26.4 for details of how this area is used on VM entries.

### 24.8.3 VM-Entry Controls for Event Injection

VM entry can be configured to conclude by delivering an event through the IDT (after all guest state and MSRs have been loaded). This process is called **event injection** and is controlled by the following three VM-entry control fields:

- **VM-entry interruption-information field** (32 bits). This field provides details about the event to be injected. Table 24-13 describes the field.

#### Table 24-13. Format of the VM-Entry Interruption-Information Field

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Vector of interrupt or exception</td>
</tr>
</tbody>
</table>

¹ Future implementations may allow more MSRs to be loaded reliably. Software should consult the VMX capability MSR IA32_VMX_MISC to determine the number supported (see Appendix A.6).
— The vector (bits 7:0) determines which entry in the IDT is used or which other event is injected.

— The interruption type (bits 10:8) determines details of how the injection is performed. In general, a VMM should use the type hardware exception for all exceptions other than breakpoint exceptions (#BP; generated by INT3) and overflow exceptions (#OF; generated by INTO); it should use the type software exception for #BP and #OF. The type other event is used for injection of events that are not delivered through the IDT.

— For exceptions, the deliver-error-code bit (bit 11) determines whether delivery pushes an error code on the guest stack.

— VM entry injects an event if and only if the valid bit (bit 31) is 1. The valid bit in this field is cleared on every VM exit (see Section 27.2).

• VM-entry exception error code (32 bits). This field is used if and only if the valid bit (bit 31) and the deliver-error-code bit (bit 11) are both set in the VM-entry interruption-information field.

• VM-entry instruction length (32 bits). For injection of events whose type is software interrupt, software exception, or privileged software exception, this field is used to determine the value of RIP that is pushed on the stack.

See Section 26.5 for details regarding the mechanics of event injection, including the use of the interruption type and the VM-entry instruction length.

VM exits clear the valid bit (bit 31) in the VM-entry interruption-information field.

### 24.9 VM-EXIT INFORMATION FIELDS

The VMCS contains a section of fields that contain information about the most recent VM exit.

On some processors, attempts to write to these fields with VMWRITE fail (see “VMWRITE—Write Field to Virtual-Machine Control Structure” in Chapter 30).

### 24.9.1 Basic VM-Exit Information

The following VM-exit information fields provide basic information about a VM exit:

---

1. Software can discover whether these fields can be written by reading the VMX capability MSR IA32_VMX_MISC (see Appendix A.6).
• **Exit reason** (32 bits). This field encodes the reason for the VM exit and has the structure given in Table 24-14.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:0</td>
<td>Basic exit reason</td>
</tr>
<tr>
<td>27:16</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>28</td>
<td>Pending MTF VM exit</td>
</tr>
<tr>
<td>29</td>
<td>VM exit from VMX root operation</td>
</tr>
<tr>
<td>30</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>31</td>
<td>VM-entry failure (0 = true VM exit; 1 = VM-entry failure)</td>
</tr>
</tbody>
</table>

— Bits 15:0 provide basic information about the cause of the VM exit (if bit 31 is clear) or of the VM-entry failure (if bit 31 is set). Appendix C enumerates the basic exit reasons.

— Bit 28 is set only by an SMM VM exit (see Section 34.15.2) that took priority over an MTF VM exit (see Section 25.5.2) that would have occurred had the SMM VM exit not occurred. See Section 34.15.2.3.

— Bit 29 is set if and only if the processor was in VMX root operation at the time the VM exit occurred. This can happen only for SMM VM exits. See Section 34.15.2.

— Because some VM-entry failures load processor state from the host-state area (see Section 26.7), software must be able to distinguish such cases from true VM exits. Bit 31 is used for that purpose.

• **Exit qualification** (64 bits; 32 bits on processors that do not support Intel 64 architecture). This field contains additional information about the cause of VM exits due to the following: debug exceptions; page-fault exceptions; start-up IPIs (SIPIs); task switches; INVEPT; INVLPG; INVVPID; LGDT; LIDT; LLDT; LTR; SGDT; SIDT; SLDT; STR; VMCLARE; VMIPTRLD; VMIPTRST; VMREAD; VMWRITE; VMXON; control-register accesses; MOV DR; I/O instructions; and MWAIT. The format of the field depends on the cause of the VM exit. See Section 27.2.1 for details.

• **Guest-linear address** (64 bits; 32 bits on processors that do not support Intel 64 architecture). This field is used in the following cases:
  — VM exits due to attempts to execute LMSW with a memory operand.
  — VM exits due to attempts to execute INS or OUTS.
  — VM exits due to system-management interrupts (SMIs) that arrive immediately after retirement of I/O instructions.
  — Certain VM exits due to EPT violations

See Section 27.2.1 and Section 34.15.2.3 for details of when and how this field is used.

• **Guest-physical address** (64 bits). This field is used VM exits due to EPT violations and EPT misconfigurations. See Section 27.2.1 for details of when and how this field is used.

### 24.9.2 Information for VM Exits Due to Vectored Events

Event-specific information is provided for VM exits due to the following vectored events: exceptions (including those generated by the instructions INT3, INTO, BOUND, and UD2); external interrupts that occur while the “acknowledge interrupt on exit” VM-exit control is 1; and non-maskable interrupts (NMIs). This information is provided in the following fields:

• **VM-exit interruption information** (32 bits). This field receives basic information associated with the event causing the VM exit. Table 24-15 describes this field.
• **VM-exit interruption error code** (32 bits). For VM exits caused by hardware exceptions that would have delivered an error code on the stack, this field receives that error code.

Section 27.2.2 provides details of how these fields are saved on VM exits.

### 24.9.3 Information for VM Exits That Occur During Event Delivery

Additional information is provided for VM exits that occur during event delivery in VMX non-root operation. This information is provided in the following fields:

- **IDT-vectoring information** (32 bits). This field receives basic information associated with the event that was being delivered when the VM exit occurred. Table 24-16 describes this field.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Vector of interrupt or exception</td>
</tr>
<tr>
<td>10:8</td>
<td>Interruption type:</td>
</tr>
<tr>
<td></td>
<td>0: External interrupt</td>
</tr>
<tr>
<td></td>
<td>1: Not used</td>
</tr>
<tr>
<td></td>
<td>2: Non-maskable interrupt (NMI)</td>
</tr>
<tr>
<td></td>
<td>3: Hardware exception</td>
</tr>
<tr>
<td></td>
<td>4 - 5: Not used</td>
</tr>
<tr>
<td></td>
<td>6: Software exception</td>
</tr>
<tr>
<td></td>
<td>7: Not used</td>
</tr>
<tr>
<td>11</td>
<td>Error code valid (0 = invalid; 1 = valid)</td>
</tr>
<tr>
<td>12</td>
<td>NMI unblocking due to IRET</td>
</tr>
<tr>
<td>30:13</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>31</td>
<td>Valid</td>
</tr>
</tbody>
</table>

- **IDT-vectoring error code** (32 bits). For VM exits that occur during delivery of hardware exceptions that would have delivered an error code on the stack, this field receives that error code.

See Section 27.2.3 provides details of how these fields are saved on VM exits.

---

1. This includes cases in which the event delivery was caused by event injection as part of VM entry; see Section 26.5.1.2.
24.9.4 Information for VM Exits Due to Instruction Execution

The following fields are used for VM exits caused by attempts to execute certain instructions in VMX non-root operation:

- **VM-exit instruction length** (32 bits). For VM exits resulting from instruction execution, this field receives the length in bytes of the instruction whose execution led to the VM exit.\(^1\) See Section 27.2.4 for details of when and how this field is used.

- **VM-exit instruction information** (32 bits). This field is used for VM exits due to attempts to execute INS, INVEPT, INVVPID, LIDT, LGDT, LLDT, LTR, OUTS, SIDT, SGDT, SLDT, STR, VMCLEAR, VMPTRLD, VMPTRST, VMREAD, VMWRITE, or VMXON.\(^2\) The format of the field depends on the cause of the VM exit. See Section 27.2.4 for details.

The following fields (64 bits each; 32 bits on processors that do not support Intel 64 architecture) are used only for VM exits due to SMIs that arrive immediately after retirement of I/O instructions. They provide information about that I/O instruction:

- **I/O RCX**. The value of RCX before the I/O instruction started.
- **I/O RSI**. The value of RSI before the I/O instruction started.
- **I/O RDI**. The value of RDI before the I/O instruction started.
- **I/O RIP**. The value of RIP before the I/O instruction started (the RIP that addressed the I/O instruction).

24.9.5 VM-Instruction Error Field

The 32-bit **VM-instruction error field** does not provide information about the most recent VM exit. In fact, it is not modified on VM exits. Instead, it provides information about errors encountered by a non-faulting execution of one of the VMX instructions.

24.10 VMCS TYPES: ORDINARY AND SHADOW

Every VMCS is either an **ordinary VMCS** or a **shadow VMCS**. A VMCS’s type is determined by the shadow-VMCS indicator in the VMCS region (this is the value of bit 31 of the first 4 bytes of the VMCS region; see Table 24-1): 0 indicates an ordinary VMCS, while 1 indicates a shadow VMCS. Shadow VMCSs are supported only on processors that support the 1-setting of the “VMCS shadowing” VM-execution control (see Section 24.6.2).

A shadow VMCS differs from an ordinary VMCS in two ways:

- An ordinary VMCS can be used for VM entry but a shadow VMCS cannot. Attempts to perform VM entry when the current VMCS is a shadow VMCS fail (see Section 26.1).

- The VMREAD and VMWRITE instructions can be used in VMX non-root operation to access a shadow VMCS but not an ordinary VMCS. This fact results from the following:
  - If the “VMCS shadowing” VM-execution control is 0, execution of the VMREAD and VMWRITE instructions in VMX non-root operation always cause VM exits (see Section 25.1.3).
  - If the “VMCS shadowing” VM-execution control is 1, execution of the VMREAD and VMWRITE instructions in VMX non-root operation can access the VMCS referenced by the VMX capability MSR IA32_VMX_BASIC (see Section 30.3).
  - If the “VMCS shadowing” VM-execution control is 1, VM entry ensures that any VMCS referenced by the VMCS link pointer is a shadow VMCS (see Section 26.3.1.5).

In VMX root operation, both types of VMCSs can be accessed with the VMREAD and VMWRITE instructions.

Software should not modify the shadow-VMCS indicator in the VMCS region of a VMCS that is active. Doing so may cause the VMCS to become corrupted (see Section 24.11.1). Before modifying the shadow-VMCS indicator, software should execute VMCLEAR for the VMCS to ensure that it is not active.

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1. This field is also used for VM exits that occur during the delivery of a software interrupt or software exception.
2. Whether the processor provides this information on VM exits due to attempts to execute INS or OUTS can be determined by consulting the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).
24.11 SOFTWARE USE OF THE VMCS AND RELATED STRUCTURES

This section details guidelines that software should observe when using a VMCS and related structures. It also provides descriptions of consequences for failing to follow guidelines.

24.11.1 Software Use of Virtual-Machine Control Structures

To ensure proper processor behavior, software should observe certain guidelines when using an active VMCS. No VMCS should ever be active on more than one logical processor. If a VMCS is to be “migrated” from one logical processor to another, the first logical processor should execute VMCLEAR for the VMCS (to make it inactive on that logical processor and to ensure that all VMCS data are in memory) before the other logical processor executes VMPTRLD for the VMCS (to make it active on the second logical processor). A VMCS that is made active on more than one logical processor may become corrupted (see below).

Software should not modify the shadow-VMCS indicator (see Table 24-1) in the VMCS region of a VMCS that is active. Doing so may cause the VMCS to become corrupted. Before modifying the shadow-VMCS indicator, software should execute VMCLEAR for the VMCS to ensure that it is not active.

Software should use the VMREAD and VMWRITE instructions to access the different fields in the current VMCS (see Section 24.11.2). Software should never access or modify the VMCS data of an active VMCS using ordinary memory operations, in part because the format used to store the VMCS data is implementation-specific and not architecturally defined, and also because a logical processor may maintain some VMCS data of an active VMCS on the processor and not in the VMCS region. The following items detail some of the hazards of accessing VMCS data using ordinary memory operations:

- Any data read from a VMCS with an ordinary memory read does not reliably reflect the state of the VMCS. Results may vary from time to time or from logical processor to logical processor.
- Writing to a VMCS with an ordinary memory write is not guaranteed to have a deterministic effect on the VMCS. Doing so may cause the VMCS to become corrupted (see below).

(Software can avoid these hazards by removing any linear-address mappings to a VMCS region before executing a VMPTRLD for that region and by not remapping it until after executing VMCLEAR for that region.)

If a logical processor leaves VMX operation, any VMCSs active on that logical processor may be corrupted (see below). To prevent such corruption of a VMCS that may be used either after a return to VMX operation or on another logical processor, software should execute VMCLEAR for that VMCS before executing the VMXOFF instruction or removing power from the processor (e.g., as part of a transition to the S3 and S4 power states).

This section has identified operations that may cause a VMCS to become corrupted. These operations may cause the VMCS’s data to become undefined. Behavior may be unpredictable if that VMCS used subsequently on any logical processor. The following items detail some hazards of VMCS corruption:

- VM entries may fail for unexplained reasons or may load undesired processor state.
- The processor may not correctly support VMX non-root operation as documented in Chapter 27 and may generate unexpected VM exits.
- VM exits may load undesired processor state, save incorrect state into the VMCS, or cause the logical processor to transition to a shutdown state.

24.11.2 VMREAD, VMWRITE, and Encodings of VMCS Fields

Every field of the VMCS is associated with a 32-bit value that is its encoding. The encoding is provided in an operand to VMREAD and VMWRITE when software wishes to read or write that field. These instructions fail if given, in 64-bit mode, an operand that sets an encoding bit beyond bit 32. See Chapter 30 for a description of these instructions.

---

1. As noted in Section 24.1, execution of the VMPTRLD instruction makes a VMCS is active. In addition, VM entry makes active any shadow VMCS referenced by the VMCS link pointer in the current VMCS. If a shadow VMCS is made active by VM entry, it is necessary to execute VMCLEAR for that VMCS before allowing that VMCS to become active on another logical processor.
The structure of the 32-bit encodings of the VMCS components is determined principally by the width of the fields and their function in the VMCS. See Table 24-17.

**Table 24-17. Structure of VMCS Component Encoding**

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Access type (0 = full; 1 = high); must be full for 16-bit, 32-bit, and natural-width fields</td>
</tr>
<tr>
<td>9:1</td>
<td>Index</td>
</tr>
<tr>
<td>11:10</td>
<td>Type:</td>
</tr>
<tr>
<td></td>
<td>0: control</td>
</tr>
<tr>
<td></td>
<td>1: VM-exit information</td>
</tr>
<tr>
<td></td>
<td>2: guest state</td>
</tr>
<tr>
<td></td>
<td>3: host state</td>
</tr>
<tr>
<td>12</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>14:13</td>
<td>Width:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 64-bit</td>
</tr>
<tr>
<td></td>
<td>2: 32-bit</td>
</tr>
<tr>
<td></td>
<td>3: natural-width</td>
</tr>
<tr>
<td>31:15</td>
<td>Reserved (must be 0)</td>
</tr>
</tbody>
</table>

The following items detail the meaning of the bits in each encoding:

- **Field width.** Bits 14:13 encode the width of the field.
  - A value of 0 indicates a 16-bit field.
  - A value of 1 indicates a 64-bit field.
  - A value of 2 indicates a 32-bit field.
  - A value of 3 indicates a natural-width field. Such fields have 64 bits on processors that support Intel 64 architecture and 32 bits on processors that do not.

Fields whose encodings use value 1 are specially treated to allow 32-bit software access to all 64 bits of the field. Such access is allowed by defining, for each such field, an encoding that allows direct access to the high 32 bits of the field. See below.

- **Field type.** Bits 11:10 encode the type of VMCS field: control, guest-state, host-state, or VM-exit information. (The last category also includes the VM-instruction error field.)

- **Index.** Bits 9:1 distinguish components with the same field width and type.

- **Access type.** Bit 0 must be 0 for all fields except for 64-bit fields (those with field-width 1; see above). A VMREAD or VMWRITE using an encoding with this bit cleared to 0 accesses the entire field. For a 64-bit field with field-width 1, a VMREAD or VMWRITE using an encoding with this bit set to 1 accesses only the high 32 bits of the field.

Appendix B gives the encodings of all fields in the VMCS.

The following describes the operation of VMREAD and VMWRITE based on processor mode, VMCS-field width, and access type:

- **16-bit fields:**
  - A VMREAD returns the value of the field in bits 15:0 of the destination operand; other bits of the destination operand are cleared to 0.
  - A VMWRITE writes the value of bits 15:0 of the source operand into the VMCS field; other bits of the source operand are not used.

- **32-bit fields:**
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— A VMREAD returns the value of the field in bits 31:0 of the destination operand; in 64-bit mode, bits 63:32 of the destination operand are cleared to 0.

— A VMWRITE writes the value of bits 31:0 of the source operand into the VMCS field; in 64-bit mode, bits 63:32 of the source operand are not used.

• 64-bit fields and natural-width fields using the full access type outside IA-32e mode.
  — A VMREAD returns the value of bits 31:0 of the field in its destination operand; bits 63:32 of the field are ignored.
  — A VMWRITE writes the value of its source operand to bits 31:0 of the field and clears bits 63:32 of the field.

• 64-bit fields and natural-width fields using the full access type in 64-bit mode (only on processors that support Intel 64 architecture).
  — A VMREAD returns the value of the field in bits 63:0 of the destination operand
  — A VMWRITE writes the value of bits 63:0 of the source operand into the VMCS field.

• 64-bit fields using the high access type.
  — A VMREAD returns the value of bits 63:32 of the field in bits 31:0 of the destination operand; in 64-bit mode, bits 63:32 of the destination operand are cleared to 0.
  — A VMWRITE writes the value of bits 31:0 of the source operand to bits 63:32 of the field; in 64-bit mode, bits 63:32 of the source operand are not used.

Software seeking to read a 64-bit field outside IA-32e mode can use VMREAD with the full access type (reading bits 31:0 of the field) and VMREAD with the high access type (reading bits 63:32 of the field); the order of the two VMREAD executions is not important. Software seeking to modify a 64-bit field outside IA-32e mode should first use VMWRITE with the full access type (establishing bits 31:0 of the field while clearing bits 63:32) and then use VMWRITE with the high access type (establishing bits 63:32 of the field).

24.11.3 Initializing a VMCS

Software should initialize fields in a VMCS (using VMWRITE) before using the VMCS for VM entry. Failure to do so may result in unpredictable behavior; for example, a VM entry may fail for unexplained reasons, or a successful transition (VM entry or VM exit) may load processor state with unexpected values.

It is not necessary to initialize fields that the logical processor will not use. (For example, it is not necessary to unitize the MSR-bitmap address if the “use MSR bitmaps” VM-execution control is 0.)

A processor maintains some VMCS information that cannot be modified with the VMWRITE instruction; this includes a VMCS’s launch state (see Section 24.1). Such information may be stored in the VMCS data portion of a VMCS region. Because the format of this information is implementation-specific, there is no way for software to know, when it first allocates a region of memory for use as a VMCS region, how the processor will determine this information from the contents of the memory region.

In addition to its other functions, the VMCLEAR instruction initializes any implementation-specific information in the VMCS region referenced by its operand. To avoid the uncertainties of implementation-specific behavior, software should execute VMCLEAR on a VMCS region before making the corresponding VMCS active with VMPTRLD for the first time. (Figure 24-1 illustrates how execution of VMCLEAR puts a VMCS into a well-defined state.)

The following software usage is consistent with these limitations:
• VMCLEAR should be executed for a VMCS before it is used for VM entry for the first time.
• VMLAUNCH should be used for the first VM entry using a VMCS after VMCLEAR has been executed for that VMCS.
• VMRESUME should be used for any subsequent VM entry using a VMCS (until the next execution of VMCLEAR for the VMCS).

It is expected that, in general, VMRESUME will have lower latency than VMLAUNCH. Since "migrating" a VMCS from one logical processor to another requires use of VMCLEAR (see Section 24.11.1), which sets the launch state of the VMCS to "clear", such migration requires the next VM entry to be performed using VMLAUNCH. Software developers can avoid the performance cost of increased VM-entry latency by avoiding unnecessary migration of a VMCS from one logical processor to another.

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24.11.4 Software Access to Related Structures

In addition to data in the VMCS region itself, VMX non-root operation can be controlled by data structures that are referenced by pointers in a VMCS (for example, the I/O bitmaps). While the pointers to these data structures are parts of the VMCS, the data structures themselves are not. They are not accessible using VMREAD and VMWRITE but by ordinary memory writes.

Software should ensure that each such data structure is modified only when no logical processor with a current VMCS that references it is in VMX non-root operation. Doing otherwise may lead to unpredictable behavior (including behaviors identified in Section 24.11.1).

24.11.5 VMXON Region

Before executing VMXON, software allocates a region of memory (called the VMXON region)\(^1\) that the logical processor uses to support VMX operation. The physical address of this region (the VMXON pointer) is provided in an operand to VMXON. The VMXON pointer is subject to the limitations that apply to VMCS pointers:

- The VMXON pointer must be 4-KByte aligned (bits 11:0 must be zero).
- The VMXON pointer must not set any bits beyond the processor’s physical-address width.\(^2,3\)

Before executing VMXON, software should write the VMCS revision identifier (see Section 24.2) to the VMXON region. (Specifically, it should write the 31-bit VMCS revision identifier to bits 30:0 of the first 4 bytes of the VMXON region; bit 31 should be cleared to 0.) It need not initialize the VMXON region in any other way. Software should use a separate region for each logical processor and should not access or modify the VMXON region of a logical processor between execution of VMXON and VMXOFF on that logical processor. Doing otherwise may lead to unpredictable behavior (including behaviors identified in Section 24.11.1).

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1. The amount of memory required for the VMXON region is the same as that required for a VMCS region. This size is implementation specific and can be determined by consulting the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).

2. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.

3. If IA32_VMX_BASIC[48] is read as 1, the VMXON pointer must not set any bits in the range 63:32; see Appendix A.1.
CHAPTER 25
VMX NON-ROOT OPERATION

In a virtualized environment using VMX, the guest software stack typically runs on a logical processor in VMX non-root operation. This mode of operation is similar to that of ordinary processor operation outside of the virtualized environment. This chapter describes the differences between VMX non-root operation and ordinary processor operation with special attention to causes of VM exits (which bring a logical processor from VMX non-root operation to root operation). The differences between VMX non-root operation and ordinary processor operation are described in the following sections:

- Section 25.1, “Instructions That Cause VM Exits”
- Section 25.2, “Other Causes of VM Exits”
- Section 25.3, “Changes to Instruction Behavior in VMX Non-Root Operation”
- Section 25.4, “Other Changes in VMX Non-Root Operation”
- Section 25.5, “Features Specific to VMX Non-Root Operation”
- Section 25.6, “Unrestricted Guests”

Chapter 26, “VM Entries,” describes the data control structures that govern VMX non-root operation. Chapter 26, “VM Entries,” describes the operation of VM entries by which the processor transitions from VMX root operation to VMX non-root operation. Chapter 25, “VMX Non-Root Operation,” describes the operation of VM exits by which the processor transitions from VMX non-root operation to VMX root operation.

Chapter 28, “VMX Support for Address Translation,” describes two features that support address translation in VMX non-root operation. Chapter 29, “APIC Virtualization and Virtual Interrupts,” describes features that support virtualization of interrupts and the Advanced Programmable Interrupt Controller (APIC) in VMX non-root operation.

25.1 INSTRUCTIONS THAT CAUSE VM EXITS

Certain instructions may cause VM exits if executed in VMX non-root operation. Unless otherwise specified, such VM exits are “fault-like,” meaning that the instruction causing the VM exit does not execute and no processor state is updated by the instruction. Section 27.1 details architectural state in the context of a VM exit.

Section 25.1.1 defines the prioritization between faults and VM exits for instructions subject to both. Section 25.1.2 identifies instructions that cause VM exits whenever they are executed in VMX non-root operation (and thus can never be executed in VMX non-root operation). Section 25.1.3 identifies instructions that cause VM exits depending on the settings of certain VM-execution control fields (see Section 24.6).

25.1.1 Relative Priority of Faults and VM Exits

The following principles describe the ordering between existing faults and VM exits:

- Certain exceptions have priority over VM exits. These include invalid-opcode exceptions, faults based on privilege level, and general-protection exceptions that are based on checking I/O permission bits in the task-state segment (TSS). For example, execution of RDMSR with CPL = 3 generates a general-protection exception and not a VM exit.

- Faults incurred while fetching instruction operands have priority over VM exits that are conditioned based on the contents of those operands (see LMSW in Section 25.1.3).

- VM exits caused by execution of the INS and OUTS instructions (resulting either because the “unconditional I/O exiting” VM-execution control is 1 or because the “use I/O bitmap control is 1”) have priority over the following faults:

1. These include faults generated by attempts to execute, in virtual-8086 mode, privileged instructions that are not recognized in that mode.
2. MOV DR is an exception to this rule; see Section 25.1.3.
VMX NON-ROOT OPERATION

- A general-protection fault due to the relevant segment (ES for INS; DS for OUTS unless overridden by an instruction prefix) being unusable
- A general-protection fault due to an offset beyond the limit of the relevant segment
- An alignment-check exception

Fault-like VM exits have priority over exceptions other than those mentioned above. For example, RDMSR of a non-existent MSR with CPL = 0 generates a VM exit and not a general-protection exception.

When Section 25.1.2 or Section 25.1.3 (below) identify an instruction execution that may lead to a VM exit, it is assumed that the instruction does not incur a fault that takes priority over a VM exit.

25.1.2 Instructions That Cause VM Exits Unconditionally

The following instructions cause VM exits when they are executed in VMX non-root operation: CPUID, GETSEC, INVD, and XSETBV. This is also true of instructions introduced with VMX, which include: INVEPT, INVVPID, VMCALL, VMCLEAR, VMLAUNCH, VMPTRLD, VMPTRST, VMRESUME, VMXOFF, and VMXON.

25.1.3 Instructions That Cause VM Exits Conditionally

Certain instructions cause VM exits in VMX non-root operation depending on the setting of the VM-execution controls. The following instructions can cause "fault-like" VM exits based on the conditions described:

- **CLTS.** The CLTS instruction causes a VM exit if the bits in position 3 (corresponding to CR0.TS) are set in both the CR0 guest/host mask and the CR0 read shadow.
- **HLT.** The HLT instruction causes a VM exit if the "HLT exiting" VM-execution control is 1.
- **IN, INS/INSB/INSW/INSD, OUT, OUTS/OUTSB/OUTSW/OUTSD.** The behavior of each of these instructions is determined by the settings of the "unconditional I/O exiting" and "use I/O bitmaps" VM-execution controls:
  - If both controls are 0, the instruction executes normally.
  - If the "unconditional I/O exiting" VM-execution control is 1 and the "use I/O bitmaps" VM-execution control is 0, the instruction causes a VM exit.
  - If the "use I/O bitmaps" VM-execution control is 1, the instruction causes a VM exit if it attempts to access an I/O port corresponding to a bit set to 1 in the appropriate I/O bitmap (see Section 24.6.4). If an I/O operation "wraps around" the 16-bit I/O-port space (accesses ports FFFFH and 0000H), the I/O instruction causes a VM exit (the "unconditional I/O exiting" VM-execution control is ignored if the "use I/O bitmaps" VM-execution control is 1).

See Section 25.1.1 for information regarding the priority of VM exits relative to faults that may be caused by the INS and OUTS instructions.

- **INVLPG.** The INVLPG instruction causes a VM exit if the "INVLPG exiting" VM-execution control is 1.
- **INVPCID.** The INVPCID instruction causes a VM exit if the "INVLPG exiting" and "enable INVPCID” VM-execution controls are both 1.
- **LGDTR, LDTR, LLDT, LTR, SGDT, SIDT, SLDT, STR.** These instructions cause VM exits if the "descriptor-table exiting” VM-execution control is 1.
- **LMSW.** In general, the LMSW instruction causes a VM exit if it would write, for any bit set in the low 4 bits of the CR0 guest/host mask, a value different than the corresponding bit in the CR0 read shadow. LMSW never clears bit 0 of CR0 (CR0.PE); thus, LMSW causes a VM exit if either of the following are true:

1. An execution of GETSEC in VMX non-root operation causes a VM exit if CR4.SMXE[Bit 14] = 1 regardless of the value of CPL or RAX. An execution of GETSEC causes an invalid-opcode exception (#UD) if CR4.SMXE[Bit 14] = 0.
2. Under the dual-monitor treatment of SMIs and SMM, executions of VMCALL cause SMM VM exits in VMX root operation outside SMM. See Section 34.15.2.
3. Many of the items in this section refer to secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if these controls were all 0. See Section 24.6.2.
— The bits in position 0 (corresponding to CR0.PE) are set in both the CR0 guest/mask and the source operand, and the bit in position 0 is clear in the CR0 read shadow.

— For any bit position in the range 3:1, the bit in that position is set in the CR0 guest/mask and the values of the corresponding bits in the source operand and the CR0 read shadow differ.

• **MONITOR.** The MONITOR instruction causes a VM exit if the “MONITOR exiting” VM-execution control is 1.

• **MOV from CR3.** The MOV from CR3 instruction causes a VM exit if the “CR3-store exiting” VM-execution control is 1. The first processors to support the virtual-machine extensions supported only the 1-setting of this control.

• **MOV from CR8.** The MOV from CR8 instruction causes a VM exit if the “CR8-store exiting” VM-execution control is 1.

• **MOV to CR0.** The MOV to CR0 instruction causes a VM exit unless the value of its source operand matches, for the position of each bit set in the CR0 guest/host mask, the corresponding bit in the CR0 read shadow. (If every bit is clear in the CR0 guest/host mask, MOV to CR0 cannot cause a VM exit.)

• **MOV to CR3.** The MOV to CR3 instruction causes a VM exit unless the “CR3-load exiting” VM-execution control is 0 or the value of its source operand is equal to one of the CR3-target values specified in the VMCS. If the CR3-target count in n, only the first n CR3-target values are considered; if the CR3-target count is 0, MOV to CR3 always causes a VM exit.

The first processors to support the virtual-machine extensions supported only the 1-setting of the “CR3-load exiting” VM-execution control. These processors always consult the CR3-target controls to determine whether an execution of MOV to CR3 causes a VM exit.

• **MOV to CR4.** The MOV to CR4 instruction causes a VM exit unless the value of its source operand matches, for the position of each bit set in the CR4 guest/host mask, the corresponding bit in the CR4 read shadow.

• **MOV to CR8.** The MOV to CR8 instruction causes a VM exit if the “CR8-load exiting” VM-execution control is 1.

• **MOV DR.** The MOV DR instruction causes a VM exit if the “MOV-DR exiting” VM-execution control is 1. Such VM exits represent an exception to the principles identified in Section 25.1.1 in that they take priority over the following: general-protection exceptions based on privilege level; and invalid-opcode exceptions that occur because CR4.DE=1 and the instruction specified access to DR4 or DR5.

• **MWAIT.** The MWAIT instruction causes a VM exit if the “MWAIT exiting” VM-execution control is 1. If this control is 0, the behavior of the MWAIT instruction may be modified (see Section 25.3).

• **PAUSE.** The behavior of each of this instruction depends on CPL and the settings of the “PAUSE exiting” and “PAUSE-loop exiting” VM-execution controls:
  — CPL = 0.
    • If the “PAUSE exiting” and “PAUSE-loop exiting” VM-execution controls are both 0, the PAUSE instruction executes normally.
    • If the “PAUSE exiting” VM-execution control is 1, the PAUSE instruction causes a VM exit (the “PAUSE-loop exiting” VM-execution control is ignored if CPL = 0 and the “PAUSE exiting” VM-execution control is 1).
    • If the “PAUSE exiting” VM-execution control is 0 and the “PAUSE-loop exiting” VM-execution control is 1, the following treatment applies.
      The processor determines the amount of time between this execution of PAUSE and the previous execution of PAUSE at CPL 0. If this amount of time exceeds the value of the VM-execution control field PLE_Gap, the processor considers this execution to be the first execution of PAUSE in a loop. (It also does so for the first execution of PAUSE at CPL 0 after VM entry.)
      Otherwise, the processor determines the amount of time since the most recent execution of PAUSE that was considered to be the first in a loop. If this amount of time exceeds the value of the VM-execution control field PLE_Window, a VM exit occurs.
      For purposes of these computations, time is measured based on a counter that runs at the same rate as the timestamp counter (TSC).
  — CPL > 0.
    • If the “PAUSE exiting” VM-execution control is 0, the PAUSE instruction executes normally.
• If the “PAUSE exiting” VM-execution control is 1, the PAUSE instruction causes a VM exit. The “PAUSE-loop exiting” VM-execution control is ignored if CPL > 0.

• **RDMSR.** The RDMSR instruction causes a VM exit if any of the following are true:
  — The “use MSR bitmaps” VM-execution control is 0.
  — The value of ECX is not in the ranges 00000000H – 00001FFFH and C0000000H – C0001FFFH.
  — The value of ECX is in the range 00000000H – 00001FFFH and bit \( n \) in read bitmap for low MSRs is 1, where \( n \) is the value of ECX.
  — The value of ECX is in the range C0000000H – C0001FFFH and bit \( n \) in read bitmap for high MSRs is 1, where \( n \) is the value of ECX & 00001FFFH.

See Section 24.6.9 for details regarding how these bitmaps are identified.

• **RDPMC.** The RDPMC instruction causes a VM exit if the “RDPMC exiting” VM-execution control is 1.

• **RDRAND.** The RDRAND instruction causes a VM exit if the “RDRAND exiting” VM-execution control is 1.

• **RDSEED.** The RDSEED instruction causes a VM exit if the “RDSEED exiting” VM-execution control is 1.

• **RDTSC.** The RDTSC instruction causes a VM exit if the “RDTSC exiting” VM-execution control is 1.

• **RDTSCP.** The RDTSCP instruction causes a VM exit if the “RDTSC exiting” and “enable RDTSCP” VM-execution controls are both 1.

• **RSM.** The RSM instruction causes a VM exit if executed in system-management mode (SMM).\(^1\)

• **VMREAD.** The VMREAD instruction causes a VM exit if any of the following are true:
  — The “VMCS shadowing” VM-execution control is 0.
  — Bits 63:15 (bits 31:15 outside 64-bit mode) of the register source operand are not all 0.
  — Bit \( n \) in VMREAD bitmap is 1, where \( n \) is the value of bits 14:0 of the register source operand. See Section 24.6.16 for details regarding how the VMREAD bitmap is identified.

If the VMREAD instruction does not cause a VM exit, it reads from the VMCS referenced by the VMCS link pointer. See Chapter 30, “VMREAD—Read Field from Virtual-Machine Control Structure” for details of the operation of the VMREAD instruction.

• **VMWRITE.** The VMWRITE instruction causes a VM exit if any of the following are true:
  — The “VMCS shadowing” VM-execution control is 0.
  — Bits 63:15 (bits 31:15 outside 64-bit mode) of the register source operand are not all 0.
  — Bit \( n \) in VMWRITE bitmap is 1, where \( n \) is the value of bits 14:0 of the register source operand. See Section 24.6.16 for details regarding how the VMWRITE bitmap is identified.

If the VMWRITE instruction does not cause a VM exit, it writes to the VMCS referenced by the VMCS link pointer. See Chapter 30, “VMWRITE—Write Field to Virtual-Machine Control Structure” for details of the operation of the VMWRITE instruction.

• **WBINVD.** The WBINVD instruction causes a VM exit if the “WBINVD exiting” VM-execution control is 1.

• **WRMSR.** The WRMSR instruction causes a VM exit if any of the following are true:
  — The “use MSR bitmaps” VM-execution control is 0.
  — The value of ECX is not in the ranges 00000000H – 00001FFFH and C0000000H – C0001FFFH.
  — The value of ECX is in the range 00000000H – 00001FFFH and bit \( n \) in write bitmap for low MSRs is 1, where \( n \) is the value of ECX.
  — The value of ECX is in the range C0000000H – C0001FFFH and bit \( n \) in write bitmap for high MSRs is 1, where \( n \) is the value of ECX & 00001FFFH.

See Section 24.6.9 for details regarding how these bitmaps are identified.

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1. Execution of the RSM instruction outside SMM causes an invalid-opcode exception regardless of whether the processor is in VMX operation. It also does so in VMX root operation in SMM; see Section 34.15.3.
• **XRSTORS.** The XRSTORS instruction causes a VM exit if the "enable XSAVE/XRSTORS" VM-execution control is 1 and any bit is set in the logical-AND of the following three values: EDX:EAX, the IA32_XSS MSR, and the XSS-exiting bitmap (see Section 24.6.18).

• **XSAVES.** The XSAVES instruction causes a VM exit if the "enable XSAVE/XRSTORS" VM-execution control is 1 and any bit is set in the logical-AND of the following three values: EDX:EAX, the IA32_XSS MSR, and the XSS-exiting bitmap (see Section 24.6.18).

25.2 OTHER CAUSES OF VM EXITS

In addition to VM exits caused by instruction execution, the following events can cause VM exits:

• **Exceptions.** Exceptions (faults, traps, and aborts) cause VM exits based on the exception bitmap (see Section 24.6.3). If an exception occurs, its vector (in the range 0–31) is used to select a bit in the exception bitmap. If the bit is 1, a VM exit occurs; if the bit is 0, the exception is delivered normally through the guest IDT. This use of the exception bitmap applies also to exceptions generated by the instructions INT3, INTO, BOUND, and UD2.

Page faults (exceptions with vector 14) are specially treated. When a page fault occurs, a processor consults (1) bit 14 of the exception bitmap; (2) the error code produced with the page fault [PFEC]; (3) the page-fault error-code mask field [PFEC_MASK]; and (4) the page-fault error-code match field [PFEC_MATCH]. It checks if PFEC & PFEC_MASK = PFEC_MATCH. If there is equality, the specification of bit 14 in the exception bitmap is followed (for example, a VM exit occurs if that bit is set). If there is inequality, the meaning of that bit is reversed (for example, a VM exit occurs if that bit is clear).

Thus, if software desires VM exits on all page faults, it can set bit 14 in the exception bitmap to 1 and set the page-fault error-code mask and match fields each to 00000000H. If software desires VM exits on no page faults, it can set bit 14 in the exception bitmap to 1, the page-fault error-code mask field to 00000000H, and the page-fault error-code match field to FFFFFFFFH.

• **Triple fault.** A VM exit occurs if the logical processor encounters an exception while attempting to call the double-fault handler and that exception itself does not cause a VM exit due to the exception bitmap. This applies to the case in which the double-fault exception was generated within VMX non-root operation, the case in which the double-fault exception was generated during event injection by VM entry, and to the case in which VM entry is injecting a double-fault exception.

• **External interrupts.** An external interrupt causes a VM exit if the "external-interrupt exiting” VM-execution control is 1. (See Section 25.6 for an exception.) Otherwise, the interrupt is delivered normally through the IDT. (If a logical processor is in the shutdown state or the wait-for-SIPI state, external interrupts are blocked. The interrupt is not delivered through the IDT and no VM exit occurs.)

• **Non-maskable interrupts (NMIs).** An NMI causes a VM exit if the "NMI exiting” VM-execution control is 1. Otherwise, it is delivered using descriptor 2 of the IDT. (If a logical processor is in the wait-for-SIPI state, NMIs are blocked. The NMI is not delivered through the IDT and no VM exit occurs.)

• **INIT signals.** INIT signals cause VM exits. A logical processor performs none of the operations normally associated with these events. Such exits do not modify register state or clear pending events as they would outside of VMX operation. (If a logical processor is in the wait-for-SIPI state, INIT signals are blocked. They do not cause VM exits in this case.)

• **Start-up IPIs (SIPIs).** SIPIs cause VM exits. If a logical processor is not in the wait-for-SIPI activity state when a SIPI arrives, no VM exit occurs and the SIPI is discarded. VM exits due to SIPIs do not perform any of the normal operations associated with those events: they do not modify register state as they would outside of VMX operation. (If a logical processor is not in the wait-for-SIPI state, SIPIs are blocked. They do not cause VM exits in this case.)

• **Task switches.** Task switches are not allowed in VMX non-root operation. Any attempt to effect a task switch in VMX non-root operation causes a VM exit. See Section 25.4.2.

• **System-management interrupts (SMIs).** If the logical processor is using the dual-monitor treatment of SMIs and system-management mode (SMM), SMIs cause SMM VM exits. See Section 34.15.2.1

1. Under the dual-monitor treatment of SMIs and SMM, SMIs also cause SMM VM exits if they occur in VMX root operation outside SMM. If the processor is using the default treatment of SMIs and SMM, SMIs are delivered as described in Section 34.14.1.
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- **VMX-preemption timer.** A VM exit occurs when the timer counts down to zero. See Section 25.5.1 for details of operation of the VMX-preemption timer.

  Debug-trap exceptions and higher priority events take priority over VM exits caused by the VMX-preemption timer. VM exits caused by the VMX-preemption timer take priority over VM exits caused by the “NMI-window exiting” VM-execution control and lower priority events.

  These VM exits wake a logical processor from the same inactive states as would a non-maskable interrupt. Specifically, they wake a logical processor from the shutdown state and from the states entered using the HLT and MWAIT instructions. These VM exits do not occur if the logical processor is in the wait-for-SIPI state.

  In addition, there are controls that cause VM exits based on the readiness of guest software to receive interrupts:

  - If the “interrupt-window exiting” VM-execution control is 1, a VM exit occurs before execution of any instruction if RFLAGS.IF = 1 and there is no blocking of events by STI or by MOV SS (see Table 24-3). Such a VM exit occurs immediately after VM entry if the above conditions are true (see Section 26.6.5).

    Non-maskable interrupts (NMIs) and higher priority events take priority over VM exits caused by this control. VM exits caused by this control take priority over external interrupts and lower priority events.

    These VM exits wake a logical processor from the same inactive states as would an external interrupt. Specifically, they wake a logical processor from the states entered using the HLT and MWAIT instructions. These VM exits do not occur if the logical processor is in the shutdown state or the wait-for-SIPI state.

  - If the “NMI-window exiting” VM-execution control is 1, a VM exit occurs before execution of any instruction if there is no virtual-NMI blocking and there is no blocking of events by MOV SS (see Table 24-3). (A logical processor may also prevent such a VM exit if there is blocking of events by STI.) Such a VM exit occurs immediately after VM entry if the above conditions are true (see Section 26.6.6).

    VM exits caused by the VMX-preemption timer and higher priority events take priority over VM exits caused by this control. VM exits caused by this control take priority over non-maskable interrupts (NMIs) and lower priority events.

    These VM exits wake a logical processor from the same inactive states as would an NMI. Specifically, they wake a logical processor from the shutdown state and from the states entered using the HLT and MWAIT instructions. These VM exits do not occur if the logical processor is in the wait-for-SIPI state.

### 25.3 CHANGES TO INSTRUCTION BEHAVIOR IN VMX NON-ROOT OPERATION

The behavior of some instructions is changed in VMX non-root operation. Some of these changes are determined by the settings of certain VM-execution control fields. The following items detail such changes:

- **CLTS.** Behavior of the CLTS instruction is determined by the bits in position 3 (corresponding to CR0.TS) in the CR0 guest/host mask and the CR0 read shadow:

  - If bit 3 in the CR0 guest/host mask is 0, CLTS clears CR0.TS normally (the value of bit 3 in the CR0 read shadow is irrelevant in this case), unless CR0.TS is fixed to 1 in VMX operation (see Section 23.8), in which case CLTS causes a general-protection exception.

  - If bit 3 in the CR0 guest/host mask is 1 and bit 3 in the CR0 read shadow is 0, CLTS completes but does not change the contents of CR0.TS.

  - If the bits in position 3 in the CR0 guest/host mask and the CR0 read shadow are both 1, CLTS causes a VM exit.

- **INVPCID.** Behavior of the INVPCID instruction is determined first by the setting of the “enable INVPCID” VM-execution control:

  - If the “enable INVPCID” VM-execution control is 0, INVPCID causes an invalid-opcode exception (#UD). This exception takes priority over any other exception the instruction may incur.

  - If the “enable INVPCID” VM-execution control is 1, treatment is based on the setting of the “INVLPG exiting” VM-execution control:

1. Some of the items in this section refer to secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if these controls were all 0. See Section 24.6.2.
• If the "INVLPG exiting" VM-execution control is 0, INVPCID operates normally.
• If the "INVLPG exiting" VM-execution control is 1, INVPCID causes a VM exit.

• **IRET.** Behavior of IRET with regard to NMI blocking (see Table 24-3) is determined by the settings of the "NMI exiting" and "virtual NMIs" VM-execution controls:
  — If the "NMI exiting" VM-execution control is 0, IRET operates normally and unblocks NMIs. (If the "NMI exiting" VM-execution control is 0, the "virtual NMIs" control must be 0; see Section 26.2.1.1.)
  — If the "NMI exiting" VM-execution control is 1, IRET does not affect blocking of NMIs. If, in addition, the "virtual NMIs" VM-execution control is 1, the logical processor tracks virtual-NMI blocking. In this case, IRET removes any virtual-NMI blocking.

The unblocking of NMIs or virtual NMIs specified above occurs even if IRET causes a fault.

• **LMSW.** Outside of VMX non-root operation, LMSW loads its source operand into CR0[3:0], but it does not clear CR0.PE if that bit is set. In VMX non-root operation, an execution of LMSW that does not cause a VM exit (see Section 25.1.3) leaves unmodified any bit in CR0[3:0] corresponding to a bit set in the CR0 guest/host mask. An attempt to set any other bit in CR0[3:0] to a value not supported in VMX operation (see Section 23.8) causes a general-protection exception. Attempts to clear CR0.PE are ignored without fault.

• **MOV from CR0.** The behavior of MOV from CR0 is determined by the CR0 guest/host mask and the CR0 read shadow. For each position corresponding to a bit clear in the CR0 guest/host mask, the destination operand is loaded with the value of the corresponding bit in CR0. For each position corresponding to a bit set in the CR0 guest/host mask, the destination operand is loaded with the value of the corresponding bit in the CR0 read shadow. Thus, if every bit is cleared in the CR0 guest/host mask, MOV from CR0 reads normally from CR0; if every bit is set in the CR0 guest/host mask, MOV from CR0 returns the value of the CR0 read shadow.

Depending on the contents of the CR0 guest/host mask and the CR0 read shadow, bits may be set in the destination that would never be set when reading directly from CR0.

• **MOV from CR3.** If the "enable EPT" VM-execution control is 1 and an execution of MOV from CR3 does not cause a VM exit (see Section 25.1.3), the value loaded from CR3 is a guest-physical address; see Section 28.2.1.

• **MOV from CR4.** The behavior of MOV from CR4 is determined by the CR4 guest/host mask and the CR4 read shadow. For each position corresponding to a bit clear in the CR4 guest/host mask, the destination operand is loaded with the value of the corresponding bit in CR4. For each position corresponding to a bit set in the CR4 guest/host mask, the destination operand is loaded with the value of the corresponding bit in the CR4 read shadow. Thus, if every bit is cleared in the CR4 guest/host mask, MOV from CR4 reads normally from CR4; if every bit is set in the CR4 guest/host mask, MOV from CR4 returns the value of the CR4 read shadow.

Depending on the contents of the CR4 guest/host mask and the CR4 read shadow, bits may be set in the destination that would never be set when reading directly from CR4.

• **MOV from CR8.** If the MOV from CR8 instruction does not cause a VM exit (see Section 25.1.3), its behavior is modified if the "use TPR shadow" VM-execution control is 1; see Section 29.3.

• **MOV to CR0.** An execution of MOV to CR0 that does not cause a VM exit (see Section 25.1.3) leaves unmodified any bit in CR0 corresponding to a bit set in the CR0 guest/host mask. Treatment of attempts to modify other bits in CR0 depends on the setting of the "unrestricted guest" VM-execution control:
  — If the control is 0, MOV to CR0 causes a general-protection exception if it attempts to set any bit in CR0 to a value not supported in VMX operation (see Section 23.8).
  — If the control is 1, MOV to CR0 causes a general-protection exception if it attempts to set any bit in CR0 other than bit 0 (PE) or bit 31 (PG) to a value not supported in VMX operation. It remains the case, however, that MOV to CR0 causes a general-protection exception if it would result in CR0.PE = 0 and CR0.PG = 1 or if it would result in CR0.PG = 1, CR4.PAE = 0, and IA32_EFER.LME = 1.

• **MOV to CR3.** If the "enable EPT" VM-execution control is 1 and an execution of MOV to CR3 does not cause a VM exit (see Section 25.1.3), the value loaded into CR3 is treated as a guest-physical address; see Section 28.2.1.
  — If PAE paging is not being used, the instruction does not use the guest-physical address to access memory and it does not cause it to be translated through EPT.1
  — If PAE paging is being used, the instruction translates the guest-physical address through EPT and uses the result to load the four (4) page-directory-pointer-table entries (PDPTEs). The instruction does not use the
guest-physical addresses the PDPTEs to access memory and it does not cause them to be translated through EPT.

- **MOV to CR4.** An execution of MOV to CR4 that does not cause a VM exit (see Section 25.1.3) leaves unmodified any bit in CR4 corresponding to a bit set in the CR4 guest/host mask. Such an execution causes a general-protection exception if it attempts to set any bit in CR4 (not corresponding to a bit set in the CR4 guest/host mask) to a value not supported in VMX operation (see Section 23.8).

- **MOV to CR8.** If the MOV to CR8 instruction does not cause a VM exit (see Section 25.1.3), its behavior is modified if the "use TPR shadow" VM-execution control is 1; see Section 29.3.

- **MWAIT.** Behavior of the MWAIT instruction (which always causes an invalid-opcode exception—#UD—if CPL > 0) is determined by the setting of the "MWAIT exiting" VM-execution control:
  - If the "MWAIT exiting" VM-execution control is 1, MWAIT causes a VM exit.
  - If the "MWAIT exiting" VM-execution control is 0, MWAIT operates normally if one of the following are true: (1) ECX[0] is 0; (2) RFLAGS.IF = 1; or both of the following are true: (a) the "interrupt-window exiting" VM-execution control is 0; and (b) the logical processor has not recognized a pending virtual interrupt (see Section 29.2.1).
  - If the "MWAIT exiting" VM-execution control is 0, ECX[0] = 1, and RFLAGS.IF = 0, MWAIT does not cause the processor to enter an implementation-dependent optimized state if either the "interrupt-window exiting" VM-execution control is 1 or the logical processor has recognized a pending virtual interrupt; instead, control passes to the instruction following the MWAIT instruction.

- **RDMSR.** Section 25.1.3 identifies when executions of the RDMSR instruction cause VM exits. If such an execution causes neither a fault due to CPL > 0 nor a VM exit, the instruction’s behavior may be modified for certain values of ECX:
  - If ECX contains 10H (indicating the IA32_TIME_STAMP_COUNTER MSR), the value returned by the instruction is determined by the setting of the "use TSC offsetting" VM-execution control:
    - If the control is 0, RDMSR operates normally, loading EAX:EDX with the value of the IA32_TIME_STAMP_COUNTER MSR.
    - If the control is 1, the value returned is determined by the setting of the "use TSC scaling" VM-execution control:
      - If the control is 0, RDMSR loads EAX:EDX with the sum of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC offset.
      - If the control is 1, RDMSR first computes the product of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC multiplier. It then shifts the value of the product right 48 bits and loads EAX:EDX with the sum of that shifted value and the value of the TSC offset.
  - The 1-setting of the "use TSC-offsetting" VM-execution control does not affect executions of RDMSR if ECX contains 6E0H (indicating the IA32_TSC_DEADLINE MSR). Such executions return the APIC-timer deadline relative to the actual timestamp counter without regard to the TSC offset.
  - If ECX is in the range 800H–8FFH (indicating an APIC MSR), instruction behavior may be modified if the "virtualize x2APIC mode" VM-execution control is 1; see Section 29.5.

- **RDTSC.** Behavior of the RDTSC instruction is determined by the settings of the "RDTSC exiting" and "use TSC offsetting" VM-execution controls:
  - If both controls are 0, RDTSC operates normally.
  - If the "RDTSC exiting" VM-execution control is 0 and the "use TSC offsetting" VM-execution control is 1, the value returned is determined by the setting of the "use TSC scaling" VM-execution control:
    - If the control is 0, RDTSC loads EAX:EDX with the sum of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC offset.

1. A logical processor uses PAE paging if CR0.PG = 1, CR4.PAE = 1 and IA32_EFER.LMA = 0. See Section 4.4 in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A*. 

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• If the control is 1, RDTSC first computes the product of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC multiplier. It then shifts the value of the product right 48 bits and loads EAX:EDX with the sum of that shifted value and the value of the TSC offset.

— If the “RDTSC exiting” VM-execution control is 1, RDTSC causes a VM exit.

• RDTSCP. Behavior of the RDTSCP instruction is determined first by the setting of the “enable RDTSCP” VM-execution control:
  — If the “enable RDTSCP” VM-execution control is 0, RDTSCP causes an invalid-opcode exception (#UD). This exception takes priority over any other exception the instruction may incur.
  — If the “enable RDTSCP” VM-execution control is 1, treatment is based on the settings of the “RDTSC exiting” and “use TSC offsetting” VM-execution controls:
    • If both controls are 0, RDTSCP operates normally.
    • If the “RDTSC exiting” VM-execution control is 0 and the “use TSC offsetting” VM-execution control is 1, the value returned is determined by the setting of the “use TSC scaling” VM-execution control:
      — If the control is 0, RDTSCP loads EAX:EDX with the sum of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC offset.
      — If the control is 1, RDTSCP first computes the product of the value of the IA32_TIME_STAMP_COUNTER MSR and the value of the TSC multiplier. It then shifts the value of the product right 48 bits and loads EAX:EDX with the sum of that shifted value and the value of the TSC offset.
    In either case, RDTSCP also loads ECX with the value of bits 31:0 of the IA32_TSC_AUX MSR.
    • If the “RDTSC exiting” VM-execution control is 1, RDTSCP causes a VM exit.

• SMSW. The behavior of SMSW is determined by the CR0 guest/host mask and the CR0 read shadow. For each position corresponding to a bit clear in the CR0 guest/host mask, the destination operand is loaded with the value of the corresponding bit in CR0. For each position corresponding to a bit set in the CR0 guest/host mask, the destination operand is loaded with the value of the corresponding bit in the CR0 read shadow. Thus, if every bit is cleared in the CR0 guest/host mask, MOV from CR0 reads normally from CR0; if every bit is set in the CR0 guest/host mask, MOV from CR0 returns the value of the CR0 read shadow.

Note the following: (1) for any memory destination or for a 16-bit register destination, only the low 16 bits of the CR0 guest/host mask and the CR0 read shadow are used (bits 63:16 of a register destination are left unchanged); (2) for a 32-bit register destination, only the low 32 bits of the CR0 guest/host mask and the CR0 read shadow are used (bits 63:32 of the destination are cleared); and (3) depending on the contents of the CR0 guest/host mask and the CR0 read shadow, bits may be set in the destination that would never be set when reading directly from CR0.

• WRMSR. Section 25.1.3 identifies when executions of the WRMSR instruction cause VM exits. If such an execution neither a fault due to CPL > 0 nor a VM exit, the instruction’s behavior may be modified for certain values of ECX:
  — If ECX contains 79H (indicating IA32_BIOS_UPDT_TRIG MSR), no microcode update is loaded, and control passes to the next instruction. This implies that microcode updates cannot be loaded in VMX non-root operation.
  — If ECX contains 808H (indicating the TPR MSR), 80BH (the EOI MSR), or 83FH (self-IPI MSR), instruction behavior may modified if the “virtualize x2APIC mode” VM-execution control is 1; see Section 29.5.

• XRSTORS. Behavior of the XRSTORS instruction is determined first by the setting of the “enable XSAVES/XRSTORS” VM-execution control:
  — If the “enable XSAVES/XRSTORS” VM-execution control is 0, XRSTORS causes an invalid-opcode exception (#UD).
  — If the “enable XSAVES/XRSTORS” VM-execution control is 1, treatment is based on the value of the XSS-exiting bitmap (see Section 24.6.18):
    • XRSTORS causes a VM exit if any bit is set in the logical-AND of the following three values: EDX:EAX, the IA32_XSS MSR, and the XSS-exiting bitmap.
    • Otherwise, XRSTORS operates normally.
• **XSAVES.** Behavior of the XSAVES instruction is determined first by the setting of the “enable XSAVES/XRSTORS” VM-execution control:
  — If the “enable XSAVES/XRSTORS” VM-execution control is 0, XSAVES causes an invalid-opcode exception (#UD).
  — If the “enable XSAVES/XRSTORS” VM-execution control is 1, treatment is based on the value of the XSS-exiting bitmap (see Section 24.6.18):
    • XSAVES causes a VM exit if any bit is set in the logical-AND of the following three values: EDX:EAX, the IA32_XSS MSR, and the XSS-exiting bitmap.
    • Otherwise, XSAVES operates normally.

### 25.4 OTHER CHANGES IN VMX NON-ROOT OPERATION

Treatments of event blocking and of task switches differ in VMX non-root operation as described in the following sections.

#### 25.4.1 Event Blocking

Event blocking is modified in VMX non-root operation as follows:

• If the “external-interrupt exiting” VM-execution control is 1, RFLAGS.IF does not control the blocking of external interrupts. In this case, an external interrupt that is not blocked for other reasons causes a VM exit (even if RFLAGS.IF = 0).

• If the “external-interrupt exiting” VM-execution control is 1, external interrupts may or may not be blocked by STI or by MOV SS (behavior is implementation-specific).

• If the “NMI exiting” VM-execution control is 1, non-maskable interrupts (NMIs) may or may not be blocked by STI or by MOV SS (behavior is implementation-specific).

#### 25.4.2 Treatment of Task Switches

Task switches are not allowed in VMX non-root operation. Any attempt to effect a task switch in VMX non-root operation causes a VM exit. However, the following checks are performed (in the order indicated), possibly resulting in a fault, before there is any possibility of a VM exit due to task switch:

1. If a task gate is being used, appropriate checks are made on its P bit and on the proper values of the relevant privilege fields. The following cases detail the privilege checks performed:
   a. If CALL, INT \( n \), or JMP accesses a task gate in IA-32e mode, a general-protection exception occurs.
   b. If CALL, INT \( n \), INT3, INTO, or JMP accesses a task gate outside IA-32e mode, privilege-levels checks are performed on the task gate but, if they pass, privilege levels are not checked on the referenced task-state segment (TSS) descriptor.
   c. If CALL or JMP accesses a TSS descriptor directly in IA-32e mode, a general-protection exception occurs.
   d. If CALL or JMP accesses a TSS descriptor directly outside IA-32e mode, privilege levels are checked on the TSS descriptor.
   e. If a non-maskable interrupt (NMI), an exception, or an external interrupt accesses a task gate in the IDT in IA-32e mode, a general-protection exception occurs.
   f. If a non-maskable interrupt (NMI), an exception other than breakpoint exceptions (#BP) and overflow exceptions (#OF), or an external interrupt accesses a task gate in the IDT outside IA-32e mode, no privilege checks are performed.
   g. If IRET is executed with RFLAGS.NT = 1 in IA-32e mode, a general-protection exception occurs.
   h. If IRET is executed with RFLAGS.NT = 1 outside IA-32e mode, a TSS descriptor is accessed directly and no privilege checks are made.
2. Checks are made on the new TSS selector (for example, that is within GDT limits).
3. The new TSS descriptor is read. (A page fault results if a relevant GDT page is not present).
4. The TSS descriptor is checked for proper values of type (depends on type of task switch), P bit, S bit, and limit. Only if checks 1–4 all pass (do not generate faults) might a VM exit occur. However, the ordering between a VM exit due to a task switch and a page fault resulting from accessing the old TSS or the new TSS is implementation-specific. Some processors may generate a page fault (instead of a VM exit due to a task switch) if accessing either TSS would cause a page fault. Other processors may generate a VM exit due to a task switch even if accessing either TSS would cause a page fault.

If an attempt at a task switch through a task gate in the IDT causes an exception (before generating a VM exit due to the task switch) and that exception causes a VM exit, information about the event whose delivery accessed the task gate is recorded in the IDT-vectoring information fields and information about the exception that caused the VM exit is recorded in the VM-exit interruption-information fields. See Section 27.2. The fact that a task gate was being accessed is not recorded in the VMCS.

If an attempt at a task switch through a task gate in the IDT causes VM exit due to the task switch, information about the event whose delivery accessed the task gate is recorded in the IDT-vectoring fields of the VMCS. Since the cause of such a VM exit is a task switch and not an interruption, the valid bit for the VM-exit interruption information field is 0. See Section 27.2.

### 25.5 FEATURES SPECIFIC TO VMX NON-ROOT OPERATION

Some VM-execution controls support features that are specific to VMX non-root operation. These are the VMX-preemption timer (Section 25.5.1) and the monitor trap flag (Section 25.5.2), translation of guest-physical addresses (Section 25.5.3), VM functions (Section 25.5.5), and virtualization exceptions (Section 25.5.6).

#### 25.5.1 VMX-Preemption Timer

If the last VM entry was performed with the 1-setting of “activate VMX-preemption timer” VM-execution control, the VMX-preemption timer counts down (from the value loaded by VM entry; see Section 26.6.4) in VMX non-root operation. When the timer counts down to zero, it stops counting down and a VM exit occurs (see Section 25.2).

The VMX-preemption timer counts down at rate proportional to that of the timestamp counter (TSC). Specifically, the timer counts down by 1 every time bit X in the TSC changes due to a TSC increment. The value of X is in the range 0–31 and can be determined by consulting the VMX capability MSR IA32_VMX_MISC (see Appendix A.6).

The VMX-preemption timer operates in the C-states C0, C1, and C2; it also operates in the shutdown and wait-for-SIPI states. If the timer counts down to zero in any state other than the wait-for-SIPI state, the logical processor transitions to the C0 C-state and causes a VM exit; the timer does not cause a VM exit if it counts down to zero in the wait-for-SIPI state. The timer is not decremented in C-states deeper than C2.

Treatment of the timer in the case of system management interrupts (SMIs) and system-management mode (SMM) depends on whether the treatment of SMIs and SMM:

- If the default treatment of SMIs and SMM (see Section 34.14) is active, the VMX-preemption timer counts across an SMI to VMX non-root operation, subsequent execution in SMM, and the return from SMM via the RSM instruction. However, the timer can cause a VM exit only from VMX non-root operation. If the timer expires during SMI, in SMM, or during RSM, a timer-induced VM exit occurs immediately after RSM with its normal priority unless it is blocked based on activity state (Section 25.2).
- If the dual-monitor treatment of SMIs and SMM (see Section 34.15) is active, transitions into and out of SMM are VM exits and VM entries, respectively. The treatment of the VMX-preemption timer by those transitions is mostly the same as for ordinary VM exits and VM entries; Section 34.15.2 and Section 34.15.4 detail some differences.
25.5.2 Monitor Trap Flag

The monitor trap flag is a debugging feature that causes VM exits to occur on certain instruction boundaries in VMX non-root operation. Such VM exits are called MTF VM exits. An MTF VM exit may occur on an instruction boundary in VMX non-root operation as follows:

- If the “monitor trap flag” VM-execution control is 1 and VM entry is injecting a vectored event (see Section 26.5.1), an MTF VM exit is pending on the instruction boundary before the first instruction following the VM entry.
- If VM entry is injecting a pending MTF VM exit (see Section 26.5.2), an MTF VM exit is pending on the instruction boundary before the first instruction following the VM entry. This is the case even if the “monitor trap flag” VM-execution control is 0.
- If the “monitor trap flag” VM-execution control is 1, VM entry is not injecting an event, and a pending event (e.g., debug exception or interrupt) is delivered before an instruction can execute, an MTF VM exit is pending on the instruction boundary following delivery of the event (or any nested exception).
- Suppose that the “monitor trap flag” VM-execution control is 1, VM entry is not injecting an event, and the first instruction following VM entry is a REP-prefixed string instruction:
  - If the first iteration of the instruction causes a fault, an MTF VM exit is pending on the instruction boundary following delivery of the fault (or any nested exception).
  - If the first iteration of the instruction does not cause a fault, an MTF VM exit is pending on the instruction boundary after that iteration.
- Suppose that the “monitor trap flag” VM-execution control is 1, VM entry is not injecting an event, and the first instruction following VM entry is the XBEGIN instruction. In this case, an MTF VM exit is pending at the fallback instruction address of the XBEGIN instruction. This behavior applies regardless of whether advanced debugging of RTM transactional regions has been enabled (see Section 15.3.7, “RTM-Enabled Debugger Support,” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1).
- Suppose that the “monitor trap flag” VM-execution control is 1, VM entry is not injecting an event, and the first instruction following VM entry is neither a REP-prefixed string instruction nor the XBEGIN instruction:
  - If the instruction causes a fault, an MTF VM exit is pending on the instruction boundary following delivery of the fault (or any nested exception).
  - If the instruction does not cause a fault, an MTF VM exit is pending on the instruction boundary following execution of that instruction. If the instruction is INT3 or INTO, this boundary follows delivery of any software exception. If the instruction is INT n, this boundary follows delivery of a software interrupt. If the instruction is HLT, the MTF VM exit will be from the HLT activity state.

No MTF VM exit occurs if another VM exit occurs before reaching the instruction boundary on which an MTF VM exit would be pending (e.g., due to an exception or triple fault).

An MTF VM exit occurs on the instruction boundary on which it is pending unless a higher priority event takes precedence or the MTF VM exit is blocked due to the activity state:

- System-management interrupts (SMIs), INIT signals, and higher priority events take priority over MTF VM exits. MTF VM exits take priority over debug-trap exceptions and lower priority events.
- No MTF VM exit occurs if the processor is in either the shutdown activity state or wait-for-SIPI activity state. If a non-maskable interrupt subsequently takes the logical processor out of the shutdown activity state without causing a VM exit, an MTF VM exit is pending after delivery of that interrupt.

25.5.3 Translation of Guest-Physical Addresses Using EPT

The extended page-table mechanism (EPT) is a feature that can be used to support the virtualization of physical memory. When EPT is in use, certain physical addresses are treated as guest-physical addresses and are not used to access memory directly. Instead, guest-physical addresses are translated by traversing a set of EPT paging structures to produce physical addresses that are used to access memory.

1. This item includes the cases of an invalid opcode exception—#UD—generated by the UD2 instruction and a BOUND-range exceeded exception—#BR—generated by the BOUND instruction.
Details of the EPT mechanism are given in Section 28.2.

### 25.5.4 APIC Virtualization

APIC virtualization is a collection of features that can be used to support the virtualization of interrupts and the Advanced Programmable Interrupt Controller (APIC). When APIC virtualization is enabled, the processor emulates many accesses to the APIC, tracks the state of the virtual APIC, and delivers virtual interrupts — all in VMX non-root operation without a VM exit.

Details of the APIC virtualization are given in Chapter 29.

### 25.5.5 VM Functions

A **VM function** is an operation provided by the processor that can be invoked from VMX non-root operation without a VM exit. VM functions are enabled and configured by the settings of different fields in the VMCS. Software in VMX non-root operation invokes a VM function with the **VMFUNC** instruction; the value of EAX selects the specific VM function being invoked.

Section 25.5.5.1 explains how VM functions are enabled. Section 25.5.5.2 specifies the behavior of the VMFUNC instruction. Section 25.5.5.3 describes a specific VM function called **EPTP switching**.

#### 25.5.5.1 Enabling VM Functions

Software enables VM functions generally by setting the “enable VM functions” VM-execution control. A specific VM function is enabled by setting the corresponding VM-function control.

Suppose, for example, that software wants to enable EPTP switching (VM function 0; see Section 24.6.15). To do so, it must set the “activate secondary controls” VM-execution control (bit 31 of the primary processor-based VM-execution controls), the “enable VM functions” VM-execution control (bit 13 of the secondary processor-based VM-execution controls) and the “EPTP switching” VM-function control (bit 0 of the VM-function controls).

#### 25.5.5.2 General Operation of the VMFUNC Instruction

The VMFUNC instruction causes an invalid-opcode exception (#UD) if the “enable VM functions” VM-execution controls is 0 or the value of EAX is greater than 63 (only VM functions 0–63 can be enable). Otherwise, the instruction causes a VM exit if the bit at position EAX is 0 in the VM-function controls (the selected VM function is not enabled). If such a VM exit occurs, the basic exit reason used is 59 (3BH), indicating “VMFUNC”, and the length of the VMFUNC instruction is saved into the VM-exit instruction-length field. If the instruction causes neither an invalid-opcode exception nor a VM exit due to a disabled VM function, it performs the functionality of the VM function specified by the value in EAX.

Individual VM functions may perform additional fault checking (e.g., one might cause a general-protection exception if CPL > 0). In addition, specific VM functions may include checks that might result in a VM exit. If such a VM exit occurs, VM-exit information is saved as described in the previous paragraph. The specification of a VM function may indicate that additional VM-exit information is provided.

The specific behavior of the EPTP-switching VM function (including checks that result in VM exits) is given in Section 25.5.5.3.

#### 25.5.5.3 EPTP Switching

EPTP switching is VM function 0. This VM function allows software in VMX non-root operation to load a new value for the EPT pointer (EPTP), thereby establishing a different EPT paging-structure hierarchy (see Section 28.2 for details of the operation of EPT). Software is limited to selecting from a list of potential EPTP values configured in advance by software in VMX root operation.

---

1. “Enable VM functions” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if the “enable VM functions” VM-execution control were 0. See Section 24.6.2.
Specifically, the value of ECX is used to select an entry from the EPTP list, the 4-KByte structure referenced by the EPTP-list address (see Section 24.6.15; because this structure contains 512 8-Byte entries, VMFUNC causes a VM exit if ECX ≥ 512). If the selected entry is a valid EPTP value (it would not cause VM entry to fail; see Section 26.2.1.1), it is stored in the EPTP field of the current VMCS and is used for subsequent accesses using guest-physical addresses. The following pseudocode provides details:

```plaintext
IF ECX ≥ 512
    THEN VM exit;
ELSE
    tent_EPTP ← 8 bytes from EPTP-list address + 8 * ECX;
    IF tent_EPTP is not a valid EPTP value (would cause VM entry to fail if in EPTP)
        THEN VMexit;
        ELSE
            write tent_EPTP to the EPTP field in the current VMCS;
            use tent_EPTP as the new EPTP value for address translation;
            IF processor supports the 1-setting of the "EPT-violation #VE" VM-execution control
                THEN
                    write ECX[15:0] to EPTP-index field in current VMCS;
                    use ECX[15:0] as EPTP index for subsequent EPT-violation virtualization exceptions (see Section 25.5.6.2);
                FI;
            FI;
FI;
```

Execution of the EPTP-switching VM function does not modify the state of any registers; no flags are modified.

As noted in Section 25.5.5.2, an execution of the EPTP-switching VM function that causes a VM exit (as specified above), uses the basic exit reason 59, indicating "VMFUNC". The length of the VMFUNC instruction is saved into the VM-exit instruction-length field. No additional VM-exit information is provided.

An execution of VMFUNC loads EPTP from the EPTP list (and thus does not cause a fault or VM exit) is called an **EPTP-switching VMFUNC**. After an EPTP-switching VMFUNC, control passes to the next instruction. The logical processor starts creating and using guest-physical and combined mappings associated with the new value of bits 51:12 of EPTP; the combined mappings created and used are associated with the current VPID and PCID (these are not changed by VMFUNC). If the "enable VPID" VM-execution control is 0, an EPTP-switching VMFUNC invalidates combined mappings associated with VPID 0000H (for all PCIDs and for all EP4TA values, where EP4TA is the value of bits 51:12 of EPTP).

Because an EPTP-switching VMFUNC may change the translation of guest-physical addresses, it may affect use of the guest-physical address in CR3. The EPTP-switching VMFUNC cannot itself cause a VM exit due to an EPT violation or an EPT misconfiguration due to the translation of that guest-physical address through the new EPT paging structures. The following items provide details that apply if CR0.PG = 1:

- If 32-bit paging or IA-32e paging is in use (either CR4.PAE = 0 or IA32_EFER.LMA = 1), the next memory access with a linear address uses the translation of the guest-physical address in CR3 through the new EPT paging structures. As a result, this access may cause a VM exit due to an EPT violation or an EPT misconfiguration encountered during that translation.

- If PAE paging is in use (CR4.PAE = 1 and IA32_EFER.LMA = 0), an EPTP-switching VMFUNC does not load the four page-directory-pointer-table entries (PDPTEs) from the guest-physical address in CR3. The logical processor continues to use the four guest-physical addresses already present in the PDPTEs. The guest-physical address in CR3 is not translated through the new EPT paging structures (until some operation that would load the PDPTEs).

The EPTP-switching VMFUNC cannot itself cause a VM exit due to an EPT violation or an EPT misconfiguration encountered during the translation of a guest-physical address in any of the PDPTEs. A subsequent memory access with a linear address uses the translation of the guest-physical address in the appropriate PDPTE through the new EPT paging structures. As a result, such an access may cause a VM exit due to an EPT violation or an EPT misconfiguration encountered during that translation.

---

1. If the "enable VPID" VM-execution control is 0, the current VPID is 0000H; if CR4.PCIDE = 0, the current PCID is 000H.
If an EPTP-switching VMFUNC establishes an EPTP value that enables accessed and dirty flags for EPT (by setting bit 6), subsequent memory accesses may fail to set those flags as specified if there has been no appropriate execution of INVEPT since the last use of an EPTP value that does not enable accessed and dirty flags for EPT (because bit 6 is clear) and that is identical to the new value on bits 51:12.

IF the processor supports the 1-setting of the “EPT-violation #VE” VM-execution control, an EPTP-switching VMFUNC loads the value in ECX[15:0] into to EPTP-index field in current VMCS. Subsequent EPT-violation virtualization exceptions will save this value into the virtualization-exception information area (see Section 25.5.6.2);

25.5.6 Virtualization Exceptions

A virtualization exception is a new processor exception. It uses vector 20 and is abbreviated #VE.

A virtualization exception can occur only in VMX non-root operation. Virtualization exceptions occur only with certain settings of certain VM-execution controls. Generally, these settings imply that certain conditions that would normally cause VM exits instead cause virtualization exceptions.

In particular, the 1-setting of the “EPT-violation #VE” VM-execution control causes some EPT violations to generate virtualization exceptions instead of VM exits. Section 25.5.6.1 provides the details of how the processor determines whether an EPT violation causes a virtualization exception or a VM exit.

When the processor encounters a virtualization exception, it saves information about the exception to the virtualization-exception information area; see Section 25.5.6.2.

After saving virtualization-exception information, the processor delivers a virtualization exception as it would any other exception; see Section 25.5.6.3 for details.

25.5.6.1 Convertible EPT Violations

If the “EPT-violation #VE” VM-execution control is 0 (e.g., on processors that do not support this feature), EPT violations always cause VM exits. If instead the control is 1, certain EPT violations may be converted to cause virtualization exceptions instead; such EPT violations are convertible.

The values of certain EPT paging-structure entries determine which EPT violations are convertible. Specifically, bit 63 of certain EPT paging-structure entries may be defined to mean suppress #VE:

• If bits 2:0 of an EPT paging-structure entry are all 0, the entry is not present. If the processor encounters such an entry while translating a guest-physical address, it causes an EPT violation. The EPT violation is convertible if and only if bit 63 of the entry is 0.

• If bits 2:0 of an EPT paging-structure entry are not all 0, the following cases apply:
  — If the value of the EPT paging-structure entry is not supported, the entry is misconfigured. If the processor encounters such an entry while translating a guest-physical address, it causes an EPT misconfiguration (not an EPT violation). EPT misconfigurations always cause VM exits.
  — If the value of the EPT paging-structure entry is supported, the following cases apply:
    • If bit 7 of the entry is 1, or if the entry is an EPT PTE, the entry maps a page. If the processor uses such an entry to translate a guest-physical address, and if an access to that address causes an EPT violation, the EPT violation is convertible if and only if bit 63 of the entry is 0.
    • If bit 7 of the entry is 0 and the entry is not an EPT PTE, the entry references another EPT paging structure. The processor does not use the value of bit 63 of the entry to determine whether any subsequent EPT violation is convertible.

If an access to a guest-physical address causes an EPT violation, bit 63 of exactly one of the EPT paging-structure entries used to translate that address is used to determine whether the EPT violation is convertible: either a entry that is not present (if the guest-physical address does not translate to a physical address) or an entry that maps a page (if it does).

A convertible EPT violation instead causes a virtualization exception if the following all hold:

• CR0.PE = 1;

• the logical processor is not in the process of delivering an event through the IDT; and
• the 32 bits at offset 4 in the virtualization-exception information area are all 0.

Delivery of virtualization exceptions writes the value FFFFFFFFH to offset 4 in the virtualization-exception information area (see Section 25.5.6.2). Thus, once a virtualization exception occurs, another can occur only if software clears this field.

### 25.5.6.2 Virtualization-Exception Information

Virtualization exceptions save data into the virtualization-exception information area (see Section 24.6.17). Table 25-1 enumerates the data saved and the format of the area.

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The 32-bit value that would have been saved into the VMCS as an exit reason had a VM exit occurred instead of the virtualization exception. For EPT violations, this value is 48 (00000030H)</td>
</tr>
<tr>
<td>4</td>
<td>FFFFFFFF</td>
</tr>
<tr>
<td>8</td>
<td>The 64-bit value that would have been saved into the VMCS as an exit qualification had a VM exit occurred instead of the virtualization exception</td>
</tr>
<tr>
<td>16</td>
<td>The 64-bit value that would have been saved into the VMCS as a guest-linear address had a VM exit occurred instead of the virtualization exception</td>
</tr>
<tr>
<td>24</td>
<td>The 64-bit value that would have been saved into the VMCS as a guest-physical address had a VM exit occurred instead of the virtualization exception</td>
</tr>
<tr>
<td>32</td>
<td>The current 16-bit value of the EPTP index VM-execution control (see Section 24.6.17 and Section 25.5.5.3)</td>
</tr>
</tbody>
</table>

### 25.5.6.3 Delivery of Virtualization Exceptions

After saving virtualization-exception information, the processor treats a virtualization exception as it does other exceptions:

• If bit 20 (#VE) is 1 in the exception bitmap in the VMCS, a virtualization exception causes a VM exit (see below). If the bit is 0, the virtualization exception is delivered using gate descriptor 20 in the IDT.

• Virtualization exceptions produce no error code. Delivery of a virtualization exception pushes no error code on the stack.

• With respect to double faults, virtualization exceptions have the same severity as page faults. If delivery of a virtualization exception encounters a nested fault that is either contributory or a page fault, a double fault (#DF) is generated. See Chapter 6, "Interrupt 8—Double Fault Exception (#DF)" in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

It is not possible for a virtualization exception to be encountered while delivering another exception (see Section 25.5.6.1).

If a virtualization exception causes a VM exit directly (because bit 20 is 1 in the exception bitmap), information about the exception is saved normally in the VM-exit interruption information field in the VMCS (see Section 27.2.2). Specifically, the event is reported as a hardware exception with vector 20 and no error code. Bit 12 of the field (NMI unblocking due to IRET) is set normally.

If a virtualization exception causes a VM exit indirectly (because bit 20 is 0 in the exception bitmap and delivery of the exception generates an event that causes a VM exit), information about the exception is saved normally in the IDT-vectoring information field in the VMCS (see Section 27.2.3). Specifically, the event is reported as a hardware exception with vector 20 and no error code.
25.6 UNRESTRICTED GUESTS

The first processors to support VMX operation require CR0.PE and CR0.PG to be 1 in VMX operation (see Section 23.8). This restriction implies that guest software cannot be run in unpaged protected mode or in real-address mode. Later processors support a VM-execution control called "unrestricted guest".1 If this control is 1, CR0.PE and CR0.PG may be 0 in VMX non-root operation. Such processors allow guest software to run in unpaged protected mode or in real-address mode. The following items describe the behavior of such software:

- The MOV CR0 instructions does not cause a general-protection exception simply because it would set either CR0.PE and CR0.PG to 0. See Section 25.3 for details.
- A logical processor treats the values of CR0.PE and CR0.PG in VMX non-root operation just as it does outside VMX operation. Thus, if CR0.PE = 0, the processor operates as it does normally in real-address mode (for example, it uses the 16-bit interrupt table to deliver interrupts and exceptions). If CR0.PG = 0, the processor operates as it does normally when paging is disabled.
- Processor operation is modified by the fact that the processor is in VMX non-root operation and by the settings of the VM-execution controls just as it is in protected mode or when paging is enabled. Instructions, interrupts, and exceptions that cause VM exits in protected mode or when paging is enabled also do so in real-address mode or when paging is disabled. The following examples should be noted:
  - If CR0.PG = 0, page faults do not occur and thus cannot cause VM exits.
  - If CR0.PE = 0, invalid-TSS exceptions do not occur and thus cannot cause VM exits.
  - If CR0.PE = 0, the following instructions cause invalid-opcode exceptions and do not cause VM exits: INVEPT, INVVPID, LLDT, LTR, SLDT, STR, VMCLEAR, VMLAUNCH, VMPTRLD, VMPRTRST, VMREAD, VMRESUME, VMWRITE, VMXOFF, and VMXON.
- If CR0.PG = 0, each linear address is passed directly to the EPT mechanism for translation to a physical address.2 The guest memory type passed on to the EPT mechanism is WB (writeback).

1. “Unrestricted guest” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if the “unrestricted guest” VM-execution control were 0. See Section 24.6.2.
2. As noted in Section 26.2.1.1, the “enable EPT” VM-execution control must be 1 if the “unrestricted guest” VM-execution control is 1.
VMX NON-ROOT OPERATION
Software can enter VMX non-root operation using either of the VM-entry instructions VMLAUNCH and VMRESUME. VMLAUNCH can be used only with a VMCS whose launch state is clear and VMRESUME can be used only with a VMCS whose the launch state is launched. VMLAUNCH should be used for the first VM entry after VMCLEAR; VMRESUME should be used for subsequent VM entries with the same VMCS.

Each VM entry performs the following steps in the order indicated:

1. Basic checks are performed to ensure that VM entry can commence (Section 26.1).
2. The control and host-state areas of the VMCS are checked to ensure that they are proper for supporting VMX non-root operation and that the VMCS is correctly configured to support the next VM exit (Section 26.2).
3. The following may be performed in parallel or in any order (Section 26.3):
   - The guest-state area of the VMCS is checked to ensure that, after the VM entry completes, the state of the logical processor is consistent with IA-32 and Intel 64 architectures.
   - Processor state is loaded from the guest-state area and based on controls in the VMCS.
   - Address-range monitoring is cleared.
4. MSRs are loaded from the VM-entry MSR-load area (Section 26.4).
5. If VMLAUNCH is being executed, the launch state of the VMCS is set to “launched.”
6. An event may be injected in the guest context (Section 26.5).

Steps 1–4 above perform checks that may cause VM entry to fail. Such failures occur in one of the following three ways:

- Some of the checks in Section 26.1 may generate ordinary faults (for example, an invalid-opcode exception). Such faults are delivered normally.
- Some of the checks in Section 26.1 and all the checks in Section 26.2 cause control to pass to the instruction following the VM-entry instruction. The failure is indicated by setting RFLAGS.ZF1 (if there is a current VMCS) or RFLAGS.CF (if there is no current VMCS). If there is a current VMCS, an error number indicating the cause of the failure is stored in the VM-instruction error field. See Chapter 30 for the error numbers.
- The checks in Section 26.3 and Section 26.4 cause processor state to be loaded from the host-state area of the VMCS (as would be done on a VM exit). Information about the failure is stored in the VM-exit information fields. See Section 26.7 for details.

EFLAGS.TF = 1 causes a VM-entry instruction to generate a single-step debug exception only if failure of one of the checks in Section 26.1 and Section 26.2 causes control to pass to the following instruction. A VM-entry does not generate a single-step debug exception in any of the following cases: (1) the instruction generates a fault; (2) failure of one of the checks in Section 26.3 or in loading MSRs causes processor state to be loaded from the host-state area of the VMCS; or (3) the instruction passes all checks in Section 26.1, Section 26.2, and Section 26.3 and there is no failure in loading MSRs.

Section 34.15 describes the dual-monitor treatment of system-management interrupts (SMIs) and system-management mode (SMM). Under this treatment, code running in SMM returns using VM entries instead of the RSM instruction. A VM entry returns from SMM if it is executed in SMM and the “entry to SMM” VM-entry control is 0. VM entries that return from SMM differ from ordinary VM entries in ways that are detailed in Section 34.15.4.

---

1. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For IA-32 processors, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.). In a few places, notation such as EAX is used to refer specifically to lower 32 bits of the indicated register.
26.1 BASIC VM-ENTRY CHECKS

Before a VM entry commences, the current state of the logical processor is checked in the following order:

1. If the logical processor is in virtual-8086 mode or compatibility mode, an invalid-opcode exception is generated.
2. If the current privilege level (CPL) is not zero, a general-protection exception is generated.
3. If there is no current VMCS, RFLAGS.CF is set to 1 and control passes to the next instruction.
4. If there is a current VMCS but the current VMCS is a shadow VMCS (see Section 24.10), RFLAGS.CF is set to 1 and control passes to the next instruction.
5. If there is a current VMCS that is not a shadow VMCS, the following conditions are evaluated in order; any of these cause VM entry to fail:
   a. if there is MOV-SS blocking (see Table 24-3)
   b. if the VM entry is invoked by VMLAUNCH and the VMCS launch state is not clear
   c. if the VM entry is invoked by VMRESUME and the VMCS launch state is not launched

If any of these checks fail, RFLAGS.ZF is set to 1 and control passes to the next instruction. An error number indicating the cause of the failure is stored in the VM-instruction error field. See Chapter 30 for the error numbers.

26.2 CHECKS ON VMX CONTROLS AND HOST-STATE AREA

If the checks in Section 26.1 do not cause VM entry to fail, the control and host-state areas of the VMCS are checked to ensure that they are proper for supporting VMX non-root operation, that the VMCS is correctly configured to support the next VM exit, and that, after the next VM exit, the processor's state is consistent with the Intel 64 and IA-32 architectures.

VM entry fails if any of these checks fail. When such failures occur, control is passed to the next instruction, RFLAGS.ZF is set to 1 to indicate the failure, and the VM-instruction error field is loaded with an error number that indicates whether the failure was due to the controls or the host-state area (see Chapter 30).

These checks may be performed in any order. Thus, an indication by error number of one cause (for example, host state) does not imply that there are not also other errors. Different processors may thus give different error numbers for the same VMCS. Some checks prevent establishment of settings (or combinations of settings) that are currently reserved. Future processors may allow such settings (or combinations) and may not perform the corresponding checks. The correctness of software should not rely on VM-entry failures resulting from the checks documented in this section.

The checks on the controls and the host-state area are presented in Section 26.2.1 through Section 26.2.4. These sections reference VMCS fields that correspond to processor state. Unless otherwise stated, these references are to fields in the host-state area.

26.2.1 Checks on VMX Controls

This section identifies VM-entry checks on the VMX control fields.

26.2.1.1 VM-Execution Control Fields

VM entries perform the following checks on the VM-execution control fields:1

- Reserved bits in the pin-based VM-execution controls must be set properly. Software may consult the VMX capability MSRs to determine the proper settings (see Appendix A.3.1).

---

1. If the "activate secondary controls" primary processor-based VM-execution control is 0, VM entry operates as if each secondary processor-based VM-execution control were 0.
• Reserved bits in the primary processor-based VM-execution controls must be set properly. Software may consult the VMX capability MSRs to determine the proper settings (see Appendix A.3.2).

• If the “activate secondary controls” primary processor-based VM-execution control is 1, reserved bits in the secondary processor-based VM-execution controls must be cleared. Software may consult the VMX capability MSRs to determine which bits are reserved (see Appendix A.3.3).

If the “activate secondary controls” primary processor-based VM-execution control is 0 (or if the processor does not support the 1-setting of that control), no checks are performed on the secondary processor-based VM-execution controls. The logical processor operates as if all the secondary processor-based VM-execution controls were 0.

• The CR3-target count must not be greater than 4. Future processors may support a different number of CR3-target values. Software should read the VMX capability MSR IA32_VMX_MISC to determine the number of values supported (see Appendix A.6).

• If the “use I/O bitmaps” VM-execution control is 1, bits 11:0 of each I/O-bitmap address must be 0. Neither address should set any bits beyond the processor’s physical-address width.1,2

• If the “use MSR bitmaps” VM-execution control is 1, bits 11:0 of the MSR-bitmap address must be 0. The address should not set any bits beyond the processor’s physical-address width.3

• If the “use TPR shadow” VM-execution control is 1, the virtual-APIC address must satisfy the following checks:
  — Bits 11:0 of the address must be 0.
  — The address should not set any bits beyond the processor’s physical-address width.4

If all of the above checks are satisfied and the “use TPR shadow” VM-execution control is 1, bytes 3:1 of VTPR (see Section 29.1.1) may be cleared (behavior may be implementation-specific).

The clearing of these bytes may occur even if the VM entry fails. This is true either if the failure causes control to pass to the instruction following the VM-entry instruction or if it causes processor state to be loaded from the host-state area of the VMCS.

• If the “use TPR shadow” VM-execution control is 1 and the “virtual-interrupt delivery” VM-execution control is 0, bits 31:4 of the TPR threshold VM-execution control field must be 0.5

• The following check is performed if the “use TPR shadow” VM-execution control is 1 and the “virtualize APIC accesses” and “virtual-interrupt delivery” VM-execution controls are both 0: the value of bits 3:0 of the TPR threshold VM-execution control field should not be greater than the value of bits 7:4 of VTPR (see Section 29.1.1).

• If the “NMI exiting” VM-execution control is 0, the “virtual NMI” VM-execution control must be 0.

• If the “virtual NMI” VM-execution control is 0, the “NMI-window exiting” VM-execution control must be 0.

• If the “virtualize APIC accesses” VM-execution control is 1, the APIC-access address must satisfy the following checks:
  — Bits 11:0 of the address must be 0.
  — The address should not set any bits beyond the processor’s physical-address width.6

• If the “use TPR shadow” VM-execution control is 0, the following VM-execution controls must also be 0: “virtualize x2APIC mode”, “APIC-register virtualization”, and “virtual interrupt delivery”.7

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1. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.

2. If IA32_VMX_BASIC[48] is read as 1, these addresses must not set any bits in the range 63:32; see Appendix A.1.

3. If IA32_VMX_BASIC[48] is read as 1, this address must not set any bits in the range 63:32; see Appendix A.1.

4. If IA32_VMX_BASIC[48] is read as 1, this address must not set any bits in the range 63:32; see Appendix A.1.

5. “Virtual-interrupt delivery” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “virtual-interrupt delivery” VM-execution control were 0. See Section 24.6.2.

6. If IA32_VMX_BASIC[48] is read as 1, this address must not set any bits in the range 63:32; see Appendix A.1.

7. “Virtualize x2APIC mode” and “APIC-register virtualization” are secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if these controls were 0. See Section 24.6.2.
• If the "virtualize x2APIC mode" VM-execution control is 1, the "virtualize APIC accesses" VM-execution control must be 0.
• If the "virtual-interrupt delivery" VM-execution control is 1, the "external-interrupt exiting" VM-execution control must be 1.
• If the "process posted interrupts" VM-execution control is 1, the following must be true:
  — The "virtual-interrupt delivery" VM-execution control is 1.
  — The "acknowledge interrupt on exit" VM-exit control is 1.
  — The posted-interrupt notification vector has a value in the range 0–255 (bits 15:8 are all 0).
  — Bits 5:0 of the posted-interrupt descriptor address are all 0.
  — The posted-interrupt descriptor address does not set any bits beyond the processor's physical-address width.
• If the "enable VPID" VM-execution control is 1, the value of the VPID VM-execution control field must not be 0000H.
• If the "enable EPT" VM-execution control is 1, the EPTP VM-execution control field (see Table 24-8 in Section 24.6.11) must satisfy the following checks:
  — The EPT memory type (bits 2:0) must be a value supported by the processor as indicated in the IA32_VMX_EPT_VPID_CAP MSR (see Appendix A.10).
  — Bits 5:3 (1 less than the EPT page-walk length) must be 3, indicating an EPT page-walk length of 4; see Section 28.2.2.
  — Bit 6 (enable bit for accessed and dirty flags for EPT) must be 0 if bit 21 of the IA32_VMX_EPT_VPID_CAP MSR (see Appendix A.10) is read as 0, indicating that the processor does not support accessed and dirty flags for EPT.
  — Reserved bits 11:7 and 63:N (where N is the processor's physical-address width) must all be 0.
• If the "enable PML" VM-execution control is 1, the "enable EPT" VM-execution control must also be 1. In addition, the PML address must satisfy the following checks:
  — Bits 11:0 of the address must be 0.
  — The address should not set any bits beyond the processor's physical-address width.
• If the "unrestricted guest" VM-execution control is 1, the "enable EPT" VM-execution control must also be 1.
• If the "enable VM functions" processor-based VM-execution control is 1, reserved bits in the VM-function controls must be clear. Software may consult the VMX capability MSRs to determine which bits are reserved (see Appendix A.11). In addition, the following check is performed based on the setting of bits in the VM-function controls (see Section 24.6.15):
  — If "EPTP switching" VM-function control is 1, the "enable EPT" VM-execution control must also be 1. In addition, the EPTP-list address must satisfy the following checks:

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1. "Process posted interrupts" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "process posted interrupts" VM-execution control were 0. See Section 24.6.2.
2. If IA32_VMX_BASIC[48] is read as 1, this address must not set any bits in the range 63:32; see Appendix A.1.
3. "Enable VPID" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "enable VPID" VM-execution control were 0. See Section 24.6.2.
4. "Enable EPT" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "enable EPT" VM-execution control were 0. See Section 24.6.2.
5. "Enable PML" and "enable EPT" are both secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if both these controls were 0. See Section 24.6.2.
6. If IA32_VMX_BASIC[48] is read as 1, this address must not set any bits in the range 63:32; see Appendix A.1.
7. "Unrestricted guest" and "enable EPT" are both secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if both these controls were 0. See Section 24.6.2.
8. "Enable VM functions" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "enable VM functions" VM-execution control were 0. See Section 24.6.2.
• Bits 11:0 of the address must be 0.
• The address must not set any bits beyond the processor’s physical-address width.

If the “enable VM functions” processor-based VM-execution control is 0, no checks are performed on the VM-function controls.

• If the “VMCS shadowing” VM-execution control is 1, the VMREAD-bitmap and VMWRITE-bitmap addresses must each satisfy the following checks:¹
  — Bits 11:0 of the address must be 0.
  — The address must not set any bits beyond the processor’s physical-address width.

• If the “EPT-violation #VE” VM-execution control is 1, the virtualization-exception information address must satisfy the following checks:²
  — Bits 11:0 of the address must be 0.
  — The address must not set any bits beyond the processor’s physical-address width.

### 26.2.1.2 VM-Exit Control Fields

VM entries perform the following checks on the VM-exit control fields.

• Reserved bits in the VM-exit controls must be set properly. Software may consult the VMX capability MSRs to determine the proper settings (see Appendix A.4).

• If the “activate VMX-preemption timer” VM-execution control is 0, the “save VMX-preemption timer value” VM-exit control must also be 0.

• The following checks are performed for the VM-exit MSR-store address if the VM-exit MSR-store count field is non-zero:
  — The lower 4 bits of the VM-exit MSR-store address must be 0. The address should not set any bits beyond the processor’s physical-address width.³
  — The address of the last byte in the VM-exit MSR-store area should not set any bits beyond the processor’s physical-address width. The address of this last byte is VM-exit MSR-store address + (MSR count * 16) – 1. (The arithmetic used for the computation uses more bits than the processor’s physical-address width.) If IA32_VMX_BASIC[48] is read as 1, neither address should set any bits in the range 63:32; see Appendix A.1.

• The following checks are performed for the VM-exit MSR-load address if the VM-exit MSR-load count field is non-zero:
  — The lower 4 bits of the VM-exit MSR-load address must be 0. The address should not set any bits beyond the processor’s physical-address width.
  — The address of the last byte in the VM-exit MSR-load area should not set any bits beyond the processor’s physical-address width. The address of this last byte is VM-exit MSR-load address + (MSR count * 16) – 1. (The arithmetic used for the computation uses more bits than the processor’s physical-address width.) If IA32_VMX_BASIC[48] is read as 1, neither address should set any bits in the range 63:32; see Appendix A.1.

### 26.2.1.3 VM-Entry Control Fields

VM entries perform the following checks on the VM-entry control fields.

1. “VMCS shadowing” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “VMCS shadowing” VM-execution control were 0. See Section 24.6.2.

2. “EPT-violation #VE” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “EPT-violation #VE” VM-execution control were 0. See Section 24.6.2.

3. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
Reserved bits in the VM-entry controls must be set properly. Software may consult the VMX capability MSRs to determine the proper settings (see Appendix A.5).

Fields relevant to VM-entry event injection must be set properly. These fields are the VM-entry interruption-information field (see Table 24-13 in Section 24.8.3), the VM-entry exception error code, and the VM-entry instruction length. If the valid bit (bit 31) in the VM-entry interruption-information field is 1, the following must hold:

The field’s interruption type (bits 10:8) is not set to a reserved value. Value 1 is reserved on all logical processors; value 7 (other event) is reserved on logical processors that do not support the 1-setting of the “monitor trap flag” VM-execution control.

The field’s vector (bits 7:0) is consistent with the interruption type:
- If the interruption type is non-maskable interrupt (NMI), the vector is 2.
- If the interruption type is hardware exception, the vector is at most 31.
- If the interruption type is other event, the vector is 0 (pending MTF VM exit).

The field’s deliver-error-code bit (bit 11) is 1 if and only if (1) either (a) the “unrestricted guest” VM-execution control is 0; or (b) bit 0 (corresponding to CR0.PE) is set in the CR0 field in the guest-state area; (2) the interruption type is hardware exception; and (3) the vector indicates an exception that would normally deliver an error code (8 = #DF; 10 = TS; 11 = #NP; 12 = #SS; 13 = #GP; 14 = #PF; or 17 = #AC).

Reserved bits in the field (30:12) are 0.

If the deliver-error-code bit (bit 11) is 1, bits 31:15 of the VM-entry exception error-code field are 0.

If the interruption type is software interrupt, software exception, or privileged software exception, the VM-entry instruction-length field is in the range 1–15.

The following checks are performed for the VM-entry MSR-load address if the VM-entry MSR-load count field is non-zero:

The lower 4 bits of the VM-entry MSR-load address must be 0. The address should not set any bits beyond the processor’s physical-address width.1

The address of the last byte in the VM-entry MSR-load area should not set any bits beyond the processor’s physical-address width. The address of this last byte is VM-entry MSR-load address + (MSR count * 16) – 1. (The arithmetic used for the computation uses more bits than the processor’s physical-address width.)

If IA32_VMX_BASIC[48] is read as 1, neither address should set any bits in the range 63:32; see Appendix A.1.

If the processor is not in SMM, the “entry to SMM” and “deactivate dual-monitor treatment” VM-entry controls must be 0.

The “entry to SMM” and “deactivate dual-monitor treatment” VM-entry controls cannot both be 1.

### 26.2.2 Checks on Host Control Registers and MSRs

The following checks are performed on fields in the host-state area that correspond to control registers and MSRs:

- The CR0 field must not set any bit to a value not supported in VMX operation (see Section 23.8).2
- The CR4 field must not set any bit to a value not supported in VMX operation (see Section 23.8).
- On processors that support Intel 64 architecture, the CR3 field must be such that bits 63:52 and bits in the range 51:32 beyond the processor’s physical-address width must be 0.3,4

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1. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
2. The bits corresponding to CR0.NW (bit 29) and CR0.CD (bit 30) are never checked because the values of these bits are not changed by VM exit; see Section 27.5.1.
3. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
On processors that support Intel 64 architecture, the IA32_SYSENTER_ESP field and the IA32_SYSENTER_EIP field must each contain a canonical address.

If the "load IA32_PERF_GLOBAL_CTRL" VM-exit control is 1, bits reserved in the IA32_PERF_GLOBAL_CTRL MSR must be 0 in the field for that register (see Figure 18-3).

If the "load IA32_PAT" VM-exit control is 1, the value of the field for the IA32_PAT MSR must be one that could be written by WRMSR without fault at CPL 0. Specifically, each of the 8 bytes in the field must have one of the values 0 (UC), 1 (WC), 4 (WT), 5 (WP), 6 (WB), or 7 (UC-).

If the "load IA32_EFER" VM-exit control is 1, bits reserved in the IA32_EFER MSR must be 0 in the field for that register. In addition, the values of the LMA and LME bits in the field must each be that of the "host address-space size" VM-exit control.

### 26.2.3 Checks on Host Segment and Descriptor-Table Registers

The following checks are performed on fields in the host-state area that correspond to segment and descriptor-table registers:

- In the selector field for each of CS, SS, DS, ES, FS, GS and TR, the RPL (bits 1:0) and the TI flag (bit 2) must be 0.
- The selector fields for CS and TR cannot be 0000H.
- The selector field for SS cannot be 0000H if the "host address-space size" VM-exit control is 0.
- On processors that support Intel 64 architecture, the base-address fields for FS, GS, GDTR, IDTR, and TR must contain canonical addresses.

### 26.2.4 Checks Related to Address-Space Size

On processors that support Intel 64 architecture, the following checks related to address-space size are performed on VMX controls and fields in the host-state area:

- If the logical processor is outside IA-32e mode (if IA32_EFER.LMA = 0) at the time of VM entry, the following must hold:
  - The "IA-32e mode guest" VM-entry control is 0.
  - The "host address-space size" VM-exit control is 0.
- If the logical processor is in IA-32e mode (if IA32_EFER.LMA = 1) at the time of VM entry, the "host address-space size" VM-exit control must be 1.
- If the "host address-space size" VM-exit control is 0, the following must hold:
  - The "IA-32e mode guest" VM-entry control is 0.
  - Bit 17 of the CR4 field (corresponding to CR4.PCIDE) is 0.
  - Bits 63:32 in the RIP field is 0.
- If the "host address-space size" VM-exit control is 1, the following must hold:
  - Bit 5 of the CR4 field (corresponding to CR4.PAE) is 1.
  - The RIP field contains a canonical address.

On processors that do not support Intel 64 architecture, checks are performed to ensure that the "IA-32e mode guest" VM-entry control and the "host address-space size" VM-exit control are both 0.

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4. Bit 63 of the CR3 field in the host-state area must be 0. This is true even though, if CR4.PCIDE = 1, bit 63 of the source operand to MOV to CR3 is used to determine whether cached translation information is invalidated.
### 26.3 Checking and Loading Guest State

If all checks on the VMX controls and the host-state area pass (see Section 26.2), the following operations take place concurrently: (1) the guest-state area of the VMCS is checked to ensure that, after the VM entry completes, the state of the logical processor is consistent with IA-32 and Intel 64 architectures; (2) processor state is loaded from the guest-state area or as specified by the VM-entry control fields; and (3) address-range monitoring is cleared.

Because the checking and the loading occur concurrently, a failure may be discovered only after some state has been loaded. For this reason, the logical processor responds to such failures by loading state from the host-state area, as it would for a VM exit. See Section 26.7.

#### 26.3.1 Checks on the Guest State Area

This section describes checks performed on fields in the guest-state area. These checks may be performed in any order. Some checks prevent establishment of settings (or combinations of settings) that are currently reserved. Future processors may allow such settings (or combinations) and may not perform the corresponding checks. The correctness of software should not rely on VM-entry failures resulting from the checks documented in this section.

The following subsections reference fields that correspond to processor state. Unless otherwise stated, these references are to fields in the guest-state area.

#### 26.3.1.1 Checks on Guest Control Registers, Debug Registers, and MSRs

The following checks are performed on fields in the guest-state area corresponding to control registers, debug registers, and MSRs:

- The CR0 field must not set any bit to a value not supported in VMX operation (see Section 23.8). The following are exceptions:
  - Bit 0 (corresponding to CR0.PE) and bit 31 (PG) are not checked if the “unrestricted guest” VM-execution control is 1.\(^1\)
  - Bit 29 (corresponding to CR0.NW) and bit 30 (CD) are never checked because the values of these bits are not changed by VM entry; see Section 26.3.2.1.
- If bit 31 in the CR0 field (corresponding to PG) is 1, bit 0 in that field (PE) must also be 1.\(^2\)
- The CR4 field must not set any bit to a value not supported in VMX operation (see Section 23.8).
- If the “load debug controls” VM-entry control is 1, bits reserved in the IA32_DEBUGCTL MSR must be 0 in the field for that register. The first processors to support the virtual-machine extensions supported only the 1-setting of this control and thus performed this check unconditionally.
- The following checks are performed on processors that support Intel 64 architecture:
  - If the “IA-32e mode guest” VM-entry control is 1, bit 31 in the CR0 field (corresponding to CR0.PG) and bit 5 in the CR4 field (corresponding to CR4.PAE) must each be 1.\(^3\)
  - If the “IA-32e mode guest” VM-entry control is 0, bit 17 in the CR4 field (corresponding to CR4.PCIDE) must be 0.
  - The CR3 field must be such that bits 63:52 and bits in the range 51:32 beyond the processor’s physical-address width are 0.\(^4,5\)

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1. “Unrestricted guest” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “unrestricted guest” VM-execution control were 0. See Section 24.6.2.
2. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PE must be 1 in VMX operation, bit 0 in the CR0 field must be 1 unless the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
3. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PG must be 1 in VMX operation, bit 31 in the CR0 field must be 1 unless the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
4. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
— If the “load debug controls” VM-entry control is 1, bits 63:32 in the DR7 field must be 0. The first processors to support the virtual-machine extensions supported only the 1-setting of this control and thus performed this check unconditionally (if they supported Intel 64 architecture).

— The IA32_SYSENTER_ESP field and the IA32_SYSENTER_EIP field must each contain a canonical address.

• If the “load IA32_PERF_GLOBAL_CTRL” VM-entry control is 1, bits reserved in the IA32_PERF_GLOBAL_CTRL MSR must be 0 in the field for that register (see Figure 18-3).

• If the “load IA32_PAT” VM-entry control is 1, the value of the field for the IA32_PAT MSR must be one that could be written by WRMSR without fault at CPL 0. Specifically, each of the 8 bytes in the field must have one of the values 0 (UC), 1 (WC), 4 (WT), 5 (WP), 6 (WB), or 7 (UC-).

• If the “load IA32_EFER” VM-entry control is 1, the following checks are performed on the field for the IA32_EFER MSR:
  — Bits reserved in the IA32_EFER MSR must be 0.
  — Bit 10 (corresponding to IA32_EFER.LMA) must equal the value of the “IA-32e mode guest” VM-entry control. It must also be identical to bit 8 (LME) if bit 31 in the CR0 field (corresponding to CR0.PG) is 1.\(^1\)

26.3.1.2 Checks on Guest Segment Registers

This section specifies the checks on the fields for CS, SS, DS, ES, FS, GS, TR, and LDTR. The following terms are used in defining these checks:

• The guest will be **virtual-8086** if the VM flag (bit 17) is 1 in the RFLAGS field in the guest-state area.

• The guest will be **IA-32e mode** if the “IA-32e mode guest” VM-entry control is 1. (This is possible only on processors that support Intel 64 architecture.)

• Any one of these registers is said to be **usable** if the unusable bit (bit 16) is 0 in the access-rights field for that register.

The following are the checks on these fields:

• Selector fields.
  — TR. The TI flag (bit 2) must be 0.
  — LDTR. If LDTR is usable, the TI flag (bit 2) must be 0.
  — SS. If the guest will not be virtual-8086 and the “unrestricted guest” VM-execution control is 0, the RPL (bits 1:0) must equal the RPL of the selector field for CS.\(^2\)

• Base-address fields.
  — CS, SS, DS, ES, FS, GS. If the guest will be virtual-8086, the address must be the selector field shifted left 4 bits (multiplied by 16).

  — The following checks are performed on processors that support Intel 64 architecture:
    • TR, FS, GS. The address must be canonical.
    • LDTR. If LDTR is usable, the address must be canonical.
    • CS. Bits 63:32 of the address must be zero.
    • SS, DS, ES. If the register is usable, bits 63:32 of the address must be zero.

• Limit fields for CS, SS, DS, ES, FS, GS. If the guest will be virtual-8086, the field must be 0000FFFFH.

• Access-rights fields.
  — CS, SS, DS, ES, FS, GS.

5. Bit 63 of the CR3 field in the guest-state area must be 0. This is true even though, if CR4.PCIDE = 1, bit 63 of the source operand to MOV to CR3 is used to determine whether cached translation information is invalidated.

1. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PG must be 1 in VMX operation, bit 31 in the CR0 field must be 1 unless the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.

2. “Unrestricted guest” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “unrestricted guest” VM-execution control were 0. See Section 24.6.2.
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• If the guest will be virtual-8086, the field must be 000000F3H. This implies the following:
  — Bits 3:0 (Type) must be 3, indicating an expand-up read/write accessed data segment.
  — Bit 4 (S) must be 1.
  — Bits 6:5 (DPL) must be 3.
  — Bit 7 (P) must be 1.
  — Bits 11:8 (reserved), bit 12 (software available), bit 13 (reserved/L), bit 14 (D/B), bit 15 (G),
    bit 16 (unusable), and bits 31:17 (reserved) must all be 0.
• If the guest will not be virtual-8086, the different sub-fields are considered separately:
  — Bits 3:0 (Type).
    • CS. The values allowed depend on the setting of the “unrestricted guest” VM-execution control:
      — If the control is 0, the Type must be 9, 11, 13, or 15 (accessed code segment).
      — If the control is 1, the Type must be either 3 (read/write accessed expand-up data segment) or one of 9, 11, 13, and 15 (accessed code segment).
    • SS. If SS is usable, the Type must be 3 or 7 (read/write, accessed data segment).
    • DS, ES, FS, GS. The following checks apply if the register is usable:
      — Bit 0 of the Type must be 1 (accessed).
      — If bit 3 of the Type is 1 (code segment), then bit 1 of the Type must be 1 (readable).
  — Bit 4 (S). If the register is CS or if the register is usable, S must be 1.
  — Bits 6:5 (DPL).
    • CS.
      — If the Type is 3 (read/write accessed expand-up data segment), the DPL must be 0. The Type can be 3 only if the “unrestricted guest” VM-execution control is 1.
      — If the Type is 9 or 11 (non-conforming code segment), the DPL must equal the DPL in the access-rights field for SS.
      — If the Type is 13 or 15 (conforming code segment), the DPL cannot be greater than the DPL in the access-rights field for SS.
    • SS.
      — If the “unrestricted guest” VM-execution control is 0, the DPL must equal the RPL from the selector field.
      — The DPL must be 0 either if the Type in the access-rights field for CS is 3 (read/write accessed expand-up data segment) or if bit 0 in the CR0 field (corresponding to CR0.PE) is 0.1
    • DS, ES, FS, GS. The DPL cannot be less than the RPL in the selector field if (1) the “unrestricted guest” VM-execution control is 0; (2) the register is usable; and (3) the Type in the access-rights field is in the range 0 – 11 (data segment or non-conforming code segment).
  — Bit 7 (P). If the register is CS or if the register is usable, P must be 1.
  — Bits 11:8 (reserved). If the register is CS or if the register is usable, these bits must all be 0.
  — Bit 14 (D/B). For CS, D/B must be 0 if the guest will be IA-32e mode and the L bit (bit 13) in the access-rights field is 1.
  — Bit 15 (G). The following checks apply if the register is CS or if the register is usable:

1. The following apply if either the “unrestricted guest” VM-execution control or bit 31 of the primary processor-based VM-execution controls is 0: (1) bit 0 in the CR0 field must be 1 if the capability MSR IA32_VMX_CRO_FIXED0 reports that CR0.PE must be 1 in VMX operation; and (2) the Type in the access-rights field for CS cannot be 3.
• If any bit in the limit field in the range 11:0 is 0, G must be 0.
• If any bit in the limit field in the range 31:20 is 1, G must be 1.
  — Bits 31:17 (reserved). If the register is CS or if the register is usable, these bits must all be 0.
— TR. The different sub-fields are considered separately:
  • Bits 3:0 (Type).
    — If the guest will not be IA-32e mode, the Type must be 3 (16-bit busy TSS) or 11 (32-bit busy TSS).
    — If the guest will be IA-32e mode, the Type must be 11 (64-bit busy TSS).
  • Bit 4 (S). S must be 0.
  • Bit 7 (P). P must be 1.
  • Bits 11:8 (reserved). These bits must all be 0.
  • Bit 15 (G).
    — If any bit in the limit field in the range 11:0 is 0, G must be 0.
    — If any bit in the limit field in the range 31:20 is 1, G must be 1.
  • Bit 16 (Unusable). The unusable bit must be 0.
  • Bits 31:17 (reserved). These bits must all be 0.
— LDTR. The following checks on the different sub-fields apply only if LDTR is usable:
  • Bits 3:0 (Type). The Type must be 2 (LDT).
  • Bit 4 (S). S must be 0.
  • Bit 7 (P). P must be 1.
  • Bits 11:8 (reserved). These bits must all be 0.
  • Bit 15 (G).
    — If any bit in the limit field in the range 11:0 is 0, G must be 0.
    — If any bit in the limit field in the range 31:20 is 1, G must be 1.
  • Bits 31:17 (reserved). These bits must all be 0.

26.3.1.3 Checks on Guest Descriptor-Table Registers

The following checks are performed on the fields for GDTR and IDTR:
• On processors that support Intel 64 architecture, the base-address fields must contain canonical addresses.
• Bits 31:16 of each limit field must be 0.

26.3.1.4 Checks on Guest RIP and RFLAGS

The following checks are performed on fields in the guest-state area corresponding to RIP and RFLAGS:
• RIP. The following checks are performed on processors that support Intel 64 architecture:
  — Bits 63:32 must be 0 if the “IA-32e mode guest” VM-entry control is 0 or if the L bit (bit 13) in the access-rights field for CS is 0.
  — If the processor supports N < 64 linear-address bits, bits 63:N must be identical if the “IA-32e mode guest” VM-entry control is 1 and the L bit in the access-rights field for CS is 1.1 (No check applies if the processor supports 64 linear-address bits.)

1. Software can determine the number N by executing CPUID with 80000008H in EAX. The number of linear-address bits supported is returned in bits 15:8 of EAX.
VM ENTRIES

• RFLAGS.
  — Reserved bits 63:22 (bits 31:22 on processors that do not support Intel 64 architecture), bit 15, bit 5 and bit 3 must be 0 in the field, and reserved bit 1 must be 1.
  — The VM flag (bit 17) must be 0 either if the "IA-32e mode guest" VM-entry control is 1 or if bit 0 in the CR0 field (corresponding to CR0.PE) is 0.¹
  — The IF flag (RFLAGS[bit 9]) must be 1 if the valid bit (bit 31) in the VM-entry interruption-information field is 1 and the interruption type (bits 10:8) is external interrupt.

26.3.1.5 Checks on Guest Non-Register State

The following checks are performed on fields in the guest-state area corresponding to non-register state:

• Activity state.
  — The activity-state field must contain a value in the range 0 – 3, indicating an activity state supported by the implementation (see Section 24.4.2). Future processors may include support for other activity states. Software should read the VMX capability MSR IA32_VMX_MISC (see Appendix A.6) to determine what activity states are supported.
  — The activity-state field must not indicate the HLT state if the DPL (bits 6:5) in the access-rights field for SS is not 0.²
  — The activity-state field must indicate the active state if the interruptibility-state field indicates blocking by either MOV-SS or by STI (if either bit 0 or bit 1 in that field is 1).
  — If the valid bit (bit 31) in the VM-entry interruption-information field is 1, the interruption to be delivered (as defined by interruption type and vector) must not be one that would normally be blocked while a logical processor is in the activity state corresponding to the contents of the activity-state field. The following items enumerate the interruptions (as specified in the VM-entry interruption-information field) whose injection is allowed for the different activity states:
    • Active. Any interruption is allowed.
    • HLT. The only events allowed are the following:
      — Those with interruption type external interrupt or non-maskable interrupt (NMI).
      — Those with interruption type hardware exception and vector 1 (debug exception) or vector 18 (machine-check exception).
      — Those with interruption type other event and vector 0 (pending MTF VM exit).
      See Table 24-13 in Section 24.8.3 for details regarding the format of the VM-entry interruption-information field.
    • Shutdown. Only NMIs and machine-check exceptions are allowed.
    • Wait-for-SIPI. No interruptions are allowed.
      — The activity-state field must not indicate the wait-for-SIPI state if the "entry to SMM" VM-entry control is 1.

• Interruptibility state.
  — The reserved bits (bits 31:4) must be 0.
  — The field cannot indicate blocking by both STI and MOV SS (bits 0 and 1 cannot both be 1).
  — Bit 0 (blocking by STI) must be 0 if the IF flag (bit 9) is 0 in the RFLAGS field.
  — Bit 0 (blocking by STI) and bit 1 (blocking by MOV-SS) must both be 0 if the valid bit (bit 31) in the VM-entry interruption-information field is 1 and the interruption type (bits 10:8) in that field has value 0, indicating external interrupt.

¹ If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PE must be 1 in VMX operation, bit 0 in the CR0 field must be 1 unless the "unrestricted guest" VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
² As noted in Section 24.4.1, SS.DPL corresponds to the logical processor's current privilege level (CPL).
— Bit 1 (blocking by MOV-SS) must be 0 if the valid bit (bit 31) in the VM-entry interruption-information field is 1 and the interruption type (bits 10:8) in that field has value 2, indicating non-maskable interrupt (NMI).
— Bit 2 (blocking by SMI) must be 0 if the processor is not in SMM.
— Bit 2 (blocking by SMI) must be 1 if the "entry to SMM" VM-entry control is 1.
— A processor may require bit 0 (blocking by STI) to be 0 if the valid bit (bit 31) in the VM-entry interruption-information field is 1 and the interruption type (bits 10:8) in that field has value 2, indicating NMI. Other processors may not make this requirement.
— Bit 3 (blocking by NMI) must be 0 if the "virtual NMIs" VM-execution control is 1, the valid bit (bit 31) in the VM-entry interruption-information field is 1, and the interruption type (bits 10:8) in that field has value 2 (indicating NMI).

**NOTE**

If the "virtual NMIs" VM-execution control is 0, there is no requirement that bit 3 be 0 if the valid bit in the VM-entry interruption-information field is 1 and the interruption type in that field has value 2.

- Pending debug exceptions.
  — Bits 11:4, bit 13, bit 15, and bits 63:17 (bits 31:17 on processors that do not support Intel 64 architecture) must be 0.
  — The following checks are performed if any of the following holds: (1) the interruptibility-state field indicates blocking by STI (bit 0 in that field is 1); (2) the interruptibility-state field indicates blocking by MOV SS (bit 1 in that field is 1); or (3) the activity-state field indicates HLT:
    - Bit 14 (BS) must be 1 if the TF flag (bit 8) in the RFLAGS field is 1 and the BTF flag (bit 1) in the IA32_DEBUGCTL field is 0.
    - Bit 14 (BS) must be 0 if the TF flag (bit 8) in the RFLAGS field is 0 or the BTF flag (bit 1) in the IA32_DEBUGCTL field is 1.
  — The following checks are performed if bit 16 (RTM) is 1:
    - Bits 11:0, bits 15:13, and bits 63:17 (bits 31:17 on processors that do not support Intel 64 architecture) must be 0; bit 12 must be 1.
    - The interruptibility-state field must not indicate blocking by MOV SS (bit 1 in that field must be 0).
- VMCS link pointer. The following checks apply if the field contains a value other than FFFFFFFF_FFFFFFFFH:
  — Bits 11:0 must be 0.
  — Bits beyond the processor’s physical-address width must be 0.\(^1,2\)
  — The 4 bytes located in memory referenced by the value of the field (as a physical address) must satisfy the following:
    - Bits 30:0 must contain the processor’s VMCS revision identifier (see Section 24.2).\(^3\)
    - Bit 31 must contain the setting of the "VMCS shadowing" VM-execution control.\(^4\) This implies that the referenced VMCS is a shadow VMCS (see Section 24.10) if and only if the "VMCS shadowing" VM-execution control is 1.

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1. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
2. If IA32_VMX_BASIC[48] is read as 1, this field must not set any bits in the range 63:32; see Appendix A.1.
3. Earlier versions of this manual specified that the VMCS revision identifier was a 32-bit field. For all processors produced prior to this change, bit 31 of the VMCS revision identifier was 0.
4. "VMCS shadowing" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "VMCS shadowing" VM-execution control were 0. See Section 24.6.2.
— If the processor is not in SMM or the “entry to SMM” VM-entry control is 1, the field must not contain the current VMCS pointer.
— If the processor is in SMM and the “entry to SMM” VM-entry control is 0, the field must differ from the executive-VMCS pointer.

### 26.3.1.6 Checks on Guest Page-Directory-Pointer-Table Entries

If CR0.PG =1, CR4.PAE = 1, and IA32_EFER.LMA = 0, the logical processor also uses PAE paging (see Section 4.4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A). When PAE paging is in use, the physical address in CR3 references a table of page-directory-pointer-table entries (PDPTEs). A MOV to CR3 when PAE paging is in use checks the validity of the PDPTEs.

A VM entry is to a guest that uses PAE paging if (1) bit 31 (corresponding to CR0.PG) is set in the CR0 field in the guest-state area; (2) bit 5 (corresponding to CR4.PAE) is set in the CR4 field; and (3) the “IA-32e mode guest” VM-entry control is 0. Such a VM entry checks the validity of the PDPTEs:

- If the “enable EPT” VM-execution control is 0, VM entry checks the validity of the PDPTEs referenced by the CR3 field in the guest-state area if either (1) PAE paging was not in use before the VM entry; or (2) the value of CR3 is changing as a result of the VM entry. VM entry may check their validity even if neither (1) nor (2) hold.
- If the “enable EPT” VM-execution control is 1, VM entry checks the validity of the PDPTE fields in the guest-state area (see Section 24.4.2).

A VM entry to a guest that does not use PAE paging does not check the validity of any PDPTEs.

A VM entry that checks the validity of the PDPTEs uses the same checks that are used when CR3 is loaded with MOV to CR3 when PAE paging is in use. If MOV to CR3 would cause a general-protection exception due to the PDPTEs that would be loaded (e.g., because a reserved bit is set), the VM entry fails.

### 26.3.2 Loading Guest State

Processor state is updated on VM entries in the following ways:

- Some state is loaded from the guest-state area.
- Some state is determined by VM-entry controls.
- The page-directory pointers are loaded based on the values of certain control registers.

This loading may be performed in any order and in parallel with the checking of VMCS contents (see Section 26.3.1).

The loading of guest state is detailed in Section 26.3.2.1 to Section 26.3.2.4. These sections reference VMCS fields that correspond to processor state. Unless otherwise stated, these references are to fields in the guest-state area.

In addition to the state loading described in this section, VM entries may load MSRs from the VM-entry MSR-load area (see Section 26.4). This loading occurs only after the state loading described in this section and the checking of VMCS contents described in Section 26.3.1.

#### 26.3.2.1 Loading Guest Control Registers, Debug Registers, and MSRs

The following items describe how guest control registers, debug registers, and MSRs are loaded on VM entry:

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1. On processors that support Intel 64 architecture, the physical-address extension may support more than 36 physical-address bits. Software can determine the number physical-address bits supported by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
2. “Enable EPT” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “enable EPT” VM-execution control were 0. See Section 24.6.2.
3. This implies that (1) bits 11:9 in each PDPTE are ignored; and (2) if bit 0 (present) is clear in one of the PDPTEs, bits 63:1 of that PDPTE are ignored.
• CR0 is loaded from the CR0 field with the exception of the following bits, which are never modified on VM entry: ET (bit 4); reserved bits 15:6, 17, and 28:19; NW (bit 29) and CD (bit 30). The values of these bits in the CR0 field are ignored.

• CR3 and CR4 are loaded from the CR3 field and the CR4 field, respectively.

• If the "load debug controls" VM-entry control is 1, DR7 is loaded from the DR7 field with the exception that bit 12 and bits 15:14 are always 0 and bit 10 is always 1. The values of these bits in the DR7 field are ignored.

The first processors to support the virtual-machine extensions supported only the 1-setting of the "load debug controls" VM-entry control and thus always loaded DR7 from the DR7 field.

• The following describes how some MSRs are loaded using fields in the guest-state area:
  — If the "load debug controls" VM-entry control is 1, the IA32_DEBUGCTL MSR is loaded from the IA32_DEBUGCTL field. The first processors to support the virtual-machine extensions supported only the 1-setting of this control and thus always loaded the IA32_DEBUGCTL MSR from the IA32_DEBUGCTL field.
  — The IA32_SYSENTER_CS MSR is loaded from the IA32_SYSENTER_CS field. Since this field has only 32 bits, bits 63:32 of the MSR are cleared to 0.
  — The IA32_SYSENTER_ESP and IA32_SYSENTER_EIP MSRs are loaded from the IA32_SYSENTER_ESP field and the IA32_SYSENTER_EIP field, respectively. On processors that do not support Intel 64 architecture, these fields have only 32 bits; bits 63:32 of the MSRs are cleared to 0.
  — The following are performed on processors that support Intel 64 architecture:
    • The MSRs FS.base and GS.base are loaded from the base-address fields for FS and GS, respectively (see Section 26.3.2.2).
    • If the "load IA32_EFER" VM-entry control is 0, bits in the IA32_EFER MSR are modified as follows:
      — IA32_EFER.LMA is loaded with the setting of the "IA-32e mode guest" VM-entry control.
      — If CR0 is being loaded so that CR0.PG = 1, IA32_EFER.LME is also loaded with the setting of the "IA-32e mode guest" VM-entry control. Otherwise, IA32_EFER.LME is unmodified.

    See below for the case in which the "load IA32_EFER" VM-entry control is 1
    — If the "load IA32_PERF_GLOBAL_CTRL" VM-entry control is 1, the IA32_PERF_GLOBAL_CTRL MSR is loaded from the IA32_PERF_GLOBAL_CTRL field.
    — If the "load IA32_PAT" VM-entry control is 1, the IA32_PAT MSR is loaded from the IA32_PAT field.
    — If the "load IA32_EFER" VM-entry control is 1, the IA32_EFER MSR is loaded from the IA32_EFER field.

    With the exception of FS.base and GS.base, any of these MSRs is subsequently overwritten if it appears in the VM-entry MSR-load area. See Section 26.4.
  — The SMBASE register is unmodified by all VM entries except those that return from SMM.

26.3.2.2 Loading Guest Segment Registers and Descriptor-Table Registers

For each of CS, SS, DS, ES, FS, GS, TR, and LDTR, fields are loaded from the guest-state area as follows:

• The unusable bit is loaded from the access-rights field. This bit can never be set for TR (see Section 26.3.1.2). If it is set for one of the other registers, the following apply:
  — For each of CS, SS, DS, ES, FS, and GS, uses of the segment cause faults (general-protection exception or stack-fault exception) outside 64-bit mode, just as they would had the segment been loaded using a null selector. This bit does not cause accesses to fault in 64-bit mode.
  — If this bit is set for LDTR, uses of LDTR cause general-protection exceptions in all modes, just as they would had LDTR been loaded using a null selector.

1. Bits 15:6, bit 17, and bit 28:19 of CR0 and CR0.ET are unchanged by executions of MOV to CR0. Bits 15:6, bit 17, and bit 28:19 of CR0 are always 0 and CR0.ET is always 1.

2. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PG must be 1 in VMX operation, VM entry must be loading CR0 so that CR0.PG = 1 unless the "unrestricted guest" VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
If this bit is clear for any of CS, SS, DS, ES, FS, GS, TR, and LDTR, a null selector value does not cause a fault (general-protection exception or stack-fault exception).

- TR. The selector, base, limit, and access-rights fields are loaded.
- CS.
  - The following fields are always loaded: selector, base address, limit, and (from the access-rights field) the L, D, and G bits.
  - For the other fields, the unusable bit of the access-rights field is consulted:
    - If the unusable bit is 0, all of the access-rights field is loaded.
    - If the unusable bit is 1, the remainder of CS access rights are undefined after VM entry.
- SS, DS, ES, FS, GS, and LDTR.
  - The selector fields are loaded.
  - For the other fields, the unusable bit of the corresponding access-rights field is consulted:
    - If the unusable bit is 0, the base-address, limit, and access-rights fields are loaded.
    - If the unusable bit is 1, the base address, the segment limit, and the remainder of the access rights are undefined after VM entry with the following exceptions:
      - Bits 3:0 of the base address for SS are cleared to 0.
      - SS.DPL is always loaded from the SS access-rights field. This will be the current privilege level (CPL) after the VM entry completes.
      - SS.B is always set to 1.
      - The base addresses for FS and GS are loaded from the corresponding fields in the VMCS. On processors that support Intel 64 architecture, the values loaded for base addresses for FS and GS are also manifest in the FS.base and GS.base MSRs.
      - On processors that support Intel 64 architecture, the base address for LDTR is set to an undefined but canonical value.
      - On processors that support Intel 64 architecture, bits 63:32 of the base addresses for SS, DS, and ES are cleared to 0.

GDTR and IDTR are loaded using the base and limit fields.

### 26.3.2.3 Loading Guest RIP, RSP, and RFLAGS

RSP, RIP, and RFLAGS are loaded from the RSP field, the RIP field, and the RFLAGS field, respectively. The following items regard the upper 32 bits of these fields on VM entries that are not to 64-bit mode:

- Bits 63:32 of RSP are undefined outside 64-bit mode. Thus, a logical processor may ignore the contents of bits 63:32 of the RSP field on VM entries that are not to 64-bit mode.
- As noted in Section 26.3.1.4, bits 63:32 of the RIP and RFLAGS fields must be 0 on VM entries that are not to 64-bit mode.

### 26.3.2.4 Loading Page-Directory-Pointer-Table Entries

As noted in Section 26.3.1.6, the logical processor uses PAE paging if bit 5 in CR4 (CR4.PAE) is 1 and IA32_EFER.LMA is 0. A VM entry to a guest that uses PAE paging loads the PDPTEs into internal, non-architectural registers based on the setting of the "enable EPT" VM-execution control:

- If the control is 0, the PDPTEs are loaded from the page-directory-pointer table referenced by the physical address in the value of CR3 being loaded by the VM entry (see Section 26.3.2.1). The values loaded are treated as physical addresses in VMX non-root operation.
- If the control is 1, the PDPTEs are loaded from corresponding fields in the guest-state area (see Section 24.4.2). The values loaded are treated as guest-physical addresses in VMX non-root operation.
26.3.2.5 Updating Non-Register State

Section 28.3 describes how the VMX architecture controls how a logical processor manages information in the TLBs and paging-structure caches. The following items detail how VM entries invalidate cached mappings:

- If the “enable VPID” VM-execution control is 0, the logical processor invalidates linear mappings and combined mappings associated with VPID 0000H (for all PCIDs); combined mappings for VPID 0000H are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP).
- VM entries are not required to invalidate any guest-physical mappings, nor are they required to invalidate any linear mappings or combined mappings if the “enable VPID” VM-execution control is 1.

If the “virtual-interrupt delivery” VM-execution control is 1, VM entry loads the values of RVI and SVI from the guest interrupt-status field in the VMCS (see Section 24.4.2). After doing so, the logical processor first causes PPR virtualization (Section 29.1.3) and then evaluates pending virtual interrupts (Section 29.2.1).

If a virtual interrupt is recognized, it may be delivered in VMX non-root operation immediately after VM entry (including any specified event injection) completes; see Section 26.6.5. See Section 29.2.2 for details regarding the delivery of virtual interrupts.

26.3.3 Clearing Address-Range Monitoring

The Intel 64 and IA-32 architectures allow software to monitor a specified address range using the MONITOR and MWAIT instructions. See Section 8.10.4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A. VM entries clear any address-range monitoring that may be in effect.

26.4 LOADING MSRS

VM entries may load MSRs from the VM-entry MSR-load area (see Section 24.8.2). Specifically each entry in that area (up to the number specified in the VM-entry MSR-load count) is processed in order by loading the MSR indexed by bits 31:0 with the contents of bits 127:64 as they would be written by WRMSR.¹

Processing of an entry fails in any of the following cases:

- The value of bits 31:0 is either C0000100H (the IA32_FS_BASE MSR) or C0000101 (the IA32_GS_BASE MSR).
- The value of bits 31:8 is 000008H, meaning that the indexed MSR is one that allows access to an APIC register when the local APIC is in x2APIC mode.
- The value of bits 31:0 indicates an MSR that can be written only in system-management mode (SMM) and the VM entry did not commence in SMM. (IA32_SMM_MONITOR_CTL is an MSR that can be written only in SMM.)
- The value of bits 31:0 indicates an MSR that cannot be loaded on VM entries for model-specific reasons. A processor may prevent loading of certain MSRs even if they can normally be written by WRMSR. Such model-specific behavior is documented in Chapter 35.
- Bits 63:32 are not all 0.
- An attempt to write bits 127:64 to the MSR indexed by bits 31:0 of the entry would cause a general-protection exception if executed via WRMSR with CPL = 0.²

The VM entry fails if processing fails for any entry. The logical processor responds to such failures by loading state from the host-state area, as it would for a VM exit. See Section 26.7.

If any MSR is being loaded in such a way that would architecturally require a TLB flush, the TLBs are updated so that, after VM entry, the logical processor will not use any translations that were cached before the transition.

¹. Because attempts to modify the value of IA32_EFER.LMA by WRMSR are ignored, attempts to modify it using the VM-entry MSR-load area are also ignored.

². If CR0.PG = 1, WRMSR to the IA32_EFER MSR causes a general-protection exception if it would modify the LME bit. If VM entry has established CR0.PG = 1, the IA32_EFER MSR should not be included in the VM-entry MSR-load area for the purpose of modifying the LME bit.
26.5 EVENT INJECTION

If the valid bit in the VM-entry interruption-information field (see Section 24.8.3) is 1, VM entry causes an event to be delivered (or made pending) after all components of guest state have been loaded (including MSRs) and after the VM-execution control fields have been established.

- If the interruption type in the field is 0 (external interrupt), 2 (non-maskable interrupt), 3 (hardware exception), 4 (software interrupt), 5 (privileged software exception), or 6 (software exception), the event is delivered as described in Section 26.5.1.
- If the interruption type in the field is 7 (other event) and the vector field is 0, an MTF VM exit is pending after VM entry. See Section 26.5.2.

26.5.1 Vectored-Event Injection

VM entry delivers an injected vectored event within the guest context established by VM entry. This means that delivery occurs after all components of guest state have been loaded (including MSRs) and after the VM-execution control fields have been established.¹ The event is delivered using the vector in that field to select a descriptor in the IDT. Since event injection occurs after loading IDTR from the guest-state area, this is the guest IDT.

Section 26.5.1.1 provides details of vectored-event injection. In general, the event is delivered exactly as if it had been generated normally.

If event delivery encounters a nested exception (for example, a general-protection exception because the vector indicates a descriptor beyond the IDT limit), the exception bitmap is consulted using the vector of that exception:

- If the bit for the nested exception is 0, the nested exception is delivered normally. If the nested exception is benign, it is delivered through the IDT. If it is contributory or a page fault, a double fault may be generated, depending on the nature of the event whose delivery encountered the nested exception. See Chapter 6, “Interrupt 8—Double Fault Exception (#DF)” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.²
- If the bit for the nested exception is 1, a VM exit occurs. Section 26.5.1.2 details cases in which event injection causes a VM exit.

26.5.1.1 Details of Vectored-Event Injection

The event-injection process is controlled by the contents of the VM-entry interruption information field (format given in Table 24-13), the VM-entry exception error-code field, and the VM-entry instruction-length field. The following items provide details of the process:

- The value pushed on the stack for RFLAGS is generally that which was loaded from the guest-state area. The value pushed for the RF flag is not modified based on the type of event being delivered. However, the pushed value of RFLAGS may be modified if a software interrupt is being injected into a guest that will be in virtual-8086 mode (see below). After RFLAGS is pushed on the stack, the value in the RFLAGS register is modified as is done normally when delivering an event through the IDT.
- The instruction pointer that is pushed on the stack depends on the type of event and whether nested exceptions occur during its delivery. The term current guest RIP refers to the value to be loaded from the guest-state area. The value pushed is determined as follows:³
  - If VM entry successfully injects (with no nested exception) an event with interruption type external interrupt, NMI, or hardware exception, the current guest RIP is pushed on the stack.

¹ This does not imply that injection of an exception or interrupt will cause a VM exit due to the settings of VM-execution control fields (such as the exception bitmap) that would cause a VM exit if the event had occurred in VMX non-root operation. In contrast, a nested exception encountered during event delivery may cause a VM exit; see Section 26.5.1.1.
² Hardware exceptions with the following unused vectors are considered benign: 15 and 21–31. A hardware exception with vector 20 is considered benign unless the processor supports the 1-setting of the “EPT-violation #VE” VM-execution control; in that case, it has the same severity as page faults.
³ While these items refer to RIP, the width of the value pushed (16 bits, 32 bits, or 64 bits) is determined normally.
— If VM entry successfully injects (with no nested exception) an event with interruption type software interrupt, privileged software exception, or software exception, the current guest RIP is incremented by the VM-entry instruction length before being pushed on the stack.

— If VM entry encounters an exception while injecting an event and that exception does not cause a VM exit, the current guest RIP is pushed on the stack regardless of event type or VM-entry instruction length. If the encountered exception does cause a VM exit that saves RIP, the saved RIP is current guest RIP.

• If the deliver-error-code bit (bit 11) is set in the VM-entry interruption-information field, the contents of the VM-entry exception error-code field is pushed on the stack as an error code would be pushed during delivery of an exception.

• DR6, DR7, and the IA32_DEBUGCTL MSR are not modified by event injection, even if the event has vector 1 (normal deliveries of debug exceptions, which have vector 1, do update these registers).

• If VM entry is injecting a software interrupt and the guest will be in virtual-8086 mode (RFLAGS.VM = 1), no general-protection exception can occur due to RFLAGS.IOPL < 3. A VM monitor should check RFLAGS.IOPL before injecting such an event and, if desired, inject a general-protection exception instead of a software interrupt.

• If VM entry is injecting a software interrupt and the guest will be in virtual-8086 mode with virtual-8086 mode extensions (RFLAGS.VM = CR4.VME = 1), event delivery is subject to VME-based interrupt redirection based on the software interrupt redirection bitmap in the task-state segment (TSS) as follows:
  — If bit n in the bitmap is clear (where n is the number of the software interrupt), the interrupt is directed to an 8086 program interrupt handler: the processor uses a 16-bit interrupt-vector table (IVT) located at linear address zero. If the value of RFLAGS.IOPL is less than 3, the following modifications are made to the value of RFLAGS that is pushed on the stack: IOPL is set to 3, and IF is set to the value of VIF.
  — If bit n in the bitmap is set (where n is the number of the software interrupt), the interrupt is directed to a protected-mode interrupt handler. (In other words, the injection is treated as described in the next item.) In this case, the software interrupt does not invoke such a handler if RFLAGS.IOPL < 3 (a general-protection exception occurs instead). However, as noted above, RFLAGS.IOPL cannot cause an injected software interrupt to cause such an exception. Thus, in this case, the injection invokes a protected-mode interrupt handler independent of the value of RFLAGS.IOPL.

Injection of events of other types are not subject to this redirection.

• If VM entry is injecting a software interrupt (not redirected as described above) or software exception, privilege checking is performed on the IDT descriptor being accessed as would be the case for executions of INT n, INT3, or INTO (the descriptor’s DPL cannot be less than CPL). There is no checking of RFLAGS.IOPL, even if the guest will be in virtual-8086 mode. Failure of this check may lead to a nested exception. Injection of an event with interruption type external interrupt, NMI, hardware exception, and privileged software exception, or with interruption type software interrupt and being redirected as described above, do not perform these checks.

• If VM entry is injecting a non-maskable interrupt (NMI) and the “virtual NMI”s” VM-execution control is 1, virtual-NMI blocking is in effect after VM entry.

The transition causes a last-branch record to be logged if the LBR bit is set in the IA32_DEBUGCTL MSR. This is true even for events such as debug exceptions, which normally clear the LBR bit before delivery.

The last-exception record MSRs (LERs) may be updated based on the setting of the LBR bit in the IA32_DEBUGCTL MSR. Events such as debug exceptions, which normally clear the LBR bit before they are delivered, and therefore do not normally update the LERs, may do so as part of VM-entry event injection.

• If injection of an event encounters a nested exception that does not itself cause a VM exit, the value of the EXT bit (bit 0) in any error code pushed on the stack is determined as follows:
  — If event being injected has interruption type external interrupt, NMI, hardware exception, or privileged software exception and encounters a nested exception (but does not produce a double fault), the error code for the first such exception encountered sets the EXT bit.
  — If event being injected is a software interrupt or an software exception and encounters a nested exception (but does not produce a double fault), the error code for the first such exception encountered clears the EXT bit.
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— If event delivery encounters a nested exception and delivery of that exception encounters another exception (but does not produce a double fault), the error code for that exception sets the EXT bit. If a double fault is produced, the error code for the double fault is 0000H (the EXT bit is clear).

26.5.1.2 VM Exits During Event Injection

An event being injected never causes a VM exit directly regardless of the settings of the VM-execution controls. For example, setting the "NMI exiting" VM-execution control to 1 does not cause a VM exit due to injection of an NMI.

However, the event-delivery process may lead to a VM exit:

• If the vector in the VM-entry interruption-information field identifies a task gate in the IDT, the attempted task switch may cause a VM exit just as it would had the injected event occurred during normal execution in VMX non-root operation (see Section 25.4.2).
• If event delivery encounters a nested exception, a VM exit may occur depending on the contents of the exception bitmap (see Section 25.2).
• If event delivery generates a double-fault exception (due to a nested exception); the logical processor encounters another nested exception while attempting to call the double-fault handler; and that exception does not cause a VM exit due to the exception bitmap; then a VM exit occurs due to triple fault (see Section 25.2).
• If event delivery injects a double-fault exception and encounters a nested exception that does not cause a VM exit due to the exception bitmap, then a VM exit occurs due to triple fault (see Section 25.2).
• If the "virtualize APIC accesses" VM-execution control is 1 and event delivery generates an access to the APIC-access page, that access is treated as described in Section 29.4 and may cause a VM exit.1

If the event-delivery process does cause a VM exit, the processor state before the VM exit is determined just as it would be had the injected event occurred during normal execution in VMX non-root operation. If the injected event directly accesses a task gate that cause a VM exit or if the first nested exception encountered causes a VM exit, information about the injected event is saved in the IDT-vectoring information field (see Section 27.2.3).

26.5.1.3 Event Injection for VM Entries to Real-Address Mode

If VM entry is loading CR0.PE with 0, any injected vectored event is delivered as would normally be done in real-address mode.2 Specifically, VM entry uses the vector provided in the VM-entry interruption-information field to select a 4-byte entry from an interrupt-vector table at the linear address in IDTR.base. Further details are provided in Section 15.1.4 in Volume 3A of the IA-32 Intel® Architecture Software Developer’s Manual.

Because bit 11 (deliver error code) in the VM-entry interruption-information field must be 0 if CR0.PE will be 0 after VM entry (see Section 26.2.1.3), vectored events injected with CR0.PE = 0 do not push an error code on the stack. This is consistent with event delivery in real-address mode.

If event delivery encounters a fault (due to a violation of IDTR.limit or of SS.limit), the fault is treated as if it had occurred during event delivery in VMX non-root operation. Such a fault may lead to a VM exit as discussed in Section 26.5.1.2.

26.5.2 Injection of Pending MTF VM Exits

If the interruption type in the VM-entry interruption-information field is 7 (other event) and the vector field is 0, VM entry causes an MTF VM exit to be pending on the instruction boundary following VM entry. This is the case even if the "monitor trap flag" VM-execution control is 0. See Section 25.5.2 for the treatment of pending MTF VM exits.

1. “Virtualize APIC accesses” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the “virtualize APIC accesses” VM-execution control were 0. See Section 24.6.2.
2. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PE must be 1 in VMX operation, VM entry must be loading CR0.PE with 1 unless the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
26.6 SPECIAL FEATURES OF VM ENTRY

This section details a variety of features of VM entry. It uses the following terminology: a VM entry is **vectoring** if the valid bit (bit 31) of the VM-entry interruption information field is 1 and the interruption type in the field is 0 (external interrupt), 2 (non-maskable interrupt); 3 (hardware exception), 4 (software interrupt), 5 (privileged software exception), or 6 (software exception).

26.6.1 Interruptibility State

The interruptibility-state field in the guest-state area (see Table 24-3) contains bits that control blocking by STI, blocking by MOV SS, and blocking by NMI. This field impacts event blocking after VM entry as follows:

- If the VM entry is vectoring, there is no blocking by STI or by MOV SS following the VM entry, regardless of the contents of the interruptibility-state field.
- If the VM entry is not vectoring, the following apply:
  - Events are blocked by STI if and only if bit 0 in the interruptibility-state field is 1. This blocking is cleared after the guest executes one instruction or incurs an exception (including a debug exception made pending by VM entry; see Section 26.6.3).
  - Events are blocked by MOV SS if and only if bit 1 in the interruptibility-state field is 1. This may affect the treatment of pending debug exceptions; see Section 26.6.3. This blocking is cleared after the guest executes one instruction or incurs an exception (including a debug exception made pending by VM entry).
- The blocking of non-maskable interrupts (NMIs) is determined as follows:
  - If the “virtual NMIs” VM-execution control is 0, NMIs are blocked if and only if bit 3 (blocking by NMI) in the interruptibility-state field is 1. If the “NMI exiting” VM-execution control is 0, execution of the IRET instruction removes this blocking (even if the instruction generates a fault). If the “NMI exiting” control is 1, IRET does not affect this blocking.
  - The following items describe the use of bit 3 (blocking by NMI) in the interruptibility-state field if the “virtual NMIs” VM-execution control is 1:
    - The bit’s value does not affect the blocking of NMIs after VM entry. NMIs are not blocked in VMX non-root operation (except for ordinary blocking for other reasons, such as by the MOV SS instruction, the wait-for-SIPI state, etc.)
    - The bit’s value determines whether there is virtual-NMI blocking after VM entry. If the bit is 1, virtual-NMI blocking is in effect after VM entry. If the bit is 0, there is no virtual-NMI blocking after VM entry unless the VM entry is injecting an NMI (see Section 26.5.1.1). Execution of IRET removes virtual-NMI blocking (even if the instruction generates a fault).

If the “NMI exiting” VM-execution control is 0, the “virtual NMIs” control must be 0; see Section 26.2.1.1.

- Blocking of system-management interrupts (SMIs) is determined as follows:
  - If the VM entry was not executed in system-management mode (SMM), SMI blocking is unchanged by VM entry.
  - If the VM entry was executed in SMM, SMIs are blocked after VM entry if and only if the bit 2 in the interruptibility-state field is 1.

26.6.2 Activity State

The activity-state field in the guest-state area controls whether, after VM entry, the logical processor is active or in one of the inactive states identified in Section 24.4.2. The use of this field is determined as follows:

- If the VM entry is vectoring, the logical processor is in the active state after VM entry. While the consistency checks described in Section 26.3.1.5 on the activity-state field do apply in this case, the contents of the activity-state field do not determine the activity state after VM entry.
- If the VM entry is not vectoring, the logical processor ends VM entry in the activity state specified in the guest-state area. If VM entry ends with the logical processor in an inactive activity state, the VM entry generates any special bus cycle that is normally generated when that activity state is entered from the active state. If
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VM entry would end with the logical processor in the shutdown state and the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs. The error code used is 0000H, indicating “legacy shutdown.” See Intel® Trusted Execution Technology Preliminary Architecture Specification.

• Some activity states unconditionally block certain events. The following blocking is in effect after any VM entry that puts the processor in the indicated state:
  — The active state blocks start-up IPIs (SIPIs). SIPIs that arrive while a logical processor is in the active state and in VMX non-root operation are discarded and do not cause VM exits.
  — The HLT state blocks start-up IPIs (SIPIs). SIPIs that arrive while a logical processor is in the HLT state and in VMX non-root operation are discarded and do not cause VM exits.
  — The shutdown state blocks external interrupts and SIPIs. External interrupts that arrive while a logical processor is in the shutdown state and in VMX non-root operation do not cause VM exits even if the “external-interrupt exiting” VM-execution control is 1. SIPIs that arrive while a logical processor is in the shutdown state and in VMX non-root operation are discarded and do not cause VM exits.
  — The wait-for-SIPI state blocks external interrupts, non-maskable interrupts (NMIs), INIT signals, and system-management interrupts (SMIs). Such events do not cause VM exits if they arrive while a logical processor is in the wait-for-SIPI state and in VMX non-root operation do not cause VM exits regardless of the settings of the pin-based VM-execution controls.

26.6.3 Delivery of Pending Debug Exceptions after VM Entry

The pending debug exceptions field in the guest-state area indicates whether there are debug exceptions that have not yet been delivered (see Section 24.4.2). This section describes how these are treated on VM entry.

There are no pending debug exceptions after VM entry if any of the following are true:

• The VM entry is vectoring with one of the following interruption types: external interrupt, non-maskable interrupt (NMI), hardware exception, or privileged software exception.
• The interruptibility-state field does not indicate blocking by MOV SS and the VM entry is vectoring with either of the following interruption type: software interrupt or software exception.
• The VM entry is not vectoring and the activity-state field indicates either shutdown or wait-for-SIPI.

If none of the above hold, the pending debug exceptions field specifies the debug exceptions that are pending for the guest. There are valid pending debug exceptions if either the BS bit (bit 14) or the enable-breakpoint bit (bit 12) is 1. If there are valid pending debug exceptions, they are handled as follows:

• If the VM entry is not vectoring, the pending debug exceptions are treated as they would had they been encountered normally in guest execution:
  — If the logical processor is not blocking such exceptions (the interruptibility-state field indicates no blocking by MOV SS), a debug exception is delivered after VM entry (see below).
  — If the logical processor is blocking such exceptions (due to blocking by MOV SS), the pending debug exceptions are held pending or lost as would normally be the case.
• If the VM entry is vectoring (with interruption type software interrupt or software exception and with blocking by MOV SS), the following items apply:
  — For injection of a software interrupt or of a software exception with vector 3 (#BP) or vector 4 (#OF), the pending debug exceptions are treated as they would had they been encountered normally in guest execution if the corresponding instruction (INT3 or INTO) were executed after a MOV SS that encountered a debug trap.
  — For injection of a software exception with a vector other than 3 and 4, the pending debug exceptions may be lost or they may be delivered after injection (see below).

If there are no valid pending debug exceptions (as defined above), no pending debug exceptions are delivered after VM entry.

1. A logical processor is in SMX operation if GETSEC[SENTER] has not been executed since the last execution of GETSEC[SEXIT]. See Chapter 6, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
If a pending debug exception is delivered after VM entry, it has the priority of “traps on the previous instruction” (see Section 6.9 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A). Thus, INIT signals and system-management interrupts (SMIs) take priority of such an exception, as do VM exits induced by the TPR threshold (see Section 26.6.7) and pending MTF VM exits (see Section 26.6.8. The exception takes priority over any pending non-maskable interrupt (NMI) or external interrupt and also over VM exits due to the 1-settings of the “interrupt-window exiting” and “NMI-window exiting” VM-execution controls.

A pending debug exception delivered after VM entry causes a VM exit if the bit 1 (#DB) is 1 in the exception bitmap. If it does not cause a VM exit, it updates DR6 normally.

26.6.4 VMX-Preemption Timer

If the "activate VMX-preemption timer" VM-execution control is 1, VM entry starts the VMX-preemption timer with the unsigned value in the VMX-preemption timer-value field.

It is possible for the VMX-preemption timer to expire during VM entry (e.g., if the value in the VMX-preemption timer-value field is zero). If this happens (and if the VM entry was not to the wait-for-SIPI state), a VM exit occurs with its normal priority after any event injection and before execution of any instruction following VM entry. For example, any pending debug exceptions established by VMentry (see Section 26.6.3) take priority over a timer-induced VM exit. (The timer-induced VM exit will occur after delivery of the debug exception, unless that exception or its delivery causes a different VM exit.)

See Section 25.5.1 for details of the operation of the VMX-preemption timer in VMX non-root operation, including the blocking and priority of the VM exits that it causes.

26.6.5 Interrupt-Window Exiting and Virtual-Interrupt Delivery

If "interrupt-window exiting" VM-execution control is 1, an open interrupt window may cause a VM exit immediately after VM entry (see Section 25.2 for details). If the "interrupt-window exiting" VM-execution control is 0 but the "virtual-interrupt delivery" VM-execution control is 1, a virtual interrupt may be delivered immediately after VM entry (see Section 26.3.2.5 and Section 29.2.1).

The following items detail the treatment of these events:

• These events occur after any event injection specified for VM entry.
• Non-maskable interrupts (NMIs) and higher priority events take priority over these events. These events take priority over external interrupts and lower priority events.
• These events wake the logical processor if it just entered the HLT state because of a VM entry (see Section 26.6.2). They do not occur if the logical processor just entered the shutdown state or the wait-for-SIPI state.

26.6.6 NMI-Window Exiting

The "NMI-window exiting" VM-execution control may cause a VM exit to occur immediately after VM entry (see Section 25.2 for details).

The following items detail the treatment of these VM exits:

• These VM exits follow event injection if such injection is specified for VM entry.
• Debug-trap exceptions (see Section 26.6.3) and higher priority events take priority over VM exits caused by this control. VM exits caused by this control take priority over non-maskable interrupts (NMIs) and lower priority events.
• VM exits caused by this control wake the logical processor if it just entered either the HLT state or the shutdown state because of a VM entry (see Section 26.6.2). They do not occur if the logical processor just entered the wait-for-SIPI state.
26.6.7 VM Exits Induced by the TPR Threshold

If the “use TPR shadow” and “virtualize APIC accesses” VM-execution controls are both 1 and the “virtual-interrupt delivery” VM-execution control is 0, a VM exit occurs immediately after VM entry if the value of bits 3:0 of the TPR threshold VM-execution control field is greater than the value of bits 7:4 of VTPR (see Section 29.1.1).

The following items detail the treatment of these VM exits:

- The VM exits are not blocked if RFLAGS.IF = 0 or by the setting of bits in the interruptibility-state field in guest-state area.
- The VM exits follow event injection if such injection is specified for VM entry.
- VM exits caused by this control take priority over system-management interrupts (SMIs), INIT signals, and lower priority events. They thus have priority over the VM exits described in Section 26.6.5, Section 26.6.6, and Section 26.6.8, as well as any interrupts or debug exceptions that may be pending at the time of VM entry.
- These VM exits wake the logical processor if it just entered the HLT state as part of a VM entry (see Section 26.6.2). They do not occur if the logical processor just entered the shutdown state or the wait-for-SIPI state.
- If such a VM exit is suppressed because the processor just entered the shutdown state, it occurs after the delivery of any event that cause the logical processor to leave the shutdown state while remaining in VMX non-root operation (e.g., due to an NMI that occurs while the “NMI-exiting” VM-execution control is 0).
- The basic exit reason is “TPR below threshold.”

26.6.8 Pending MTF VM Exits

As noted in Section 26.5.2, VM entry may cause an MTF VM exit to be pending immediately after VM entry. The following items detail the treatment of these VM exits:

- System-management interrupts (SMIs), INIT signals, and higher priority events take priority over these VM exits. These VM exits take priority over debug-trap exceptions and lower priority events.
- These VM exits wake the logical processor if it just entered the HLT state because of a VM entry (see Section 26.6.2). They do not occur if the logical processor just entered the shutdown state or the wait-for-SIPI state.

26.6.9 VM Entries and Advanced Debugging Features

VM entries are not logged with last-branch records, do not produce branch-trace messages, and do not update the branch-trace store.

26.7 VM-ENTRY FAILURES DURING OR AFTER LOADING GUEST STATE

VM-entry failures due to the checks identified in Section 26.3.1 and failures during the MSR loading identified in Section 26.4 are treated differently from those that occur earlier in VM entry. In these cases, the following steps take place:

1. Information about the VM-entry failure is recorded in the VM-exit information fields:
   - Exit reason.
     - Bits 15:0 of this field contain the basic exit reason. It is loaded with a number indicating the general cause of the VM-entry failure. The following numbers are used:
       33. VM-entry failure due to invalid guest state. A VM entry failed one of the checks identified in Section 26.3.1.
       34. VM-entry failure due to MSR loading. A VM entry failed in an attempt to load MSRs (see Section 26.4).

1. “Virtualize APIC accesses” and “virtual-interrupt delivery” are secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if these controls were 0. See Section 24.6.2.
41. VM-entry failure due to machine-check event. A machine-check event occurred during VM entry (see Section 26.8).

- Bit 31 is set to 1 to indicate a VM-entry failure.
- The remainder of the field (bits 30:16) is cleared.

- Exit qualification. This field is set based on the exit reason.
  - VM-entry failure due to invalid guest state. In most cases, the exit qualification is cleared to 0. The following non-zero values are used in the cases indicated:
    1. Not used.
    2. Failure was due to a problem loading the PDPTEs (see Section 26.3.1.6).
    3. Failure was due to an attempt to inject a non-maskable interrupt (NMI) into a guest that is blocking events through the STI blocking bit in the interruptibility-state field. Such failures are implementation-specific (see Section 26.3.1.5).
    4. Failure was due to an invalid VMCS link pointer (see Section 26.3.1.5).
  - VM-entry checks on guest-state fields may be performed in any order. Thus, an indication by exit qualification of one cause does not imply that there are not also other errors. Different processors may give different exit qualifications for the same VMCS.
  - VM-entry failure due to MSR loading. The exit qualification is loaded to indicate which entry in the VM-entry MSR-load area caused the problem (1 for the first entry, 2 for the second, etc.).

- All other VM-exit information fields are unmodified.

2. Processor state is loaded as would be done on a VM exit (see Section 27.5). If this results in \([\text{CR4.PAE} \& \text{CR0.PG} \& \sim \text{IA32_EFER.LMA}] = 1\), page-directory-pointer-table entries (PDPTEs) may be checked and loaded (see Section 27.5.4).

3. The state of blocking by NMI is what it was before VM entry.

4. MSRs are loaded as specified in the VM-exit MSR-load area (see Section 27.6).

Although this process resembles that of a VM exit, many steps taken during a VM exit do not occur for these VM-entry failures:

- Most VM-exit information fields are not updated (see step 1 above).
- The valid bit in the VM-entry interruption-information field is not cleared.
- The guest-state area is not modified.
- No MSRs are saved into the VM-exit MSR-store area.

### 26.8 MACHINE-CHECK EVENTS DURING VM ENTRY

If a machine-check event occurs during a VM entry, one of the following occurs:

- The machine-check event is handled as if it occurred before the VM entry:
  - If \(\text{CR4.MCE} = 0\), operation of the logical processor depends on whether the logical processor is in SMX operation:
    - If the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs. The error code used is 000CH, indicating "unrecoverable machine-check condition."
    - If the logical processor is outside SMX operation, it goes to the shutdown state.
  - If \(\text{CR4.MCE} = 1\), a machine-check exception (#MC) is delivered through the IDT.

1. A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B*. 

— If the VM entry ends with CR4.MCE = 0, operation of the logical processor depends on whether the logical processor is in SMX operation:
  • If the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs with error code 000CH (unrecoverable machine-check condition).
  • If the logical processor is outside SMX operation, it goes to the shutdown state.
— If the VM entry ends with CR4.MCE = 1, a machine-check exception (#MC) is generated:
  • If bit 18 (#MC) of the exception bitmap is 0, the exception is delivered through the guest IDT.
  • If bit 18 of the exception bitmap is 1, the exception causes a VM exit.
  • A VM-entry failure occurs as described in Section 26.7. The basic exit reason is 41, for “VM-entry failure due to machine-check event.”

The first option is not used if the machine-check event occurs after any guest state has been loaded. The second option is used only if VM entry is able to load all guest state.
VM exits occur in response to certain instructions and events in VMX non-root operation as detailed in Section 25.1 through Section 25.2. VM exits perform the following operations:

1. Information about the cause of the VM exit is recorded in the VM-exit information fields and VM-entry control fields are modified as described in Section 27.2.
2. Processor state is saved in the guest-state area (Section 27.3).
3. MSRs may be saved in the VM-exit MSR-store area (Section 27.4). This step is not performed for SMM VM exits that activate the dual-monitor treatment of SMIs and SMM.
4. The following may be performed in parallel and in any order (Section 27.5):
   - Processor state is loaded based in part on the host-state area and some VM-exit controls. This step is not performed for SMM VM exits that activate the dual-monitor treatment of SMIs and SMM. See Section 34.15.6 for information on how processor state is loaded by such VM exits.
   - Address-range monitoring is cleared.
5. MSRs may be loaded from the VM-exit MSR-load area (Section 27.6). This step is not performed for SMM VM exits that activate the dual-monitor treatment of SMIs and SMM.

VM exits are not logged with last-branch records, do not produce branch-trace messages, and do not update the branch-trace store.

Section 27.1 clarifies the nature of the architectural state before a VM exit begins. The steps described above are detailed in Section 27.2 through Section 27.6.

Section 34.15 describes the dual-monitor treatment of system-management interrupts (SMIs) and system-management mode (SMM). Under this treatment, ordinary transitions to SMM are replaced by VM exits to a separate SMM monitor. Called SMM VM exits, these are caused by the arrival of an SMI or the execution of VMCALL in VMX root operation. SMM VM exits differ from other VM exits in ways that are detailed in Section 34.15.2.

### 27.1 ARCHITECTURAL STATE BEFORE A VM EXIT

This section describes the architectural state that exists before a VM exit, especially for VM exits caused by events that would normally be delivered through the IDT. Note the following:

- An exception causes a VM exit **directly** if the bit corresponding to that exception is set in the exception bitmap. A non-maskable interrupt (NMI) causes a VM exit directly if the "NMI exiting" VM-execution control is 1. An external interrupt causes a VM exit directly if the "external-interrupt exiting" VM-execution control is 1. A start-up IPI (SIPi) that arrives while a logical processor is in the wait-for-SIPI activity state causes a VM exit directly. INIT signals that arrive while the processor is not in the wait-for-SIPI activity state cause a VM exit directly.
- An exception, NMI, external interrupt, or software interrupt causes a VM exit **indirectly** if it does not do so directly but delivery of the event causes a nested exception, double fault, task switch, APIC access (see Section 27.4), EPT violation, EPT misconfiguration, or page-modification log-full event that causes a VM exit.
- An event **results** in a VM exit if it causes a VM exit (directly or indirectly).

The following bullets detail when architectural state is and is not updated in response to VM exits:

- If an event causes a VM exit directly, it does not update architectural state as it would have if it had it not caused the VM exit:
  - A debug exception does not update DR6, DR7.GD, or IA32_DEBUGCTL.LBR. (Information about the nature of the debug exception is saved in the exit qualification field.)
  - A page fault does not update CR2. (The linear address causing the page fault is saved in the exit-qualification field.)
  - An NMI causes subsequent NMIIs to be blocked, but only after the VM exit completes.
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- An external interrupt does not acknowledge the interrupt controller and the interrupt remains pending, unless the “acknowledge interrupt on exit” VM-exit control is 1. In such a case, the interrupt controller is acknowledged and the interrupt is no longer pending.

- The flags L0 – L3 in DR7 (bit 0, bit 2, bit 4, and bit 6) are not cleared when a task switch causes a VM exit.

- If a task switch causes a VM exit, none of the following are modified by the task switch: old task-state segment (TSS); new TSS; old TSS descriptor; new TSS descriptor; RFLAGS.NT1; or the TR register.

- No last-exception record is made if the event that would do so directly causes a VM exit.

- If a machine-check exception causes a VM exit directly, this does not prevent machine-check MSRs from being updated. These are updated by the machine-check event itself and not the resulting machine-check exception.

- If the logical processor is in an inactive state (see Section 24.4.2) and not executing instructions, some events may be blocked but others may return the logical processor to the active state. Unblocked events may cause VM exits. If an unblocked event causes a VM exit directly, a return to the active state occurs only after the VM exit completes. The VM exit generates any special bus cycle that is normally generated when the active state is entered from that activity state.

MTF VM exits (see Section 25.5.2 and Section 26.6.8) are not blocked in the HLT activity state. If an MTF VM exit occurs in the HLT activity state, the logical processor returns to the active state only after the VM exit completes. MTF VM exits are blocked the shutdown state and the wait-for-SIPI state.

- If an event causes a VM exit indirectly, the event does update architectural state:
  - A debug exception updates DR6, DR7, and the IA32_DEBUGCTL MSR. No debug exceptions are considered pending.
  - A page fault updates CR2.
  - An NMI causes subsequent NMIs to be blocked before the VM exit commences.
  - An external interrupt acknowledges the interrupt controller and the interrupt is no longer pending.
  - If the logical processor had been in an inactive state, it enters the active state and, before the VM exit commences, generates any special bus cycle that is normally generated when the active state is entered from that activity state.
  - There is no blocking by STI or by MOV SS when the VM exit commences.
  - Processor state that is normally updated as part of delivery through the IDT (CS, RIP, SS, RSP, RFLAGS) is not modified. However, the incomplete delivery of the event may write to the stack.
  - The treatment of last-exception records is implementation dependent:
    - Some processors make a last-exception record when beginning the delivery of an event through the IDT (before it can encounter a nested exception). Such processors perform this update even if the event encounters a nested exception that causes a VM exit (including the case where nested exceptions lead to a triple fault).
    - Other processors delay making a last-exception record until event delivery has reached some event handler successfully (perhaps after one or more nested exceptions). Such processors do not update the last-exception record if a VM exit or triple fault occurs before an event handler is reached.
  - If the “virtual NMIs” VM-execution control is 1, VM entry injects an NMI, and delivery of the NMI causes a nested exception, double fault, task switch, or APIC access that causes a VM exit, virtual-NMI blocking is in effect before the VM exit commences.

1. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.). In a few places, notation such as EAX is used to refer specifically to lower 32 bits of the indicated register.
2. If a VM exit takes the processor from an inactive state resulting from execution of a specific instruction (HLT or MWAIT), the value saved for RIP by that VM exit will reference the following instruction.
3. An exception is made if the logical processor had been inactive due to execution of MWAIT; in this case, it is considered to have become active before the VM exit.
• If a VM exit results from a fault, EPT violation, EPT misconfiguration, or page-modification log-full event is encountered during execution of IRET and the “NMI exiting” VM-execution control is 0, any blocking by NMI is cleared before the VM exit commences. However, the previous state of blocking by NMI may be recorded in the VM-exit interruption-information field; see Section 27.2.2.

• If a VM exit results from a fault, EPT violation, EPT misconfiguration, or page-modification log-full event is encountered during execution of IRET and the “virtual NMIs” VM-execution control is 1, virtual-NMI blocking is cleared before the VM exit commences. However, the previous state of virtual-NMI blocking may be recorded in the VM-exit interruption-information field; see Section 27.2.2.

• Suppose that a VM exit is caused directly by an x87 FPU Floating-Point Error (#MF) or by any of the following events if the event was unblocked due to (and given priority over) an x87 FPU Floating-Point Error: an INIT signal, an external interrupt, an NMI, an SMI; or a machine-check exception. In these cases, there is no blocking by STI or by MOV SS when the VM exit commences.

• Normally, a last-branch record may be made when an event is delivered through the IDT. However, if such an event results in a VM exit, no last-branch record is made.

• If machine-check exception results in a VM exit, processor state is suspect and may result in suspect state being saved to the guest-state area. A VM monitor should consult the RIPV and EIPV bits in the IA32_MCG_STATUS MSR before resuming a guest that caused a VM exit resulting from a machine-check exception.

• If a VM exit results from a fault, APIC access (see Section 29.4), EPT violation, EPT misconfiguration, or page-modification log-full event is encountered while executing an instruction, data breakpoints due to that instruction may have been recognized and information about them may be saved in the pending debug exceptions field (see Section 27.3.4).

• The following VM exits are considered to happen after an instruction is executed:
  — VM exits resulting from debug traps (single-step, I/O breakpoints, and data breakpoints).
  — VM exits resulting from debug exceptions whose recognition was delayed by blocking by MOV SS.
  — VM exits resulting from some machine-check exceptions.
  — Trap-like VM exits due to execution of MOV to CR8 when the “CR8-load exiting” VM-execution control is 0 and the “use TPR shadow” VM-execution control is 1 (see Section 29.3). (Such VM exits can occur only from 64-bit mode and thus only on processors that support Intel 64 architecture.)
  — Trap-like VM exits due to execution of WRMSR when the “use MSR bitmaps” VM-execution control is 1; the value of ECX is in the range 800H–8FFH; and the bit corresponding to the ECX value in write bitmap for low MSRs is 0; and the “virtualize x2APIC mode” VM-execution control is 1. See Section 29.5.
  — VM exits caused by APIC-write emulation (see Section 29.4.3.2) that result from APIC accesses as part of instruction execution.

For these VM exits, the instruction’s modifications to architectural state complete before the VM exit occurs. Such modifications include those to the logical processor’s interruptibility state (see Table 24-3). If there had been blocking by MOV SS, POP SS, or STI before the instruction executed, such blocking is no longer in effect.

### 27.2 RECORDING VM-EXIT INFORMATION AND UPDATING VM-ENTRY CONTROL FIELDS

VM exits begin by recording information about the nature of and reason for the VM exit in the VM-exit information fields. Section 27.2.1 to Section 27.2.4 detail the use of these fields.

In addition to updating the VM-exit information fields, the valid bit (bit 31) is cleared in the VM-entry interruption-information field. If bit 5 of the IA32_VMX_MISC MSR (index 485H) is read as 1 (see Appendix A.6), the value of IA32_EFER.LMA is stored into the “IA-32e mode guest” VM-entry control.1

---

1. Bit 5 of the IA32_VMX_MISC MSR is read as 1 on any logical processor that supports the 1-setting of the “unrestricted guest” VM-execution control.
### 27.2.1 Basic VM-Exit Information

Section 24.9.1 defines the basic VM-exit information fields. The following items detail their use.

- **Exit reason.**
  - Bits 15:0 of this field contain the basic exit reason. It is loaded with a number indicating the general cause of the VM exit. Appendix C lists the numbers used and their meaning.
  - The remainder of the field (bits 31:16) is cleared to 0 (certain SMM VM exits may set some of these bits; see Section 34.15.2.3).\(^1\)

- **Exit qualification.** This field is saved for VM exits due to the following causes: debug exceptions; page-fault exceptions; start-up IPIs (SIPIs); system-management interrupts (SMIs) that arrive immediately after the retirement of I/O instructions; task switches; INVEPT; INVLPD; INVPCID; INVPID; LGDT; LDIT; LLDT; LTR; SGDT; SIDT; SDLT; STR; VMCLEAR; VMPTRLD; VMPTRST; VMREAD; VMWRITE; VMXON; XRSTORS; XSAVES; control-register accesses; MOV DR; I/O instructions; MWAIT; accesses to the APIC-access page (see Section 29.4); EPT violations; EOI virtualization (see Section 29.1.4); APIC-write emulation (see Section 29.4.3.3); and page-modification log full (see Section 28.2.5). For all other VM exits, this field is cleared. The following items provide details:
  - For a debug exception, the exit qualification contains information about the debug exception. The information has the format given in Table 27-1.
  - For a page-fault exception, the exit qualification contains the linear address that caused the page fault. On processors that support Intel 64 architecture, bits 63:32 are cleared if the logical processor was not in 64-bit mode before the VM exit.
  - For a start-up IPI (SIPI), the exit qualification contains the SIPI vector information in bits 7:0. Bits 63:8 of the exit qualification are cleared to 0.
  - For a task switch, the exit qualification contains details about the task switch, encoded as shown in Table 27-2.
  - For INVLPG, the exit qualification contains the linear-address operand of the instruction.
    - On processors that support Intel 64 architecture, bits 63:32 are cleared if the logical processor was not in 64-bit mode before the VM exit.
    - If the INVLPG source operand specifies an unusable segment, the linear address specified in the exit qualification will match the linear address that the INVLPG would have used if no VM exit occurred. This address is not architecturally defined and may be implementation-specific.

---

1. Bit 31 of this field is set on certain VM-entry failures; see Section 26.7.
VM EXITS

— For INVEPT, INVPCID, INVPID, LGDT, LIDT, LLDT, LTR, SGDT, SIDT, SLDT, STR, VMCLEAR, VMPTRLD, VMPTRST, VMREAD, VMWRITE, VMXON, XRSTORS, and XSAVES, the exit qualification receives the value of the instruction’s displacement field, which is sign-extended to 64 bits if necessary (32 bits on processors that do not support Intel 64 architecture). If the instruction has no displacement (for example, has a register operand), zero is stored into the exit qualification.

On processors that support Intel 64 architecture, an exception is made for RIP-relative addressing (used only in 64-bit mode). Such addressing causes an instruction to use an address that is the sum of the displacement field and the value of RIP that references the following instruction. In this case, the exit qualification is loaded with the sum of the displacement field and the appropriate RIP value.

In all cases, bits of this field beyond the instruction’s address size are undefined. For example, suppose that the address-size field in the VM-exit instruction-information field (see Section 24.9.4 and Section 27.2.4) reports an \( n \)-bit address size. Then bits 63:\( n \) (bits 31:\( n \) on processors that do not support Intel 64 architecture) of the instruction displacement are undefined.

— For a control-register access, the exit qualification contains information about the access and has the format given in Table 27-3.

— For MOV DR, the exit qualification contains information about the instruction and has the format given in Table 27-4.

— For an I/O instruction, the exit qualification contains information about the instruction and has the format given in Table 27-5.

— For MWAIT, the exit qualification contains a value that indicates whether address-range monitoring hardware was armed. The exit qualification is set either to 0 (if address-range monitoring hardware is not armed) or to 1 (if address-range monitoring hardware is armed).

— For an APIC-access VM exit resulting from a linear access or a guest-physical access to the APIC-access page (see Section 29.4), the exit qualification contains information about the access and has the format given in Table 27-6.\(^1\)

Such a VM exit that set bits 15:12 of the exit qualification to 0000b (data read during instruction execution) or 0001b (data write during instruction execution) set bit 12—which distinguishes data read from data write—to that which would have been stored in bit 1—W/R—of the page-fault error code had the access caused a page fault instead of an APIC-access VM exit. This implies the following:

• For an APIC-access VM exit caused by the CLFLUSH and CLFLUSHOPTH instructions, the access type is “data read during instruction execution.”

• For an APIC-access VM exit caused by the ENTER instruction, the access type is “data write during instruction execution.”

---

\(^1\) The exit qualification is undefined if the access was part of the logging of a branch record or a precise-event-based-sampling (PEBS) record to the DS save area. It is recommended that software configure the paging structures so that no address in the DS save area translates to an address on the APIC-access page.
For an APIC-access VM exit caused by the MASKMOVQ instruction or the MASKMOVDQU instruction, the access type is “data write during instruction execution.”

For an APIC-access VM exit caused by the MONITOR instruction, the access type is “data read during instruction execution.”

Such a VM exit stores 1 for bit 31 for IDT-vectoring information field (see Section 27.2.3) if and only if it sets bits 15:12 of the exit qualification to 0011b (linear access during event delivery) or 1010b (guest-physical access during event delivery).

See Section 29.4.4 for further discussion of these instructions and APIC-access VM exits.

For APIC-access VM exits resulting from physical accesses to the APIC-access page (see Section 29.4.6), the exit qualification is undefined.

– For an EPT violation, the exit qualification contains information about the access causing the EPT violation and has the format given in Table 27-7.

An EPT violation that occurs during as a result of execution of a read-modify-write operation sets bit 1 (data write). Whether it also sets bit 0 (data read) is implementation-specific and, for a given implementation, may differ for different kinds of read-modify-write operations.

---

Table 27-3. Exit Qualification for Control-Register Accesses

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Number of control register (0 for CLTS and LMSW). Bit 3 is always 0 on processors that do not support Intel 64 architecture as they do not support CR8.</td>
</tr>
<tr>
<td>5:4</td>
<td>Access type:</td>
</tr>
<tr>
<td></td>
<td>0 = MOV to CR</td>
</tr>
<tr>
<td></td>
<td>1 = MOV from CR</td>
</tr>
<tr>
<td></td>
<td>2 = CLTS</td>
</tr>
<tr>
<td></td>
<td>3 = LMSW</td>
</tr>
<tr>
<td>6</td>
<td>LMSW operand type:</td>
</tr>
<tr>
<td></td>
<td>0 = register</td>
</tr>
<tr>
<td></td>
<td>1 = memory</td>
</tr>
<tr>
<td></td>
<td>For CLTS and MOV CR, cleared to 0</td>
</tr>
<tr>
<td>7</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>11:8</td>
<td>For MOV CR, the general-purpose register:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>For CLTS and LMSW, cleared to 0</td>
</tr>
<tr>
<td>15:12</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>31:16</td>
<td>For LMSW, the LMSW source data</td>
</tr>
<tr>
<td></td>
<td>For CLTS and MOV CR, cleared to 0</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved (cleared to 0). These bits exist only on processors that support Intel 64 architecture.</td>
</tr>
</tbody>
</table>
Bit 12 is undefined in any of the following cases:

- If the "NMI exiting" VM-execution control is 1 and the "virtual NMIs" VM-execution control is 0.
- If the VM exit sets the valid bit in the IDT-vectoring information field (see Section 27.2.3).

Otherwise, bit 12 is defined as follows:

- If the "virtual NMIs" VM-execution control is 0, the EPT violation was caused by a memory access as part of execution of the IRET instruction, and blocking by NMI (see Table 24-3) was in effect before execution of IRET, bit 12 is set to 1.

### Table 27-4. Exit Qualification for MOV DR

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Number of debug register</td>
</tr>
<tr>
<td>3</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>4</td>
<td>Direction of access (0 = MOV to DR; 1 = MOV from DR)</td>
</tr>
<tr>
<td>7:5</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>11:8</td>
<td>General-purpose register:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8 - 15 = R8 - R15, respectively</td>
</tr>
<tr>
<td>63:12</td>
<td>Reserved (cleared to 0)</td>
</tr>
</tbody>
</table>

### Table 27-5. Exit Qualification for I/O Instructions

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Size of access:</td>
</tr>
<tr>
<td></td>
<td>0 = 1-byte</td>
</tr>
<tr>
<td></td>
<td>1 = 2-byte</td>
</tr>
<tr>
<td></td>
<td>3 = 4-byte</td>
</tr>
<tr>
<td></td>
<td>Other values not used</td>
</tr>
<tr>
<td>3</td>
<td>Direction of the attempted access (0 = OUT, 1 = IN)</td>
</tr>
<tr>
<td>4</td>
<td>String instruction (0 = not string; 1 = string)</td>
</tr>
<tr>
<td>5</td>
<td>REP prefixed (0 = not REP; 1 = REP)</td>
</tr>
<tr>
<td>6</td>
<td>Operand encoding (0 = DX, 1 = immediate)</td>
</tr>
<tr>
<td>15:7</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>31:16</td>
<td>Port number (as specified in DX or in an immediate operand)</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved (cleared to 0). These bits exist only on processors that support Intel 64 architecture.</td>
</tr>
</tbody>
</table>
If the "virtual NMIs" VM-execution control is 1, the EPT violation was caused by a memory access as part of execution of the IRET instruction, and virtual-NMI blocking was in effect before execution of IRET, bit 12 is set to 1.

For all other relevant VM exits, bit 12 is cleared to 0.

For VM exits caused as part of EOI virtualization (Section 29.1.4), bits 7:0 of the exit qualification are set to vector of the virtual interrupt that was dismissed by the EOI virtualization. Bits above bit 7 are cleared.

For APIC-write VM exits (Section 29.4.3.3), bits 11:0 of the exit qualification are set to the page offset of the write access that caused the VM exit. Bits above bit 11 are cleared.

For a VM exit due to a page-modification log-full event (Section 28.2.5), only bit 12 of the exit qualification is defined, and only in some cases. It is undefined in the following cases:

- If the "NMI exiting" VM-execution control is 1 and the "virtual NMIs" VM-execution control is 0.
- If the VM exit sets the valid bit in the IDT-vectoring information field (see Section 27.2.3).

Otherwise, it is defined as follows:

- If the "virtual NMIs" VM-execution control is 0, the page-modification log-full event was caused by a memory access as part of execution of the IRET instruction, and blocking by NMI (see Table 24-3) was in effect before execution of IRET, bit 12 is set to 1.

- If the "virtual NMIs" VM-execution control is 1, the page-modification log-full event was caused by a memory access as part of execution of the IRET instruction, and virtual-NMI blocking was in effect before execution of IRET, bit 12 is set to 1.

For all other relevant VM exits, bit 12 is cleared to 0.

For these VM exits, all bits other than bit 12 are undefined.

**Guest-linear address.** For some VM exits, this field receives a linear address that pertains to the VM exit. The field is set for different VM exits as follows:

- VM exits due to attempts to execute LMSW with a memory operand. In these cases, this field receives the linear address of that operand. Bits 63:32 are cleared if the logical processor was not in 64-bit mode before the VM exit.

- VM exits due to attempts to execute INS or OUTS for which the relevant segment is usable (if the relevant segment is not usable, the value is undefined). (ES is always the relevant segment for INS; for OUTS, the relevant segment is DS unless overridden by an instruction prefix.) The linear address is the base address of relevant segment plus (E)DI (for INS) or (E)SI (for OUTS). Bits 63:32 are cleared if the logical processor was not in 64-bit mode before the VM exit.

---

Table 27-6. Exit Qualification for APIC-Access VM Exits from Linear Accesses and Guest-Physical Accesses

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
</table>
| 11:0            | - If the APIC-access VM exit is due to a linear access, the offset of access within the APIC page.  
                   - Undefined if the APIC-access VM exit is due a guest-physical access |
| 15:12           | Access type:  
                   0 = linear access for a data read during instruction execution  
                   1 = linear access for a data write during instruction execution  
                   2 = linear access for an instruction fetch  
                   3 = linear access (read or write) during event delivery  
                   10 = guest-physical access during event delivery  
                   15 = guest-physical access for an instruction fetch or during instruction execution  
                   Other values not used |
| 63:16           | Reserved (cleared to 0). Bits 63:32 exist only on processors that support Intel 64 architecture. |

---

 Execution of WRMSR with ECX = B3FH (self-IPI MSR) can lead to an APIC-write VM exit; the exit qualification for such an APIC-write VM exit is 3F0H.
VM EXITS

Table 27-7. Exit Qualification for EPT Violations

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Set if the access causing the EPT violation was a data read.¹</td>
</tr>
<tr>
<td>1</td>
<td>Set if the access causing the EPT violation was a data write.¹</td>
</tr>
<tr>
<td>2</td>
<td>Set if the access causing the EPT violation was an instruction fetch.</td>
</tr>
<tr>
<td>3</td>
<td>The logical-AND of bit 0 in the EPT paging-structure entries used to translate the guest-physical address of the access causing the EPT violation (indicates that the guest-physical address was readable).²</td>
</tr>
<tr>
<td>4</td>
<td>The logical-AND of bit 1 in the EPT paging-structure entries used to translate the guest-physical address of the access causing the EPT violation (indicates that the guest-physical address was writeable).</td>
</tr>
<tr>
<td>5</td>
<td>The logical-AND of bit 2 in the EPT paging-structure entries used to translate the guest-physical address of the access causing the EPT violation (indicates that the guest-physical address was executable).</td>
</tr>
<tr>
<td>6</td>
<td>Reserved (cleared to 0).</td>
</tr>
<tr>
<td>7</td>
<td>Set if the guest linear-address field is valid. The guest linear-address field is valid for all EPT violations except those resulting from an attempt to load the guest PDPTEs as part of the execution of the MOV CR instruction.</td>
</tr>
<tr>
<td>8</td>
<td>If bit 7 is 1:</td>
</tr>
<tr>
<td></td>
<td>• Set if the access causing the EPT violation is to a guest-physical address that is the translation of a linear address.</td>
</tr>
<tr>
<td></td>
<td>• Clear if the access causing the EPT violation is to a paging-structure entry as part of a page walk or the update of an accessed or dirty bit.</td>
</tr>
<tr>
<td></td>
<td>Reserved if bit 7 is 0 (cleared to 0).</td>
</tr>
<tr>
<td>11:9</td>
<td>Reserved (cleared to 0).</td>
</tr>
<tr>
<td>12</td>
<td>NMI unblocking due to IRET</td>
</tr>
<tr>
<td>63:13</td>
<td>Reserved (cleared to 0).</td>
</tr>
</tbody>
</table>

NOTES:

1. If accessed and dirty flags for EPT are enabled, processor accesses to guest paging-structure entries are treated as writes with regard to EPT violations (see Section 28.2.3.2). If such an access causes an EPT violation, the processor sets both bit 0 and bit 1 of the exit qualification.

2. Bits 5:3 are cleared to 0 if any of EPT paging-structure entries used to translate the guest-physical address of the access causing the EPT violation is not present (see Section 28.2.2).

   — VM exits due to EPT violations that set bit 7 of the exit qualification (see Table 27-7; these are all EPT violations except those resulting from an attempt to load the PDPTEs as of execution of the MOV CR instruction). The linear address may translate to the guest-physical address whose access caused the EPT violation. Alternatively, translation of the linear address may reference a paging-structure entry whose access caused the EPT violation. Bits 63:32 are cleared if the logical processor was not in 64-bit mode before the VM exit.

   — For all other VM exits, the field is undefined.

• **Guest-physical address.** For a VM exit due to an EPT violation or an EPT misconfiguration, this field receives the guest-physical address that caused the EPT violation or EPT misconfiguration. For all other VM exits, the field is undefined.
Information for VM Exits Due to Vectored Events

Section 24.9.2 defines fields containing information for VM exits due to the following events: exceptions (including those generated by the instructions INT3, INTO, BOUND, and UD2); external interrupts that occur while the "acknowledge interrupt on exit" VM-exit control is 1; and non-maskable interrupts (NMIs). Such VM exits include those that occur on an attempt at a task switch that causes an exception before generating the VM exit due to the task switch that causes the VM exit.

The following items detail the use of these fields:

- **VM-exit interruption information** (format given in Table 24-15). The following items detail how this field is established for VM exits due to these events:
  - For an exception, bits 7:0 receive the exception vector (at most 31). For an NMI, bits 7:0 are set to 2. For an external interrupt, bits 7:0 receive the vector.
  - Bits 10:8 are set to 0 (external interrupt), 2 (non-maskable interrupt), 3 (hardware exception), or 6 (software exception). Hardware exceptions comprise all exceptions except breakpoint exceptions (#BP; generated by INT3) and overflow exceptions (#OF; generated by INTO); these are software exceptions. BOUND-range exceeded exceptions (#BR; generated by BOUND) and invalid opcode exceptions (#UD) generated by UD2 are hardware exceptions.
  - Bit 11 is set to 1 if the VM exit is caused by a hardware exception that would have delivered an error code on the stack. This bit is always 0 if the VM exit occurred while the logical processor was in real-address mode (CR0.PE=0). If bit 11 is set to 1, the error code is placed in the VM-exit interruption error code (see below).
  - Bit 12 is undefined in any of the following cases:
    - If the "NMI exiting” VM-execution control is 1 and the “virtual NMIs” VM-execution control is 0.
    - If the VM exit sets the valid bit in the IDT-vectoring information field (see Section 27.2.3).
    - If the VM exit is due to a double fault (the interruption type is hardware exception and the vector is 8).
  - For other VM exits (including those due to external interrupts when the "acknowledge interrupt on exit” VM-exit control is 0), the field is marked invalid (by clearing bit 31) and the remainder of the field is undefined.

- **VM-exit interruption error code.**
  - For VM exits that set both bit 31 (valid) and bit 11 (error code valid) in the VM-exit interruption-information field, this field receives the error code that would have been pushed on the stack had the event causing the VM exit been delivered normally through the IDT. The EXT bit is set in this field exactly when it would be set normally. For exceptions that occur during the delivery of double fault (if the IDT-vectoring information field indicates a double fault), the EXT bit is set to 1, assuming that (1) the exception would produce an error code normally (if not incident to double-fault delivery) and (2) that the error code uses the EXT bit (not for page faults, which use a different format).

1. If the capability MSR IA32_VMX_CRO_FIXED0 reports that CR0.PE must be 1 in VMX operation, a logical processor cannot be in real-address mode unless the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
2. The conditions imply that, if the "NMI exiting” VM-execution control is 0 or the “virtual NMIs” VM-execution control is 1, bit 12 is always cleared to 0 by VM exits due to debug exceptions.
27.2.3 Information for VM Exits During Event Delivery

Section 24.9.3 defined fields containing information for VM exits that occur while delivering an event through the IDT and as a result of any of the following cases:

- A fault occurs during event delivery and causes a VM exit (because the bit associated with the fault is set to 1 in the exception bitmap).
- A task switch is invoked through a task gate in the IDT. The VM exit occurs due to the task switch only after the initial checks of the task switch pass (see Section 25.4.2).
- Event delivery causes an APIC-access VM exit (see Section 29.4).
- An EPT violation, EPT misconfiguration, or page-modification log-full event that occurs during event delivery.

These fields are used for VM exits that occur during delivery of events injected as part of VM entry (see Section 26.5.1.2).

A VM exit is not considered to occur during event delivery in any of the following circumstances:

- The original event causes the VM exit directly (for example, because the original event is a non-maskable interrupt (NMI) and the "NMI exiting" VM-execution control is 1).
- The original event results in a double-fault exception that causes the VM exit directly.
- The VM exit occurred as a result of fetching the first instruction of the handler invoked by the event delivery.
- The VM exit is caused by a triple fault.

The following items detail the use of these fields:

- IDT-vectoring information (format given in Table 24-16). The following items detail how this field is established for VM exits that occur during event delivery:
  - If the VM exit occurred during delivery of an exception, bits 7:0 receive the exception vector (at most 31).
  - If the VM exit occurred during delivery of an NMI, bits 7:0 are set to 2. If the VM exit occurred during delivery of an external interrupt, bits 7:0 receive the vector.
  - Bits 10:8 are set to indicate the type of event that was being delivered when the VM exit occurred: 0 (external interrupt), 2 (non-maskable interrupt), 3 (hardware exception), 4 (software interrupt), 5 (privileged software interrupt), or 6 (software exception).
  - Hardware exceptions comprise all exceptions except breakpoint exceptions (#BP; generated by INT3) and overflow exceptions (#OF; generated by INTO); these are software exceptions. BOUND-range exceeded exceptions (#BR; generated by BOUND) and invalid opcode exceptions (#UD) generated by UD2 are hardware exceptions.
  - Bits 10:8 may indicate privileged software interrupt if such an event was injected as part of VM entry.
  - Bit 11 is set to 1 if the VM exit occurred during delivery of a hardware exception that would have delivered an error code on the stack. This bit is always 0 if the VM exit occurred while the logical processor was in real-address mode (CR0.PE=0). If bit 11 is set to 1, the error code is placed in the IDT-vectoring error code (see below).
  - Bit 12 is undefined.
  - Bits 30:13 are always set to 0.
  - Bit 31 is always set to 1.

For other VM exits, the field is marked invalid (by clearing bit 31) and the remainder of the field is undefined.

---

1. This includes the case in which a VM exit occurs while delivering a software interrupt (INT n) through the 16-bit IVT (interrupt vector table) that is used in virtual-8086 mode with virtual-machine extensions (if RFLAGS.VM = CR4.VME = 1).

2. If the capability MSR IA32_VMX_CRO_FIXED0 reports that CR0.PE must be 1 in VMX operation, a logical processor cannot be in real-address mode unless the "unrestricted guest" VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
• IDT-vectoring error code.
  — For VM exits that set both bit 31 (valid) and bit 11 (error code valid) in the IDT-vectoring information field, this field receives the error code that would have been pushed on the stack by the event that was being delivered through the IDT at the time of the VM exit. The EXT bit is set in this field when it would be set normally.
  — For other VM exits, the value of this field is undefined.

27.2.4 Information for VM Exits Due to Instruction Execution

Section 24.9.4 defined fields containing information for VM exits that occur due to instruction execution. (The VM-exit instruction length is also used for VM exits that occur during the delivery of a software interrupt or software exception.) The following items detail their use.

• VM-exit instruction length. This field is used in the following cases:
  — For fault-like VM exits due to attempts to execute one of the following instructions that cause VM exits unconditionally (see Section 25.1.2) or based on the settings of VM-execution controls (see Section 25.1.3): CLTS, CPUID, GETSEC, HLT, IN, INS, INV, INVEPT, INVPG, INVPID, LGDT, LIDT, LLDT, LMSW, LTR, MONITOR, MOV CR, MOV DR, MWAIT, OUT, OUTS, PAUSE, RDMSR, RDPMC, RDRAND, RDSEED, RDTSC, RDTSCP, RSM, SGDT, SIDT, SLDT, STR, VMCALL, VMCLEAR, VMLAUNCH, VMPTRLD, VMPTRST, VMREAD, VMRESUME, VMWRITE, VMXOFF, VMXON, WBINVD, WRMSR, XRSTORS, XSETBV, and XSAVE.1
  — For VM exits due to software exceptions (those generated by executions of INT3 or INTO).
  — For VM exits due to faults encountered during delivery of a software interrupt, privileged software exception, or software exception.
  — For VM exits due to attempts to effect a task switch via instruction execution. These are VM exits that produce an exit reason indicating task switch and either of the following:
    • An exit qualification indicating execution of CALL, IRET, or JMP instruction.
    • An exit qualification indicating a task gate in the IDT and an IDT-vectoring information field indicating that the task gate was encountered during delivery of a software interrupt, privileged software exception, or software exception.
  — For APIC-access VM exits resulting from accesses (see Section 29.4) during delivery of a software interrupt, privileged software exception, or software exception.2
  — For VM exits due executions of VMFUNC that fail because one of the following is true:
    • EAX indicates a VM function that is not enabled (the bit at position EAX is 0 in the VM-function controls; see Section 25.5.5.2).
    • EAX = 0 and either ECX ≥ 512 or the value of ECX selects an invalid tentative EPTP value (see Section 25.5.5.3).

In all the above cases, this field receives the length in bytes (1–15) of the instruction (including any instruction prefixes) whose execution led to the VM exit (see the next paragraph for one exception).

The cases of VM exits encountered during delivery of a software interrupt, privileged software exception, or software exception include those encountered during delivery of events injected as part of VM entry (see Section 26.5.1.2). If the original event was injected as part of VM entry, this field receives the value of the VM-entry instruction length.

All VM exits other than those listed in the above items leave this field undefined.

1. This item applies only to fault-like VM exits. It does not apply to trap-like VM exits following executions of the MOV to CR8 instruction when the “use TPR shadow” VM-execution control is 1 or to those following executions of the WRMSR instruction when the “virtualize x2APIC mode” VM-execution control is 1.
2. The VM-exit instruction-length field is not defined following APIC-access VM exits resulting from physical accesses (see Section 29.4.6) even if encountered during delivery of a software interrupt, privileged software exception, or software exception.
VM-EXIT instruction information. For VM exits due to attempts to execute INS, INVEPT, INVPCID, INVVPID, LIDT, LGDT, LLDT, LTR, OUTS, RDRAND, RDSEEED, SIDT, SGDT, SLDT, STR, VMCLEAR, VMPtrLD, VMPtrST, VMREAD, VMWRITE, VMXON, XRSTORS, or XSAVES, this field receives information about the instruction that caused the VM exit. The format of the field depends on the identity of the instruction causing the VM exit:

- For VM exits due to attempts to execute INS or OUTS, the field has the format is given in Table 27-8.1
- For VM exits due to attempts to execute INVEPT, INVPCID, or INVVPID, the field has the format is given in Table 27-9.
- For VM exits due to attempts to execute LIDT, LGDT, SIDT, or SGDT, the field has the format is given in Table 27-10.
- For VM exits due to attempts to execute LLDT, LTR, SLDT, or STR, the field has the format is given in Table 27-11.
- For VM exits due to attempts to execute RDRAND or RDSEEED, the field has the format is given in Table 27-12.
- For VM exits due to attempts to execute VMCLEAR, VMPtrLD, VMPtrST, VMXON, XRSTORS, or XSAVES, the field has the format is given in Table 27-13.
- For VM exits due to attempts to execute VMREAD or VMWRITE, the field has the format is given in Table 27-14.

For all other VM exits, the field is undefined.

I/O RCX, I/O RSI, I/O RDI, I/O RIP. These fields are undefined except for SMM VM exits due to system-management interrupts (SMIs) that arrive immediately after retirement of I/O instructions. See Section 34.15.2.3.

Table 27-8. Format of the VM-Exit Instruction-Information Field as Used for INS and OUTS

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:0</td>
<td>Undefined.</td>
</tr>
<tr>
<td>9:7</td>
<td>Address size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>14:10</td>
<td>Undefined.</td>
</tr>
<tr>
<td>17:15</td>
<td>Segment register:</td>
</tr>
<tr>
<td></td>
<td>0: ES</td>
</tr>
<tr>
<td></td>
<td>1: CS</td>
</tr>
<tr>
<td></td>
<td>2: SS</td>
</tr>
<tr>
<td></td>
<td>3: DS</td>
</tr>
<tr>
<td></td>
<td>4: FS</td>
</tr>
<tr>
<td></td>
<td>5: GS</td>
</tr>
<tr>
<td></td>
<td>Other values not used. Undefined for VM exits due to execution of INS.</td>
</tr>
<tr>
<td>31:18</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>

1. The format of the field was undefined for these VM exits on the first processors to support the virtual-machine extensions. Software can determine whether the format specified in Table 27-8 is used by consulting the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).
### Table 27-9. Format of the VM-Exit Instruction-Information Field as Used for INVEPT, INVPCID, and INVVID

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Scaling:</td>
</tr>
<tr>
<td></td>
<td>0: no scaling</td>
</tr>
<tr>
<td></td>
<td>1: scale by 2</td>
</tr>
<tr>
<td></td>
<td>2: scale by 4</td>
</tr>
<tr>
<td></td>
<td>3: scale by 8 (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>6:2</td>
<td>Undefined.</td>
</tr>
<tr>
<td>9:7</td>
<td>Address size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>10</td>
<td>Cleared to 0.</td>
</tr>
<tr>
<td>14:11</td>
<td>Undefined.</td>
</tr>
<tr>
<td>17:15</td>
<td>Segment register:</td>
</tr>
<tr>
<td></td>
<td>0: ES</td>
</tr>
<tr>
<td></td>
<td>1: CS</td>
</tr>
<tr>
<td></td>
<td>2: SS</td>
</tr>
<tr>
<td></td>
<td>3: DS</td>
</tr>
<tr>
<td></td>
<td>4: FS</td>
</tr>
<tr>
<td></td>
<td>5: GS</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>21:18</td>
<td>IndexReg:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>22</td>
<td>IndexReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>26:23</td>
<td>BaseReg (encoded as IndexReg above)</td>
</tr>
<tr>
<td></td>
<td>Undefined for memory instructions with no base register (bit 27 is set).</td>
</tr>
<tr>
<td>27</td>
<td>BaseReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>31:28</td>
<td>Reg2 (same encoding as IndexReg above)</td>
</tr>
</tbody>
</table>

### Table 27-10. Format of the VM-Exit Instruction-Information Field as Used for LIDT, LGDT, SIDT, or SGDT

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Scaling:</td>
</tr>
<tr>
<td></td>
<td>0: no scaling</td>
</tr>
<tr>
<td></td>
<td>1: scale by 2</td>
</tr>
<tr>
<td></td>
<td>2: scale by 4</td>
</tr>
<tr>
<td></td>
<td>3: scale by 8 (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>6:2</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>
Table 27-10. Format of the VM-Exit Instruction-Information Field as Used for LIDT, LGDT, SIDT, or SGDT (Contd.)

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:7</td>
<td>Address size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>10</td>
<td>Cleared to 0.</td>
</tr>
<tr>
<td>11</td>
<td>Operand size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>Undefined for VM exits from 64-bit mode.</td>
</tr>
<tr>
<td>14:12</td>
<td>Undefined.</td>
</tr>
<tr>
<td>17:15</td>
<td>Segment register:</td>
</tr>
<tr>
<td></td>
<td>0: ES</td>
</tr>
<tr>
<td></td>
<td>1: CS</td>
</tr>
<tr>
<td></td>
<td>2: SS</td>
</tr>
<tr>
<td></td>
<td>3: DS</td>
</tr>
<tr>
<td></td>
<td>4: FS</td>
</tr>
<tr>
<td></td>
<td>5: GS</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>21:18</td>
<td>IndexReg:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>22</td>
<td>IndexReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>26:23</td>
<td>BaseReg (encoded as IndexReg above)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no base register (bit 27 is set).</td>
</tr>
<tr>
<td>27</td>
<td>BaseReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>29:28</td>
<td>Instruction identity:</td>
</tr>
<tr>
<td></td>
<td>0: SGDT</td>
</tr>
<tr>
<td></td>
<td>1: SIDT</td>
</tr>
<tr>
<td></td>
<td>2: LGDT</td>
</tr>
<tr>
<td></td>
<td>3: LIDT</td>
</tr>
<tr>
<td>31:30</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>
Table 27-11. Format of the VM-Exit Instruction-Information Field as Used for LLDT, LTR, SLDT, and STR

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Scaling:</td>
</tr>
<tr>
<td></td>
<td>0: no scaling</td>
</tr>
<tr>
<td></td>
<td>1: scale by 2</td>
</tr>
<tr>
<td></td>
<td>2: scale by 4</td>
</tr>
<tr>
<td></td>
<td>3: scale by 8 (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set) and for memory instructions with no index register (bit 10 is clear and bit 22 is set).</td>
</tr>
<tr>
<td>2</td>
<td>Undefined.</td>
</tr>
<tr>
<td>6:3</td>
<td>Reg1:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for memory instructions (bit 10 is clear).</td>
</tr>
<tr>
<td>9:7</td>
<td>Address size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Other values not used. Undefined for register instructions (bit 10 is set).</td>
</tr>
<tr>
<td>10</td>
<td>Mem/Reg (0 = memory; 1 = register).</td>
</tr>
<tr>
<td>14:11</td>
<td>Undefined.</td>
</tr>
<tr>
<td>17:15</td>
<td>Segment register:</td>
</tr>
<tr>
<td></td>
<td>0: ES</td>
</tr>
<tr>
<td></td>
<td>1: CS</td>
</tr>
<tr>
<td></td>
<td>2: SS</td>
</tr>
<tr>
<td></td>
<td>3: DS</td>
</tr>
<tr>
<td></td>
<td>4: FS</td>
</tr>
<tr>
<td></td>
<td>5: GS</td>
</tr>
<tr>
<td></td>
<td>Other values not used. Undefined for register instructions (bit 10 is set).</td>
</tr>
<tr>
<td>21:18</td>
<td>IndexReg (encoded as Reg1 above)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set) and for memory instructions with no index register (bit 10 is clear and bit 22 is set).</td>
</tr>
<tr>
<td>22</td>
<td>IndexReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set).</td>
</tr>
<tr>
<td>26:23</td>
<td>BaseReg (encoded as Reg1 above)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set) and for memory instructions with no base register (bit 10 is clear and bit 27 is set).</td>
</tr>
<tr>
<td>27</td>
<td>BaseReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set).</td>
</tr>
</tbody>
</table>
### Table 27-11. Format of the VM-Exit Instruction-Information Field as Used for LLDT, LTR, SLDT, and STR (Contd.)

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>29:28</td>
<td>Instruction identity:</td>
</tr>
<tr>
<td></td>
<td>0: SLDT</td>
</tr>
<tr>
<td></td>
<td>1: STR</td>
</tr>
<tr>
<td></td>
<td>2: LLDT</td>
</tr>
<tr>
<td></td>
<td>3: LTR</td>
</tr>
<tr>
<td>31:30</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>

### Table 27-12. Format of the VM-Exit Instruction-Information Field as Used for RDRAND and RDSEED

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Undefined.</td>
</tr>
<tr>
<td>6:3</td>
<td>Destination register:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td>8–15</td>
<td>represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td>10:7</td>
<td>Undefined.</td>
</tr>
<tr>
<td>12:11</td>
<td>Operand size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit</td>
</tr>
<tr>
<td></td>
<td>The value 3 is not used.</td>
</tr>
<tr>
<td>31:13</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>

### Table 27-13. Format of the VM-Exit Instruction-Information Field as Used for VMCLEAR, VMPTRLD, VMPTRST, VMXON, XRSTORS, and XSAVEs

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Scaling:</td>
</tr>
<tr>
<td></td>
<td>0: no scaling</td>
</tr>
<tr>
<td></td>
<td>1: scale by 2</td>
</tr>
<tr>
<td></td>
<td>2: scale by 4</td>
</tr>
<tr>
<td></td>
<td>3: scale by 8 (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>6:2</td>
<td>Undefined.</td>
</tr>
<tr>
<td>9:7</td>
<td>Address size:</td>
</tr>
<tr>
<td></td>
<td>0: 16-bit</td>
</tr>
<tr>
<td></td>
<td>1: 32-bit</td>
</tr>
<tr>
<td></td>
<td>2: 64-bit (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>10</td>
<td>Cleared to 0.</td>
</tr>
<tr>
<td>14:11</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>
VM EXITS

Table 27-13. Format of the VM-Exit Instruction-Information Field as Used for VMCLEAR, VMPTRLD, VMPTRST, VMXON, XRSTORS, and XSAVES (Contd.)

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>17:15</td>
<td>Segment register:</td>
</tr>
<tr>
<td></td>
<td>0: ES</td>
</tr>
<tr>
<td></td>
<td>1: CS</td>
</tr>
<tr>
<td></td>
<td>2: SS</td>
</tr>
<tr>
<td></td>
<td>3: DS</td>
</tr>
<tr>
<td></td>
<td>4: FS</td>
</tr>
<tr>
<td></td>
<td>5: GS</td>
</tr>
<tr>
<td></td>
<td>Other values not used.</td>
</tr>
<tr>
<td>21:18</td>
<td>IndexReg:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no index register (bit 22 is set).</td>
</tr>
<tr>
<td>22</td>
<td>IndexReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>26:23</td>
<td>BaseReg (encoded as IndexReg above)</td>
</tr>
<tr>
<td></td>
<td>Undefined for instructions with no base register (bit 27 is set).</td>
</tr>
<tr>
<td>27</td>
<td>BaseReg invalid (0 = valid; 1 = invalid)</td>
</tr>
<tr>
<td>31:28</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>

Table 27-14. Format of the VM-Exit Instruction-Information Field as Used for VMREAD and VMWRITE

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Content</th>
</tr>
</thead>
<tbody>
<tr>
<td>1:0</td>
<td>Scaling:</td>
</tr>
<tr>
<td></td>
<td>0: no scaling</td>
</tr>
<tr>
<td></td>
<td>1: scale by 2</td>
</tr>
<tr>
<td></td>
<td>2: scale by 4</td>
</tr>
<tr>
<td></td>
<td>3: scale by 8 (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for register instructions (bit 10 is set) and for memory instructions with no index register (bit 10 is clear and bit 22 is set).</td>
</tr>
<tr>
<td>2</td>
<td>Undefined.</td>
</tr>
<tr>
<td>6:3</td>
<td>Reg1:</td>
</tr>
<tr>
<td></td>
<td>0 = RAX</td>
</tr>
<tr>
<td></td>
<td>1 = RCX</td>
</tr>
<tr>
<td></td>
<td>2 = RDX</td>
</tr>
<tr>
<td></td>
<td>3 = RBX</td>
</tr>
<tr>
<td></td>
<td>4 = RSP</td>
</tr>
<tr>
<td></td>
<td>5 = RBP</td>
</tr>
<tr>
<td></td>
<td>6 = RSI</td>
</tr>
<tr>
<td></td>
<td>7 = RDI</td>
</tr>
<tr>
<td></td>
<td>8–15 represent R8–R15, respectively (used only on processors that support Intel 64 architecture)</td>
</tr>
<tr>
<td></td>
<td>Undefined for memory instructions (bit 10 is clear).</td>
</tr>
</tbody>
</table>
27.3 SAVING GUEST STATE

Each field in the guest-state area of the VMCS (see Section 24.4) is written with the corresponding component of processor state. On processors that support Intel 64 architecture, the full values of each natural-width field (see Section 24.11.2) is saved regardless of the mode of the logical processor before and after the VM exit.

In general, the state saved is that which was in the logical processor at the time the VM exit commences. See Section 27.1 for a discussion of which architectural updates occur at that time.

Section 27.3.1 through Section 27.3.4 provide details for how certain components of processor state are saved. These sections reference VMCS fields that correspond to processor state. Unless otherwise stated, these references are to fields in the guest-state area.

27.3.1 Saving Control Registers, Debug Registers, and MSRs

Contents of certain control registers, debug registers, and MSRs is saved as follows:

- The contents of CR0, CR3, CR4, and the IA32_SYSENTER_CS, IA32_SYSENTER_ESP, and IA32_SYSENTER_EIP MSRs are saved into the corresponding fields. Bits 63:32 of the IA32_SYSENTER_CS MSR are not saved. On processors that do not support Intel 64 architecture, bits 63:32 of the IA32_SYSENTER_ESP and IA32_SYSENTER_EIP MSRs are not saved.
• If the "save debug controls" VM-exit control is 1, the contents of DR7 and the IA32_DEBUGCTL MSR are saved into the corresponding fields. The first processors to support the virtual-machine extensions supported only the 1-setting of this control and thus always saved data into these fields.

• If the "save IA32_PAT" VM-exit control is 1, the contents of the IA32_PAT MSR are saved into the corresponding field.

• If the "save IA32_EFER" VM-exit control is 1, the contents of the IA32_EFER MSR are saved into the corresponding field.

• The value of the SMBASE field is undefined after all VM exits except SMM VM exits. See Section 34.15.2.

27.3.2 Saving Segment Registers and Descriptor-Table Registers

For each segment register (CS, SS, DS, ES, FS, GS, LDTR, or TR), the values saved for the base-address, segment-limit, and access rights are based on whether the register was unusable (see Section 24.4.1) before the VM exit:

• If the register was unusable, the values saved into the following fields are undefined: (1) base address; (2) segment limit; and (3) bits 7:0 and bits 15:12 in the access-rights field. The following exceptions apply:
  — CS.
    • The base-address and segment-limit fields are saved.
    • The L, D, and G bits are saved in the access-rights field.
  — SS.
    • DPL is saved in the access-rights field.
    • On processors that support Intel 64 architecture, bits 63:32 of the value saved for the base address are always zero.
  — DS and ES. On processors that support Intel 64 architecture, bits 63:32 of the values saved for the base addresses are always zero.
  — FS and GS. The base-address field is saved.
  — LDTR. The value saved for the base address is always canonical.

• If the register was not unusable, the values saved into the following fields are those which were in the register before the VM exit: (1) base address; (2) segment limit; and (3) bits 7:0 and bits 15:12 in the access-rights field. The following exceptions apply:

  Bits 31:17 and 11:8 in the access-rights field are always cleared. Bit 16 is set to 1 if and only if the segment is unusable.

The contents of the GDTR and IDTR registers are saved into the corresponding base-address and limit fields.

27.3.3 Saving RIP, RSP, and RFLAGS

The contents of the RIP, RSP, and RFLAGS registers are saved as follows:

• The value saved in the RIP field is determined by the nature and cause of the VM exit:
  — If the VM exit occurs due to by an attempt to execute an instruction that causes VM exits unconditionally or that has been configured to cause a VM exit via the VM-execution controls, the value saved references that instruction.
  — If the VM exit is caused by an occurrence of an INIT signal, a start-up IPI (SIPI), or system-management interrupt (SMI), the value saved is that which was in RIP before the event occurred.
  — If the VM exit occurs due to the 1-setting of either the "interrupt-window exiting" VM-execution control or the "NMI-window exiting" VM-execution control, the value saved is that which would be in the register had the VM exit not occurred.
  — If the VM exit is due to an external interrupt, non-maskable interrupt (NMI), or hardware exception (as defined in Section 27.2.2), the value saved is the return pointer that would have been saved (either on the stack had the event been delivered through a trap or interrupt gate, or into the old task-state segment had the event been delivered through a task gate).
— If the VM exit is due to a triple fault, the value saved is the return pointer that would have been saved (either on the stack had the event been delivered through a trap or interrupt gate, or into the old task-state segment had the event been delivered through a task gate) had delivery of the double fault not encountered the nested exception that caused the triple fault.

— If the VM exit is due to a software exception (due to an execution of INT3 or INTO), the value saved references the INT3 or INTO instruction that caused that exception.

— Suppose that the VM exit is due to a task switch that was caused by execution of CALL, IRET, or JMP or by execution of a software interrupt (INT n) or software exception (due to execution of INT3 or INTO) that encountered a task gate in the IDT. The value saved references the instruction that caused the task switch (CALL, IRET, JMP, INT n, INT3, or INTO).

— Suppose that the VM exit is due to a task switch that was caused by a task gate in the IDT that was encountered for any reason except the direct access by a software interrupt or software exception. The value saved is that which would have been saved in the old task-state segment had the task switch completed normally.

— If the VM exit is due to an execution of MOV to CR8 or WRMSR that reduced the value of bits 7:4 of VTPR (see Section 29.1.1) below that of TPR threshold VM-execution control field (see Section 29.1.2), the value saved references the instruction following the MOV to CR8 or WRMSR.

— If the VM exit was caused by APIC-write emulation (see Section 29.4.3.2) that results from an APIC access as part of instruction execution, the value saved references the instruction following the one whose execution caused the APIC-write emulation.

• The contents of the RSP register are saved into the RSP field.

• With the exception of the resume flag (RF; bit 16), the contents of the RFLAGS register is saved into the RFLAGS field. RFLAGS.RF is saved as follows:

  — If the VM exit is caused directly by an event that would normally be delivered through the IDT, the value saved is that which would appear in the saved RFLAGS image (either that which would be saved on the stack had the event been delivered through a trap or interrupt gate1 or into the old task-state segment had the event been delivered through a task gate) had the event been delivered through the IDT. See below for VM exits due to task switches caused by task gates in the IDT.

  — If the VM exit is caused by a triple fault, the value saved is that which the logical processor would have in RF in the RFLAGS register had the triple fault taken the logical processor to the shutdown state.

  — If the VM exit is caused by a task switch (including one caused by a task gate in the IDT), the value saved is that which would have been saved in the RFLAGS image in the old task-state segment (TSS) had the task switch completed normally without exception.

  — If the VM exit is caused by an attempt to execute an instruction that unconditionally causes VM exits or one that was configured to do with a VM-execution control, the value saved is 0.2

  — For APIC-access VM exits and for VM exits caused by EPT violations EPT misconfigurations, and page-modification log-full events, the value saved depends on whether the VM exit occurred during delivery of an event through the IDT:

    • If the VM exit stored 0 for bit 31 for IDT-vectoring information field (because the VM exit did not occur during delivery of an event through the IDT; see Section 27.2.3), the value saved is 1.

    • If the VM exit stored 1 for bit 31 for IDT-vectoring information field (because the VM exit did occur during delivery of an event through the IDT), the value saved is the value that would have appeared in the saved RFLAGS image had the event been delivered through the IDT (see above).

1. The reference here is to the full value of RIP before any truncation that would occur had the stack width been only 32 bits or 16 bits.

1. The reference here is to the full value of RFLAGS before any truncation that would occur had the stack width been only 32 bits or 16 bits.

2. This is true even if RFLAGS.RF was 1 before the instruction was executed. If, in response to such a VM exit, a VM monitor re-enters the guest to re-execute the instruction that caused the VM exit (for example, after clearing the VM-execution control that caused the VM exit), the instruction may encounter a code breakpoint that has already been processed. A VM monitor can avoid this by setting the guest value of RFLAGS.RF to 1 before resuming guest software.
— For all other VM exits, the value saved is the value RFLAGS.RF had before the VM exit occurred.

### 27.3.4 Saving Non-Register State

Information corresponding to guest non-register state is saved as follows:

- The activity-state field is saved with the logical processor’s activity state before the VM exit.\(^1\) See Section 27.1 for details of how events leading to a VM exit may affect the activity state.

- The interruptibility-state field is saved to reflect the logical processor’s interruptibility before the VM exit. See Section 27.1 for details of how events leading to a VM exit may affect this state. VM exits that end outside system-management mode (SMM) save bit 2 (blocking by SMI) as 0 regardless of the state of such blocking before the VM exit.

Bit 3 (blocking by NMI) is treated specially if the “virtual NMIs” VM-execution control is 1. In this case, the value saved for this field does not indicate the blocking of NMIs but rather the state of virtual-NMI blocking.

- The pending debug exceptions field is saved as clear for all VM exits except the following:
  - A VM exit caused by an INIT signal, a machine-check exception, or a system-management interrupt (SMI).
  - A VM exit with basic exit reason “TPR below threshold”,\(^2\) “virtualized EOI”, “APIC write”, or “monitor trap flag.”
  - VM exits that are not caused by debug exceptions and that occur while there is MOV-SS blocking of debug exceptions.

For VM exits that do not clear the field, the value saved is determined as follows:

- Each of bits 3:0 may be set if it corresponds to a matched breakpoint. This may be true even if the corresponding breakpoint is not enabled in DR7.

- Suppose that a VM exit is due to an INIT signal, a machine-check exception, or an SMI; or that a VM exit has basic exit reason “TPR below threshold” or “monitor trap flag.” In this case, the value saved sets bits corresponding to the causes of any debug exceptions that were pending at the time of the VM exit.

If the VM exit occurs immediately after VM entry, the value saved may match that which was loaded on VM entry (see Section 26.6.3). Otherwise, the following items apply:

- Bit 12 (enabled breakpoint) is set to 1 in any of the following cases:
  - If there was at least one matched data or I/O breakpoint that was enabled in DR7.
  - If it had been set on VM entry, causing there to be valid pending debug exceptions (see Section 26.6.3) and the VM exit occurred before those exceptions were either delivered or lost.
  - If the XBEGIN instruction was executed immediately before the VM exit and advanced debugging of RTM transactional regions had been enabled (see Section 15.3.7, “RTM-Enabled Debugger Support,” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1). (This does not apply to VM exits with basic exit reason “monitor trap flag.”)

In other cases, bit 12 is cleared to 0.

- Bit 14 (BS) is set if RFLAGS.TF = 1 in either of the following cases:
  - IA32_DEBUGCTL.BTF = 0 and the cause of a pending debug exception was the execution of a single instruction.
  - IA32_DEBUGCTL.BTF = 1 and the cause of a pending debug exception was a taken branch.

- Bit 16 (RTM) is set if a debug exception (#DB) or a breakpoint exception (#BP) occurred inside an RTM region while advanced debugging of RTM transactional regions had been enabled. (This does not apply to VM exits with basic exit reason “monitor trap flag.”)

---

1. If this activity state was an inactive state resulting from execution of a specific instruction (HLT or MWAIT), the value saved for RIP by that VM exit will reference the following instruction.

2. This item includes VM exits that occur as a result of certain VM entries (Section 26.6.7).
— Suppose that a VM exit is due to another reason (but not a debug exception) and occurs while there is MOV-SS blocking of debug exceptions. In this case, the value saved sets bits corresponding to the causes of any debug exceptions that were pending at the time of the VM exit. If the VM exit occurs immediately after VM entry (no instructions were executed in VMX non-root operation), the value saved may match that which was loaded on VM entry (see Section 26.6.3). Otherwise, the following items apply:

• Bit 12 (enabled breakpoint) is set to 1 if there was at least one matched data or I/O breakpoint that was enabled in DR7. Bit 12 is also set if it had been set on VM entry, causing there to be valid pending debug exceptions (see Section 26.6.3) and the VM exit occurred before those exceptions were either delivered or lost. In other cases, bit 12 is cleared to 0.

• The setting of bit 14 (BS) is implementation-specific. However, it is not set if RFLAGS.TF = 0 or IA32_DEBUGCTL.BTF = 1.

— The reserved bits in the field are cleared.

• If the “save VMX-preemption timer value” VM-exit control is 1, the value of timer is saved into the VMX-preemption timer-value field. This is the value loaded from this field on VM entry as subsequently decremented (see Section 25.5.1). VM exits due to timer expiration save the value 0. Other VM exits may also save the value 0 if the timer expired during VM exit. (If the “save VMX-preemption timer value” VM-exit control is 0, VM exit does not modify the value of the VMX-preemption timer-value field.)

• If the logical processor supports the 1-setting of the “enable EPT” VM-execution control, values are saved into the four (4) PDPTPE fields as follows:

— If the “enable EPT” VM-execution control is 1 and the logical processor was using PAE paging at the time of the VM exit, the PDPTPE values currently in use are saved:\(^1\)

  • The values saved into bits 11:9 of each of the fields is undefined.
  • If the value saved into one of the fields has bit 0 (present) clear, the value saved into bits 63:1 of that field is undefined. That value need not correspond to the value that was loaded by VM entry or to any value that might have been loaded in VMX non-root operation.
  • If the value saved into one of the fields has bit 0 (present) set, the value saved into bits 63:12 of the field is a guest-physical address.

— If the “enable EPT” VM-execution control is 0 or the logical processor was not using PAE paging at the time of the VM exit, the values saved are undefined.

27.4 SAVING MSRS

After processor state is saved to the guest-state area, values of MSRs may be stored into the VM-exit MSR-store area (see Section 24.7.2). Specifically each entry in that area (up to the number specified in the VM-exit MSR-store count) is processed in order by storing the value of the MSR indexed by bits 31:0 (as they would be read by RDMSR) into bits 127:64. Processing of an entry fails in either of the following cases:

• The value of bits 31:8 is 000008H, meaning that the indexed MSR is one that allows access to an APIC register when the local APIC is in x2APIC mode.

• The value of bits 31:0 indicates an MSR that can be read only in system-management mode (SMM) and the VM exit will not end in SMM. (IA32_SMBASE is an MSR that can be read only in SMM.)

• The value of bits 31:0 indicates an MSR that cannot be saved on VM exits for model-specific reasons. A processor may prevent certain MSRs (based on the value of bits 31:0) from being stored on VM exits, even if they can normally be read by RDMSR. Such model-specific behavior is documented in Chapter 35.

• Bits 63:32 of the entry are not all 0.

• An attempt to read the MSR indexed by bits 31:0 would cause a general-protection exception if executed via RDMSR with CPL = 0.

1. A logical processor uses PAE paging if CR0.PG = 1, CR4.PAE = 1 and IA32_EFER.LMA = 0. See Section 4.4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A. “Enable EPT” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM exit functions as if the “enable EPT” VM-execution control were 0. See Section 24.6.2.
A VMX abort occurs if processing fails for any entry. See Section 27.7.

27.5  LOADING HOST STATE

Processor state is updated on VM exits in the following ways:

• Some state is loaded from or otherwise determined by the contents of the host-state area.
• Some state is determined by VM-exit controls.
• Some state is established in the same way on every VM exit.
• The page-directory pointers are loaded based on the values of certain control registers.

This loading may be performed in any order.

On processors that support Intel 64 architecture, the full values of each 64-bit field loaded (for example, the base address for GDTR) is loaded regardless of the mode of the logical processor before and after the VM exit.

The loading of host state is detailed in Section 27.5.1 to Section 27.5.5. These sections reference VMCS fields that correspond to processor state. Unless otherwise stated, these references are to fields in the host-state area.

A logical processor is in IA-32e mode after a VM exit only if the "host address-space size" VM-exit control is 1. If the logical processor was in IA-32e mode before the VM exit and this control is 0, a VMX abort occurs. See Section 27.7.

In addition to loading host state, VM exits clear address-range monitoring (Section 27.5.6).

After the state loading described in this section, VM exits may load MSRs from the VM-exit MSR-load area (see Section 27.6). This loading occurs only after the state loading described in this section.

27.5.1  Loading Host Control Registers, Debug Registers, MSRs

VM exits load new values for controls registers, debug registers, and some MSRs:

• CR0, CR3, and CR4 are loaded from the CR0 field, the CR3 field, and the CR4 field, respectively, with the following exceptions:
  — The following bits are not modified:
    • For CR0, ET, CD, NW; bits 63:32 (on processors that support Intel 64 architecture), 28:19, 17, and 15:6; and any bits that are fixed in VMX operation (see Section 23.8).\(^1\)
    • For CR3, bits 63:52 and bits in the range 51:32 beyond the processor's physical-address width (they are cleared to 0).\(^2\) (This item applies only to processors that support Intel 64 architecture.)
    • For CR4, any bits that are fixed in VMX operation (see Section 23.8).
  — CR4.PAE is set to 1 if the "host address-space size" VM-exit control is 1.
  — CR4.PCIDE is set to 0 if the "host address-space size" VM-exit control is 0.
• DR7 is set to 400H.
• The following MSRs are established as follows:
  — The IA32_DEBUGCTL MSR is cleared to 00000000_00000000H.
  — The IA32_SYSENTER_CS MSR is loaded from the IA32_SYSENTER_CS field. Since that field has only 32 bits, bits 63:32 of the MSR are cleared to 0.
  — IA32_SYSENTER_ESP MSR and IA32_SYSENTER_EIP MSR are loaded from the IA32_SYSENTER_ESP field and the IA32_SYSENTER_EIP field, respectively.

---

1. Bits 28:19, 17, and 15:6 of CR0 and CR0.ET are unchanged by executions of MOV to CR0. CR0.ET is always 1 and the other bits are always 0.
2. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
If the processor does not support the Intel 64 architecture, these fields have only 32 bits; bits 63:32 of the MSRs are cleared to 0.

If the processor does support the Intel 64 architecture and the processor supports N < 64 linear-address bits, each of bits 63:N is set to the value of bit N−1.¹

— The following steps are performed on processors that support Intel 64 architecture:
  • The MSRs FS.base and GS.base are loaded from the base-address fields for FS and GS, respectively (see Section 27.5.2).
  • The LMA and LME bits in the IA32_EFER MSR are each loaded with the setting of the “host address-space size” VM-exit control.
  — If the “load IA32_PERF_GLOBAL_CTRL” VM-exit control is 1, the IA32_PERF_GLOBAL_CTRL MSR is loaded from the IA32_PERF_GLOBAL_CTRL field. Bits that are reserved in that MSR are maintained with their reserved values.
  — If the “load IA32_PAT” VM-exit control is 1, the IA32_PAT MSR is loaded from the IA32_PAT field. Bits that are reserved in that MSR are maintained with their reserved values.
  — If the “load IA32_EFER” VM-exit control is 1, the IA32_EFER MSR is loaded from the IA32_EFER field. Bits that are reserved in that MSR are maintained with their reserved values.

With the exception of FS.base and GS.base, any of these MSRs is subsequently overwritten if it appears in the VM-exit MSR-load area. See Section 27.6.

27.5.2 Loading Host Segment and Descriptor-Table Registers

Each of the registers CS, SS, DS, ES, FS, GS, and TR is loaded as follows (see below for the treatment of LDTR):
  • The selector is loaded from the selector field. The segment is unusable if its selector is loaded with zero. The checks specified Section 26.3.1.2 limit the selector values that may be loaded. In particular, CS and TR are never loaded with zero and are thus never unusable. SS can be loaded with zero only on processors that support Intel 64 architecture and only if the VM exit is to 64-bit mode (64-bit mode allows use of segments marked unusable).
  • The base address is set as follows:
    — CS. Cleared to zero.
    — SS, DS, and ES. Undefined if the segment is unusable; otherwise, cleared to zero.
    — FS and GS. Undefined (but, on processors that support Intel 64 architecture, canonical) if the segment is unusable and the VM exit is not to 64-bit mode; otherwise, loaded from the base-address field.
    If the processor supports the Intel 64 architecture and the processor supports N < 64 linear-address bits, each of bits 63:N is set to the value of bit N−1.² The values loaded for base addresses for FS and GS are also manifest in the FS.base and GS.base MSRs.
    — TR. Loaded from the host-state area. If the processor supports the Intel 64 architecture and the processor supports N < 64 linear-address bits, each of bits 63:N is set to the value of bit N−1.
  • The segment limit is set as follows:
    — CS. Set to FFFFFFFFH (corresponding to a descriptor limit of FFFFFH and a G-bit setting of 0).
    — SS, DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, set to FFFFFFFFH.
    — TR. Set to 00000067H.
  • The type field and S bit are set as follows:
    — CS. Type set to 11 and S set to 1 (execute/read, accessed, non-conforming code segment).

1. Software can determine the number N by executing CPUID with 80000008H in EAX. The number of linear-address bits supported is returned in bits 15:8 of EAX.
2. Software can determine the number N by executing CPUID with 80000008H in EAX. The number of linear-address bits supported is returned in bits 15:8 of EAX.
— SS, DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, type set to 3 and S set to 1 (read/write, accessed, expand-up data segment).

— TR. Type set to 11 and S set to 0 (busy 32-bit task-state segment).

• The DPL is set as follows:
  — CS, SS, and TR. Set to 0. The current privilege level (CPL) will be 0 after the VM exit completes.
  — DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, set to 0.

• The P bit is set as follows:
  — CS, TR. Set to 1.
  — SS, DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, set to 1.

• On processors that support Intel 64 architecture, CS.L is loaded with the setting of the “host address-space size” VM-exit control. Because the value of this control is also loaded into IA32_EFER.LMA (see Section 27.5.1), no VM exit is ever to compatibility mode (which requires IA32_EFER.LMA = 1 and CS.L = 0).

• D/B.
  — CS. Loaded with the inverse of the setting of the “host address-space size” VM-exit control. For example, if that control is 0, indicating a 32-bit guest, CS.D/B is set to 1.
  — SS. Set to 1.
  — DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, set to 1.
  — TR. Set to 0.

• G.
  — CS. Set to 1.
  — SS, DS, ES, FS, and GS. Undefined if the segment is unusable; otherwise, set to 1.
  — TR. Set to 0.

The host-state area does not contain a selector field for LDTR. LDTR is established as follows on all VM exits: the selector is cleared to 0000H, the segment is marked unusable and is otherwise undefined (although the base address is always canonical).

The base addresses for GDTR and IDTR are loaded from the GDTR base-address field and the IDTR base-address field, respectively. If the processor supports the Intel 64 architecture and the processor supports $N < 64$ linear-address bits, each of bits 63:$N$ of each base address is set to the value of bit N–1 of that base address. The GDTR and IDTR limits are each set to FFFFH.

### 27.5.3 Loading Host RIP, RSP, and RFLAGS

RIP and RSP are loaded from the RIP field and the RSP field, respectively. RFLAGS is cleared, except bit 1, which is always set.

### 27.5.4 Checking and Loading Host Page-Directory-Pointer-Table Entries

If CR0.PG = 1, CR4.PAE = 1, and IA32_EFER.LMA = 0, the logical processor uses PAE paging. See Section 4.4 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A. When in PAE paging is in use, the physical address in CR3 references a table of page-directory-pointer-table entries (PDPTES). A MOV to CR3 when PAE paging is in use checks the validity of the PDPTES and, if they are valid, loads them into the processor (into internal, non-architectural registers).

A VM exit is to a VMM that uses PAE paging if (1) bit 5 (corresponding to CR4.PAE) is set in the CR4 field in the host-state area of the VMCS; and (2) the “host address-space size” VM-exit control is 0. Such a VM exit may check the

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1. On processors that support Intel 64 architecture, the physical-address extension may support more than 36 physical-address bits. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
validity of the PDPTEs referenced by the CR3 field in the host-state area of the VMCS. Such a VM exit must check their validity if either (1) PAE paging was not in use before the VM exit; or (2) the value of CR3 is changing as a result of the VM exit. A VM exit to a VMM that does not use PAE paging must not check the validity of the PDPTEs.

A VM exit that checks the validity of the PDPTEs uses the same checks that are used when CR3 is loaded with MOV to CR3 when PAE paging is in use. If MOV to CR3 would cause a general-protection exception due to the PDPTEs that would be loaded (e.g., because a reserved bit is set), a VMX abort occurs (see Section 27.7). If a VM exit to a VMM that uses PAE does not cause a VMX abort, the PDPTEs are loaded into the processor as would MOV to CR3, using the value of CR3 being load by the VM exit.

27.5.5 Updating Non-Register State

VM exits affect the non-register state of a logical processor as follows:

- A logical processor is always in the active state after a VM exit.
- Event blocking is affected as follows:
  - There is no blocking by STI or by MOV SS after a VM exit.
  - VM exits caused directly by non-maskable interrupts (NMIs) cause blocking by NMI (see Table 24-3). Other VM exits do not affect blocking by NMI. (See Section 27.1 for the case in which an NMI causes a VM exit indirectly.)
- There are no pending debug exceptions after a VM exit.

Section 28.3 describes how the VMX architecture controls how a logical processor manages information in the TLBs and paging-structure caches. The following items detail how VM exits invalidate cached mappings:

- If the "enable VPID" VM-execution control is 0, the logical processor invalidates linear mappings and combined mappings associated with VPID 0000H (for all PCIDs); combined mappings for VPID 0000H are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP).
- VM exits are not required to invalidate any guest-physical mappings, nor are they required to invalidate any linear mappings or combined mappings if the "enable VPID" VM-execution control is 1.

27.5.6 Clearing Address-Range Monitoring

The Intel 64 and IA-32 architectures allow software to monitor a specified address range using the MONITOR and MWAIT instructions. See Section 8.10.4 in the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3A. VM exits clear any address-range monitoring that may be in effect.

27.6 LOADING MSRS

VM exits may load MSRs from the VM-exit MSR-load area (see Section 24.7.2). Specifically each entry in that area (up to the number specified in the VM-exit MSR-load count) is processed in order by loading the MSR indexed by bits 31:0 with the contents of bits 127:64 as they would be written by WRMSR.

Processing of an entry fails in any of the following cases:

- The value of bits 31:0 is either C0000100H (the IA32_FS_BASE MSR) or C0000101H (the IA32_GS_BASE MSR).
- The value of bits 31:8 is 000008H, meaning that the indexed MSR is one that allows access to an APIC register when the local APIC is in x2APIC mode.
- The value of bits 31:0 indicates an MSR that can be written only in system-management mode (SMM) and the VM exit will not end in SMM. (IA32_SMM_MONITOR_CTL is an MSR that can be written only in SMM.)
- The value of bits 31:0 indicates an MSR that cannot be loaded on VM exits for model-specific reasons. A processor may prevent loading of certain MSRs even if they can normally be written by WRMSR. Such model-specific behavior is documented in Chapter 35.
- Bits 63:32 are not all 0.
• An attempt to write bits 127:64 to the MSR indexed by bits 31:0 of the entry would cause a general-protection exception if executed via WRMSR with CPL = 0.\(^1\)

If processing fails for any entry, a VMX abort occurs. See Section 27.7.

If any MSR is being loaded in such a way that would architecturally require a TLB flush, the TLBs are updated so that, after VM exit, the logical processor does not use any translations that were cached before the transition.

### 27.7 VMX ABORTS

A problem encountered during a VM exit leads to a **VMX abort**. A VMX abort takes a logical processor into a shutdown state as described below.

A VMX abort does not modify the VMCS data in the VMCS region of any active VMCS. The contents of these data are thus suspect after the VMX abort.

On a VMX abort, a logical processor saves a nonzero 32-bit VMX-abort indicator field at byte offset 4 in the VMCS region of the VMCS whose misconfiguration caused the failure (see Section 24.2). The following values are used:

1. There was a failure in saving guest MSRs (see Section 27.4).
2. Host checking of the page-directory-pointer-table entries (PDPTEs) failed (see Section 27.5.4).
3. The current VMCS has been corrupted (through writes to the corresponding VMCS region) in such a way that the logical processor cannot complete the VM exit properly.
4. There was a failure on loading host MSRs (see Section 27.6).
5. There was a machine-check event during VM exit (see Section 27.8).
6. The logical processor was in IA-32e mode before the VM exit and the “host address-space size” VM-entry control was 0 (see Section 27.5).

Some of these causes correspond to failures during the loading of state from the host-state area. Because the loading of such state may be done in any order (see Section 27.5) a VM exit that might lead to a VMX abort for multiple reasons (for example, the current VMCS may be corrupt and the host PDPTEs might not be properly configured). In such cases, the VMX-abort indicator could correspond to any one of those reasons.

A logical processor never reads the VMX-abort indicator in a VMCS region and writes it only with one of the nonzero values mentioned above. The VMX-abort indicator allows software on one logical processor to diagnose the VMX-abort on another. For this reason, it is recommended that software running in VMX root operation zero the VMX-abort indicator in the VMCS region of any VMCS that it uses.

After saving the VMX-abort indicator, operation of a logical processor experiencing a VMX abort depends on whether the logical processor is in SMX operation:²

- If the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs. The error code used is 000DH, indicating “VMX abort.” See Intel® Trusted Execution Technology Measured Launched Environment Programming Guide.

- If the logical processor is outside SMX operation, it issues a special bus cycle (to notify the chipset) and enters the **VMX-abort shutdown state**. RESET is the only event that wakes a logical processor from the VMX-abort shutdown state. The following events do not affect a logical processor in this state: machine-check events; INIT signals; external interrupts; non-maskable interrupts (NMIs); start-up IPIs (SIPIs); and system-management interrupts (SMIs).

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\(^1\) Note the following about processors that support Intel 64 architecture. If CR0.PG = 1, WRMSR to the IA32_EFER MSR causes a general-protection exception if it would modify the LME bit. Since CR0.PG is always 1 in VMX operation, the IA32_EFER MSR should not be included in the VM-exit MSR-load area for the purpose of modifying the LME bit.

\(^2\) A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B.
### 27.8 MACHINE-CHECK EVENTS DURING VM EXIT

If a machine-check event occurs during VM exit, one of the following occurs:

- The machine-check event is handled as if it occurred before the VM exit:
  - If CR4.MCE = 0, operation of the logical processor depends on whether the logical processor is in SMX operation:
    - If the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs. The error code used is 000CH, indicating "unrecoverable machine-check condition."
    - If the logical processor is outside SMX operation, it goes to the shutdown state.
  - If CR4.MCE = 1, a machine-check exception (#MC) is generated:
    - If bit 18 (#MC) of the exception bitmap is 0, the exception is delivered through the guest IDT.
    - If bit 18 of the exception bitmap is 1, the exception causes a VM exit.
- The machine-check event is handled after VM exit completes:
  - If the VM exit ends with CR4.MCE = 0, operation of the logical processor depends on whether the logical processor is in SMX operation:
    - If the logical processor is in SMX operation, an Intel® TXT shutdown condition occurs with error code 000CH (unrecoverable machine-check condition).
    - If the logical processor is outside SMX operation, it goes to the shutdown state.
  - If the VM exit ends with CR4.MCE = 1, a machine-check exception (#MC) is delivered through the host IDT.
- A VMX abort is generated (see Section 27.7). The logical processor blocks events as done normally in VMX abort. The VMX abort indicator is 5, for "machine-check event during VM exit."

The first option is not used if the machine-check event occurs after any host state has been loaded. The second option is used only if VM entry is able to load all host state.

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1. A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2B.*
VM EXITS
CHAPTER 28
VMX SUPPORT FOR ADDRESS TRANSLATION

The architecture for VMX operation includes two features that support address translation: virtual-processor identifiers (VPIDs) and the extended page-table mechanism (EPT). VPIDs are a mechanism for managing translations of linear addresses. EPT defines a layer of address translation that augments the translation of linear addresses.

Section 28.1 details the architecture of VPIDs. Section 28.2 provides the details of EPT. Section 28.3 explains how a logical processor may cache information from the paging structures, how it may use that cached information, and how software can managed the cached information.

28.1 VIRTUAL PROCESSOR IDENTIFIERS (VPIDS)

The original architecture for VMX operation required VMX transitions to flush the TLBs and paging-structure caches. This ensured that translations cached for the old linear-address space would not be used after the transition.

Virtual-processor identifiers (VPIDs) introduce to VMX operation a facility by which a logical processor may cache information for multiple linear-address spaces. When VPIDs are used, VMX transitions may retain cached information and the logical processor switches to a different linear-address space.

Section 28.3 details the mechanisms by which a logical processor manages information cached for multiple address spaces. A logical processor may tag some cached information with a 16-bit VPID. This section specifies how the current VPID is determined at any point in time:

• The current VPID is 0000H in the following situations:
  — Outside VMX operation. (This includes operation in system-management mode under the default treatment of SMIs and SMM with VMX operation; see Section 34.14.)
  — In VMX root operation.
  — In VMX non-root operation when the “enable VPID” VM-execution control is 0.
• If the logical processor is in VMX non-root operation and the “enable VPID” VM-execution control is 1, the current VPID is the value of the VPID VM-execution control field in the VMCS. (VM entry ensures that this value is never 0000H; see Section 26.2.1.1.)

VPIDs and PCIDs (see Section 4.10.1) can be used concurrently. When this is done, the processor associates cached information with both a VPID and a PCID. Such information is used only if the current VPID and PCID both match those associated with the cached information.

28.2 THE EXTENDED PAGE TABLE MECHANISM (EPT)

The extended page-table mechanism (EPT) is a feature that can be used to support the virtualization of physical memory. When EPT is in use, certain addresses that would normally be treated as physical addresses (and used to access memory) are instead treated as guest-physical addresses. Guest-physical addresses are translated by traversing a set of EPT paging structures to produce physical addresses that are used to access memory.

• Section 28.2.1 gives an overview of EPT.
• Section 28.2.2 describes operation of EPT-based address translation.
• Section 28.2.3 discusses VM exits that may be caused by EPT.
• Section 28.2.6 describes interactions between EPT and memory typing.

28.2.1 EPT Overview

EPT is used when the “enable EPT” VM-execution control is 1. It translates the guest-physical addresses used in VMX non-root operation and those used by VM entry for event injection.
The translation from guest-physical addresses to physical addresses is determined by a set of EPT paging structures. The EPT paging structures are similar to those used to translate linear addresses while the processor is in IA-32e mode. Section 28.2.2 gives the details of the EPT paging structures.

If CR0.PG = 1, linear addresses are translated through paging structures referenced through control register CR3. While the “enable EPT” VM-execution control is 1, these are called guest paging structures. There are no guest paging structures if CR0.PG = 0.1

When the “enable EPT” VM-execution control is 1, the identity of guest-physical addresses depends on the value of CR0.PG:

• If CR0.PG = 0, each linear address is treated as a guest-physical address.
• If CR0.PG = 1, guest-physical addresses are those derived from the contents of control register CR3 and the guest paging structures. (This includes the values of the PDPTEs, which logical processors store in internal, non-architectural registers.) The latter includes (in page-table entries and in other paging-structure entries for which bit 7—PS—is 1) the addresses to which linear addresses are translated by the guest paging structures.

If CR0.PG = 1, the translation of a linear address to a physical address requires multiple translations of guest-physical addresses using EPT. Assume, for example, that CR4.PAE = CR4.PSE = 0. The translation of a 32-bit linear address then operates as follows:

• Bits 31:22 of the linear address select an entry in the guest page directory located at the guest-physical address in CR3. The guest-physical address of the guest page-directory entry (PDE) is translated through EPT to determine the guest PDE’s physical address.
• Bits 21:12 of the linear address select an entry in the guest page table located at the guest-physical address in the guest PDE. The guest-physical address of the guest page-table entry (PTE) is translated through EPT to determine the guest PTE’s physical address.
• Bits 11:0 of the linear address is the offset in the page frame located at the guest-physical address in the guest PTE. The guest-physical address determined by this offset is translated through EPT to determine the physical address to which the original linear address translates.

In addition to translating a guest-physical address to a physical address, EPT specifies the privileges that software is allowed when accessing the address. Attempts at disallowed accesses are called EPT violations and cause VM exits. See Section 28.2.3.

A logical processor uses EPT to translate guest-physical addresses only when those addresses are used to access memory. This principle implies the following:

• The MOV to CR3 instruction loads CR3 with a guest-physical address. Whether that address is translated through EPT depends on whether PAE paging is being used.2
  — If PAE paging is not being used, the instruction does not use that address to access memory and does not cause it to be translated through EPT. (If CR0.PG = 1, the address will be translated through EPT on the next memory accessing using a linear address.)
  — If PAE paging is being used, the instruction loads the four (4) page-directory-pointer-table entries (PDPTEs) from that address and it does cause the address to be translated through EPT.
• Section 4.4.1 identifies executions of MOV to CR0 and MOV to CR4 that load the PDPTEs from the guest-physical address in CR3. Such executions cause that address to be translated through EPT.
• The PDPTEs contain guest-physical addresses. The instructions that load the PDPTEs (see above) do not use those addresses to access memory and do not cause them to be translated through EPT. The address in a PDPTE will be translated through EPT on the next memory accessing using a linear address that uses that PDPTE.

1. “Enable EPT” is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, the logical processor operates as if the “enable EPT” VM-execution control were 0. See Section 24.6.2.
1. If the capability MSR IA32_VMX_CRO_FIXE0D reports that CR0.PG must be 1 in VMX operation, CR0.PG can be 0 in VMX non-root operation only if the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
2. A logical processor uses PAE paging if CR0.PG = 1, CR4.PAE = 1 and IA32_EFER.LMA = 0. See Section 4.4 in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
28.2.2 EPT Translation Mechanism

The EPT translation mechanism uses only bits 47:0 of each guest-physical address.\(^1\) It uses a page-walk length of 4, meaning that at most 4 EPT paging-structure entries are accessed to translate a guest-physical address.\(^2\)

These 48 bits are partitioned by the logical processor to traverse the EPT paging structures:

- A 4-KByte naturally aligned EPT PML4 table is located at the physical address specified in bits 51:12 of the extended-page-table pointer (EPTP), a VM-execution control field (see Table 24-8 in Section 24.6.11). An EPT PML4 table comprises 512 64-bit entries (EPT PML4Es). An EPT PML4E is selected using the physical address defined as follows:
  - Bits 63:52 are all 0.
  - Bits 51:12 are from the EPTP.
  - Bits 11:3 are bits 47:39 of the guest-physical address.
  - Bits 2:0 are all 0.

Because an EPT PML4E is identified using bits 47:39 of the guest-physical address, it controls access to a 512-GByte region of the guest-physical-address space. The format of an EPT PML4E is given in Table 28-1.

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 512-GByte region controlled by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 512-GByte region controlled by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 512-GByte region controlled by this entry</td>
</tr>
<tr>
<td>7:3</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 512-GByte region controlled by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:9</td>
<td>Ignored</td>
</tr>
<tr>
<td>(N-1):12</td>
<td>Physical address of 4-KByte aligned EPT page-directory-pointer table referenced by this entry(^1)</td>
</tr>
<tr>
<td>51:N</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>63:52</td>
<td>Ignored</td>
</tr>
</tbody>
</table>

**NOTES:**

1. \(N\) is the physical-address width supported by the processor. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.

2. A 4-KByte naturally aligned EPT page-directory-pointer table is located at the physical address specified in bits 51:12 of the EPT PML4E. An EPT page-directory-pointer table comprises 512 64-bit entries (EPT PDPTEs). An EPT PDPTE is selected using the physical address defined as follows:
  - Bits 63:52 are all 0.
  - Bits 51:12 are from the EPT PML4E.

---

1. No processors supporting the Intel 64 architecture support more than 48 physical-address bits. Thus, no such processor can produce a guest-physical address with more than 48 bits. An attempt to use such an address causes a page fault. An attempt to load CR3 with such an address causes a general-protection fault. If PAE paging is being used, an attempt to load CR3 that would load a PDPT with such an address causes a general-protection fault.

2. Future processors may include support for other EPT page-walk lengths. Software should read the VMX capability MSR IA32_VMX_EPT_VPID_CAP (see Appendix A.10) to determine what EPT page-walk lengths are supported.
VMX SUPPORT FOR ADDRESS TRANSLATION

— Bits 11:3 are bits 38:30 of the guest-physical address.
— Bits 2:0 are all 0.

Because an EPT PDPT is identified using bits 47:30 of the guest-physical address, it controls access to a 1-GByte region of the guest-physical-address space. Use of the EPT PDPT depends on the value of bit 7 in that entry:

• If bit 7 of the EPT PDPT is 1, the EPT PDPT maps a 1-GByte page. The final physical address is computed as follows:
  — Bits 63:52 are all 0.
  — Bits 51:30 are from the EPT PDPT.
  — Bits 29:0 are from the original guest-physical address.
  The format of an EPT PDPT that maps a 1-GByte page is given in Table 28-2.

• If bit 7 of the EPT PDPT is 0, a 4-KByte naturally aligned EPT page directory is located at the physical address specified in bits 51:12 of the EPT PDPT. The format of an EPT PDPT that references an EPT page directory is given in Table 28-3.

1. Not all processors allow bit 7 of an EPT PDPT to be set to 1. Software should read the VMX capability MSR IA32_VMX_EPT_VPID_CAP (see Appendix A.10) to determine whether this is allowed.

Table 28-2. Format of an EPT Page-Directory-Pointer-Table Entry (PDPT) that Maps a 1-GByte Page

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 1-GByte page referenced by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 1-GByte page referenced by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 1-GByte page referenced by this entry</td>
</tr>
<tr>
<td>5:3</td>
<td>EPT memory type for this 1-GByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>6</td>
<td>Ignore PAT memory type for this 1-GByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>7</td>
<td>Must be 1 (otherwise, this entry references an EPT page directory)</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 1-GByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>9</td>
<td>If bit 6 of EPTP is 1, dirty flag for EPT; indicates whether software has written to the 1-GByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:10</td>
<td>Ignored</td>
</tr>
<tr>
<td>29:12</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>(N–1):30</td>
<td>Physical address of the 1-GByte page referenced by this entry</td>
</tr>
<tr>
<td>51:N</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>62:52</td>
<td>Ignored</td>
</tr>
<tr>
<td>63</td>
<td>Suppress #VE. If the “EPT-violation #VE” VM-execution control is 1, EPT violations caused by accesses to this page are convertible to virtualization exceptions only if this bit is 0 (see Section 25.5.6.1). If “EPT-violation #VE” VM-execution control is 0, this bit is ignored.</td>
</tr>
</tbody>
</table>

NOTES:
1. N is the physical-address width supported by the logical processor.

1. Not all processors allow bit 7 of an EPT PDPT to be set to 1. Software should read the VMX capability MSR IA32_VMX_EPT_VPID_CAP (see Appendix A.10) to determine whether this is allowed.
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An EPT page-directory comprises 512 64-bit entries (PDEs). An EPT PDE is selected using the physical address defined as follows:
— Bits 63:52 are all 0.
— Bits 51:12 are from the EPT PDPTE.
— Bits 11:3 are bits 29:21 of the guest-physical address.
— Bits 2:0 are all 0.

Because an EPT PDE is identified using bits 47:21 of the guest-physical address, it controls access to a 2-MByte region of the guest-physical-address space. Use of the EPT PDE depends on the value of bit 7 in that entry:
• If bit 7 of the EPT PDE is 1, the EPT PDE maps a 2-MByte page. The final physical address is computed as follows:
  — Bits 63:52 are all 0.
  — Bits 51:21 are from the EPT PDE.
  — Bits 20:0 are from the original guest-physical address.
• If bit 7 of the EPT PDE is 0, a 4-KByte naturally aligned EPT page table is located at the physical address specified in bits 51:12 of the EPT PDE. The format of an EPT PDE that references an EPT page table is given in Table 28-5.

An EPT page table comprises 512 64-bit entries (PTEs). An EPT PTE is selected using a physical address defined as follows:
— Bits 63:52 are all 0.
— Bits 51:12 are from the EPT PDE.
— Bits 11:3 are bits 20:12 of the guest-physical address.
— Bits 2:0 are all 0.

Because an EPT PTE is identified using bits 47:12 of the guest-physical address, every EPT PTE maps a 4-KByte page. The final physical address is computed as follows:
— Bits 63:52 are all 0.

Table 28-3. Format of an EPT Page-Directory-Pointer-Table Entry (PDPTE) that References an EPT Page Directory

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 1-GByte region controlled by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 1-GByte region controlled by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 1-GByte region controlled by this entry</td>
</tr>
<tr>
<td>7:3</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 1-GByte region controlled by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:9</td>
<td>Ignored</td>
</tr>
<tr>
<td>(N-1):12</td>
<td>Physical address of 4-KByte aligned EPT page directory referenced by this entry¹</td>
</tr>
<tr>
<td>51:N</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>63:52</td>
<td>Ignored</td>
</tr>
</tbody>
</table>

NOTES:
1. N is the physical-address width supported by the logical processor.

An EPT page-directory comprises 512 64-bit entries (PDEs). An EPT PDE is selected using the physical address defined as follows:
— Bits 63:52 are all 0.
— Bits 51:12 are from the EPT PDPTE.
— Bits 11:3 are bits 29:21 of the guest-physical address.
— Bits 2:0 are all 0.

Because an EPT PDE is identified using bits 47:21 of the guest-physical address, it controls access to a 2-MByte region of the guest-physical-address space. Use of the EPT PDE depends on the value of bit 7 in that entry:
• If bit 7 of the EPT PDE is 1, the EPT PDE maps a 2-MByte page. The final physical address is computed as follows:
  — Bits 63:52 are all 0.
  — Bits 51:21 are from the EPT PDE.
  — Bits 20:0 are from the original guest-physical address.
• If bit 7 of the EPT PDE is 0, a 4-KByte naturally aligned EPT page table is located at the physical address specified in bits 51:12 of the EPT PDE. The format of an EPT PDE that references an EPT page table is given in Table 28-5.

An EPT page table comprises 512 64-bit entries (PTEs). An EPT PTE is selected using a physical address defined as follows:
— Bits 63:52 are all 0.
— Bits 51:12 are from the EPT PDE.
— Bits 11:3 are bits 20:12 of the guest-physical address.
— Bits 2:0 are all 0.

Because an EPT PTE is identified using bits 47:12 of the guest-physical address, every EPT PTE maps a 4-KByte page. The final physical address is computed as follows:
— Bits 63:52 are all 0.
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Table 28-4. Format of an EPT Page-Directory Entry (PDE) that Maps a 2-MByte Page

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 2-MByte page referenced by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 2-MByte page referenced by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 2-MByte page referenced by this entry</td>
</tr>
<tr>
<td>5:3</td>
<td>EPT memory type for this 2-MByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>6</td>
<td>Ignore PAT memory type for this 2-MByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>7</td>
<td>Must be 1 (otherwise, this entry references an EPT page table)</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 2-MByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>9</td>
<td>If bit 6 of EPTP is 1, dirty flag for EPT; indicates whether software has written to the 2-MByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:10</td>
<td>Ignored</td>
</tr>
<tr>
<td>20:12</td>
<td>Reserved (must be 0)</td>
</tr>
</tbody>
</table>
| (N–1):21        | Physical address of the 2-MByte page referenced by this entry

— Bits 51:12 are from the EPT PTE.
— Bits 11:0 are from the original guest-physical address.

The format of an EPT PTE is given in Table 28-6.

If bits 2:0 of an EPT paging-structure entry are all 0, the entry is not present. The processor ignores bits 62:3 and uses the entry neither to reference another EPT paging-structure entry nor to produce a physical address. A reference using a guest-physical address whose translation encounters an EPT paging-structure that is not present causes an EPT violation (see Section 28.2.3.2). (If the “EPT-violation #VE” VM-execution control is 1, the EPT violation is convertible to a virtualization exception only if this bit is 0 (see Section 25.5.6.1). If “EPT-violation #VE” VM-execution control is 0, this bit is ignored.)

The discussion above describes how the EPT paging structures reference each other and how the logical processor traverses those structures when translating a guest-physical address. It does not cover all details of the translation process. Additional details are provided as follows:

- Situations in which the translation process may lead to VM exits (sometimes before the process completes) are described in Section 28.2.3.
- Interactions between the EPT translation mechanism and memory typing are described in Section 28.2.6.

Figure 28-1 gives a summary of the formats of the EPTP and the EPT paging-structure entries. For the EPT paging structure entries, it identifies separately the format of entries that map pages, those that reference other EPT paging structures, and those that do neither because they are “not present”; bits 2:0 and bit 7 are highlighted because they determine how a paging-structure entry is used.

NOTES:

1. N is the physical-address width supported by the logical processor.
28.2.3 EPT-Induced VM Exits

Accesses using guest-physical addresses may cause VM exits due to EPT misconfigurations, EPT violations, and page-modification log-full events. An **EPT misconfiguration** occurs when, in the course of translating a guest-physical address, the logical processor encounters an EPT paging-structure entry that contains an unsupported value (see Section 28.2.3.1). An **EPT violation** occurs when there is no EPT misconfiguration but the EPT paging-structure entries disallow an access using the guest-physical address (see Section 28.2.3.2). A **page-modification log-full event** occurs when the logical processor determines a need to create a page-modification log entry and the current log is full (see Section 28.2.5).

These events occur only due to an attempt to access memory with a guest-physical address. Loading CR3 with a guest-physical address with the MOV to CR3 instruction can cause neither an EPT configuration nor an EPT violation until that address is used to access a paging structure.1

If the “EPT-violation #VE” VM-execution control is 1, certain EPT violations may cause virtualization exceptions instead of VM exits. See Section 25.5.6.1.

### 28.2.3.1 EPT Misconfigurations

An EPT misconfiguration occurs if any of the following is identified while translating a guest-physical address:

- The value of bits 2:0 of an EPT paging-structure entry is either 010b (write-only) or 110b (write/execute).
- The value of bits 2:0 of an EPT paging-structure entry is 100b (execute-only) and this value is not supported by the logical processor. Software should read the VMX capability MSR IA32_VMX_EPT_VPID_CAP to determine whether this value is supported (see Appendix A.10).1
- The value of bits 2:0 of an EPT paging-structure entry is not 000b (the entry is present) and one of the following holds:
  - The logical processor is using PAE paging—because CR0.PG = CR4.PAE = 1 and IA32_EFER.LMA = 0—the MOV to CR3 instruction loads the PDPTes from memory using the guest-physical address being loaded into CR3. In this case, therefore, the MOV to CR3 instruction may cause an EPT misconfiguration, an EPT violation, or a page-modification log-full event.

#### Table 28-5. Format of an EPT Page-Directory Entry (PDE) that References an EPT Page Table

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 2-MByte region controlled by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 2-MByte region controlled by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 2-MByte region controlled by this entry</td>
</tr>
<tr>
<td>6:3</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>7</td>
<td>Must be 0 (otherwise, this entry maps a 2-MByte page)</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 2-MByte region controlled by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:9</td>
<td>Ignored</td>
</tr>
<tr>
<td>(N–1):12</td>
<td>Physical address of 4-KByte aligned EPT page table referenced by this entry1</td>
</tr>
<tr>
<td>51:N</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>63:52</td>
<td>Ignored</td>
</tr>
</tbody>
</table>

**NOTES:**

1. N is the physical-address width supported by the logical processor.

1. If the logical processor is using PAE paging—because CR0.PG = CR4.PAE = 1 and IA32_EFER.LMA = 0—the MOV to CR3 instruction loads the PDPTes from memory using the guest-physical address being loaded into CR3. In this case, therefore, the MOV to CR3 instruction may cause an EPT misconfiguration, an EPT violation, or a page-modification log-full event.
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28.2.2 EPT Violations

An EPT violation may occur during an access using a guest-physical address whose translation does not cause an EPT misconfiguration. An EPT violation occurs in any of the following situations:

- Translation of the guest-physical address encounters an EPT paging-structure entry that is not present (see Section 28.2.2).
- The access is a data read and bit 0 was clear in any of the EPT paging-structure entries used to translate the guest-physical address. Reads by the logical processor of guest paging structures to translate a linear address are considered to be data reads.

Table 28-6. Format of an EPT Page-Table Entry that Maps a 4-KByte Page

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Read access; indicates whether reads are allowed from the 4-KByte page referenced by this entry</td>
</tr>
<tr>
<td>1</td>
<td>Write access; indicates whether writes are allowed to the 4-KByte page referenced by this entry</td>
</tr>
<tr>
<td>2</td>
<td>Execute access; indicates whether instruction fetches are allowed from the 4-KByte page referenced by this entry</td>
</tr>
<tr>
<td>5:3</td>
<td>EPT memory type for this 4-KByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>6</td>
<td>Ignore PAT memory type for this 4-KByte page (see Section 28.2.6)</td>
</tr>
<tr>
<td>7</td>
<td>Ignored</td>
</tr>
<tr>
<td>8</td>
<td>If bit 6 of EPTP is 1, accessed flag for EPT; indicates whether software has accessed the 4-KByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>9</td>
<td>If bit 6 of EPTP is 1, dirty flag for EPT; indicates whether software has written to the 4-KByte page referenced by this entry (see Section 28.2.4). Ignored if bit 6 of EPTP is 0</td>
</tr>
<tr>
<td>11:10</td>
<td>Ignored</td>
</tr>
<tr>
<td>(N–1):12</td>
<td>Physical address of the 4-KByte page referenced by this entry</td>
</tr>
<tr>
<td>51:N</td>
<td>Reserved (must be 0)</td>
</tr>
<tr>
<td>62:52</td>
<td>Ignored</td>
</tr>
<tr>
<td>63</td>
<td>Suppress #VE. If the “EPT-violation #VE” VM-execution control is 1, EPT violations caused by accesses to this page are convertible to virtualization exceptions only if this bit is 0 (see Section 25.5.6.1). If “EPT-violation #VE” VM-execution control is 0, this bit is ignored.</td>
</tr>
</tbody>
</table>

NOTES:

1. N is the physical-address width supported by the logical processor.

- A reserved bit is set. This includes the setting of a bit in the range 51:12 that is beyond the logical processor’s physical-address width.¹ See Section 28.2.2 for details of which bits are reserved in which EPT paging-structure entries.
- The entry is the last one used to translate a guest physical address (either an EPT PDE with bit 7 set to 1 or an EPT PTE) and the value of bits 5:3 (EPT memory type) is 2, 3, or 7 (these values are reserved).

EPT misconfigurations result when an EPT paging-structure entry is configured with settings reserved for future functionality. Software developers should be aware that such settings may be used in the future and that an EPT paging-structure entry that causes an EPT misconfiguration on one processor might not do so in the future.

28.2.3.2 EPT Violations

An EPT violation may occur during an access using a guest-physical address whose translation does not cause an EPT misconfiguration. An EPT violation occurs in any of the following situations:

- Translation of the guest-physical address encounters an EPT paging-structure entry that is not present (see Section 28.2.2).
- The access is a data read and bit 0 was clear in any of the EPT paging-structure entries used to translate the guest-physical address. Reads by the logical processor of guest paging structures to translate a linear address are considered to be data reads.

¹. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
The access is a data write and bit 1 was clear in any of the EPT paging-structure entries used to translate the
guest-physical address. Writes by the logical processor to guest paging structures to update accessed and dirty
flags are considered to be data writes.

If bit 6 of the EPT pointer (EPTP) is 1 (enabling accessed and dirty flags for EPT), processor accesses to guest
paging-structure entries are treated as writes with regard to EPT violations. Thus, if bit 1 is clear in any of the
EPT paging-structure entries used to translate the guest-physical address of a guest paging-structure entry, an
attempt to use that entry to translate a linear address causes an EPT violation.

(This does not apply to loads of the PDPTE registers by the MOV to CR instruction for PAE paging; see Section
4.4.1. Those loads of guest PDPTEs are treated as reads and do not cause EPT violations due to a guest-
physical address not being writable.)

The access is an instruction fetch and bit 2 was clear in any of the EPT paging-structure entries used to
translate the guest-physical address.

---

NOTES:
1. M is an abbreviation for MAXPHYADDR.
2. See Section 24.6.11 for details of the EPTP.
3. Suppress #VE. If the “EPT-violation #VE” VM-execution control is 0, this bit is ignored.

- The access is a data write and bit 1 was clear in any of the EPT paging-structure entries used to translate the
guest-physical address. Writes by the logical processor to guest paging structures to update accessed and dirty
flags are considered to be data writes.

If bit 6 of the EPT pointer (EPTP) is 1 (enabling accessed and dirty flags for EPT), processor accesses to guest
paging-structure entries are treated as writes with regard to EPT violations. Thus, if bit 1 is clear in any of the
EPT paging-structure entries used to translate the guest-physical address of a guest paging-structure entry, an
attempt to use that entry to translate a linear address causes an EPT violation.

(This does not apply to loads of the PDPTE registers by the MOV to CR instruction for PAE paging; see Section
4.4.1. Those loads of guest PDPTEs are treated as reads and do not cause EPT violations due to a guest-
physical address not being writable.)

- The access is an instruction fetch and bit 2 was clear in any of the EPT paging-structure entries used to
translate the guest-physical address.
28.2.3.3 Prioritization of EPT Misconfigurations and EPT Violations

The translation of a linear address to a physical address requires one or more translations of guest-physical addresses using EPT (see Section 28.2.1). This section specifies the relative priority of EPT-induced VM exits with respect to each other and to other events that may be encountered when accessing memory using a linear address.

For an access to a guest-physical address, determination of whether an EPT misconfiguration or an EPT violation occurs is based on an iterative process:

1. An EPT paging-structure entry is read (initially, this is an EPT PML4 entry):
   a. If the entry is not present (bits 2:0 are all 0), an EPT violation occurs.
   b. If the entry is present but its contents are not configured properly (see Section 28.2.3.1), an EPT misconfiguration occurs.
   c. If the entry is present and its contents are configured properly, operation depends on whether the entry references another EPT paging structure (whether it is an EPT PDE with bit 7 set to 1 or an EPT PTE):
      i) If the entry does reference another EPT paging structure, an entry from that structure is accessed; step 1 is executed for that other entry.
      ii) Otherwise, the entry is used to produce the ultimate physical address (the translation of the original guest-physical address); step 2 is executed.

2. Once the ultimate physical address is determined, the privileges determined by the EPT paging-structure entries are evaluated:
   a. If the access to the guest-physical address is not allowed by these privileges (see Section 28.2.3.2), an EPT violation occurs.
   b. If the access to the guest-physical address is allowed by these privileges, memory is accessed using the ultimate physical address.

If CR0.PG = 1, the translation of a linear address is also an iterative process, with the processor first accessing an entry in the guest paging structure referenced by the guest-physical address in CR3 (or, if PAE paging is in use, the guest-physical address in the appropriate PDPTE register), then accessing an entry in another guest paging structure referenced by the guest-physical address in the first guest paging-structure entry, etc. Each guest-physical address is itself translated using EPT and may cause an EPT-induced VM exit. The following items detail how page faults and EPT-induced VM exits are recognized during this iterative process:

1. An attempt is made to access a guest paging-structure entry with a guest-physical address (initially, the address in CR3 or PDPTE register):
   a. If the access fails because of an EPT misconfiguration or an EPT violation (see above), an EPT-induced VM exit occurs.
   b. If the access does not cause an EPT-induced VM exit, bit 0 (the present flag) of the entry is consulted:
      i) If the present flag is 0 or any reserved bit is set, a page fault occurs.
      ii) If the present flag is 1, no reserved bit is set, operation depends on whether the entry references another guest paging structure (whether it is a guest PDE with PS = 1 or a guest PTE):
         • If the entry does reference another guest paging structure, an entry from that structure is accessed; step 1 is executed for that other entry.
         • Otherwise, the entry is used to produce the ultimate guest-physical address (the translation of the original linear address); step 2 is executed.

2. Once the ultimate guest-physical address is determined, the privileges determined by the guest paging-structure entries are evaluated:
   a. If the access to the linear address is not allowed by these privileges (e.g., it was a write to a read-only page), a page fault occurs.
   b. If the access to the linear address is allowed by these privileges, an attempt is made to access memory at the ultimate guest-physical address:

1. This is a simplification of the more detailed description given in Section 28.2.2.
28.2.4 Accessed and Dirty Flags for EPT

The Intel 64 architecture supports accessed and dirty flags in ordinary paging-structure entries (see Section 4.8). Some processors also support corresponding flags in EPT paging-structure entries. Software should read the VMX capability MSR IA32_VMX_EPT_VPID_CAP (see Appendix A.10) to determine whether the processor supports this feature.

Software can enable accessed and dirty flags for EPT using bit 6 of the extended-page-table pointer (EPTP), a VM-execution control field (see Table 24-8 in Section 24.6.11). If this bit is 1, the processor will set the accessed and dirty flags for EPT as described below. In addition, setting this flag causes processor accesses to guest paging-structure entries to be treated as writes (see below and Section 28.2.3.2).

For any EPT paging-structure entry that is used during guest-physical-address translation, bit 8 is the accessed flag. For a EPT paging-structure entry that maps a page (as opposed to referencing another EPT paging structure), bit 9 is the dirty flag.

Whenever the processor uses an EPT paging-structure entry as part of guest-physical-address translation, it sets the accessed flag in that entry (if it is not already set).

Whenever there is a write to a guest-physical address, the processor sets the dirty flag (if it is not already set) in the EPT paging-structure entry that identifies the final physical address for the guest-physical address (either an EPT PTE or an EPT paging-structure entry in which bit 7 is 1).

When accessed and dirty flags for EPT are enabled, processor accesses to guest paging-structure entries are treated as writes (see Section 28.2.3.2). Thus, such an access will cause the processor to set the dirty flag in the EPT paging-structure entry that identifies the final physical address of the guest paging-structure entry.

(This does not apply to loads of the PDPT registers for PAE paging by the MOV to CR instruction; see Section 4.4.1. Those loads of guest PDPTes are treated as reads and do not cause the processor to set the dirty flag in any EPT paging-structure entry.)

These flags are “sticky,” meaning that, once set, the processor does not clear them; only software can clear them.

A processor may cache information from the EPT paging-structure entries in TLBs and paging-structure caches (see Section 28.3). This fact implies that, if software changes an accessed flag or a dirty flag from 1 to 0, the processor might not set the corresponding bit in memory on a subsequent access using an affected guest-physical address.

28.2.5 Page-Modification Logging

When accessed and dirty flags for EPT are enabled, software can track writes to guest-physical addresses using a feature called page-modification logging.

Software can enable page-modification logging by setting the "enable PML" VM-execution control (see Table 24-7 in Section 24.6.2). When this control is 1, the processor adds entries to the page-modification log as described below. The page-modification log is a 4-KByte region of memory located at the physical address in the PML address VM-execution control field. The page-modification log consists of 512 64-bit entries; the PML index VM-execution control field indicates the next entry to use.

Before allowing a guest-physical access, the processor may determine that it first needs to set an accessed or dirty flag for EPT (see Section 28.2.4). When this happens, the processor examines the PML index. If the PML index is
not in the range 0–511, there is a page-modification log-full event and a VM exit occurs. In this case, the accessed or dirty flag is not set, and the guest-physical access that triggered the event does not occur.

If instead the PML index is in the range 0–511, the processor proceeds to update accessed or dirty flags for EPT as described in Section 28.2.4. If the processor updated a dirty flag for EPT (changing it from 0 to 1), it then operates as follows:

1. The guest-physical address of the access is written to the page-modification log. Specifically, the guest-physical address is written to physical address determined by adding 8 times the PML index to the PML address. Bits 11:0 of the value written are always 0 (the guest-physical address written is thus 4-KByte aligned).
2. The PML index is decremented by 1 (this may cause the value to transition from 0 to FFFFH).

Because the processor decrements the PML index with each log entry, the value may transition from 0 to FFFFH. At that point, no further logging will occur, as the processor will determine that the PML index is not in the range 0–511 and will generate a page-modification log-full event (see above).

### 28.2.6 EPT and Memory Typing

This section specifies how a logical processor determines the memory type used for a memory access while EPT is in use. (See Chapter 11, “Memory Cache Control” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A for details of memory typing in the Intel 64 architecture.) Section 28.2.6.1 explains how the memory type is determined for accesses to the EPT paging structures. Section 28.2.6.2 explains how the memory type is determined for an access using a guest-physical address that is translated using EPT.

#### 28.2.6.1 Memory Type Used for Accessing EPT Paging Structures

This section explains how the memory type is determined for accesses to the EPT paging structures. The determination is based first on the value of bit 30 (cache disable—CD) in control register CR0:

- If CR0.CD = 0, the memory type used for any such reference is the EPT paging-structure memory type, which is specified in bits 2:0 of the extended-page-table pointer (EPTP), a VM-execution control field (see Section 24.6.11). A value of 0 indicates the uncacheable type (UC), while a value of 6 indicates the write-back type (WB). Other values are reserved.
- If CR0.CD = 1, the memory type used for any such reference is uncacheable (UC).

The MTRRs have no effect on the memory type used for an access to an EPT paging structure.

#### 28.2.6.2 Memory Type Used for Translated Guest-Physical Addresses

The effective memory type of a memory access using a guest-physical address (an access that is translated using EPT) is the memory type that is used to access memory. The effective memory type is based on the value of bit 30 (cache disable—CD) in control register CR0; the last EPT paging-structure entry used to translate the guest-physical address (either an EPT PDE with bit 7 set to 1 or an EPT PTE); and the PAT memory type (see below):

- The PAT memory type depends on the value of CR0.PG:
  - If CR0.PG = 0, the PAT memory type is WB (writeback).\(^1\)
  - If CR0.PG = 1, the PAT memory type is the memory type selected from the IA32_PAT MSR as specified in Section 11.12.3, ”Selecting a Memory Type from the PAT”.\(^2\)

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1. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PG must be 1 in VMX operation, CR0.PG can be 0 in VMX non-root operation only if the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
2. Table 11-11 in Section 11.12.3, “Selecting a Memory Type from the PAT” illustrates how the PAT memory type is selected based on the values of the PAT, PCD, and PwT bits in a page-table entry (or page-directory entry with PS = 1). For accesses to a guest paging-structure entry X, the PAT memory type is selected from the table by using a value of 0 for the PAT bit with the values of PCD and PwT from the paging-structure entry Y that references X (or from CR3 if X is in the root paging structure). With PAE paging, the PAT memory type for accesses to the PDPTES is WB.
• The **EPT memory type** is specified in bits 5:3 of the last EPT paging-structure entry: 0 = UC; 1 = WC; 4 = WT; 5 = WP; and 6 = WB. Other values are reserved and cause EPT misconfigurations (see Section 28.2.3).

• If CR0.CD = 0, the effective memory type depends upon the value of bit 6 of the last EPT paging-structure entry:
  — If the value is 0, the effective memory type is the combination of the EPT memory type and the PAT memory type specified in Table 11-7 in Section 11.5.2.2, using the EPT memory type in place of the MTRR memory type.
  — If the value is 1, the memory type used for the access is the EPT memory type. The PAT memory type is ignored.

• If CR0.CD = 1, the effective memory type is UC.

The MTRRs have no effect on the memory type used for an access to a guest-physical address.

### 28.3 CACHING TRANSLATION INFORMATION

Processors supporting Intel® 64 and IA-32 architectures may accelerate the address-translation process by caching on the processor data from the structures in memory that control that process. Such caching is discussed in Section 4.10, “Caching Translation Information” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*. The current section describes how this caching interacts with the VMX architecture.

The VPID and EPT features of the architecture for VMX operation augment this caching architecture. EPT defines the guest-physical address space and defines translations to that address space (from the linear-address space) and from that address space (to the physical-address space). Both features control the ways in which a logical processor may create and use information cached from the paging structures.

Section 28.3.1 describes the different kinds of information that may be cached. Section 28.3.2 specifies when such information may be cached and how it may be used. Section 28.3.3 details how software can invalidate cached information.

#### 28.3.1 Information That May Be Cached

Section 4.10, “Caching Translation Information” in *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A* identifies two kinds of translation-related information that may be cached by a logical processor: translations, which are mappings from linear page numbers to physical page frames, and paging-structure caches, which map the upper bits of a linear page number to information from the paging-structure entries used to translate linear addresses matching those upper bits.

The same kinds of information may be cached when VPIDs and EPT are in use. A logical processor may cache and use such information based on its function. Information with different functionality is identified as follows:

• **Linear mappings.**¹ There are two kinds:
  — Linear translations. Each of these is a mapping from a linear page number to the physical page frame to which it translates, along with information about access privileges and memory typing.
  — Linear paging-structure-cache entries. Each of these is a mapping from the upper portion of a linear address to the physical address of the paging structure used to translate the corresponding region of the linear-address space, along with information about access privileges. For example, bits 47:39 of a linear address would map to the address of the relevant page-directory-pointer table.

Linear mappings do not contain information from any EPT paging structure.

• **Guest-physical mappings.**² There are two kinds:
  — Guest-physical translations. Each of these is a mapping from a guest-physical page number to the physical page frame to which it translates, along with information about access privileges and memory typing.

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¹ Earlier versions of this manual used the term “VPID-tagged” to identify linear mappings.
² Earlier versions of this manual used the term “EPTP-tagged” to identify guest-physical mappings.
— Guest-physical paging-structure-cache entries. Each of these is a mapping from the upper portion of a guest-physical address to the physical address of the EPT paging structure used to translate the corresponding region of the guest-physical address space, along with information about access privileges.

The information in guest-physical mappings about access privileges and memory typing is derived from EPT paging structures.

- **Combined mappings**. There are two kinds:
  - Combined translations. Each of these is a mapping from a linear page number to the physical page frame to which it translates, along with information about access privileges and memory typing.
  - Combined paging-structure-cache entries. Each of these is a mapping from the upper portion of a linear address to the physical address of the paging structure used to translate the corresponding region of the linear-address space, along with information about access privileges.

The information in combined mappings about access privileges and memory typing is derived from both guest paging structures and EPT paging structures.

### 28.3.2 Creating and Using Cached Translation Information

The following items detail the creation of the mappings described in the previous section:

- The following items describe the creation of mappings while EPT is not in use (including execution outside VMX non-root operation):
  - Linear mappings may be created. They are derived from the paging structures referenced (directly or indirectly) by the current value of CR3 and are associated with the current VPID and the current PCID.
  - No linear mappings are created with information derived from paging-structure entries that are not present (bit 0 is 0) or that set reserved bits. For example, if a PTE is not present, no linear mapping are created for any linear page number whose translation would use that PTE.
  - No guest-physical or combined mappings are created while EPT is not in use.

- The following items describe the creation of mappings while EPT is in use:
  - Guest-physical mappings may be created. They are derived from the EPT paging structures referenced (directly or indirectly) by bits 51:12 of the current EPTP. These 40 bits contain the address of the EPT-PML4-table. (the notation EP4TA refers to those 40 bits). Newly created guest-physical mappings are associated with the current EP4TA.
  - Combined mappings may be created. They are derived from the EPT paging structures referenced (directly or indirectly) by the current EP4TA. If CR0.PG = 1, they are also derived from the paging structures referenced (directly or indirectly) by the current value of CR3. They are associated with the current VPID, the current PCID, and the current EP4TA. If CR0.PG = 0, no combined paging-structure-cache entries are created if CR0.PG = 0.
  - No guest-physical mappings or combined mappings are created with information derived from EPT paging-structure entries that are not present (bits 2:0 are all 0) or that are misconfigured (see Section 28.2.3.1).
  - No combined mappings are created with information derived from guest paging-structure entries that are not present or that set reserved bits.
  - No linear mappings are created while EPT is in use.

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1. Earlier versions of this manual used the term “dual-tagged” to identify combined mappings.
2. This section associated cached information with the current VPID and PCID. If PCIDs are not supported or are not being used (e.g., because CR4.PCIDE = 0), all the information is implicitly associated with PCID 000H; see Section 4.10.1, “Process-Context Identifiers (PCIDs)” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
3. At any given time, a logical processor may be caching combined mappings for a VPID and a PCID that are associated with different EP4TAs. Similarly, it may be caching combined mappings for an EP4TA that are associated with different VPIDs and PCIDs.
4. If the capability MSR IA32_VMX_CR0_FIXED0 reports that CR0.PG must be 1 in VMX operation, CR0.PG can be 0 in VMX non-root operation only if the “unrestricted guest” VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.
The following items detail the use of the various mappings:

- If EPT is not in use (e.g., when outside VMX non-root operation), a logical processor may use cached mappings as follows:
  - For accesses using linear addresses, it may use linear mappings associated with the current VPID and the current PCID. It may also use global TLB entries (linear mappings) associated with the current VPID and any PCID.
  - No guest-physical or combined mappings are used while EPT is not in use.

- If EPT is in use, a logical processor may use cached mappings as follows:
  - For accesses using linear addresses, it may use combined mappings associated with the current VPID, the current PCID, and the current EP4TA. It may also use global TLB entries (combined mappings) associated with the current VPID, the current EP4TA, and any PCID.
  - For accesses using guest-physical addresses, it may use guest-physical mappings associated with the current EP4TA.
  - No linear mappings are used while EPT is in use.

### 28.3.3 Invalidating Cached Translation Information

Software modifications of paging structures (including EPT paging structures) may result in inconsistencies between those structures and the mappings cached by a logical processor. Certain operations invalidate information cached by a logical processor and can be used to eliminate such inconsistencies.

#### 28.3.3.1 Operations that Invalidate Cached Mappings

The following operations invalidate cached mappings as indicated:

- Operations that architecturally invalidate entries in the TLBs or paging-structure caches independent of VMX operation (e.g., the INVLPG and INVPID instructions) invalidate linear mappings and combined mappings. They are required to do so only for the current VPID (but, for combined mappings, all EP4TAs). Linear mappings for the current VPID are invalidated even if EPT is in use. Combined mappings for the current VPID are invalidated even if EPT is not in use.

- An EPT violation invalidates any guest-physical mappings (associated with the current EP4TA) that would be used to translate the guest-physical address that caused the EPT violation. If that guest-physical address was the translation of a linear address, the EPT violation also invalidates any combined mappings for that linear address associated with the current PCID, the current VPID and the current EP4TA.

- If the "enable VPID" VM-execution control is 0, VM entries and VM exits invalidate linear mappings and combined mappings associated with VPID 0000H (for all PCIDs). Combined mappings for VPID 0000H are invalidated for all EP4TAs.

- Execution of the INVPID instruction invalidates linear mappings and combined mappings. Invalidation is based on instruction operands, called the INVPID type and the INVPID descriptor. Four INVPID types are currently defined:
  - **Individual-address.** If the INVPID type is 0, the logical processor invalidates linear mappings and combined mappings associated with the VPID specified in the INVPID descriptor and that would be used to translate the linear address specified in of the INVPID descriptor. Linear mappings and combined mappings for that VPID and linear address are invalidated for all PCIDs and, for combined mappings, all

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1. See Section 4.10.4, "Invalidation of TLBs and Paging-Structure Caches," in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A for an enumeration of operations that architecturally invalidate entries in the TLBs and paging-structure caches independent of VMX operation.

2. While no linear mappings are created while EPT is in use, a logical processor may retain, while EPT is in use, linear mappings (for the same VPID as the current one) there were created earlier, when EPT was not in use.

3. While no combined mappings are created while EPT is not in use, a logical processor may retain, while EPT is in not use, combined mappings (for the same VPID as the current one) there were created earlier, when EPT was in use.
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EP4TAs. (The instruction may also invalidate mappings associated with other VPIDs and for other linear addresses.)

— Single-context. If the INVVPID type is 1, the logical processor invalidates all linear mappings and combined mappings associated with the VPID specified in the INVVPID descriptor. Linear mappings and combined mappings for that VPID are invalidated for all PCIDs and, for combined mappings, all EP4TAs. (The instruction may also invalidate mappings associated with other VPIDs.)

— All-context. If the INVVPID type is 2, the logical processor invalidates linear mappings and combined mappings associated with all VPIDs except VPID 0000H and with all PCIDs. (The instruction may also invalidate linear mappings with VPID 0000H.) Combined mappings are invalidated for all EP4TAs.

— Single-context-retaining-globals. If the INVVPID type is 3, the logical processor invalidates linear mappings and combined mappings associated with the VPID specified in the INVVPID descriptor. Linear mappings and combined mappings for that VPID are invalidated for all PCIDs and, for combined mappings, all EP4TAs. The logical processor is not required to invalidate information that was used for global translations (although it may do so). See Section 4.10, “Caching Translation Information” for details regarding global translations. (The instruction may also invalidate mappings associated with other VPIDs.)

See Chapter 30 for details of the INVVPID instruction. See Section 28.3.3.3 for guidelines regarding use of this instruction.

• Execution of the INVEPT instruction invalidates guest-physical mappings and combined mappings. Invalidation is based on instruction operands, called the INVEPT type and the INVEPT descriptor. Two INVEPT types are currently defined:
  — Single-context. If the INVEPT type is 1, the logical processor invalidates all guest-physical mappings and combined mappings associated with the EP4TA specified in the INVEPT descriptor. Combined mappings for that EP4TA are invalidated for all VPIDs and all PCIDs. (The instruction may invalidate mappings associated with other EP4TAs.)
  — All-context. If the INVEPT type is 2, the logical processor invalidates guest-physical mappings and combined mappings associated with all EP4TAs (and, for combined mappings, for all VPIDs and PCIDs).

See Chapter 30 for details of the INVEPT instruction. See Section 28.3.3.4 for guidelines regarding use of this instruction.

• A power-up or a reset invalidates all linear mappings, guest-physical mappings, and combined mappings.

28.3.3.2 Operations that Need Not Invalidate Cached Mappings

The following items detail cases of operations that are not required to invalidate certain cached mappings:

• Operations that architecturally invalidate entries in the TLBs or paging-structure caches independent of VMX operation are not required to invalidate any guest-physical mappings.
• The INVVPID instruction is not required to invalidate any guest-physical mappings.
• The INVEPT instruction is not required to invalidate any linear mappings.
• VMX transitions are not required to invalidate any guest-physical mappings. If the “enable VPID” VM-execution control is 1, VMX transitions are not required to invalidate any linear mappings or combined mappings.
• The VMXOFF and VMXON instructions are not required to invalidate any linear mappings, guest-physical mappings, or combined mappings.

A logical processor may invalidate any cached mappings at any time. For this reason, the operations identified above may invalidate the indicated mappings despite the fact that doing so is not required.

28.3.3.3 Guidelines for Use of the INVVPID Instruction

The need for VMM software to use the INVVPID instruction depends on how that software is virtualizing memory (e.g., see Section 32.3, “Memory Virtualization”).

If EPT is not in use, it is likely that the VMM is virtualizing the guest paging structures. Such a VMM may configure the VMCS so that all or some of the operations that invalidate entries the TLBs and the paging-structure caches (e.g., the INVLPG instruction) cause VM exits. If VMM software is emulating these operations, it may be necessary
to use the INVVPID instruction to ensure that the logical processor’s TLBs and the paging-structure caches are appropriately invalidated.

Requirements of when software should use the INVVPID instruction depend on the specific algorithm being used for page-table virtualization. The following items provide guidelines for software developers:

• Emulation of the INVLPG instruction may require execution of the INVVPID instruction as follows:
  — The INVVPID type is individual-address (0).
  — The VPID in the INVVPID descriptor is the one assigned to the virtual processor whose execution is being emulated.
  — The linear address in the INVVPID descriptor is that of the operand of the INVLPG instruction being emulated.

• Some instructions invalidate all entries in the TLBs and paging-structure caches—except for global translations. An example is the MOV to CR3 instruction. (See Section 4.10, “Caching Translation Information” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A for details regarding global translations.) Emulation of such an instruction may require execution of the INVVPID instruction as follows:
  — The INVVPID type is single-context-retaining-globals (3).
  — The VPID in the INVVPID descriptor is the one assigned to the virtual processor whose execution is being emulated.

• Some instructions invalidate all entries in the TLBs and paging-structure caches—including for global translations. An example is the MOV to CR4 instruction if the value of value of bit 4 (page global enable—PGE) is changing. Emulation of such an instruction may require execution of the INVVPID instruction as follows:
  — The INVVPID type is single-context (1).
  — The VPID in the INVVPID descriptor is the one assigned to the virtual processor whose execution is being emulated.

If EPT is not in use, the logical processor associates all mappings it creates with the current VPID, and it will use such mappings to translate linear addresses. For that reason, a VMM should not use the same VPID for different non-EPT guests that use different page tables. Doing so may result in one guest using translations that pertain to the other.

If EPT is in use, the instructions enumerated above might not be configured to cause VM exits and the VMM might not be emulating them. In that case, executions of the instructions by guest software properly invalidate the required entries in the TLBs and paging-structure caches (see Section 28.3.3.1); execution of the INVVPID instruction is not required.

If EPT is in use, the logical processor associates all mappings it creates with the value of bits 51:12 of current EPTP. If a VMM uses different EPTP values for different guests, it may use the same VPID for those guests. Doing so cannot result in one guest using translations that pertain to the other.

The following guidelines apply more generally and are appropriate even if EPT is in use:

• As detailed in Section 29.4.5, an access to the APIC-access page might not cause an APIC-access VM exit if software does not properly invalidate information that may be cached from the paging structures. If, at one time, the current VPID on a logical processor was a non-zero value X, it is recommended that software use the INVVPID instruction with the “single-context” INVVPID type and with VPID X in the INVVPID descriptor before a VM entry on the same logical processor that establishes VPID X and either (a) the “virtualize APIC accesses” VM-execution control was changed from 0 to 1; or (b) the value of the APIC-access address was changed.

• Software can use the INVVPID instruction with the “all-context” INVVPID type immediately after execution of the VMXON instruction or immediately prior to execution of the VMXOFF instruction. Either prevents potentially undesired retention of information cached from paging structures between separate uses of VMX operation.

28.3.3.4 Guidelines for Use of the INVEPT Instruction

The following items provide guidelines for use of the INVEPT instruction to invalidate information cached from the EPT paging structures.
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• Software should use the INVEPT instruction with the “single-context” INVEPT type after making any of the following changes to an EPT paging-structure entry (the INVEPT descriptor should contain an EPTP value that references — directly or indirectly — the modified EPT paging structure):
  — Changing any of the privilege bits 2:0 from 1 to 0.
  — Changing the physical address in bits 51:12.
  — Clearing bit 8 (the accessed flag) if accessed and dirty flags for EPT will be enabled.
  — For an EPT PDPT or an EPT PDE, changing bit 7 (which determines whether the entry maps a page).
  — For the last EPT paging-structure entry used to translate a guest-physical address (an EPT PDPT with bit 7 set to 1, an EPT PDE with bit 7 set to 1, or an EPT PTE), changing either bits 5:3 or bit 6. (These bits determine the effective memory type of accesses using that EPT paging-structure entry; see Section 28.2.6.)
  — For the last EPT paging-structure entry used to translate a guest-physical address (an EPT PDPT with bit 7 set to 1, an EPT PDE with bit 7 set to 1, or an EPT PTE), clearing bit 9 (the dirty flag) if accessed and dirty flags for EPT will be enabled.

• Software should use the INVEPT instruction with the “single-context” INVEPT type before a VM entry with an EPTP value X such that X[6] = 1 (accessed and dirty flags for EPT are enabled) if the logical processor had earlier been in VMX non-root operation with an EPTP value Y such that Y[6] = 0 (accessed and dirty flags for EPT are not enabled) and Y[51:12] = X[51:12].

• Software may use the INVEPT instruction after modifying a present EPT paging-structure entry to change any of the privilege bits 2:0 from 0 to 1. Failure to do so may cause an EPT violation that would not otherwise occur. Because an EPT violation invalidates any mappings that would be used by the access that caused the EPT violation (see Section 28.3.3.1), an EPT violation will not recur if the original access is performed again, even if the INVEPT instruction is not executed.

• Because a logical processor does not cache any information derived from EPT paging-structure entries that are not present or misconfigured (see Section 28.2.3.1), it is not necessary to execute INVEPT following modification of an EPT paging-structure entry that had been not present or misconfigured.

• As detailed in Section 29.4.5, an access to the APIC-access page might not cause an APIC-access VM exit if software does not properly invalidate information that may be cached from the EPT paging structures. If EPT was in use on a logical processor at one time with EPTP X, it is recommended that software use the INVEPT instruction with the “single-context” INVEPT type and with EPTP X in the INVEPT descriptor before a VM entry on the same logical processor that enables EPT with EPTP X and either (a) the “virtualize APIC accesses” VM-execution control was changed from 0 to 1; or (b) the value of the APIC-access address was changed.

• Software can use the INVEPT instruction with the “all-context” INVEPT type immediately after execution of the VMXON instruction or immediately prior to execution of the VMXOFF instruction. Either prevents potentially undesired retention of information cached from EPT paging structures between separate uses of VMX operation.

In a system containing more than one logical processor, software must account for the fact that information from an EPT paging-structure entry may be cached on logical processors other than the one that modifies that entry. The process of propagating the changes to a paging-structure entry is commonly referred to as "TLB shootdown." A discussion of TLB shootdown appears in Section 4.10.5, “Propagation of Paging-Structure Changes to Multiple Processors,” in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.
CHAPTER 29
APIC VIRTUALIZATION AND VIRTUAL INTERRUPTS

The VMCS includes controls that enable the virtualization of interrupts and the Advanced Programmable Interrupt Controller (APIC).

When these controls are used, the processor will emulate many accesses to the APIC, track the state of the virtual APIC, and deliver virtual interrupts — all in VMX non-root operation with out a VM exit.1

The processor tracks the state of the virtual APIC using a virtual-APIC page identified by the virtual-machine monitor (VMM). Section 29.1 discusses the virtual-APIC page and how the processor uses it to track the state of the virtual APIC.

The following are the VM-execution controls relevant to APIC virtualization and virtual interrupts (see Section 24.6 for information about the locations of these controls):

- **Virtual-interrupt delivery.** This controls enables the evaluation and delivery of pending virtual interrupts (Section 29.2). It also enables the emulation of writes (memory-mapped or MSR-based, as enabled) to the APIC registers that control interrupt prioritization.

- **Use TPR shadow.** This control enables emulation of accesses to the APIC’s task-priority register (TPR) via CR8 (Section 29.3) and, if enabled, via the memory-mapped or MSR-based interfaces.

- **Virtualize APIC accesses.** This control enables virtualization of memory-mapped accesses to the APIC (Section 29.4) by causing VM exits on accesses to a VMM-specified APIC-access page. Some of the other controls, if set, may cause some of these accesses to be emulated rather than causing VM exits.

- **Virtualize x2APIC mode.** This control enables virtualization of MSR-based accesses to the APIC (Section 29.5).

- **APIC-register virtualization.** This control allows memory-mapped and MSR-based reads of most APIC registers (as enabled) by satisfying them from the virtual-APIC page. It directs memory-mapped writes to the APIC-access page to the virtual-APIC page, following them by VM exits for VMM emulation.

- **Process posted interrupts.** This control allows software to post virtual interrupts in a data structure and send a notification to another logical processor; upon receipt of the notification, the target processor will process the posted interrupts by copying them into the virtual-APIC page (Section 29.6).

"Virtualize APIC accesses", "virtualize x2APIC mode", "virtual-interrupt delivery", and "APIC-register virtualization" are all secondary processor-based VM-execution controls. If bit 31 of the primary processor-based VM-execution controls is 0, the processor operates as if these controls were all 0. See Section 24.6.2.

### 29.1 VIRTUAL APIC STATE

The **virtual-APIC page** is a 4-KByte region of memory that the processor uses the virtual-APIC page to virtualize certain accesses to APIC registers and to manage virtual interrupts. The physical address of the virtual-APIC page is the **virtual-APIC address**, a 64-bit VM-execution control field in the VMCS (see Section 24.6.8).

Depending on the settings of certain VM-execution controls, the processor may virtualize certain fields on the virtual-APIC page with functionality analogous to that performed by the local APIC. Section 29.1.1 identifies and defines these fields. Section 29.1.2, Section 29.1.3, Section 29.1.4, and Section 29.1.5 detail the actions taken to virtualize updates to some of these fields.

#### 29.1.1 Virtualized APIC Registers

Depending on the setting of certain VM-execution controls, a logical processor may virtualize certain accesses to APIC registers using the following fields on the virtual-APIC page:

- **Virtual task-priority register (VTPR)**: the 32-bit field located at offset 080H on the virtual-APIC page.

---

1. In most cases, it is not necessary for a virtual-machine monitor (VMM) to inject virtual interrupts as part of VM entry.
• **Virtual processor-priority register (VPPR)**: the 32-bit field located at offset 0A0H on the virtual-APIC page.

• **Virtual end-of-interrupt register (VEOI)**: the 32-bit field located at offset 0B0H on the virtual-APIC page.

• **Virtual interrupt-service register (VISR)**: the 256-bit value comprising eight non-contiguous 32-bit fields at offsets 100H, 110H, 120H, 130H, 140H, 150H, 160H, and 170H on the virtual-APIC page. Bit x of the VISR is at bit position (x & 1FH) at offset (100H | ((x & E0H) » 1)). The processor uses only the low 4 bytes of each of the 16-byte fields at offsets 100H, 110H, 120H, 130H, 140H, 150H, 160H, and 170H.

• **Virtual interrupt-request register (VIRR)**: the 256-bit value comprising eight non-contiguous 32-bit fields at offsets 200H, 210H, 220H, 230H, 240H, 250H, 260H, and 270H on the virtual-APIC page. Bit x of the VIRR is at bit position (x & 1FH) at offset (200H | ((x & E0H) » 1)). The processor uses only the low 4 bytes of each of the 16-byte fields at offsets 200H, 210H, 220H, 230H, 240H, 250H, 260H, and 270H.

• **Virtual interrupt-command register (VICR_LO)**: the 32-bit field located at offset 300H on the virtual-APIC page.

• **Virtual interrupt-command register (VICR_HI)**: the 32-bit field located at offset 310H on the virtual-APIC page.

### 29.1.2 TPR Virtualization

The processor performs **TPR virtualization** in response to the following operations: (1) virtualization of the MOV to CR8 instruction; (2) virtualization of a write to offset 080H on the APIC-access page; and (3) virtualization of the WRMSR instruction with ECX = 808H. See Section 29.3, Section 29.4.3, and Section 29.5 for details of when TPR virtualization is performed.

The following pseudocode details the behavior of TPR virtualization:

```
IF "virtual-interrupt delivery" is 0
  THEN
    IF VTPR[7:4] < TPR threshold (see Section 24.6.8)
      THEN cause VM exit due to TPR below threshold;
    ELSE
      perform PPR virtualization (see Section 29.1.3);
    evaluate pending virtual interrupts (see Section 29.2.1);
  FI;
ELSE
  perform PPR virtualization (see Section 29.1.3);
  evaluate pending virtual interrupts (see Section 29.2.1);
FI;
```

Any VM exit caused by TPR virtualization is trap-like: the instruction causing TPR virtualization completes before the VM exit occurs (for example, the value of CS:RIP saved in the guest-state area of the VMCS references the next instruction).

### 29.1.3 PPR Virtualization

The processor performs **PPR virtualization** in response to the following operations: (1) VM entry; (2) TPR virtualization; and (3) EOI virtualization. See Section 26.3.2.5, Section 29.1.2, and Section 29.1.4 for details of when PPR virtualization is performed.

PPR virtualization uses the guest interrupt status (specifically, SVI; see Section 24.4.2) and VTPR. The following pseudocode details the behavior of PPR virtualization:

```
  THEN VPPR ← VTPR & FFH;
  ELSE VPPR ← SVI & F0H;
  FI;
```

PPR virtualization always clears bytes 3:1 of VPPR.

PPR virtualization is caused only by TPR virtualization, EOI virtualization, and VM entry. Delivery of a virtual interrupt also modifies VPPR, but in a different way (see Section 29.2.2). No other operations modify VPPR, even if they modify SVI, VISR, or VTPR.
29.1.4 EOI Virtualization

The processor performs **EOI virtualization** in response to the following operations: (1) virtualization of a write to offset 0B0H on the APIC-access page; and (2) virtualization of the WRMSR instruction with ECX = 80BH. See Section 29.4.3 and Section 29.5 for details of when EOI virtualization is performed. EOI virtualization occurs only if the "virtual-interrupt delivery” VM-execution control is 1.

EOI virtualization uses and updates the guest interrupt status (specifically, SVI; see Section 24.4.2). The following pseudocode details the behavior of EOI virtualization:

Vector ← SVI;
VISR[Vector] ← 0; (see Section 29.1.1 for definition of VISR)
IF any bits set in VISR
    THEN SVI ← highest index of bit set in VISR
    ELSE SVI ← 0;
FI;
perform PPR virtualiation (see Section 29.1.3);
IF EOI_exit_bitmap[Vector] = 1 (see Section 24.6.8 for definition of EOI_exit_bitmap)
    THEN cause EOI-induced VM exit with Vector as exit qualification;
    ELSE evaluate pending virtual interrupts; (see Section 29.2.1)
FI;

Any VM exit caused by EOI virtualization is trap-like: the instruction causing EOI virtualization completes before the VM exit occurs (for example, the value of CS:RIP saved in the guest-state area of the VMCS references the next instruction).

29.1.5 Self-IPI Virtualization

The processor performs **self-IPI virtualization** in response to the following operations: (1) virtualization of a write to offset 300H on the APIC-access page; and (2) virtualization of the WRMSR instruction with ECX = 83FH. See Section 29.4.3 and Section 29.5 for details of when self-IPI virtualization is performed. Self-IPI virtualization occurs only if the "virtual-interrupt delivery” VM-execution control is 1.

Each operation that leads to self-IPI virtualization provides an 8-bit vector (see Section 29.4.3 and Section 29.5). Self-IPI virtualization updates the guest interrupt status (specifically, RVI; see Section 24.4.2). The following pseudocode details the behavior of self-IPI virtualization:

VIRR[Vector] ← 1; (see Section 29.1.1 for definition of VIRR)
RVI ← max{RVI,Vector};
evaluate pending virtual interrupts; (see Section 29.2.1)

29.2 Evaluation and Delivery of Virtual Interrupts

If the "virtual-interrupt delivery” VM-execution control is 1, certain actions in VMX non-root operation or during VM entry cause the processor to evaluate and deliver virtual interrupts.

Evaluation of virtual interrupts is triggered by certain actions change the state of the virtual-APIC page and is described in Section 29.2.1. This evaluation may result in recognition of a virtual interrupt. Once a virtual interrupt is recognized, the processor may deliver it within VMX non-root operation without a VM exit. Virtual-interrupt delivery is described in Section 29.2.2.

29.2.1 Evaluation of Pending Virtual Interrupts

If the "virtual-interrupt delivery” VM-execution control is 1, certain actions cause a logical processor to **evaluate pending virtual interrupts**.

The following actions cause the evaluation of pending virtual interrupts: VM entry; TPR virtualization; EOI virtualization; self-IPI virtualization; and posted-interrupt processing. See Section 26.3.2.5, Section 29.1.2, Section
29.1.4, Section 29.1.5, and Section 29.6 for details of when evaluation of pending virtual interrupts is performed. No other operations cause the evaluation of pending virtual interrupts, even if they modify RVI or VPPR.

Evaluation of pending virtual interrupts uses the guest interrupt status (specifically, RVI; see Section 24.4.2). The following pseudocode details the evaluation of pending virtual interrupts:

\[
\text{IF } \text{"interrupt-window exiting" is 0 AND} \\
\text{RVI}[7:4] > VPPR[7:4] (see Section 29.1.1 for definition of VPPR) \text{ THEN recognize a pending virtual interrupt;} \\
\text{ELSE} \text{ do not recognize a pending virtual interrupt;} \\
\text{FI;
}\]

Once recognized, a virtual interrupt may be delivered in VMX non-root operation; see Section 29.2.2.

Evaluation of pending virtual interrupts is caused only by VM entry, TPR virtualization, EOI virtualization, self-IPI virtualization, and posted-interrupt processing. No other operations do so, even if they modify RVI or VPPR. The logical processor ceases recognition of a pending virtual interrupt following the delivery of a virtual interrupt.

### 29.2.2 Virtual-Interrupt Delivery

If a virtual interrupt has been recognized (see Section 29.2.1), it will be delivered at an instruction boundary when the following conditions all hold: (1) RFLAGS.IF = 1; (2) there is no blocking by STI; (3) there is no blocking by MOV SS or by POP SS; and (4) the "interrupt-window exiting" VM-execution control is 0.

Virtual-interrupt delivery has the same priority as that of VM exits due to the 1-setting of the "interrupt-window exiting" VM-execution control. Thus, non-maskable interrupts (NMIs) and higher priority events take priority over delivery of a virtual interrupt; delivery of a virtual interrupt takes priority over external interrupts and lower priority events.

Virtual-interrupt delivery wakes a logical processor from the same inactive activity states as would an external interrupt. Specifically, it wakes a logical processor from the states entered using the HLT and MWAIT instructions. It does not wake a logical processor in the shutdown state or in the wait-for-SIPI state.

Virtual-interrupt delivery updates the guest interrupt status (both RVI and SVI; see Section 24.4.2) and delivers an event within VMX non-root operation without a VM exit. The following pseudocode details the behavior of virtual-interrupt delivery (see Section 29.1.1 for definition of VISR, VIRR, and VPPR):

\[
\text{Vector } \leftarrow \text{RVI;} \\
\text{VISR}[\text{Vector}] \leftarrow 1; \\
\text{SVI } \leftarrow \text{Vector;} \\
\text{VPPR } \leftarrow \text{Vector } \& \text{ FOH;} \\
\text{VIRR}[\text{Vector}] \leftarrow 0; \\
\text{IF any bits set in VIRR} \\
\text{ THEN RVI } \leftarrow \text{highest index of bit set in VIRR} \\
\text{ ELSE RVI } \leftarrow 0; \\
\text{FI;} \\
\text{deliver interrupt with Vector through IDT;} \\
\text{cease recognition of any pending virtual interrupt;
}\]

### 29.3 Virtualizing CR8-Based TPR Accesses

In 64-bit mode, software can access the local APIC’s task-priority register (TPR) through CR8. Specifically, software uses the MOV from CR8 and MOV to CR8 instructions (see Section 10.8.6, “Task Priority in IA-32e Mode”). This section describes how these accesses can be virtualized.

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2. A logical processor never recognizes or delivers a virtual interrupt if the "interrupt-window exiting" VM-execution control is 1. Because of this, the relative priority of virtual-interrupt delivery and VM exits due to the 1-setting of that control is not defined.
A virtual-machine monitor can virtualize these CR8-based APIC accesses by setting the "CR8-load exiting" and "CR8-store exiting" VM-execution controls, ensuring that the accesses cause VM exits (see Section 25.1.3). Alternatively, there are methods for virtualizing some CR8-based APIC accesses without VM exits.

Normally, an execution of MOV from CR8 or MOV to CR8 that does not fault or cause a VM exit accesses the APIC's TPR. However, such an execution are treated specially if the "use TPR shadow" VM-execution control is 1. The following items provide details:

- **MOV from CR8.** The instruction loads bits 3:0 of its destination operand with bits 7:4 of VTPR (see Section 29.1.1). Bits 63:4 of the destination operand are cleared.
- **MOV to CR8.** The instruction stores bits 3:0 of its source operand into bits 7:4 of VTPR; the remainder of VTPR (bits 3:0 and bits 31:8) are cleared. Following this, the processor performs TPR virtualization (see Section 29.1.2).

### 29.4 VIRTUALIZING MEMORY-MAPPED APIC ACCESSES

When the local APIC is in xAPIC mode, software accesses the local APIC's control registers using a memory-mapped interface. Specifically, software uses linear addresses that translate to physical addresses on page frame indicated by the base address in the IA32_APIC_BASE MSR (see Section 10.4.4, "Local APIC Status and Location"). This section describes how these accesses can be virtualized.

A virtual-machine monitor (VMM) can virtualize these memory-mapped APIC accesses by ensuring that any access to a linear address that would access the local APIC instead causes a VM exit. This could be done using paging or the extended page-table mechanism (EPT). Another way is by using the 1-setting of the "virtualize APIC accesses" VM-execution control.

If the "virtualize APIC accesses" VM-execution control is 1, the logical processor treats specially memory accesses using linear addresses that translate to physical addresses in the 4-KByte APIC-access page.3 (The APIC-access page is identified by the APIC-access address, a field in the VMCS; see Section 24.6.8.)

In general, an access to the APIC-access page causes an APIC-access VM exit. APIC-access VM exits provide a VMM with information about the access causing the VM exit. Section 29.4.1 discusses the priority of APIC-access VM exits.

Certain VM-execution controls enable the processor to virtualize certain accesses to the APIC-access page without a VM exit. In general, this virtualization causes these accesses to be made to the virtual-APIC page instead of the APIC-access page.

### NOTES

Unless stated otherwise, this section characterizes only linear accesses to the APIC-access page; an access to the APIC-access page is a linear access if (1) it results from a memory access using a linear address; and (2) the access’s physical address is the translation of that linear address. Section 29.4.6 discusses accesses to the APIC-access page that are not linear accesses.

The distinction between the APIC-access page and the virtual-APIC page allows a VMM to share paging structures or EPT paging structures among the virtual processors of a virtual machine (the shared paging structures referencing the same APIC-access address, which appears in the VMCS of all the virtual processors) while giving each virtual processor its own virtual APIC (the VMCS of each virtual processor will have a unique virtual-APIC address).

Section 29.4.2 discusses when and how the processor may virtualize read accesses from the APIC-access page. Section 29.4.3 does the same for write accesses. When virtualizing a write to the APIC-access page, the processor typically takes actions in addition to passing the write through to the virtual-APIC page.

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3. Even when addresses are translated using EPT (see Section 28.2), the determination of whether an APIC-access VM exit occurs depends on an access’s physical address, not its guest-physical address. Even when CR0.PG = 0, ordinary memory accesses by software use linear addresses; the fact that CR0.PG = 0 means only that the identity translation is used to convert linear addresses to physical (or guest-physical) addresses.
The discussion in those sections uses the concept of an **operation** within which these memory accesses may occur. For those discussions, an “operation” can be an iteration of a REP-prefixed string instruction, an execution of any other instruction, or delivery of an event through the IDT.

The 1-setting of the “virtualize APIC accesses” VM-execution control may also affect accesses to the APIC-access page that do not result directly from linear addresses. This is discussed in Section 29.4.6.

### 29.4.1 Priority of APIC-Access VM Exits

The following items specify the priority of APIC-access VM exits relative to other events.

- The priority of an APIC-access VM exit due to a memory access is below that of any page fault or EPT violation that that access may incur. That is, an access does not cause an APIC-access VM exit if it would cause a page fault or an EPT violation.
- A memory access does not cause an APIC-access VM exit until after the accessed flags are set in the paging structures (including EPT paging structures, if enabled).
- A write access does not cause an APIC-access VM exit until after the dirty flags are set in the appropriate paging structure and EPT paging structure (if enabled).
- With respect to all other events, any APIC-access VM exit due to a memory access has the same priority as any page fault or EPT violation that the access could cause. (This item applies to other events that the access may generate as well as events that may be generated by other accesses by the same operation.)

These principles imply, among other things, that an APIC-access VM exit may occur during the execution of a repeated string instruction (including INS and OUTS). Suppose, for example, that the first \( n \) iterations \( (n \leq 0) \) of such an instruction do not access the APIC-access page and that the next iteration does access that page. As a result, the first \( n \) iterations may complete and be followed by an APIC-access VM exit. The instruction pointer saved in the VMCS references the repeated string instruction and the values of the general-purpose registers reflect the completion of \( n \) iterations.

### 29.4.2 Virtualizing Reads from the APIC-Access Page

A read access from the APIC-access page causes an APIC-access VM exit if any of the following are true:

- The “use TPR shadow” VM-execution control is 0.
- The access is for an instruction fetch.
- The access is more than 32 bits in size.
- The access is part of an operation for which the processor has already virtualized a write to the APIC-access page.
- The access is not entirely contained within the low 4 bytes of a naturally aligned 16-byte region. That is, bits 3:2 of the access’s address are 0, and the same is true of the address of the highest byte accessed.

If none of the above are true, whether a read access is virtualized depends on the setting of the “APIC-register virtualization” VM-execution control:

- If “APIC-register virtualization” is 0, a read access is virtualized if its page offset is 080H (task priority); otherwise, the access causes an APIC-access VM exit.
- If “APIC-register virtualization” is 1, a read access is virtualized if it is entirely within one the following ranges of offsets:
  - 020H–023H (local APIC ID);
  - 030H–033H (local APIC version);
  - 080H–083H (task priority);
  - 0B0H–0B3H (end of interrupt);
  - 0D0H–0D3H (logical destination);
  - 0E0H–0E3H (destination format);
— 0F0H–0F3H (spurious-interrupt vector);
173H (in-service);
— 180H–183H, 190H–193H, 1A0H–1A3H, 1B0H–1B3H, 1C0H–1C3H, 1D0H–1D3H, 1E0H–1E3H, or 1F0H–
1F3H (trigger mode);
273H (interrupt request);
— 280H–283H (error status);
— 300H–303H or 310H–313H (interrupt command);
— 380H–383H (initial count); or
— 3E0H–3E3H (divide configuration).

In all other cases, the access causes an APIC-access VM exit.

A read access from the APIC-access page that is virtualized returns data from the corresponding page offset on the
virtual-APIC page.4

29.4.3 Virtualizing Writes to the APIC-Access Page

Whether a write access to the APIC-access page is virtualized depends on the settings of the VM-execution controls
and the page offset of the access. Section 29.4.3.1 details when APIC-write virtualization occurs.

Unlike reads, writes to the local APIC have side effects; because of this, virtualization of writes to the APIC-access
page may require emulation specific to the access's page offset (which identifies the APIC register being accessed).
Section 29.4.3.2 describes this APIC-write emulation.

For some page offsets, it is necessary for software to complete the virtualization after a write completes. In these
cases, the processor causes an APIC-write VM exit to invoke VMM software. Section 29.4.3.3 discusses APIC-
write VM exits.

29.4.3.1 Determining Whether a Write Access is Virtualized

A write access to the APIC-access page causes an APIC-access VM exit if any of the following are true:

• The “use TPR shadow” VM-execution control is 0.
• The access is more than 32 bits in size.
• The access is part of an operation for which the processor has already virtualized a write (with a different page
offset or a different size) to the APIC-access page.
• The access is not entirely contained within the low 4 bytes of a naturally aligned 16-byte region. That is, bits
3:2 of the access's address are 0, and the same is true of the address of the highest byte accessed.

If none of the above are true, whether a write access is virtualized depends on the settings of the “APIC-register
virtualization” and “virtual-interrupt delivery” VM-execution controls:

• If the "APIC-register virtualization" and "virtual-interrupt delivery" VM-execution controls are both 0, a write
access is virtualized if its page offset is 080H; otherwise, the access causes an APIC-access VM exit.
• If the "APIC-register virtualization" VM-execution control is 0 and the "virtual-interrupt delivery" VM-execution
control is 1, a write access is virtualized if its page offset is 080H (task priority), 0B0H (end of interrupt), and
300H (interrupt command — low); otherwise, the access causes an APIC-access VM exit.
• If "APIC-register virtualization is 1, a write access is virtualized if it is entirely within one the following ranges of
offsets:

4. The memory type used for accesses that read from the virtual-APIC page is reported in bits 53:50 of the IA32_VMX_BASIC MSR
(see Appendix A.1).
— 020H–023H (local APIC ID);
— 080H–083H (task priority);
— 080H–083H (end of interrupt);
— 0D0H–0D3H (logical destination);
— 0E0H–0E3H (destination format);
— 0F0H–0F3H (spurious-interrupt vector);
— 280H–283H (error status);
— 300H–303H or 310H–313H (interrupt command);
— 380H–383H (initial count); or
— 3E0H–3E3H (divide configuration).

In all other cases, the access causes an APIC-access VM exit.

The processor virtualizes a write access to the APIC-access page by writing data to the corresponding page offset on the virtual-APIC page. Following this, the processor performs certain actions after completion of the operation of which the access was a part. APIC-write emulation is described in Section 29.4.3.2.

### 29.4.3.2 APIC-Write Emulation

If the processor virtualizes a write access to the APIC-access page, it performs additional actions after completion of an operation of which the access was a part. These actions are called **APIC-write emulation**.

The details of APIC-write emulation depend upon the page offset of the virtualized write access:

- **080H (task priority)**. The processor clears bytes 3:1 of VTPR and then causes TPR virtualization (Section 29.1.2).
- **0B0H (end of interrupt)**. If the "virtual-interrupt delivery" VM-execution control is 1, the processor clears VEOI and then causes EOI virtualization (Section 29.1.4); otherwise, the processor causes an APIC-write VM exit (Section 29.4.3.3).
- **300H (interrupt command — low)**. If the "virtual-interrupt delivery" VM-execution control is 1, the processor checks the value of VICR_LO to determine whether the following are all true:
  - Reserved bits (31:20, 17:16, 13) and bit 12 (delivery status) are all 0.
  - Bits 19:18 (destination shorthand) are 01B (self).
  - Bit 15 (trigger mode) is 0 (edge).
  - Bits 10:8 (delivery mode) are 000B (fixed).
  - Bits 7:4 (the upper half of the vector) are not 0000B.

  If all of the items above are true, the processor performs self-IPI virtualization using the 8-bit vector in byte 0 of VICR_LO (Section 29.1.5).

  If the "virtual-interrupt delivery" VM-execution control is 0, or if any of the items above are false, the processor causes an APIC-write VM exit (Section 29.4.3.3).

- **310H–313H (interrupt command — high)**. The processor clears bytes 2:0 of VICR_HI. No other virtualization or VM exit occurs.
- Any other page offset. The processor causes an APIC-write VM exit (Section 29.4.3.3).

5. The memory type used for accesses that write to the virtual-APIC page is reported in bits 53:50 of the IA32_VMX_BASIC MSR (see Appendix A.1).
6. Recall that, for the purposes of this discussion, an operation is an iteration of a REP-prefixed string instruction, an execution of any other instruction, or delivery of an event through the IDT.
7. For any operation, there can be only one page offset for which a write access was virtualized. This is because a write access is not virtualized if the processor has already virtualized a write access for the same operation with a different page offset.
APIC-write emulation takes priority over system-management interrupts (SMIs), INIT signals, and lower priority events. APIC-write emulation is not blocked if RFLAGS.IF = 0 or by the MOV SS, POP SS, or STI instructions.

If an operation causes a fault after a write access to the APIC-access page and before APIC-write emulation, and that fault is delivered without a VM exit, APIC-write emulation occurs after the fault is delivered and before the fault handler can execute. If an operation causes a VM exit (perhaps due to a fault) after a write access to the APIC-access page and before APIC-write emulation, the APIC-write emulation does not occur.

### 29.4.3.3 APIC-Write VM Exits

In certain cases, VMM software must be invoked to complete the virtualization of a write access to the APIC-access page. In this case, APIC-write emulation causes an **APIC-write VM exit**. (Section 29.4.3.2 details the cases that causes APIC-write VM exits.)

APIC-write VM exits are invoked by APIC-write emulation, and APIC-write emulation occurs after an operation that performs a write access to the APIC-access page. Because of this, every APIC-write VM exit is trap-like: it occurs after completion of the operation containing the write access that caused the VM exit (for example, the value of CS:RIP saved in the guest-state area of the VMCS references the next instruction).

The basic exit reason for an APIC-write VM exit is “APIC write.” The exit qualification is the page offset of the write access that led to the VM exit.

As noted in Section 29.5, execution of WRMSR with ECX = 83FH (self-IPI MSR) can lead to an APIC-write VM exit if the “virtual-interrupt delivery” VM-execution control is 1. The exit qualification for such an APIC-write VM exit is 3F0H.

### 29.4.4 Instruction-Specific Considerations

Certain instructions that use linear address may cause page faults even though they do not use those addresses to access memory. The APIC-virtualization features may affect these instructions as well:

- **CLFLUSH, CLFLUSHOPT.** With regard to faulting, the processor operates as if each of these instructions reads from the linear address in its source operand. If that address translates to one on the APIC-access page, the instruction may cause an APIC-access VM exit. If it does not, it will flush the corresponding cache line on the virtual-APIC page instead of the APIC-access page.

- **ENTER.** With regard to faulting, the processor operates if ENTER writes to the byte referenced by the final value of the stack pointer (even though it does not if its size operand is non-zero). If that value translates to an address on the APIC-access page, the instruction may cause an APIC-access VM exit. If it does not, it will cause the APIC-write emulation appropriate to the address’s page offset.

- **MASKMOVQ and MAKSMOVQDQU.** Even if the instruction’s mask is zero, the processor may operate with regard to faulting as if MASKMOVQ or MASKMOVDQU writes to memory (the behavior is implementation-specific). In such a situation, an APIC-access VM exit may occur.

- **MONITOR.** With regard to faulting, the processor operates as if MONITOR reads from the effective address in RAX. If the resulting linear address translates to one on the APIC-access page, the instruction may cause an APIC-access VM exit. If it does not, it will monitor the corresponding address on the virtual-APIC page instead of the APIC-access page.

- **PREFETCH.** An execution of the PREFETCH instruction that would result in an access to the APIC-access page does not cause an APIC-access VM exit. Such an access may prefetch data; if so, it is from the corresponding address on the virtual-APIC page.

Virtualization of accesses to the APIC-access page is principally intended for basic instructions such as AND, MOV, OR, TEST, XCHG, and XOR. Use of an instruction that normally operates on floating-point, SSE, AVX, or AVX-512 registers may cause an APIC-access VM exit unconditionally regardless of the page offset it accesses on the APIC-access page.

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8. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For IA-32 processors, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.). In a few places, notation such as EAX is used to refer specifically to lower 32 bits of the indicated register.
29.4.5 Issues Pertaining to Page Size and TLB Management

The 1-setting of the "virtualize APIC accesses" VM-execution is guaranteed to apply only if translations to the APIC-access address use a 4-KByte page. The following items provide details:

- If EPT is not in use, any linear address that translates to an address on the APIC-access page should use a 4-KByte page. Any access to a linear address that translates to the APIC-access page using a larger page may operate as if the "virtualize APIC accesses" VM-execution control were 0.

- If EPT is in use, any guest-physical address that translates to an address on the APIC-access page should use a 4-KByte page. Any access to a linear address that translates to a guest-physical address that in turn translates to the APIC-access page using a larger page may operate as if the "virtualize APIC accesses" VM-execution control were 0. (This is true also for guest-physical accesses to the APIC-access page; see Section 29.4.6.1.)

In addition, software should perform appropriate TLB invalidation when making changes that may affect APIC-virtualization. The specifics depend on whether VPIDs or EPT is being used:

- **VPIDs being used but EPT not being used.** Suppose that there is a VPID that has been used before and that software has since made either of the following changes: (1) set the "virtualize APIC accesses" VM-execution control when it had previously been 0; or (2) changed the paging structures so that some linear address translates to the APIC-access address when it previously did not. In that case, software should execute INVVPID (see "INVVPID— Invalidate Translations Based on VPID" in Section 30.3) before performing on the same logical processor and with the same VPID.9

- **EPT being used.** Suppose that there is an EPTP value that has been used before and that software has since made either of the following changes: (1) set the "virtualize APIC accesses" VM-execution control when it had previously been 0; or (2) changed the EPT paging structures so that some guest-physical address translates to the APIC-access address when it previously did not. In that case, software should execute INVEPT (see "INVEPT— Invalidate Translations Derived from EPT" in Section 30.3) before performing on the same logical processor and with the same EPTP value.10

- **Neither VPIDs nor EPT being used.** No invalidation is required.

Failure to perform the appropriate TLB invalidation may result in the logical processor operating as if the "virtualize APIC accesses" VM-execution control were 0 in responses to accesses to the affected address. (No invalidation is necessary if neither VPIDs nor EPT is being used.)

29.4.6 APIC Accesses Not Directly Resulting From Linear Addresses

Section 29.4 has described the treatment of accesses that use linear addresses that translate to addresses on the APIC-access page. This section considers memory accesses that do not result directly from linear addresses.

- An access is called a **guest-physical access** if (1) CR0.PG = 1;11 (2) the "enable EPT" VM-execution control is 1;12 (3) the access’s physical address is the result of an EPT translation; and (4) either (a) the access was not generated by a linear address; or (b) the access’s guest-physical address is not the translation of the access’s linear address. Section 29.4.6.1 discusses the treatment of guest-physical accesses to the APIC-access page.

- An access is called a **physical access** if (1) either (a) the "enable EPT" VM-execution control is 0; or (b) the access’s physical address is not the result of a translation through the EPT paging structures; and (2) either (a) the access was not generated by a linear address; or (b) the access’s physical address is not the translation of its linear address. Section 29.4.6.2 discusses the treatment of physical accesses to the APIC-access page.

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9. INVVPID should use either (1) the all-contexts INVVPID type; (2) the single-context INVVPID type with the VPID in the INVVPID descriptor; or (3) the individual-address INVVPID type with the linear address and the VPID in the INVVPID descriptor.

10. INVEPT should use either (1) the global INVEPT type; or (2) the single-context INVEPT type with the EPTP value in the INVEPT descriptor.

11. If the capability MSR IA32_VMX_CR0FIXED0 reports that CR0.PG must be 1 in VMX operation, CR0.PG must be 1 unless the "unrestricted guest" VM-execution control and bit 31 of the primary processor-based VM-execution controls are both 1.

12. "Enable EPT" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VMX non-root operation functions as if the "enable EPT" VM-execution control were 0. See Section 24.6.2.
29.4.6.1 Guest-Physical Accesses to the APIC-Access Page

Guest-physical accesses include the following when guest-physical addresses are being translated using EPT:

• Reads from the guest paging structures when translating a linear address (such an access uses a guest-physical address that is not the translation of that linear address).

• Loads of the page-directory-pointer-table entries by MOV to CR when the logical processor is using (or that causes the logical processor to use) PAE paging (see Section 4.4).

• Updates to the accessed and dirty flags in the guest paging structures when using a linear address (such an access uses a guest-physical address that is not the translation of that linear address).

Every guest-physical access to an address on the APIC-access page causes an APIC-access VM exit. Such accesses are never virtualized regardless of the page offset.

The following items specify the priority relative to other events of APIC-access VM exits caused by guest-physical accesses to the APIC-access page.

• The priority of an APIC-access VM exit caused by a guest-physical access to memory is below that of any EPT violation that that access may incur. That is, a guest-physical access does not cause an APIC-access VM exit if it would cause an EPT violation.

• With respect to all other events, any APIC-access VM exit caused by a guest-physical access has the same priority as any EPT violation that the guest-physical access could cause.

29.4.6.2 Physical Accesses to the APIC-Access Page

Physical accesses include the following:

• If the “enable EPT” VM-execution control is 0:
  — Reads from the paging structures when translating a linear address.
  — Loads of the page-directory-pointer-table entries by MOV to CR when the logical processor is using (or that causes the logical processor to use) PAE paging (see Section 4.4).
  — Updates to the accessed and dirty flags in the paging structures.

• If the “enable EPT” VM-execution control is 1, accesses to the EPT paging structures (including updates to the accessed and dirty flags for EPT).

• Any of the following accesses made by the processor to support VMX non-root operation:
  — Accesses to the VMCS region.
  — Accesses to data structures referenced (directly or indirectly) by physical addresses in VM-execution control fields in the VMCS. These include the I/O bitmaps, the MSR bitmaps, and the virtual-APIC page.

• Accesses that effect transitions into and out of SMM.13 These include the following:
  — Accesses to SMRAM during SMI delivery and during execution of RSM.
  — Accesses during SMM VM exits (including accesses to MSEG) and during VM entries that return from SMM.

A physical access to the APIC-access page may or may not cause an APIC-access VM exit. If it does not cause an APIC-access VM exit, it may access the APIC-access page or the virtual-APIC page. Physical write accesses to the APIC-access page may or may not cause APIC-write emulation or APIC-write VM exits.

The priority of an APIC-access VM exit caused by physical access is not defined relative to other events that the access may cause.

It is recommended that software not set the APIC-access address to any of the addresses used by physical memory accesses (identified above). For example, it should not set the APIC-access address to the physical address of any of the active paging structures if the “enable EPT” VM-execution control is 0.

13. Technically, these accesses do not occur in VMX non-root operation. They are included here for clarity.
29.5 VIRTUALIZING MSR-BASED APIC ACCESSES

When the local APIC is in x2APIC mode, software accesses the local APIC’s control registers using the MSR interface. Specifically, software uses the RDMSR and WRMSR instructions, setting ECX (identifying the MSR being accessed) to values in the range 800H–8FFH (see Section 10.12, “Extended XAPIC (x2APIC”)). This section describes how these accesses can be virtualized.

A virtual-machine monitor can virtualize these MSR-based APIC accesses by configuring the MSR bitmaps (see Section 24.6.9) to ensure that the accesses cause VM exits (see Section 25.1.3). Alternatively, there are methods for virtualizing some MSR-based APIC accesses without VM exits.

Normally, an execution of RDMSR or WRMSR that does not fault or cause a VM exit accesses the MSR indicated in ECX. However, such an execution treats some values of ECX in the range 800H–8FFH specially if the “virtualize x2APIC mode” VM-execution control is 1. The following items provide details:

- **RDMSR.** The instruction’s behavior depends on the setting of the “APIC-register virtualization” VM-execution control.
  - If the “APIC-register virtualization” VM-execution control is 0, behavior depends upon the value of ECX.
    - If ECX contains 808H (indicating the TPR MSR), the instruction reads the 8 bytes from offset 080H on the virtual-APIC page (VTPR and the 4 bytes above it) into EDX:EAX. This occurs even if the local APIC is not in x2APIC mode (no general-protection fault occurs because the local APIC is not x2APIC mode).
    - If ECX contains any other value in the range 800H–8FFH, the instruction operates normally. If the local APIC is in x2APIC mode and ECX indicates a readable APIC register, EDX and EAX are loaded with the value of that register. If the local APIC is not in x2APIC mode or ECX does not indicate a readable APIC register, a general-protection fault occurs.
  - If “APIC-register virtualization” is 1 and ECX contains a value in the range 800H–8FFH, the instruction reads the 8 bytes from offset X on the virtual-APIC page into EDX:EAX, where X = (ECX & FFH) « 4. This occurs even if the local APIC is not in x2APIC mode (no general-protection fault occurs because the local APIC is not in x2APIC mode).

- **WRMSR.** The instruction’s behavior depends on the value of ECX and the setting of the “virtual-interrupt delivery” VM-execution control.
  Special processing applies in the following cases: (1) ECX contains 808H (indicating the TPR MSR); (2) ECX contains 80BH (indicating the EOI MSR) and the “virtual-interrupt delivery” VM-execution control is 1; and (3) ECX contains 83FH (indicating the self-IPI MSR) and the “virtual-interrupt delivery” VM-execution control is 1.

  If special processing applies, no general-protection exception is produced due to the fact that the local APIC is in xAPIC mode. However, WRMSR does perform the normal reserved-bit checking:
  - If ECX contains 808H or 83FH, a general-protection fault occurs if either EDX or EAX[31:8] is non-zero.
  - If ECX contains 80BH, a general-protection fault occurs if either EDX or EAX is non-zero.
  If there is no fault, WRMSR stores EDX:EAX at offset X on the virtual-APIC page, where X = (ECX & FFH) « 4. Following this, the processor performs an operation depending on the value of ECX:
    - If ECX contains 808H, the processor performs TPR virtualization (see Section 29.1.2).
    - If ECX contains 80BH, the processor performs EOI virtualization (see Section 29.1.4).
    - If ECX contains 83FH, the processor then checks the value of EAX[7:4] and proceeds as follows:
      - If the value is non-zero, the logical processor performs self-IPI virtualization with the 8-bit vector in EAX[7:0] (see Section 29.1.5).
      - If the value is zero, the logical processor causes an APIC-write VM exit as if there had been a write access to page offset 3F0H on the APIC-access page (see Section 29.4.3.3).

  If special processing does not apply, the instruction operates normally. If the local APIC is in x2APIC mode and ECX indicates a writeable APIC register, the value in EDX:EAX is written to that register. If the local APIC is not in x2APIC mode or ECX does not indicate a writeable APIC register, a general-protection fault occurs.
29.6 POSTED-INTERRUPT PROCESSING

Posted-interrupt processing is a feature by which a processor processes the virtual interrupts by recording them as pending on the virtual-APIC page.

Posted-interrupt processing is enabled by setting the “process posted interrupts” VM-execution control. The processing is performed in response to the arrival of an interrupt with the posted-interrupt notification vector. In response to such an interrupt, the processor processes virtual interrupts recorded in a data structure called a posted-interrupt descriptor. The posted-interrupt notification vector and the address of the posted-interrupt descriptor are fields in the VMCS; see Section 24.6.8.

If the “process posted interrupts” VM-execution control is 1, a logical processor uses a 64-byte posted-interrupt descriptor located at the posted-interrupt descriptor address. The posted-interrupt descriptor has the following format:

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>255:0</td>
<td>Posted-interrupt requests</td>
<td>One bit for each interrupt vector. There is a posted-interrupt request for a vector if the corresponding bit is 1</td>
</tr>
<tr>
<td>256</td>
<td>Outstanding notification</td>
<td>If this bit is set, there is a notification outstanding for one or more posted interrupts in bits 255:0</td>
</tr>
<tr>
<td>511:257</td>
<td>Reserved for software and other agents</td>
<td>These bits may be used by software and by other agents in the system (e.g., chipset). The processor does not modify these bits.</td>
</tr>
</tbody>
</table>

The notation `PIR` (posted-interrupt requests) refers to the 256 posted-interrupt bits in the posted-interrupt descriptor.

Use of the posted-interrupt descriptor differs from that of other data structures that are referenced by pointers in a VMCS. There is a general requirement that software ensure that each such data structure is modified only when no logical processor with a current VMCS that references it is in VMX non-root operation. That requirement does not apply to the posted-interrupt descriptor. There is a requirement, however, that such modifications be done using locked read-modify-write instructions.

If the “external-interrupt exiting” VM-execution control is 1, any unmasked external interrupt causes a VM exit (see Section 25.2). If the “process posted interrupts” VM-execution control is also 1, this behavior is changed and the processor handles an external interrupt as follows:14

1. The local APIC is acknowledged; this provides the processor core with an interrupt vector, called here the **physical vector**.
2. If the physical vector equals the posted-interrupt notification vector, the logical processor continues to the next step. Otherwise, a VM exit occurs as it would normally due to an external interrupt; the vector is saved in the VM-exit interruption-information field.
3. The processor clears the outstanding-notification bit in the posted-interrupt descriptor. This is done atomically so as to leave the remainder of the descriptor unmodified (e.g., with a locked AND operation).
4. The processor writes zero to the EOI register in the local APIC; this dismisses the interrupt with the posted-interrupt notification vector from the local APIC.
5. The logical processor performs a logical-OR of PIR into VIRR and clears PIR. No other agent can read or write a PIR bit (or group of bits) between the time it is read (to determine what to OR into VIRR) and when it is cleared.
6. The logical processor sets RVI to be the maximum of the old value of RVI and the highest index of all bits that were set in PIR; if no bit was set in PIR, RVI is left unmodified.
7. The logical processor evaluates pending virtual interrupts as described in Section 29.2.1.

The logical processor performs the steps above in an uninterruptible manner. If step #7 leads to recognition of a virtual interrupt, the processor may deliver that interrupt immediately.

14. VM entry ensures that the “process posted interrupts” VM-execution control is 1 only if the “external-interrupt exiting” VM-execution control is also 1. See Section 26.2.1.1.
Steps #1 to #7 above occur when the interrupt controller delivers an unmasked external interrupt to the CPU core. This delivery can occur when the logical processor is in the active, HLT, or MWAIT states. If the logical processor had been in the active or MWAIT state before the arrival of the interrupt, it is in the active state following completion of step #7; if it had been in the HLT state, it returns to the HLT state after step #7 (if a pending virtual interrupt was recognized, the logical processor may immediately wake from the HLT state).
CHAPTER 30
VMX INSTRUCTION REFERENCE

NOTE
This chapter was previously located in the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B as chapter 5.

30.1 OVERVIEW
This chapter describes the virtual-machine extensions (VMX) for the Intel 64 and IA-32 architectures. VMX is intended to support virtualization of processor hardware and a system software layer acting as a host to multiple guest software environments. The virtual-machine extensions (VMX) includes five instructions that manage the virtual-machine control structure (VMCS), four instructions that manage VMX operation, two TLB-management instructions, and two instructions for use by guest software. Additional details of VMX are described in Chapter 23 through Chapter 29.

The behavior of the VMCS-maintenance instructions is summarized below:

- **VMPTRLD** — This instruction takes a single 64-bit source operand that is in memory. It makes the referenced VMCS active and current, loading the current-VMCS pointer with this operand and establishes the current VMCS based on the contents of VMCS-data area in the referenced VMCS region. Because this makes the referenced VMCS active, a logical processor may start maintaining on the processor some of the VMCS data for the VMCS.

- **VMPTRST** — This instruction takes a single 64-bit destination operand that is in memory. The current-VMCS pointer is stored into the destination operand.

- **VMCLEAR** — This instruction takes a single 64-bit operand that is in memory. The instruction sets the launch state of the VMCS referenced by the operand to “clear”, renders that VMCS inactive, and ensures that data for the VMCS have been written to the VMCS-data area in the referenced VMCS region. If the operand is the same as the current-VMCS pointer, that pointer is made invalid.

- **VMREAD** — This instruction reads a component from a VMCS (the encoding of that field is given in a register operand) and stores it into a destination operand that may be a register or in memory.

- **VMWRITE** — This instruction writes a component to a VMCS (the encoding of that field is given in a register operand) from a source operand that may be a register or in memory.

The behavior of the VMX management instructions is summarized below:

- **VMLAUNCH** — This instruction launches a virtual machine managed by the VMCS. A VM entry occurs, transferring control to the VM.

- **VMRESUME** — This instruction resumes a virtual machine managed by the VMCS. A VM entry occurs, transferring control to the VM.

- **VMXOFF** — This instruction causes the processor to leave VMX operation.

- **VMXON** — This instruction takes a single 64-bit source operand that is in memory. It causes a logical processor to enter VMX root operation and to use the memory referenced by the operand to support VMX operation.

The behavior of the VMX-specific TLB-management instructions is summarized below:

- **INVEPT** — This instruction invalidates entries in the TLBs and paging-structure caches that were derived from extended page tables (EPT).

- **INVVPID** — This instruction invalidates entries in the TLBs and paging-structure caches based on a Virtual-Processor Identifier (VPID).

None of the instructions above can be executed in compatibility mode; they generate invalid-opcode exceptions if executed in compatibility mode.

The behavior of the guest-available instructions is summarized below:

- **VMCALL** — This instruction allows software in VMX non-root operation to call the VMM for service. A VM exit occurs, transferring control to the VMM.
• **VMFUNC** — This instruction allows software in VMX non-root operation to invoke a VM function (processor functionality enabled and configured by software in VMX root operation) without a VM exit.

### 30.2 CONVENTIONS

The operation sections for the VMX instructions in Section 30.3 use the pseudo-function VMexit, which indicates that the logical processor performs a VM exit.

The operation sections also use the pseudo-functions VMsucceed, VMfail, VMfailInvalid, and VMfailValid. These pseudo-functions signal instruction success or failure by setting or clearing bits in RFLAGS and, in some cases, by writing the VM-instruction error field. The following pseudocode fragments detail these functions:

```plaintext
VMsucceed:
    CF ← 0;
    PF ← 0;
    AF ← 0;
    ZF ← 0;
    SF ← 0;
    OF ← 0;

VMfail(ErrorCode):
    IF VMCS pointer is valid
    THEN VMfailValid(ErrorCode);
    ELSE VMfailInvalid;
    FI;

VMfailInvalid:
    CF ← 1;
    PF ← 0;
    AF ← 0;
    ZF ← 0;
    SF ← 0;
    OF ← 0;

VMfailValid(ErrorCode): // executed only if there is a current VMCS
    CF ← 0;
    PF ← 0;
    AF ← 0;
    ZF ← 1;
    SF ← 0;
    OF ← 0;
    Set the VM-instruction error field to ErrorCode;
```

The different VM-instruction error numbers are enumerated in Section 30.4, “VM Instruction Error Numbers”.

### 30.3 VMX INSTRUCTIONS

This section provides detailed descriptions of the VMX instructions.
INVEPT— Invalidate Translations Derived from EPT

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 80</td>
<td>INVEPT r64, m128</td>
<td>Invalidates EPT-derived entries in the TLBs and paging-structure caches (in 64-bit mode)</td>
</tr>
<tr>
<td>66 0F 38 80</td>
<td>INVEPT r32, m128</td>
<td>Invalidates EPT-derived entries in the TLBs and paging-structure caches (outside 64-bit mode)</td>
</tr>
</tbody>
</table>

Description

Invalidates mappings in the translation lookaside buffers (TLBs) and paging-structure caches that were derived from extended page tables (EPT). (See Chapter 28, "VMX Support for Address Translation"). Invalidation is based on the INVEPT type specified in the register operand and the INVEPT descriptor specified in the memory operand.

Outside IA-32e mode, the register operand is always 32 bits, regardless of the value of CS.D; in 64-bit mode, the register operand has 64 bits (the instruction cannot be executed in compatibility mode).

The INVEPT types supported by a logical processors are reported in the IA32_VMX_EPT_VPID_CAP MSR (see Appendix A, "VMX Capability Reporting Facility"). There are two INVEPT types currently defined:

- Single-context invalidation. If the INVEPT type is 1, the logical processor invalidates all mappings associated with bits 51:12 of the EPT pointer (EPTP) specified in the INVEPT descriptor. It may invalidate other mappings as well.
- Global invalidation: If the INVEPT type is 2, the logical processor invalidates mappings associated with all EPTPs.

If an unsupported INVEPT type is specified, the instruction fails.

INVEPT invalidates all the specified mappings for the indicated EPTP(s) regardless of the VPID and PCID values with which those mappings may be associated.

The INVEPT descriptor comprises 128 bits and contains a 64-bit EPTP value in bits 63:0 (see Figure 30-1).

```
127 64 63 0
Reserved (must be zero) EPT pointer (EPTP)
```

Figure 30-1. INVEPT Descriptor

Operation

IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
    THEN #UD;
ELSIF in VMX non-root operation
    THEN VM exit;
ELSIF CPL > 0
    THEN #GP(0);
ELSE
    INVEPT_TYPE ← value of register operand;
    IF IA32_VMX_EPT_VPID_CAP MSR indicates that processor does not support INVEPT_TYPE
        THEN VMfail(Invalid operand to INVEPT/INVVPID);
    ELSE
        // INVEPT_TYPE must be 1 or 2
        INVEPT_DESC ← value of memory operand;
        EPTP ← INVEPT_DESC[63:0];
CASE INVEPT_TYPE OF
  1:  // single-context invalidation
      IF VM entry with the "enable EPT" VM execution control set to 1
          would fail due to the EPTP value
          THEN VMfail(Invalid operand to INVEPT/INVVPID);
          ELSE
              Invalidate mappings associated with EPTP[51:12];
              VMsucceed;
      FI;
  BREAK;
  2:  // global invalidation
      Invalidate mappings associated with all EPTPs;
      VMsucceed;
      BREAK;
ESAC;
FI;

Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
If the memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains an unusable segment.
If the source operand is located in an execute-only code segment.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory operand effective address is outside the SS segment limit.
If the SS register contains an unusable segment.
#UD If not in VMX operation.
If the logical processor does not support EPT (IA32_VMX_PROCBASED_CTLS2[33]=0).
If the logical processor supports EPT (IA32_VMX_PROCBASED_CTLS2[33]=1) but does not
support the INVEPT instruction (IA32_VMX_EPT_VPID_CAP[20]=0).

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The INVEPT instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The INVEPT instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
If the memory operand is in the CS, DS, ES, FS, or GS segments and the memory address is
in a non-canonical form.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory operand is in the SS segment and the memory address is in a non-canonical
form.
#UD If not in VMX operation.
If the logical processor does not support EPT (IA32_VMX_PROCBASED_CNTL2[33]=0).
If the logical processor supports EPT (IA32_VMX_PROCBASED_CNTL2[33]=1) but does not support the INVEPT instruction (IA32_VMX_EPT_VPID_CAP[20]=0).
INVVPID— Invalidate Translations Based on VPID

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F 38 81</td>
<td>INVVPID r64, m128</td>
<td>Invalidates entries in the TLBs and paging-structure caches based on VPID (in 64-bit mode)</td>
</tr>
<tr>
<td>66 0F 38 81</td>
<td>INVVPID r32, m128</td>
<td>Invalidates entries in the TLBs and paging-structure caches based on VPID (outside 64-bit mode)</td>
</tr>
</tbody>
</table>

**Description**

Invalidates mappings in the translation lookaside buffers (TLBs) and paging-structure caches based on virtual-processor identifier (VPID). (See Chapter 28, “VMX Support for Address Translation”.) Invalidation is based on the **INVVPID type** specified in the register operand and the **INVVPID descriptor** specified in the memory operand.

Outside IA-32e mode, the register operand is always 32 bits, regardless of the value of CS.D; in 64-bit mode, the register operand has 64 bits (the instruction cannot be executed in compatibility mode).

The INVVPID types supported by a logical processors are reported in the IA32_VMX_EPT_VPID_CAP MSR (see Appendix A, “VMX Capability Reporting Facility”). There are four INVVPID types currently defined:

- **Individual-address invalidation**: If the INVVPID type is 0, the logical processor invalidates mappings for the linear address and VPID specified in the INVVPID descriptor. In some cases, it may invalidate mappings for other linear addresses (or other VPIIDs) as well.

- **Single-context invalidation**: If the INVVPID type is 1, the logical processor invalidates all mappings tagged with the VPID specified in the INVVPID descriptor. In some cases, it may invalidate mappings for other VPIIDs as well.

- **All-contexts invalidation**: If the INVVPID type is 2, the logical processor invalidates all mappings tagged with all VPIIDs except VPID 0000H. In some cases, it may invalidate translations with VPID 0000H as well.

- **Single-context invalidation, retaining global translations**: If the INVVPID type is 3, the logical processor invalidates all mappings tagged with the VPID specified in the INVVPID descriptor except global translations. In some cases, it may invalidate global translations (and mappings with other VPIIDs) as well. See the “Caching Translation Information” section in Chapter 4 of the *IA-32 Intel Architecture Software Developer’s Manual, Volumes 3A* for information about global translations.

If an unsupported INVVPID type is specified, the instruction fails.

INVVPID invalidates all the specified mappings for the indicated VPID(s) regardless of the EPTP and PCID values with which those mappings may be associated.

The INVVPID descriptor comprises 128 bits and consists of a VPID and a linear address as shown in Figure 30-2.
Operation

IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
    THEN #UD;
ELSIF in VMX non-root operation
    THEN VM exit;
ELSIF CPL > 0
    THEN #GP(0);
ELSE
    INVVPID_TYPE ← value of register operand;
    IF IA32_VMX_EPT_VPID_CAP MSR indicates that processor does not support
        INVVPID_TYPE
        THEN VMfail(Invalid operand to INVEPT/INVVPID);
        ELSE // INVVPID_TYPE must be in the range 0–3
            INVVPID_DESC ← value of memory operand;
            IF INVVPID_DESC[63:16] ≠ 0
                THEN VMfail(Invalid operand to INVEPT/INVVPID);
            ELSE
                CASE INVVPID_TYPE OF
                    0: // individual-address invalidation
                        VPID ← INVVPID_DESC[15:0];
                        IF VPID = 0
                            THEN VMfail(Invalid operand to INVEPT/INVVPID);
                            ELSE
                                GL_ADDR ← INVVPID_DESC[127:64];
                                IF (GL_ADDR is not in a canonical form)
                                    THEN
                                        VMfail(Invalid operand to INVEPT/INVVPID);
                                    ELSE
                                        Invalidate mappings for GL_ADDR tagged with VPID;
                                        VMsucceed;
                                FI;
                            FI;
                        BREAK;
                    1: // single-context invalidation
                        VPID ← INVVPID_DESC[15:0];
                        IF VPID = 0
                            THEN VMfail(Invalid operand to INVEPT/INVVPID);
                            ELSE
                                Invalidate all mappings tagged with VPID;
                                VMsucceed;
                            FI;
                        BREAK;
                    2: // all-context invalidation
                        Invalidate all mappings tagged with all non-zero VPIDs;
                        VMsucceed;
                BREAK;
                    3: // single-context invalidation retaining globals
                        VPID ← INVVPID_DESC[15:0];
                        IF VPID = 0
                            THEN VMfail(Invalid operand to INVEPT/INVVPID);
                            ELSE
                                Invalidate all mappings tagged with VPID except global translations;
                                VMsucceed;
                    FI;
VMX INSTRUCTION REFERENCE

FI;
BREAK;
ESAC;
FI;
FI;
FI;
FI;

Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
If the memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains an unusable segment.
If the source operand is located in an execute-only code segment.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory operand effective address is outside the SS segment limit.
If the SS register contains an unusable segment.
#UD If not in VMX operation.
If the logical processor does not support VPIDs (IA32_VMX_PROCBASED_CTLS2[37]=0).
If the logical processor supports VPIDs (IA32_VMX_PROCBASED_CTLS2[37]=1) but does not support the INVVPID instruction (IA32_VMX_EPT_VPID_CAP[32]=0).

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The INVVPID instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The INVVPID instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
If the memory operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory destination operand is in the SS segment and the memory address is in a non-canonical form.
#UD If not in VMX operation.
If the logical processor does not support VPIDs (IA32_VMX_PROCBASED_CTLS2[37]=0).
If the logical processor supports VPIDs (IA32_VMX_PROCBASED_CTLS2[37]=1) but does not support the INVVPID instruction (IA32_VMX_EPT_VPID_CAP[32]=0).
VMCALL—Call to VM Monitor

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C1</td>
<td>VMCALL</td>
<td>Call to VM monitor by causing VM exit.</td>
</tr>
</tbody>
</table>

**Description**

This instruction allows guest software can make a call for service into an underlying VM monitor. The details of the programming interface for such calls are VMM-specific; this instruction does nothing more than cause a VM exit, registering the appropriate exit reason.

Use of this instruction in VMX root operation invokes an SMM monitor (see Section 34.15.2). This invocation will activate the dual-monitor treatment of system-management interrupts (SMIs) and system-management mode (SMM) if it is not already active (see Section 34.15.6).

**Operation**

IF not in VMX operation
    THEN #UD;
ELSIF in VMX non-root operation
    THEN VM exit;
ELSIF (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
    THEN #UD;
ELSIF CPL > 0
    THEN #GP(0);
ELSIF in SMM or the logical processor does not support the dual-monitor treatment of SMIs and SMM or the valid bit in the IA32_SMM_MONITOR_CTL MSR is clear
    THEN VMfail (VMCALL executed in VMX root operation);
ELSIF dual-monitor treatment of SMIs and SMM is active
    THEN perform an SMM VM exit (see Section 34.15.2);
ELSIF current-VMCS pointer is not valid
    THEN VMfailInvalid;
ELSIF launch state of current VMCS is not clear
    THEN VMfailValid(VMCALL with non-clear VMCS);
ELSIF VM-exit control fields are not valid (see Section 34.15.6.1)
    THEN VMfailValid (VMCALL with invalid VM-exit control fields);
ELSE
    enter SMM;
    read revision identifier in MSEG;
    IF revision identifier does not match that supported by processor
        THEN
            leave SMM;
            VMfailValid(VMCALL with incorrect MSEG revision identifier);
        ELSE
            read SMM-monitor features field in MSEG (see Section 34.15.6.2);
            IF features field is invalid
                THEN
                    leave SMM;
                    VMfailValid(VMCALL with invalid SMM-monitor features);
                ELSE
                    activate dual-monitor treatment of SMIs and SMM (see Section 34.15.6);
                FI;
            FI;
        FI;
Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0 and the logical processor is in VMX root operation.
#UD If executed outside VMX operation.

Real-Address Mode Exceptions
#UD If executed outside VMX operation.

Virtual-8086 Mode Exceptions
#UD If executed outside VMX non-root operation.

Compatibility Mode Exceptions
#UD If executed outside VMX non-root operation.

64-Bit Mode Exceptions
#UD If executed outside VMX operation.
VMCLEAR—Clear Virtual-Machine Control Structure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 0F C7 /6</td>
<td>VMCLEAR m64</td>
<td>Copy VMCS data to VMCS region in memory.</td>
</tr>
</tbody>
</table>

Description

This instruction applies to the VMCS whose VMCS region resides at the physical address contained in the instruction operand. The instruction ensures that VMCS data for that VMCS (some of these data may be currently maintained on the processor) are copied to the VMCS region in memory. It also initializes parts of the VMCS region (for example, it sets the launch state of that VMCS to clear). See Chapter 24, “Virtual-Machine Control Structures”.

The operand of this instruction is always 64 bits and is always in memory. If the operand is the current-VMCS pointer, then that pointer is made invalid (set to FFFFFFFF_FFFFFFFFH).

Note that the VMCLEAR instruction might not explicitly write any VMCS data to memory; the data may be already resident in memory before the VMCLEAR is executed.

Operation

IF (register operand) or (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
    THEN #UD;
ELSIF in VMX non-root operation
    THEN VM exit;
ELSIF CPL > 0
    THEN #GP(0);
ELSE
    addr ← contents of 64-bit in-memory operand;
    IF addr is not 4KB-aligned OR
    addr sets any bits beyond the physical-address width1
    THEN VMfail(VMCLEAR with invalid physical address);
    ELSIF addr = VMXON pointer
    THEN VMfail(VMCLEAR with VMXON pointer);
    ELSE
        ensure that data for VMCS referenced by the operand is in memory;
        initialize implementation-specific data in VMCS region;
        launch state of VMCS referenced by the operand ← “clear”
        IF operand addr = current-VMCS pointer
            THEN current-VMCS pointer ← FFFFFFFF_FFFFFFFFH;
            FI;
        VMsucceed;
        FI;
    FI;

Flags Affected

See the operation section and Section 30.2.

Protected Mode Exceptions

#GP(0)  If the current privilege level is not 0.
        If the memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains an unusable segment.
        If the operand is located in an execute-only code segment.

1. If IA32_VMX_BASIC[48] is read as 1, VMfail occurs if addr sets any bits in the range 63:32; see Appendix A.1.
VMX INSTRUCTION REFERENCE

#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the memory operand effective address is outside the SS segment limit.
    If the SS register contains an unusable segment.
#UD If operand is a register.
    If not in VMX operation.

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The VMCLEAR instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The VMCLEAR instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
    If the source operand is in the CS, DS, ES, FS, or GS segments and the memory address is in
    a non-canonical form.
#PF(fault-code) If a page fault occurs in accessing the memory operand.
#SS(0) If the source operand is in the SS segment and the memory address is in a non-canonical
    form.
#UD If operand is a register.
    If not in VMX operation.
VMFUNC—Invoke VM function

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 D4</td>
<td>VMFUNC</td>
<td>Invoke VM function specified in EAX.</td>
</tr>
</tbody>
</table>

Description
This instruction allows software in VMX non-root operation to invoke a VM function, which is processor functionality enabled and configured by software in VMX root operation. The value of EAX selects the specific VM function being invoked.

The behavior of each VM function (including any additional fault checking) is specified in Section 25.5.5, "VM Functions".

Operation
Perform functionality of the VM function specified in EAX;

Flags Affected
Depends on the VM function specified in EAX. See Section 25.5.5, "VM Functions".

Protected Mode Exceptions (not including those defined by specific VM functions)
- #UD If executed outside VMX non-root operation.
  - If “enable VM functions” VM-execution control is 0.
  - If EAX ≥ 64.

Real-Address Mode Exceptions
Same exceptions as in protected mode.

Virtual-8086 Exceptions
Same exceptions as in protected mode.

Compatibility Mode Exceptions
Same exceptions as in protected mode.

64-Bit Mode Exceptions
Same exceptions as in protected mode.
VMLAUNCH/VMRESUME—Launch/Resume Virtual Machine

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C2</td>
<td>VMLAUNCH</td>
<td>Launch virtual machine managed by current VMCS.</td>
</tr>
<tr>
<td>0F 01 C3</td>
<td>VMRESUME</td>
<td>Resume virtual machine managed by current VMCS.</td>
</tr>
</tbody>
</table>

Description

Effects a VM entry managed by the current VMCS.

- VMLAUNCH fails if the launch state of current VMCS is not “clear”. If the instruction is successful, it sets the launch state to “launched.”
- VMRESUME fails if the launch state of the current VMCS is not “launched.”

If VM entry is attempted, the logical processor performs a series of consistency checks as detailed in Chapter 26, “VM Entries”. Failure to pass checks on the VMX controls or on the host-state area passes control to the instruction following the VMLAUNCH or VMRESUME instruction. If these pass but checks on the guest-state area fail, the logical processor loads state from the host-state area of the VMCS, passing control to the instruction referenced by the RIP field in the host-state area.

VM entry is not allowed when events are blocked by MOV SS or POP SS. Neither VMLAUNCH nor VMRESUME should be used immediately after either MOV to SS or POP to SS.

Operation

IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
THEN #UD;
ELSIF in VMX non-root operation
THEN VMexit;
ELSIF CPL > 0
THEN #GP(0);
ELSIF current-VMCS pointer is not valid
THEN VMfailInvalid;
ELSIF events are being blocked by MOV SS
THEN VMfailValid(VM entry with events blocked by MOV SS);
ELSIF (VMLAUNCH and launch state of current VMCS is not “clear”)
THEN VMfailValid(VMLAUNCH with non-clear VMCS);
ELSIF (VMRESUME and launch state of current VMCS is not “launched”)
THEN VMfailValid(VMRESUME with non-launched VMCS);
ELSE

Check settings of VMX controls and host-state area;
IF invalid settings
THEN VMfailValid(VM entry with invalid VMX-control field(s)) or
VMfailValid(VM entry with invalid host-state field(s)) or
VMfailValid(VM entry with invalid executive-VMCS pointer)) or
VMfailValid(VM entry with non-launched executive VMCS) or
VMfailValid(VM entry with executive-VMCS pointer not VMXON pointer) or
VMfailValid(VM entry with invalid VM-execution control fields in executive VMCS)
as appropriate;
ELSE

Attempt to load guest state and PDPTRs as appropriate;
clear address-range monitoring;
IF failure in checking guest state or PDPTRs
THEN VM entry fails (see Section 26.7);
ELSE
   Attempt to load MSRs from VM-entry MSR-load area;
   IF failure
      THEN VM entry fails
      (see Section 26.7);
   ELSE
      IF VMLAUNCH
         THEN launch state of VMCS ← “launched”;
      FI;
      IF in SMM and “entry to SMM” VM-entry control is 0
         THEN
            IF “deactivate dual-monitor treatment” VM-entry
               control is 0
               THEN SMM-transfer VMCS pointer ←
                    current-VMCS pointer;
               FI;
            IF executive-VMCS pointer is VMXON pointer
               THEN current-VMCS pointer ←
                    VMCS-link pointer;
               ELSE current-VMCS pointer ←
                    executive-VMCS pointer;
            FI;
            leave SMM;
      FI;
      VM entry succeeds;
   FI;
FI;
FI;
Further details of the operation of the VM-entry appear in Chapter 26.

Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions
#GP(0) If the current privilege level is not 0.
#UD If executed outside VMX operation.

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The VMLAUNCH and VMRESUME instructions are not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The VMLAUNCH and VMRESUME instructions are not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
#UD If executed outside VMX operation.
VMX INSTRUCTION REFERENCE

VMPTRLD—Load Pointer to Virtual-Machine Control Structure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C7 /6</td>
<td>VMPTRLD m64</td>
<td>Loads the current VMCS pointer from memory.</td>
</tr>
</tbody>
</table>

**Description**

Marks the current-VMCS pointer valid and loads it with the physical address in the instruction operand. The instruction fails if its operand is not properly aligned, sets unsupported physical-address bits, or is equal to the VMXON pointer. In addition, the instruction fails if the 32 bits in memory referenced by the operand do not match the VMCS revision identifier supported by this processor.2

The operand of this instruction is always 64 bits and is always in memory.

**Operation**

IF (register operand) or (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
THEN #UD;
ELSIF in VMX non-root operation
THEN VMexit;
ELSIF CPL > 0
THEN #GP(0);
ELSE
addr ← contents of 64-bit in-memory source operand;
IF addr is not 4KB-aligned OR
addr sets any bits beyond the physical-address width3
THEN VMfail(VMPTRLD with invalid physical address);
ELSIF addr = VMXON pointer
THEN VMfail(VMPTRLD with VMXON pointer);
ELSE
rev ← 32 bits located at physical address addr;
IF rev[30:0] ≠ VMCS revision identifier supported by processor OR
rev[31] = 1 AND processor does not support 1-setting of “VMCS shadowing”
THEN VMfail(VMPTRLD with incorrect VMCS revision identifier);
ELSE
current-VMCS pointer ← addr;
VMsucceed;
FI;
FI;
FI;

**Flags Affected**

See the operation section and Section 30.2.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.
#GP(0) If the memory source operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#GP(0) If the DS, ES, FS, or GS register contains an unusable segment.

---

2. Software should consult the VMX capability MSR VMX_BASIC to discover the VMCS revision identifier supported by this processor (see Appendix A, “VMX Capability Reporting Facility”).

3. If IA32_VMX_BASIC[48] is read as 1, VMfail occurs if addr sets any bits in the range 63:32; see Appendix A.1.
If the source operand is located in an execute-only code segment.

#PF(fault-code) If a page fault occurs in accessing the memory source operand.

#SS(0) If the memory source operand effective address is outside the SS segment limit.
If the SS register contains an unusable segment.

#UD If operand is a register.
If not in VMX operation.

**Real-Address Mode Exceptions**

#UD If executed outside VMX root operation.

**Virtual-8086 Mode Exceptions**

#UD The VMPTRLD instruction is not recognized in virtual-8086 mode.

**Compatibility Mode Exceptions**

#UD The VMPTRLD instruction is not recognized in compatibility mode.

**64-Bit Mode Exceptions**

#GP(0) If the current privilege level is not 0.
If the source operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs in accessing the memory source operand.

#SS(0) If the source operand is in the SS segment and the memory address is in a non-canonical form.

#UD If operand is a register.
If not in VMX operation.
VMX INSTRUCTION REFERENCE

VMPTRST—Store Pointer to Virtual-Machine Control Structure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C7 /7</td>
<td>VMPTRST m64</td>
<td>Stores the current VMCS pointer into memory.</td>
</tr>
</tbody>
</table>

**Description**
Stores the current-VMCS pointer into a specified memory address. The operand of this instruction is always 64 bits and is always in memory.

**Operation**

IF (register operand) or (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)  
THEN #UD;  
ELSIF in VMX non-root operation  
THEN VMexit;  
ELSIF CPL > 0  
THEN #GP(0);  
ELSE  
   64-bit in-memory destination operand ← current-VMCS pointer;  
   VMsucceed;  
FI;

**Flags Affected**
See the operation section and Section 30.2.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.  
If the memory destination operand effective address is outside the CS, DS, ES, FS, or GS segment limit.  
If the DS, ES, FS, or GS register contains an unusable segment.  
If the destination operand is located in a read-only data segment or any code segment.

#PF(fault-code) If a page fault occurs in accessing the memory destination operand.

#SS(0) If the memory destination operand effective address is outside the SS segment limit.  
If the SS register contains an unusable segment.

#UD If operand is a register.  
If not in VMX operation.

**Real-Address Mode Exceptions**

#UD If executed outside VMX root operation.

**Virtual-8086 Mode Exceptions**

#UD The VMPTRST instruction is not recognized in virtual-8086 mode.

**Compatibility Mode Exceptions**

#UD The VMPTRST instruction is not recognized in compatibility mode.
64-Bit Mode Exceptions

#GP(0)  If the current privilege level is not 0.
       If the destination operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.

#PF(fault-code)  If a page fault occurs in accessing the memory destination operand.

#SS(0)  If the destination operand is in the SS segment and the memory address is in a non-canonical form.

#UD  If operand is a register.
       If not in VMX operation.
VMREAD—Read Field from Virtual-Machine Control Structure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 78</td>
<td>VMREAD r/m64, r64</td>
<td>Reads a specified VMCS field (in 64-bit mode).</td>
</tr>
<tr>
<td>0F 78</td>
<td>VMREAD r/m32, r32</td>
<td>Reads a specified VMCS field (outside 64-bit mode).</td>
</tr>
</tbody>
</table>

Description

Reads a specified field from a VMCS and stores it into a specified destination operand (register or memory). In VMX root operation, the instruction reads from the current VMCS. If executed in VMX non-root operation, the instruction reads from the VMCS referenced by the VMCS link pointer field in the current VMCS.

The VMCS field is specified by the VMCS-field encoding contained in the register source operand. Outside IA-32e mode, the source operand has 32 bits, regardless of the value of CS.D. In 64-bit mode, the source operand has 64 bits.

The effective size of the destination operand, which may be a register or in memory, is always 32 bits outside IA-32e mode (the setting of CS.D is ignored with respect to operand size) and 64 bits in 64-bit mode. If the VMCS field specified by the source operand is shorter than this effective operand size, the high bits of the destination operand are cleared to 0. If the VMCS field is longer, then the high bits of the field are not read.

Note that any faults resulting from accessing a memory destination operand can occur only after determining, in the operation section below, that the relevant VMCS pointer is valid and that the specified VMCS field is supported.

Operation

IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
    THEN #UD;
ELSIF in VMX non-root operation AND (“VMCS shadowing” is 0 OR source operand sets bits in range 63:15 OR VMREAD bit corresponding to bits 14:0 of source operand is 1)4
    THEN VMexit;
ELSIF CPL > 0
    THEN #GP(0);
ELSIF (in VMX root operation AND current-VMCS pointer is not valid) OR
    (in VMX non-root operation AND VMCS link pointer is not valid)
    THEN VMfailInvalid;
ELSIF source operand does not correspond to any VMCS field
    THEN VMfailValid(VMREAD/VMWRITE from/to unsupported VMCS component);
ELSE
    IF in VMX root operation
        THEN destination operand ← contents of field indexed by source operand in current VMCS;
    ELSE
        destination operand ← contents of field indexed by source operand in VMCS referenced by VMCS link pointer;
    FI;
    VMsucceed;
FI;

Flags Affected

See the operation section and Section 30.2.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.

4. The VMREAD bit for a source operand is defined as follows. Let x be the value of bits 14:0 of the source operand and let addr be the VMREAD-bitmap address. The corresponding VMREAD bit is in bit position x & 7 of the byte at physical address addr | (x >> 3).
If a memory destination operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains an unusable segment.
If the destination operand is located in a read-only data segment or any code segment.

#PF(fault-code) If a page fault occurs in accessing a memory destination operand.
#SS(0) If a memory destination operand effective address is outside the SS segment limit.
#UD If the SS register contains an unusable segment.
#UD If not in VMX operation.

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The VMREAD instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions
#UD The VMREAD instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If the current privilege level is not 0.
If the memory destination operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.
#PF(fault-code) If a page fault occurs in accessing a memory destination operand.
#SS(0) If the memory destination operand is in the SS segment and the memory address is in a non-canonical form.
#UD If not in VMX operation.
VMRESUME—Resume Virtual Machine

See VMLAUNCH/VMRESUME—Launch/Resume Virtual Machine.
VMWRITE—Write Field to Virtual-Machine Control Structure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 79</td>
<td>VMWRITE r64, r/m64</td>
<td>Writes a specified VMCS field (in 64-bit mode)</td>
</tr>
<tr>
<td>0F 79</td>
<td>VMWRITE r32, r/m32</td>
<td>Writes a specified VMCS field (outside 64-bit mode)</td>
</tr>
</tbody>
</table>

**Description**

Writes the contents of a primary source operand (register or memory) to a specified field in a VMCS. In VMX root operation, the instruction writes to the current VMCS. If executed in VMX non-root operation, the instruction writes to the VMCS referenced by the VMCS link pointer field in the current VMCS.

The VMCS field is specified by the VMCS-field encoding contained in the register secondary source operand. Outside IA-32e mode, the secondary source operand is always 32 bits, regardless of the value of CS.D. In 64-bit mode, the secondary source operand has 64 bits.

The effective size of the primary source operand, which may be a register or in memory, is always 32 bits outside IA-32e mode (the setting of CS.D is ignored with respect to operand size) and 64 bits in 64-bit mode. If the VMCS field specified by the secondary source operand is shorter than this effective operand size, the high bits of the primary source operand are ignored. If the VMCS field is longer, then the high bits of the field are cleared to 0.

Note that any faults resulting from accessing a memory source operand occur after determining, in the operation section below, that the relevant VMCS pointer is valid but before determining if the destination VMCS field is supported.

**Operation**

IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0)
  THEN #UD;
ELSIF in VMX non-root operation AND (“VMCS shadowing” is 0 OR secondary source operand sets bits in range 63:15 OR VMWRITE bit corresponding to bits 14:0 of secondary source operand is 1)5
  THEN VMexit;
ELSIF CPL > 0
  THEN #GP(0);
ELSIF (in VMX root operation AND current-VMCS pointer is not valid) OR (in VMX non-root operation AND VMCS-link pointer is not valid)
  THEN VMfailInvalid;
ELSIF secondary source operand does not correspond to any VMCS field
  THEN VMfailInvalid(VMREAD/VMWRITE from/to unsupported VMCS component);
ELSIF VMCS field indexed by secondary source operand is a VM-exit information field AND processor does not support writing to such fields6
  THEN VMfailInvalid(VMWRITE to read-only VMCS component);
ELSE
  IF in VMX root operation
    THEN field indexed by secondary source operand in current VMCS ← primary source operand;
    ELSE field indexed by secondary source operand in VMCS referenced by VMCS link pointer ← primary source operand;
  FI;
  VMsucceed;
FI;

5. The VMWRITE bit for a secondary source operand is defined as follows. Let \( x \) be the value of bits 14:0 of the secondary source operand and let \( addr \) be the VMWRITE-bitmap address. The corresponding VMWRITE bit is in bit position \( x \& 7 \) of the byte at physical address \( addr \ll 3 \).

6. Software can discover whether these fields can be written by reading the VMX capability MSR IA32_VMX_MISC (see Appendix A.6).
Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions

#GP(0)    If the current privilege level is not 0.
          If a memory source operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register contains an unusable segment.
          If the source operand is located in an execute-only code segment.

#PF(fault-code)  If a page fault occurs in accessing a memory source operand.
#SS(0)  If a memory source operand effective address is outside the SS segment limit.
          If the SS register contains an unusable segment.
#UD    If not in VMX operation.

Real-Address Mode Exceptions

#UD    If executed outside VMX root operation.

Virtual-8086 Mode Exceptions

#UD    The VMWRITE instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions

#UD    The VMWRITE instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions

#GP(0)    If the current privilege level is not 0.
          If the memory source operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.

#PF(fault-code)  If a page fault occurs in accessing a memory source operand.
#SS(0)  If the memory source operand is in the SS segment and the memory address is in a non-canonical form.
#UD    If not in VMX operation.
VMXOFF—Leave VMX Operation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 C4</td>
<td>VMXOFF</td>
<td>Leaves VMX operation.</td>
</tr>
</tbody>
</table>

Description
Takes the logical processor out of VMX operation, unblocks INIT signals, conditionally re-enables A20M, and clears any address-range monitoring.7

Operation
IF (not in VMX operation) or (CR0.PE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0) THEN #UD;
ELSIF in VMX non-root operation THEN VMexit;
ELSIF CPL > 0 THEN #GP(0);
ELSIF dual-monitor treatment of SMIs and SMM is active THEN VMfail(VMXOFF under dual-monitor treatment of SMIs and SMM);
ELSE
leave VMX operation;
unblock INIT;
IF IA32_SMM_MONITOR_CTL[2] = 0 THEN unblock SMIs;
IF outside SMX operation9 THEN unblock and enable A20M;
FI;
clear address-range monitoring;
VMsucceed;
FI;

Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions
#GP(0) If executed in VMX root operation with CPL > 0.
#UD If executed outside VMX operation.

Real-Address Mode Exceptions
#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions
#UD The VMXOFF instruction is not recognized in virtual-8086 mode.

---

7. See the information on MONITOR/MWAIT in Chapter 8, “Multiple-Processor Management,” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

8. Setting IA32_SMM_MONITOR_CTL[bit 2] to 1 prevents VMXOFF from unblocking SMIs regardless of the value of the register’s value bit (bit 0). Not all processors allow this bit to be set to 1. Software should consult the VMX capability MSR IA32_VMX_MISC (see Appendix A.6) to determine whether this is allowed.

9. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference.”
Compatibility Mode Exceptions
#UD The VMXOFF instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions
#GP(0) If executed in VMX root operation with CPL > 0.
#UD If executed outside VMX operation.
## VMXON—Enter VMX Operation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 0F C7 /6</td>
<td>VMXON m64</td>
<td>Enter VMX root operation.</td>
</tr>
</tbody>
</table>

### Description

Puts the logical processor in VMX operation with no current VMCS, blocks INIT signals, disables A20M, and clears any address-range monitoring established by the MONITOR instruction.\(^{10}\)

The operand of this instruction is a 4KB-aligned physical address (the VMXON pointer) that references the VMXON region, which the logical processor may use to support VMX operation. This operand is always 64 bits and is always in memory.

### Operation

\[
\text{IF (register operand) or (CR0.PE = 0) or (CR4.VMXE = 0) or (RFLAGS.VM = 1) or (IA32_EFER.LMA = 1 and CS.L = 0) THEN #UD;}
\]

\[
\text{ELSIF not in VMX operation THEN}
\]

\[
\text{IF (CPL > 0) or (in A20M mode) or (the values of CR0 and CR4 are not supported in VMX operation; see Section 23.8) or (bit 0 (lock bit) of IA32_FEATURE_CONTROL MSR is clear) or (in SMX operation and bit 1 of IA32_FEATURE_CONTROL MSR is clear) or (outside SMX operation and bit 2 of IA32_FEATURE_CONTROL MSR is clear) THEN #GP(0);}
\]

\[
\text{ELSE addr ← contents of 64-bit in-memory source operand;}
\]

\[
\text{IF addr is not 4KB-aligned or addr sets any bits beyond the physical-address width}^{12}\text{ THEN VMfailInvalid;}
\]

\[
\text{ELSE rev ← 32 bits located at physical address addr;}
\]

\[
\text{IF rev[30:0] ≠ VMCS revision identifier supported by processor OR rev[31] = 1 THEN VMfailInvalid;}
\]

\[
\text{ELSE current-VMCS pointer ← FFFFFFFF_FFFFFFFH;}
\]

\[
\text{enter VMX operation; block INIT signals; block and disable A20M; clear address-range monitoring; VMsucceed;}
\]

\[
\text{FI;}
\]

\[
\text{FI;}
\]

\[
\text{ELSIF in VMX non-root operation THEN VMexit;}
\]

---

10. See the information on MONITOR/MWAIT in Chapter 8, “Multiple-Processor Management,” of the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*.

11. A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference.”

12. If IA32_VMX_BASIC[48] is read as 1, VMfailInvalid occurs if addr sets any bits in the range 63:32; see Appendix A.1.
ELSIF CPL > 0
    THEN #GP(0);
    ELSE VMfail("VMXON executed in VMX root operation");
FI;

Flags Affected
See the operation section and Section 30.2.

Protected Mode Exceptions

#GP(0) If executed outside VMX operation with CPL>0 or with invalid CR0 or CR4 fixed bits.
If executed in A20M mode.
If the memory source operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains an unusable segment.
If the source operand is located in an execute-only code segment.

#PF(fault-code) If a page fault occurs in accessing the memory source operand.

#SS(0) If the memory source operand effective address is outside the SS segment limit.
If the SS register contains an unusable segment.

#UD If operand is a register.
If executed with CR4.VMXE = 0.

Real-Address Mode Exceptions

#UD If executed outside VMX root operation.

Virtual-8086 Mode Exceptions

#UD The VMXON instruction is not recognized in virtual-8086 mode.

Compatibility Mode Exceptions

#UD The VMXON instruction is not recognized in compatibility mode.

64-Bit Mode Exceptions

#GP(0) If executed outside VMX operation with CPL > 0 or with invalid CR0 or CR4 fixed bits.
If executed in A20M mode.
If the source operand is in the CS, DS, ES, FS, or GS segments and the memory address is in a non-canonical form.

#PF(fault-code) If a page fault occurs in accessing the memory source operand.

#SS(0) If the source operand is in the SS segment and the memory address is in a non-canonical form.

#UD If operand is a register.
If executed with CR4.VMXE = 0.
30.4 VM INSTRUCTION ERROR NUMBERS

For certain error conditions, the VM-instruction error field is loaded with an error number to indicate the source of the error. Table 30-1 lists VM-instruction error numbers.

<table>
<thead>
<tr>
<th>Error Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VMCALL executed in VMX root operation</td>
</tr>
<tr>
<td>2</td>
<td>VMCLEAR with invalid physical address</td>
</tr>
<tr>
<td>3</td>
<td>VMCLEAR with VMXON pointer</td>
</tr>
<tr>
<td>4</td>
<td>VMLAUNCH with non-clear VMCS</td>
</tr>
<tr>
<td>5</td>
<td>VMRESUME with non-launched VMCS</td>
</tr>
<tr>
<td>6</td>
<td>VMRESUME after VMXOFF (VMXOFF and VMXON between VMLAUNCH and VMRESUME)(^a)</td>
</tr>
<tr>
<td>7</td>
<td>VM entry with invalid control field(s)(^b,c)</td>
</tr>
<tr>
<td>8</td>
<td>VM entry with invalid host-state field(s)(^b)</td>
</tr>
<tr>
<td>9</td>
<td>VMPTRLD with invalid physical address</td>
</tr>
<tr>
<td>10</td>
<td>VMPTRLD with VMXON pointer</td>
</tr>
<tr>
<td>11</td>
<td>VMPTRLD with incorrect VMCS revision identifier</td>
</tr>
<tr>
<td>12</td>
<td>VMREAD/VMWRITE from/to unsupported VMCS component</td>
</tr>
<tr>
<td>13</td>
<td>VMWRITE to read-only VMCS component</td>
</tr>
<tr>
<td>15</td>
<td>VMXON executed in VMX root operation</td>
</tr>
<tr>
<td>16</td>
<td>VM entry with invalid executive-VMCS pointer(^b)</td>
</tr>
<tr>
<td>17</td>
<td>VM entry with non-launched executive VMCS(^b)</td>
</tr>
<tr>
<td>18</td>
<td>VM entry with executive-VMCS pointer not VMXON pointer (when attempting to deactivate the dual-monitor treatment of SMIs and SMM)(^b)</td>
</tr>
<tr>
<td>19</td>
<td>VMCALL with non-clear VMCS (when attempting to activate the dual-monitor treatment of SMIs and SMM)</td>
</tr>
<tr>
<td>20</td>
<td>VMCALL with invalid VM-exit control fields</td>
</tr>
<tr>
<td>22</td>
<td>VMCALL with incorrect MSEG revision identifier (when attempting to activate the dual-monitor treatment of SMIs and SMM)</td>
</tr>
<tr>
<td>23</td>
<td>VMXOFF under dual-monitor treatment of SMIs and SMM</td>
</tr>
<tr>
<td>24</td>
<td>VMCALL with invalid SMM-monitor features (when attempting to activate the dual-monitor treatment of SMIs and SMM)</td>
</tr>
<tr>
<td>25</td>
<td>VM entry with invalid VM-execution control fields in executive VMCS (when attempting to return from SMM)(^b,c)</td>
</tr>
<tr>
<td>26</td>
<td>VM entry with events blocked by MOV SS.</td>
</tr>
<tr>
<td>28</td>
<td>Invalid operand to INVEPT/INVVPID.</td>
</tr>
</tbody>
</table>

NOTES:

a. Earlier versions of this manual described this error as “VMRESUME with a corrupted VMCS”.

b. VM-entry checks on control fields and host-state fields may be performed in any order. Thus, an indication by error number of one cause does not imply that there are not also other errors. Different processors may give different error numbers for the same VMCS.

c. Error number 7 is not used for VM entries that return from SMM that fail due to invalid VM-execution control fields in the executive VMCS. Error number 25 is used for these cases.
31.1 VMX SYSTEM PROGRAMMING OVERVIEW

The Virtual Machine Monitor (VMM) is a software class used to manage virtual machines (VM). This chapter describes programming considerations for VMMs.

Each VM behaves like a complete physical machine and can run operating system (OS) and applications. The VMM software layer runs at the most privileged level and has complete ownership of the underlying system hardware. The VMM controls creation of a VM, transfers control to a VM, and manages situations that can cause transitions between the guest VMs and host VMM. The VMM allows the VMs to share the underlying hardware and yet provides isolation between the VMs. The guest software executing in a VM is unaware of any transitions that might have occurred between the VM and its host.

31.2 SUPPORTING PROCESSOR OPERATING MODES IN GUEST ENVIRONMENTS

Typically, VMMs transfer control to a VM using VMX transitions referred to as VM entries. The boundary conditions that define what a VM is allowed to execute in isolation are specified in a virtual-machine control structure (VMCS).

As noted in Section 23.8, processors may fix certain bits in CR0 and CR4 to specific values and not support other values. The first processors to support VMX operation require that CR0.PE and CR0.PG be 1 in VMX operation. Thus, a VM entry is allowed only to guests with paging enabled that are in protected mode or in virtual-8086 mode. Guest execution in other processor operating modes need to be specially handled by the VMM.

One example of such a condition is guest execution in real-mode. A VMM could support guest real-mode execution using at least two approaches:

- By using a fast instruction set emulator in the VMM.
- By using the similarity between real-mode and virtual-8086 mode to support real-mode guest execution in a virtual-8086 container. The virtual-8086 container may be implemented as a virtual-8086 container task within a monitor that emulates real-mode guest state and instructions, or by running the guest VM as the virtual-8086 container (by entering the guest with RFLAGS.VM1 set). Attempts by real-mode code to access privileged state outside the virtual-8086 container would trap to the VMM and would also need to be emulated.

Another example of such a condition is guest execution in protected mode with paging disabled. A VMM could support such guest execution by using “identity” page tables to emulate unpaged protected mode.

31.2.1 Using Unrestricted Guest Mode

Processors which support the “unrestricted guest” VM-execution control allow VM software to run in real-address mode and unpaged protected mode. Since these modes do not use paging, VMM software must virtualize guest memory using EPT.

Special notes for 64-bit VMM software using the 1-setting of the “unrestricted guest” VM-execution control:

- It is recommended that 64-bit VMM software use the 1-settings of the "load IA32_EFER" VM entry control and the "save IA32_EFER" VM-exit control. If VM entry is establishing CR0.PG=0 and if the "IA-32e mode guest" and "load IA32_EFER" VM entry controls are both 0, VM entry leaves IA32_EFER.LME unmodified (i.e., the host value will persist in the guest).
- It is not necessary for VMM software to track guest transitions into and out of IA-32e mode for the purpose of maintaining the correct setting of the "IA-32e mode guest" VM entry control. This is because VM exits on

---

1. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.).
processors supporting the 1-setting of the "unrestricted guest" VM-execution control save the (guest) value of IA32_EFER.LMA into the "IA-32e mode guest" VM entry control.

### 31.3 MANAGING VMCS REGIONS AND POINTERS

A VMM must observe necessary procedures when working with a VMCS, the associated VMCS pointer, and the VMCS region. It must also not assume the state of persistency for VMCS regions in memory or cache.

Before entering VMX operation, the host VMM allocates a VMXON region. A VMM can host several virtual machines and have many VMCSs active under its management. A unique VMCS region is required for each virtual machine; a VMXON region is required for the VMM itself.

A VMM determines the VMCS region size by reading IA32_VMX_BASIC MSR; it creates VMCS regions of this size using a 4-KByte-aligned area of physical memory. Each VMCS region needs to be initialized with a VMCS revision identifier (at byte offset 0) identical to the revision reported by the processor in the VMX capability MSR.

**NOTE**

Software must not read or write directly to the VMCS data region as the format is not architecturally defined. Consequently, Intel recommends that the VMM remove any linear-address mappings to VMCS regions before loading.

System software does not need to do special preparation to the VMXON region before entering into VMX operation. The address of the VMXON region for the VMM is provided as an operand to VMXON instruction. Once in VMX root operation, the VMM needs to prepare data fields in the VMCS that control the execution of a VM upon a VM entry. The VMM can make a VMCS the current VMCS by using the VMPTRLD instruction. VMCS data fields must be read or written only through VMREAD and VMWRITE commands respectively.

Every component of the VMCS is identified by a 32-bit encoding that is provided as an operand to VMREAD and VMWRITE. Appendix B provides the encodings. A VMM must properly initialize all fields in a VMCS before using the current VMCS for VM entry.

A VMCS is referred to as a controlling VMCS if it is the current VMCS on a logical processor in VMX non-root operation. A current VMCS for controlling a logical processor in VMX non-root operation may be referred to as a working VMCS if the logical processor is not in VMX non-root operation. The relationship of active, current (i.e. working) and controlling VMCS during VMX operation is shown in Figure 31-1.

**NOTE**

As noted in Section 24.1, the processor may optimize VMX operation by maintaining the state of an active VMCS (one for which VMPTRLD has been executed) on the processor. Before relinquishing control to other system software that may, without informing the VMM, remove power from the processor (e.g., for transitions to S3 or S4) or leave VMX operation, a VMM must VMCLEAR all active VMCSs. This ensures that all VMCS data cached by the processor are flushed to memory and that no other software can corrupt the current VMM's VMCS data. It is also recommended that the VMM execute VMXOFF after such executions of VMCLEAR.

The VMX capability MSR IA32_VMX_BASIC reports the memory type used by the processor for accessing a VMCS or any data structures referenced through pointers in the VMCS. Software must maintain the VMCS structures in cache-coherent memory. Software must always map the regions hosting the I/O bitmaps, MSR bitmaps, VM-exit MSR-store area, VM-exit MSR-load area, and VM-entry MSR-load area to the write-back (WB) memory type. Mapping these regions to uncachable (UC) memory type is supported, but strongly discouraged due to negative impact on performance.

### 31.4 USING VMX INSTRUCTIONS

VMX instructions are allowed only in VMX root operation. An attempt to execute a VMX instruction in VMX non-root operation causes a VM exit.
Processors perform various checks while executing any VMX instruction. They follow well-defined error handling on failures. VMX instruction execution failures detected before loading of a guest state are handled by the processor as follows:

- If the working-VMCS pointer is not valid, the instruction fails by setting RFLAGS.CF to 1.
- If the working-VMCS pointer is valid, RFLAGS.ZF is set to 1 and the proper error-code is saved in the VM-instruction error field of the working-VMCS.

Software is required to check RFLAGS.CF and RFLAGS.ZF to determine the success or failure of VMX instruction executions.

The following items provide details regarding use of the VM-entry instructions (VMLAUNCH and VMRESUME):

- If the working-VMCS pointer is valid, the state of the working VMCS may cause the VM-entry instruction to fail. RFLAGS.ZF is set to 1 and one of the following values is saved in the VM-instruction error field:
  - 4: VMLAUNCH with non-clear VMCS.
    If this error occurs, software can avoid the error by executing VMRESUME.
  - 5: VMRESUME with non-launched VMCS.
    If this error occurs, software can avoid the error by executing VMLAUNCH.

---

**Figure 31-1. VMX Transitions and States of VMCS in a Logical Processor**

<table>
<thead>
<tr>
<th>Processor Operation</th>
<th>VMXON</th>
<th>VM Entry</th>
<th>VM Exit</th>
<th>VMXOFF</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM Entry</td>
<td></td>
<td>VM Entry</td>
<td>VM Exit</td>
<td>VM Exit</td>
</tr>
<tr>
<td>VM Exit</td>
<td>VM Entry</td>
<td>VM Exit</td>
<td>VM Exit</td>
<td></td>
</tr>
</tbody>
</table>

**Legend:**
- Outside VMX Operation
- VMX Root Operation
- VMX Non-Root Operation

**VMCS States:**
- VMCS B
- VMCS A
- VMPTRLD A
- VMPTRLD B
- VMRESUME
- VMCLEAR A
- VMCLEAR B
- VMLAUNCH

**VMX Transitions:**
- VMXON
- VMXOFF
- VM Entry
- VM Exit

**Legend:**
- Inactive VMCS
- Current VMCS (working)
- Active VMCS (not current)
- Current VMCS (controlling)
— 6: VMRESUME after VMXOFF.\(^1\)

If this error occurs, software can avoid the error by executing the following sequence of instructions:

- VMPTRST (working-VMCS pointer)
- VMCLEAR (working-VMCS pointer)
- VMPTRLD (working-VMCS pointer)
- VMLAUNCH

(VMPTRST may not be necessary if software already knows the working-VMCS pointer.)

- If none of the above errors occur, the processor checks on the VMX controls and host-state area. If any of these checks fail, the VM-entry instruction fails. RFLAGS.ZF is set to 1 and either 7 (VM entry with invalid control field(s)) or 8 (VM entry with invalid host-state field(s)) is saved in the VM-instruction error field.

- After a VM-entry instruction (VMRESUME or VMLAUNCH) successfully completes the general checks and checks on VMX controls and the host-state area (see Section 26.2), any errors encountered while loading of guest-state (due to bad guest-state or bad MSR loading) causes the processor to load state from the host-state area of the working VMCS as if a VM exit had occurred (see Section 31.7).

This failure behavior differs from that of VM exits in that no guest-state is saved to the guest-state area. A VMM can detect its VM-exit handler was invoked by such a failure by checking bit 31 (for 1) in the exit reason field of the working VMCS and further identify the failure by using the exit qualification field.

See Chapter 26 for more details about the VM-entry instructions.

### 31.5 VMM SETUP & TEAR DOWN

VMMs need to ensure that the processor is running in protected mode with paging before entering VMX operation. The following list describes the minimal steps required to enter VMX root operation with a VMM running at CPL = 0.

- Check VMX support in processor using CPUID.
- Determine the VMX capabilities supported by the processor through the VMX capability MSRs. See Section 31.5.1 and Appendix A.
- Create a VMXON region in non-pageable memory of a size specified by IA32_VMX_BASIC MSR and aligned to a 4-KByte boundary. Software should read the capability MSRs to determine width of the physical addresses that may be used for the VMXON region and ensure the entire VMXON region can be addressed by addresses with that width. Also, software must ensure that the VMXON region is hosted in cache-coherent memory.
- Initialize the version identifier in the VMXON region (the first 31 bits) with the VMCS revision identifier reported by capability MSRs. Clear bit 31 of the first 4 bytes of the VMXON region.
- Ensure the current processor operating mode meets the required CR0 fixed bits (CR0.PE = 1, CR0.PG = 1). Other required CR0 fixed bits can be detected through the IA32_VMX_CR0FIXED0 and IA32_VMX_CR0FIXED1 MSRs.
- Enable VMX operation by setting CR4.VMXE = 1. Ensure the resultant CR4 value supports all the CR4 fixed bits reported in the IA32_VMX_CR4FIXED0 and IA32_VMX_CR4FIXED1 MSRs.
- Ensure that the IA32_FEATURE_CONTROL MSR (MSR index 3AH) has been properly programmed and that its lock bit is set (Bit 0 = 1). This MSR is generally configured by the BIOS using WRMSR.
- Execute VMXON with the physical address of the VMXON region as the operand. Check successful execution of VMXON by checking if RFLAGS.CF = 0.

Upon successful execution of the steps above, the processor is in VMX root operation.

A VMM executing in VMX root operation and CPL = 0 leaves VMX operation by executing VMXOFF and verifies successful execution by checking if RFLAGS.CF = 0 and RFLAGS.ZF = 0.

If an SMM monitor has been configured to service SMIs while in VMX operation (see Section 34.15), the SMM monitor needs to be torn down before the executive monitor can leave VMX operation (see Section 34.15.7). VMXOFF fails for the executive monitor (a VMM that entered VMX operation by way of issuing VMXON) if SMM monitor is configured.

---

1. Earlier versions of this manual described this error as “VMRESUME with a corrupted VMCS”.

---
31.5.1 Algorithms for Determining VMX Capabilities

As noted earlier, a VMM should determine the VMX capabilities supported by the processor by reading the VMX capability MSRs. The architecture for these MSRs is detailed in Appendix A.

As noted in Chapter 26, “VM Entries”, certain VMX controls are reserved and must be set to a specific value (0 or 1) determined by the processor. The specific value to which a reserved control must be set is its default setting. Most controls have a default setting of 0; Appendix A.2 identifies those controls that have a default setting of 1. The term default describes the class of controls whose default setting is 1. There are no secondary processor-based VM-execution controls in the default1 class.

Future processors may define new functionality for one or more reserved controls. Such processors would allow each newly defined control to be set either to 0 or to 1. Software that does not desire a control’s new functionality should set the control to its default setting.

The capability MSRs IA32_VMX_PINBASED_CTLS, IA32_VMX_PROCBASED_CTLS, IA32_VMX_EXIT_CTLS, and IA32_VMX_ENTRY_CTLS report, respectively, on the allowed settings of most of the pin-based VM-execution controls, the primary processor-based VM-execution controls, the VM-exit controls, and the VM-entry controls. However, they will always report that any control in the default1 class must be 1. If a logical processor allows any control in the default1 class to be 0, it indicates this fact by returning 1 for the value of bit 55 of the IA32_VMX_BASIC MSR. If this bit is 1, the logical processor supports the capability MSRs IA32_VMX_TRUE_PINBASED_CTLS, IA32_VMX_TRUE_PROCBASED_CTLS, IA32_VMX_TRUE_EXIT_CTLS, and IA32_VMX_TRUE_ENTRY_CTLS. These capability MSRs report, respectively, on the allowed settings of all of the pin-based VM-execution controls, the primary processor-based VM-execution controls, the VM-exit controls, and the VM-entry controls.

Software may use one of the following high-level algorithms to determine the correct default control settings: 1

1. The following algorithm does not use the details given in Appendix A.2:
   a. Ignore bit 55 of the IA32_VMX_BASIC MSR.
   b. Using RDMSR, read the VMX capability MSRs IA32_VMX_PINBASED_CTLS, IA32_VMX_PROCBASED_CTLS, IA32_VMX_EXIT_CTLS, and IA32_VMX_ENTRY_CTLS.
   c. Set the VMX controls as follows:
      i) If the relevant VMX capability MSR reports that a control has a single setting, use that setting.
      ii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; and (2) the control’s meaning is known to the VMM; then set the control based on functionality desired.
      iii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; and (2) the control’s meaning is not known to the VMM; then set the control to 0.

   A VMM using this algorithm will set to 1 all controls in the default1 class (in step (c)(ii)). It will operate correctly even on processors that allow some controls in the default1 class to be 0. However, such a VMM will not be able to use the new features enabled by the 0-setting of such controls. For that reason, this algorithm is not recommended.

2. The following algorithm uses the details given in Appendix A.2. This algorithm requires software to know the identity of the controls in the default1 class:
   a. Using RDMSR, read the IA32_VMX_BASIC MSR.
   b. Use bit 55 of that MSR as follows:
      i) If bit 55 is 0, use RDMSR to read the VMX capability MSRs IA32_VMX_PINBASED_CTLS, IA32_VMX_PROCBASED_CTLS, IA32_VMX_EXIT_CTLS, and IA32_VMX_ENTRY_CTLS.
      ii) If bit 55 is 1, use RDMSR to read the VMX capability MSRs IA32_VMX_TRUE_PINBASED_CTLS, IA32_VMX_TRUE_PROCBASED_CTLS, IA32_VMX_TRUE_EXIT_CTLS, and IA32_VMX_TRUE_ENTRY_CTLS.

1. These algorithms apply only to the pin-based VM-execution controls, the primary processor-based VM-execution controls, the VM-exit controls, and the VM-entry controls. Because there are no secondary processor-based VM-execution controls in the default1 class, a VMM can always set to 0 any such control whose meaning is unknown to it.
c. Set the VMX controls as follows:
   i) If the relevant VMX capability MSR reports that a control has a single setting, use that setting.
   ii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; and (2) the control’s meaning is known to the VMM; then set the control based on functionality desired.
   iii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; (2) the control’s meaning is not known to the VMM; and (3) the control is not in the default 1 class; then set the control to 0.
   iv) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; (2) the control’s meaning is not known to the VMM; and (3) the control is in the default 1 class; then set the control to 1.

A VMM using this algorithm will set to 1 all controls in default 1 class whose meaning it does not know (either in step (c)(i) or step (c)(iv)). It will operate correctly even on processors that allow some controls in the default 1 class to be 0. Unlike a VMM using Algorithm 1, a VMM using Algorithm 2 will be able to use the new features enabled by the 0-setting of such controls.

3. The following algorithm uses the details given in Appendix A.2. This algorithm does not require software to know the identity of the controls in the default 1 class:
   a. Using RDMSR, read the VMX capability MSRs IA32_VMX_BASIC, IA32_VMX_PINBASED_CTLS, IA32_VMX_PROCBASED_CTLS, IA32_VMX_EXIT_CTLS, and IA32_VMX_ENTRY_CTLS.
   b. If bit 55 of the IA32_VMX_BASIC MSR is 0, set the VMX controls as follows:
      i) If the relevant VMX capability MSR reports that a control has a single setting, use that setting.
      ii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; and (2) the control’s meaning is known to the VMM; then set the control based on functionality desired.
      iii) If (1) the relevant VMX capability MSR reports that a control can be set to 0 or 1; and (2) the control’s meaning is not known to the VMM; then set the control to 0.
   c. If bit 55 of the IA32_VMX_BASIC MSR is 1, use RDMSR to read the VMX capability MSRs IA32_VMX_TRUE_PINBASED_CTLS, IA32_VMX_TRUE_PROCBASED_CTLS, IA32_VMX_TRUE_EXIT_CTLS, and IA32_VMX_TRUE_ENTRY_CTLS. Set the VMX controls as follows:
      i) If the relevant VMX capability MSR just read reports that a control has a single setting, use that setting.
      ii) If (1) the relevant VMX capability MSR just read reports that a control can be set to 0 or 1; and (2) the control’s meaning is known to the VMM; then set the control based on functionality desired.
      iii) If (1) the relevant VMX capability MSR just read reports that a control can be set to 0 or 1; (2) the control’s meaning is not known to the VMM; and (3) the relevant VMX capability MSR as read in step (a) reports that a control can be set to 0; then set the control to 0.
      iv) If (1) the relevant VMX capability MSR just read reports that a control can be set to 0 or 1; (2) the control’s meaning is not known to the VMM; and (3) the relevant VMX capability MSR as read in step (a) reports that a control must be 1; then set the control to 1.

A VMM using this algorithm will set to 1 all controls in the default 1 class whose meaning it does not know (in step (b)(i), step (c)(i), or step (c)(iv)). It will operate correctly even on processors that allow some controls in the default 1 class to be 0. Unlike a VMM using Algorithm 1, a VMM using Algorithm 2 will be able to use the new features enabled by the 0-setting of such controls. Unlike a VMM using Algorithm 2, a VMM using Algorithm 3 need not know the identities of the controls in the default 1 class.

31.6 PREPARATION AND LAUNCHING A VIRTUAL MACHINE

The following list describes the minimal steps required by the VMM to set up and launch a guest VM.

- Create a VMCS region in non-pageable memory of size specified by the VMX capability MSR IA32_VMX_BASIC and aligned to 4-KBytes. Software should read the capability MSRs to determine width of the physical addresses that may be used for a VMCS region and ensure the entire VMCS region can be addressed by
addresses with that width. The term “guest-VMCS address” refers to the physical address of the new VMCS region for the following steps.

- Initialize the version identifier in the VMCS (first 31 bits) with the VMCS revision identifier reported by the VMX capability MSR IA32_VMX_BASIC. Clear bit 31 of the first 4 bytes of the VMCS region.

- Execute the VMCLEAR instruction by supplying the guest-VMCS address. This will initialize the new VMCS region in memory and set the launch state of the VMCS to “clear”. This action also invalidates the working-VMCS pointer register to FFFFFFFF_FFFFFFFH. Software should verify successful execution of VMCLEAR by checking if RFLAGS.CF = 0 and RFLAGS.ZF = 0.

- Execute the VMPTRLD instruction by supplying the guest-VMCS address. This initializes the working-VMCS pointer with the new VMCS region’s physical address.

- Issue a sequence of VMWRITEs to initialize various host-state area fields in the working VMCS. The initialization sets up the context and entry-points to the VMM upon subsequent VM exits from the guest. Host-state fields include control registers (CR0, CR3 and CR4), selector fields for the segment registers (CS, SS, DS, ES, FS, GS and TR), and base-address fields (for FS, GS, TR, GDTR and IDTR; RSP, RIP and the MSRs that control fast system calls).

Chapter 27 describes the host-state consistency checking done by the processor for VM entries. The VMM is required to set up host-state that comply with these consistency checks. For example, VMX requires the host-area to have a task register (TR) selector with TI and RPL fields set to 0 and pointing to a valid TSS.

- Use VMWRITEs to set up the various VM-exit control fields, VM-entry control fields, and VM-execution control fields in the VMCS. Care should be taken to make sure the settings of individual fields match the allowed 0 and 1 settings for the respective controls as reported by the VMX capability MSRs (see Appendix A). Any settings inconsistent with the settings reported by the capability MSRs will cause VM entries to fail.

- Use VMWRITE to initialize various guest-state area fields in the working VMCS. This sets up the context and entry-point for guest execution upon VM entry. Chapter 27 describes the guest-state loading and checking done by the processor for VM entries to protected and virtual-8086 guest execution.

- The VMM is required to set up guest-state that complies with these consistency checks:
  - If the VMM design requires the initial VM launch to cause guest software (typically the guest virtual BIOS) execution from the guest’s reset vector, it may need to initialize the guest execution state to reflect the state of a physical processor at power-on reset (described in Chapter 9, Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A).
  - The VMM may need to initialize additional guest execution state that is not captured in the VMCS guest-state area by loading them directly on the respective processor registers. Examples include general purpose registers, the CR2 control register, debug registers, floating point registers and so forth. VMM may support lazy loading of FPU, MMX, SSE, and SSE2 states with CR0.TS = 1 (described in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A).

- Execute VMLAUNCH to launch the guest VM. If VMLAUNCH fails due to any consistency checks before guest-state loading, RFLAGS.CF or RFLAGS.ZF will be set and the VM-instruction error field (see Section 24.9.5) will contain the error-code. If guest-state consistency checks fail upon guest-state loading, the processor loads state from the host-state area as if a VM exit had occurred (see Section 31.6).

VMLAUNCH updates the controlling-VMCS pointer with the working-VMCS pointer and saves the old value of controlling-VMCS as the parent pointer. In addition, the launch state of the guest VMCS is changed to “launched” from “clear”. Any programmed exit conditions will cause the guest to VM exit to the VMM. The VMM should execute VMRESUME instruction for subsequent VM entries to guests in a “launched” state.

### 31.7 HANDLING OF VM EXITS

This section provides examples of software steps involved in a VMM’s handling of VM-exit conditions:

- Determine the exit reason through a VMREAD of the exit-reason field in the working-VMCS. Appendix C describes exit reasons and their encodings.

- VMREAD the exit-qualification from the VMCS if the exit-reason field provides a valid qualification. The exit-qualification field provides additional details on the VM-exit condition. For example, in case of page faults, the exit-qualification field provides the guest linear address that caused the page fault.
Depending on the exit reason, fetch other relevant fields from the VMCS. Appendix C lists the various exit reasons.

Handle the VM-exit condition appropriately in the VMM. This may involve the VMM emulating one or more guest instructions, programming the underlying host hardware resources, and then re-entering the VM to continue execution.

31.7.1 Handling VM Exits Due to Exceptions

As noted in Section 25.2, an exception causes a VM exit if the bit corresponding to the exception’s vector is set in the exception bitmap. (For page faults, the error code also determines whether a VM exit occurs.) This section provide some guidelines of how a VMM might handle such exceptions.

Exceptions result when a logical processor encounters an unusual condition that software may not have expected. When guest software encounters an exception, it may be the case that the condition was caused by the guest software. For example, a guest application may attempt to access a page that is restricted to supervisor access. Alternatively, the condition causing the exception may have been established by the VMM. For example, a guest OS may attempt to access a page that the VMM has chosen to make not present.

When the condition causing an exception was established by guest software, the VMM may choose to reflect the exception to guest software. When the condition was established by the VMM itself, the VMM may choose to resume guest software after removing the condition.

31.7.1.1 Reflecting Exceptions to Guest Software

If the VMM determines that a VM exit was caused by an exception due to a condition established by guest software, it may reflect that exception to guest software. The VMM would cause the exception to be delivered to guest software, where it can be handled as it would be if the guest were running on a physical machine. This section describes how that may be done.

In general, the VMM can deliver the exception to guest software using VM-entry event injection as described in Section 26.5. The VMM can copy (using VMREAD and VMWRITE) the contents of the VM-exit interruption-information field (which is valid, since the VM exit was caused by an exception) to the VM-entry interruption-information field (which, if valid, will cause the exception to be delivered as part of the next VM entry). The VMM would also copy the contents of the VM-exit interruption error-code field to the VM-entry exception error-code field; this need not be done if bit 11 (error code valid) is clear in the VM-exit interruption-information field. After this, the VMM can execute VMRESUME.

The following items provide details that may qualify the general approach:

- Care should be taken to ensure that reserved bits 30:12 in the VM-entry interruption-information field are 0. In particular, some VM exits may set bit 12 in the VM-exit interruption-information field to indicate NMI unblocking due to IRET. If this bit is copied as 1 into the VM-entry interruption-information field, the next VM entry will fail because that bit should be 0.

- Bit 31 (valid) of the IDT-vectoring information field indicates, if set, that the exception causing the VM exit occurred while another event was being delivered to guest software. If this is the case, it may not be appropriate simply to reflect that exception to guest software. To provide proper virtualization of the exception architecture, a VMM should handle nested events as a physical processor would. Processor handling is described in Chapter 6, "Interrupt 8—Double Fault Exception (#DF)" in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A.

  - The VMM should reflect the exception causing the VM exit to guest software in any of the following cases:
    - The value of bits 10:8 (interruption type) of the IDT-vectoring information field is anything other than 3 (hardware exception).
    - The value of bits 7:0 (vector) of the IDT-vectoring information field indicates a benign exception (1, 2, 3, 4, 5, 6, 7, 9, 16, 17, 18, or 19).
    - The value of bits 7:0 (vector) of the VM-exit interruption-information field indicates a benign exception.
• The value of bits 7:0 of the IDT-vectoring information field indicates a contributory exception (0, 10, 11, 12, or 13) and the value of bits 7:0 of the VM-exit interruption-information field indicates a page fault (14).

  — If the value of bits 10:8 of the IDT-vectoring information field is 3 (hardware exception), the VMM should reflect a double-fault exception to guest software in any of the following cases:
    • The value of bits 7:0 of the IDT-vectoring information field and the value of bits 7:0 of the VM-exit interruption-information field each indicates a contributory exception.
    • The value of bits 7:0 of the IDT-vectoring information field indicates a page fault and the value of bits 7:0 of the VM-exit interruption-information field indicates either a contributory exception or a page fault.

  A VMM can reflect a double-fault exception to guest software by setting the VM-entry interruption-information and VM-entry exception error-code fields as follows:
  • Set bits 7:0 (vector) of the VM-entry interruption-information field to 8 (#DF).
  • Set bits 10:8 (interruption type) of the VM-entry interruption-information field to 3 (hardware exception).
  • Set bit 11 (deliver error code) of the VM-entry interruption-information field to 1.
  • Clear bits 30:12 (reserved) of VM-entry interruption-information field.
  • Set bit 31 (valid) of VM-entry interruption-information field.
  • Set the VM-entry exception error-code field to zero.

  — If the value of bits 10:8 of the IDT-vectoring information field is 3 (hardware exception) and the value of bits 7:0 is 8 (#DF), guest software would have encountered a triple fault. Event injection should not be used in this case. The VMM may choose to terminate the guest, or it might choose to enter the guest in the shutdown activity state.

31.7.1.2 Resuming Guest Software after Handling an Exception

If the VMM determines that a VM exit was caused by an exception due to a condition established by the VMM itself, it may choose to resume guest software after removing the condition. The approach for removing the condition may be specific to the VMM's software architecture and algorithms. This section describes how guest software may be resumed after removing the condition.

In general, the VMM can resume guest software simply by executing VMRESUME. The following items provide details of cases that may require special handling:

• If the "NMI exiting" VM-execution control is 0, bit 12 of the VM-exit interruption-information field indicates that the VM exit was due to a fault encountered during an execution of the IRET instruction that unblocked non-maskable interrupts (NMIs). In particular, it provides this indication if the following are both true:
  — Bit 31 (valid) in the IDT-vectoring information field is 0.
  — The value of bits 7:0 (vector) of the VM-exit interruption-information field is not 8 (the VM exit is not due to a double-fault exception).

  If both are true and bit 12 of the VM-exit interruption-information field is 1, NMIs were blocked before guest software executed the IRET instruction that caused the fault that caused the VM exit. The VMM should set bit 3 (blocking by NMI) in the interruptibility-state field (using VMREAD and VMWRITE) before resuming guest software.

• If the "virtual NMIs" VM-execution control is 1, bit 12 of the VM-exit interruption-information field indicates that the VM exit was due to a fault encountered during an execution of the IRET instruction that removed virtual-NMI blocking. In particular, it provides this indication if the following are both true:
  — Bit 31 (valid) in the IDT-vectoring information field is 0.
  — The value of bits 7:0 (vector) of the VM-exit interruption-information field is not 8 (the VM exit is not due to a double-fault exception).

  If both are true and bit 12 of the VM-exit interruption-information field is 1, there was virtual-NMI blocking before guest software executed the IRET instruction that caused the fault that caused the VM exit. The VMM
should set bit 3 (blocking by NMI) in the interruptibility-state field (using VMREAD and VMWRITE) before resuming guest software.

- Bit 31 (valid) of the IDT-vectoring information field indicates, if set, that the exception causing the VM exit occurred while another event was being delivered to guest software. The VMM should ensure that the other event is delivered when guest software is resumed. It can do so using the VM-entry event injection described in Section 26.5 and detailed in the following paragraphs:
  - The VMM can copy (using VMREAD and VMWRITE) the contents of the IDT-vectoring information field (which is presumed valid) to the VM-entry interruption-information field (which, if valid, will cause the exception to be delivered as part of the next VM entry).
  - The VMM should ensure that reserved bits 30:12 in the VM-entry interruption-information field are 0. In particular, the value of bit 12 in the IDT-vectoring information field is undefined after all VM exits. If this bit is copied as 1 into the VM-entry interruption-information field, the next VM entry will fail because the bit should be 0.
  - If the “virtual NMIs” VM-execution control is 1 and the value of bits 10:8 (interruption type) in the IDT-vectoring information field is 2 (indicating NMI), the VM exit occurred during delivery of an NMI that had been injected as part of the previous VM entry. In this case, bit 3 (blocking by NMI) will be 1 in the interruptibility-state field in the VMCS. The VMM should clear this bit; otherwise, the next VM entry will fail (see Section 26.3.1.5).
  - The VMM can also copy the contents of the IDT-vectoring error-code field to the VM-entry exception error-code field. This need not be done if bit 11 (error code valid) is clear in the IDT-vectoring information field.
  - The VMM can also copy the contents of the VM-exit instruction-length field to the VM-entry instruction-length field. This need be done only if bits 10:8 (interruption type) in the IDT-vectoring information field indicate either software interrupt, privileged software exception, or software exception.

### 31.8 MULTI-PROCESSOR CONSIDERATIONS

The most common VMM design will be the symmetric VMM. This type of VMM runs the same VMM binary on all logical processors. Like a symmetric operating system, the symmetric VMM is written to ensure all critical data is updated by only one processor at a time, IO devices are accessed sequentially, and so forth. Asymmetric VMM designs are possible. For example, an asymmetric VMM may run its scheduler on one processor and run just enough of the VMM on other processors to allow the correct execution of guest VMs. The remainder of this section focuses on the multi-processor considerations for a symmetric VMM.

A symmetric VMM design does not preclude asymmetry in its operations. For example, a symmetric VMM can support asymmetric allocation of logical processor resources to guests. Multiple logical processors can be brought into a single guest environment to support an MP-aware guest OS. Because an active VMCS can not control more than one logical processor simultaneously, a symmetric VMM must make copies of its VMCS to control the VM allocated to support an MP-aware guest OS. Care must be taken when accessing data structures shared between these VMCSs. See Section 31.8.4.

Although it may be easier to develop a VMM that assumes a fully-symmetric view of hardware capabilities (with all processors supporting the same processor feature sets, including the same revision of VMX), there are advantages in developing a VMM that comprehends different levels of VMX capability (reported by VMX capability MSRs). One possible advantage of such an approach could be that an existing software installation (VMM and guest software stack) could continue to run without requiring software upgrades to the VMM, when the software installation is upgraded to run on hardware with enhancements in the processor’s VMX capabilities. Another advantage could be that a single software installation image, consisting of a VMM and guests, could be deployed to multiple hardware platforms with varying VMX capabilities. In such cases, the VMM could fall back to a common subset of VMX features supported by all VMX revisions, or choose to understand the asymmetry of the VMX capabilities and assign VMs accordingly.

This section outlines some of the considerations to keep in mind when developing an MP-aware VMM.
31.8.1 Initialization

Before enabling VMX, an MP-aware VMM must check to make sure that all processors in the system are compatible and support features required. This can be done by:

- Checking the CPUID on each logical processor to ensure VMX is supported and that the overall feature set of each logical processor is compatible.
- Checking VMCS revision identifiers on each logical processor.
- Checking each of the “allowed-1” or “allowed-0” fields of the VMX capability MSR’s on each processor.

31.8.2 Moving a VMCS Between Processors

An MP-aware VMM is free to assign any logical processor to a VM. But for performance considerations, moving a guest VMCS to another logical processor is slower than resuming that guest VMCS on the same logical processor. Certain VMX performance features (such as caching of portions of the VMCS in the processor) are optimized for a guest VMCS that runs on the same logical processor.

The reasons are:

- To restart a guest on the same logical processor, a VMM can use VMRESUME. VMRESUME is expected to be faster than VMLAUNCH in general.
- To migrate a VMCS to another logical processor, a VMM must use the sequence of VMCLEAR, VMPTRLD and VMLAUNCH.
- Operations involving VMCLEAR can impact performance negatively. See Section 24.11.3.

A VMM scheduler should make an effort to schedule a guest VMCS to run on the logical processor where it last ran. Such a scheduler might also benefit from doing lazy VMCLEARS (that is: performing a VMCLEAR on a VMCS only when the scheduler knows the VMCS is being moved to a new logical processor). The remainder of this section describes the steps a VMM must take to move a VMCS from one processor to another.

A VMM must check the VMCS revision identifier in the VMX capability MSR IA32_VMX_BASIC to determine if the VMCS regions are identical between all logical processors. If the VMCS regions are identical (same revision ID) the following sequence can be used to move or copy the VMCS from one logical processor to another:

- Perform a VMCLEAR operation on the source logical processor. This ensures that all VMCS data that may be cached by the processor are flushed to memory.
- Copy the VMCS region from one memory location to another location. This is an optional step assuming the VMM wishes to relocate the VMCS or move the VMCS to another system.
- Perform a VMPTRLD of the physical address of VMCS region on the destination processor to establish its current VMCS pointer.

If the revision identifiers are different, each field must be copied to an intermediate structure using individual reads (VMREAD) from the source fields and writes (VMWRITE) to destination fields. Care must be taken on fields that are hard-wired to certain values on some processor implementations.

31.8.3 Paired Index-Data Registers

A VMM may need to virtualize hardware that is visible to software using paired index-data registers. Paired index-data register interfaces, such as those used in PCI (CF8, CFC), require special treatment in cases where a VM performing writes to these pairs can be moved during execution. In this case, the index (e.g. CF8) should be part of the virtualized state. If the VM is moved during execution, writes to the index should be redone so subsequent data reads/writes go to the right location.

31.8.4 External Data Structures

Certain fields in the VMCS point to external data structures (for example: the MSR bitmap, the I/O bitmaps). If a logical processor is in VMX non-root operation, none of the external structures referenced by that logical
processor’s current VMCS should be modified by any logical processor or DMA. Before updating one of these structures, the VMM must ensure that no logical processor whose current VMCS references the structure is in VMX non-root operation.

If a VMM uses multiple VMCS with each VMCS using separate external structures, and these structures must be kept synchronized, the VMM must apply the same care to updating these structures.

### 31.8.5 CPUID Emulation

CPUID reports information that is used by OS and applications to detect hardware features. It also provides multi-threading/multi-core configuration information. For example, MP-aware OSs rely on data reported by CPUID to discover the topology of logical processors in a platform (see Section 8.9, “Programming Considerations for Hardware Multi-Threading Capable Processors,” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A*).

If a VMM is to support asymmetric allocation of logical processor resources to guest OSs that are MP aware, then the VMM must emulate CPUID for its guests. The emulation of CPUID by the VMM must ensure the guest’s view of CPUID leaves are consistent with the logical processor allocation committed by the VMM to each guest OS.

### 31.9 32-BIT AND 64-BIT GUEST ENVIRONMENTS

For the most part, extensions provided by VMX to support virtualization are orthogonal to the extensions provided by Intel 64 architecture. There are considerations that impact VMM designs. These are described in the following subsections.

#### 31.9.1 Operating Modes of Guest Environments

For Intel 64 processors, VMX operation supports host and guest environments that run in IA-32e mode or without IA-32e mode. VMX operation also supports host and guest environments on IA-32 processors.

A VMM entering VMX operation while IA-32e mode is active is considered to be an IA-32e mode host. A VMM entering VMX operation while IA-32e mode is not activated or not available is referred to as a 32-bit VMM. The type of guest operations such VMMs support are summarized in Table 31-1.

<table>
<thead>
<tr>
<th>Capability</th>
<th>Guest Operation in IA-32e mode</th>
<th>Guest Operation Not Requiring IA-32e Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA-32e mode VMM</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>32-bit VMM</td>
<td>Not supported</td>
<td>Yes</td>
</tr>
</tbody>
</table>

A VM exit may occur to an IA-32e mode guest in either 64-bit sub-mode or compatibility sub-mode of IA-32e mode. VMMS may resume guests in either mode. The sub-mode in which an IA-32e mode guest resumes VMX non-root operation is determined by the attributes of the code segment which experienced the VM exit. If CS.L = 1, the guest is executing in 64-bit mode; if CS.L = 0, the guest is executing in compatibility mode (see Section 31.9.5).

Not all of an IA-32e mode VMM must run in 64-bit mode. While some parts of an IA-32e mode VMM must run in 64-bit mode, there are only a few restrictions preventing a VMM from executing in compatibility mode. The most notable restriction is that most VMX instructions cause exceptions when executed in compatibility mode.

#### 31.9.2 Handling Widths of VMCS Fields

Individual VMCS control fields must be accessed using VMREAD or VMWRITE instructions. Outside of 64-Bit mode, VMREAD and VMWRITE operate on 32 bits of data. The widths of VMCS control fields may vary depending on whether a processor supports Intel 64 architecture.
Many VMCS fields are architected to extend transparently on processors supporting Intel 64 architecture (64 bits on processors that support Intel 64 architecture, 32 bits on processors that do not). Some VMCS fields are 64-bits wide regardless of whether the processor supports Intel 64 architecture or is in IA-32e mode.

### 31.9.2.1 Natural-Width VMCS Fields

Many VMCS fields operate using natural width. Such fields return (on reads) and set (on writes) 32-bits when operating in 32-bit mode and 64-bits when operating in 64-bit mode. For the most part, these fields return the naturally expected data widths. The “Guest RIP” field in the VMCS guest-state area is an example of this type of field.

### 31.9.2.2 64-Bit VMCS Fields

Unlike natural width fields, these fields are fixed to 64-bit width on all processors. When in 64-bit mode, reads of these fields return 64-bit wide data and writes to these fields write 64-bits. When outside of 64-bit mode, reads of these fields return the low 32-bits and writes to these fields write the low 32-bits and zero the upper 32-bits. Should a non-IA-32e mode host require access to the upper 32-bits of these fields, a separate VMCS encoding is used when issuing VMREAD/VMWRITE instructions.

The VMCS control field “MSR bitmap address” (which contains the physical address of a region of memory which specifies which MSR accesses should generate VM-exits) is an example of this type of field. Specifying encoding 00002004H to VMREAD returns the lower 32-bits to non-IA-32e mode hosts and returns 64-bits to 64-bit hosts. The separate encoding 00002005H returns only the upper 32-bits.

### 31.9.3 IA-32e Mode Hosts

An IA-32e mode host is required to support 64-bit guest environments. Because activating IA-32e mode currently requires that paging be disabled temporarily and VMX entry requires paging to be enabled, IA-32e mode must be enabled before entering VMX operation. For this reason, it is not possible to toggle in and out of IA-32e mode in a VMM.

Section 31.5 describes the steps required to launch a VMM. An IA-32e mode host is also required to set the “host address-space size” VMCS VM-exit control to 1. The value of this control is then loaded in the IA32_EFER.LME/LMA and CS.L bits on each VM exit. This establishes a 64-bit host environment as execution transfers to the VMM entry point. At a minimum, the entry point is required to be in a 64-bit code segment. Subsequently, the VMM can, if it chooses, switch to 32-bit compatibility mode on a code-segment basis (see Section 31.9.1). Note, however, that VMX instructions other than VMCALL and VMFUNC are not supported in compatibility mode; they generate an invalid opcode exception if used.

The following VMCS controls determine the value of IA32_EFER when a VM exit occurs: the “host address-space size” control (described above), the “load IA32_EFER” VM-exit control, the “VM-exit MSR-load count,” and the “VM-exit MSR-load address” (see Section 27.3).

If the “load IA32_EFER” VM-exit control is 1, the value of the LME and LMA bits in the IA32_EFER field in the host-state area must be the value of the “host address-space size” VM-exit control.

The loading of IA32_EFER.LME/LMA and CS.L bits established by the “host address-space size” control precede any loading of the IA32_EFER MSR due from the VM-exit MSR-load area. If IA32_EFER is specified in the VM-exit MSR-load area, the value of the LME bit in the load image of IA32_EFER should match the setting of the “host address-space size” control. Otherwise the attempt to modify the LME bit (while paging is enabled) will lead to a VMX-abort. However, IA32_EFER.LMA is always set by the processor to equal IA32_EFER.LME & CR0.PG; the value specified for LMA in the load image of the IA32_EFER MSR is ignored. For these and performance reasons, VMM writers may choose to not use the VM-exit/entry MSR-load/save areas for IA32_EFER.

On a VMM teardown, VMX operation should be exited before deactivating IA-32e mode if the latter is required.

### 31.9.4 IA-32e Mode Guests

A 32-bit guest can be launched by either IA-32e-mode hosts or non-IA-32e-mode hosts. A 64-bit guests can only be launched by a IA-32e-mode host.
In addition to the steps outlined in Section 31.6, VMM writers need to:

- Set the "IA-32e-mode guest" VM-entry control to 1 in the VMCS to assure VM-entry (VMLAUNCH or VMRESUME) will establish a 64-bit (or 32-bit compatible) guest operating environment.
- Enable paging (CR0.PG) and PAE mode (CR4.PAE) to assure VM-entry to a 64-bit guest will succeed.
- Ensure that the host to be in IA-32e mode (the IA32_EFER.LMA must be set to 1) and the setting of the VM-exit "host address-space size" control bit in the VMCS must also be set to 1.

If each of the above conditions holds true, then VM-entry will copy the value of the VM-entry "IA-32e-mode guest” control bit into the guests IA32_EFER.LME bit, which will result in subsequent activation of IA-32e mode. If any of the above conditions is false, the VM-entry will fail and load state from the host-state area of the working VMCS as if a VM exit had occurred (see Section 26.7).

The following VMCS controls determine the value of IA32_EFER on a VM entry: the "IA-32e-mode guest” VM-entry control (described above), the “load IA32_EFER” VM-entry control, the “VM-entry MSR-load count,” and the “VM-entry MSR-load address” (see Section 26.4).

If the "load IA32_EFER” VM-entry control is 1, the value of the LME and LMA bits in the IA32_EFER field in the guest-state area must be the value of the "IA-32e-mode guest” VM-entry control. Otherwise, the VM entry fails.

The loading of IA32_EFER.LME bit (described above) precedes any loading of the IA32_EFER MSR from the VM-entry MSR-load area of the VMCS. If loading of IA32_EFER is specified in the VM-entry MSR-load area, the value of the LME bit in the load image should be match the setting of the "IA-32e-mode guest” VM-entry control. Otherwise, the attempt to modify the LME bit (while paging is enabled) results in a failed VM entry. However, IA32_EFER.LMA is always set by the processor to equal IA32_EFER.LME & CR0.PG; the value specified for LMA in the load image of the IA32_EFER MSR is ignored. For these and performance reasons, VMM writers may choose to not use the VM-exit/entry MSR-load/save areas for IA32_EFER MSR.

Note that the VMM can control the processor’s architectural state when transferring control to a VM. VMM writers may choose to launch guests in protected mode and subsequently allow the guest to activate IA-32e mode or they may allow guests to toggle in and out of IA-32e mode. In this case, the VMM should require VM exit on accesses to the IA32_EFER MSR to detect changes in the operating mode and modify the VM-entry “IA-32e-mode guest” control accordingly.

A VMM should save/restore the extended (full 64-bit) contents of the guest general-purpose registers, the new general-purpose registers (R8-R15) and the SIMD registers introduced in 64-bit mode should it need to modify these upon VM exit.

### 31.9.5 32-Bit Guests

To launch or resume a 32-bit guest, VMM writers can follow the steps outlined in Section 31.6, making sure that the "IA-32e-mode guest” VM-entry control bit is set to 0. Then the "IA-32e-mode guest” control bit is copied into the guest IA32_EFER.LME bit, establishing IA32_EFER.LMA as 0.

### 31.10 HANDLING MODEL SPECIFIC REGISTERS

Model specific registers (MSR) provide a wide range of functionality. They affect processor features, control the programming interfaces, or are used in conjunction with specific instructions. As part of processor virtualization, a VMM may wish to protect some or all MSR resources from direct guest access.

VMX operation provides the following features to virtualize processor MSRs.

#### 31.10.1 Using VM-Execution Controls

Processor-based VM-execution controls provide two levels of support for handling guest access to processor MSRs using RDMSR and WRMSR:

- **MSR bitmaps**: In VMX implementations that support a 1-setting (see Appendix A) of the user-MSR-bitmaps execution control bit, MSR bitmaps can be used to provide flexibility in managing guest MSR accesses. The
MSR-bitmap-address in the guest VMCS can be programmed by VMM to point to a bitmap region which specifies VM-exit behavior when reading and writing individual MSRs.

MSR bitmaps form a 4-KByte region in physical memory and are required to be aligned to a 4-KByte boundary. The first 1-KByte region manages read control of MSRs in the range 00000000H-00001FFFH; the second 1-KByte region covers read control of MSR addresses in the range C0000000H-C0001FFFH. The bitmaps for write control of these MSRs are located in the 2-KByte region immediately following the read control bitmaps. While the MSR bitmap address is part of VMCS, the MSR bitmaps themselves are not. This implies MSR bitmaps are not accessible through VMREAD and VMWRITE instructions but rather by using ordinary memory writes. Also, they are not specially cached by the processor and may be placed in normal cache-coherent memory by the VMM.

When MSR bitmap addresses are properly programmed and the use-MSR-bitmap control (see Section 24.6.2) is set, the processor consults the associated bit in the appropriate bitmap on guest MSR accesses to the corresponding MSR and causes a VM exit if the bit in the bitmap is set. Otherwise, the access is permitted to proceed. This level of protection may be utilized by VMMs to selectively allow guest access to some MSRs while virtualizing others.

- **Default MSR protection**: If the use-MSR-bitmap control is not set, an attempt by a guest to access any MSR causes a VM exit. This also occurs for any attempt to access an MSR outside the ranges identified above (even if the use-MSR-bitmap control is set).

VM exits due to guest MSR accesses may be identified by the VMM through VM-exit reason codes. The MSR-read exit reason implies guest software attempted to read an MSR protected either by default or through MSR bitmaps. The MSR-write exit reason implies guest software attempting to write a MSR protected through the VM-execution controls. Upon VM exits caused by MSR accesses, the VMM may virtualize the guest MSR access through emulation of RDMSR/WRMSR.

### 31.10.2 Using VM-Exit Controls for MSRs

If a VMM allows its guest to access MSRs directly, the VMM may need to store guest MSR values and load host MSR values for these MSRs on VM exits. This is especially true if the VMM uses the same MSRs while in VMX root operation.

A VMM can use the VM-exit MSR-store-address and the VM-exit MSR-store-count exit control fields (see Section 24.7.2) to manage how MSRs are stored on VM exits. The VM-exit MSR-store-address field contains the physical address (16-byte aligned) of the VM-exit MSR-store area (a table of entries with 16 bytes per entry). Each table entry specifies an MSR whose value needs to be stored on VM exits. The VM-exit MSR-store-count contains the number of entries in the table.

Similarly the VM-exit MSR-load-address and VM-exit MSR-load-count fields point to the location and size of the VM-exit MSR load area. The entries in the VM-exit MSR-load area contain the host expected values of specific MSRs when a VM exit occurs.

Upon VM-exit, bits 127:64 of each entry in the VM-exit MSR-store area is updated with the contents of the MSR indexed by bits 31:0. Also, bits 127:64 of each entry in the VM-exit MSR-load area is updated by loading with values from bits 127:64 the contents of the MSR indexed by bits 31:0.

### 31.10.3 Using VM-Entry Controls for MSRs

A VMM may require specific MSRs to be loaded explicitly on VM entries while launching or resuming guest execution. The VM-entry MSR-load-address and VM-entry MSR-load-count entry control fields determine how MSRs are loaded on VM-entries. The VM-entry MSR-load-address and count fields are similar in structure and function to the VM-exit MSR-load address and count fields, except the MSR loading is done on VM-entries.

### 31.10.4 Handling Special-Case MSRs and Instructions

A number of instructions make use of designated MSRs in their operation. The VMM may need to consider saving the states of those MSRs. Instructions that merit such consideration include SYSENTER/SYSEXIT, SYSCALL/SYSRET, SWAPGS.
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31.10.4.1 Handling IA32_EFER MSR

The IA32_EFER MSR includes bit fields that allow system software to enable processor features. For example: the SCE bit enables SYSCALL/SYSRET and the NXE bit enables the execute-disable bits in the paging-structure entries. VMX provides hardware support to load the IA32_EFER MSR on VMX transitions and to save it on VM exits. Because of this, VMM software need not use the RDMSR and WRMSR instruction to give the register different values during host and guest execution.

31.10.4.2 Handling the SYSENTER and SYSEXIT Instructions

The SYSENTER and SYSEXIT instructions use three dedicated MSRs (IA32_SYSENTER_CS, IA32_SYSENTER_ESP and IA32_SYSENTER_EIP) to manage fast system calls. These MSRs may be utilized by both the VMM and the guest OS to manage system calls in VMX root operation and VMX non-root operation respectively. VM entries load these MSRs from fields in the guest-state area of the VMCS. VM exits save the values of these MSRs into those fields and loads the MSRs from fields in the host-state area.

31.10.4.3 Handling the SYSCALL and SYSRET Instructions

The SYSCALL/SYSRET instructions are similar to SYSENTER/SYSEXIT but are designed to operate within the context of a 64-bit flat code segment. They are available only in 64-bit mode and only when the SCE bit of the IA32_EFER MSR is set. SYSCALL/SYSRET invocations can occur from either 32-bit compatibility mode application code or from 64-bit application code. Three related MSR registers (IA32_STAR, IA32_LSTAR, IA32_FMASK) are used in conjunction with fast system calls/returns that use these instructions.

64-Bit hosts which make use of these instructions in the VMM environment will need to save the guest state of the above registers on VM exit, load the host state, and restore the guest state on VM entry. One possible approach is to use the VM-exit MSR-save and MSR-load areas and the VM-entry MSR-load area defined by controls in the VMCS. A disadvantage to this approach, however, is that the approach results in the unconditional saving, loading, and restoring of MSR registers on each VM exit or VM entry.

Depending on the design of the VMM, it is likely that many VM-exits will require no fast system call support but the VMM will be burdened with the additional overhead of saving and restoring MSRs if the VMM chooses to support fast system call uniformly. Further, even if the host intends to support fast system calls during a VM-exit, some of the MSR values (such as the setting of the SCE bit in IA32_EFER) may not require modification as they may already be set to the appropriate value in the guest.

For performance reasons, a VMM may perform lazy save, load, and restore of these MSR values on certain VM exits when it is determined that this is acceptable. The lazy-save-load-restore operation can be carried out “manually” using RDMSR and WRMSR.

31.10.4.4 Handling the SWAPGS Instruction

The SWAPGS instruction is available only in 64-bit mode. It swaps the contents of two specific MSRs (IA32_GSBASE and IA32_KERNEL_GSBASE). The IA32_GSBASE MSR shadows the base address portion of the GS descriptor register; the IA32_KERNEL_GSBASE MSR holds the base address of the GS segment used by the kernel (typically it houses kernel structures). SWAPGS is intended for use with fast system calls when in 64-bit mode to allow immediate access to kernel structures on transition to kernel mode.

Similar to SYSCALL/SYSRET, IA-32e mode hosts which use fast system calls may need to save, load, and restore these MSR registers on VM exit and VM entry using the guidelines discussed in previous paragraphs.

31.10.4.5 Implementation Specific Behavior on Writing to Certain MSRs

As noted in Section 26.4 and Section 27.4, a processor may prevent writing to certain MSRs when loading guest states on VM entries or storing guest states on VM exits. This is done to ensure consistent operation. The subset and number of MSRs subject to restrictions are implementation specific. For initial VMX implementations, there are two MSRs: IA32_BIOS_UPDT_TRIG and IA32_BIOS_SIGN_ID (see Chapter 35).
31.10.5 Handling Accesses to Reserved MSR Addresses

Privileged software (either a VMM or a guest OS) can access a model specific register by specifying addresses in MSR address space. VMMs, however, must prevent a guest from accessing reserved MSR addresses in MSR address space.

Consult Chapter 35 for lists of supported MSRs and their usage. Use the MSR bitmap control to cause a VM exit when a guest attempts to access a reserved MSR address. The response to such a VM exit should be to reflect #GP(0) back to the guest.

31.11 Handling Accesses to Control Registers

Bit fields in control registers (CR0, CR4) control various aspects of processor operation. The VMM must prevent guests from modifying bits in CR0 or CR4 that are reserved at the time the VMM is written.

Guest/host masks should be used by the VMM to cause VM exits when a guest attempts to modify reserved bits. Read shadows should be used to ensure that the guest always reads the reserved value (usually 0) for such bits. The VMM response to VM exits due to attempts from a guest to modify reserved bits should be to emulate the response which the processor would have normally produced (usually a #GP(0)).

31.12 Performance Considerations

VMX provides hardware features that may be used for improving processor virtualization performance. VMMs must be designed to use this support properly. The basic idea behind most of these performance optimizations of the VMM is to reduce the number of VM exits while executing a guest VM.

This section lists ways that VMMs can take advantage of the performance enhancing features in VMX.

- **Read Access to Control Registers.** Analysis of common client workloads with common PC operating systems in a virtual machine shows a large number of VM-exits are caused by control register read accesses (particularly CR0). Reads of CR0 and CR4 do not cause VM exits. Instead, they return values from the CR0/CR4 read-shadows configured by the VMM in the guest controlling-VMCS with the guest-expected values.

- **Write Access to Control Registers.** Most VMM designs require only certain bits of the control registers to be protected from direct guest access. Write access to CR0/CR4 registers can be reduced by defining the host-owned and guest-owned bits in them through the CR0/CR4 host/guest masks in the VMCS. CR0/CR4 write values by the guest are qualified with the mask bits. If they change only guest-owned bits, they are allowed without causing VM exits. Any write that cause changes to host-owned bits cause VM exits and need to be handled by the VMM.

- **Access Rights based Page Table Protection.** For VMM that implement access-rights-based page table protection, the VMCS provides a CR3 target value list that can be consulted by the processor to determine if a VM exit is required. Loading of CR3 with a value matching an entry in the CR3 target-list are allowed to proceed without VM exits. The VMM can utilize the CR3 target-list to save page-table hierarchies whose state is previously verified by the VMM.

- **Page-fault Handling.** Another common cause for a VM exit is due to page-faults induced by guest address remapping done through virtual memory virtualization. VMX provides page-fault error-code mask and match fields in the VMCS to filter VM exits due to page-faults based on their cause (reflected in the error-code).

31.13 Use of the VMX-Preemption Timer

The VMX-preemption timer allows VMM software to preempt guest VM execution after a specified amount of time. Typical VMX-preemption timer usage is to program the initial VM quantum into the timer, save the timer value on each successive VM-exit (using the VM-exit control “save preemption timer value”) and run the VM until the timer expires.

In an alternative scenario, the VMM may use another timer (e.g. the TSC) to track the amount of time the VM has run while still using the VMX-preemption timer for VM preemption. In this scenario the VMM would not save the...
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VMX-preemption timer on each VM-exit but instead would reload the VMX-preemption timer with initial VM quantum less the time the VM has already run. This scenario includes all the VM-entry and VM-exit latencies in the VM run time.

In both scenarios, on each successive VM-entry the VMX-preemption timer contains a smaller value until the VM quantum ends. If the VMX-preemption timer is loaded with a value smaller than the VM-entry latency then the VM will not execute any instructions before the timer expires. The VMM must ensure the initial VM quantum is greater than the VM-entry latency; otherwise the VM will make no forward progress.
CHAPTER 32
VIRTUALIZATION OF SYSTEM RESOURCES

32.1 OVERVIEW

When a VMM is hosting multiple guest environments (VMs), it must monitor potential interactions between software components using the same system resources. These interactions can require the virtualization of resources. This chapter describes the virtualization of system resources. These include: debugging facilities, address translation, physical memory, and microcode update facilities.

32.2 VIRTUALIZATION SUPPORT FOR DEBUGGING FACILITIES

The Intel 64 and IA-32 debugging facilities (see Chapter 17) provide breakpoint instructions, exception conditions, register flags, debug registers, control registers and storage buffers for functions related to debugging system and application software. In VMX operation, a VMM can support debugging system and application software from within virtual machines if the VMM properly virtualizes debugging facilities. The following list describes features relevant to virtualizing these facilities.

- The VMM can program the exception-bitmap (see Section 24.6.3) to ensure it gets control on debug functions (like breakpoint exceptions occurring while executing guest code such as INT3 instructions). Normally, debug exceptions modify debug registers (such as DR6, DR7, IA32_DEBUGCTL). However, if debug exceptions cause VM exits, exiting occurs before register modification.
- The VMM may utilize the VM-entry event injection facilities described in Section 26.5 to inject debug or breakpoint exceptions to the guest. See Section 32.2.1 for a more detailed discussion.
- The MOV-DR exiting control bit in the processor-based VM-execution control field (see Section 24.6.2) can be enabled by the VMM to cause VM exits on explicit guest access of various processor debug registers (for example, MOV to/from DR0-DR7). These exits would always occur on guest access of DR0-DR7 registers regardless of the values in CPL, DR4.DE or DR7.GD. Since all guest task switches cause VM exits, a VMM can control any indirect guest access or modification of debug registers during guest task switches.
- Guest software access to debug-related model-specific registers (such as IA32_DEBUGCTL MSR) can be trapped by the VMM through MSR access control features (such as the MSR-bitmaps that are part of processor-based VM-execution controls). See Section 31.10 for details on MSR virtualization.
- Debug registers such as DR7 and the IA32_DEBUGCTL MSR may be explicitly modified by the guest (through MOV-DR or WRMSR instructions) or modified implicitly by the processor as part of generating debug exceptions. The current values of DR7 and the IA32_DEBUGCTL MSR are saved to guest-state area of VMCS on every VM exit. Pending debug exceptions are debug exceptions that are recognized by the processor but not yet delivered. See Section 26.6.3 for details on pending debug exceptions.
- DR7 and the IA32_DEBUGCTL MSR are loaded from values in the guest-state area of the VMCS on every VM entry. This allows the VMM to properly virtualize debug registers when injecting debug exceptions to guest. Similarly, the RFLAGS\(^1\) register is loaded on every VM entry (or pushed to stack if injecting a virtual event) from guest-state area of the VMCS. Pending debug exceptions are also loaded from guest-state area of VMCS so that they may be delivered after VM entry is completed.

32.2.1 Debug Exceptions

If a VMM emulates a guest instruction that would encounter a debug trap (single step or data or I/O breakpoint), it should cause that trap to be delivered. The VMM should not inject the debug exception using VM-entry event injection, but should set the appropriate bits in the pending debug exceptions field. This method will give the trap the

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\(^1\) This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.).
right priority with respect to other events. (If the exception bitmap was programmed to cause VM exits on debug exceptions, the debug trap will cause a VM exit. At this point, the trap can be injected during VM entry with the proper priority.)

There is a valid pending debug exception if the BS bit (see Table 24-4) is set, regardless of the values of RFLAGS.TF or IA32_DEBUGCTL.BTF. The values of these bits do not impact the delivery of pending debug exceptions.

VMMs should exercise care when emulating a guest write (attempted using WRMSR) to IA32_DEBUGCTL to modify BTF if this is occurring with RFLAGS.TF = 1 and after a MOV SS or POP SS instruction (for example: while debug exceptions are blocked). Note the following:

• Normally, if WRMSR clears BTF while RFLAGS.TF = 1 and with debug exceptions blocked, a single-step trap will occur after WRMSR. A VMM emulating such an instruction should set the BS bit (see Table 24-4) in the pending debug exceptions field before VM entry.

• Normally, if WRMSR sets BTF while RFLAGS.TF = 1 and with debug exceptions blocked, neither a single-step trap nor a taken-branch trap can occur after WRMSR. A VMM emulating such an instruction should clear the BS bit (see Table 24-4) in the pending debug exceptions field before VM entry.

### 32.3 MEMORY VIRTUALIZATION

VMMs must control physical memory to ensure VM isolation and to remap guest physical addresses in host physical address space for virtualization. Memory virtualization allows the VMM to enforce control of physical memory and yet support guest OSs’ expectation to manage memory address translation.

#### 32.3.1 Processor Operating Modes & Memory Virtualization

Memory virtualization is required to support guest execution in various processor operating modes. This includes: protected mode with paging, protected mode with no paging, real-mode and any other transient execution modes. VMX allows guest operation in protected-mode with paging enabled and in virtual-8086 mode (with paging enabled) to support guest real-mode execution. Guest execution in transient operating modes (such as in real mode with one or more segment limits greater than 64-KByte) must be emulated by the VMM.

Since VMX operation requires processor execution in protected mode with paging (through CR0 and CR4 fixed bits), the VMM may utilize paging structures to support memory virtualization. To support guest real-mode execution, the VMM may establish a simple flat page table for guest linear to host physical address mapping. Memory virtualization algorithms may also need to capture other guest operating conditions (such as guest performing A20M# address masking) to map the resulting 20-bit effective guest physical addresses.

#### 32.3.2 Guest & Host Physical Address Spaces

Memory virtualization provides guest software with contiguous guest physical address space starting zero and extending to the maximum address supported by the guest virtual processor’s physical address width. The VMM utilizes guest physical to host physical address mapping to locate all or portions of the guest physical address space in host memory. The VMM is responsible for the policies and algorithms for this mapping which may take into account the host system physical memory map and the virtualized physical memory map exposed to a guest by the VMM. The memory virtualization algorithm needs to accommodate various guest memory uses (such as: accessing DRAM, accessing memory-mapped registers of virtual devices or core logic functions and so forth). For example:

• To support guest DRAM access, the VMM needs to map DRAM-backed guest physical addresses to host-DRAM regions. The VMM also requires the guest to host memory mapping to be at page granularity.

• Virtual devices (I/O devices or platform core logic) emulated by the VMM may claim specific regions in the guest physical address space to locate memory-mapped registers. Guest access to these virtual registers may be configured to cause page-fault induced VM-exits by marking these regions as always not present. The VMM may handle these VM exits by invoking appropriate virtual device emulation code.
32.3.3 Virtualizing Virtual Memory by Brute Force

VMX provides the hardware features required to fully virtualize guest virtual memory accesses. VMX allows the VMM to trap guest accesses to the PAT (Page Attribute Table) MSR and the MTRR (Memory Type Range Registers). This control allows the VMM to virtualize the specific memory type of a guest memory. The VMM may control caching by controlling the guest CR0.CRD and CR0.NW bits, as well as by trapping guest execution of the INVD instruction. The VMM can trap guest CR3 loads and stores, and it may trap guest execution of INVLPG.

Because a VMM must retain control of physical memory, it must also retain control over the processor's address-translation mechanisms. Specifically, this means that only the VMM can access CR3 (which contains the base of the page directory) and can execute INVLPG (the only other instruction that directly manipulates the TLB).

At the same time that the VMM controls address translation, a guest operating system will also expect to perform normal memory management functions. It will access CR3, execute INVLPG, and modify (what it believes to be) page directories and page tables. Virtualization of address translation must tolerate and support guest attempts to control address translation.

A simple-minded way to do this would be to ensure that all guest attempts to access address-translation hardware trap to the VMM where such operations can be properly emulated. It must ensure that accesses to page directories and page tables also get trapped. This may be done by protecting these in-memory structures with conventional page-based protection. The VMM can do this because it can locate the page directory because its base address is in CR3 and the VMM receives control on any change to CR3; it can locate the page tables because their base addresses are in the page directory.

Such a straightforward approach is not necessarily desirable. Protection of the in-memory translation structures may be cumbersome. The VMM may maintain these structures with different values (e.g., different page base addresses) than guest software. This means that there must be traps on guest attempt to read these structures and that the VMM must maintain, in auxiliary data structures, the values to return to these reads. There must also be traps on modifications to these structures even if the translations they effect are never used. All this implies considerable overhead that should be avoided.

32.3.4 Alternate Approach to Memory Virtualization

Guest software is allowed to freely modify the guest page-table hierarchy without causing traps to the VMM. Because of this, the active page-table hierarchy might not always be consistent with the guest hierarchy. Any potential problems arising from inconsistencies can be solved using techniques analogous to those used by the processor and its TLB.

This section describes an alternative approach that allows guest software to freely access page directories and page tables. Traps occur on CR3 accesses and executions of INVLPG. They also occur when necessary to ensure that guest modifications to the translation structures actually take effect. The software mechanisms to support this approach are collectively called virtual TLB. This is because they emulate the functionality of the processor's physical translation look-aside buffer (TLB).

The basic idea behind the virtual TLB is similar to that behind the processor TLB. While the page-table hierarchy defines the relationship between physical to linear address, it does not directly control the address translation of each memory access. Instead, translation is controlled by the TLB, which is occasionally filled by the processor with translations derived from the page-table hierarchy. With a virtual TLB, the page-table hierarchy established by guest software (specifically, the guest operating system) does not control translation, either directly or indirectly. Instead, translation is controlled by the processor (through its TLB) and by the VMM (through a page-table hierarchy that it maintains).

Specifically, the VMM maintains an alternative page-table hierarchy that effectively caches translations derived from the hierarchy maintained by guest software. The remainder of this document refers to the former as the active page-table hierarchy (because it is referenced by CR3 and may be used by the processor to load its TLB) and the latter as the guest page-table hierarchy (because it is maintained by guest software). The entries in the active hierarchy may resemble the corresponding entries in the guest hierarchy in some ways and may differ in others.

Guest software is allowed to freely modify the guest page-table hierarchy without causing VM exits to the VMM. Because of this, the active page-table hierarchy might not always be consistent with the guest hierarchy. Any potential problems arising from any inconsistencies can be solved using techniques analogous to those used by the processor and its TLB. Note the following:
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• Suppose the guest page-table hierarchy allows more access than active hierarchy (for example: there is a translation for a linear address in the guest hierarchy but not in the active hierarchy); this is analogous to a situation in which the TLB allows less access than the page-table hierarchy. If an access occurs that would be allowed by the guest hierarchy but not the active one, a page fault occurs; this is analogous to a TLB miss. The VMM gains control (as it handles all page faults) and can update the active page-table hierarchy appropriately; this corresponds to a TLB fill.

• Suppose the guest page-table hierarchy allows less access than the active hierarchy; this is analogous to a situation in which the TLB allows more access than the page-table hierarchy. This situation can occur only if the guest operating system has modified a page-table entry to reduce access (for example: by marking it not-present). Because the older, more permissive translation may have been cached in the TLB, the processor is architecturally permitted to use the older translation and allow more access. Thus, the VMM may (through the active page-table hierarchy) also allow greater access. For the new, less permissive translation to take effect, guest software should flush any older translations from the TLB either by executing INVLPD or by loading CR3. Because both these operations will cause a trap to the VMM, the VMM will gain control and can remove from the active page-table hierarchy the translations indicated by guest software (the translation of a specific linear address for INVLPD or all translations for a load of CR3).

As noted previously, the processor reads the page-table hierarchy to cache translations in the TLB. It also writes to the hierarchy to maintain the accessed (A) and dirty (D) bits in the PDEs and PTEs. The virtual TLB emulates this behavior as follows:

• When a page is accessed by guest software, the A bit in the corresponding PTE (or PDE for a 4-MByte page) in the active page-table hierarchy will be set by the processor (the same is true for PDEs when active page tables are accessed by the processor). For guest software to operate properly, the VMM should update the A bit in the guest entry at this time. It can do this reliably if it keeps the active PTE (or PDE) marked not-present until it has set the A bit in the guest entry.

• When a page is written by guest software, the D bit in the corresponding PTE (or PDE for a 4-MByte page) in the active page-table hierarchy will be set by the processor. For guest software to operate properly, the VMM should update the D bit in the guest entry at this time. It can do this reliably if it keeps the active PTE (or PDE) marked read-only until it has set the D bit in the guest entry. This solution is valid for guest software running at privilege level 3; support for more privileged guest software is described in Section 32.3.5.

32.3.5 Details of Virtual TLB Operation

This section describes in more detail how a VMM could support a virtual TLB. It explains how an active page-table hierarchy is initialized and how it is maintained in response to page faults, uses of INVLPD, and accesses to CR3. The mechanisms described here are the minimum necessary. They may not result in the best performance.
As noted above, the VMM maintains an active page-table hierarchy for each virtual machine that it supports. It also maintains, for each machine, values that the machine expects for control registers CR0, CR2, CR3, and CR4 (they control address translation). These values are called the guest control registers.

In general, the VMM selects the physical-address space that is allocated to guest software. The term guest address refers to an address installed by guest software in the guest CR3, in a guest PDE (as a page table base address or a page base address), or in a guest PTE (as a page base address). While guest software considers these to be specific physical addresses, the VMM may map them differently.

### 32.3.5.1 Initialization of Virtual TLB

To enable the Virtual TLB scheme, the VMCS must be set up to trigger VM exits on:

- All writes to CR3 (the CR3-target count should be 0) or the paging-mode bits in CR0 and CR4 (using the CR0 and CR4 guest/host masks)
- Page-fault (#PF) exceptions
- Execution of INVLPG

When guest software first enables paging, the VMM creates an aligned 4-KByte active page directory that is invalid (all entries marked not-present). This invalid directory is analogous to an empty TLB.

### 32.3.5.2 Response to Page Faults

Page faults can occur for a variety of reasons. In some cases, the page fault alerts the VMM to an inconsistency between the active and guest page-table hierarchy. In such cases, the VMM can update the former and re-execute the faulting instruction. In other cases, the hierarchies are already consistent and the fault should be handled by the guest operating system. The VMM can detect this and use an established mechanism for raising a page fault to guest software.

The VMM can handle a page fault by following these steps (The steps below assume the guest is operating in a paging mode without PAE. Analogous steps to handle address translation using PAE or four-level paging mecha-
nisms can be derived by VMM developers according to the paging behavior defined in Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A):

1. First consult the active PDE, which can be located using the upper 10 bits of the faulting address and the current value of CR3. The active PDE is the source of the fault if it is marked not present or if its R/W bit and U/S bits are inconsistent with the attempted guest access (the guest privilege level and the values of CR0.WP and CR4.SMEP should also be taken into account).

2. If the active PDE is the source of the fault, consult the corresponding guest PDE using the same 10 bits from the faulting address and the physical address that corresponds to the guest address in the guest CR3. If the guest PDE would cause a page fault (for example: it is marked not present), then raise a page fault to the guest operating system.

The following steps assume that the guest PDE would not have caused a page fault.

3. If the active PDE is the source of the fault and the guest PDE contains, as page-table base address (if PS = 0) or page base address (PS = 1), a guest address that the VMM has chosen not to support; then raise a machine check (or some other abort) to the guest operating system.

The following steps assume that the guest address in the guest PDE is supported for the virtual machine.

4. If the active PDE is marked not-present, then set the active PDE to correspond to guest PDE as follows:
   a. If the active PDE contains a page-table base address (if PS = 0), then allocate an aligned 4-KByte active page table marked completely invalid and set the page-table base address in the active PDE to be the physical address of the newly allocated page table.
   b. If the active PDE contains a page base address (if PS = 1), then set the page base address in the active PDE to be the physical page base address that corresponds to the guest address in the guest PDE.
   c. Set the P, U/S, and PS bits in the active PDE to be identical to those in the guest PDE.
   d. Set the PWT, PCD, and G bits according to the policy of the VMM.
   e. Set A = 1 in the guest PDE.
   f. If D = 1 in the guest PDE or PS = 0 (meaning that this PDE refers to a page table), then set the R/W bit in the active PDE as in the guest PDE.
   g. If D = 0 in the guest PDE, PS = 1 (this is a 4-MByte page), and the attempted access is a write; then set R/W in the active PDE as in the guest PDE and set D = 1 in the guest PDE.
   h. If D = 0 in the guest PDE, PS = 1, and the attempted access is not a write; then set R/W = 0 in the active PDE.
   i. After modifying the active PDE, re-execute the faulting instruction.

The remaining steps assume that the active PDE is already marked present.

5. If the active PDE is the source of the fault, the active PDE refers to a 4-MByte page (PS = 1), the attempted access is a write; D = 0 in the guest PDE, and the active PDE has caused a fault solely because it has R/W = 0; then set R/W in the active PDE as in the guest PDE; set D = 1 in the guest PDE, and re-execute the faulting instruction.

6. If the active PDE is the source of the fault and none of the above cases apply, then raise a page fault of the guest operating system.

The remaining steps assume that the source of the original page fault is not the active PDE.

NOTE

It is possible that the active PDE might be causing a fault even though the guest PDE would not. However, this can happen only if the guest operating system increased access in the guest PDE and did not take action to ensure that older translations were flushed from the TLB. Such translations might have caused a page fault if the guest software were running on bare hardware.

7. If the active PDE refers to a 4-MByte page (PS = 1) but is not the source of the fault, then the fault resulted from an inconsistency between the active page-table hierarchy and the processor’s TLB. Since the transition to
the VMM caused an address-space change and flushed the processor’s TLB, the VMM can simply re-execute the faulting instruction.

The remaining steps assume that PS = 0 in the active and guest PDEs.

8. Consult the active PTE, which can be located using the next 10 bits of the faulting address (bits 21–12) and the physical page-table base address in the active PDE. The active PTE is the source of the fault if it is marked not-present or if its R/W bit and U/S bits are inconsistent with the attempted guest access (the guest privilege level and the values of CR0.WP and CR4.SMEP should also be taken into account).

9. If the active PTE is not the source of the fault, then the fault has resulted from an inconsistency between the active page-table hierarchy and the processor’s TLB. Since the transition to the VMM caused an address-space change and flushed the processor’s TLB, the VMM simply re-executes the faulting instruction.

The remaining steps assume that the active PTE is the source of the fault.

10. Consult the corresponding guest PTE using the same 10 bits from the faulting address and the physical address that correspond to the guest page-table base address in the guest PDE. If the guest PTE would cause a page fault (it is marked not-present), the raise a page fault to the guest operating system.

The following steps assume that the guest PTE would not have caused a page fault.

11. If the guest PTE contains, as page base address, a physical address that is not valid for the virtual machine being supported; then raise a machine check (or some other abort) to the guest operating system.

The following steps assume that the address in the guest PTE is valid for the virtual machine.

12. If the active PTE is marked not-present, then set the active PTE to correspond to guest PTE:
   a. Set the page base address in the active PTE to be the physical address that corresponds to the guest page base address in the guest PTE.
   b. Set the P, U/S, and PS bits in the active PTE to be identical to those in the guest PTE.
   c. Set the PWT, PCD, and G bits according to the policy of the VMM.
   d. Set A = 1 in the guest PTE.
   e. If D = 1 in the guest PTE, then set the R/W bit in the active PTE as in the guest PTE.
   f. If D = 0 in the guest PTE and the attempted access is a write, then set R/W in the active PTE as in the guest PTE and set D = 1 in the guest PTE.
   g. If D = 0 in the guest PTE and the attempted access is not a write, then set R/W = 0 in the active PTE.
   h. After modifying the active PTE, re-execute the faulting instruction.

The remaining steps assume that the active PTE is already marked present.

13. If the attempted access is a write, D = 0 (not dirty) in the guest PTE and the active PTE has caused a fault solely because it has R/W = 0 (read-only); then set R/W in the active PTE as in the guest PTE, set D = 1 in the guest PTE and re-execute the faulting instruction.

14. If none of the above cases apply, then raise a page fault of the guest operating system.

### 32.3.5.3 Response to Uses of INVLPG

Operating-systems can use INVLPG to flush entries from the TLB. This instruction takes a linear address as an operand and software expects any cached translations for the address to be flushed. A VMM should set the processor-based VM-execution control “INVLPG exiting” to 1 so that any attempts by a privileged guest to execute INVLPG will trap to the VMM. The VMM can then modify the active page-table hierarchy to emulate the desired effect of the INVLPG.

The following steps are performed. Note that these steps are performed only if the guest invocation of INVLPG would not fault and only if the guest software is running at privilege level 0:

1. Locate the relevant active PDE using the upper 10 bits of the operand address and the current value of CR3. If the PDE refers to a 4-MByte page (PS = 1), then set P = 0 in the PDE.
2. If the PDE is marked present and refers to a page table (PS = 0), locate the relevant active PTE using the next 10 bits of the operand address (bits 21–12) and the page-table base address in the PDE. Set P = 0 in the PTE.
Examine all PTEs in the page table; if they are now all marked not-present, de-allocate the page table and set 
P = 0 in the PDE (this step may be optional).

32.3.5.4  Response to CR3 Writes
A guest operating system may attempt to write to CR3. Any write to CR3 implies a TLB flush and a possible page 
table change. The following steps are performed:
1. The VMM notes the new CR3 value (used later to walk guest page tables) and emulates the write.
2. The VMM allocates a new PD page, with all invalid entries.
3. The VMM sets actual processor CR3 register to point to the new PD page.
The VMM may, at this point, speculatively fill in VTLB mappings for performance reasons.

32.4  MICROCODE UPDATE FACILITY
The microcode code update facility may be invoked at various points during the operation of a platform. Typically, 
the BIOS invokes the facility on all processors during the BIOS boot process. This is sufficient to boot the BIOS and 
operating system. As a microcode update more current than the system BIOS may be available, system software 
should provide another mechanism for invoking the microcode update facility. The implications of the microcode 
update mechanism on the design of the VMM are described in this section.

NOTE
Microcode updates must not be performed during VMX non-root operation. Updates performed in 
VMX non-root operation may result in unpredictable system behavior.

32.4.1  Early Load of Microcode Updates
The microcode update facility may be invoked early in the VMM or guest OS boot process. Loading the microcode 
update early provides the opportunity to correct errata affecting the boot process but the technique generally 
requires a reboot of the software.
A microcode update may be loaded from the OS or VMM image loader. Typically, such image loaders do not run on 
every logical processor, so this method effects only one logical processor. Later in the VMM or OS boot process, 
after bringing all application processors on-line, the VMM or OS needs to invoke the microcode update facility for all 
application processors.
Depending on the order of the VMM and the guest OS boot, the microcode update facility may be invoked by the 
VMM or the guest OS. For example, if the guest OS boots first and then loads the VMM, the guest OS may invoke 
the microcode update facility on all the logical processors. If a VMM boots before its guests, then the VMM may 
invoke the microcode update facility during its boot process. In both cases, the VMM or OS should invoke the micro-
code update facilities soon after performing the multiprocessor startup.
In the early load scenario, microcode updates may be contained in the VMM or OS image or, the VMM or OS may 
manage a separate database or file of microcode updates. Maintaining a separate microcode update image data-
base has the advantage of reducing the number of required VMM or OS releases as a result of microcode update 
releases.

32.4.2  Late Load of Microcode Updates
A microcode update may be loaded during normal system operation. This allows system software to activate the 
microcode update at anytime without requiring a system reboot. This scenario does not allow the microcode update 
to correct errata which affect the processor’s boot process but does allow high-availability systems to activate 
microcode updates without interrupting the availability of the system. In this late load scenario, either the VMM or 
a designated guest may load the microcode update. If the guest is loading the microcode update, the VMM must
make sure that the entire guest memory buffer (which contains the microcode update image) will not cause a page fault when accessed.

If the VMM loads the microcode update, then the VMM must have access to the current set of microcode updates. These updates could be part of the VMM image or could be contained in a separate microcode update image database (for example: a database file on disk or in memory). Again, maintaining a separate microcode update image database has the advantage of reducing the number of required VMM or OS releases as a result of microcode update releases.

The VMM may wish to prevent a guest from loading a microcode update or may wish to support the microcode update requested by a guest using emulation (without actually loading the microcode update). To prevent microcode update loading, the VMM may return a microcode update signature value greater than the value of IA32_BIOS_SIGN_ID MSR. A well-behaved guest will not attempt to load an older microcode update. The VMM may also drop the guest attempts to write to IA32_BIOS_UPDT_TRIG MSR, preventing the guest from loading any microcode updates. Later, when the guest queries IA32_BIOS_SIGN_ID MSR, the VMM could emulate the microcode update signature that the guest expects.

In general, loading a microcode update later will limit guest software’s visibility of features that may be enhanced by a microcode update.
VIRTUALIZATION OF SYSTEM RESOURCES
33.1 OVERVIEW

This chapter describes what a VMM must consider when handling exceptions, interrupts, error conditions, and transitions between activity states.

33.2 INTERRUPT HANDLING IN VMX OPERATION

The following bullets summarize VMX support for handling interrupts:

- **Control of processor exceptions.** The VMM can get control on specific guest exceptions through the exception-bitmap in the guest controlling VMCS. The exception bitmap is a 32-bit field that allows the VMM to specify processor behavior on specific exceptions (including traps, faults, and aborts). Setting a specific bit in the exception bitmap implies VM exits will be generated when the corresponding exception occurs. Any exceptions that are programmed not to cause VM exits are delivered directly to the guest through the guest IDT. The exception bitmap also controls execution of relevant instructions such as BOUND, INTO and INT3. VM exits on page-faults are treated in such a way the page-fault error code is qualified through the page-fault-error-code mask and match fields in the VMCS.

- **Control over triple faults.** If a fault occurs while attempting to call a double-fault handler in the guest and that fault is not configured to cause a VM exit in the exception bitmap, the resulting triple fault causes a VM exit.

- **Control of external interrupts.** VMX allows both host and guest control of external interrupts through the "external-interrupt exiting" VM execution control. If the control is 0, external-interrupts do not cause VM exits and the interrupt delivery is masked by the guest programmed RFLAGS.IF value. If the control is 1, external-interrupts causes VM exits and are not masked by RFLAGS.IF. The VMM can identify VM exits due to external interrupts by checking the exit reason for an "external interrupt" (value = 1).

- **Control of other events.** There is a pin-based VM-execution control that controls system behavior (exit or no-exit) for NMI events. Most VMM usages will need handling of NMI external events in the VMM and hence will specify host control of these events.

Some processors also support a pin-based VM-execution control called "virtual NMIs." When this control is set, NMIs cause VM exits, but the processor tracks guest readiness for virtual NMIs. This control interacts with the "NMI-window exiting" VM-execution control (see below).

INIT and SIPI events always cause VM exits.

- **Acknowledge interrupt on exit.** The "acknowledge interrupt on exit" VM-exit control in the controlling VMCS controls processor behavior for external interrupt acknowledgement. If the control is 1, the processor acknowledges the interrupt controller to acquire the interrupt vector upon VM exit, and stores the vector in the VM-exit interruption-information field. If the control is 0, the external interrupt is not acknowledged during VM exit. Since RFLAGS.IF is automatically cleared on VM exits due to external interrupts, VMM re-enabling of interrupts (setting RFLAGS.IF = 1) initiates the external interrupt acknowledgement and vectoring of the external interrupt through the monitor/host IDT.

- **Event-masking Support.** VMX captures the masking conditions of specific events while in VMX non-root operation through the interruptibility-state field in the guest-state area of the VMCS.

This feature allows proper virtualization of various interrupt blocking states, such as: (a) blocking of external interrupts for the instruction following STI; (b) blocking of interrupts for the instruction following a MOV-SS or POP-SS instruction; (c) SMI blocking of subsequent SMIs until the next execution of RSM; and (d) NMI/SMI blocking of NMIs until the next execution of IRET or RSM.

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1. This chapter uses the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of those registers (EAX, EIP, ESP, EFLAGS, etc.).
INIT and SIPI events are treated specially. INIT assertions are always blocked in VMX root operation and while in SMM, and unblocked otherwise. SIPI events are always blocked in VMX root operation.

The interruptibility state is loaded from the VMCS guest-state area on every VM entry and saved into the VMCS on every VM exit.

- **Event injection.** VMX operation allows injecting interruptions to a guest virtual machine through the use of VM-entry interrupt-information field in VMCS. Injectable interruptions include external interrupts, NMI, processor exceptions, software generated interrupts, and software traps. If the interrupt-information field indicates a valid interrupt, exception or trap event upon the next VM entry; the processor will use the information in the field to vector a virtual interruption through the guest IDT after all guest state and MSRs are loaded. Delivery through the guest IDT emulates vectoring in non-VMX operation by doing the normal privilege checks and pushing appropriate entries to the guest stack (entries may include RFLAGS, EIP and exception error code). A VMM with host control of NMI and external interrupts can use the event-injection facility to forward virtual interruptions to various guest virtual machines.

- **Interrupt-window exiting.** When set to 1, the "interrupt-window exiting" VM-execution control (Section 24.6.2) causes VM exits when guest RFLAGS.IF is 1 and no other conditions block external interrupts. A VM exit occurs at the beginning of any instruction at which RFLAGS.IF = 1 and on which the interruptibility state of the guest would allow delivery of an interrupt. For example: when the guest executes an STI instruction, RFLAGS = 1, and if at the completion of next instruction the interruptibility state masking due to STI is removed; a VM exit occurs if the "interrupt-window exiting" VM-execution control is 1. This feature allows a VMM to queue a virtual interrupt to the guest when the guest is not in an interruptible state. The VMM can set the "interrupt-window exiting" VM-execution control for the guest and depend on a VM exit to know when the guest becomes interruptible (and, therefore, when it can inject a virtual interrupt). The VMM can detect such VM exits by checking for the basic exit reason "interrupt-window" (value = 7). If this feature is not used, the VMM will need to poll and check the interruptibility state of the guest to deliver virtual interrupts.

- **NMI-window exiting.** If the "virtual NMIs" VM-execution is set, the processor tracks virtual-NMI blocking. The "NMI-window exiting" VM-execution control (Section 24.6.2) causes VM exits when there is no virtual-NMI blocking. For example, after execution of the IRET instruction, a VM exit occurs if the "NMI-window exiting" VM-execution control is 1. This feature allows a VMM to queue a virtual NMI to a guest when the guest is not ready to receive NMIs. The VMM can set the "NMI-window exiting" VM-execution control for the guest and depend on a VM exit to know when the guest becomes ready for NMIs (and, therefore, when it can inject a virtual NMI). The VMM can detect such VM exits by checking for the basic exit reason "NMI window" (value = 8). If this feature is not used, the VMM will need to poll and check the interruptibility state of the guest to deliver virtual NMIs.

- **VM-exit information.** The VM-exit information fields provide details on VM exits due to exceptions and interrupts. This information is provided through the exit-qualification, VM-exit-interruption-information, instruction-length and interruption-error-code fields. Also, for VM exits that occur in the course of vectoring through the guest IDT, information about the event that was being vectored through the guest IDT is provided in the IDT-vectoring-information and IDT-vectoring-error-code fields. These information fields allow the VMM to identify the exception cause and to handle it properly.

### 33.3 EXTERNAL INTERRUPT VIRTUALIZATION

VMX operation allows both host and guest control of external interrupts. While guest control of external interrupts might be suitable for partitioned usages (different CPU cores/threads and I/O devices partitioned to independent virtual machines), most VMMs built upon VMX are expected to utilize host control of external interrupts. The rest of this section describes a general host-controlled interrupt virtualization architecture for standard PC platforms through the use of VMX supported features.

With host control of external interrupts, the VMM (or the host OS in a hosted VMM model) manages the physical interrupt controllers in the platform and the interrupts generated through them. The VMM exposes software-emulated virtual interrupt controller devices (such as PIC and APIC) to each guest virtual machine instance.
33.3.1 Virtualization of Interrupt Vector Space

The Intel 64 and IA-32 architectures use 8-bit vectors of which 224 (20H – FFH) are available for external interrupts. Vectors are used to select the appropriate entry in the interrupt descriptor table (IDT). VMX operation allows each guest to control its own IDT. Host vectors refer to vectors delivered by the platform to the processor during the interrupt acknowledgement cycle. Guest vectors refer to vectors programmed by a guest to select an entry in its guest IDT. Depending on the I/O resource management models supported by the VMM design, the guest vector space may or may not overlap with the underlying host vector space.

- Interrupts from virtual devices: Guest vector numbers for virtual interrupts delivered to guests on behalf of emulated virtual devices have no direct relation to the host vector numbers of interrupts from physical devices on which they are emulated. A guest-vector assigned for a virtual device by the guest operating environment is saved by the VMM and utilized when injecting virtual interrupts on behalf of the virtual device.

- Interrupts from assigned physical devices: Hardware support for I/O device assignment allows physical I/O devices in the host platform to be assigned (direct-mapped) to VMs. Guest vectors for interrupts from direct-mapped physical devices take up equivalent space from the host vector space, and require the VMM to perform host-vector to guest-vector mapping for interrupts.

Figure 33-1 illustrates the functional relationship between host external interrupts and guest virtual external interrupts. Device A is owned by the host and generates external interrupts with host vector X. The host IDT is set up such that the interrupt service routine (ISR) for device driver A is hooked to host vector X as normal. VMM emulates (over device A) virtual device C in software which generates virtual interrupts to the VM with guest expected vector P. Device B is assigned to a VM and generates external interrupts with host vector Y. The host IDT is programmed to hook the VMM interrupt service routine (ISR) for assigned devices for vector Y, and the VMM handler injects virtual interrupt with guest vector Q to the VM. The guest operating system programs the guest to hook appropriate guest driver’s ISR to vectors P and Q.
33.3.2 Control of Platform Interrupts

To meet the interrupt virtualization requirements, the VMM needs to take ownership of the physical interrupts and the various interrupt controllers in the platform. VMM control of physical interrupts may be enabled through the host-control settings of the “external-interrupt exiting” VM-execution control. To take ownership of the platform interrupt controllers, the VMM needs to expose the virtual interrupt controller devices to the virtual machines and restrict guest access to the platform interrupt controllers.

Intel 64 and IA-32 platforms can support three types of external interrupt control mechanisms: Programmable Interrupt Controllers (PIC), Advanced Programmable Interrupt Controllers (APIC), and Message Signaled Interrupts (MSI). The following sections provide information on the virtualization of each of these mechanisms.

33.3.2.1 PIC Virtualization

Typical PIC-enabled platform implementations support dual 8259 interrupt controllers cascaded as master and slave controllers. They supporting up to 15 possible interrupt inputs. The 8259 controllers are programmed through initialization command words (ICWx) and operation command words (OCWx) accessed through specific I/O ports. The various interrupt line states are captured in the PIC through interrupt requests, interrupt service routines and interrupt mask registers.

Guest access to the PIC I/O ports can be restricted by activating I/O bitmaps in the guest controlling-VMCS (activate-I/O-bitmap bit in VM-execution control field set to 1) and pointing the I/O-bitmap physical addresses to valid
bitmap regions. Bits corresponding to the PIC I/O ports can be cleared to cause a VM exit on guest access to these ports.

If the VMM is not supporting direct access to any I/O ports from a guest, it can set the unconditional-I/O-exiting in the VM-execution control field instead of activating I/O bitmaps. The exit-reason field in VM-exit information allows identification of VM exits due to I/O access and can provide an exit-qualification to identify details about the guest I/O operation that caused the VM exit.

The VMM PIC virtualization needs to emulate the platform PIC functionality including interrupt priority, mask, request and service states, and specific guest programmed modes of PIC operation.

### 33.3.2.2 xAPIC Virtualization

Most modern Intel 64 and IA-32 platforms include support for an APIC. While the standard PIC is intended for use on uniprocessor systems, APIC can be used in either uniprocessor or multi-processor systems.

APIC based interrupt control consists of two physical components: the interrupt acceptance unit (Local APIC) which is integrated with the processor, and the interrupt delivery unit (I/O APIC) which is part of the I/O subsystem. APIC virtualization involves protecting the platform’s local and I/O APICs and emulating them for the guest.

### 33.3.2.3 Local APIC Virtualization

The local APIC is responsible for the local interrupt sources, interrupt acceptance, dispensing interrupts to the logical processor, and generating inter-processor interrupts. Software interacts with the local APIC by reading and writing its memory-mapped registers residing within a 4-KByte uncached memory region with base address stored in the IA32_APIC_BASE MSR. Since the local APIC registers are memory-mapped, the VMM can utilize memory virtualization techniques (such as page-table virtualization) to trap guest accesses to the page frame hosting the virtual local APIC registers.

Local APIC virtualization in the VMM needs to emulate the various local APIC operations and registers, such as: APIC identification/format registers, the local vector table (LVT), the interrupt command register (ICR), interrupt capture registers (TMR, IRR and ISR), task and processor priority registers (TPR, PPR), the EOI register and the APIC-timer register. Since local APICs are designed to operate with non-specific EOI, local APIC emulation also needs to emulate broadcast of EOI to the guest’s virtual I/O APICs for level triggered virtual interrupts.

A local APIC allows interrupt masking at two levels: (1) mask bit in the local vector table entry for local interrupts and (2) raising processor priority through the TPR registers for masking lower priority external interrupts. The VMM needs to comprehend these virtual local APIC mask settings as programmed by the guest in addition to the guest virtual processor interruptibility state (when injecting APIC routed external virtual interrupts to a guest VM).

VMX provides several features which help the VMM to virtualize the local APIC. These features allow many of guest TPR accesses (using CR8 only) to occur without VM exits to the VMM:

- The VMCS contains a “virtual-APIC address” field. This 64-bit field is the physical address of the 4-KByte virtual APIC page (4-KByte aligned). The virtual-APIC page contains a TPR shadow, which is accessed by the MOV CR8 instruction. The TPR shadow comprises bits 7:4 in byte 80H of the virtual-APIC page.

- The TPR threshold: bits 3:0 of this 32-bit field determine the threshold below which the TPR shadow cannot fall. A VM exit will occur after an execution of MOV CR8 that reduces the TPR shadow below this value.

- The processor-based VM-execution controls field contains a “use TPR shadow” bit and a “CR8-store exiting” bit. If the “use TPR shadow” VM-execution control is 1 and the “CR8-store exiting” VM-execution control is 0, then a MOV from CR8 reads from the TPR shadow. If the “CR8-store exiting” VM-execution control is 1, then MOV from CR8 causes a VM exit; the “use TPR shadow” VM-execution control is ignored in this case.

- The processor-based VM-execution controls field contains a “CR8-load exiting” bit. If the “use TPR shadow” VM-execution control is set and the “CR8-load exiting” VM-execution control is clear, then MOV to CR8 writes to the “TPR shadow”. A VM exit will occur after this write if the value written is below the TPR threshold. If the “CR8-load exiting” VM-execution control is set, then MOV to CR8 causes a VM exit; the “use TPR shadow” VM-execution control is ignored in this case.
### 33.3.2.4 I/O APIC Virtualization

The I/O APIC registers are typically mapped to a 1 MByte region where each I/O APIC is allocated a 4K address window within this range. The VMM may utilize physical memory virtualization to trap guest accesses to the virtual I/O APIC memory-mapped registers. The I/O APIC virtualization needs to emulate the various I/O APIC operations and registers such as identification/version registers, indirect-I/O-access registers, EOI register, and the I/O redirection table. I/O APIC virtualization also need to emulate various redirection table entry settings such as delivery mode, destination mode, delivery status, polarity, masking, and trigger mode programmed by the guest and track remote-IRR state on guest EOI writes to various virtual local APICs.

### 33.3.2.5 Virtualization of Message Signaled Interrupts

The PCI Local Bus Specification (Rev. 2.2) introduces the concept of message signaled interrupts (MSI). MSI enable PCI devices to request service by writing a system-specified message to a system specified address. The transaction address specifies the message destination while the transaction data specifies the interrupt vector, trigger mode and delivery mode. System software is expected to configure the message data and address during MSI device configuration, allocating one or more no-shared messages to MSI capable devices. Chapter 10, “Advanced Programmable Interrupt Controller (APIC),” specifies the MSI message address and data register formats to be followed on Intel 64 and IA-32 platforms. While MSI is optional for conventional PCI devices, it is the preferred interrupt mechanism for PCI-Express devices.

Since the MSI address and data are configured through PCI configuration space, to control these physical interrupts the VMM needs to assume ownership of PCI configuration space. This allows the VMM to capture the guest configuration of message address and data for MSI-capable virtual and assigned guest devices. PCI configuration transactions on PC-compatible systems are generated by software through two different methods:

1. The standard CONFIG_ADDRESS/CONFIG_DATA register mechanism (CFCH/CF8H ports) as defined in the PCI Local Bus Specification.
2. The enhanced flat memory-mapped (MEMCFG) configuration mechanism as defined in the PCI-Express Base Specification (Rev. 1.0a.).

The CFCH/CF8H configuration access from guests can be trapped by the VMM through use of I/O-bitmap VM-execution controls. The memory-mapped PCI-Express MEMCFG guest configuration accesses can be trapped by VMM through physical memory virtualization.

### 33.3.3 Examples of Handling of External Interrupts

The following sections illustrate interrupt processing in a VMM (when used to support the external interrupt virtualization requirements).

#### 33.3.3.1 Guest Setup

The VMM sets up the guest to cause a VM exit to the VMM on external interrupts. This is done by setting the “external-interrupt exiting” VM-execution control in the guest controlling-VMCS.

#### 33.3.3.2 Processor Treatment of External Interrupt

Interrupts are automatically masked by hardware in the processor on VM exit by clearing RFLAGS.IF. The exit-reason field in VMCS is set to 1 to indicate an external interrupt as the exit reason.

If the VMM is utilizing the acknowledge-on-exit feature (by setting the “acknowledge interrupt on exit” VM-exit control), the processor acknowledges the interrupt, retrieves the host vector, and saves the interrupt in the VM-exit-interruption-information field (in the VM-exit information region of the VMCS) before transitioning control to the VMM.
33.3.3.3 Processing of External Interrupts by VMM

Upon VM exit, the VMM can determine the exit cause of an external interrupt by checking the exit-reason field (value = 1) in VMCS. If the acknowledge-interrupt-on-exit control (see Section 24.7.1) is enabled, the VMM can use the saved host vector (in the exit-interruption-information field) to switch to the appropriate interrupt handler. If the "acknowledge interrupt on exit" VM-exit control is 0, the VMM may re-enable interrupts (by setting RFLAGS.IF) to allow vectoring of external interrupts through the monitor/host IDT.

The following steps may need to be performed by the VMM to process an external interrupt:

- **Host Owned I/O Devices**: For host-owned I/O devices, the interrupting device is owned by the VMM (or hosting OS in a hosted VMM). In this model, the interrupt service routine in the VMM/host driver is invoked and, upon ISR completion, the appropriate write sequences (TPR updates, EOI etc.) to respective interrupt controllers are performed as normal. If the work completion indicated by the driver implies virtual device activity, the VMM runs the virtual device emulation. Depending on the device class, physical device activity could imply activity by multiple virtual devices mapped over the device. For each affected virtual device, the VMM injects a virtual external interrupt event to respective guest virtual machines. The guest driver interacts with the emulated virtual device to process the virtual interrupt. The interrupt controller emulation in the VMM supports various guest accesses to the VMM’s virtual interrupt controller.

- **Guest Assigned I/O Devices**: For assigned I/O devices, either the VMM uses a software proxy or it can directly map the physical device to the assigned VM. In both cases, servicing of the interrupt condition on the physical device is initiated by the driver running inside the guest VM. With host control of external interrupts, interrupts from assigned physical devices cause VM exits to the VMM and vectoring through the host IDT to the registered VMM interrupt handler. To unblock delivery of other low priority platform interrupts, the VMM interrupt handler must mask the interrupt source (for level triggered interrupts) and issue the appropriate EOI write sequences.

Once the physical interrupt source is masked and the platform EOI generated, the VMM can map the host vector to its corresponding guest vector to inject the virtual interrupt into the assigned VM. The guest software does EOI write sequences to its virtual interrupt controller after completing interrupt processing. For level triggered interrupts, these EOI writes to the virtual interrupt controller may be trapped by the VMM which may in turn unmask the previously masked interrupt source.

33.3.3.4 Generation of Virtual Interrupt Events by VMM

The following provides some of the general steps that need to be taken by VMM designs when generating virtual interrupts:

1. Check virtual processor interruptibility state. The virtual processor interruptibility state is reflected in the guest RFLAGS.IF flag and the processor interruptibility-state saved in the guest state area of the controlling-VMCS. If RFLAGS.IF is set and the interruptibility state indicates readiness to take external interrupts (STI-masking and MOV-SS/POP-SS-masking bits are clear), the guest virtual processor is ready to take external interrupts. If the VMM design supports non-active guest sleep states, the VMM needs to make sure the current guest sleep state allows injection of external interrupt events.

2. If the guest virtual processor state is currently not interruptible, a VMM may utilize the "interrupt-window exiting" VM-execution to notify the VMM (through a VM exit) when the virtual processor state changes to interruptible state.

3. Check the virtual interrupt controller state. If the guest VM exposes a virtual local APIC, the current value of its processor priority register specifies if guest software allows dispensing an external virtual interrupt with a specific priority to the virtual processor. If the virtual interrupt is routed through the local vector table (LVT) entry of the local APIC, the mask bits in the corresponding LVT entry specifies if the interrupt is currently masked. Similarly, the virtual interrupt controller’s current mask (IO-APIC or PIC) and priority settings reflect guest state to accept specific external interrupts. The VMM needs to check both the virtual processor and interrupt controller states to verify its guest interruptibility state. If the guest is currently interruptible, the VMM can inject the virtual interrupt. If the current guest state does not allow injecting a virtual interrupt, the interrupt needs to be queued by the VMM until it can be delivered.

4. Prioritize the use of VM-entry event injection. A VMM may use VM-entry event injection to deliver various virtual events (such as external interrupts, exceptions, traps, and so forth). VMM designs may prioritize use of virtual-interrupt injection between these event types. Since each VM entry allows injection of one event,
depending on the VMM event priority policies, the VMM may need to queue the external virtual interrupt if a higher priority event is to be delivered on the next VM entry. Since the VMM has masked this particular interrupt source (if it was level triggered) and done EOI to the platform interrupt controller, other platform interrupts can be serviced while this virtual interrupt event is queued for later delivery to the VM.

5. Update the virtual interrupt controller state. When the above checks have passed, before generating the virtual interrupt to the guest, the VMM updates the virtual interrupt controller state (Local-APIC, IO-APIC and/or PIC) to reflect assertion of the virtual interrupt. This involves updating the various interrupt capture registers, and priority registers as done by the respective hardware interrupt controllers. Updating the virtual interrupt controller state is required for proper interrupt event processing by guest software.

6. Inject the virtual interrupt on VM entry. To inject an external virtual interrupt to a guest VM, the VMM sets up the VM-entry interruption-information field in the guest controlling-VMCS before entry to guest using VMRESUME. Upon VM entry, the processor will use this vector to access the gate in guest’s IDT and the value of RFLAGS and EIP in guest-state area of controlling-VMCS is pushed on the guest stack. If the guest RFLAGS.IF is clear, the STI-masking bit is set, or the MOV-SS/POP-SS-masking bit is set, the VM entry will fail and the processor will load state from the host-state area of the working VMCS as if a VM exit had occurred (see Section 26.7).

33.4 ERROR HANDLING BY VMM

Error conditions may occur during VM entries and VM exits and a few other situations. This section describes how VMM should handle these error conditions, including triple faults and machine-check exceptions.

33.4.1 VM-Exit Failures

All VM exits load processor state from the host-state area of the VMCS that was the controlling VMCS before the VM exit. This state is checked for consistency while being loaded. Because the host-state is checked on VM entry, these checks will generally succeed. Failure is possible only if host software is incorrect or if VMCS data in the VMCS region in memory has been written by guest software (or by I/O DMA) since the last VM entry. VM exits may fail for the following reasons:

• There was a failure on storing guest MSRs.
• There was failure in loading a PD PTR.
• The controlling VMCS has been corrupted (through writes to the corresponding VMCS region) in such a way that the implementation cannot complete the VM exit.
• There was a failure on loading host MSRs.
• A machine-check event occurred.

If one of these problems occurs on a VM exit, a VMX abort results.

33.4.2 Machine-Check Considerations

The following sequence determine how machine-check events are handled during VMXON, VMXOFF, VM entries, and VM exits:

• VMXOFF and VMXON:
  If a machine-check event occurs during VMXOFF or VMXON and CR4.MCE = 1, a machine-check exception (#MC) is generated. If CR4.MCE = 0, the processor goes to shutdown state.

• VM entry:
  If a machine-check event occurs during VM entry, one of the following three treatments must occur:
  a. Normal delivery before VM entry. If CR4.MCE = 1 before VM entry, delivery of a machine-check exception (#MC) through the host IDT occurs. If CR4.MCE = 0, the processor goes to shutdown state.
HANDLING BOUNDARY CONDITIONS IN A VIRTUAL MACHINE MONITOR

b. Normal delivery after VM entry. If CR4.MCE = 1 after VM entry, delivery of a machine-check exception (#MC) through the guest IDT occurs (alternatively, this exception may cause a VM exit). If CR4.MCE = 0, the processor goes to shutdown state.

c. Load state from the host-state area of the working VMCS as if a VM exit had occurred (see Section 26.7). The basic exit reason will be “VM-entry failure due to machine-check event.”

If the machine-check event occurs after any guest state has been loaded, option a above will not be used; it may be used if the machine-check event occurs while checking host state and VMX controls (or while reporting a failure due to such checks). An implementation may use option b only if all guest state has been loaded properly.

• VM exit:

If a machine-check event occurs during VM exit, one of the following three treatments must occur:

a. Normal delivery before VM exit. If CR4.MCE = 1 before the VM exit, delivery of a machine-check exception (#MC) through the guest IDT (alternatively, this may cause a VM exit). If CR4.MCE = 0, the processor goes to shutdown state.

b. Normal delivery after VM exit. If CR4.MCE = 1 after the VM exit, delivery of a machine-check exception (#MC) through the host IDT. If CR4.MCE = 0, the processor goes to shutdown state.

c. Fail the VM exit. If the VM exit is to VMX root operation, a VMX abort will result; it will block events as done normally in VMX abort. The VMX abort indicator will show that a machine-check event induced the abort operation.

If a machine-check event is induced by an action in VMX non-root operation before any determination is made that the inducing action may cause a VM exit, that machine-check event should be considered as happening during guest execution in VMX non-root operation. This is the case even if the part of the action that caused the machine-check event was VMX-specific (for example, the processor’s consulting an I/O bitmap). If a machine-check exception occurs and if bit 12H of the exception bitmap is cleared to 0, the exception is delivered to the guest through gate 12H of its IDT; if the bit is set to 1, the machine-check exception causes a VM exit.

NOTE

The state saved in the guest-state area on VM exits due to machine-check exceptions should be considered suspect. A VMM should consult the RIPV and EIPV bits in the IA32_MCG_STATUS MSR before resuming a guest that caused a VM exit due to a machine-check exception.

33.4.3 MCA Error Handling Guidelines for VMM

Section 33.4.2 covers general requirements for VMMs to handle machine-check exceptions, when normal operation of the guest machine and/or the VMM is no longer possible. Enhancements of machine-check architecture in newer processors may support software recovery of uncorrected MC errors (UCR) signaled through either machine-check exceptions or corrected machine-check interrupt (CMCI). Section 15.5 and Section 15.6 describes details of these more recent enhancements of machine-check architecture.

In general, Virtual Machine Monitor (VMM) error handling should follow the recommendations for OS error handling described in Section 15.3, Section 15.6, Section 15.9, and Section 15.10. This section describes additional guidelines for hosted and native hypervisor-based VMM implementations to support corrected MC errors and recoverable uncorrected MC errors.

Because a hosted VMM provides virtualization services in the context of an existing standard host OS, the host OS controls platform hardware through the host OS services such as the standard OS device drivers. In hosted VMMs, MCA errors will be handled by the host OS error handling software.

In native VMMS, the hypervisor runs on the hardware directly, and may provide only a limited set of platform services for guest VMs. Most platform services may instead be provided by a “control OS”. In hypervisor-based VMMs, MCA errors will either be delivered directly to the VMM MCA handler (when the error is signaled while in the VMM context) or cause by a VM exit from a guest VM or be delivered to the MCA intercept handler. There are two general approaches the hypervisor can use to handle the MCA error: either within the hypervisor itself or by forwarding the error to the control OS.
33.4.3.1 VMM Error Handling Strategies

Broadly speaking, there are two strategies that VMMs may take for error handling:

- **Basic error handling:** in this approach the guest VM is treated as any other thread of execution. If the error recovery action does not support restarting the thread after handling the error, the guest VM should be terminated.

- **MCA virtualization:** in this approach, the VMM virtualizes the MCA events and hardware. This enables the VMM to intercept MCA events and inject an MCA into the guest VM. The guest VM then has the opportunity to attempt error recovery actions, rather than being terminated by the VMM.

Details of these approaches and implementation considerations for hosted and native VMMs are discussed below.

33.4.3.2 Basic VMM MCA error recovery handling

The simplest approach is for the VMM to treat the guest VM as any other thread of execution:

- MCE's that occur outside the stream of execution of a virtual machine guest will cause an MCE abort and may be handled by the MCA error handler following the recovery actions and guidelines described in Section 15.9, and Section 15.10. This includes logging the error and taking appropriate recovery actions when necessary. The VMM must not resume the interrupted thread of execution or another VM until it has taken the appropriate recovery action or, in the case of fatal MCAs, reset the system.

- MCE's that occur while executing in the context of a virtual machine will be intercepted by the VMM. The MCA intercept handler may follow the error handling guidelines listed in Section 15.9 and Section 15.10 for SRAO and SRAR errors. For SRAR errors, terminating the thread of execution will involve terminating the affected guest VM. For fatal errors the MCA handler should log the error and reset the system -- the VMM should not resume execution of the interrupted VM.

33.4.3.3 Implementation Considerations for the Basic Model

For hosted VMMs, the host OS MCA error handling code will perform error analysis and initiate the appropriate recovery actions. For the basic model this flow does not change when terminating a guest VM although the specific actions needed to terminate a guest VM may be different than terminating an application or user process.

For native, hypervisor-based VMMs, MCA errors will either be delivered directly to the VMM MCA handler (when the error is signaled while in the VMM context) or cause a VM exit from a guest VM or be delivered to the MCA intercept handler. There are two general approaches the hypervisor can use to handle the MCA error: either by forwarding the error to the control OS or within the hypervisor itself. These approaches are described in the following paragraphs.

The hypervisor may forward the error to the control OS for handling errors. This approach simplifies the hypervisor error handling since it relies on the control OS to implement the basic error handling model. The control OS error handling code will be similar to the error handling code in the hosted VMM. Errors can be forwarded to the control OS via an OS callback or by injecting an MCE event into the control OS. Injecting an MCE will cause the control OS MCA error handler to be invoked. The control OS is responsible for terminating the affected guest VM, if necessary, which may require cooperation from the hypervisor.

Alternatively, the error may be handled completely in the hypervisor. The hypervisor error handler is enhanced to implement the basic error handling model and the hypervisor error handler has the capability to fully analyze the error information and take recovery actions based on the guidelines. In this case error handling steps in the hypervisor are similar to those for the hosted VMM described above (where the hypervisor replaces the host OS actions). The hypervisor is responsible for terminating the affected guest VM, if necessary.

In all cases, if a fatal error is detected the VMM error handler should log the error and reset the system. The VMM error handler must ensure that guest VMs are not resumed after a fatal error is detected to ensure error containment is maintained.

33.4.3.4 MCA Virtualization

A more sophisticated approach for handling errors is to virtualize the MCA. This involves virtualizing the MCA hardware and intercepting the MCA event in the VMM when a guest VM is interrupted by an MCA. After analyzing the
error, the VMM error handler may then decide to inject an MCE abort into the guest VM for attempted guest VM error recovery. This would enable the guest OS the opportunity to take recovery actions specific to that guest.

For MCA virtualization, the VMM must provide the guest physical address for memory errors instead of the system physical address when reporting the errors to the guest VM. To compute the guest physical address, the VMM needs to maintain a reverse mapping of system physical page addresses to guest physical page addresses.

When the MCE is injected into the guest VM, the guest OS MCA handler would be invoked. The guest OS implements the MCA handling guidelines and it could potentially terminate the interrupted thread of execution within the guest instead of terminating the VM. The guest OS may also disable use of the affected page by the guest. When disabling the page the VMM error handler may handle the case where a page is shared by the VMM and a guest or by two guests. In these cases the page use must be disabled in both contexts to ensure no subsequent consumption errors are generated.

### 33.4.3.5 Implementation Considerations for the MCA Virtualization Model

MCA virtualization may be done in either hosted VMMs or hypervisor-based VMMs. The error handling flow is similar to the flow described in the basic handling case. The major difference is that the recovery action includes injecting the MCE abort into the guest VM to enable recovery by the guest OS when the MCA interrupts the execution of a guest VM.

### 33.5 HANDLING ACTIVITY STATES BY VMM

A VMM might place a logic processor in the wait-for-SIPI activity state if supporting certain guest operating system using the multi-processor (MP) start-up algorithm. A guest with direct access to the physical local APIC and using the MP start-up algorithm sends an INIT-SIPI-SIPI IPI sequence to start the application processor. In order to trap the SIPIs, the VMM must start the logic processor which is the target of the SIPIs in wait-for-SIPI mode.
This chapter describes aspects of IA-64 and IA-32 architecture used in system management mode (SMM).

SMM provides an alternate operating environment that can be used to monitor and manage various system resources for more efficient energy usage, to control system hardware, and/or to run proprietary code. It was introduced into the IA-32 architecture in the Intel386 SL processor (a mobile specialized version of the Intel386 processor). It is also available in the Pentium M, Pentium 4, Intel Xeon, P6 family, and Pentium and Intel486 processors (beginning with the enhanced versions of the Intel486 SL and Intel486 processors).

34.1 SYSTEM MANAGEMENT MODE OVERVIEW

SMM is a special-purpose operating mode provided for handling system-wide functions like power management, system hardware control, or proprietary OEM-designed code. It is intended for use only by system firmware, not by applications software or general-purpose systems software. The main benefit of SMM is that it offers a distinct and easily isolated processor environment that operates transparently to the operating system or executive and software applications.

When SMM is invoked through a system management interrupt (SMI), the processor saves the current state of the processor (the processor’s context), then switches to a separate operating environment defined by a new address space. The system management software executive (SMI handler) starts execution in that environment, and the critical code and data of the SMI handler reside in a physical memory region (SMRAM) within that address space. While in SMM, the processor executes SMI handler code to perform operations such as powering down unused disk drives or monitors, executing proprietary code, or placing the whole system in a suspended state. When the SMI handler has completed its operations, it executes a resume (RSM) instruction. This instruction causes the processor to reload the saved context of the processor, switch back to protected or real mode, and resume executing the interrupted application or operating-system program or task.

The following SMM mechanisms make it transparent to applications programs and operating systems:

- The only way to enter SMM is by means of an SMI.
- The processor executes SMM code in a separate address space that can be made inaccessible from the other operating modes.
- Upon entering SMM, the processor saves the context of the interrupted program or task.
- All interrupts normally handled by the operating system are disabled upon entry into SMM.
- The RSM instruction can be executed only in SMM.

Section 34.3 describes transitions into and out of SMM. The execution environment after entering SMM is in real-address mode with paging disabled (CR0.PE = CR0.PG = 0). In this initial execution environment, the SMI handler can address up to 4 GBytes of memory and can execute all I/O and system instructions. Section 34.5 describes in detail the initial SMM execution environment for an SMI handler and operation within that environment. The SMI handler may subsequently switch to other operating modes while remaining in SMM.

NOTES

Software developers should be aware that, even if a logical processor was using the physical-address extension (PAE) mechanism (introduced in the P6 family processors) or was in IA-32e mode before an SMI, this will not be the case after the SMI is delivered. This is because delivery of an SMI disables paging (see Table 34-4). (This does not apply if the dual-monitor treatment of SMIs and SMM is active; see Section 34.15.)

34.1.1 System Management Mode and VMX Operation

Traditionally, SMM services system management interrupts and then resumes program execution (back to the software stack consisting of executive and application software; see Section 34.2 through Section 34.13).
A virtual machine monitor (VMM) using VMX can act as a host to multiple virtual machines and each virtual machine can support its own software stack of executive and application software. On processors that support VMX, virtual-machine extensions may use system-management interrupts (SMIs) and system-management mode (SMM) in one of two ways:

- **Default treatment.** System firmware handles SMIs. The processor saves architectural states and critical states relevant to VMX operation upon entering SMM. When the firmware completes servicing SMIs, it uses RSM to resume VMX operation.

- **Dual-monitor treatment.** Two VM monitors collaborate to control the servicing of SMIs: one VMM operates outside of SMM to provide basic virtualization in support for guests; the other VMM operates inside SMM (while in VMX operation) to support system-management functions. The former is referred to as executive monitor, the latter SMM-transfer monitor (STM).¹

The default treatment is described in Section 34.14, "Default Treatment of SMIs and SMM with VMX Operation and SMX Operation". Dual-monitor treatment of SMM is described in Section 34.15, "Dual-Monitor Treatment of SMIs and SMM".

### 34.2 SYSTEM MANAGEMENT INTERRUPT (SMI)

The only way to enter SMM is by signaling an SMI through the SMI# pin on the processor or through an SMI message received through the APIC bus. The SMI is a nonmaskable external interrupt that operates independently from the processor’s interrupt- and exception-handling mechanism and the local APIC. The SMI takes precedence over an NMI and a maskable interrupt. SMM is non-reentrant; that is, the SMI is disabled while the processor is in SMM.

**NOTES**

In the Pentium 4, Intel Xeon, and P6 family processors, when a processor that is designated as an application processor during an MP initialization sequence is waiting for a startup IPI (SIPI), it is in a mode where SMIs are masked. However if a SMI is received while an application processor is in the wait for SIPI mode, the SMI will be pended. The processor then responds on receipt of a SIPI by immediately servicing the pended SMI and going into SMM before handling the SIPI.

An SMI may be blocked for one instruction following execution of STI, MOV to SS, or POP into SS.

### 34.3 SWITCHING BETWEEN SMM AND THE OTHER PROCESSOR OPERATING MODES

Figure 2-3 shows how the processor moves between SMM and the other processor operating modes (protected, real-address, and virtual-8086). Signaling an SMI while the processor is in real-address, protected, or virtual-8086 modes always causes the processor to switch to SMM. Upon execution of the RSM instruction, the processor always returns to the mode it was in when the SMI occurred.

### 34.3.1 Entering SMM

The processor always handles an SMI on an architecturally defined “interruptible” point in program execution (which is commonly at an IA-32 architecture instruction boundary). When the processor receives an SMI, it waits for all instructions to retire and for all stores to complete. The processor then saves its current context in SMRAM (see Section 34.4), enters SMM, and begins to execute the SMI handler.

Upon entering SMM, the processor signals external hardware that SMI handling has begun. The signaling mechanism used is implementation dependent. For the P6 family processors, an SMI acknowledge transaction is gener-

¹ The dual-monitor treatment may not be supported by all processors. Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1) to determine whether it is supported.
ated on the system bus and the multiplexed status signal EXF4 is asserted each time a bus transaction is generated while the processor is in SMM. For the Pentium and Intel486 processors, the SMIACT# pin is asserted.

An SMI has a greater priority than debug exceptions and external interrupts. Thus, if an NMI, maskable hardware interrupt, or a debug exception occurs at an instruction boundary along with an SMI, only the SMI is handled. Subsequent SMI requests are not acknowledged while the processor is in SMM. The first SMI interrupt request that occurs while the processor is in SMM (that is, after SMM has been acknowledged to external hardware) is latched and serviced when the processor exits SMM with the RSM instruction. The processor will latch only one SMI while in SMM.

See Section 34.5 for a detailed description of the execution environment when in SMM.

### 34.3.2 Exiting From SMM

The only way to exit SMM is to execute the RSM instruction. The RSM instruction is only available to the SMI handler; if the processor is not in SMM, attempts to execute the RSM instruction result in an invalid-opcode exception (#UD) being generated.

The RSM instruction restores the processor’s context by loading the state save image from SMRAM back into the processor’s registers. The processor then returns an SMIACK transaction on the system bus and returns program control back to the interrupted program.

Upon successful completion of the RSM instruction, the processor signals external hardware that SMM has been exited. For the P6 family processors, an SMI acknowledge transaction is generated on the system bus and the multiplexed status signal EXF4 is no longer generated on bus cycles. For the Pentium and Intel486 processors, the SMIACT# pin is deserted.

If the processor detects invalid state information saved in the SMRAM, it enters the shutdown state and generates a special bus cycle to indicate it has entered shutdown state. Shutdown happens only in the following situations:

- A reserved bit in control register CR4 is set to 1 on a write to CR4. This error should not happen unless SMI handler code modifies reserved areas of the SMRAM saved state map (see Section 34.4.1). CR4 is saved in the state map in a reserved location and cannot be read or modified in its saved state.
- An illegal combination of bits is written to control register CR0, in particular PG set to 1 and PE set to 0, or NW set to 1 and CD set to 0.
- CR4.PCIDE would be set to 1 and IA32_EFER.LMA to 0.
- (For the Pentium and Intel486 processors only.) If the address stored in the SMBASE register when an RSM instruction is executed is not aligned on a 32-KByte boundary. This restriction does not apply to the P6 family processors.

In the shutdown state, Intel processors stop executing instructions until a RESET#, INIT# or NMI# is asserted. While Pentium family processors recognize the SMI# signal in shutdown state, P6 family and Intel486 processors do not. Intel does not support using SMI# to recover from shutdown states for any processor family; the response of processors in this circumstance is not well defined. On Pentium 4 and later processors, shutdown will inhibit INTR and A20M but will not change any of the other inhibits. On these processors, NMIs will be inhibited if no action is taken in the SMI handler to uninhibit them (see Section 34.8).

If the processor is in the HALT state when the SMI is received, the processor handles the return from SMM slightly differently (see Section 34.10). Also, the SMBASE address can be changed on a return from SMM (see Section 34.11).

### 34.4 SMRAM

Upon entering SMM, the processor switches to a new address space. Because paging is disabled upon entering SMM, this initial address space maps all memory accesses to the low 4 GBytes of the processor’s physical address space. The SMI handler’s critical code and data reside in a memory region referred to as system-management RAM (SMRAM). The processor uses a pre-defined region within SMRAM to save the processor’s pre-SMI context. SMRAM can also be used to store system management information (such as the system configuration and specific information about powered-down devices) and OEM-specific information.
The default SMRAM size is 64 KBytes beginning at a base physical address in physical memory called the SMBASE (see Figure 34-1). The SMBASE default value following a hardware reset is 30000H. The processor looks for the first instruction of the SMI handler at the address [SMBASE + 8000H]. It stores the processor’s state in the area from [SMBASE + FE00H] to [SMBASE + FFFFH]. See Section 34.4.1 for a description of the mapping of the state save area.

The system logic is minimally required to decode the physical address range for the SMRAM from [SMBASE + 8000H] to [SMBASE + FFFFH]. A larger area can be decoded if needed. The size of this SMRAM can be between 32 KBytes and 4 GBytes.

The location of the SMRAM can be changed by changing the SMBASE value (see Section 34.11). It should be noted that all processors in a multiple-processor system are initialized with the same SMBASE value (30000H). Initialization software must sequentially place each processor in SMM and change its SMBASE so that it does not overlap those of other processors.

The actual physical location of the SMRAM can be in system memory or in a separate RAM memory. The processor generates an SMI acknowledge transaction (P6 family processors) or asserts the SMIACT# pin (Pentium and Intel486 processors) when the processor receives an SMI (see Section 34.3.1).

System logic can use the SMI acknowledge transaction or the assertion of the SMIACT# pin to decode accesses to the SMRAM and redirect them (if desired) to specific SMRAM memory. If a separate RAM memory is used for SMRAM, system logic should provide a programmable method of mapping the SMRAM into system memory space when the processor is not in SMM. This mechanism will enable start-up procedures to initialize the SMRAM space (that is, load the SMI handler) before executing the SMI handler during SMM.

### 34.4.1 SMRAM State Save Map

When an IA-32 processor that does not support Intel 64 architecture initially enters SMM, it writes its state to the state save area of the SMRAM. The state save area begins at [SMBASE + 8000H + 7FFFH] and extends down to [SMBASE + 8000H + 7E00H]. Table 34-1 shows the state save map. The offset in column 1 is relative to the SMBASE value plus 8000H. Reserved spaces should not be used by software.

Some of the registers in the SMRAM state save area (marked YES in column 3) may be read and changed by the SMI handler, with the changed values restored to the processor registers by the RSM instruction. Some register images are read-only, and must not be modified (modifying these registers will result in unpredictable behavior). An SMI handler should not rely on any values stored in an area that is marked as reserved.

---

**Figure 34-1. SMRAM Usage**

| SMBASE + FFFFH | Start of State Save Area |
| SMBASE + 8000H | SMI Handler Entry Point |
| SMBASE        |                           |
The following registers are saved (but not readable) and restored upon exiting SMM:
- Control register CR4. (This register is cleared to all 0s when entering SMM).
- The hidden segment descriptor information stored in segment registers CS, DS, ES, FS, GS, and SS.

If an SMI request is issued for the purpose of powering down the processor, the values of all reserved locations in the SMM state save must be saved to nonvolatile memory.

The following state is not automatically saved and restored following an SMI and the RSM instruction, respectively:

---

### Table 34-1. SMRAM State Save Map

<table>
<thead>
<tr>
<th>Offset (Added to SMBASE + 8000H)</th>
<th>Register</th>
<th>Writable?</th>
</tr>
</thead>
<tbody>
<tr>
<td>7FFCH</td>
<td>CR0</td>
<td>No</td>
</tr>
<tr>
<td>7FF8H</td>
<td>CR3</td>
<td>No</td>
</tr>
<tr>
<td>7FF4H</td>
<td>EFLAGS</td>
<td>Yes</td>
</tr>
<tr>
<td>7FF0H</td>
<td>EIP</td>
<td>Yes</td>
</tr>
<tr>
<td>7FCCH</td>
<td>EDI</td>
<td>Yes</td>
</tr>
<tr>
<td>7FE8H</td>
<td>ESI</td>
<td>Yes</td>
</tr>
<tr>
<td>7FE4H</td>
<td>EBP</td>
<td>Yes</td>
</tr>
<tr>
<td>7FE0H</td>
<td>ESP</td>
<td>Yes</td>
</tr>
<tr>
<td>7FDCH</td>
<td>EBX</td>
<td>Yes</td>
</tr>
<tr>
<td>7FD8H</td>
<td>EDX</td>
<td>Yes</td>
</tr>
<tr>
<td>7FD4H</td>
<td>ECX</td>
<td>Yes</td>
</tr>
<tr>
<td>7DOH</td>
<td>EAX</td>
<td>Yes</td>
</tr>
<tr>
<td>7FCCH</td>
<td>DR6</td>
<td>No</td>
</tr>
<tr>
<td>7FC8H</td>
<td>DR7</td>
<td>No</td>
</tr>
<tr>
<td>7FC4H</td>
<td>TR¹</td>
<td>No</td>
</tr>
<tr>
<td>7FC0H</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>7F8CH</td>
<td>GS¹</td>
<td>No</td>
</tr>
<tr>
<td>7FB8H</td>
<td>FS¹</td>
<td>No</td>
</tr>
<tr>
<td>7F84H</td>
<td>DS¹</td>
<td>No</td>
</tr>
<tr>
<td>7FB0H</td>
<td>SS¹</td>
<td>No</td>
</tr>
<tr>
<td>7FA8H</td>
<td>CS¹</td>
<td>No</td>
</tr>
<tr>
<td>7F8AH</td>
<td>ES¹</td>
<td>No</td>
</tr>
<tr>
<td>7FA4H</td>
<td>I/O State Field, see Section 34.7</td>
<td>No</td>
</tr>
<tr>
<td>7FA0H</td>
<td>I/O Memory Address Field, see Section 34.7</td>
<td>No</td>
</tr>
<tr>
<td>7F9FH-7F03H</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>7F02H</td>
<td>Auto HALT Restart Field (Word)</td>
<td>Yes</td>
</tr>
<tr>
<td>7F00H</td>
<td>I/O Instruction Restart Field (Word)</td>
<td>Yes</td>
</tr>
<tr>
<td>7EFCH</td>
<td>SMM Revision Identifier Field (Doubleword)</td>
<td>No</td>
</tr>
<tr>
<td>7EF8H</td>
<td>SMBASE Field (Doubleword)</td>
<td>Yes</td>
</tr>
<tr>
<td>7EF7H - 7E00H</td>
<td>Reserved</td>
<td>No</td>
</tr>
</tbody>
</table>

**NOTE:**
1. The two most significant bytes are reserved.
SYSTEM MANAGEMENT MODE

- Debug registers DR0 through DR3.
- The x87 FPU registers.
- The MTRRs.
- Control register CR2.
- The model-specific registers (for the P6 family and Pentium processors) or test registers TR3 through TR7 (for the Pentium and Intel486 processors).
- The state of the trap controller.
- The machine-check architecture registers.
- The APIC internal interrupt state (ISR, IRR, etc.).
- The microcode update state.

If an SMI is used to power down the processor, a power-on reset will be required before returning to SMM, which will reset much of this state back to its default values. So an SMI handler that is going to trigger power down should first read these registers listed above directly, and save them (along with the rest of RAM) to nonvolatile storage. After the power-on reset, the continuation of the SMI handler should restore these values, along with the rest of the system's state. Anytime the SMI handler changes these registers in the processor, it must also save and restore them.

NOTES

A small subset of the MSRs (such as, the time-stamp counter and performance-monitoring counters) are not arbitrarily writable and therefore cannot be saved and restored. SMM-based power-down and restoration should only be performed with operating systems that do not use or rely on the values of these registers.

Operating system developers should be aware of this fact and insure that their operating-system assisted power-down and restoration software is immune to unexpected changes in these register values.

34.4.1.1 SMRAM State Save Map and Intel 64 Architecture

When the processor initially enters SMM, it writes its state to the state save area of the SMRAM. The state save area on an Intel 64 processor at [SMBASE + 8000H + 7FFFH] and extends to [SMBASE + 8000H + 7C00H]. Support for Intel 64 architecture is reported by CPUID.80000001:EDX[29] = 1. The layout of the SMRAM state save map is shown in Table 34-3.

Additionally, the SMRAM state save map shown in Table 34-3 also applies to processors with the following CPUID signatures listed in Table 34-2, irrespective of the value in CPUID.80000001:EDX[29].

<table>
<thead>
<tr>
<th>DisplayFamily_DisplayModel</th>
<th>Processor Families/Processor Number Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>06_17H</td>
<td>Intel Xeon Processor 5200, 5400 series, Intel Core 2 Quad processor Q9xxx, Intel Core 2 Duo processors E8000, T9000,</td>
</tr>
<tr>
<td>06_0FH</td>
<td>Intel Xeon Processor 3000, 3200, 5100, 5300, 7300 series, Intel Core 2 Quad, Intel Core 2 Extreme, Intel Core 2 Duo processors, Intel Pentium dual-core processors</td>
</tr>
<tr>
<td>06_1CH</td>
<td>45 nm Intel® Atom™ processors</td>
</tr>
</tbody>
</table>
## Table 34-3. SMRAM State Save Map for Intel 64 Architecture

<table>
<thead>
<tr>
<th>Offset (Added to SMBASE + 8000H)</th>
<th>Register</th>
<th>Writable?</th>
</tr>
</thead>
<tbody>
<tr>
<td>7FF8H</td>
<td>CR0</td>
<td>No</td>
</tr>
<tr>
<td>7FF0H</td>
<td>CR3</td>
<td>No</td>
</tr>
<tr>
<td>7FE8H</td>
<td>RFLAGS</td>
<td>Yes</td>
</tr>
<tr>
<td>7FE0H</td>
<td>IA32_EFER</td>
<td>Yes</td>
</tr>
<tr>
<td>7F08H</td>
<td>RIP</td>
<td>Yes</td>
</tr>
<tr>
<td>7F00H</td>
<td>DR6</td>
<td>No</td>
</tr>
<tr>
<td>7FC8H</td>
<td>DR7</td>
<td>No</td>
</tr>
<tr>
<td>7F4CH</td>
<td>TR SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7FC0H</td>
<td>LDTR SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7F8CH</td>
<td>GS SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7F88H</td>
<td>FS SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7FB4H</td>
<td>DS SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7F80H</td>
<td>SS SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7FA4H</td>
<td>CS SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7FA8H</td>
<td>ES SEL(^1)</td>
<td>No</td>
</tr>
<tr>
<td>7FA4H</td>
<td>IO_MISC</td>
<td>No</td>
</tr>
<tr>
<td>7F9CH</td>
<td>IO_MEM_ADDR</td>
<td>No</td>
</tr>
<tr>
<td>7F94H</td>
<td>RDI</td>
<td>Yes</td>
</tr>
<tr>
<td>7F8CH</td>
<td>RSI</td>
<td>Yes</td>
</tr>
<tr>
<td>7F84H</td>
<td>RBP</td>
<td>Yes</td>
</tr>
<tr>
<td>7F7CH</td>
<td>RSP</td>
<td>Yes</td>
</tr>
<tr>
<td>7F74H</td>
<td>RBX</td>
<td>Yes</td>
</tr>
<tr>
<td>7F6CH</td>
<td>RDX</td>
<td>Yes</td>
</tr>
<tr>
<td>7F64H</td>
<td>RCX</td>
<td>Yes</td>
</tr>
<tr>
<td>7F5CH</td>
<td>RAX</td>
<td>Yes</td>
</tr>
<tr>
<td>7F54H</td>
<td>R8</td>
<td>Yes</td>
</tr>
<tr>
<td>7F4CH</td>
<td>R9</td>
<td>Yes</td>
</tr>
<tr>
<td>7F44H</td>
<td>R10</td>
<td>Yes</td>
</tr>
<tr>
<td>7F3CH</td>
<td>R11</td>
<td>Yes</td>
</tr>
<tr>
<td>7F34H</td>
<td>R12</td>
<td>Yes</td>
</tr>
<tr>
<td>7F2CH</td>
<td>R13</td>
<td>Yes</td>
</tr>
<tr>
<td>7F24H</td>
<td>R14</td>
<td>Yes</td>
</tr>
<tr>
<td>7F1CH</td>
<td>R15</td>
<td>Yes</td>
</tr>
<tr>
<td>7F1BH-7F04H</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>7F02H</td>
<td>Auto HALT Restart Field (Word)</td>
<td>Yes</td>
</tr>
<tr>
<td>7F00H</td>
<td>I/O Instruction Restart Field (Word)</td>
<td>Yes</td>
</tr>
<tr>
<td>7F6CH</td>
<td>SMM Revision Identifier Field (Doubleword)</td>
<td>No</td>
</tr>
<tr>
<td>7EF8H</td>
<td>SMBASE Field (Doubleword)</td>
<td>Yes</td>
</tr>
</tbody>
</table>
34.4.2 SMRAM Caching

An IA-32 processor does not automatically write back and invalidate its caches before entering SMM or before exiting SMM. Because of this behavior, care must be taken in the placement of the SMRAM in system memory and in the caching of the SMRAM to prevent cache incoherence when switching back and forth between SMM and protected mode operation. Either of the following three methods of locating the SMRAM in system memory will guarantee cache coherency:

- Place the SRAM in a dedicated section of system memory that the operating system and applications are prevented from accessing. Here, the SRAM can be designated as cacheable (WB, WT, or WC) for optimum processor performance, without risking cache incoherence when entering or exiting SMM.

- Place the SRAM in a section of memory that overlaps an area used by the operating system (such as the video memory), but designate the SMRAM as uncacheable (UC). This method prevents cache access when in SMM to maintain cache coherency, but the use of uncacheable memory reduces the performance of SMM code.

- Place the SRAM in a section of system memory that overlaps an area used by the operating system and/or application code, but explicitly flush (write back and invalidate) the caches upon entering and exiting SMM mode. This method maintains cache coherency, but incurs the overhead of two complete cache flushes.

For Pentium 4, Intel Xeon, and P6 family processors, a combination of the first two methods of locating the SMRAM is recommended. Here the SMRAM is split between an overlapping and a dedicated region of memory. Upon entering SMM, the SMRAM space that is accessed overlaps video memory (typically located in low memory). This SMRAM section is designated as UC memory. The initial SMM code then jumps to a second SMRAM section that is located in a dedicated region of system memory (typically in high memory). This SMRAM section can be cached for optimum processor performance.
For systems that explicitly flush the caches upon entering SMM (the third method described above), the cache flush can be accomplished by asserting the FLUSH# pin at the same time as the request to enter SMM (generally initiated by asserting the SMI# pin). The priorities of the FLUSH# and SMI# pins are such that the FLUSH# is serviced first. To guarantee this behavior, the processor requires that the following constraints on the interaction of FLUSH# and SMI# be met. In a system where the FLUSH# and SMI# pins are synchronous and the set up and hold times are met, then the FLUSH# and SMI# pins may be asserted in the same clock. In asynchronous systems, the FLUSH# pin must be asserted at least one clock before the SMI# pin to guarantee that the FLUSH# pin is serviced first.

Upon leaving SMM (for systems that explicitly flush the caches), the WBINVD instruction should be executed prior to leaving SMM to flush the caches.

**NOTES**
In systems based on the Pentium processor that use the FLUSH# pin to write back and invalidate cache contents before entering SMM, the processor will prefetch at least one cache line in between when the Flush Acknowledge cycle is run and the subsequent recognition of SMI# and the assertion of SMIACT#.

It is the obligation of the system to ensure that these lines are not cached by returning KEN# inactive to the Pentium processor.

### 34.4.2.1 System Management Range Registers (SMRR)

SMI handler code and data stored by SMM code resides in SMRAM. The SMRR interface is an enhancement in Intel 64 architecture to limit cacheable reference of addresses in SMRAM to code running in SMM. The SMRR interface can be configured only by code running in SMM. Details of SMRR is described in Section 11.11.2.4.

### 34.5 SMI HANDLER EXECUTION ENVIRONMENT

Section 34.5.1 describes the initial execution environment for an SMI handler. An SMI handler may re-configure its execution environment to other supported operating modes. Section 34.5.2 discusses modifications an SMI handler can make to its execution environment.

#### 34.5.1 Initial SMM Execution Environment

After saving the current context of the processor, the processor initializes its core registers to the values shown in Table 34-4. Upon entering SMM, the PE and PG flags in control register CR0 are cleared, which places the processor in an environment similar to real-address mode. The differences between the SMM execution environment and the real-address mode execution environment are as follows:

- The addressable address space ranges from 0 to FFFFFFFFH (4 GBytes).
- The normal 64-KByte segment limit for real-address mode is increased to 4 GBytes.
- The default operand and address sizes are set to 16 bits, which restricts the addressable SMRAM address space to the 1-MByte real-address mode limit for native real-address-mode code. However, operand-size and address-size override prefixes can be used to access the address space beyond the 1-MByte.

#### Table 34-4. Processor Register Initialization in SMM

<table>
<thead>
<tr>
<th>Register</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>General-purpose registers</td>
<td>Undefined</td>
</tr>
<tr>
<td>EFLAGS</td>
<td>000000002H</td>
</tr>
<tr>
<td>EIP</td>
<td>00008000H</td>
</tr>
<tr>
<td>CS selector</td>
<td>SMM Base shifted right 4 bits (default 3000H)</td>
</tr>
<tr>
<td>CS base</td>
<td>SMM Base (default 30000H)</td>
</tr>
<tr>
<td>DS, ES, FS, GS, SS Selectors</td>
<td>0000H</td>
</tr>
</tbody>
</table>
SYSTEM MANAGEMENT MODE

Near jumps and calls can be made to anywhere in the 4-GByte address space if a 32-bit operand-size override prefix is used. Due to the real-address-mode style of base-address formation, a far call or jump cannot transfer control to a segment with a base address of more than 20 bits (1 MByte). However, since the segment limit in SMM is 4 GBytes, offsets into a segment that go beyond the 1-MByte limit are allowed when using 32-bit operand-size override prefixes. Any program control transfer that does not have a 32-bit operand-size override prefix truncates the EIP value to the 16 low-order bits.

Data and the stack can be located anywhere in the 4-GByte address space, but can be accessed only with a 32-bit address-size override if they are located above 1 MByte. As with the code segment, the base address for a data or stack segment cannot be more than 20 bits.

The value in segment register CS is automatically set to the default of 30000H for the SMBASE shifted 4 bits to the right; that is, 3000H. The EIP register is set to 8000H. When the EIP value is added to shifted CS value (the SMBASE), the resulting linear address points to the first instruction of the SMI handler.

The other segment registers (DS, SS, ES, FS, and GS) are cleared to 0 and their segment limits are set to 4 GBytes. In this state, the SMRAM address space may be treated as a single flat 4-GByte linear address space. If a segment register is loaded with a 16-bit value, that value is then shifted left by 4 bits and loaded into the segment base (hidden part of the segment register). The limits and attributes are not modified.

Maskable hardware interrupts, exceptions, NMI interrupts, SMI interrupts, A20M interrupts, single-step traps, breakpoint traps, and INIT operations are inhibited when the processor enters SMM. Maskable hardware interrupts, exceptions, single-step traps, and breakpoint traps can be enabled in SMM if the SMM execution environment provides and initializes an interrupt table and the necessary interrupt and exception handlers (see Section 34.6).

### Table 34-4. Processor Register Initialization in SMM

<table>
<thead>
<tr>
<th>Segment Registers</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DS, ES, FS, GS, SS Bases</td>
<td>000000000H</td>
</tr>
<tr>
<td>DS, ES, FS, GS, SS Limits</td>
<td>0FFFFFFFFH</td>
</tr>
<tr>
<td>CR0</td>
<td>PE, EM, TS, and PG flags set to 0; others unmodified</td>
</tr>
<tr>
<td>CR4</td>
<td>Cleared to zero</td>
</tr>
<tr>
<td>DR6</td>
<td>Undefined</td>
</tr>
<tr>
<td>DR7</td>
<td>00000400H</td>
</tr>
</tbody>
</table>

34.6 EXCEPTIONS AND INTERRUPTS WITHIN SMM

When the processor enters SMM, all hardware interrupts are disabled in the following manner:

```
DS, ES, FS, GS, SS Bases 000000000H
DS, ES, FS, GS, SS Limits 0FFFFFFFFH
CR0 PE, EM, TS, and PG flags set to 0; others unmodified
CR4 Cleared to zero
DR6 Undefined
DR7 00000400H
```
The IF flag in the EFLAGS register is cleared, which inhibits maskable hardware interrupts from being generated.

The TF flag in the EFLAGS register is cleared, which disables single-step traps.

Debug register DR7 is cleared, which disables breakpoint traps. (This action prevents a debugger from accidentally breaking into an SMI handler if a debug breakpoint is set in normal address space that overlays code or data in SMRAM.)

NMI, SMI, and A20M interrupts are blocked by internal SMM logic. (See Section 34.8 for more information about how NMIs are handled in SMM.)

Software-invoked interrupts and exceptions can still occur, and maskable hardware interrupts can be enabled by setting the IF flag. Intel recommends that SMM code be written in so that it does not invoke software interrupts (with the INT n, INTO, INT 3, or BOUND instructions) or generate exceptions.

If the SMI handler requires interrupt and exception handling, an SMM interrupt table and the necessary exception and interrupt handlers must be created and initialized from within SMM. Until the interrupt table is correctly initialized (using the LIDT instruction), exceptions and software interrupts will result in unpredictable processor behavior.

The following restrictions apply when designing SMM interrupt and exception-handling facilities:

- The interrupt table should be located at linear address 0 and must contain real-address mode style interrupt vectors (4 bytes containing CS and IP).
- Due to the real-address mode style of base address formation, an interrupt or exception cannot transfer control to a segment with a base address of more than 20 bits.
- An interrupt or exception cannot transfer control to a segment offset of more than 16 bits (64 KBytes).
- When an exception or interrupt occurs, only the 16 least-significant bits of the return address (EIP) are pushed onto the stack. If the offset of the interrupted procedure is greater than 64 KBytes, it is not possible for the interrupt/exception handler to return control to that procedure. (One solution to this problem is for a handler to adjust the return address on the stack.)
- The SMBASE relocation feature affects the way the processor will return from an interrupt or exception generated while the SMI handler is executing. For example, if the SMBASE is relocated to above 1 MByte, but the exception handlers are below 1 MByte, a normal return to the SMI handler is not possible. One solution is to provide the exception handler with a mechanism for calculating a return address above 1 MByte from the 16-bit return address on the stack, then use a 32-bit far call to return to the interrupted procedure.
- If an SMI handler needs access to the debug trap facilities, it must insure that an SMM accessible debug handler is available and save the current contents of debug registers DR0 through DR3 (for later restoration). Debug registers DR0 through DR3 and DR7 must then be initialized with the appropriate values.
- If an SMI handler needs access to the single-step mechanism, it must insure that an SMM accessible single-step handler is available, and then set the TF flag in the EFLAGS register.
- If the SMI design requires the processor to respond to maskable hardware interrupts or software-generated interrupts while in SMM, it must ensure that SMM accessible interrupt handlers are available and then set the IF flag in the EFLAGS register. Software interrupts are not blocked upon entry to SMM, so they do not need to be enabled.

### 34.7 MANAGING SYNCHRONOUS AND ASYNCHRONOUS SYSTEM MANAGEMENT INTERRUPTS

When coding for a multiprocessor system or a system with Intel HT Technology, it was not always possible for an SMI handler to distinguish between a synchronous SMI (triggered during an I/O instruction) and an asynchronous SMI. To facilitate the discrimination of these two events, incremental state information has been added to the SMM state save map.

Processors that have an SMM revision ID of 30004H or higher have the incremental state information described below.
34.7.1 I/O State Implementation

Within the extended SMM state save map, a bit (IO_SMI) is provided that is set only when an SMI is either taken immediately after a successful I/O instruction or is taken after a successful iteration of a REP I/O instruction (the successful notion pertains to the processor point of view; not necessarily to the corresponding platform function). When set, the IO_SMI bit provides a strong indication that the corresponding SMI was synchronous. In this case, the SMM State Save Map also supplies the port address of the I/O operation. The IO_SMI bit and the I/O Port Address may be used in conjunction with the information logged by the platform to confirm that the SMI was indeed synchronous.

The IO_SMI bit by itself is a strong indication, not a guarantee, that the SMI is synchronous. This is because an asynchronous SMI might coincidentally be taken after an I/O instruction. In such a case, the IO_SMI bit would still be set in the SMM state save map.

Information characterizing the I/O instruction is saved in two locations in the SMM State Save Map (Table 34-5). The IO_SMI bit also serves as a valid bit for the rest of the I/O information fields. The contents of these I/O information fields are not defined when the IO_SMI bit is not set.

<table>
<thead>
<tr>
<th>Table 34-5. I/O Instruction Information in the SMM State Save Map</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>State</strong> (SMM Rev. ID: 30004H or higher)</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

When IO_SMI is set, the other fields may be interpreted as follows:

- I/O length:
  - 001 – Byte
  - 010 – Word
  - 100 – Dword

- I/O instruction type (Table 34-6)

<table>
<thead>
<tr>
<th>Table 34-6. I/O Instruction Type Encodings</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Instruction</strong></td>
</tr>
<tr>
<td>IN Immediate</td>
</tr>
<tr>
<td>IN DX</td>
</tr>
<tr>
<td>OUT Immediate</td>
</tr>
<tr>
<td>OUT DX</td>
</tr>
<tr>
<td>INS</td>
</tr>
<tr>
<td>OUTS</td>
</tr>
<tr>
<td>REP INS</td>
</tr>
<tr>
<td>REP OUTS</td>
</tr>
</tbody>
</table>
34.8 NMI HANDLING WHILE IN SMM

NMI interrupts are blocked upon entry to the SMI handler. If an NMI request occurs during the SMI handler, it is latched and serviced after the processor exits SMM. Only one NMI request will be latched during the SMI handler. If an NMI request is pending when the processor executes the RSM instruction, the NMI is serviced before the next instruction of the interrupted code sequence. This assumes that NMIs were not blocked before the SMI occurred. If NMIs were blocked before the SMI occurred, they are blocked after execution of RSM.

Although NMI requests are blocked when the processor enters SMM, they may be enabled through software by executing an IRET instruction. If the SMI handler requires the use of NMI interrupts, it should invoke a dummy interrupt service routine for the purpose of executing an IRET instruction. Once an IRET instruction is executed, NMI interrupt requests are serviced in the same "real mode" manner in which they are handled outside of SMM.

A special case can occur if an SMI handler nests inside an NMI handler and then another NMI occurs. During NMI interrupt handling, NMI interrupts are disabled, so normally NMI interrupts are serviced and completed with an IRET instruction one at a time. When the processor enters SMM while executing an NMI handler, the processor saves the SMRAM state save map but does not save the attribute to keep NMI interrupts disabled. Potentially, an NMI could be latched (while in SMM or upon exit) and serviced upon exit of SMM even though the previous NMI handler has still not completed. One or more NMIs could thus be nested inside the first NMI handler. The NMI interrupt handler should take this possibility into consideration.

Also, for the Pentium processor, exceptions that invoke a trap or fault handler will enable NMI interrupts from inside of SMM. This behavior is implementation specific for the Pentium processor and is not part of the IA-32 architecture.

34.9 SMM REVISION IDENTIFIER

The SMM revision identifier field is used to indicate the version of SMM and the SMM extensions that are supported by the processor (see Figure 34-2). The SMM revision identifier is written during SMM entry and can be examined in SMRAM space at offset 7EFCH. The lower word of the SMM revision identifier refers to the version of the base SMM architecture.

![Figure 34-2. SMM Revision Identifier](image)

The upper word of the SMM revision identifier refers to the extensions available. If the I/O instruction restart flag (bit 16) is set, the processor supports the I/O instruction restart (see Section 34.12); if the SMBASE relocation flag (bit 17) is set, SMRAM base address relocation is supported (see Section 34.11).

34.10 AUTO HALT RESTART

If the processor is in a HALT state (due to the prior execution of a HLT instruction) when it receives an SMI, the processor records the fact in the auto HALT restart flag in the saved processor state (see Figure 34-3). (This flag is located at offset 7F02H and bit 0 in the state save area of the SMRAM.)

If the processor sets the auto HALT restart flag upon entering SMM (indicating that the SMI occurred when the processor was in the HALT state), the SMI handler has two options:
• It can leave the auto HALT restart flag set, which instructs the RSM instruction to return program control to the HLT instruction. This option in effect causes the processor to re-enter the HALT state after handling the SMI. (This is the default operation.)

• It can clear the auto HALT restart flag, which instructs the RSM instruction to return program control to the instruction following the HLT instruction.

![Figure 34-3. Auto HALT Restart Field](image)

These options are summarized in Table 34-7. If the processor was not in a HALT state when the SMI was received (the auto HALT restart flag is cleared), setting the flag to 1 will cause unpredictable behavior when the RSM instruction is executed.

<table>
<thead>
<tr>
<th>Value of Flag After Entry to SMM</th>
<th>Value of Flag When Exiting SMM</th>
<th>Action of Processor When Exiting SMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Returns to next instruction in interrupted program or task.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Unpredictable.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Returns to next instruction after HLT instruction.</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Returns to HALT state.</td>
</tr>
</tbody>
</table>

If the HLT instruction is restarted, the processor will generate a memory access to fetch the HLT instruction (if it is not in the internal cache), and execute a HLT bus transaction. This behavior results in multiple HLT bus transactions for the same HLT instruction.

### 34.10.1 Executing the HLT Instruction in SMM

The HLT instruction should not be executed during SMM, unless interrupts have been enabled by setting the IF flag in the EFLAGS register. If the processor is halted in SMM, the only event that can remove the processor from this state is a maskable hardware interrupt or a hardware reset.

### 34.11 SMBASE RELOCATION

The default base address for the SMRAM is 30000H. This value is contained in an internal processor register called the SMBASE register. The operating system or executive can relocate the SMRAM by setting the SMBASE field in the saved state map (at offset 7EF8H) to a new value (see Figure 34-4). The RSM instruction reloads the internal SMBASE register with the value in the SMBASE field each time it exits SMM. All subsequent SMI requests will use the new SMBASE value to find the starting address for the SMI handler (at SMBASE + 8000H) and the SMRAM state save area (from SMBASE + FE00H to SMBASE + FFFFH). (The processor resets the value in its internal SMBASE register to 30000H on a RESET, but does not change it on an INIT.)
In multiple-processor systems, initialization software must adjust the SMBASE value for each processor so that the SMRAM state save areas for each processor do not overlap. (For Pentium and Intel486 processors, the SMBASE values must be aligned on a 32-KByte boundary or the processor will enter shutdown state during the execution of a RSM instruction.)

If the SMBASE relocation flag in the SMM revision identifier field is set, it indicates the ability to relocate the SMBASE (see Section 34.9).

### 34.12 I/O INSTRUCTION RESTART

If the I/O instruction restart flag in the SMM revision identifier field is set (see Section 34.9), the I/O instruction restart mechanism is present on the processor. This mechanism allows an interrupted I/O instruction to be re-executed upon returning from SMM mode. For example, if an I/O instruction is used to access a powered-down I/O device, a chip set supporting this device can intercept the access and respond by asserting SMI#. This action invokes the SMI handler to power-up the device. Upon returning from the SMI handler, the I/O instruction restart mechanism can be used to re-execute the I/O instruction that caused the SMI.

The I/O instruction restart field (at offset 7F00H in the SMM state-save area, see Figure 34-5) controls I/O instruction restart. When an RSM instruction is executed, if this field contains the value FFH, then the EIP register is modified to point to the I/O instruction that received the SMI request. The processor will then automatically re-execute the I/O instruction that the SMI trapped. (The processor saves the necessary machine state to insure that re-execution of the instruction is handled coherently.)

If the I/O instruction restart field contains the value 00H when the RSM instruction is executed, then the processor begins program execution with the instruction following the I/O instruction. (When a repeat prefix is being used, the next instruction may be the next I/O instruction in the repeat loop.) Not re-executing the interrupted I/O instruction is the default behavior; the processor automatically initializes the I/O instruction restart field to 00H upon entering SMM. Table 34-8 summarizes the states of the I/O instruction restart field.

<table>
<thead>
<tr>
<th>Value of Flag After Entry to SMM</th>
<th>Value of Flag When Exiting SMM</th>
<th>Action of Processor When Exiting SMM</th>
</tr>
</thead>
<tbody>
<tr>
<td>00H</td>
<td>00H</td>
<td>Does not re-execute trapped I/O instruction.</td>
</tr>
<tr>
<td>00H</td>
<td>FFH</td>
<td>Re-executes trapped I/O instruction.</td>
</tr>
</tbody>
</table>

The I/O instruction restart mechanism does not indicate the cause of the SMI. It is the responsibility of the SMI handler to examine the state of the processor to determine the cause of the SMI and to determine if an I/O instruction was interrupted and should be restarted upon exiting SMM. If an SMI interrupt is signaled on a non-I/O instruction boundary, setting the I/O instruction restart field to FFH prior to executing the RSM instruction will likely result in a program error.
34.12.1 Back-to-Back SMI Interrupts When I/O Instruction Restart Is Being Used

If an SMI interrupt is signaled while the processor is servicing an SMI interrupt that occurred on an I/O instruction boundary, the processor will service the new SMI request before restarting the originally interrupted I/O instruction. If the I/O instruction restart field is set to FFH prior to returning from the second SMI handler, the EIP will point to an address different from the originally interrupted I/O instruction, which will likely lead to a program error. To avoid this situation, the SMI handler must be able to recognize the occurrence of back-to-back SMI interrupts when I/O instruction restart is being used and insure that the handler sets the I/O instruction restart field to 00H prior to returning from the second invocation of the SMI handler.

34.13 SMM MULTIPLE-PROCESSOR CONSIDERATIONS

The following should be noted when designing multiple-processor systems:

- Any processor in a multiprocessor system can respond to an SMM.
- Each processor needs its own SMRAM space. This space can be in system memory or in a separate RAM.
- The SMRAMs for different processors can be overlapped in the same memory space. The only stipulation is that each processor needs its own state save area and its own dynamic data storage area. (Also, for the Pentium and Intel486 processors, the SMBASE address must be located on a 32-KByte boundary.) Code and static data can be shared among processors. Overlapping SMRAM spaces can be done more efficiently with the P6 family processors because they do not require that the SMBASE address be on a 32-KByte boundary.
- The SMI handler will need to initialize the SMBASE for each processor.
- Processors can respond to local SMIs through their SMI# pins or to SMIs received through the APIC interface. The APIC interface can distribute SMIs to different processors.
- Two or more processors can be executing in SMM at the same time.
- When operating Pentium processors in dual processing (DP) mode, the SMIACT# pin is driven only by the MRM processor and should be sampled with ADS#. For additional details, see Chapter 14 of the Pentium Processor Family User’s Manual, Volume 1.

SMM is not re-entrant, because the SMRAM State Save Map is fixed relative to the SMBASE. If there is a need to support two or more processors in SMM mode at the same time then each processor should have dedicated SMRAM spaces. This can be done by using the SMBASE Relocation feature (see Section 34.11).

34.14 DEFAULT TREATMENT OF SMIS AND SMM WITH VMX OPERATION AND SMX OPERATION

Under the default treatment, the interactions of SMIs and SMM with VMX operation are few. This section details those interactions. It also explains how this treatment affects SMX operation.

34.14.1 Default Treatment of SMI Delivery

Ordinary SMI delivery saves processor state into SMRAM and then loads state based on architectural definitions. Under the default treatment, processors that support VMX operation perform SMI delivery as follows:

```
enter SMM;
save the following internal to the processor:
    CR4.VMXE
    an indication of whether the logical processor was in VMX operation (root or non-root)
IF the logical processor is in VMX operation
    THEN
        save current VMCS pointer internal to the processor;
        leave VMX operation;
        save VMX-critical state defined below;
```
If the logical processor supports SMX operation

THEN

save internal to the logical processor an indication of whether the Intel® TXT private space is locked;

IF the TXT private space is unlocked

THEN lock the TXT private space;

FI;

FI;

CR4.VMXE ← 0;

perform ordinary SMI delivery:

save processor state in SMRAM;

set processor state to standard SMM values;

invalidate linear mappings and combined mappings associated with VPID 0000H (for all PCIDs); combined mappings for VPID 0000H are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP; see Section 28.3);

The pseudocode above makes reference to the saving of VMX-critical state. This state consists of the following:

1. SS.DPL (the current privilege level); 
2. RFLAGS.VM;
3. the state of blocking by STI and by MOV SS (see Table 24-3 in Section 24.4.2); 
4. the state of virtual-NMI blocking (only if the processor is in VMX non-root operation and the "virtual NMIs" VM-execution control is 1); and
5. an indication of whether an MTF VM exit is pending (see Section 25.5.2). These data may be saved internal to the processor or in the VMCS region of the current VMCS. Processors that do not support SMI recognition while there is blocking by STI or by MOV SS need not save the state of such blocking.

If the logical processor supports the 1-setting of the "enable EPT" VM-execution control and the logical processor was in VMX non-root operation at the time of an SMI, it saves the value of that control into bit 0 of the 32-bit field at offset SMBASE + 8000H + 7EE0H (SMBASE + FEE0H; see Table 34-3). If the logical processor was not in VMX non-root operation at the time of the SMI, it saves 0 into that bit. If the logical processor saves 1 into that bit (it was in VMX non-root operation and the "enable EPT" VM-execution control was 1), it saves the value of the EPT pointer (EPTP) into the 64-bit field at offset SMBASE + 8000H + 7ED8H (SMBASE + FED8H).

Because SMI delivery causes a logical processor to leave VMX operation, all the controls associated with VMX non-root operation are disabled in SMM and thus cannot cause VM exits while the logical processor in SMM.

### 34.14.2 Default Treatment of RSM

Ordinary execution of RSM restores processor state from SMRAM. Under the default treatment, processors that support VMX operation perform RSM as follows:

IF VMXE = 1 in CR4 image in SMRAM

THEN fail and enter shutdown state;

ELSE

restore state normally from SMRAM;

invalidate linear mappings and combined mappings associated with all VPIIDs and all PCIDs; combined mappings are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP; see Section 28.3);

IF the logical processor supports SMX operation and the Intel® TXT private space was unlocked at the time of the last SMI (as saved)

THEN unlock the TXT private space;

FI;

CR4.VMXE ← value stored internally;

---

1. This causes the logical processor to block INIT signals, NMIs, and SMIs.

2. Section 34.14 and Section 34.15 use the notation RAX, RIP, RSP, RFLAGS, etc. for processor registers because most processors that support VMX operation also support Intel 64 architecture. For processors that do not support Intel 64 architecture, this notation refers to the 32-bit forms of these registers (EAX, EIP, ESP, EFLAGS, etc.). In a few places, notation such as EAX is used to refer specifically to the lower 32 bits of the register.

3. "Enable EPT" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, SMI functions as the "enable EPT" VM-execution control were 0. See Section 24.6.2.
IF internal storage indicates that the logical processor had been in VMX operation (root or non-root)  
THEN  
enter VMX operation (root or non-root);  
restore VMX-critical state as defined in Section 34.14.1;  
set to their fixed values any bits in CR0 and CR4 whose values must be fixed in VMX operation (see Section 23.8):  
IF RFLAGS.VM = 0 AND (in VMX root operation OR the "unrestricted guest" VM-execution control is 0)  
THEN  
CS.RPL ← SS.DPL;  
SS.RPL ← SS.DPL;  
FI;  
restore current VMCS pointer;  
FI;  
leave SMM;  
IF logical processor will be in VMX operation or in SMX operation after RSM  
THEN block A20M and leave A20M mode;  
FI;  
FI;  
RSM unblocks SMIs. It restores the state of blocking by NMI (see Table 24-3 in Section 24.4.2) as follows:  
• If the RSM is not to VMX non-root operation or if the “virtual NMIs” VM-execution control will be 0, the state of NMI blocking is restored normally.  
• If the RSM is to VMX non-root operation and the “virtual NMIs” VM-execution control will be 1, NMIs are not blocked after RSM. The state of virtual-NMI blocking is restored as part of VMX-critical state.  
INIT signals are blocked after RSM if and only if the logical processor will be in VMX root operation.  
If RSM returns a logical processor to VMX non-root operation, it re-establishes the controls associated with the current VMCS. If the “interrupt-window exiting” VM-execution control is 1, a VM exit occurs immediately after RSM if the enabling conditions apply. The same is true for the “NMI-window exiting” VM-execution control. Such VM exits occur with their normal priority. See Section 25.2.  
If an MTF VM exit was pending at the time of the previous SMI, an MTF VM exit is pending on the instruction boundary following execution of RSM. The following items detail the treatment of MTF VM exits that may be pending following RSM:  
• System-management interrupts (SMIs), INIT signals, and higher priority events take priority over these MTF VM exits. These MTF VM exits take priority over debug-trap exceptions and lower priority events.  
• These MTF VM exits wake the logical processor if RSM caused the logical processor to enter the HLT state (see Section 34.10). They do not occur if the logical processor just entered the shutdown state.  

34.14.3 Protection of CR4.VMXE in SMM

Under the default treatment, CR4.VMXE is treated as a reserved bit while a logical processor is in SMM. Any attempt by software running in SMM to set this bit causes a general-protection exception. In addition, software cannot use VMX instructions or enter VMX operation while in SMM.

34.14.4 VMXOFF and SMI Unblocking

The VMXOFF instruction can be executed only with the default treatment (see Section 34.15.1) and only outside SMM. If SMIs are blocked when VMXOFF is executed, VMXOFF unblocks them unless

1. If the RSM is to VMX non-root operation and both the "unrestricted guest" VM-execution control and bit 31 of the primary processor-based VM-execution controls will be 1, CR0.PE and CR0.PG retain the values that were loaded from SMRAM regardless of what is reported in the capability MSR IA32_VMX_CR0_FIXED0.

2. "Unrestricted guest" is a secondary processor-based VM-execution control. If bit 31 of the primary processor-based VM-execution controls is 0, VM entry functions as if the "unrestricted guest" VM-execution control were 0. See Section 24.6.2.
IA32_SMM_MONITOR_CTL[bit 2] is 1 (see Section 34.15.5 for details regarding this MSR). Section 34.15.7 identifies a case in which SMIs may be blocked when VMXOFF is executed.

Not all processors allow this bit to be set to 1. Software should consult the VMX capability MSR IA32_VMX_MISC (see Appendix A.6) to determine whether this is allowed.

### 34.15 DUAL-MONITOR TREATMENT OF SMIs AND SMM

Dual-monitor treatment is activated through the cooperation of the **executive monitor** (the VMM that operates outside of SMM to provide basic virtualization) and the **SMM-transfer monitor (STM)**; the VMM that operates inside SMM—while in VMX operation—to support system-management functions. Control is transferred to the STM through VM exits; VM entries are used to return from SMM.

The dual-monitor treatment may not be supported by all processors. Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1) to determine whether it is supported.

#### 34.15.1 Dual-Monitor Treatment Overview

The dual-monitor treatment uses an executive monitor and an SMM-transfer monitor (STM). Transitions from the executive monitor or its guests to the STM are called **SMM VM exits** and are discussed in Section 34.15.2. SMM VM exits are caused by SMIs as well as executions of VMCALL in VMX root operation. The latter allow the executive monitor to call the STM for service.

The STM runs in VMX root operation and uses VMX instructions to establish a VMCS and perform VM entries to its own guests. This is done all inside SMM (see Section 34.15.3). The STM returns from SMM, not by using the RSM instruction, but by using a VM entry that returns from SMM. Such VM entries are described in Section 34.15.4.

Initially, there is no STM and the default treatment (Section 34.14) is used. The dual-monitor treatment is not used until it is enabled and activated. The steps to do this are described in Section 34.15.5 and Section 34.15.6.

It is not possible to leave VMX operation under the dual-monitor treatment; VMXOFF will fail if executed. The dual-monitor treatment must be deactivated first. The STM deactivates dual-monitor treatment using a VM entry that returns from SMM with the “deactivate dual-monitor treatment” VM-entry control set to 1 (see Section 34.15.7).

The executive monitor configures any VMCS that it uses for VM exits to the executive monitor. SMM VM exits, which transfer control to the STM, use a different VMCS. Under the dual-monitor treatment, each logical processor uses a separate VMCS called the **SMM-transfer VMCS**. When the dual-monitor treatment is active, the logical processor maintains another VMCS pointer called the **SMM-transfer VMCS pointer**. The SMM-transfer VMCS pointer is established when the dual-monitor treatment is activated.

#### 34.15.2 SMM VM Exits

An SMM VM exit is a VM exit that begins outside SMM and that ends in SMM.

Unlike other VM exits, SMM VM exits can begin in VMX root operation. SMM VM exits result from the arrival of an SMI outside SMM or from execution of VMCALL in VMX root operation outside SMM. Execution of VMCALL in VMX root operation causes an SMM VM exit only if the valid bit is set in the IA32_SMM_MONITOR_CTL MSR (see Section 34.15.5).

Execution of VMCALL in VMX root operation causes an SMM VM exit even under the default treatment. This SMM VM exit activates the dual-monitor treatment (see Section 34.15.6).

Differences between SMM VM exits and other VM exits are detailed in Sections 34.15.2.1 through 34.15.2.5. Differences between SMM VM exits that activate the dual-monitor treatment and other SMM VM exits are described in Section 34.15.6.

1. Setting IA32_SMM_MONITOR_CTL[bit 2] to 1 prevents VMXOFF from unblocking SMIs regardless of the value of the register’s valid bit (bit 0).
### 34.15.2.1 Architectural State Before a VM Exit

System-management interrupts (SMIs) that cause SMM VM exits always do so directly. They do not save state to SMRAM as they do under the default treatment.

### 34.15.2.2 Updating the Current-VMCS and Executive-VMCS Pointers

SMM VM exits begin by performing the following steps:

1. The executive-VMCS pointer field in the SMM-transfer VMCS is loaded as follows:
   - If the SMM VM exit commenced in VMX non-root operation, it receives the current-VMCS pointer.
   - If the SMM VM exit commenced in VMX root operation, it receives the VMXON pointer.

2. The current-VMCS pointer is loaded with the value of the SMM-transfer VMCS pointer.

The last step ensures that the current VMCS is the SMM-transfer VMCS. VM-exit information is recorded in that VMCS, and VM-entry control fields in that VMCS are updated. State is saved into the guest-state area of that VMCS. The VM-exit controls and host-state area of that VMCS determine how the VM exit operates.

### 34.15.2.3 Recording VM-Exit Information

SMM VM exits differ from other VM exit with regard to the way they record VM-exit information. The differences follow.

- **Exit reason.**
  - Bits 15:0 of this field contain the basic exit reason. The field is loaded with the reason for the SMM VM exit: I/O SMI (an SMI arrived immediately after retirement of an I/O instruction), other SMI, or VMCALL. See Appendix C, "VMX Basic Exit Reasons".
  - SMM VM exits are the only VM exits that may occur in VMX root operation. Because the SMM-transfer monitor may need to know whether it was invoked from VMX root or VMX non-root operation, this information is stored in bit 29 of the exit-reason field (see Table 24-14 in Section 24.9.1). The bit is set by SMM VM exits from VMX root operation.
  - If the SMM VM exit occurred in VMX non-root operation and an MTF VM exit was pending, bit 28 of the exit-reason field is set; otherwise, it is cleared.
  - Bits 27:16 and bits 31:30 are cleared.

- **Exit qualification.** For an SMM VM exit due an SMI that arrives immediately after the retirement of an I/O instruction, the exit qualification contains information about the I/O instruction that retired immediately before the SMI. It has the format given in Table 34-9.

#### Table 34-9. Exit Qualification for SMIs That Arrive Immediately After the Retirement of an I/O Instruction

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
</table>
| 2:0             | Size of access:  
|                 | 0 = 1-byte  
|                 | 1 = 2-byte  
|                 | 3 = 4-byte  
|                 | Other values not used. |
| 3               | Direction of the attempted access (0 = OUT, 1 = IN) |
| 4               | String instruction (0 = not string; 1 = string) |
| 5               | REP prefixed (0 = not REP; 1 = REP) |
| 6               | Operand encoding (0 = DX, 1 = immediate) |
• **Guest linear address.** This field is used for VM exits due to SMIs that arrive immediately after the retirement of an INS or OUTS instruction for which the relevant segment (ES for INS; DS for OUTS unless overridden by an instruction prefix) is usable. The field receives the value of the linear address generated by ES:(E)DI (for INS) or segment:(E)SI (for OUTS; the default segment is DS but can be overridden by a segment override prefix) at the time the instruction started. If the relevant segment is not usable, the value is undefined. On processors that support Intel 64 architecture, bits 63:32 are clear if the logical processor was not in 64-bit mode before the VM exit.

• **I/O RCX, I/O RSI, I/O RDI, and I/O RIP.** For an SMM VM exit due an SMI that arrives immediately after the retirement of an I/O instruction, these fields receive the values that were in RCX, RSI, RDI, and RIP, respectively, before the I/O instruction executed. Thus, the value saved for I/O RIP addresses the I/O instruction.

### 34.15.2.4 Saving Guest State

SMM VM exits save the contents of the SMBASE register into the corresponding field in the guest-state area. The value of the VMX-preemption timer is saved into the corresponding field in the guest-state area if the "save VMX-preemption timer value" VM-exit control is 1. That field becomes undefined if, in addition, either the SMM VM exit is from VMX root operation or the SMM VM exit is from VMX non-root operation and the "activate VMX-preemption timer" VM-execution control is 0.

### 34.15.2.5 Updating Non-Register State

SMM VM exits affect the non-register state of a logical processor as follows:

- SMM VM exits cause non-maskable interrupts (NMI) to be blocked; they may be unblocked through execution of IRET or through a VM entry (depending on the value loaded for the interruptibility state and the setting of the "virtual NMI" VM-execution control).

- SMM VM exits cause SMIs to be blocked; they may be unblocked by a VM entry that returns from SMM (see Section 34.15.4).

SMM VM exits invalidate linear mappings and combined mappings associated with VPID 0000H for all PCIDs. Combined mappings for VPID 0000H are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP; see Section 28.3). (Ordinary VM exits are not required to perform such invalidation if the "enable VPID" VM-execution control is 1; see Section 27.5.5.)

### 34.15.3 Operation of the SMM-Transfer Monitor

Once invoked, the SMM-transfer monitor (STM) is in VMX root operation and can use VMX instructions to configure VMCSs and to cause VM entries to virtual machines supported by those structures. As noted in Section 34.15.1, the VMXOFF instruction cannot be used under the dual-monitor treatment and thus cannot be used by the STM.

The RSM instruction also cannot be used under the dual-monitor treatment. As noted in Section 25.1.3, it causes a VM exit if executed in SMM in VMX non-root operation. If executed in VMX root operation, it causes an invalid-opcode exception. The STM uses VM entries to return from SMM (see Section 34.15.4).

### Table 34-9. Exit Qualification for SMIs That Arrive Immediately After the Retirement of an I/O Instruction (Contd.)

<table>
<thead>
<tr>
<th>Bit Position(s)</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>15:7</td>
<td>Reserved (cleared to 0)</td>
</tr>
<tr>
<td>31:16</td>
<td>Port number (as specified in the I/O instruction)</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved (cleared to 0). These bits exist only on processors that support Intel 64 architecture.</td>
</tr>
</tbody>
</table>
34.15.4 VM Entries that Return from SMM

The SMM-transfer monitor (STM) returns from SMM using a VM entry with the “entry to SMM” VM-entry control clear. VM entries that return from SMM reverse the effects of an SMM VM exit (see Section 34.15.2). VM entries that return from SMM may differ from other VM entries in that they do not necessarily enter VMX non-root operation. If the executive-VMCS pointer field in the current VMCS contains the VMXON pointer, the logical processor remains in VMX root operation after VM entry.

For differences between VM entries that return from SMM and other VM entries see Sections 34.15.4.1 through 34.15.4.10.

34.15.4.1 Checks on the Executive-VMCS Pointer Field

VM entries that return from SMM perform the following checks on the executive-VMCS pointer field in the current VMCS:

- Bits 11:0 must be 0.
- The pointer must not set any bits beyond the processor’s physical-address width.1,2
- The 32 bits located in memory referenced by the physical address in the pointer must contain the processor’s VMCS revision identifier (see Section 24.2).

The checks above are performed before the checks described in Section 34.15.4.2 and before any of the following checks:

- If the “deactivate dual-monitor treatment” VM-entry control is 0 and the executive-VMCS pointer field does not contain the VMXON pointer, the launch state of the executive VMCS (the VMCS referenced by the executive-VMCS pointer field) must be launched (see Section 24.11.3).
- If the “deactivate dual-monitor treatment” VM-entry control is 1, the executive-VMCS pointer field must contain the VMXON pointer (see Section 34.15.7).3

34.15.4.2 Checks on VM-Execution Control Fields

VM entries that return from SMM differ from other VM entries with regard to the checks performed on the VM-execution control fields specified in Section 26.2.1.1. They do not apply the checks to the current VMCS. Instead, VM-entry behavior depends on whether the executive-VMCS pointer field contains the VMXON pointer:

- If the executive-VMCS pointer field contains the VMXON pointer (the VM entry remains in VMX root operation), the checks are not performed at all.
- If the executive-VMCS pointer field does not contain the VMXON pointer (the VM entry enters VMX non-root operation), the checks are performed on the VM-execution control fields in the executive VMCS (the VMCS referenced by the executive-VMCS pointer field in the current VMCS). These checks are performed after checking the executive-VMCS pointer field itself (for proper alignment).

Other VM entries ensure that, if “activate VMX-preemption timer” VM-execution control is 0, the “save VMX-preemption timer value” VM-exit control is also 0. This check is not performed by VM entries that return from SMM.

34.15.4.3 Checks on VM-Entry Control Fields

VM entries that return from SMM differ from other VM entries with regard to the checks performed on the VM-entry control fields specified in Section 26.2.1.3.

Specifically, if the executive-VMCS pointer field contains the VMXON pointer (the VM entry remains in VMX root operation), the following must not all hold for the VM-entry interruption-information field:

---

1. Software can determine a processor’s physical-address width by executing CPUID with 80000008H in EAX. The physical-address width is returned in bits 7:0 of EAX.
2. If IA32_VMX_BASIC[48] is read as 1, this pointer must not set any bits in the range 63:32; see Appendix A.1.
3. The STM can determine the VMXON pointer by reading the executive-VMCS pointer field in the current VMCS after the SMM VM exit that activates the dual-monitor treatment.
• the valid bit (bit 31) in the VM-entry interruption-information field is 1
• the interruption type (bits 10:8) is not 7 (other event); and
• the vector (bits 7:0) is not 0 (pending MTF VM exit).

34.15.4.4 Checks on the Guest State Area

Section 26.3.1 specifies checks performed on fields in the guest-state area of the VMCS. Some of these checks are conditioned on the settings of certain VM-execution controls (e.g., “virtual NMIs” or “unrestricted guest”). VM entries that return from SMM modify these checks based on whether the executive-VMCS pointer field contains the VMXON pointer:

• If the executive-VMCS pointer field contains the VMXON pointer (the VM entry remains in VMX root operation), the checks are performed as all relevant VM-execution controls were 0. (As a result, some checks may not be performed at all.)

• If the executive-VMCS pointer field does not contain the VMXON pointer (the VM entry enters VMX non-root operation), this check is performed based on the settings of the VM-execution controls in the executive VMCS (the VMCS referenced by the executive-VMCS pointer field in the current VMCS).

For VM entries that return from SMM, the activity-state field must not indicate the wait-for-SIPI state if the executive-VMCS pointer field contains the VMXON pointer (the VM entry is to VMX root operation).

34.15.4.5 Loading Guest State

VM entries that return from SMM load the SMBASE register from the SMBASE field. VM entries that return from SMM invalidate linear mappings and combined mappings associated with all VPIIDs. Combined mappings are invalidated for all EP4TA values (EP4TA is the value of bits 51:12 of EPTP; see Section 28.3). (Ordinary VM entries are required to perform such invalidation only for VPID 0000H and are not required to do even that if the “enable VPID” VM-execution control is 1; see Section 26.3.2.5.)

34.15.4.6 VMX-Preemption Timer

A VM entry that returns from SMM activates the VMX-preemption timer only if the executive-VMCS pointer field does not contain the VMXON pointer (the VM entry enters VMX non-root operation) and the “activate VMX-preemption timer” VM-execution control is 1 in the executive VMCS (the VMCS referenced by the executive-VMCS pointer field). In this case, VM entry starts the VMX-preemption timer with the value in the VMX-preemption timer-value field in the current VMCS.

34.15.4.7 Updating the Current-VMCS and SMM-Transfer VMCS Pointers

Successful VM entries (returning from SMM) load the SMM-transfer VMCS pointer with the current-VMCS pointer. Following this, they load the current-VMCS pointer from a field in the current VMCS:

• If the executive-VMCS pointer field contains the VMXON pointer (the VM entry remains in VMX root operation), the current-VMCS pointer is loaded from the VMCS-link pointer field.

• If the executive-VMCS pointer field does not contain the VMXON pointer (the VM entry enters VMX non-root operation), the current-VMCS pointer is loaded with the value of the executive-VMCS pointer field.

If the VM entry successfully enters VMX non-root operation, the VM-execution controls in effect after the VM entry are those from the new current VMCS. This includes any structures external to the VMCS referenced by VM-execution control fields.

The updating of these VMCS pointers occurs before event injection. Event injection is determined, however, by the VM-entry control fields in the VMCS that was current when the VM entry commenced.

1. The STM can determine the VMXON pointer by reading the executive-VMCS pointer field in the current VMCS after the SMM VM exit that activates the dual-monitor treatment.
34.15.4.8 VM Exits Induced by VM Entry
Section 26.5.1.2 describes how the event-delivery process invoked by event injection may lead to a VM exit. Section 26.6.3 to Section 26.6.7 describe other situations that may cause a VM exit to occur immediately after a VM entry.

Whether these VM exits occur is determined by the VM-execution control fields in the current VMCS. For VM entries that return from SMM, they can occur only if the executive-VMCS pointer field does not contain the VMXON pointer (the VM entry enters VMX non-root operation).

In this case, determination is based on the VM-execution control fields in the VMCS that is current after the VM entry. This is the VMCS referenced by the value of the executive-VMCS pointer field at the time of the VM entry (see Section 34.15.4.7). This VMCS also controls the delivery of such VM exits. Thus, VM exits induced by a VM entry returning from SMM are to the executive monitor and not to the STM.

34.15.4.9 SMI Blocking
VM entries that return from SMM determine the blocking of system-management interrupts (SMIs) as follows:

- If the “deactivate dual-monitor treatment” VM-entry control is 0, SMIs are blocked after VM entry if and only if the bit 2 in the interruptibility-state field is 1.
- If the “deactivate dual-monitor treatment” VM-entry control is 1, the blocking of SMIs depends on whether the logical processor is in SMX operation:
  - If the logical processor is in SMX operation, SMIs are blocked after VM entry.
  - If the logical processor is outside SMX operation, SMIs are unblocked after VM entry.

VM entries that return from SMM and that do not deactivate the dual-monitor treatment may leave SMIs blocked. This feature exists to allow the STM to invoke functionality outside of SMM without unblocking SMIs.

34.15.4.10 Failures of VM Entries That Return from SMM
Section 26.7 describes the treatment of VM entries that fail during or after loading guest state. Such failures record information in the VM-exit information fields and load processor state as would be done on a VM exit. The VMCS used is the one that was current before the VM entry commenced. Control is thus transferred to the STM and the logical processor remains in SMM.

34.15.5 Enabling the Dual-Monitor Treatment
Code and data for the SMM-transfer monitor (STM) reside in a region of SMRAM called the monitor segment (MSEG). Code running in SMM determines the location of MSEG and establishes its content. This code is also responsible for enabling the dual-monitor treatment.

SMM code enables the dual-monitor treatment and specifies the location of MSEG by writing to the IA32_SMM_MONITOR_CTL MSR (index 9BH). The MSR has the following format:

- Bit 0 is the register’s valid bit. The STM may be invoked using VMCALL only if this bit is 1. Because VMCALL is used to activate the dual-monitor treatment (see Section 34.15.6), the dual-monitor treatment cannot be activated if the bit is 0. This bit is cleared when the logical processor is reset.
- Bit 1 is reserved.
- Bit 2 determines whether executions of VMXOFF unblock SMIs under the default treatment of SMIs and SMM. Executions of VMXOFF unblock SMIs unless bit 2 is 1 (the value of bit 0 is irrelevant). See Section 34.14.4. Certain leaf functions of the GETSEC instruction clear this bit (see Chapter 5, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2C).

1. A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
• Bits 11:3 are reserved.
• Bits 31:12 contain a value that, when shifted right 12 bits, is the physical address of MSEG (the MSEG base address).
• Bits 63:32 are reserved.

The following items detail use of this MSR:
• The IA32_SMM_MONITOR_CTL MSR is supported only on processors that support the dual-monitor treatment.1 On other processors, accesses to the MSR using RDMSR or WRMSR generate a general-protection fault (#GP(0)).
• A write to the IA32_SMM_MONITOR_CTL MSR using WRMSR generates a general-protection fault (#GP(0)) if executed outside of SMM or if an attempt is made to set any reserved bit. An attempt to write to the IA32_SMM_MONITOR_CTL MSR fails if made as part of a VM exit that does not end in SMM or part of a VM entry that does not begin in SMM.
• Reads from the IA32_SMM_MONITOR_CTL MSR using RDMSR are allowed any time RDMSR is allowed. The MSR may be read as part of any VM exit.
• The dual-monitor treatment can be activated only if the valid bit in the MSR is set to 1.

The 32 bytes located at the MSEG base address are called the **MSEG header**. The format of the MSEG header is given in Table 34-10 (each field is 32 bits).

**Table 34-10. Format of MSEG Header**

<table>
<thead>
<tr>
<th>Byte Offset</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>MSEG-header revision identifier</td>
</tr>
<tr>
<td>4</td>
<td>SMM-transfer monitor features</td>
</tr>
<tr>
<td>8</td>
<td>GDTR limit</td>
</tr>
<tr>
<td>12</td>
<td>GDTR base offset</td>
</tr>
<tr>
<td>16</td>
<td>CS selector</td>
</tr>
<tr>
<td>20</td>
<td>EIP offset</td>
</tr>
<tr>
<td>24</td>
<td>ESP offset</td>
</tr>
<tr>
<td>28</td>
<td>CR3 offset</td>
</tr>
</tbody>
</table>

To ensure proper behavior in VMX operation, software should maintain the MSEG header in writeback cacheable memory. Future implementations may allow or require a different memory type.2 Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1).

SMM code should enable the dual-monitor treatment (by setting the valid bit in IA32_SMM_MONITOR_CTL MSR) only after establishing the content of the MSEG header as follows:
• Bytes 3:0 contain the **MSEG revision identifier**. Different processors may use different MSEG revision identifiers. These identifiers enable software to avoid using an MSEG header formatted for one processor on a processor that uses a different format. Software can discover the MSEG revision identifier that a processor uses by reading the VMX capability MSR IA32_VMX_MISC (see Appendix A.6).

---

1. Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1) to determine whether the dual-monitor treatment is supported.
2. Alternatively, software may map the MSEG header with the UC memory type; this may be necessary, depending on how memory is organized. Doing so is strongly discouraged unless necessary as it will cause the performance of transitions using those structures to suffer significantly. In addition, the processor will continue to use the memory type reported in the VMX capability MSR IA32_VMX_BASIC with exceptions noted in Appendix A.1.
• Bytes 7:4 contain the **SMM-transfer monitor features** field. Bits 31:1 of this field are reserved and must be zero. Bit 0 of the field is the **IA-32e mode SMM feature bit**. It indicates whether the logical processor will be in IA-32e mode after the STM is activated (see Section 34.15.6).

• Bytes 31:8 contain fields that determine how processor state is loaded when the STM is activated (see Section 34.15.6.6). SMM code should establish these fields so that activating of the STM invokes the STM’s initialization code.

### 34.15.6 Activating the Dual-Monitor Treatment

The dual-monitor treatment may be enabled by SMM code as described in Section 34.15.5. The dual-monitor treatment is activated only if it is enabled and only by the executive monitor. The executive monitor activates the dual-monitor treatment by executing VMCALL in VMX root operation.

When VMCALL activates the dual-monitor treatment, it causes an SMM VM exit. Differences between this SMM VM exit and other SMM VM exits are discussed in Sections 34.15.6.1 through 34.15.6.7. See also “VMCALL—Call to VM Monitor” in Chapter 30.

#### 34.15.6.1 Initial Checks

An execution of VMCALL attempts to activate the dual-monitor treatment if (1) the processor supports the dual-monitor treatment; (2) the logical processor is in VMX root operation; (3) the logical processor is outside SMM and the valid bit is set in the IA32_SMM_MONITOR_CTL MSR; (4) the logical processor is not in virtual-8086 mode and not in compatibility mode; (5) CPL = 0; and (6) the dual-monitor treatment is not active.

The VMCS that manages SMM VM exit caused by this VMCALL is the current VMCS established by the executive monitor. The VMCALL performs the following checks on the current VMCS in the order indicated:

1. There must be a current VMCS pointer.
2. The launch state of the current VMCS must be clear.
3. Reserved bits in the VM-exit controls in the current VMCS must be set properly. Software may consult the VMX capability MSR IA32_VMX_EXIT_CTLS to determine the proper settings (see Appendix A.4).

If any of these checks fail, subsequent checks are skipped and VMCALL fails. If all these checks succeed, the logical processor uses the IA32_SMM_MONITOR_CTL MSR to determine the base address of MSEG. The following checks are performed in the order indicated:

1. The logical processor reads the 32 bits at the base of MSEG and compares them to the processor’s MSEG revision identifier.
2. The logical processor reads the SMM-transfer monitor features field:
   - Bit 0 of the field is the IA-32e mode SMM feature bit, and it indicates whether the logical processor will be in IA-32e mode after the SMM-transfer monitor (STM) is activated.
     - If the VMCALL is executed on a processor that does not support Intel 64 architecture, the IA-32e mode SMM feature bit must be 0.
     - If the VMCALL is executed in 64-bit mode, the IA-32e mode SMM feature bit must be 1.
   - Bits 31:1 of this field are currently reserved and must be zero.

If any of these checks fail, subsequent checks are skipped and the VMCALL fails.

#### 34.15.6.2 MSEG Checking

SMM VM exits that activate the dual-monitor treatment check the following before updating the current-VMCS pointer and the executive-VMCS pointer field (see Section 34.15.2.2):

---

1. Software should consult the VMX capability MSR IA32_VMX_BASIC (see Appendix A.1) to determine whether the dual-monitor treatment is supported.
• The 32 bits at the MSEG base address (used as a physical address) must contain the processor’s MSEG revision identifier.
• Bits 31:1 of the SMM-transfer monitor features field in the MSEG header (see Table 34-10) must be 0. Bit 0 of the field (the IA-32e mode SMM feature bit) must be 0 if the processor does not support Intel 64 architecture. If either of these checks fail, execution of VMCALL fails.

34.15.6.3 Updating the Current-VMCS and Executive-VMCS Pointers

Before performing the steps in Section 34.15.2.2, SMM VM exits that activate the dual-monitor treatment begin by loading the SMM-transfer VMCS pointer with the value of the current-VMCS pointer.

34.15.6.4 Saving Guest State

As noted in Section 34.15.2.4, SMM VM exits save the contents of the SMBASE register into the corresponding field in the guest-state area. While this is true also for SMM VM exits that activate the dual-monitor treatment, the VMCS used for those VM exits exists outside SMRAM.

The SMM-transfer monitor (STM) can also discover the current value of the SMBASE register by using the RDMSR instruction to read the IA32_SMBASE MSR (MSR address 9EH). The following items detail use of this MSR:
• The MSR is supported only if IA32_VMX_MISC[15] = 1 (see Appendix A.6).
• A write to the IA32_SMBASE MSR using WRMSR generates a general-protection fault (#GP(0)). An attempt to write to the IA32_SMBASE MSR fails if made as part of a VM exit or part of a VM entry.
• A read from the IA32_SMBASE MSR using RDMSR generates a general-protection fault (#GP(0)) if executed outside of SMM. An attempt to read from the IA32_SMBASE MSR fails if made as part of a VM exit that does not end in SMM.

34.15.6.5 Saving MSRs

The VM-exit MSR-store area is not used by SMM VM exits that activate the dual-monitor treatment. No MSRs are saved into that area.

34.15.6.6 Loading Host State

The VMCS that is current during an SMM VM exit that activates the dual-monitor treatment was established by the executive monitor. It does not contain the VM-exit controls and host state required to initialize the STM. For this reason, such SMM VM exits do not load processor state as described in Section 27.5. Instead, state is set to fixed values or loaded based on the content of the MSEG header (see Table 34-10):
• CR0 is set to as follows:
  — PG, NE, ET, MP, and PE are all set to 1.
  — CD and NW are left unchanged.
  — All other bits are cleared to 0.
• CR3 is set as follows:
  — Bits 63:32 are cleared on processors that supports IA-32e mode.
  — Bits 31:12 are set to bits 31:12 of the sum of the MSEG base address and the CR3-offset field in the MSEG header.
  — Bits 11:5 and bits 2:0 are cleared (the corresponding bits in the CR3-offset field in the MSEG header are ignored).
  — Bits 4:3 are set to bits 4:3 of the CR3-offset field in the MSEG header.
• CR4 is set as follows:
  — MCE and PGE are cleared.
  — PAE is set to the value of the IA-32e mode SMM feature bit.
If the IA-32e mode SMM feature bit is clear, PSE is set to 1 if supported by the processor; if the bit is set, PSE is cleared.

- All other bits are unchanged.

- DR7 is set to 400H.
- The IA32_DEBUGCTL MSR is cleared to 00000000_00000000H.
- The registers CS, SS, DS, ES, FS, and GS are loaded as follows:
  - All registers are usable.
  - CS.selector is loaded from the corresponding field in the MSEG header (the high 16 bits are ignored), with bits 2:0 cleared to 0. If the result is 0000H, CS.selector is set to 0008H.
  - The selectors for SS, DS, ES, FS, and GS are set to CS.selector+0008H. If the result is 0000H (if the CS selector was FFF8H), these selectors are instead set to 0008H.
  - The base addresses of all registers are cleared to zero.
  - The segment limits for all registers are set to FFFFFFFFH.
  - The AR bytes for the registers are set as follows:
    - CS.Type is set to 11 (execute/read, accessed, non-conforming code segment).
    - For SS, DS, FS, and GS, the Type is set to 3 (read/write, accessed, expand-up data segment).
    - The S bits for all registers are set to 1.
    - The DPL for each register is set to 0.
    - The P bits for all registers are set to 1.
    - On processors that support Intel 64 architecture, CS.L is loaded with the value of the IA-32e mode SMM feature bit.
    - CS.D is loaded with the inverse of the value of the IA-32e mode SMM feature bit.
    - For each of SS, DS, FS, and GS, the D/B bit is set to 1.
    - The G bits for all registers are set to 1.
- LDTR is unusable. The LDTR selector is cleared to 0000H, and the register is otherwise undefined (although the base address is always canonical).
- GDTR.base is set to the sum of the MSEG base address and the GDTR base-offset field in the MSEG header (bits 63:32 are always cleared on processors that supports IA-32e mode). GDTR.limit is set to the corresponding field in the MSEG header (the high 16 bits are ignored).
- IDTR.base is unchanged. IDTR.limit is cleared to 0000H.
- RIP is set to the sum of the MSEG base address and the value of the RIP-offset field in the MSEG header (bits 63:32 are always cleared on logical processors that support IA-32e mode).
- RSP is set to the sum of the MSEG base address and the value of the RSP-offset field in the MSEG header (bits 63:32 are always cleared on logical processor that supports IA-32e mode).
- RFLAGS is cleared, except bit 1, which is always set.
- The logical processor is left in the active state.
- Event blocking after the SMM VM exit is as follows:
  - There is no blocking by STI or by MOV SS.
  - There is blocking by non-maskable interrupts (NMIs) and by SMIs.
  - There are no pending debug exceptions after the SMM VM exit.
- For processors that support IA-32e mode, the IA32_EFER MSR is modified so that LME and LMA both contain the value of the IA-32e mode SMM feature bit.

If any of CR3[63:5], CR4.PAE, CR4.PSE, or IA32_EFER.LMA is changing, the TLBs are updated so that, after VM exit, the logical processor does not use translations that were cached before the transition. This is not neces-
sary for changes that would not affect paging due to the settings of other bits (for example, changes to CR4.PSE if IA32_EFER.LMA was 1 before and after the transition).

### 34.15.6.7 Loading MSRs

The VM-exit MSR-load area is not used by SMM VM exits that activate the dual-monitor treatment. No MSRs are loaded from that area.

### 34.15.7 Deactivating the Dual-Monitor Treatment

The SMM-transfer monitor may deactivate the dual-monitor treatment and return the processor to default treatment of SMIs and SMM (see Section 34.14). It does this by executing a VM entry with the “deactivate dual-monitor treatment” VM-entry control set to 1.

As noted in Section 26.2.1.3 and Section 34.15.4.1, an attempt to deactivate the dual-monitor treatment fails in the following situations: (1) the processor is not in SMM; (2) the “entry to SMM” VM-entry control is 1; or (3) the executive-VMCS pointer does not contain the VMXON pointer (the VM entry is to VMX non-root operation).

As noted in Section 34.15.4.9, VM entries that deactivate the dual-monitor treatment ignore the SMI bit in the interruptibility-state field of the guest-state area. Instead, the blocking of SMIs following such a VM entry depends on whether the logical processor is in SMX operation:

- If the logical processor is in SMX operation, SMIs are blocked after VM entry. SMIs may later be unblocked by the VMXOFF instruction (see Section 34.14.4) or by certain leaf functions of the GETSEC instruction (see Chapter 5, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2C).
- If the logical processor is outside SMX operation, SMIs are unblocked after VM entry.

### 34.16 SMI AND PROCESSOR EXTENDED STATE MANAGEMENT

On processors that support processor extended states using XSAVE/XRSTOR (see Chapter 13, “Managing State Using the XSAVE Feature Set” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1), the processor does not save any XSAVE/XRSTOR related state on an SMI. It is the responsibility of the SMI handler code to properly preserve the state information (including CR4.OSXSAVE, XCR0, and possibly processor extended states using XSAVE/XRSTOR). Therefore, the SMI handler must follow the rules described in Chapter 13, “Managing State Using the XSAVE Feature Set” of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

### 34.17 MODEL-SPECIFIC SYSTEM MANAGEMENT ENHANCEMENT

This section describes enhancement of system management features that apply only to the 4th generation Intel Core processors. These features are model-specific. BIOS and SMM handler must use CPUID to enumerate DisplayFamily_DisplayModel signature when programming with these interfaces.

#### 34.17.1 SMM Handler Code Access Control

The BIOS may choose to restrict the address ranges of code that SMM handler executes. When SMM handler code execution check is enabled, an attempt by the SMM handler to execute outside the ranges specified by SMRR (see Section 34.4.2.1) will cause the assertion of an unrecoverable machine check exception (MCE).

---

1. A logical processor is in SMX operation if GETSEC[SEXIT] has not been executed since the last execution of GETSEC[SENTER]. A logical processor is outside SMX operation if GETSEC[SENTER] has not been executed or if GETSEC[SEXIT] was executed after the last execution of GETSEC[SENTER]. See Chapter 6, “Safer Mode Extensions Reference,” in Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2B.
The interface to enable SMM handler code access check resides in a per-package scope model-specific register MSR_SMM_FEATURE_CONTROL at address 4E0H. An attempt to access MSR_SMM_FEATURE_CONTROL outside of SMM will cause a #GP. Writes to MSR_SMM_FEATURE_CONTROL is further protected by configuration interface of MSR_SMM_MCA_CAP at address 17DH.

Details of the interface of MSR_SMM_FEATURE_CONTROL and MSR_SMM_MCA_CAP are described in Table 35-24.

### 34.17.2 SMI Delivery Delay Reporting

Entry into the system management mode occurs at instruction boundary. In situations where a logical processor is executing an instruction involving a long flow of internal operations, servicing an SMI by that logical processor will be delayed. Delayed servicing of SMI of each logical processor due to executing long flows of internal operation in a physical processor can be queried via a package-scope register MSR_SMM_DELAYED at address 4E2H.

The interface to enable reporting of SMI delivery delay due to long internal flows resides in a per-package scope model-specific register MSR_SMM_DELAYED. An attempt to access MSR_SMM_DELAYED outside of SMM will cause a #GP. Availability to MSR_SMM_DELAYED is protected by configuration interface of MSR_SMM_MCA_CAP at address 17DH.

Details of the interface of MSR_SMM_DELAYED and MSR_SMM_MCA_CAP are described in Table 35-24.

### 34.17.3 Blocked SMI Reporting

A logical processor may have entered into a state and blocked from servicing other interrupts (including SMI). Logical processors in a physical processor that are blocked in serving SMI can be queried in a package-scope register MSR_SMM_BLOCKED at address 4E3H. An attempt to access MSR_SMM_BLOCKED outside of SMM will cause a #GP.

Details of the interface of MSR_SMM_BLOCKED is described in Table 35-24.
This chapter lists MSRs across Intel processor families. All MSRs listed can be read with the RDMSR and written with the WRMSR instructions.

Register addresses are given in both hexadecimal and decimal. The register name is the mnemonic register name and the bit description describes individual bits in registers.

Model specific registers and its bit-fields may be supported for a finite range of processor families/models. To distinguish between different processor family and/or models, software must use CPUID.01H leaf function to query the combination of DisplayFamily and DisplayModel to determine model-specific availability of MSRs (see CPUID instruction in Chapter 3, “Instruction Set Reference, A-M” in the *Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 2A*). Table 35-1 lists the signature values of DisplayFamily and DisplayModel for various processor families or processor number series.

<table>
<thead>
<tr>
<th>DisplayFamily_DisplayModel</th>
<th>Processor Families/Processor Number Series</th>
</tr>
</thead>
<tbody>
<tr>
<td>06_57H</td>
<td>Next Generation Intel® Xeon Phi™ Processor Family</td>
</tr>
<tr>
<td>06_4EH, 06_5EH</td>
<td>6th generation Intel Core processors and Intel Xeon processor E3-1500m v5 product family and E3-1200 v5 product family based on Skylake microarchitecture</td>
</tr>
<tr>
<td>06_56H</td>
<td>Intel Xeon processor D-1500 product family based on Broadwell microarchitecture</td>
</tr>
<tr>
<td>06_4FH</td>
<td>Next Generation Intel Xeon processor based on Broadwell microarchitecture</td>
</tr>
<tr>
<td>06_47H</td>
<td>5th generation Intel Core processors, Intel Xeon processor E3-1200 v4 product family based on Broadwell microarchitecture</td>
</tr>
<tr>
<td>06_3DH</td>
<td>Intel Core M-5xxx Processor, 5th generation Intel Core processors based on Broadwell microarchitecture</td>
</tr>
<tr>
<td>06_3FH</td>
<td>Intel Xeon processor E5-4600/2600/1600 v3 product families, Intel Xeon processor E7 v3 product families based on Haswell-E microarchitecture, Intel Core i7-59xx Processor Extreme Edition</td>
</tr>
<tr>
<td>06_3CH, 06_45H, 06_46H</td>
<td>4th Generation Intel Core processor and Intel Xeon processor E3-1200 v3 product family based on Haswell microarchitecture</td>
</tr>
<tr>
<td>06_3EH</td>
<td>Intel Xeon processor E7-8800/4800/2800 v2 product families based on Ivy Bridge-E microarchitecture</td>
</tr>
<tr>
<td>06_3EH</td>
<td>Intel Xeon processor E5-2600/1600 v2 product families and Intel Xeon processor E5-2400 v2 product family based on Ivy Bridge-E microarchitecture, Intel Core i7-49xx Processor Extreme Edition</td>
</tr>
<tr>
<td>06_3AH</td>
<td>3rd Generation Intel Core Processor and Intel Xeon processor E3-1200 v2 product family based on Ivy Bridge microarchitecture</td>
</tr>
<tr>
<td>06_2DH</td>
<td>Intel Xeon processor E5 Family based on Intel microarchitecture code name Sandy Bridge, Intel Core i7-39xx Processor Extreme Edition</td>
</tr>
<tr>
<td>06_2FH</td>
<td>Intel Xeon Processor E7 Family</td>
</tr>
<tr>
<td>06_2AH</td>
<td>Intel Xeon processor E3-1200 product family; 2nd Generation Intel Core i7, i5, i3 Processors 2xxx Series</td>
</tr>
<tr>
<td>06_2EH</td>
<td>Intel Xeon processor 7500, 6500 series</td>
</tr>
<tr>
<td>06_25H, 06_2CH</td>
<td>Intel Xeon processors 3600, 5600 series, Intel Core i7, i5 and i3 Processors</td>
</tr>
<tr>
<td>06_1EH, 06_1FH</td>
<td>Intel Core i7 and i5 Processors</td>
</tr>
<tr>
<td>06_1AH</td>
<td>Intel Core i7 Processor, Intel Xeon processor 3400, 3500, 5500 series</td>
</tr>
<tr>
<td>06_1DH</td>
<td>Intel Xeon processor MP 7400 series</td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

35.1 ARCHITECTURAL MSRS

Many MSRs have carried over from one generation of IA-32 processors to the next and to Intel 64 processors. A subset of MSRs and associated bit fields, which do not change on future processor generations, are now considered architectural MSRs. For historical reasons (beginning with the Pentium 4 processor), these “architectural MSRs” were given the prefix “IA32_.” Table 35-2 lists the architectural MSRs, their addresses, their current names, their names in previous IA-32 processors, and bit fields that are considered architectural. MSR addresses outside Table 35-2 and certain bit fields in an MSR address that overlap with architectural MSR addresses are model-specific. Code that accesses a machine specified MSR and that is executed on a processor that does not support that MSR will generate an exception.

Architectural MSR or individual bit fields in an architectural MSR may be introduced or transitioned at the granularity of certain processor family/model or the presence of certain CPUID feature flags. The right-most column of Table 35-2 provides information on the introduction of each architectural MSR or its individual fields. This information is expressed either as signature values of “DF_DM” (see Table 35-1) or via CPUID flags.

Certain bit field position may be related to the maximum physical address width, the value of which is expressed as “MAXPHYADDR” in Table 35-2. “MAXPHYADDR” is reported by CPUID.8000_0008H leaf.
MSR address range between 40000000H - 400000FFH is marked as a specially reserved range. All existing and future processors will not implement any features using any MSR in this range.

### Table 35-2. IA-32 Architectural MSRs

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H 0</td>
<td>IA32_P5_MC_ADDR (P5_MC_ADDR)</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
<td>Pentium Processor (05_01H)</td>
</tr>
<tr>
<td>1H 1</td>
<td>IA32_P5_MC_TYPE (P5_MC_TYPE)</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
<td>DF_DM = 05_01H</td>
</tr>
<tr>
<td>6H 6</td>
<td>IA32_MONITOR_FILTER_SIZE</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination.”</td>
<td>0F_03H</td>
</tr>
<tr>
<td>10H 16</td>
<td>IA32_TIME_STAMP_COUNTER (TSC)</td>
<td>See Section 17.14, “Time-Stamp Counter.”</td>
<td>05_01H</td>
</tr>
<tr>
<td>17H 23</td>
<td>IA32_PLATFORM_ID (MSR_PLATFORM_ID)</td>
<td>Platform ID (RO) The operating system can use this MSR to determine “slot” information for the processor and the proper microcode update to load.</td>
<td>06_01H</td>
</tr>
<tr>
<td>49:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>52:50</td>
<td>Platform ID (RO) Contains information concerning the intended platform for the processor.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>52 51 50</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 0 Processor Flag 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 0 1 Processor Flag 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 0 Processor Flag 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0 1 1 Processor Flag 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 0 0 Processor Flag 4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 0 1 Processor Flag 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 0 Processor Flag 6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 1 1 Processor Flag 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:53</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1BH 27</td>
<td>IA32_APIC_BASE (APIC_BASE)</td>
<td></td>
<td>06_01H</td>
</tr>
<tr>
<td>7:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>BSP flag (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Enable x2APIC mode</td>
<td></td>
<td>06_1AH</td>
</tr>
<tr>
<td>11</td>
<td>APIC Global Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(MAXPHYADDR - 1):12</td>
<td>APIC Base (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63: MAXPHYADDR</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3AH 58</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Control Features in Intel 64 Processor (R/W)</td>
<td>If any one enumeration condition for defined bit field holds</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Lock bit (R/WO): (1 = locked). When set, locks this MSR from being written, writes to this bit will result in GP(0). Note: Once the Lock bit is set, the contents of this register cannot be modified. Therefore the lock bit must be set after configuring support for Intel Virtualization Technology and prior to transferring control to an option ROM or the OS. Hence, once the Lock bit is set, the entire IA32_FEATURE_CONTROL contents are preserved across RESET when PWRGOOD is not deasserted.</td>
<td></td>
<td>If any one enumeration condition for defined bit field position greater than bit 0 holds</td>
</tr>
<tr>
<td>1</td>
<td>Enable VMX inside SMX operation (R/WL): This bit enables a system executive to use VMX in conjunction with SMX to support Intel® Trusted Execution Technology. BIOS must set this bit only when the CPUID function 1 returns VMX feature flag and SMX feature flag set (ECX bits 5 and 6 respectively).</td>
<td></td>
<td>If CPUID.01H:ECX[5] = 1 &amp;&amp; CPUID.01H:ECX[6] = 1</td>
</tr>
<tr>
<td>2</td>
<td>Enable VMX outside SMX operation (R/WL): This bit enables VMX for system executive that do not require SMX. BIOS must set this bit only when the CPUID function 1 returns VMX feature flag set (ECX bit 5).</td>
<td></td>
<td>If CPUID.01H:ECX[5] = 1</td>
</tr>
<tr>
<td>7:3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:8</td>
<td>SENTER Local Function Enables (R/WL): When set, each bit in the field represents an enable control for a corresponding SENTER function. This bit is supported only if CPUID.1:ECX.[bit 6] is set</td>
<td></td>
<td>If CPUID.01H:ECX[6] = 1</td>
</tr>
<tr>
<td>15</td>
<td>SENTER Global Enable (R/WL): This bit must be set to enable SENTER leaf functions. This bit is supported only if CPUID.1:ECX.[bit 6] is set</td>
<td></td>
<td>If CPUID.01H:ECX[6] = 1</td>
</tr>
<tr>
<td>17:16</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>SGX Global Enable (R/WL): This bit must be set to enable SGX leaf functions. This bit is supported only if CPUID.1:ECX.[bit 6] is set.</td>
<td></td>
<td>If CPUID.(EAX=07H, ECX=0H): EBX[2] = 1</td>
</tr>
<tr>
<td>19</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>LMCE On (R/WL): When set, system software can program the MSRs associated with LMCE to configure delivery of some machine check exceptions to a single logical processor.</td>
<td></td>
<td>If IA32_MCG_CAP[27] = 1</td>
</tr>
<tr>
<td>63:21</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>3BH 59</td>
<td>IA32_TSC_ADJUST</td>
<td>Per Logical Processor TSC Adjust (R/Write to clear)</td>
<td>If CPUID.(EAX=07H, ECX=0H): EBX[1] = 1</td>
</tr>
<tr>
<td>63:0</td>
<td>THREAD_ADJUST:</td>
<td>Local offset value of the IA32_TSC for a logical processor. Reset value is Zero. A write to IA32_TSC will modify the local offset in IA32_TSC_ADJUST and the content of IA32_TSC, but does not affect the internal invariant TSC hardware.</td>
<td></td>
</tr>
<tr>
<td>79H 121</td>
<td>IA32_BIOS_UPDT_TRIG (BIOS_UPDT_TRIG)</td>
<td>BIOS Update Trigger (W)</td>
<td>Executing a WRMSR instruction to this MSR causes a microcode update to be loaded into the processor. See Section 9.11.6, “Microcode Update Loader.” A processor may prevent writing to this MSR when loading guest states on VM entries or saving guest states on VM exits.</td>
</tr>
<tr>
<td>8BH 139</td>
<td>IA32_BIOS_SIGN_ID (BIOS_SIGN/BBL_CR_D3)</td>
<td>BIOS Update Signature (RO)</td>
<td>Returns the microcode update signature following the execution of CPUID.01H. A processor may prevent writing to this MSR when loading guest states on VM entries or saving guest states on VM exits.</td>
</tr>
<tr>
<td>31:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>It is recommended that this field be pre-loaded with 0 prior to executing CPUID. If the field remains 0 following the execution of CPUID; this indicates that no microcode update is loaded. Any non-zero value is the microcode update signature.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Valid (R/w)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Controls SMI unblocking by VMXOFF (see Section 34.14.4)</td>
<td>If IA32_VMX_MISC[28]</td>
<td></td>
</tr>
<tr>
<td>11:3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:12</td>
<td>MSEG Base (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9EH 158</td>
<td>IA32_SMBASE</td>
<td>Base address of the logical processor’s SMRAM image (RO, SMM only)</td>
<td>If IA32_VMX_MISC[15]</td>
</tr>
<tr>
<td>C1H 193</td>
<td>IA32_PMC0 (PERFCTR0)</td>
<td>General Performance Counter 0 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 0</td>
</tr>
<tr>
<td>C2H 194</td>
<td>IA32_PMC1 (PERFCTR1)</td>
<td>General Performance Counter 1 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 1</td>
</tr>
<tr>
<td>Hex</td>
<td>Decimal</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
</tr>
<tr>
<td>-----</td>
<td>---------</td>
<td>--------------------------------------------------------</td>
<td>---------------------</td>
</tr>
<tr>
<td>C3H</td>
<td>195</td>
<td>IA32_PMC2 General Performance Counter 2 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 2</td>
</tr>
<tr>
<td>C4H</td>
<td>196</td>
<td>IA32_PMC3 General Performance Counter 3 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 3</td>
</tr>
<tr>
<td>C5H</td>
<td>197</td>
<td>IA32_PMC4 General Performance Counter 4 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 4</td>
</tr>
<tr>
<td>C6H</td>
<td>198</td>
<td>IA32_PMC5 General Performance Counter 5 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 5</td>
</tr>
<tr>
<td>C7H</td>
<td>199</td>
<td>IA32_PMC6 General Performance Counter 6 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 6</td>
</tr>
<tr>
<td>C8H</td>
<td>200</td>
<td>IA32_PMC7 General Performance Counter 7 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 7</td>
</tr>
<tr>
<td>E7H</td>
<td>231</td>
<td>IA32_MPERF TSC Frequency Clock Counter (R/Write to clear)</td>
<td>If CPUID.06H: ECX[0] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:0 CO_MCNT: C0 TSC Frequency Clock Count</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Increments at fixed interval (relative to TSC freq.) when the logical processor is in C0. Cleared upon overflow / wrap-around of IA32_APERF.</td>
<td></td>
</tr>
<tr>
<td>E8H</td>
<td>232</td>
<td>IA32_APERF Actual Performance Clock Counter (R/Write to clear).</td>
<td>If CPUID.06H: ECX[0] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:0 CO_ACNT: C0 Actual Frequency Clock Count</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Accumulates core clock counts at the coordinated clock frequency, when the logical processor is in C0. Cleared upon overflow / wrap-around of IA32_MPERF.</td>
<td></td>
</tr>
<tr>
<td>FEH</td>
<td>254</td>
<td>IA32_MTRRCAP (MTRRcap) MTRR Capability (RO) Section 11.11.2.1, “IA32_MTRR_DEF_TYPE MSR.”</td>
<td>06.01H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7:0 VCNT: The number of variable memory type ranges in the processor.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 Fixed range MTRRs are supported when set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>9 Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 WC Supported when set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 SMRR Supported when set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:12 Reserved.</td>
<td></td>
</tr>
<tr>
<td>174H</td>
<td>372</td>
<td>IA32_SYSENTER_CS SYSENTER_CS_MSR (R/W)</td>
<td>06.01H</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15:0 CS Selector</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:16 Reserved.</td>
<td></td>
</tr>
<tr>
<td>175H</td>
<td>373</td>
<td>IA32_SYSENTER_ESP SYSENTER_ESP_MSR (R/W)</td>
<td>06.01H</td>
</tr>
<tr>
<td>176H</td>
<td>374</td>
<td>IA32_SYSENTER_EIP SYSENTER_EIP_MSR (R/W)</td>
<td>06.01H</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP (MCG_CAP)</td>
<td>Global Machine Check Capability (RO)</td>
<td>06_01H</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>Count: Number of reporting banks.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>MCG_CTL_P: IA32_MCG_CTL is present if this bit is set</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>MCG_EXT_P: Extended machine check state registers are present if this bit is set</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>MCP_CMCI_P: Support for corrected MC error event is present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>MCG_TES_P: Threshold-based error status register are present if this bit is set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:12</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td>23:16</td>
<td>MCG_EXT_CNT: Number of extended machine check state registers present.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>MCG_SER_P: The processor supports software error recovery if this bit is set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>26</td>
<td>MCG_ELOG_P: Indicates that the processor allows platform firmware to be invoked when an error is detected so that it may provide additional platform specific information in an ACPI format “Generic Error Data Entry” that augments the data included in machine check bank registers.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>27</td>
<td>MCG_LMCE_P: Indicates that the processor support extended state in IA32_MCG_STATUS and associated MSR necessary to configure Local Machine Check Exception (LMCE).</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:28</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS (MCG_STATUS)</td>
<td>Global Machine Check Status (R/W0)</td>
<td>06_01H</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>RIPV. Restart IP valid</td>
<td>06_01H</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>EIPV. Error IP valid</td>
<td>06_01H</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>MCIP. Machine check in progress</td>
<td>06_01H</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>LMCE_S.</td>
<td>If IA32_MCG_CAP.LMCE_P[2:7] =1</td>
</tr>
<tr>
<td></td>
<td>63:4</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>17BH 379</td>
<td>IA32_MCG_CTL (MCG_CTL)</td>
<td>Global Machine Check Control (R/W)</td>
<td>If IA32_MCG_CAP.CTL_P[8] =1</td>
</tr>
<tr>
<td>180H-185H</td>
<td>384-389</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0 (PERFEVTSEL0)</td>
<td>Performance Event Select Register 0 (R/W)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 0</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Event Select: Selects a performance event logic unit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:8</td>
<td>UMask: Qualifies the microarchitectural condition to detect on the selected event logic.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>USR: Counts while in privilege level is not ring 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>OS: Counts while in privilege level is ring 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Edge: Enables edge detection if set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>PC: enables pin control.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>INT: enables interrupt on counter overflow.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>AnyThread: When set to 1, it enables counting the associated event conditions occurring across all logical processors sharing a processor core. When set to 0, the counter only increments the associated event conditions occurring in the logical processor which programmed the MSR.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>EN: enables the corresponding performance counter to commence counting when this bit is set.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>INV: invert the CMASK.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:24</td>
<td>CMASK: When CMASK is not zero, the corresponding performance counter increments each cycle if the event count is greater than or equal to the CMASK.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1 (PERFEVTSEL1)</td>
<td>Performance Event Select Register 1 (R/w)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 1</td>
</tr>
<tr>
<td>188H 392</td>
<td>IA32_PERFEVTSEL2</td>
<td>Performance Event Select Register 2 (R/w)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 2</td>
</tr>
<tr>
<td>189H 393</td>
<td>IA32_PERFEVTSEL3</td>
<td>Performance Event Select Register 3 (R/w)</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 3</td>
</tr>
<tr>
<td>18AH-197H</td>
<td>Reserved</td>
<td></td>
<td>06_0EH²</td>
</tr>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>(RO)</td>
<td>0F_03H</td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td>Current performance State Value</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>(R/w)</td>
<td>0F_03H</td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td>Target performance State Value</td>
<td></td>
</tr>
<tr>
<td></td>
<td>31:16</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>IDA Engage. (R/w)</td>
<td>06_0FH (Mobile only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When set to 1: disengages IDA</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex</strong></td>
<td><strong>Decimal</strong></td>
<td><strong>Address</strong></td>
<td><strong>Architectural MSR Name and bit fields (Former MSR Name)</strong></td>
</tr>
<tr>
<td>63:33</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>19AH</td>
<td>410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Clock Modulation Control (R/W) See Section 14.7.3, “Software Controlled Clock Modulation.”</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Extended On-Demand Clock Modulation Duty Cycle:</td>
</tr>
<tr>
<td>3:1</td>
<td></td>
<td></td>
<td>On-Demand Clock Modulation Duty Cycle: Specific encoded values for target duty cycle modulation.</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>On-Demand Clock Modulation Enable: Set 1 to enable modulation.</td>
</tr>
<tr>
<td>63:5</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>19BH</td>
<td>411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Thermal Interrupt Control (R/W) Enables and disables the generation of an interrupt on temperature transitions detected with the processor’s thermal sensors and thermal monitor. See Section 14.7.2, “Thermal Monitor.”</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>High-Temperature Interrupt Enable</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Low-Temperature Interrupt Enable</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>PROCHOT# Interrupt Enable</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>FORCEPR# Interrupt Enable</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>Critical Temperature Interrupt Enable</td>
</tr>
<tr>
<td>7:5</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>14:8</td>
<td></td>
<td></td>
<td>Threshold #1 Value</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
<td>Threshold #1 Interrupt Enable</td>
</tr>
<tr>
<td>22:16</td>
<td></td>
<td></td>
<td>Threshold #2 Value</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td></td>
<td>Threshold #2 Interrupt Enable</td>
</tr>
<tr>
<td>24</td>
<td></td>
<td></td>
<td>Power Limit Notification Enable If CPUID.06H:EAX[4] = 1</td>
</tr>
<tr>
<td>63:25</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>19CH</td>
<td>412</td>
<td>IA32_THERM_STATUS</td>
<td>Thermal Status Information (RO) Contains status information about the processor’s thermal sensor and automatic thermal monitoring facilities. See Section 14.7.2, “Thermal Monitor”</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Thermal Status (RO):</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Thermal Status Log (R/w):</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>PROCHOT # or FORCEPR# event (RO)</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>PROCHOT # or FORCEPR# log (R/w/C0)</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>Critical Temperature Status (RO)</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Critical Temperature Status log (R/WC0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Thermal Threshold #1 Status (RO)</td>
<td></td>
<td>If CPUID.01H:ECX[8] = 1</td>
</tr>
<tr>
<td>7</td>
<td>Thermal Threshold #1 log (R/WC0)</td>
<td></td>
<td>If CPUID.01H:ECX[8] = 1</td>
</tr>
<tr>
<td>8</td>
<td>Thermal Threshold #2 Status (RO)</td>
<td></td>
<td>If CPUID.01H:ECX[8] = 1</td>
</tr>
<tr>
<td>9</td>
<td>Thermal Threshold #2 log (R/WC0)</td>
<td></td>
<td>If CPUID.01H:ECX[8] = 1</td>
</tr>
<tr>
<td>10</td>
<td>Power Limitation Status (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[4] = 1</td>
</tr>
<tr>
<td>11</td>
<td>Power Limitation log (R/WC0)</td>
<td></td>
<td>If CPUID.06H:EAX[4] = 1</td>
</tr>
<tr>
<td>12</td>
<td>Current Limit Status (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[7] = 1</td>
</tr>
<tr>
<td>13</td>
<td>Current Limit log (R/WC0)</td>
<td></td>
<td>If CPUID.06H:EAX[7] = 1</td>
</tr>
<tr>
<td>14</td>
<td>Cross Domain Limit Status (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[7] = 1</td>
</tr>
<tr>
<td>15</td>
<td>Cross Domain Limit log (R/WC0)</td>
<td></td>
<td>If CPUID.06H:EAX[7] = 1</td>
</tr>
<tr>
<td>22:16</td>
<td>Digital Readout (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[0] = 1</td>
</tr>
<tr>
<td>26:23</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30:27</td>
<td>Resolution in Degrees Celsius (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[0] = 1</td>
</tr>
<tr>
<td>31</td>
<td>Reading Valid (RO)</td>
<td></td>
<td>If CPUID.06H:EAX[0] = 1</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>Enable Misc. Processor Features (R/W)</td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td>0</td>
<td>Fast-Strings Enable</td>
<td></td>
<td>OF_0H</td>
</tr>
<tr>
<td>2:1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Automatic Thermal Control Circuit Enable (R/W)</td>
<td></td>
<td>OF_0H</td>
</tr>
<tr>
<td>1</td>
<td>Setting this bit enables the thermal control circuit (TCC portion of the Intel Thermal Monitor feature. This allows the processor to automatically reduce power consumption in response to TCC activation.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Disabled.</td>
<td>Note: In some products clearing this bit might be ignored in critical thermal conditions, and TM1, TM2 and adaptive thermal throttling will still be activated.</td>
<td></td>
</tr>
<tr>
<td>6:4</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Performance Monitoring Available (R)</td>
<td></td>
<td>OF_0H</td>
</tr>
<tr>
<td>1</td>
<td>Performance monitoring enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Performance monitoring disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Decimal</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td></td>
<td>Branch Trace Storage Unavailable (RO)</td>
<td>0 = BTS is supported</td>
<td>0F_0H</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>Precise Event Based Sampling (PEBS) Available (RO)</td>
<td>0 = PEBS is supported</td>
<td>06_0FH</td>
</tr>
<tr>
<td>15:13</td>
<td></td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>Enhanced Intel SpeedStep Technology Enable (R/W)</td>
<td></td>
<td>If CPUID.01H:ECX[7] =1</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>ENABLE MONITOR FSM (R/W)</td>
<td></td>
<td>0F_03H</td>
</tr>
<tr>
<td>21:19</td>
<td></td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>Limit CPUID Maxval (R/w)</td>
<td>When this bit is set to 1, CPUID.00H returns a maximum value in EAX[7:0] of 3. BIOS should contain a setup question that allows users to specify when the installed OS does not support CPUID functions greater than 3. Before setting this bit, BIOS must execute the CPUID.0H and examine the maximum value returned in EAX[7:0]. If the maximum value is greater than 3, the bit is supported. Otherwise, the bit is not supported. Writing to this bit when the maximum value is greater than 3 may generate a #GP exception. Setting this bit may cause unexpected behavior in software that depends on the availability of CPUID leaves greater than 3.</td>
<td>0F_03H</td>
</tr>
<tr>
<td>23</td>
<td>xTPR Message Disable (R/w)</td>
<td>When set to 1, xTPR messages are disabled. xTPR messages are optional messages that allow the processor to inform the chipset of its priority.</td>
<td>if CPUID.01H:ECX[14] = 1</td>
</tr>
<tr>
<td>33:24</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>XD Bit Disable (R/w)</td>
<td>When set to 1, the Execute Disable Bit feature (XD Bit) is disabled and the XD Bit extended feature flag will be clear (CPUID.80000001H: EDX[20]=0). When set to a 0 (default), the Execute Disable Bit feature (if available) allows the OS to enable PAE paging and take advantage of data only pages. BIOS must not alter the contents of this bit location, if XD bit is not supported. Writing this bit to 1 when the XD Bit extended feature flag is set to 0 may generate a #GP exception.</td>
<td>if CPUID.80000001H:EDX[20] = 1</td>
</tr>
<tr>
<td>63:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1B0H 432</td>
<td>IA32_ENERGY_PERF_BIAS Performance Energy Bias Hint (R/w)</td>
<td>if CPUID.6H:ECX[3] = 1</td>
<td></td>
</tr>
<tr>
<td>3:0</td>
<td>Power Policy Preference: 0 indicates preference to highest performance. 15 indicates preference to maximize energy saving.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:4</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
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<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>Pkg Thermal Status (RO):</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Pkg Thermal Status Log (R/W):</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Pkg PROCHOT # event (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Pkg PROCHOT # log (R/WC0)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>Pkg Critical Temperature Status (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>Pkg Critical Temperature Status log (R/WC0)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Pkg Thermal Threshold #1 Status (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>Pkg Thermal Threshold #1 log (R/WC0)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>Pkg Thermal Threshold #2 Status (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>Pkg Thermal Threshold #1 log (R/WC0)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>Pkg Power Limitation Status (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Pkg Power Limitation log (R/WC0)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:12</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>22:16</td>
<td>Pkg Digital Readout (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:23</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1B2H 434</td>
<td>IA32_PACKAGE_THERM_INTERRUPT</td>
<td>Pkg Thermal Interrupt Control (R/W) Enables and disables the generation of an interrupt on temperature transitions detected with the package's thermal sensor. See Section 14.8, &quot;Package Level Thermal Management.&quot;</td>
<td>If CPUID.06H: EAX[6] = 1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Pkg High-Temperature Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Pkg Low-Temperature Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Pkg PROCHOT# Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>Pkg Overheat Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7:5</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14:8</td>
<td>Pkg Threshold #1 Value</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>Pkg Threshold #1 Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>22:16</td>
<td>Pkg Threshold #2 Value</td>
<td></td>
</tr>
<tr>
<td></td>
<td>23</td>
<td>Pkg Threshold #2 Interrupt Enable</td>
<td></td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>Pkg Power Limit Notification Enable</td>
<td></td>
</tr>
</tbody>
</table>
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<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Decimal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:25</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1D9H</td>
<td>473</td>
<td>IA32_DEBUGCTL (MSR_DEBUGCTLA, MSR_DEBUGCTLB)</td>
<td>Trace/Profile Resource Control (R/w)</td>
</tr>
<tr>
<td>0</td>
<td>LBR: Setting this bit to 1 enables the processor to record a running trace of the most recent branches taken by the processor in the LBR stack.</td>
<td>06_01H</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>BTF: Setting this bit to 1 enables the processor to treat EFLAGS.TF as single-step on branches instead of single-step on instructions.</td>
<td>06_01H</td>
<td></td>
</tr>
<tr>
<td>5:2</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>TR: Setting this bit to 1 enables branch trace messages to be sent.</td>
<td>06_0EH</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>BTS: Setting this bit enables branch trace messages (BTMs) to be logged in a BTS buffer.</td>
<td>06_0EH</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>BTINT: When clear, BTMs are logged in a BTS buffer in circular fashion. When this bit is set, an interrupt is generated by the BTS facility when the BTS buffer is full.</td>
<td>06_0EH</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>1: BTS_OFF_OS: When set, BTS or BTM is skipped if CPL = 0.</td>
<td>06_0FH</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>BTS_OFF_USR: When set, BTS or BTM is skipped if CPL &gt; 0.</td>
<td>06_0FH</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>FREEZE_LBRS_ON_PMI: When set, the LBR stack is frozen on a PMI request.</td>
<td>If CPUID.01H: ECX[15] = 1 &amp;&amp; CPUID.0AH: EAX[7:0] &gt; 1</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>FREEZE_PERFMON_ON_PMI: When set, each ENABLE bit of the global counter control MSR are frozen (address 38FH) on a PMI request</td>
<td>If CPUID.01H: ECX[15] = 1 &amp;&amp; CPUID.0AH: EAX[7:0] &gt; 1</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>ENABLE_UNCORE_PMI: When set, enables the logical processor to receive and generate PMI on behalf of the uncore.</td>
<td>06_1AH</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>FREEZE_WHILE_SMM: When set, freezes perfmon and trace messages while in SMM.</td>
<td>If IA32_PERF_CAPABILITIES[12] = 1</td>
<td></td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1F2H</td>
<td>498</td>
<td>IA32_SMRR_PHYSBASE</td>
<td>SMRR Base Address (Writeable only in SMM)</td>
</tr>
<tr>
<td>7:0</td>
<td>Base address of SMM memory range.</td>
<td>Type. Specifies memory type of the range.</td>
<td></td>
</tr>
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</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
<td>Comment</td>
</tr>
<tr>
<td>11:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:12</td>
<td>PhysBase. SMRR physical Base Address.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1F3H 499</td>
<td>IA32_SMRR_PHYSMASK</td>
<td>SMRR Range Mask. (Writeable only in SMM)</td>
<td>Range Mask of SMM memory range.</td>
</tr>
<tr>
<td></td>
<td>10:0</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Valid</td>
<td>Enable range mask.</td>
</tr>
<tr>
<td></td>
<td>31:12</td>
<td>PhysMask</td>
<td>SMRR address range mask.</td>
</tr>
<tr>
<td></td>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1F8H 504</td>
<td>IA32_PLATFORM_DCA_CAP</td>
<td>DCA Capability (R)</td>
<td>If CPUID.01H: ECX[18] = 1</td>
</tr>
<tr>
<td>1F9H 505</td>
<td>IA32_CPU_DCA_CAP</td>
<td>If set, CPU supports Prefetch-Hint type.</td>
<td>If CPUID.01H: ECX[18] = 1</td>
</tr>
<tr>
<td>1FAH 506</td>
<td>IA32_DCA_0_CAP</td>
<td>DCA type 0 Status and Control register.</td>
<td>If CPUID.01H: ECX[18] = 1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>DCA_ACTIVE: Set by HW when DCA is fuse-enabled and no defeatures are set.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2:1</td>
<td>TRANSACTION</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6:3</td>
<td>DCA_TYPE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10:7</td>
<td>DCA_QUEUE_SIZE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12:11</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16:13</td>
<td>DCA_DELAY: Writes will update the register but have no HW side-effect.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>23:17</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>24</td>
<td>Sw_BLOCK: SW can request DCA block by setting this bit.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>26</td>
<td>Hw_BLOCK: Set when DCA is blocked by HW (e.g. CR0.CD = 1).</td>
<td></td>
</tr>
<tr>
<td></td>
<td>31:27</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>200H 512</td>
<td>IA32_MTRR_PHYSBASE0 (MTRRphysBase0)</td>
<td>See Section 11.11.2.3, “Variable Range MTRRs.”</td>
<td>If CPUID.01H: EDX.MTRR[12] =1</td>
</tr>
<tr>
<td>201H 513</td>
<td>IA32_MTRR_PHYSMASK0</td>
<td>MTRRphysMask0</td>
<td>If CPUID.01H: EDX.MTRR[12] =1</td>
</tr>
<tr>
<td>202H 514</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>MTRRphysBase1</td>
<td>If CPUID.01H: EDX.MTRR[12] =1</td>
</tr>
<tr>
<td>203H 515</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>MTRRphysMask1</td>
<td>If CPUID.01H: EDX.MTRR[12] =1</td>
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</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

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<tr>
<th>Register Address</th>
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</thead>
<tbody>
<tr>
<td>204H 516</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>MTRRphysBase2</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>205H 517</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>MTRRphysMask2</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>206H 518</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>MTRRphysBase3</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>207H 519</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>MTRRphysMask3</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>208H 520</td>
<td>IA32_MTRR_PHYSBASE4</td>
<td>MTRRphysBase4</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>209H 521</td>
<td>IA32_MTRR_PHYSMASK4</td>
<td>MTRRphysMask4</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20AH 522</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>MTRRphysBase5</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>MTRRphysMask5</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20CH 524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>MTRRphysBase6</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>MTRRphysMask6</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>MTRRphysBase7</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>MTRRphysMask7</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>210H 528</td>
<td>IA32_MTRR_PHYSBASE8</td>
<td>MTRRphysBase8</td>
<td>If IA32_MTRRCAP[7:0] &gt; 8</td>
</tr>
<tr>
<td>211H 529</td>
<td>IA32_MTRR_PHYSMASK8</td>
<td>MTRRphysMask8</td>
<td>If IA32_MTRRCAP[7:0] &gt; 8</td>
</tr>
<tr>
<td>212H 530</td>
<td>IA32_MTRR_PHYSBASE9</td>
<td>MTRRphysBase9</td>
<td>If IA32_MTRRCAP[7:0] &gt; 9</td>
</tr>
<tr>
<td>213H 531</td>
<td>IA32_MTRR_PHYSMASK9</td>
<td>MTRRphysMask9</td>
<td>If IA32_MTRRCAP[7:0] &gt; 9</td>
</tr>
<tr>
<td>250H 592</td>
<td>IA32_MTRR_FIX64K_00000</td>
<td>MTRRfix64K_00000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>MTRRfix16K_80000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>MTRRfix16K_A0000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000 (MTRRfix4K_C0000 )</td>
<td>MTRRfix4K_C0000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>269H 617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>MTRRfix4K_C8000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>26AH 618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>MTRRfix4K_D0000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>26BH 619</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>MTRRfix4K_D8000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
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</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
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<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>26CH 620</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>MTRRfix4K_E0000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>26DH 621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>MTRRfix4K_E8000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>26EH 622</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>MTRRfix4K_F0000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>26FH 623</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>MTRRfix4K_F8000</td>
<td>If CPUID.01H: EDX.MTRR[12] = 1</td>
</tr>
<tr>
<td>277H 631</td>
<td>IA32_PAT</td>
<td>IA32_PAT (R/W)</td>
<td>If CPUID.01H: EDX.MTRR[16] = 1</td>
</tr>
<tr>
<td></td>
<td>2:0</td>
<td>PA0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7:3</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>10:8</td>
<td>PA1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:11</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>18:16</td>
<td>PA2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>23:19</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>26:24</td>
<td>PA3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>31:27</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>34:32</td>
<td>PA4</td>
<td></td>
</tr>
<tr>
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<td>39:35</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>42:40</td>
<td>PA5</td>
<td></td>
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<tr>
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<td>47:43</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>50:48</td>
<td>PA6</td>
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<tr>
<td></td>
<td>55:51</td>
<td>Reserved.</td>
<td></td>
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<tr>
<td></td>
<td>58:56</td>
<td>PA7</td>
<td></td>
</tr>
<tr>
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<td>63:59</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>280H 640</td>
<td>IA32_MCG_CTL2</td>
<td>(R/W)</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 0</td>
</tr>
<tr>
<td></td>
<td>14:0</td>
<td>Corrected error count threshold.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>29:15</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>30</td>
<td>CMCI_EN</td>
<td></td>
</tr>
<tr>
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<td>63:31</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>281H 641</td>
<td>IA32_MC1_CTL2</td>
<td>(R/W) same fields as IA32_MCO_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 1</td>
</tr>
<tr>
<td>282H 642</td>
<td>IA32_MC2_CTL2</td>
<td>(R/W) same fields as IA32_MCO_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 2</td>
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</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

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<thead>
<tr>
<th>Register Address</th>
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<th>MSR/Bit Description</th>
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</tr>
</thead>
<tbody>
<tr>
<td>283H 643</td>
<td>IA32_MC3_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 3</td>
</tr>
<tr>
<td>284H 644</td>
<td>IA32_MC4_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 4</td>
</tr>
<tr>
<td>286H 646</td>
<td>IA32_MC6_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 6</td>
</tr>
<tr>
<td>287H 647</td>
<td>IA32_MC7_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 7</td>
</tr>
<tr>
<td>288H 648</td>
<td>IA32_MC8_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 8</td>
</tr>
<tr>
<td>28AH 650</td>
<td>IA32_MC10_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 10</td>
</tr>
<tr>
<td>28BH 651</td>
<td>IA32_MC11_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 11</td>
</tr>
<tr>
<td>28EH 654</td>
<td>IA32_MC14_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 14</td>
</tr>
<tr>
<td>28FH 655</td>
<td>IA32_MC15_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 15</td>
</tr>
<tr>
<td>290H 656</td>
<td>IA32_MC16_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 16</td>
</tr>
<tr>
<td>291H 657</td>
<td>IA32_MC17_CTL2</td>
<td>(R/W) same fields as IA32_MC0_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 17</td>
</tr>
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</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

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<tr>
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<tr>
<td>292H 658</td>
<td>IA32_MCG18_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 18</td>
</tr>
<tr>
<td>293H 659</td>
<td>IA32_MCG19_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 19</td>
</tr>
<tr>
<td>295H 661</td>
<td>IA32_MCG21_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 21</td>
</tr>
<tr>
<td>29AH 666</td>
<td>IA32_MCG26_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 26</td>
</tr>
<tr>
<td>29DH 669</td>
<td>IA32_MCG29_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 29</td>
</tr>
<tr>
<td>29FH 671</td>
<td>IA32_MCG31_CTL2</td>
<td>(R/W) same fields as IA32_MCG_CTL2.</td>
<td>If IA32_MCG_CAP[10] = 1 &amp;&amp; IA32_MCG_CAP[7:0] &gt; 31</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>MTRRdefType (R/W)</td>
<td>If CPUID.01H: EDX.MTRR[12] =1</td>
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</tbody>
</table>

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</thead>
<tbody>
<tr>
<td>309H 777</td>
<td>IA32_FIXED_CTR0 (MSR_PERF_FIXED_CTR0)</td>
<td>Fixed-Function Performance Counter 0 (R/W): Counts Instr_Retired.Any.</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 0</td>
</tr>
<tr>
<td>30AH 778</td>
<td>IA32_FIXED_CTR1 (MSR_PERF_FIXED_CTR1)</td>
<td>Fixed-Function Performance Counter 1 0 (R/W): Counts CPU_CLK_Unhalted.Core</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 1</td>
</tr>
<tr>
<td>30BH 779</td>
<td>IA32_FIXED_CTR2 (MSR_PERF_FIXED_CTR2)</td>
<td>Fixed-Function Performance Counter 0 0 (R/W): Counts CPU_CLK_Unhalted.Ref</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 2</td>
</tr>
<tr>
<td>345H 837</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>RO</td>
<td>If CPUID.01H: ECX[15] = 1</td>
</tr>
<tr>
<td>5:0</td>
<td>LBR format</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PEBS Trap</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PEBS_SaveArchRegs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:8</td>
<td>PEBS Record Format</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>1: Freeze while SMM is supported.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>1: Full width of counter writable via IA32_A_PMCx.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:14</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38DH 909</td>
<td>IA32_FIXED_CTR_CTRL</td>
<td>Fixed-Function Performance Counter Control (R/W)</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 1</td>
</tr>
<tr>
<td></td>
<td>Counter increments while the results of ANDing respective enable bit in IA32_PERF_GLOBAL_CTRL with the corresponding OS or USR bits in this MSR is true.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>EN0_OS: Enable Fixed Counter 0 to count while CPL = 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EN0_Usr: Enable Fixed Counter 0 to count while CPL &gt; 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>AnyThread: When set to 1, it enables counting the associated event conditions occurring across all logical processors sharing a processor core. When set to 0, the counter only increments the associated event conditions occurring in the logical processor which programmed the MSR.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>EN0_PMI: Enable PMI when fixed counter 0 overflows.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>EN1_OS: Enable Fixed Counter 1 to count while CPL = 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>EN1_Usr: Enable Fixed Counter 1 to count while CPL &gt; 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Hex</td>
<td>Decimal</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
</tr>
<tr>
<td>------------------</td>
<td>------</td>
<td>---------</td>
<td>--------------------------------------------------------</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>AnyThread: When set to 1, it enables counting the associated event conditions occurring across all logical processors sharing a processor core. When set to 0, the counter only increments the associated event conditions occurring in the logical processor which programmed the MSR.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>EN1_PMI: Enable PMI when fixed counter 1 overflows.</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>EN2_OS: Enable Fixed Counter 2 to count while CPL = 0.</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td>EN2_Usr: Enable Fixed Counter 2 to count while CPL &gt; 0.</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td>AnyThread: When set to 1, it enables counting the associated event conditions occurring across all logical processors sharing a processor core. When set to 0, the counter only increments the associated event conditions occurring in the logical processor which programmed the MSR.</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td>EN2_PMI: Enable PMI when fixed counter 2 overflows.</td>
</tr>
<tr>
<td>63:12</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>38EH 910</td>
<td>38EH</td>
<td>910</td>
<td>IA32_PERF_GLOBAL_STATUS</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Ovf_PMCO: Overflow status of IA32_PMC0.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Ovf_PMCM1: Overflow status of IA32_PMC1.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Ovf_PMCM2: Overflow status of IA32_PMC2.</td>
</tr>
<tr>
<td>31:4</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
<td>Ovf_FixedCtr0: Overflow status of IA32_FIXED_CTR0.</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td></td>
<td>Ovf_FixedCtr1: Overflow status of IA32_FIXED_CTR1.</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td></td>
<td>Ovf_FixedCtr2: Overflow status of IA32_FIXED_CTR2.</td>
</tr>
<tr>
<td>54:35</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>55</td>
<td></td>
<td></td>
<td>Trace_ToPA_PMI: A PMI occurred due to a ToPA entry memory buffer was completely filled.</td>
</tr>
<tr>
<td>57:56</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>58</td>
<td>LBR_Frz: LBRs are frozen due to • IA32_DEBUGCTL.FREEZE_LBR_ON_PMI=1, • The LBR stack overflowed</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>CTR_Frz: Performance counters in the core PMU are frozen due to • IA32_DEBUGCTL.FREEZE_PERFMON_ON_PMU=1, • one or more core PMU counters overflowed.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>ASCI: Data in the performance counters in the core PMU may include contributions from the direct or indirect operation intel SGX to protect an enclave.</td>
<td>If CPUID.(EAX=07H, ECX=0):EBX[2] = 1</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Ovf_Uncore: Uncore counter overflow status.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 2</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>OvfBuf: DS SAVE area Buffer overflow status.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>CondChgd: status bits of this register has changed.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL Global Performance Counter Control (R/W) Counter increments while the result of ANDing respective enable bit in this MSR with the corresponding OS or USR bits in the general-purpose or fixed counter control MSR is true.</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>EN_PMC0</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EN_PMC1</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>EN_PMC2</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 2</td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>EN_PMCn</td>
<td>If CPUID.0AH: EAX[15:8] &gt; n</td>
<td></td>
</tr>
<tr>
<td>31:n+1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>EN_FIXED_CTR0</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>EN_FIXED_CTR1</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>EN_FIXED_CTR2</td>
<td>If CPUID.0AH: EDX[4:0] &gt; 2</td>
<td></td>
</tr>
<tr>
<td>63:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL Global Performance Counter Overflow Control (R/W)</td>
<td>If CPUID.0AH: EAX[7:0] &gt; 0 &amp; CPUID.0AH: EAX[7:0] &lt;= 3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Set 1 to Clear Ovf_PMC0 bit.</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Set 1 to Clear Ovf_PMC1 bit.</td>
<td>If CPUID.0AH: EAX[15:8] &gt; 1</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Decimal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMC2 bit. If CPUID.0AH: EAX[15:8] &gt; 2</td>
</tr>
<tr>
<td>n</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMCn bit. If CPUID.0AH: EAX[15:8] &gt; n</td>
</tr>
<tr>
<td>31:n</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR0 bit. If CPUID.0AH: EDX[4:0] &gt; 0</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR1 bit. If CPUID.0AH: EDX[4:0] &gt; 1</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR2 bit. If CPUID.0AH: EDX[4:0] &gt; 2</td>
</tr>
<tr>
<td>54:35</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>55</td>
<td></td>
<td></td>
<td>Set 1 to Clear Trace_ToPA_PMI bit. If (CPUID.(EAX=07H, ECX=0):EBX[25] = 1) &amp;&amp; IA32_RTIT_CTL.ToPA = 1</td>
</tr>
<tr>
<td>60:56</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_Uncore bit. 06_2EH</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
<td>Set 1 to Clear OvfBuf: bit. If CPUID.0AH: EAX[7:0] &gt; 0</td>
</tr>
<tr>
<td>63</td>
<td></td>
<td></td>
<td>Set to 1 to clear CondChgd: bit. If CPUID.0AH: EAX[7:0] &gt; 0</td>
</tr>
<tr>
<td>390H 912</td>
<td></td>
<td></td>
<td>IA32_PERF_GLOBAL_STATUS_RESET: Global Performance Counter Overflow Reset Control (R/W) If CPUID.0AH: EAX[7:0] &gt; 3</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMC0 bit. If CPUID.0AH: EAX[15:8] &gt; 0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMC1 bit. If CPUID.0AH: EAX[15:8] &gt; 1</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMC2 bit. If CPUID.0AH: EAX[15:8] &gt; 2</td>
</tr>
<tr>
<td>n</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_PMCn bit. If CPUID.0AH: EAX[15:8] &gt; n</td>
</tr>
<tr>
<td>31:n</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR0 bit. If CPUID.0AH: EDX[4:0] &gt; 0</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR1 bit. If CPUID.0AH: EDX[4:0] &gt; 1</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_FIXED_CTR2 bit. If CPUID.0AH: EDX[4:0] &gt; 2</td>
</tr>
<tr>
<td>54:35</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>55</td>
<td></td>
<td></td>
<td>Set 1 to Clear Trace_ToPA_PMI bit. If (CPUID.(EAX=07H, ECX=0):EBX[25] = 1) &amp;&amp; IA32_RTIT_CTL.ToPA[8] = 1</td>
</tr>
<tr>
<td>57:56</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>58</td>
<td></td>
<td></td>
<td>Set 1 to Clear LBR_Frz bit. If CPUID.0AH: EAX[7:0] &gt; 3</td>
</tr>
<tr>
<td>59</td>
<td></td>
<td></td>
<td>Set 1 to Clear CTR_Frz bit. If CPUID.0AH: EAX[7:0] &gt; 3</td>
</tr>
<tr>
<td>58</td>
<td></td>
<td></td>
<td>Set 1 to Clear ASCI bit. If CPUID.0AH: EAX[7:0] &gt; 3</td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
<td>Set 1 to Clear Ovf_Uncore bit. 06_2EH</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
<td>Set 1 to Clear OvfBuf: bit. If CPUID.0AH: EAX[7:0] &gt; 0</td>
</tr>
<tr>
<td>Register Address</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
<td>Comment</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------------------------------------------------</td>
<td>---------------------</td>
<td>---------</td>
</tr>
<tr>
<td>63</td>
<td>Set to 1 to clear CondChgd: bit. If CPUID.0AH: EAX[7:0] &gt; 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>391H 913</td>
<td>IA32_PERF_GLOBAL_STATUS_SET Global Performance Counter Overflow Set Control (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Set 1 to cause Ovf_PMC0 = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Set 1 to cause Ovf_PMC1 = 1. If CPUID.0AH: EAX[15:8] &gt; 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Set 1 to cause Ovf_PMC2 = 1. If CPUID.0AH: EAX[15:8] &gt; 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>Set 1 to cause Ovf_PMCn = 1. If CPUID.0AH: EAX[15:8] &gt; n</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:n</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Set 1 to cause Ovf_FIXED_CTR0 = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Set 1 to cause Ovf_FIXED_CTR1 = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Set 1 to cause Ovf_FIXED_CTR2 = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>54:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Set 1 to cause Trace_ToPA_PMI = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>57:56</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Set 1 to cause LBR_Frz = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Set 1 to cause CTR_Frz = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Set 1 to cause Ovf_Uncore = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Set 1 to cause OvfBF0 = 1. If CPUID.0AH: EAX[7:0] &gt; 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>392H 914</td>
<td>IA32_PERF_GLOBAL_INUSE Indicator of core perfmon interface is in use (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>IA32_PERFEVTSEL0 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>IA32_PERFEVTSEL1 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>IA32_PERFEVTSEL2 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>n</td>
<td>IA32_PERFEVTSELn in use</td>
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</tr>
<tr>
<td>31:n</td>
<td>Reserved.</td>
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<td></td>
</tr>
<tr>
<td>32</td>
<td>IA32_FIXED_CTR0 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>IA32_FIXED_CTR1 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>IA32_FIXED_CTR2 in use</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62:35</td>
<td>Reserved or Model specific.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>PMI in use.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>IA32_PEBS_ENABLE PEBS Control (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
<td>Comment</td>
</tr>
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<td>------------------</td>
<td>--------------------------------------------------------</td>
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## Model-Specific Registers (MSRs)

Table 35-2. IA-32 Architectural MSRs (Contd.)

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<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
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<tbody>
<tr>
<td>420H 1056</td>
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<td>MC9_CTL</td>
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### Table 35-2. IA-32 Architectural MSRs (Contd.)

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<td>If IA32_MCG_CAP.CNT &gt;22</td>
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<td>If IA32_MCG_CAP.CNT &gt;22</td>
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<td>If IA32_MCG_CAP.CNT &gt;23</td>
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<td>If IA32_MCG_CAP.CNT &gt;24</td>
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<td>If IA32_MCG_CAP.CNT &gt;24</td>
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<td>MC24_MISC</td>
<td>If IA32_MCG_CAP.CNT &gt;24</td>
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<td>If IA32_MCG_CAP.CNT &gt;25</td>
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<td>If IA32_MCG_CAP.CNT &gt;25</td>
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<td>If IA32_MCG_CAP.CNT &gt;25</td>
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### Table 35-2. IA-32 Architectural MSRs (Contd.)

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<td>MC26_MISC</td>
<td>If IA32_MCG_CAP.CNT &gt;26</td>
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<td>46CH</td>
<td>IA32_MC27_CTL</td>
<td>MC27_CTL</td>
<td>If IA32_MCG_CAP.CNT &gt;27</td>
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<td>If IA32_MCG_CAP.CNT &gt;27</td>
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<td>IA32_MC28_CTL</td>
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<td>If IA32_MCG_CAP.CNT &gt;28</td>
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<td>If IA32_MCG_CAP.CNT &gt;28</td>
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<tr>
<td>473H</td>
<td>IA32_MC28_MISC</td>
<td>MC28_MISC</td>
<td>If IA32_MCG_CAP.CNT &gt;28</td>
</tr>
<tr>
<td>480H</td>
<td>IA32_VMX_BASIC</td>
<td>Reporting Register of Basic VMX Capabilities (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>481H</td>
<td>IA32_VMX_PINBASED_CTL</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>482H</td>
<td>IA32_VMX_PROCBASED_CTL</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>483H</td>
<td>IA32_VMX_EXIT_CTL</td>
<td>Capability Reporting Register of VM-exit Controls (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>484H</td>
<td>IA32_VMX_ENTRY_CTL</td>
<td>Capability Reporting Register of VM-entry Controls (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>485H</td>
<td>IA32_VMX_MISC</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>486H</td>
<td>IA32_VMX_CR0_FIXED0</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>487H</td>
<td>IA32_VMX_CR0_FIXED1</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
<tr>
<td>488H</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O)</td>
<td>If CPUID.01H:ECX.{5} = 1</td>
</tr>
</tbody>
</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>4C1H  1217</td>
<td>IA32_A_PMC0</td>
<td>Full Width Writable IA32_PMC0 Alias (R/W)</td>
<td>( If CPUID.0AH:EAX[15:8] &gt; 0 ) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C2H  1218</td>
<td>IA32_A_PMC1</td>
<td>Full Width Writable IA32_PMC1 Alias (R/W)</td>
<td>( If CPUID.0AH:EAX[15:8] &gt; 1 ) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
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</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>4C3H 1219</td>
<td>IA32_A_PMC2</td>
<td>Full Width Writable IA32_PMC2 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 2) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C4H 1220</td>
<td>IA32_A_PMC3</td>
<td>Full Width Writable IA32_PMC3 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 3) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C5H 1221</td>
<td>IA32_A_PMC4</td>
<td>Full Width Writable IA32_PMC4 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 4) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C6H 1222</td>
<td>IA32_A_PMC5</td>
<td>Full Width Writable IA32_PMC5 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 5) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C7H 1223</td>
<td>IA32_A_PMC6</td>
<td>Full Width Writable IA32_PMC6 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 6) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4C8H 1224</td>
<td>IA32_A_PMC7</td>
<td>Full Width Writable IA32_PMC7 Alias (R/W)</td>
<td>(If CPUID.0AH: EAX[15:8] &gt; 7) &amp;&amp; IA32_PERF_CAPABILITIES[13] = 1</td>
</tr>
<tr>
<td>4D0H 1232</td>
<td>IA32_MCG_EXT_CTL</td>
<td>(R/W)</td>
<td>If IA32_MCG_CAP.LMCE_P = 1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>LMCE_EN.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:1</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Lock.</td>
<td>See Section 42.12.3, &quot;Interactions with Authenticated Code Modules (ACMs)&quot;.</td>
</tr>
<tr>
<td></td>
<td>15:1</td>
<td>Reserved.</td>
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</tr>
<tr>
<td></td>
<td>23:16</td>
<td>SGX_SVN_SINIT.</td>
<td>See Section 42.12.3, &quot;Interactions with Authenticated Code Modules (ACMs)&quot;.</td>
</tr>
<tr>
<td></td>
<td>63:24</td>
<td>Reserved.</td>
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</tr>
<tr>
<td>Register Address</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
<td>Comment</td>
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<tr>
<td>------------------</td>
<td>---------------------------------------------------------</td>
<td>---------------------</td>
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</tr>
<tr>
<td></td>
<td>MAXPHYADDR&lt;sup&gt;3&lt;/sup&gt;-7</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:MAXPHYADDR</td>
<td>Base physical address</td>
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</tr>
<tr>
<td></td>
<td>6:0</td>
<td>Reserved</td>
<td></td>
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<tr>
<td></td>
<td>31:7</td>
<td>MaskOrTableOffset</td>
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</tr>
<tr>
<td></td>
<td>63:32</td>
<td>Output Offset</td>
<td></td>
</tr>
<tr>
<td>570H 1392</td>
<td>IA32_RTIT_CTL</td>
<td>Trace Control Register (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[25] = 1)</td>
</tr>
<tr>
<td>0</td>
<td>TraceEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CYCEn</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[11] = 1)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>OS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>User</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5:4</td>
<td>Reserved,</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>FabricEn</td>
<td>If (CPUID.(EAX=07H, ECX=0):ECX[3] = 1)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>CR3 filter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>ToPA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MTCEn</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[3] = 1)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>TSCEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>DisRETC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>BranchEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:14</td>
<td>MTCFreq</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[3] = 1)</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Reserved, MBZ</td>
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### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
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<tbody>
<tr>
<td>Hex</td>
<td>Decimal</td>
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<td></td>
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<tr>
<td>27:24</td>
<td>PSBFreq</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[1] = 1)</td>
<td></td>
</tr>
<tr>
<td>31:28</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35:32</td>
<td>ADDR0_CFG</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 0)</td>
<td></td>
</tr>
<tr>
<td>39:36</td>
<td>ADDR1_CFG</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 1)</td>
<td></td>
</tr>
<tr>
<td>43:40</td>
<td>ADDR2_CFG</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 2)</td>
<td></td>
</tr>
<tr>
<td>47:44</td>
<td>ADDR3_CFG</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 3)</td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>571H 1393</td>
<td>IA32_RTIT_STATUS</td>
<td>Tracing Status Register (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[25] = 1)</td>
</tr>
<tr>
<td>4</td>
<td>FilterEn, (writes ignored)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ContexEn, (writes ignored)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TriggerEn, (writes ignored)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Error</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Stopped</td>
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<td></td>
</tr>
<tr>
<td>31:6</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>48:32</td>
<td>PacketByteCnt</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[1] &gt; 3)</td>
<td></td>
</tr>
<tr>
<td>63:49</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>572H 1394</td>
<td>IA32_RTIT_CR3_MATCH</td>
<td>Trace Filter CR3 Match Register (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[25] = 1)</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:5</td>
<td>CR3[63:5] value to match</td>
<td></td>
<td></td>
</tr>
<tr>
<td>580H 1408</td>
<td>IA32_RTIT_ADDR0_A</td>
<td>Region 0 Start Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 0)</td>
</tr>
<tr>
<td>47:0</td>
<td>Virtual Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td>SignExt_VA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>581H 1409</td>
<td>IA32_RTIT_ADDR0_B</td>
<td>Region 0 End Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 0)</td>
</tr>
<tr>
<td>47:0</td>
<td>Virtual Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td>SignExt_VA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>582H 1410</td>
<td>IA32_RTIT_ADDR1_A</td>
<td>Region 1 Start Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 1)</td>
</tr>
<tr>
<td>47:0</td>
<td>Virtual Address</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td>SignExt_VA</td>
<td></td>
<td></td>
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Table 35-2. IA-32 Architectural MSRs (Contd.)

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<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>583H 1411</td>
<td>IA32_RTIT_ADDR1_B</td>
<td>Region 1 End Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:0 Virtual Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48 SignExt_VA</td>
<td></td>
</tr>
<tr>
<td>584H 1412</td>
<td>IA32_RTIT_ADDR2_A</td>
<td>Region 2 Start Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:0 Virtual Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48 SignExt_VA</td>
<td></td>
</tr>
<tr>
<td>585H 1413</td>
<td>IA32_RTIT_ADDR2_B</td>
<td>Region 2 End Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:0 Virtual Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48 SignExt_VA</td>
<td></td>
</tr>
<tr>
<td>586H 1414</td>
<td>IA32_RTIT_ADDR3_A</td>
<td>Region 3 Start Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:0 Virtual Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48 SignExt_VA</td>
<td></td>
</tr>
<tr>
<td>587H 1415</td>
<td>IA32_RTIT_ADDR3_B</td>
<td>Region 3 End Address (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=1):EAX[2:0] &gt; 3)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:0 Virtual Address</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48 SignExt_VA</td>
<td></td>
</tr>
<tr>
<td>600H 1536</td>
<td>IA32_DS_AREA</td>
<td>DS Save Area (R/W)</td>
<td>Points to the linear address of the first byte of the DS buffer management area, which is used to manage the BTS and PEBS buffers. See Section 18.12.4, “Debug Store (DS) Mechanism.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:0 The linear address of the first byte of the DS buffer management area, if IA-32e mode is active.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>31:0 The linear address of the first byte of the DS buffer management area, if not in IA-32e mode.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:32 Reserved if not in IA-32e mode.</td>
<td></td>
</tr>
<tr>
<td>6E0H 1760</td>
<td>IA32_TSC_DEADLINE</td>
<td>TSC Target of Local APIC’s TSC Deadline Mode (R/W)</td>
<td>If CPUID.01H:ECX.[24] = 1</td>
</tr>
<tr>
<td>770H 1904</td>
<td>IA32_PM_ENABLE</td>
<td>Enable/disable HWP (R/W)</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 HWP_ENABLE (R/W1-Once). See Section 14.4.2, “Enabling HWP”</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:1 Reserved.</td>
<td></td>
</tr>
<tr>
<td>771H 1905</td>
<td>IA32_HWP_CAPABILITIES</td>
<td>HWP Performance Range Enumeration (RO)</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
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</table>
## Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex, Decimal</td>
<td>Highest_Performance</td>
<td>See Section 14.4.3, “HWP Performance Range and Dynamic Capabilities”</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Guaranteed_Performance</td>
<td>See Section 14.4.3, “HWP Performance Range and Dynamic Capabilities”</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td>15:8</td>
<td>Most_Efficient_Performance</td>
<td>See Section 14.4.3, “HWP Performance Range and Dynamic Capabilities”</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td>31:24</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:42</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>773H, 1907</td>
<td>IA32_HWP_INTERRUPT</td>
<td>Control HWP Native Interrupts (R/W)</td>
<td>If CPUID.06H:EAX.[8] = 1</td>
</tr>
<tr>
<td>0</td>
<td>EN_Guaranteed_Performance_Change</td>
<td>See Section 14.4.6, “HWP Notifications”</td>
<td>If CPUID.06H:EAX.[8] = 1</td>
</tr>
<tr>
<td>1</td>
<td>EN_Excursion_Minimum</td>
<td>See Section 14.4.6, “HWP Notifications”</td>
<td>If CPUID.06H:EAX.[8] = 1</td>
</tr>
<tr>
<td>63:2</td>
<td>Reserved.</td>
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</tr>
<tr>
<td>774H, 1908</td>
<td>IA32_HWP_REQUEST</td>
<td>Power Management Control Hints to a Logical Processor (R/W)</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Minimum_Performance</td>
<td>See Section 14.4.4, “Managing HWP”</td>
<td>If CPUID.06H:EAX.[7] = 1</td>
</tr>
<tr>
<td>Hex</td>
<td>Decimal</td>
<td>Architectural MSR Name and bit fields (Former MSR Name)</td>
<td>MSR/Bit Description</td>
</tr>
<tr>
<td>------</td>
<td>---------</td>
<td>----------------------------------------------------------</td>
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</tr>
<tr>
<td>63:43</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>777H</td>
<td>1911</td>
<td>IA32_HWP_STATUS</td>
<td>Log bits indicating changes to Guaranteed &amp; excursions to Minimum (R/W)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Guaranteed_Performance_Change (R/WC0).</td>
<td>See Section 14.4.5, “HWP Feedback”</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Excursion_To_Minimum (R/wCO).</td>
<td>See Section 14.4.5, “HWP Feedback”</td>
</tr>
<tr>
<td>63:3</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>802H</td>
<td>2050</td>
<td>IA32_X2APIC_APICID</td>
<td>x2APIC ID Register (R/O) See x2APIC Specification</td>
</tr>
<tr>
<td>808H</td>
<td>2056</td>
<td>IA32_X2APIC_TPR</td>
<td>x2APIC Task Priority Register (R/W)</td>
</tr>
<tr>
<td>80AH</td>
<td>2058</td>
<td>IA32_X2APIC_PPR</td>
<td>x2APIC Processor Priority Register (R/O)</td>
</tr>
<tr>
<td>80BH</td>
<td>2059</td>
<td>IA32_X2APIC_EOI</td>
<td>x2APIC EOI Register (W/O)</td>
</tr>
<tr>
<td>80DH</td>
<td>2061</td>
<td>IA32_X2APIC_LDR</td>
<td>x2APIC Logical Destination Register (R/O)</td>
</tr>
<tr>
<td>80FH</td>
<td>2063</td>
<td>IA32_X2APIC_SIVR</td>
<td>x2APIC Spurious Interrupt Vector Register (R/w)</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
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<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>810H 2064</td>
<td>IA32_X2APIC_ISR0</td>
<td>x2APIC In-Service Register Bits 31:0 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>811H 2065</td>
<td>IA32_X2APIC_ISR1</td>
<td>x2APIC In-Service Register Bits 63:32 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>812H 2066</td>
<td>IA32_X2APIC_ISR2</td>
<td>x2APIC In-Service Register Bits 95:64 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>813H 2067</td>
<td>IA32_X2APIC_ISR3</td>
<td>x2APIC In-Service Register Bits 127:96 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>814H 2068</td>
<td>IA32_X2APIC_ISR4</td>
<td>x2APIC In-Service Register Bits 159:128 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>815H 2069</td>
<td>IA32_X2APIC_ISR5</td>
<td>x2APIC In-Service Register Bits 191:160 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>816H 2070</td>
<td>IA32_X2APIC_ISR6</td>
<td>x2APIC In-Service Register Bits 223:192 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>817H 2071</td>
<td>IA32_X2APIC_ISR7</td>
<td>x2APIC In-Service Register Bits 255:224 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>818H 2072</td>
<td>IA32_X2APIC_TMR0</td>
<td>x2APIC Trigger Mode Register Bits 31:0 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>819H 2073</td>
<td>IA32_X2APIC_TMR1</td>
<td>x2APIC Trigger Mode Register Bits 63:32 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>81AH 2074</td>
<td>IA32_X2APIC_TMR2</td>
<td>x2APIC Trigger Mode Register Bits 95:64 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>81BH 2075</td>
<td>IA32_X2APIC_TMR3</td>
<td>x2APIC Trigger Mode Register Bits 127:96 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>81CH 2076</td>
<td>IA32_X2APIC_TMR4</td>
<td>x2APIC Trigger Mode Register Bits 159:128 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>81DH 2077</td>
<td>IA32_X2APIC_TMR5</td>
<td>x2APIC Trigger Mode Register Bits 191:160 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
</tbody>
</table>
### Table 35-2. IA-32 Architectural MSRs (Contd.)

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</tr>
</thead>
<tbody>
<tr>
<td>820H 2080</td>
<td>IA32_X2APIC_IRR0</td>
<td>x2APIC Interrupt Request Register Bits 31:0 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>822H 2082</td>
<td>IA32_X2APIC_IRR2</td>
<td>x2APIC Interrupt Request Register Bits 95:64 (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>828H 2088</td>
<td>IA32_X2APIC_ESR</td>
<td>x2APIC Error Status Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>82FH 2095</td>
<td>IA32_X2APIC_LVT_CMCI</td>
<td>x2APIC LVT Corrected Machine Check Interrupt Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>830H 2096</td>
<td>IA32_X2APIC_ICR</td>
<td>x2APIC Interrupt Command Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>832H 2098</td>
<td>IA32_X2APIC_LVT_TIMER</td>
<td>x2APIC LVT Timer Interrupt Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>833H 2099</td>
<td>IA32_X2APIC_LVT_THERMAL</td>
<td>x2APIC LVT Thermal Sensor Interrupt Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>834H 2100</td>
<td>IA32_X2APIC_LVT_PMI</td>
<td>x2APIC LVT Performance Monitor Interrupt Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
</tbody>
</table>
## Table 35-2. IA-32 Architectural MSRs (Contd.)

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</tr>
</thead>
<tbody>
<tr>
<td>835H 2101</td>
<td>IA32_X2APIC_LVT_LINT0</td>
<td>x2APIC LVT LINT0 Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>836H 2102</td>
<td>IA32_X2APIC_LVT_LINT1</td>
<td>x2APIC LVT LINT1 Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>837H 2103</td>
<td>IA32_X2APIC_LVT_ERROR</td>
<td>x2APIC LVT Error Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>838H 2104</td>
<td>IA32_X2APIC_INIT_COUNT</td>
<td>x2APIC Initial Count Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>839H 2105</td>
<td>IA32_X2APIC_CUR_COUNT</td>
<td>x2APIC Current Count Register (R/O)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>83EH 2110</td>
<td>IA32_X2APIC_DIV_CONF</td>
<td>x2APIC Divide Configuration Register (R/W)</td>
<td>If CPUID.01H:ECX.[21] = 1 &amp;&amp; IA32_APIC_BASE.[10] = 1</td>
</tr>
<tr>
<td>C80H 3200</td>
<td>IA32_DEBUG_INTERFACE</td>
<td>Silicon Debug Feature Control (R/W)</td>
<td>If CPUID.01H:ECX.[11] = 1</td>
</tr>
<tr>
<td>0</td>
<td>Enable (R/W)</td>
<td>BIOS set 1 to enable Silicon debug features. Default is 0</td>
<td>If CPUID.01H:ECX.[11] = 1</td>
</tr>
<tr>
<td>29:1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Lock (R/W): If 1, locks any further change to the MSR. The lock bit is set automatically on the first SMI assertion even if not explicitly set by BIOS. Default is 0.</td>
<td>If CPUID.01H:ECX.[11] = 1</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Debug Occurred (R/O): This “sticky bit” is set by hardware to indicate the status of bit 0. Default is 0.</td>
<td>If CPUID.01H:ECX.[11] = 1</td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CB1H 3201</td>
<td>IA32_L3_QOS_CFG</td>
<td>L3 QOS Configuration (R/W)</td>
<td>If (CPUID.(EAX=10H, ECX=1):ECX.[2] = 1)</td>
</tr>
<tr>
<td>0</td>
<td>Enable (R/W)</td>
<td>Set 1 to enable L3 CAT masks and COS to operate in Code and Data Prioritization (CDP) mode</td>
<td></td>
</tr>
<tr>
<td>63:1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C8DH 3213</td>
<td>IA32_QM_EVTSEL</td>
<td>Monitoring Event Select Register (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX.[12] = 1)</td>
</tr>
<tr>
<td>7:0</td>
<td>Event ID: ID of a supported monitoring event to report via IA32_QM_CTR.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 35-2. IA-32 Architectural MSRs (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Architectural MSR Name and bit fields (Former MSR Name)</th>
<th>MSR/Bit Description</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Decimal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31: 8</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>N+31:32</td>
<td>Resource Monitoring ID: ID for monitoring hardware to report monitored data via IA32_QM_CTR.</td>
<td>N = Ceil (Log2 (CPUID.(EAX= 0FH, ECX=0H).EBX[31:0] +1))</td>
<td></td>
</tr>
<tr>
<td>63:N+32</td>
<td>Resource Monitoring ID: ID for monitoring hardware to report monitored data via IA32_QM_CTR.</td>
<td>N = Ceil (Log2 (CPUID.(EAX= 0FH, ECX=0H).EBX[31:0] +1))</td>
<td></td>
</tr>
<tr>
<td>C8EH 3214</td>
<td>IA32_QM_CTR</td>
<td>Monitoring Counter Register (R/O)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[12] = 1 )</td>
</tr>
<tr>
<td>61:0</td>
<td>Resource Monitored Data</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Unavailable: If 1, indicates data for this RMID is not available or not monitored for this resource or RMID.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Error: If 1, indicates and unsupported RMID or event type was written to IA32_PQR_QM_EVTSEL.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C8FH 3215</td>
<td>IA32_PQR_ASSOC</td>
<td>Resource Association Register (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[12] = 1 )</td>
</tr>
<tr>
<td>N-1:0</td>
<td>Resource Monitoring ID (R/W): ID for monitoring hardware to track internal operation, e.g. memory access.</td>
<td>N = Ceil (Log2 (CPUID.(EAX= 0FH, ECX=0H).EBX[31:0] +1))</td>
<td></td>
</tr>
<tr>
<td>31:N</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>COS (R/W). The class of service (COS) to enforce (on writes); returns the current COS when read.</td>
<td>If (CPUID.(EAX=07H, ECX=0):EBX[15] = 1 )</td>
<td></td>
</tr>
<tr>
<td>C8FH - D8FH</td>
<td>Reserved MSR Address Space for Platform Enforcement Mask Registers</td>
<td>See Section 17.16.3.1, “Enumeration and Detection Support of Cache Allocation Technology”</td>
<td></td>
</tr>
<tr>
<td>C90H - D8FH</td>
<td>Reserved MSR Address Space for Platform Enforcement Mask Registers</td>
<td>See Section 17.16.3.1, “Enumeration and Detection Support of Cache Allocation Technology”</td>
<td></td>
</tr>
<tr>
<td>C90H 3216</td>
<td>IA32_L3_MASK_0</td>
<td>L3 CQE Mask for COS0 (R/W)</td>
<td>If (CPUID.(EAX=10H, ECX=0H):EBX[1] != 0)</td>
</tr>
<tr>
<td>31:0</td>
<td>Capacity Bit Mask (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C90H+n</td>
<td>IA32_L3_MASK_n</td>
<td>L3 CQE Mask for COSn (R/W)</td>
<td>n = CPUID.(EAX=10H, ECX=1H):EDX[15:0]</td>
</tr>
<tr>
<td>31:0</td>
<td>Capacity Bit Mask (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D90H 3472</td>
<td>IA32_BNDCFGS</td>
<td>Supervisor State of MPX Configuration. (R/W)</td>
<td>If (CPUID.(EAX=07H, ECX=0H):EBX[14] = 1)</td>
</tr>
<tr>
<td>0</td>
<td>EN: Enable Intel MPX in supervisor mode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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</tr>
</thead>
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<tr>
<td>Hex</td>
<td>Decimal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td><strong>BNDPRESERVE</strong>: Preserve the bounds registers for near branch instructions in the absence of the BND prefix</td>
</tr>
<tr>
<td>11:2</td>
<td></td>
<td></td>
<td>Reserved, must be 0</td>
</tr>
<tr>
<td>63:12</td>
<td></td>
<td></td>
<td>Base Address of Bound Directory.</td>
</tr>
<tr>
<td>DA0H</td>
<td>3488</td>
<td><strong>IA32_XSS</strong></td>
<td>Extended Supervisor State Mask (R/W)</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>Trace Packet Configuration State (R/W)</td>
</tr>
<tr>
<td>63:9</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>DB0H</td>
<td>3504</td>
<td><strong>IA32_PKG_HDC_CTL</strong></td>
<td>Package Level Enable/disable HDC (R/W)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>HDC_Pkg_Enable (R/W)</td>
</tr>
<tr>
<td>63:1</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>DB1H</td>
<td>3505</td>
<td><strong>IA32_PM_CTL1</strong></td>
<td>Enable/disable HWP (R/W)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>HDC_Allow_Block (R/W)</td>
</tr>
<tr>
<td>63:1</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>DB2H</td>
<td>3506</td>
<td><strong>IA32_THREADSTALL</strong></td>
<td>Per-Logical_Processor HDC Idle Residency (R/O)</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Stall_Cycle_Cnt (R/W)</td>
</tr>
<tr>
<td>4000_0000H - 4000_00FFH</td>
<td></td>
<td></td>
<td>Reserved MSR Address Space</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>All existing and future processors will not implement MSR in this range.</td>
</tr>
<tr>
<td>C000_0080H</td>
<td></td>
<td><strong>IA32_EFER</strong></td>
<td>Extended Feature Enables</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>SYSCALL Enable: IA32_EFER.SCE (R/W)</td>
</tr>
<tr>
<td>7:1</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
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<tbody>
<tr>
<td>8</td>
<td>IA-32e Mode Enable: IA32_EFER.LME (R/W)</td>
<td>Enables IA-32e mode operation.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>9 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>IA-32e Mode Active: IA32_EFER.LMA (R)</td>
<td>Indicates IA-32e mode is active when set.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Execute Disable Bit Enable: IA32_EFER.NXE (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:12 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C000_0081H</td>
<td>IA32_STAR</td>
<td>System Call Target Address (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0082H</td>
<td>IA32_LSTAR</td>
<td>IA-32e Mode System Call Target Address (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0084H</td>
<td>IA32_FMASK</td>
<td>System Call Flag Mask (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0100H</td>
<td>IA32_FS_BASE</td>
<td>Map of BASE Address of FS (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0101H</td>
<td>IA32_GS_BASE</td>
<td>Map of BASE Address of GS (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0102H</td>
<td>IA32_KERNEL_GS_BASE</td>
<td>Swap Target of BASE Address of GS (R/W)</td>
<td>If CPUID.80000001:EDX[29] = 1</td>
</tr>
<tr>
<td>C000_0103H</td>
<td>IA32_TSC_AUX</td>
<td>Auxiliary TSC (Rw)</td>
<td>If CPUID.80000001:EDX[27] = 1</td>
</tr>
<tr>
<td></td>
<td>31:0 Reserved.</td>
<td>AUX: Auxiliary signature of TSC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:32 Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. In processors based on Intel NetBurst® microarchitecture, MSR addresses 180H-197H are supported, software must treat them as model-specific. Starting with Intel Core Duo processors, MSR addresses 180H-185H, 188H-197H are reserved.
2. The *ADDR MSRs may or may not be present; this depends on flag settings in IA32_MCi_STATUS. See Section 15.3.2.3 and Section 15.3.2.4 for more information.
3. MAXPHYADDR is reported by CPUID.80000008H:EAX[7:0].

### 35.2 MSRS IN THE INTEL® CORE™ 2 PROCESSOR FAMILY

Table 35-3 lists model-specific registers (MSRs) for Intel Core 2 processor family and for Intel Xeon processors based on Intel Core microarchitecture, architectural MSR addresses are also included in Table 35-3. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_0FH, see Table 35-1.
MSRs listed in Table 35-2 and Table 35-3 are also supported by processors based on the Enhanced Intel Core micro-architecture. Processors based on the Enhanced Intel Core microarchitecture have the CPUID signature DisplayFamily_DisplayModel of 06_17H.

The column “Shared/Unique” applies to multi-core processors based on Intel Core microarchitecture. “Unique” means each processor core has a separate MSR, or a bit field in an MSR governs only a core independently. “Shared” means the MSR or the bit field in an MSR address governs the operation of both processor cores.

### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H 0</td>
<td>IA32_PS_MC_ADDR</td>
<td>Unique</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H 1</td>
<td>IA32_PS_MC_TYPE</td>
<td>Unique</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>6H 6</td>
<td>IA32_MONITOR_FILTER_SIZE</td>
<td>Unique</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination,” and Table 35-2.</td>
</tr>
<tr>
<td>10H 16</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>Unique</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H 23</td>
<td>IA32_PLATFORM_ID</td>
<td>Shared</td>
<td>Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17H 23</td>
<td>MSRPLATFORM_ID</td>
<td>Shared</td>
<td>Model Specific Platform ID (R)</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>12:8</td>
<td></td>
<td>Maximum Qualified Ratio (R)</td>
<td>The maximum allowed bus ratio.</td>
</tr>
<tr>
<td>49:13</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>52:50</td>
<td></td>
<td>See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>63:53</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1BH 27</td>
<td>IA32_APIC_BASE</td>
<td>Unique</td>
<td>See Section 10.4.4, “Local APIC Status and Location.” and Table 35-2.</td>
</tr>
<tr>
<td>2AH 42</td>
<td>MSR_EBL_CR_POWERON</td>
<td>Shared</td>
<td>Processor Hard Power-On Configuration (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Enables and disables processor features; (R) indicates current processor configuration.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Data Error Checking Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: Not all processor implements R/W.</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Response Error Checking Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: Not all processor implements R/W.</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>MCERR# Drive Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: Not all processor implements R/W.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Address Parity Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Note: Not all processor implements R/W.</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 7 | BINIT# Driver Enable (R/W) | | 1 = Enabled; 0 = Disabled  
Note: Not all processor implements R/W. |
| 8 | Output Tri-state Enabled (R/O) | | 1 = Enabled; 0 = Disabled |
| 9 | Execute BIST (R/O) | | 1 = Enabled; 0 = Disabled |
| 10 | MCERR# Observation Enabled (R/O) | | 1 = Enabled; 0 = Disabled |
| 11 | Intel TXT Capable Chipset. (R/O) | | 1 = Present; 0 = Not Present |
| 12 | BINIT# Observation Enabled (R/O) | | 1 = Enabled; 0 = Disabled |
| 13 | Reserved. | | |
| 14 | 1 MByte Power on Reset Vector (R/O) | | 1 = 1 MByte; 0 = 4 GBytes |
| 15 | Reserved. | | |
| 17:16 | APIC Cluster ID (R/O) | | |
| 18 | N/2 Non-Integer Bus Ratio (R/O) | | 0 = Integer ratio; 1 = Non-integer ratio |
| 19 | Reserved. | | |
| 21:20 | Symmetric Arbitration ID (R/O) | | |
| 26:22 | Integer Bus Frequency Ratio (R/O) | | |
| 3AH 58 | MSR_FEATURE_CONTROL | Unique | Control Features in Intel 64Processor (R/W)  
See Table 35-2. |
| 3 | SMRR Enable (R/WL) | Unique |  
When this bit is set and the lock bit is set makes the  
SMRR_PHYS_BASE and SMRR_PHYS_MASK registers read visible and writeable while in SMM. |
| 40H 64 | MSR_LASTBRANCH_0_FROM_IP | Unique | Last Branch Record 0 From IP (R/W)  
One of four pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction for one of the last four branches, exceptions, or interrupts taken by the processor. See also:  
• Last Branch Record Stack TOS at 1C9H  
• Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors)” |
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 41H 65           | MSR_LASTBRANCH_1_FROM_IP | Unique | Last Branch Record 1 From IP (R/W)  
See description of MSR_LASTBRANCH_0_FROM_IP. |
| 42H 66           | MSR_LASTBRANCH_2_FROM_IP | Unique | Last Branch Record 2 From IP (R/W)  
See description of MSR_LASTBRANCH_0_FROM_IP. |
| 43H 67           | MSR_LASTBRANCH_3_FROM_IP | Unique | Last Branch Record 3 From IP (R/W)  
See description of MSR_LASTBRANCH_0_FROM_IP. |
| 60H 96           | MSR_LASTBRANCH_0_TO_IP | Unique | Last Branch Record 0 To IP (R/W)  
One of four pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the destination instruction for one of the last four branches, exceptions, or interrupts taken by the processor. |
| 61H 97           | MSR_LASTBRANCH_1_TO_IP | Unique | Last Branch Record 1 To IP (R/W)  
See description of MSR_LASTBRANCH_0_TO_IP. |
| 62H 98           | MSR_LASTBRANCH_2_TO_IP | Unique | Last Branch Record 2 To IP (R/W)  
See description of MSR_LASTBRANCH_0_TO_IP. |
| 63H 99           | MSR_LASTBRANCH_3_TO_IP | Unique | Last Branch Record 3 To IP (R/W)  
See description of MSR_LASTBRANCH_0_TO_IP. |
| 79H 121          | IA32_BIOS_UPDT_TRIG | Unique | BIOS Update Trigger Register (W)  
See Table 35-2. |
| 8BH 139          | IA32_BIOS_SIGN_ID | Unique | BIOS Update Signature ID (RO)  
See Table 35-2. |
| A0H 160          | MSR_SMRR_PHYSBASE | Unique | System Management Mode Base Address register (WO in SMM)  
Model-specific implementation of SMRR-like interface, read visible and write only in SMM.  
11:0 | Reserved.  
31:12 | PhysBase. SMRR physical Base Address.  
63:32 | Reserved. |
| A1H 161          | MSR_SMRR_PHYSMASK | Unique | System Management Mode Physical Address Mask register (WO in SMM)  
Model-specific implementation of SMRR-like interface, read visible and write only in SMM.  
10:0 | Reserved.  
11 | Valid. Physical address base and range mask are valid.  
31:12 | PhysMask. SMRR physical address range mask.  
63:32 | Reserved. |
| C1H 193          | IA32_PMC0 | Unique | Performance Counter Register  
See Table 35-2. |
| C2H 194          | IA32_PMC1 | Unique | Performance Counter Register  
See Table 35-2. |
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Shared/ Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDH</td>
<td>205</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td>Scaleable Bus Speed (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field indicates the intended scaleable bus clock speed for processors based on Intel Core microarchitecture:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2:0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 101B: 100 MHz (FSB 400)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 001B: 133 MHz (FSB 533)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 011B: 167 MHz (FSB 667)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 010B: 200 MHz (FSB 800)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 000B: 267 MHz (FSB 1067)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 100B: 333 MHz (FSB 1333)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>133.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 001B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>166.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 011B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>266.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 000B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>333.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 100B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:3</td>
</tr>
<tr>
<td>CDH</td>
<td>205</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td>Scaleable Bus Speed (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field indicates the intended scaleable bus clock speed for processors based on Enhanced Intel Core microarchitecture:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2:0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 101B: 100 MHz (FSB 400)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 001B: 133 MHz (FSB 533)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 011B: 167 MHz (FSB 667)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 010B: 200 MHz (FSB 800)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 000B: 267 MHz (FSB 1067)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 110B: 400 MHz (FSB 1600)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>133.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 001B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>166.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 011B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>266.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 110B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>333.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 111B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:3</td>
</tr>
<tr>
<td>E7H</td>
<td>231</td>
<td>IA32_MPERF</td>
<td>Unique</td>
<td>Maximum Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>E8H</td>
<td>232</td>
<td>IA32_APERF</td>
<td>Unique</td>
<td>Actual Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>F6H</td>
<td>254</td>
<td>IA32_MTRRCAP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Unique</td>
<td>SMRR Capability Using MSR 0A0H and 0A1H (R)</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Shared/ Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>11EH</td>
<td>281</td>
<td>MSR_BBL_CR_CTL3</td>
<td>Shared</td>
<td>L2 Hardware Enabled (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = If the L2 is hardware-enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = Indicates if the L2 is hardware-disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>7:1 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L2 Enabled (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = L2 cache has been initialized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Until this bit is set the processor will not respond to the WBINVD instruction or the assertion of the FLUSH# input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>22:9 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>L2 Not Present (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = L2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = L2 Not Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:24 Reserved.</td>
</tr>
<tr>
<td>174H</td>
<td>372</td>
<td>IA32_SYSENTER_CS</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H</td>
<td>373</td>
<td>IA32_SYSENTER_ESP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H</td>
<td>374</td>
<td>IA32_SYSENTER_EIP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H</td>
<td>377</td>
<td>IA32_MCG_CAP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH</td>
<td>378</td>
<td>IA32_MCG_STATUS</td>
<td>Unique</td>
<td>RIPV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) can be used to restart the program. If cleared, the program cannot be reliably restarted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>EIPV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) is directly associated with the error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MCIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that a machine check has been generated. If a second machine check is detected while this bit is still set, the processor enters a shutdown state. Software should write this bit to 0 after processing a machine check exception.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:3 Reserved.</td>
</tr>
<tr>
<td>186H</td>
<td>390</td>
<td>IA32 PERF_EVTSEL0</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>187H</td>
<td>391</td>
<td>IA32 PERF_EVTSEL1</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H</td>
<td>408</td>
<td>IA32 PERF_STATUS</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H</td>
<td>408</td>
<td>MSR PERF STATUS</td>
<td>Shared</td>
<td>Current Performance State Value.</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30:16</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>31</td>
<td>XE Operation (R/O)</td>
<td></td>
<td>If set, XE operation is enabled. Default is cleared.</td>
</tr>
<tr>
<td>39:32</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>44:40</td>
<td>Maximum Bus Ratio (R/O)</td>
<td></td>
<td>Indicates maximum bus ratio configured for the processor.</td>
</tr>
<tr>
<td>45</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>46</td>
<td>Non-Integer Bus Ratio (R/O)</td>
<td></td>
<td>Indicates non-integer bus ratio is enabled. Applies processors based on Enhanced Intel Core microarchitecture.</td>
</tr>
<tr>
<td>63:47</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Unique</td>
<td>Clock Modulation (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IA32_CLOCK_MODULATION MSR was originally named IA32_THERM_CONTROL MSR.</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Unique</td>
<td>Thermal Interrupt Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Unique</td>
<td>Thermal Monitor Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19DH 413</td>
<td>MSR_THERM2_CTL</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TM_SELECT (R/W)</td>
<td></td>
<td>Mode of automatic thermal monitor:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Thermal Monitor 1 (thermally-initiated on-die modulation of the stop-clock duty cycle)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Thermal Monitor 2 (thermally-initiated frequency transitions)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If bit 3 of the IA32_MISC_ENABLE register is cleared, TM_SELECT has no effect. Neither TM1 nor TM2 are enabled.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>Unique</td>
<td>Enable Misc. Processor Features (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td>0</td>
<td>Fast-Strings Enable</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2:1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Automatic Thermal Control Circuit Enable (R/W)</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>6:4</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>Shared</td>
<td>Performance Monitoring Available (R)</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>Hardware Prefetcher Disable (R/W)</td>
<td>When set, disables the hardware prefetcher operation on streams of data. When clear (default), enables the prefetch queue. Disabling of the hardware prefetcher may impact processor performance.</td>
</tr>
<tr>
<td>10</td>
<td>Shared</td>
<td>FERR# Multiplexing Enable (R/W)</td>
<td>1 = FERR# asserted by the processor to indicate a pending break event within the processor 0 = Indicates compatible FERR# signaling behavior This bit must be set to 1 to support XAPIC interrupt model usage.</td>
</tr>
<tr>
<td>11</td>
<td>Shared</td>
<td>Branch Trace Storage Unavailable (RO)</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>12</td>
<td>Shared</td>
<td>Precise Event Based Sampling Unavailable (RO)</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>13</td>
<td>Shared</td>
<td>TM2 Enable (R/W)</td>
<td>When this bit is set (1) and the thermal sensor indicates that the die temperature is at the pre-determined threshold, the Thermal Monitor 2 mechanism is engaged. TM2 will reduce the bus to core ratio and voltage according to the value last written to MSR_THERM2_CTL bits 15:0. When this bit is clear (0, default), the processor does not change the VID signals or the bus to core ratio when the processor enters a thermally managed state. The BIOS must enable this feature if the TM2 feature flag (CPUID.1:ECX[8]) is set; if the TM2 feature flag is not set, this feature is not supported and BIOS must not alter the contents of the TM2 bit location. The processor is operating out of specification if both this bit and the TM1 bit are set to 0.</td>
</tr>
<tr>
<td>15:14</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Shared</td>
<td>Enhanced Intel SpeedStep Technology Enable (R/W)</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>18</td>
<td>Shared</td>
<td>ENABLE MONITOR FSM (R/W)</td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>Adjacent Cache Line Prefetch Disable (R/W)</td>
<td>Shared</td>
<td>When set to 1, the processor fetches the cache line that contains data currently required by the processor. When set to 0, the processor fetches cache lines that comprise a cache line pair (128 bytes). Single processor platforms should not set this bit. Server platforms should set or clear this bit based on platform performance observed in validation and testing. BIOS may contain a setup option that controls the setting of this bit.</td>
</tr>
</tbody>
</table>
| 20               | Enhanced Intel SpeedStep Technology Select Lock (R/W0) | Shared | When set, this bit causes the following bits to become read-only:  
• Enhanced Intel SpeedStep Technology Select Lock (this bit),  
• Enhanced Intel SpeedStep Technology Enable bit.  
The bit must be set before an Enhanced Intel SpeedStep Technology transition is requested. This bit is cleared on reset. |
| 23               | xTPR Message Disable (R/W) | Shared | See Table 35-2. |
| 33:24            | Reserved.           | Unique        | See Table 35-2. |
| 34               | XD Bit Disable (R/W) | Unique        | See Table 35-2. |
| 36:35            | Reserved.           | Unique        | See Table 35-2. |
| 37               | DCU Prefetcher Disable (R/W) | Unique | When set to 1, The DCU L1 data cache prefetcher is disabled. The default value after reset is 0. BIOS may write ‘1’ to disable this feature.  
The DCU prefetcher is an L1 data cache prefetcher. When the DCU prefetcher detects multiple loads from the same line done within a time limit, the DCU prefetcher assumes the next line will be required. The next line is prefetched in to the L1 data cache from memory or L2. |
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>38</td>
<td>IDA Disable (R/w)</td>
<td>Shared</td>
<td>When set to 1 on processors that support IDA, the Intel Dynamic Acceleration feature (IDA) is disabled and the IDA_Enable feature flag will be clear (CPUID.06H: EAX[1]=0). When set to a 0 on processors that support IDA, CPUID.06H: EAX[1] reports the processor’s support of IDA is enabled. <strong>Note</strong>: the power-on default value is used by BIOS to detect hardware support of IDA. If power-on default value is 1, IDA is available in the processor. If power-on default value is 0, IDA is not available.</td>
</tr>
<tr>
<td>39</td>
<td>IP Prefetcher Disable (R/w)</td>
<td>Unique</td>
<td>When set to 1, The IP prefetcher is disabled. The default value after reset is 0. BIOS may write ‘1’ to disable this feature. The IP prefetcher is an L1 data cache prefetcher. The IP prefetcher looks for sequential load history to determine whether to prefetch the next expected data into the L1 cache from memory or L2.</td>
</tr>
<tr>
<td>63:40</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1C9H 457</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Unique</td>
<td>Last Branch Record Stack TOS (R/w) Contains an index (bits 0-3) that points to the MSR containing the most recent branch record. See MSR_LASTBRANCH_0_FROM_IP (at 40H).</td>
</tr>
<tr>
<td>1D9H 473</td>
<td>IA32_DEBUGCTL</td>
<td>Unique</td>
<td>Debug Control (R/w) See Table 35-2</td>
</tr>
<tr>
<td>1DDH 477</td>
<td>MSR_LER_FROM_LIP</td>
<td>Unique</td>
<td>Last Exception Record From Linear IP (R) Contains a pointer to the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>1DEH 478</td>
<td>MSR_LER_TO_LIP</td>
<td>Unique</td>
<td>Last Exception Record To Linear IP (R) This area contains a pointer to the target of the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>200H 512</td>
<td>IA32_MTRR_PHYSBASE0</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>201H 513</td>
<td>IA32_MTRR_PHYSMASK0</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>202H 514</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>203H 515</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>204H 516</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>205H 517</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>206H 518</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>207H 519</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>208H 520</td>
<td>IA32_MTRR_PHYSBASE4</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>209H 521</td>
<td>IA32_MTRR_PHYSMASK4</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

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<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20AH 522</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20CH 524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>250H 592</td>
<td>IA32_MTRR_FIX64K_00000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>269H 617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26AH 618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26BH 619</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26CH 620</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26DH 621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26EH 622</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26FH 623</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>277H 631</td>
<td>IA32_PAT</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>Unique</td>
<td>Default Memory Types (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>309H 777</td>
<td>IA32_FIXED_CTR0</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>309H 777</td>
<td>MSR_PERF_FIXED_CTR0</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
</tr>
<tr>
<td>30AH 778</td>
<td>IA32_FIXED_CTR1</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>30AH 778</td>
<td>MSR_PERF_FIXED_CTR1</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>30BH 779</td>
<td>IA32_FIXED_CTR2</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>30BH 779</td>
<td>MSR_PERF_FIXED_CTR2</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
</tr>
<tr>
<td>345H 837</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>Unique</td>
<td>See Table 35-2. See Section 17.4.1, “IA32_DEBUGCTL MSR.”</td>
</tr>
<tr>
<td>345H 837</td>
<td>MSR_PERF_CAPABILITIES</td>
<td>Unique</td>
<td>RO. This applies to processors that do not support architectural perfmon version 2.</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/ Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex  Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5:0</td>
<td>LBR Format. See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>PEBS Record Format.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PEBSSaveArchRegs. See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38DH 909</td>
<td>IA32_FIXED_CTR_CTRL Unique</td>
<td></td>
<td>Fixed-Function-Counter Control Register (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>38DH 909</td>
<td>MSR_PERF_FIXED_CTR_CTRL Unique</td>
<td></td>
<td>Fixed-Function-Counter Control Register (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>38EH 910</td>
<td>IA32_PERF_GLOBAL_STAUS Unique</td>
<td></td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38EH 910</td>
<td>MSR_PERF_GLOBAL_STAUS Unique</td>
<td></td>
<td>See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL Unique</td>
<td></td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38FH 911</td>
<td>MSR_PERF_GLOBAL_CTRL Unique</td>
<td></td>
<td>See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL Unique</td>
<td></td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>390H 912</td>
<td>MSR_PERF_GLOBAL_OVF_CTRL Unique</td>
<td></td>
<td>See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEBS_ENABLE Unique</td>
<td></td>
<td>See Table 35-2. See Section 18.4.4, “Precise Event Based Sampling (PEBS).”</td>
</tr>
<tr>
<td>0</td>
<td>Enable PEBS on IA32_PERF_CTRL. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>400H 1024</td>
<td>IA32_MC0_CTL Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC0_STATUS MSRs.”</td>
</tr>
<tr>
<td>401H 1025</td>
<td>IA32_MC0_STATUS Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC0_STATUS MSRs.”</td>
</tr>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR Unique</td>
<td></td>
<td>See Section 15.3.2.3, “IA32_MC0_ADDR MSRs.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The IA32_MC0_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the IA32_MC0_STATUS register is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When not implemented in the processor, all reads and writes to this MSR will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC1_CTL MSRs.”</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC1_STATUS MSRs.”</td>
</tr>
<tr>
<td>406H 1030</td>
<td>IA32_MC1_ADDR Unique</td>
<td></td>
<td>See Section 15.3.2.3, “IA32_MC1_ADDR MSRs.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The IA32_MC1_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the IA32_MC1_STATUS register is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When not implemented in the processor, all reads and writes to this MSR will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC2_CTL MSRs.”</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS Unique</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MC2_STATUS MSRs.”</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>40AH 1034</td>
<td>IA32_MC2_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>40CH 1036</td>
<td>MSR_MC4_CTL</td>
<td>Unique</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>40DH 1037</td>
<td>MSR_MC4_STATUS</td>
<td>Unique</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.”</td>
</tr>
<tr>
<td>40EH 1038</td>
<td>MSR_MC4_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The MSR_MC4_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC4_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>410H 1040</td>
<td>MSR_MC3_CTL</td>
<td></td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>411H 1041</td>
<td>MSR_MC3_STATUS</td>
<td>Unique</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.”</td>
</tr>
<tr>
<td>412H 1042</td>
<td>MSR_MC3_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The MSR_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>413H 1043</td>
<td>MSR_MC3_MISC</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>414H 1044</td>
<td>MSR_MC5_CTL</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>415H 1045</td>
<td>MSR_MC5_STATUS</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>416H 1046</td>
<td>MSR_MC5_ADDR</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>417H 1047</td>
<td>MSR_MC5_MISC</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>419H 1045</td>
<td>MSR_MC6_STATUS</td>
<td>Unique</td>
<td>Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.” and Chapter 23.</td>
</tr>
<tr>
<td>480H 1152</td>
<td>IA32_VMX_BASIC</td>
<td>Unique</td>
<td>Reporting Register of Basic VMX Capabilities (R/O) See Table 35-2. See Appendix A.1, “Basic VMX Information.”</td>
</tr>
<tr>
<td>481H 1153</td>
<td>IA32_VMX_PINBASED_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O) See Table 35-2. See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>482H 1154</td>
<td>IA32_VMX_PROCBASED_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O) See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
</tbody>
</table>
### Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>483H  1155</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of VM-exit Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.4, “VM-Exit Controls.”</td>
</tr>
<tr>
<td>484H  1156</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of VM-entry Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.5, “VM-Entry Controls.”</td>
</tr>
<tr>
<td>485H  1157</td>
<td>IA32_VMX_MISC</td>
<td>Unique</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.6, “Miscellaneous Data.”</td>
</tr>
<tr>
<td>486H  1158</td>
<td>IA32_VMX_CR0_FIXED0</td>
<td>Unique</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CR0.”</td>
</tr>
<tr>
<td>487H  1159</td>
<td>IA32_VMX_CR0_FIXED1</td>
<td>Unique</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CR0.”</td>
</tr>
<tr>
<td>488H  1160</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Unique</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.8, “VMX-Fixed Bits in CR4.”</td>
</tr>
<tr>
<td>489H  1161</td>
<td>IA32_VMX_CR4_FIXED1</td>
<td>Unique</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.8, “VMX-Fixed Bits in CR4.”</td>
</tr>
<tr>
<td>48AH  1162</td>
<td>IA32_VMX_VMCS_ENUM</td>
<td>Unique</td>
<td>Capability Reporting Register of VMCS Field Enumeration (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.9, “VMCS Enumeration.”</td>
</tr>
<tr>
<td>48BH  1163</td>
<td>IA32_VMX_PROCBASED_CTLS2</td>
<td>Unique</td>
<td>Capability Reporting Register of Secondary Processor-based VM-execution Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>600H  1536</td>
<td>IA32_DS_AREA</td>
<td>Unique</td>
<td>DS Save Area (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>107CC H</td>
<td>MSR_EMON_L3_CTR_CTL0</td>
<td>Unique</td>
<td>GBUSQ Event Control/Counter Register (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107CD H</td>
<td>MSR_EMON_L3_CTR_CTL1</td>
<td>Unique</td>
<td>GBUSQ Event Control/Counter Register (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107CE H</td>
<td>MSR_EMON_L3_CTR_CTL2</td>
<td>Unique</td>
<td>GSNPQ Event Control/Counter Register (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
</tbody>
</table>
Table 35-3. MSRs in Processors Based on Intel® Core™ Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>107CFH</td>
<td>MSR_EMON_L3_CTR_CTL3</td>
<td>Unique</td>
<td>GSNPO Event Control/Counter Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107D0H</td>
<td>MSR_EMON_L3_CTR_CTL4</td>
<td>Unique</td>
<td>FSB Event Control/Counter Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107D1H</td>
<td>MSR_EMON_L3_CTR_CTL5</td>
<td>Unique</td>
<td>FSB Event Control/Counter Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107D2H</td>
<td>MSR_EMON_L3_CTR_CTL6</td>
<td>Unique</td>
<td>FSB Event Control/Counter Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107D3H</td>
<td>MSR_EMON_L3_CTR_CTL7</td>
<td>Unique</td>
<td>FSB Event Control/Counter Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>107D8H</td>
<td>MSR_EMON_L3_GL_CTL</td>
<td>Unique</td>
<td>L3/FSB Common Control Register (R/w) Apply to Intel Xeon processor 7400 series (processor signature 06_1D) only. See Section 17.2.2</td>
</tr>
<tr>
<td>C000_0080H</td>
<td>IA32_EFER</td>
<td>Unique</td>
<td>Extended Feature Enables See Table 35-2.</td>
</tr>
<tr>
<td>C000_0081H</td>
<td>IA32_STAR</td>
<td>Unique</td>
<td>System Call Target Address (R/w) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0082H</td>
<td>IA32_LSTAR</td>
<td>Unique</td>
<td>IA-32e Mode System Call Target Address (R/w) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0084H</td>
<td>IA32_FMASK</td>
<td>Unique</td>
<td>System Call Flag Mask (R/w) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0100H</td>
<td>IA32_FS_BASE</td>
<td>Unique</td>
<td>Map of BASE Address of FS (R/w) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0101H</td>
<td>IA32_GS_BASE</td>
<td>Unique</td>
<td>Map of BASE Address of GS (R/w) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0102H</td>
<td>IA32_KERNEL_GSBASE</td>
<td>Unique</td>
<td>Swap Target of BASE Address of GS (R/w) See Table 35-2.</td>
</tr>
</tbody>
</table>

35.3 MSRS IN THE 45 NM AND 32 NM INTEL® ATOM™ PROCESSOR FAMILY

Table 35-4 lists model-specific registers (MSRs) for 45 nm and 32 nm Intel Atom processors, architectural MSR addresses are also included in Table 35-4. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_1CH, 06_26H, 06_27H, 06_35H and 06_36H; see Table 35-1.

The column “Shared/Unique” applies to logical processors sharing the same core in processors based on the Intel Atom microarchitecture. “Unique” means each logical processor has a separate MSR, or a bit field in an MSR.
governs only a logical processor. "Shared" means the MSR or the bit field in an MSR address governs the operation of both logical processors in the same core.

### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H 0</td>
<td>IA32_P5_MC_ADDR</td>
<td>Shared</td>
<td>See Section 35.20, &quot;MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H 1</td>
<td>IA32_P5_MC_TYPE</td>
<td>Shared</td>
<td>See Section 35.20, &quot;MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>6H 6</td>
<td>IA32_MONITOR_FILTER_SIZE</td>
<td>Unique</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination.” and Table 35-2</td>
</tr>
<tr>
<td>10H 16</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>Unique</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H 23</td>
<td>IA32_PLATFORM_ID</td>
<td>Shared</td>
<td>Platform ID (R)</td>
</tr>
<tr>
<td>17H 23</td>
<td>MSR_PLATFORM_ID</td>
<td>Shared</td>
<td>Model Specific Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>12:8</td>
<td>Maximum Qualified Ratio (R)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The maximum allowed bus ratio.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:13</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1BH 27</td>
<td>IA32_APIC_BASE</td>
<td>Unique</td>
<td>See Section 10.4.4, “Local APIC Status and Location,” and Table 35-2.</td>
</tr>
<tr>
<td>2AH 42</td>
<td>MSR_EBL_CR_POWERON</td>
<td>Shared</td>
<td>Processor Hard Power-On Configuration (R/W) Enables and disables processor features; (R) indicates current processor configuration.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Data Error Checking Enable (R/W) 1 = Enabled; 0 = Disabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Always 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Response Error Checking Enable (R/W) 1 = Enabled; 0 = Disabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Always 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>AERR# Drive Enable (R/W) 1 = Enabled; 0 = Disabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Always 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>BERR# Enable for initiator bus requests (R/W) 1 = Enabled; 0 = Disabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Always 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>BINIT# Driver Enable (R/W) 1 = Enabled; 0 = Disabled</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Always 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>Reserved.</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Execute BIST (R/O)</td>
<td>Unique</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td>10</td>
<td>AERR# Observation Enabled (R/O)</td>
<td>Unique</td>
<td>1 = Enabled; 0 = Disabled Always 0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved.</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>BINIT# Observation Enabled (R/O)</td>
<td>Unique</td>
<td>1 = Enabled; 0 = Disabled Always 0.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved.</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>1 MByte Power on Reset Vector (R/O)</td>
<td>Unique</td>
<td>1 = 1 MByte; 0 = 4 GBytes</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>17:16</td>
<td>APIC Cluster ID (R/O)</td>
<td>Unique</td>
<td>Always 00B.</td>
</tr>
<tr>
<td>19:18</td>
<td>Reserved</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>21:20</td>
<td>Symmetric Arbitration ID (R/O)</td>
<td>Unique</td>
<td>Always 00B.</td>
</tr>
<tr>
<td>26:22</td>
<td>Integer Bus Frequency Ratio (R/O)</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>3AH 58</td>
<td>IA32FEATURE_CONTROL</td>
<td>Unique</td>
<td>Control Features in Intel 64 Processor (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>40H 64</td>
<td>MSR_LASTBRANCH_O_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 0 From IP (R/W) One of eight pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction for one of the last eight branches, exceptions, or interrupts taken by the processor. See also: • Last Branch Record Stack TOS at 1C9H • Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors).”</td>
</tr>
<tr>
<td>41H 65</td>
<td>MSR_LASTBRANCH_1_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 1 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>42H 66</td>
<td>MSR_LASTBRANCH_2_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 2 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>43H 67</td>
<td>MSR_LASTBRANCH_3_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 3 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>44H 68</td>
<td>MSR_LASTBRANCH_4_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 4 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>45H 69</td>
<td>MSR_LASTBRANCH_5_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 5 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>46H 70</td>
<td>MSR_LASTBRANCH_6_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 6 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
</tbody>
</table>
### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>47H 71</td>
<td>MSR_LASTBRANCH_7_FROM_IP</td>
<td>Unique</td>
<td>Last Branch Record 7 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>60H 96</td>
<td>MSR_LASTBRANCH_0_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 0 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of eight pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the destination instruction for one of the last eight branches, exceptions, or interrupts taken by the processor.</td>
</tr>
<tr>
<td>61H 97</td>
<td>MSR_LASTBRANCH_1_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 1 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>62H 98</td>
<td>MSR_LASTBRANCH_2_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 2 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>63H 99</td>
<td>MSR_LASTBRANCH_3_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 3 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>64H 100</td>
<td>MSR_LASTBRANCH_4_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 4 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>65H 101</td>
<td>MSR_LASTBRANCH_5_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 5 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>66H 102</td>
<td>MSR_LASTBRANCH_6_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 6 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>67H 103</td>
<td>MSR_LASTBRANCH_7_TO_IP</td>
<td>Unique</td>
<td>Last Branch Record 7 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>79H 121</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>Shared</td>
<td>BIOS Update Trigger Register (W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8BH 139</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>Unique</td>
<td>BIOS Update Signature ID (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C1H 193</td>
<td>IA32_PMC0</td>
<td>Unique</td>
<td>Performance counter register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C2H 194</td>
<td>IA32_PMC1</td>
<td>Unique</td>
<td>Performance Counter Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>CDH 205</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td>Scaleable Bus Speed(RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This field indicates the intended scaleable bus clock speed for processors based on Intel Atom microarchitecture:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 111B: 083 MHz (FSB 333)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 101B: 100 MHz (FSB 400)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 001B: 133 MHz (FSB 533)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 011B: 167 MHz (FSB 667)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>133.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 001B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>166.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 011B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:3 Reserved.</td>
</tr>
</tbody>
</table>
### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Hex Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E7H 231</td>
<td>IA32_MPERF</td>
<td>Unique</td>
<td><strong>Maximum Performance Frequency Clock Count (RW)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>E8H 232</td>
<td>IA32_APERF</td>
<td>Unique</td>
<td><strong>Actual Performance Frequency Clock Count (RW)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>Shared</td>
<td><strong>Memory Type Range Register (R)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>11EH 281</td>
<td>MSR_BBL_CR_CTL3</td>
<td>Shared</td>
<td><strong>L2 Hardware Enabled (RO)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = If the L2 is hardware-enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Indicates if the L2 is hardware-disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7:1</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8</td>
<td><strong>L2 Enabled. (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = L2 cache has been initialized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Until this bit is set the processor will not respond to the WBINVD instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>or the assertion of the FLUSH# input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>22:9</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>23</td>
<td><strong>L2 Not Present (RO)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = L2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = L2 Not Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:24</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>174H 372</td>
<td>IA32_SYSENTER_CS</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H 373</td>
<td>IA32_SYSENTER_ESP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H 374</td>
<td>IA32_SYSENTER_EIP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS</td>
<td>Unique</td>
<td><strong>RIPV</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>pointer pushed on the stack (when the machine check was generated) can be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>used to restart the program. If cleared, the program cannot be reliably</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>Restarted.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td><strong>EIPV</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>pointer pushed on the stack (when the machine check was generated) is directly</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>associated with the error.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td><strong>MCIP</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that a machine check has been generated. If a second</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>machine check is detected while this bit is still set, the processor enters a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>shutdown state. Software should write this bit to 0 after processing a machine</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>check exception.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:3</td>
<td><strong>Reserved.</strong></td>
</tr>
</tbody>
</table>
### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H 408</td>
<td>MSR_PERF_STATUS</td>
<td>Shared</td>
<td>15:0 Current Performance State Value.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>39:16 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>44:40 Maximum Bus Ratio (R/O) Indicates maximum bus ratio configured for the processor.</td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Unique</td>
<td>Clock Modulation (R/W) See Table 35-2. IA32_CLOCK_MODULATION MSR was originally named IA32_THERM_CONTROL MSR.</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Unique</td>
<td>Thermal Interrupt Control (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Unique</td>
<td>Thermal Monitor Status (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>19DH 413</td>
<td>MSR_THERM2_CTL</td>
<td>Shared</td>
<td>15:0 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>16 TM_SELECT (R/W) Mode of automatic thermal monitor: 0 = Thermal Monitor 1 (thermally-initiated on-die modulation of the stop-clock duty cycle) 1 = Thermal Monitor 2 (thermally-initiated frequency transitions) If bit 3 of the IA32_MISC_ENABLE register is cleared, TM_SELECT has no effect. Neither TM1 nor TM2 are enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:17 Reserved.</td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>Unique</td>
<td>Enable Misc. Processor Features (R/W) Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Fast-Strings Enable See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2:1 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 Unique Automatic Thermal Control Circuit Enable (R/W) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6:4 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7 Shared Performance Monitoring Available (R) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8 Reserved.</td>
</tr>
</tbody>
</table>
### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Reserved</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>10</td>
<td>FERR# Multiplexing Enable (R/W)</td>
<td>Shared</td>
<td>1 = FERR# asserted by the processor to indicate a pending break event within the processor. 0 = Indicates compatible FERR# signaling behavior. This bit must be set to 1 to support XAPIC interrupt model usage.</td>
</tr>
<tr>
<td>11</td>
<td>Branch Trace Storage Unavailable (RO)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>12</td>
<td>Precise Event Based Sampling Unavailable (RO)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>13</td>
<td>TM2 Enable (R/W)</td>
<td>Shared</td>
<td>When this bit is set (1) and the thermal sensor indicates that the die temperature is at the pre-determined threshold, the Thermal Monitor 2 mechanism is engaged. TM2 will reduce the bus to core ratio and voltage according to the value last written to MSR_THERM2_CTL bits 15:0. When this bit is clear (0, default), the processor does not change the VID signals or the bus to core ratio when the processor enters a thermally managed state. The BIOS must enable this feature if the TM2 feature flag (CPUID.1:ECX[8]) is set; if the TM2 feature flag is not set, this feature is not supported and BIOS must not alter the contents of the TM2 bit location. The processor is operating out of specification if both this bit and the TM1 bit are set to 0.</td>
</tr>
<tr>
<td>15:14</td>
<td>Reserved</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>16</td>
<td>Enhanced Intel SpeedStep Technology Enable (R/W)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>18</td>
<td>ENABLE MONITOR FSM (R/W)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>20</td>
<td>Enhanced Intel SpeedStep Technology Select Lock (R/W)</td>
<td>Shared</td>
<td>When set, this bit causes the following bits to become read-only: • Enhanced Intel SpeedStep Technology Select Lock (this bit), • Enhanced Intel SpeedStep Technology Enable bit. The bit must be set before an Enhanced Intel SpeedStep Technology transition is requested. This bit is cleared on reset.</td>
</tr>
<tr>
<td>21</td>
<td>Reserved</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>22</td>
<td>Limit CPUID Maxval (R/W)</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>23</td>
<td>xTPR Message Disable (R/W)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>33:24</td>
<td>Reserved</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Shared/Unique</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>--------------------------------</td>
<td>---------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>34</td>
<td>Unique</td>
<td>XD Bit Disable (R/W)</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>63:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1C9H 457</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Unique</td>
<td>Last Branch Record Stack TOS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains an index (bits 0-2) that points to the MSR containing the most recent branch record.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See MSR_LASTBRANCH_0_FROM_IP (at 40H).</td>
</tr>
<tr>
<td>1D9H 473</td>
<td>IA32_DEBUGCTL</td>
<td>Unique</td>
<td>Debug Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1DDH 477</td>
<td>MSR_LER_FROM_LIP</td>
<td>Unique</td>
<td>Last Exception Record From Linear IP (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains a pointer to the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>1DEH 478</td>
<td>MSR_LER_TO_LIP</td>
<td>Unique</td>
<td>Last Exception Record To Linear IP (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This area contains a pointer to the target of the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>200H 512</td>
<td>IA32_MTRR_PHYSBASE0</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>201H 513</td>
<td>IA32_MTRR_PHYSMASK0</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>202H 514</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>203H 515</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>204H 516</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>205H 517</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>206H 518</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>207H 519</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>208H 520</td>
<td>IA32_MTRR_PHYSBASE4</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>209H 521</td>
<td>IA32_MTRR_PHYSMASK4</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20AH 522</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20CH 524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>250H 592</td>
<td>IA32_MTRR_FIX64K_70000_00000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000_80000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000_A0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000_C0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>269H 61H</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26AH 61H</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26BH 61H</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26CH 620</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26DH 621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26EH 622</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26FH 623</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>277H 631</td>
<td>IA32_PAT</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>309H 777</td>
<td>IA32_FIXED_CTR0</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>30AH 778</td>
<td>IA32_FIXED_CTR1</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>30BH 779</td>
<td>IA32_FIXED_CTR2</td>
<td>Unique</td>
<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>345H 837</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>Shared</td>
<td>See Table 35-2. See Section 17.4.1, “IA32_DEBUGCTL MSR.”</td>
</tr>
<tr>
<td>38DH 909</td>
<td>IA32_FIXED_CTR_CTRL</td>
<td>Unique</td>
<td>Fixed-Function-Counter Control Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>38EH 910</td>
<td>IA32_PERF_GLOBAL_STATUS</td>
<td>Unique</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL</td>
<td>Unique</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
<td>Unique</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEBs_ENABLE</td>
<td>Unique</td>
<td>See Table 35-2. See Section 18.4.4, &quot;Precise Event Based Sampling (PEBS).&quot;</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Enable PEBS on IA32_PMC0 (R/W)</td>
</tr>
<tr>
<td>400H 1024</td>
<td>IA32_MC0_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>401H 1025</td>
<td>IA32_MC0_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs.”</td>
</tr>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR</td>
<td>Shared</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs.”</td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs.”</td>
</tr>
<tr>
<td>Hex</td>
<td>Dec</td>
<td>Register Name</td>
<td>Shared/Unique</td>
</tr>
<tr>
<td>-----</td>
<td>------</td>
<td>---------------------</td>
<td>---------------</td>
</tr>
<tr>
<td>40AH</td>
<td>1034</td>
<td>IA32_MC2_ADDR</td>
<td>Shared</td>
</tr>
<tr>
<td>40CH</td>
<td>1036</td>
<td>MSR_MC3_CTL</td>
<td>Shared</td>
</tr>
<tr>
<td>40DH</td>
<td>1037</td>
<td>MSR_MC3_STATUS</td>
<td>Shared</td>
</tr>
<tr>
<td>40EH</td>
<td>1038</td>
<td>MSR_MC3_ADDR</td>
<td>Shared</td>
</tr>
<tr>
<td>410H</td>
<td>1040</td>
<td>MSR_MC4_CTL</td>
<td>Shared</td>
</tr>
<tr>
<td>411H</td>
<td>1041</td>
<td>MSR_MC4_STATUS</td>
<td>Shared</td>
</tr>
<tr>
<td>412H</td>
<td>1042</td>
<td>MSR_MC4_ADDR</td>
<td>Shared</td>
</tr>
<tr>
<td>480H</td>
<td>1152</td>
<td>IA32_VMX_BASIC</td>
<td>Unique</td>
</tr>
<tr>
<td>481H</td>
<td>1153</td>
<td>IA32_VMX_PINBASED_</td>
<td>Unique</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CTLS</td>
<td></td>
</tr>
<tr>
<td>482H</td>
<td>1154</td>
<td>IA32_VMX_PROCBASED_</td>
<td>Unique</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CTLS</td>
<td></td>
</tr>
<tr>
<td>483H</td>
<td>1155</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Unique</td>
</tr>
<tr>
<td>484H</td>
<td>1156</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Unique</td>
</tr>
<tr>
<td>485H</td>
<td>1157</td>
<td>IA32_VMX_MISC</td>
<td>Unique</td>
</tr>
</tbody>
</table>
Table 35-4. MSRs in 45 nm and 32 nm Intel® Atom™ Processor Family (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 486H | 1158| IA32_VMX_CRO_FIXED0 | Unique | Capability Reporting Register of CR0 Bits Fixed to 0 (R/O)  
See Table 35-2.  
See Appendix A.7, “VMX-Fixed Bits in CR0.” |
| 487H | 1159| IA32_VMX_CRO_FIXED1 | Unique | Capability Reporting Register of CR0 Bits Fixed to 1 (R/O)  
See Table 35-2.  
See Appendix A.7, “VMX-Fixed Bits in CR0.” |
| 488H | 1160| IA32_VMX_CR4_FIXED0 | Unique | Capability Reporting Register of CR4 Bits Fixed to 0 (R/O)  
See Table 35-2.  
See Appendix A.8, “VMX-Fixed Bits in CR4.” |
| 489H | 1161| IA32_VMX_CR4_FIXED1 | Unique | Capability Reporting Register of CR4 Bits Fixed to 1 (R/O)  
See Table 35-2.  
See Appendix A.8, “VMX-Fixed Bits in CR4.” |
| 48AH| 1162| IA32_VMX_VMCS_ENUM | Unique | Capability Reporting Register of VMCS Field Enumeration (R/O)  
See Table 35-2.  
See Appendix A.9, “VMCS Enumeration.” |
| 48BH| 1163| IA32_VMX_PROCBASED_CTLS2 | Unique | Capability Reporting Register of Secondary Processor-based VM-execution Controls (R/O)  
See Appendix A.3, “VM-Execution Controls.” |
| 600H| 1536| IA32_DS_AREA | Unique | DS Save Area (R/W)  
See Table 35-2.  
| C000_0080H| | IA32_EFER | Unique | Extended Feature Enables  
See Table 35-2. |
| C000_0081H| | IA32_STAR | Unique | System Call Target Address (R/W)  
See Table 35-2. |
| C000_0082H| | IA32_LSTAR | Unique | IA-32e Mode System Call Target Address (R/W)  
See Table 35-2. |
| C000_0084H| | IA32_FMASK | Unique | System Call Flag Mask (R/W)  
See Table 35-2. |
| C000_0100H| | IA32_FS_BASE | Unique | Map of BASE Address of FS (R/W)  
See Table 35-2. |
| C000_0101H| | IA32_GS_BASE | Unique | Map of BASE Address of GS (R/W)  
See Table 35-2. |
| C000_0102H| | IA32 KERNEL_GSBASE | Unique | Swap Target of BASE Address of GS (R/W) See Table 35-2. |

Table 35-5 lists model-specific registers (MSRs) that are specific to Intel® Atom™ processor with the CPUID signature with DisplayFamily_DisplayModel of 06_27H.
MODEL-SPECIFIC REGISTERS (MSRS)

35.4 MSRS IN INTEL PROCESSORS BASED ON SILVERMONT MICROARCHITECTURE

Table 35-6 lists model-specific registers (MSRs) for Intel processors based on the Silvermont microarchitecture. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_37H, 06_4AH, 06_4DH, 06_5AH, and 06_5DH; see Table 35-1.

The column “Scope” lists the core/shared/package granularity of sharing in the Silvermont microarchitecture. “Core” means each processor core has a separate MSR, or a bit field not shared with another processor core. “Shared” means the MSR or the bit field is shared by more than one processor cores in the physical package. “Package” means all processor cores in the physical package share the same MSR or bit interface.

Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0H</td>
<td>0</td>
<td>Shared</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H</td>
<td>1</td>
<td>Shared</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>6H</td>
<td>6</td>
<td>Core</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination.” and Table 35-2</td>
</tr>
<tr>
<td>10H</td>
<td>16</td>
<td>Core</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H</td>
<td>23</td>
<td>Shared</td>
<td>Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>

Table 35-5. MSRs Supported by Intel® Atom™ Processors with CPUID Signature 06_27H

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3F8H</td>
<td>MSR_PKG.C2_RESIDENCY</td>
<td>Package</td>
<td>Package C2 Residency</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 Package C2 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Time that this package is in processor-specific C2 states since last reset. Counts at 1 Mhz frequency.</td>
</tr>
<tr>
<td>3F9H</td>
<td>MSR_PKG.C4_RESIDENCY</td>
<td>Package</td>
<td>Package C4 Residency</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 Package C4 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Time that this package is in processor-specific C4 states since last reset. Counts at 1 Mhz frequency.</td>
</tr>
<tr>
<td>3FAH</td>
<td>MSR_PKG.C6_RESIDENCY</td>
<td>Package</td>
<td>Package C6 Residency</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 Package C6 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Time that this package is in processor-specific C6 states since last reset. Counts at 1 Mhz frequency.</td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17H 23</td>
<td>MSR_PLATFORM_ID</td>
<td>Shared</td>
<td>Model Specific Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>12:8</td>
<td>Maximum Qualified Ratio (R)</td>
<td>The maximum allowed bus ratio.</td>
</tr>
<tr>
<td></td>
<td>49:13</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>52:50</td>
<td>See Table 35-2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:33</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td>1BH 27</td>
<td>IA32_APIC_BASE</td>
<td>Core</td>
<td>See Section 10.4.4, “Local APIC Status and Location,” and Table 35-2.</td>
</tr>
<tr>
<td>2AH 42</td>
<td>MSR_EBL_CR_POWERON</td>
<td>Shared</td>
<td>Processor Hard Power-On Configuration (R/W) Enables and disables processor features; (R) indicates current processor configuration.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Data Error Checking Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>Response Error Checking Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>AERR# Drive Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>BERR# Enable for initiator bus requests (R/W)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>BINIT# Driver Enable (R/W)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>Execute BIST (R/O)</td>
<td>1 = Enabled; 0 = Disabled</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>AERR# Observation Enabled (R/O)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>Reserved.</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>BINIT# Observation Enabled (R/O)</td>
<td>1 = Enabled; 0 = Disabled. Always 0.</td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>Reserved.</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>14</td>
<td>1 MByte Power on Reset Vector (R/O)</td>
<td>Core</td>
<td>1 MByte; 0 = 4 GBytes</td>
</tr>
<tr>
<td>15</td>
<td>Reserved.</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>17:16</td>
<td>APIC Cluster ID (R/O)</td>
<td>Core</td>
<td>Always 00B.</td>
</tr>
<tr>
<td>19:18</td>
<td>Reserved.</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>21:20</td>
<td>Symmetric Arbitration ID (R/O)</td>
<td>Core</td>
<td>Always 00B.</td>
</tr>
<tr>
<td>26:22</td>
<td>Integer Bus Frequency Ratio (R/O)</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>34H 52</td>
<td>MSR_SMI_COUNT</td>
<td>Core</td>
<td>SMI Counter (R/O)</td>
</tr>
<tr>
<td>31:0</td>
<td>SMI Count (R/O)</td>
<td>Core</td>
<td>Running count of SMI events since last RESET.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>3AH 58</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Core</td>
<td>Control Features in Intel 64Processor (R/W)</td>
</tr>
<tr>
<td>0</td>
<td>Lock (R/WL)</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
<td>Core</td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>2</td>
<td>Enable VMX outside SMX operation (R/WL)</td>
<td>Core</td>
<td><strong>Enable VMX outside SMX operation (R/WL)</strong></td>
</tr>
<tr>
<td>40H 64</td>
<td>MSR_LASTBRANCH_0_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 0 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>One of eight pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction for one of the last eight branches, exceptions, or interrupts taken by the processor. See also:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ Last Branch Record Stack TOS at 1C9H</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>▪ Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors).”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41H 65</td>
<td>MSR_LASTBRANCH_1_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 1 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>42H 66</td>
<td>MSR_LASTBRANCH_2_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 2 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>43H 67</td>
<td>MSR_LASTBRANCH_3_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 3 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44H 68</td>
<td>MSR_LASTBRANCH_4_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 4 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>45H 69</td>
<td>MSR_LASTBRANCH_5_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 5 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46H 70</td>
<td>MSR_LASTBRANCH_6_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 6 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>47H</td>
<td>MSR_LASTBRANCH_7_FROM_IP</td>
<td>Core</td>
<td>Last Branch Record 7 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>60H</td>
<td>MSR_LASTBRANCH_0_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 0 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of eight pairs of last branch record registers on the last branch record stack.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This part of the stack contains pointers to the destination instruction for one of the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>last eight branches, exceptions, or interrupts taken by the processor.</td>
</tr>
<tr>
<td>61H</td>
<td>MSR_LASTBRANCH_1_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 1 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>62H</td>
<td>MSR_LASTBRANCH_2_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 2 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>63H</td>
<td>MSR_LASTBRANCH_3_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 3 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>64H</td>
<td>MSR_LASTBRANCH_4_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 4 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>65H</td>
<td>MSR_LASTBRANCH_5_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 5 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>66H</td>
<td>MSR_LASTBRANCH_6_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 6 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>67H</td>
<td>MSR_LASTBRANCH_7_TO_IP</td>
<td>Core</td>
<td>Last Branch Record 7 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>79H</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>Core</td>
<td>BIOS Update Trigger Register (W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8BH</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>Core</td>
<td>BIOS Update Signature ID (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C1H</td>
<td>IA32_PMC0</td>
<td>Core</td>
<td>Performance counter register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C2H</td>
<td>IA32_PMC1</td>
<td>Core</td>
<td>Performance Counter Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>CDH</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td>Scaleable Bus Speed (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This field indicates the intended scaleable bus clock speed for processors based on</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Silvermont microarchitecture:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2:0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 100B: 080.0 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 000B: 083.3 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 001B: 100.0 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 010B: 133.3 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 011B: 116.7 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>E2H</td>
<td>MSR_PKG_CST_CONFIG_CONFIG_CONTROL</td>
<td>Shared</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MiWAIT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>extension C-state parameters or ACPI C-States.</td>
</tr>
</tbody>
</table>

---

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### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2:0</td>
<td>Package C-State Limit (R/W)</td>
<td>Package C-State Limit (R/W)</td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power), for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 000b: C0 (no package C-state support) 001b: C1 (Behavior is the same as 000b) 100b: C4 110b: C6 111b: C7 (Silvermont only).</td>
</tr>
<tr>
<td>9:3</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>10</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td>When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWAIT instructions</td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/W/O)</td>
<td>CFG Lock (R/W/O)</td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>15:0</td>
<td>LVL_2 Base Address (R/W)</td>
<td>LVL_2 Base Address (R/W)</td>
<td>Specifies the base address visible to software for IO redirection. If IO MWAIT Redirection is enabled, reads to this address will be consumed by the power management logic and decoded to MWAIT instructions. When IO port address redirection is enabled, this is the IO port address reported to the OS/software.</td>
</tr>
<tr>
<td>18:16</td>
<td>C-state Range (R/W)</td>
<td>C-state Range (R/W)</td>
<td>Specifies the encoding value of the maximum C-State code name to be included when IO read to MWAIT redirection is enabled by MSR_PKG_CST_CONFIG_CONTROL[bit10]: 100b - C4 is the max C-State to include 110b - C6 is the max C-State to include 111b - C7 is the max C-State to include</td>
</tr>
<tr>
<td>63:19</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
<tr>
<td>E7H 231</td>
<td>IA32_MPERF</td>
<td>Core</td>
<td>Maximum Performance Frequency Clock Count (RW) See Table 35-2.</td>
</tr>
<tr>
<td>E8H 232</td>
<td>IA32_APERF</td>
<td>Core</td>
<td>Actual Performance Frequency Clock Count (RW) See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>Core</td>
<td>Memory Type Range Register (R) See Table 35-2.</td>
</tr>
<tr>
<td>11EH 281</td>
<td>MSR_BBL_CR_CTL3</td>
<td>Shared</td>
<td>Memory Type Range Register (R) See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>L2 Hardware Enabled (RO)</td>
<td>1 = If the L2 is hardware-enabled  &lt;br&gt; 0 = Indicates if the L2 is hardware-disabled</td>
<td></td>
</tr>
<tr>
<td>7:1</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>L2 Enabled. (R/W)</td>
<td>1 = L2 cache has been initialized  &lt;br&gt; 0 = Disabled (default) &lt;br&gt; Until this bit is set the processor will not respond to the WBINVD instruction or the assertion of the FLUSH# input.</td>
<td></td>
</tr>
<tr>
<td>22:9</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>L2 Not Present (RO)</td>
<td>0 = L2 Present  &lt;br&gt; 1 = L2 Not Present</td>
<td></td>
</tr>
<tr>
<td>63:24</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13CH 52</td>
<td>MSR_FEATURE_CONFIG</td>
<td>Core</td>
<td>AES Configuration (RW-L)  &lt;br&gt; Privileged post-BIOS agent must provide a #GP handler to handle unsuccessful read of this MSR.</td>
</tr>
<tr>
<td>1:0</td>
<td>AES Configuration (RW-L)</td>
<td>Upon a successful read of this MSR, the configuration of AES instruction set availability is as follows:  &lt;br&gt; 11b: AES instructions are not available until next RESET.  &lt;br&gt; otherwise, AES instructions are available.  &lt;br&gt; Note, AES instruction set is not available if read is unsuccessful. If the configuration is not 01b, AES instruction can be mis-configured if a privileged agent unintentionally writes 11b.</td>
<td></td>
</tr>
<tr>
<td>63:2</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>174H 372</td>
<td>IA32_SYSENTER_CS</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H 373</td>
<td>IA32_SYSENTER_ESP</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H 374</td>
<td>IA32_SYSENTER_EIP</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>RIPV</td>
<td>When set, bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) can be used to restart the program. If cleared, the program cannot be reliably restarted</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EIPV</td>
<td>When set, bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) is directly associated with the error.</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>MCIP</td>
<td>Core</td>
<td>When set, bit indicates that a machine check has been generated. If a second</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>machine check is detected while this bit is still set, the processor enters a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>shutdown state. Software should write this bit to 0 after processing a machine</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>check exception.</td>
</tr>
<tr>
<td>63-3</td>
<td>Reserved</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>7-0</td>
<td>Event Select</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>15-8</td>
<td>UMask</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>USR</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>OS</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Edge</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>PC</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>INT</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Reserved</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>EN</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>INV</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>31-24</td>
<td>CMASK</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>63-32</td>
<td>Reserved</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Core</td>
<td>Clock Modulation (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IA32_CLOCK_MODULATION MSR was originally named IA32_THERM_CONTROL MSR.</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Core</td>
<td>Thermal Interrupt Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Core</td>
<td>Thermal Monitor Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>Core</td>
<td>Enable Misc. Processor Features (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td>0</td>
<td>Fast-Strings Enable</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2:1</td>
<td>Reserved</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Automatic Thermal Control Circuit Enable (R/W)</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>6:4</td>
<td>Reserved</td>
<td>Core</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Performance Monitoring Available (R)</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>---------</td>
<td>---------------</td>
<td>-------------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>10:8</td>
<td></td>
<td>Core</td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td>Core</td>
<td>Branch Trace Storage Unavailable (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>12</td>
<td>Core</td>
<td>Precise Event Based Sampling Unavailable (RO)</td>
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</tr>
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<td></td>
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<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>15:13</td>
<td>Shared</td>
<td>Enhanced Intel SpeedStep Technology Enable (R/W)</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>18</td>
<td>Core</td>
<td>ENABLE MONITOR FSM (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>21:19</td>
<td></td>
<td>Core</td>
<td>Reserved.</td>
</tr>
<tr>
<td>22</td>
<td>Core</td>
<td>Limit CPUID Maxval (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>23</td>
<td>Shared</td>
<td>xTPR Message Disable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>33:24</td>
<td></td>
<td>Core</td>
<td>Reserved.</td>
</tr>
<tr>
<td>34</td>
<td>Core</td>
<td>XD Bit Disable (R/W)</td>
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</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>37:35</td>
<td></td>
<td>Core</td>
<td>Reserved.</td>
</tr>
<tr>
<td>38</td>
<td>Shared</td>
<td>Turbo Mode Disable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1 on processors that support Intel Turbo Boost Technology, the turbo mode feature is disabled and the IDA_Enable feature flag will be clear (CPUID.06H: EAX[1]=0). When set to a 0 on processors that support IDA, CPUID.06H: EAX[1] reports the processor’s support of turbo mode is enabled. Note: the power-on default value is used by BIOS to detect hardware support of turbo mode. If power-on default value is 1, turbo mode is available in the processor. If power-on default value is 0, turbo mode is not available.</td>
</tr>
<tr>
<td>63:39</td>
<td></td>
<td>Core</td>
<td>Reserved.</td>
</tr>
<tr>
<td>1A2H</td>
<td>MSR_TEMPERATURE_TARGET</td>
<td>Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>418</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>15:0</td>
<td></td>
<td>Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td>23:16</td>
<td>Temperature Target (R)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The default thermal throttling or PROCHOT# activation temperature in degree C. The effective temperature for thermal throttling or PROCHOT# activation is “Temperature Target” + “Target Offset”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29:24</td>
<td>Target Offset (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Specifies an offset in degrees C to adjust the throttling and PROCHOT# activation temperature from the default target specified in TEMPERATURE_TARGET (bits 23:16).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:30</td>
<td></td>
<td>Package</td>
<td>Reserved.</td>
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### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
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<th>Bit Description</th>
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<tbody>
<tr>
<td>1A6H</td>
<td>MSR_OFFCORE_RSP_0</td>
<td>Shared</td>
<td>Offcore Response Event Select Register (R/W)</td>
</tr>
<tr>
<td>1A7H</td>
<td>MSR_OFFCORE_RSP_1</td>
<td>Shared</td>
<td>Offcore Response Event Select Register (R/W)</td>
</tr>
<tr>
<td>1ADH</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode (RW)</td>
</tr>
<tr>
<td>1B0H</td>
<td>IA32_ENERGY_PERF_BIAS</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1C9H</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Core</td>
<td>Last Branch Record Stack TOS (R/W)</td>
</tr>
<tr>
<td>1D9H</td>
<td>IA32_DEBUGCTL</td>
<td>Core</td>
<td>Debug Control (R/W)</td>
</tr>
<tr>
<td>1DDH</td>
<td>MSR_LER_FROM_LIP</td>
<td>Core</td>
<td>Last Exception Record From Linear IP (R)</td>
</tr>
<tr>
<td>1DEH</td>
<td>MSR_LER_TO_LIP</td>
<td>Core</td>
<td>Last Exception Record To Linear IP (R)</td>
</tr>
<tr>
<td>1F2H</td>
<td>IA32_SMRR_PHYSBASE</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1F3H</td>
<td>IA32_SMRR_PHYSMASK</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>200H</td>
<td>IA32_MTRR_PHYSBASE0</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>201H</td>
<td>IA32_MTRR_PHYSMASK0</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>202H</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>203H</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>204H</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>205H</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>206H</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>207H</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>208H</td>
<td>IA32_MTRR_PHYSBASE4</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>209H</td>
<td>IA32_MTRR_PHYSMASK4</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20AH</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

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<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20CH 524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>250H 592</td>
<td>IA32_MTRR_FIX64K_00000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>269H 617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26AH 618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26BH 619</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26CH 620</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26DH 621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26EH 622</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26FH 623</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>277H 631</td>
<td>IA32_PAT</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>Core</td>
<td>Default Memory Types (R/W)</td>
</tr>
<tr>
<td>309H 777</td>
<td>IA32_FIXED_CTR0</td>
<td>Core</td>
<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
</tr>
<tr>
<td>30AH 778</td>
<td>IA32_FIXED_CTR1</td>
<td>Core</td>
<td>Fixed-Function Performance Counter Register 1 (R/W)</td>
</tr>
<tr>
<td>30BH 779</td>
<td>IA32_FIXED_CTR2</td>
<td>Core</td>
<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
</tr>
<tr>
<td>345H 837</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>Core</td>
<td>See Table 35-2. See Section 17.4.1, “IA32_DEBUGCTL MSR.”</td>
</tr>
<tr>
<td>380H 909</td>
<td>IA32_FIXED_CTR_CTRL</td>
<td>Core</td>
<td>Fixed-Function-Counter Control Register (R/W)</td>
</tr>
<tr>
<td>38EH 910</td>
<td>IA32_PERF_GLOBAL_STAUS</td>
<td>Core</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL</td>
<td>Core</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
<td>Core</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
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<tr>
<td>3F1H 1009</td>
<td>MSR_PEBS_ENABLE</td>
<td>Core</td>
<td>See Table 35-2. See Section 18.4.4, “Precise Event Based Sampling (PEBS).”</td>
</tr>
<tr>
<td>0</td>
<td>Enable PEBS on IA32_PMC0. (R/W)</td>
<td>Core</td>
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Table 35-6. Common MSRs in Intel Processors Based on the Silvermont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3FAH</td>
<td>MSR_PKG_C6_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 Package C6 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value since last reset that this package is in processor-specific C6 states. Counts at the TSC Frequency.</td>
</tr>
<tr>
<td>3FDH</td>
<td>MSR_CORE_C6_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 CORE C6 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value since last reset that this core is in processor-specific C6 states. Counts at the TSC Frequency.</td>
</tr>
<tr>
<td>400H</td>
<td>IA32_MC0_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>401H</td>
<td>IA32_MC0_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>402H</td>
<td>IA32_MC0_ADDR</td>
<td>Shared</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>404H</td>
<td>IA32_MC1_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>405H</td>
<td>IA32_MC1_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>408H</td>
<td>IA32_MC2_CTL</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>409H</td>
<td>IA32_MC2_STATUS</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>40AH</td>
<td>IA32_MC2_ADDR</td>
<td>Shared</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
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<td></td>
<td>The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>40CH</td>
<td>MSR_MC3_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>40DH</td>
<td>MSR_MC3_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>40EH</td>
<td>MSR_MC3_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
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<td></td>
<td>The MSR_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>410H</td>
<td>MSR_MC4_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>411H</td>
<td>MSR_MC4_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
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<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
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<tbody>
<tr>
<td>412H</td>
<td>MSR_MC4_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
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<td>The MSR_MC4_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the MSR_MC4_STATUS register is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When not implemented in the processor, all reads and writes to this MSR will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>414H</td>
<td>MSR_MC5_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>415H</td>
<td>MSR_MC5_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.”</td>
</tr>
<tr>
<td>416H</td>
<td>MSR_MC5_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
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<td></td>
<td>The MSR_MC4_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the MSR_MC4_STATUS register is clear.</td>
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<tr>
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<td>When not implemented in the processor, all reads and writes to this MSR will</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>480H</td>
<td>IA32_VMX_BASIC</td>
<td>Core</td>
<td>Reporting Register of Basic VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
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<td>See Appendix A.1, “Basic VMX Information.”</td>
</tr>
<tr>
<td>481H</td>
<td>IA32_VMX_PINBASED_CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O)</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>482H</td>
<td>IA32_VMX_PROCBASED_CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>483H</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of VM-exit Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.4, “VM-Exit Controls.”</td>
</tr>
<tr>
<td>484H</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of VM-entry Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.5, “VM-Entry Controls.”</td>
</tr>
<tr>
<td>485H</td>
<td>IA32_VMX_MISC</td>
<td>Core</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.6, “Miscellaneous Data.”</td>
</tr>
<tr>
<td>486H</td>
<td>IA32_VMX_CRO_FIXED0</td>
<td>Core</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CR0.”</td>
</tr>
<tr>
<td>487H</td>
<td>IA32_VMX_CRO_FIXED1</td>
<td>Core</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CR0.”</td>
</tr>
<tr>
<td>488H</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Core</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.8, “VMX-Fixed Bits in CR4.”</td>
</tr>
<tr>
<td>Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>----------</td>
<td>------------------------------------</td>
<td>----------------</td>
<td>--------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>489H</td>
<td>IA32_VMX_CR4_FIXED1</td>
<td>Core</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td>48AH</td>
<td>IA32_VMX_VMCS_ENUM</td>
<td>Core</td>
<td>Capability Reporting Register of VMCS Field Enumeration (R/O)</td>
</tr>
<tr>
<td>48BH</td>
<td>IA32_VMX_PROCBASED__CTLS2</td>
<td>Core</td>
<td>Capability Reporting Register of Secondary Processor-based VM-execution Controls</td>
</tr>
<tr>
<td>48CH</td>
<td>IA32_VMX_EPHT_VPID_ENUM</td>
<td>Core</td>
<td>Capability Reporting Register of EPT and VPID Controls (R/O)</td>
</tr>
<tr>
<td>48DH</td>
<td>IA32_VMX_TRUE_PINBASED__CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of Pin-based VM-execution Flex Controls (R/O)</td>
</tr>
<tr>
<td>48EH</td>
<td>IA32_VMX_TRUE_PROCBASED__CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls</td>
</tr>
<tr>
<td>48FH</td>
<td>IA32_VMX_TRUE_EXIT_CTLS</td>
<td>Core</td>
<td>Capability Reporting Register of VM-exit Flex Controls (R/O)</td>
</tr>
<tr>
<td>490H</td>
<td>IA32_VMX_TRUE_ENTRY_CTL</td>
<td>Core</td>
<td>Capability Reporting Register of VM-entry Flex Controls (R/O)</td>
</tr>
<tr>
<td>491H</td>
<td>IA32_VMX_FMFUNC</td>
<td>Core</td>
<td>Capability Reporting Register of VM-function Controls (R/O)</td>
</tr>
<tr>
<td>600H</td>
<td>IA32_DS_AREA</td>
<td>Core</td>
<td>DS Save Area (R/W)</td>
</tr>
<tr>
<td>660H</td>
<td>MSR_CORE_C1_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT</td>
</tr>
<tr>
<td>6E0H</td>
<td>IA32_TSC_DEADLINE</td>
<td>Core</td>
<td>TSC Target of Local APIC's TSC Deadline Mode (R/W)</td>
</tr>
<tr>
<td>C000_0080H</td>
<td>IA32_EFER</td>
<td>Core</td>
<td>Extended Feature Enables</td>
</tr>
<tr>
<td>C000_0081H</td>
<td>IA32_STAR</td>
<td>Core</td>
<td>System Call Target Address (R/W)</td>
</tr>
<tr>
<td>C000_0082H</td>
<td>IA32_LSTAR</td>
<td>Core</td>
<td>IA-32e Mode System Call Target Address (R/W)</td>
</tr>
</tbody>
</table>
Table 35-7 lists model-specific registers (MSRs) that are specific to Intel® Atom™ processor E3000 Series (CPUID signature with DisplayFamily_DisplayModel of 06_37H) and Intel Atom processors (CPUID signatures with DisplayFamily_DisplayModel of 06_4AH, 06_5AH, 06_5DH).

Table 35-7. Specific MSRs Supported by Intel® Atom™ Processors with CPUID Signature 06_37H, 06_4AH, 06_5AH, 06_5DH

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C000_0084H</td>
<td>IA32_FMASK</td>
<td>Core</td>
<td>System Call Flag Mask (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0100H</td>
<td>IA32_FS_BASE</td>
<td>Core</td>
<td>Map of BASE Address of FS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0101H</td>
<td>IA32_GS_BASE</td>
<td>Core</td>
<td>Map of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0102H</td>
<td>IA32_KERNEL_GS_BASE</td>
<td>Core</td>
<td>Swap Target of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0103H</td>
<td>IA32_TSC_AUX</td>
<td>Core</td>
<td>AUXILIARY TSC Signature. (R/W) See Table 35-2.</td>
</tr>
</tbody>
</table>
Table 35-8 lists model-specific registers (MSRs) that are specific to Intel® Atom™ processor E3000 Series (CPUID signature with DisplayFamily_DisplayModel of 06_37H).

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>668H 1640</td>
<td>MSR_CC6_DEMOTION_POLICY_CONFIG</td>
<td>Package</td>
<td>Core C6 demotion policy config MSR</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Controls per-core C6 demotion policy. Writing a value of 0 disables core level HW demotion policy.</td>
</tr>
<tr>
<td>669H 1641</td>
<td>MSR_MC6_DEMOTION_POLICY_CONFIG</td>
<td>Package</td>
<td>Module C6 demotion policy config MSR</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Controls module (i.e. two cores sharing the second-level cache) C6 demotion policy. Writing a value of 0 disables module level HW demotion policy.</td>
</tr>
<tr>
<td>664H 1636</td>
<td>MSR_MC6_RESIDENCY_COUNTER</td>
<td>Module</td>
<td>Module C6 Residency Counter (R/O)</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. Time that this module is in module-specific C6 states since last reset. Counts at 1 Mhz frequency.</td>
</tr>
</tbody>
</table>

Table 35-9 lists model-specific registers (MSRs) that are specific to Intel® Atom™ processor C2000 Series (CPUID signature with DisplayFamily_DisplayModel of 06_4DH).
<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit of Turbo Mode (RW)</strong></td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 1C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 2C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td></td>
<td>23:16</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 3C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td></td>
<td>31:24</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 4C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td></td>
<td>39:32</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 5C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 5 core active.</td>
</tr>
<tr>
<td></td>
<td>47:40</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 6C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 6 core active.</td>
</tr>
<tr>
<td></td>
<td>55:48</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 7C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 7 core active.</td>
</tr>
<tr>
<td></td>
<td>63:56</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit for 8C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 8 core active.</td>
</tr>
<tr>
<td>606H 1542</td>
<td>MSR_RAPL_POWER_UNIT</td>
<td>Package</td>
<td><strong>Unit Multipliers used in RAPL Interfaces (R/O)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
</tr>
<tr>
<td></td>
<td>3:0</td>
<td></td>
<td><strong>Power Units.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Power related information (in milliWatts) is based on the multipliers, $2^{PU}$; where $PU$ is an unsigned integer represented by bits 3:0. Default value is 0101b, indicating power unit is in 32 milliwatts increment.</td>
</tr>
<tr>
<td></td>
<td>7:4</td>
<td></td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td></td>
<td>12:8</td>
<td></td>
<td><strong>Energy Status Units.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Energy related information (in microjoules) is based on the multiplier, $2^{ESU}$; where $ESU$ is an unsigned integer represented by bits 12:8. Default value is 00101b, indicating energy unit is in 32 microjoules increment.</td>
</tr>
<tr>
<td></td>
<td>15:13</td>
<td></td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td></td>
<td>19:16</td>
<td></td>
<td><strong>Time Unit.</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The value is 0000b, indicating time unit is in one second.</td>
</tr>
<tr>
<td></td>
<td>63:20</td>
<td></td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>610H 1552</td>
<td>MSR_PKGPOWER_LIMIT</td>
<td>Package</td>
<td><strong>PKG RAPL Power Limit Control (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>66EH 1646</td>
<td>MSR_PKGPOWER_INFO</td>
<td>Package</td>
<td><strong>PKG RAPL Parameter (R/O)</strong></td>
</tr>
<tr>
<td></td>
<td>14:0</td>
<td></td>
<td><strong>Thermal Spec Power.</strong> (R/O)**</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The unsigned integer value is the equivalent of thermal specification power of the package domain. The unit of this field is specified by the “Power Units” field of MSR_RAPL_POWER_UNIT</td>
</tr>
</tbody>
</table>
35.4.1 MSRs In Intel Atom Processors Based on Airmont Microarchitecture

Intel Atom processor X7-Z8000 and X5-Z8000 series are based on the Airmont microarchitecture. These processors support MSRs listed in Table 35-6, Table 35-7, and Table 35-10. These processors have a CPUID signature with DisplayFamily_DisplayModel including 06_4CH; see Table 35-1.

Table 35-10. MSRs in Intel Atom Processors Based on the Airmont Microarchitecture

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDH 205</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td>Scaleable Bus Speed (RO) This field indicates the intended scaleable bus clock speed for processors based on Airmont microarchitecture:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0000B: 083.3 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0001B: 100.0 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0010B: 133.3 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0011B: 116.7 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0100B: 080.0 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0101B: 093.3 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0110B: 090.0 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 0111B: 088.9 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 10sure00B: 087.5 MHz</td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONTROL</td>
<td>Shared</td>
<td>C-State Configuration Control (R/W) Note: C-state values are processor specific C-state code names, unrelated to MWait extension C-state parameters or ACPI C-States. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Package C-State Limit (R/W) Specifies the lowest processor-specific C-state code name (consuming the least power), for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: No limit</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: C1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: C2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>110b: C6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111b: C7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>I/O MWait Redirection Enable (R/W) When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWait instructions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
Table 35-10. MSRs in Intel Atom Processors Based on the Airmont Microarchitecture (Contd.)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>CFG Lock (R/WO)</td>
<td></td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E4H</td>
<td>MSR_PMG_IO_CAPTURE_BASE</td>
<td>Shared</td>
<td>Power Management IO Redirection in C-state (R/W)</td>
</tr>
<tr>
<td>15:0</td>
<td>LVL_2 Base Address (R/W)</td>
<td></td>
<td>Specifies the base address visible to software for IO redirection. If IO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MWait Redirection is enabled, reads to this address will be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>consumed by the power management logic and decoded to MWait</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>instructions. When IO port address redirection is enabled, this is the IO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>port address reported to the OS/software.</td>
</tr>
<tr>
<td>18:16</td>
<td>C-state Range (R/w)</td>
<td></td>
<td>Specifies the encoding value of the maximum C-State code name to be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>included when IO read to MWait redirection is enabled by MSR_PKG_CST_CONFIG</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CONTROL[bit10]:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b - C3 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b - Deep Power Down Technology is the max C-State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b - C7 is the max C-State to include</td>
</tr>
<tr>
<td>63:19</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>638H</td>
<td>MSR_PP0_POWER_LIMIT</td>
<td>Package</td>
<td>PPO RAPL Power Limit Control (R/w)</td>
</tr>
<tr>
<td>14:0</td>
<td>PP0 Power Limit #1. (R/W)</td>
<td></td>
<td>See Section 14.9.4, “PPO/PP1 RAPL Domains,” and MSR RAPL POWER_UNIT in Table</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>35-7.</td>
</tr>
<tr>
<td>16</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:17</td>
<td>Time Window for Power Limit #1. (R/W)</td>
<td></td>
<td>Specifies the time duration over which the average power must remain below</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PPO POWER LIMIT #1 (14:0). Supported Encodings:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x0: 1 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x1: 5 second time duration (Default).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x2: 10 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x3: 15 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x4: 20 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x5: 25 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x6: 30 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x7: 35 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x8: 40 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x9: 45 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0xA: 50 second time duration.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0xB-0x7F - reserved.</td>
</tr>
<tr>
<td>63:24</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
35.5 MSRS IN THE INTEL® MICROARCHITECTURE CODE NAME NEHALEM

Table 35-11 lists model-specific registers (MSRs) that are common for Intel® microarchitecture code name Nehalem. These include Intel Core i7 and i5 processor family. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_1AH, 06_1EH, 06_1FH, 06_2EH, see Table 35-1. Additional MSRs specific to 06_1AH, 06_1EH, 06_1FH are listed in Table 35-12. Some MSRs listed in these tables are used by BIOS. More information about these MSR can be found at http://biosbits.org.

The column “Scope” represents the package/core/thread scope of individual bit field of an MSR. “Thread” means this bit field must be programmed on each logical processor independently. “Core” means the bit field must be programmed on each processor core independently, logical processors in the same core will be affected by change of this bit on the other logical processor in the same core. “Package” means the bit field must be programmed once for each physical package. Change of a bit filed with a package scope will affect all logical processors in that physical package.

Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0H</td>
<td>0 IA32_P5_MC_ADDR</td>
<td>Thread</td>
<td>See Section 35.20, ”MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H</td>
<td>1 IA32_P5_MC_TYPE</td>
<td>Thread</td>
<td>See Section 35.20, ”MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>6H</td>
<td>6 IA32_MONITOR_FILTER_SIZE</td>
<td>Thread</td>
<td>See Section 8.10.5, ”Monitor/Mwait Address Range Determination,” and Table 35-2.</td>
</tr>
<tr>
<td>10H</td>
<td>16 IA32_TIME_STAMP_COUNTER</td>
<td>Thread</td>
<td>See Section 17.14, ”Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H</td>
<td>23 IA32_PLATFORM_ID</td>
<td>Package</td>
<td>Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17H</td>
<td>23 MSR_PLATFORM_ID</td>
<td>Package</td>
<td>Model Specific Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>49:0 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>52:50 See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:53 Reserved.</td>
</tr>
<tr>
<td>1BH</td>
<td>27 IA32_APIC_BASE</td>
<td>Thread</td>
<td>See Section 10.4.4, ”Local APIC Status and Location,” and Table 35-2.</td>
</tr>
<tr>
<td>34H</td>
<td>52 MSR_SMI_COUNT</td>
<td>Thread</td>
<td>SMI Count (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31:0 SMI Count (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Running count of SMI events since last RESET.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:32 Reserved.</td>
</tr>
<tr>
<td>3AH</td>
<td>58 IA32_FEATURE_CONTROL</td>
<td>Thread</td>
<td>Control Features in Intel 64Processor (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>79H</td>
<td>121 IA32_BIOS_UPDT_TRIG</td>
<td>Core</td>
<td>BIOS Update Trigger Register (W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8BH</td>
<td>139 IA32_BIOS_SIGN_ID</td>
<td>Thread</td>
<td>BIOS Update Signature ID (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C1H</td>
<td>193 IA32_PMC0</td>
<td>Thread</td>
<td>Performance Counter Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C2H 194</td>
<td>IA32_PMC1</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3H 195</td>
<td>IA32_PMC2</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C4H 196</td>
<td>IA32_PMC3</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CEH 206</td>
<td>MSR_PLATFORM_INFO</td>
<td>Package</td>
<td>see <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>7:0</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15:8</td>
<td>Package Maximum Non-Turbo Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The is the ratio of the frequency that invariant TSC runs at. The</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>invariant TSC frequency can be computed by multiplying this ratio</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>by 133.33 MHz.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>27:16</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>28</td>
<td>Package Programmable Ratio Limit for Turbo Mode (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1, indicates that Programmable Ratio Limits for Turbo</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>mode is enabled, and when set to 0, indicates Programmable Ratio</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Limits for Turbo mode is disabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>29</td>
<td>Package Programmable TDC-TDP Limit for Turbo Mode (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1, indicates that TDC/TDP Limits for Turbo mode are</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>programmable, and when set to 0, indicates TDC and TDP Limits for</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Turbo mode are not programmable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>39:30</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>47:40</td>
<td>Package Maximum Efficiency Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The is the minimum ratio (maximum efficiency) that the processor</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>can operates, in units of 133.33MHz.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>63:48</td>
<td>Reserved.</td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td>CONFIGURATION</td>
<td></td>
<td>Note: C-state values are processor specific C-state code names,</td>
</tr>
<tr>
<td></td>
<td>CONTROL</td>
<td></td>
<td>unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>2:0 Package C-State Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power), for the package. The default is set as factory-configured</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>package C-state limit. The following C-state code name encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: C0 (no package C-state support)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: C1 (Behavior is the same as 000b)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: C3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011b: C6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100b: C7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101b and 110b: Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: No package C-state limit. Note: This field cannot be used to limit package C-state to C3.</td>
</tr>
<tr>
<td>9:3</td>
<td>Reserved.</td>
<td></td>
<td>10 I/O MWAIT Redirection Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWAIT instructions.</td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved.</td>
<td></td>
<td>15 CFG Lock (R/W/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
</tr>
<tr>
<td>23:16</td>
<td>Reserved.</td>
<td></td>
<td>24 Interrupt filtering enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, processor cores in a deep C-State will wake only when the event message is destined for that core. When 0, all processor cores in a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>deep C-State will wake for an event message.</td>
</tr>
<tr>
<td>25</td>
<td>C3 state auto demotion enable (R/W)</td>
<td></td>
<td>When set, the processor will conditionally demote C6/C7 requests to C3 based on uncore auto-demote information.</td>
</tr>
<tr>
<td>26</td>
<td>C1 state auto demotion enable (R/W)</td>
<td></td>
<td>When set, the processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information.</td>
</tr>
<tr>
<td>63:27</td>
<td>Reserved.</td>
<td></td>
<td>E4H 228 MSR_PMG_IO_CAPTURE_BASE Core</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15:0 LVL_2 Base Address (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the base address visible to software for IO redirection. If IO MWAIT Redirection is enabled, reads to this address will be consumed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>by the power management logic and decoded to MWAIT instructions. When IO port address redirection is enabled, this is the IO port address</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>reported to the OS/software.</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:16</td>
<td></td>
<td></td>
<td>C-state Range (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the encoding value of the maximum C-State code name to be included when</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IO read to MWAIT redirection is enabled by MSR_PKG_CST_CONFIG_CONTROL[bit10]:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b - C3 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b - C6 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b - C7 is the max C-State to include</td>
</tr>
<tr>
<td>63:19</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>E7H 231</td>
<td>IA32_MPERF</td>
<td>Thread</td>
<td>Maximum Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>E8H 232</td>
<td>IA32_APERF</td>
<td>Thread</td>
<td>Actual Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>174H 372</td>
<td>IA32_SYSENTER_CS</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H 373</td>
<td>IA32_SYSENTER_ESP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H 374</td>
<td>IA32_SYSENTER_EIP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS</td>
<td>Thread</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>RIPV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>pointer pushed on the stack (when the machine check was generated) can be used</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>to restart the program. If cleared, the program cannot be reliably restarted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>EIPV</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that the instruction addressed by the instruction</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>pointer pushed on the stack (when the machine check was generated) is directly</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>associated with the error.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>MCIP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, bit indicates that a machine check has been generated. If a second</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>machine check is detected while this bit is still set, the processor enters a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>shutdown state. Software should write this bit to 0 after processing a machine</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>check exception.</td>
</tr>
<tr>
<td>63:3</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td></td>
<td>Event Select</td>
</tr>
<tr>
<td>15:8</td>
<td></td>
<td></td>
<td>UMask</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
<td>USR</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
<td>OS</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td></td>
<td>Edge</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td></td>
<td>PC</td>
</tr>
</tbody>
</table>

**Note:** Details on the tables are not included in the image, but the table structure is provided.
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>INT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>AnyThread</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>EN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>INV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:24</td>
<td>CMASK</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>188H 392</td>
<td>IA32_PERFEVTSEL2</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>189H 393</td>
<td>IA32_PERFEVTSEL3</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td>Current Performance State Value.</td>
<td></td>
</tr>
<tr>
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<td>63:16</td>
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<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>Thread</td>
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<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Thread</td>
<td>Clock Modulation (R/w)</td>
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<td>3:1</td>
<td>On demand Clock Modulation Duty Cycle (R/w)</td>
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<td>4</td>
<td>On demand Clock Modulation Enable (R/w)</td>
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<td>63:5</td>
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<tr>
<td>198H 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Core</td>
<td>Thermal Interrupt Control (R/w)</td>
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<tr>
<td></td>
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<td>See Table 35-2.</td>
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<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Core</td>
<td>Thermal Monitor Status (R/w)</td>
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<tr>
<td></td>
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<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td></td>
<td>Enable Misc. Processor Features (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
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<tr>
<td></td>
<td>0</td>
<td>Thread</td>
<td>Fast-Strings Enable</td>
</tr>
<tr>
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<td>See Table 35-2.</td>
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<tr>
<td></td>
<td>3</td>
<td>Thread</td>
<td>Automatic Thermal Control Circuit Enable (R/w)</td>
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<tr>
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<td>See Table 35-2.</td>
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<td>7</td>
<td>Thread</td>
<td>Performance Monitoring Available (R)</td>
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<tr>
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<td>See Table 35-2.</td>
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<td>10:8</td>
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Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

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<tr>
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<th>Scope</th>
<th>Bit Description</th>
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<tr>
<td>11</td>
<td>Thread</td>
<td>Branch Trace Storage Unavailable (RO)</td>
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<tr>
<td></td>
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<td>See Table 35-2.</td>
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<tr>
<td>12</td>
<td>Thread</td>
<td>Precise Event Based Sampling Unavailable (RO)</td>
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<td></td>
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<td>See Table 35-2.</td>
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<td>15:13</td>
<td>Package</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Package</td>
<td>Enhanced Intel SpeedStep Technology Enable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Table 35-2.</td>
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</tr>
<tr>
<td>18</td>
<td>Thread</td>
<td>ENABLE MONITOR FSM. (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>21:19</td>
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<td>Reserved.</td>
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</tr>
<tr>
<td>22</td>
<td>Thread</td>
<td>Limit CPUID Maxval (R/W)</td>
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<td></td>
<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>23</td>
<td>Thread</td>
<td>xTPR Message Disable (R/W)</td>
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<td>See Table 35-2.</td>
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<tr>
<td>33:24</td>
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<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>XD Bit Disable (R/W)</td>
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</tr>
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<td>See Table 35-2.</td>
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<tr>
<td>37:35</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Package</td>
<td>Turbo Mode Disable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>When set to 1 on processors that support Intel Turbo Boost Technology, the turbo mode feature is disabled and the IDA_Enable feature flag will be clear (CPUID.O6H: EAX[1]=0). When set to a 0 on processors that support IDA, CPUID.O6H: EAX[1] reports the processor’s support of turbo mode is enabled. Note: the power-on default value is used by BIOS to detect hardware support of turbo mode. If power-on default value is 1, turbo mode is available in the processor. If power-on default value is 0, turbo mode is not available.</td>
<td></td>
</tr>
<tr>
<td>63:39</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1A2H 418</td>
<td>Thread</td>
<td>MSR_TEMPERATURE_TARGET</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td></td>
<td>Temperature Target (R)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The minimum temperature at which PROCHOT# will be asserted. The value is degree C.</td>
<td></td>
</tr>
<tr>
<td>63:24</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>1A4H 420</td>
<td>Core</td>
<td>MSR_MISC_FEATURE_CONTROL</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>L2 Hardware Prefetcher Disable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>If 1, disables the L2 hardware prefetcher, which fetches additional lines of code or data into the L2 cache.</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex</strong></td>
<td><strong>Dec</strong></td>
<td><strong>Register Name</strong></td>
<td><strong>Scope</strong></td>
</tr>
<tr>
<td>1</td>
<td>Core</td>
<td>14:0 Package</td>
<td>TDP Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TDP limit in 1/8 Watt granularity.</td>
</tr>
<tr>
<td>2</td>
<td>Core</td>
<td>15 Package</td>
<td>TDP Limit Override Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A value = 0 indicates override is not active, and a value = 1 indicates active.</td>
</tr>
<tr>
<td>3</td>
<td>Core</td>
<td>30:16 Package</td>
<td>TDC Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>TDC limit in 1/8 Amp granularity.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>31 Package</td>
<td>TDC Limit Override Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>A value = 0 indicates override is not active, and a value = 1 indicates active.</td>
</tr>
<tr>
<td>4</td>
<td>Core</td>
<td>63:32 Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td>5</td>
<td>Core</td>
<td>7:0 Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO[28] = 0, RW if MSR_PLATFORM_INFO[28] = 1</td>
</tr>
</tbody>
</table>

**Additional Notes:**

- **L2 Adjacent Cache Line Prefetcher Disable (R/W):**
  If 1, disables the adjacent cache line prefetcher, which fetches the cache line that comprises a cache line pair (128 bytes).

- **DCU Hardware Prefetcher Disable (R/W):**
  If 1, disables the L1 data cache prefetcher, which fetches the next cache line into L1 data cache.

- **DCU IP Prefetcher Disable (R/W):**
  If 1, disables the L1 data cache IP prefetcher, which uses sequential load history (based on instruction Pointer of previous loads) to determine whether to prefetch additional lines.

- **EIST Hardware Coordination Disable (R/W):**
  When 0, enables hardware coordination of Enhanced Intel Speedstep Technology request from processor cores; when 1, disables hardware coordination of Enhanced Intel Speedstep Technology requests.

- **Energy/Performance Bias Enable (R/W):**
  This bit makes the IA32_ENERGY_PERF_BIAS register (MSR 1B0h) visible to software with Ring 0 privileges. This bit's status (1 or 0) is also reflected by CPUID(EAX=06h):ECX[3].

- **TDP Limit Override Enable (R/W):**
  A value = 0 indicates override is not active, and a value = 1 indicates active.

- **TDC Limit Override Enable (R/W):**
  A value = 0 indicates override is not active, and a value = 1 indicates active.
<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 15:8 Package     | Maximum Ratio Limit for 2C  
Maximum turbo ratio limit of 2 core active. |
| 23:16 Package    | Maximum Ratio Limit for 3C  
Maximum turbo ratio limit of 3 core active. |
| 31:24 Package    | Maximum Ratio Limit for 4C  
Maximum turbo ratio limit of 4 core active. |
| 63:32            | Reserved.              |
| 1C8H 456         | MSR_LBR_SELECT Core    | Last Branch Record Filtering Select Register (R/W)  
See Section 17.6.2, “Filtering of Last Branch Records.” |
| 0                | CPL_EQ_0               |
| 1                | CPL_NEQ_0              |
| 2                | JCC                    |
| 3                | NEAR_REL_CALL          |
| 4                | NEAR_IND_CALL          |
| 5                | NEAR_RET               |
| 6                | NEAR_IND_JMP           |
| 7                | NEAR_REL_JMP           |
| 8                | FAR_BRANCH             |
| 63:9             | Reserved.              |
| 1C9H 457         | MSR_LASTBRANCH_TOS Thread | Last Branch Record Stack TOS (R/W)  
Contains an index (bits 0-3) that points to the MSR containing the  
most recent branch record.  
See MSR_LASTBRANCH_0_FROM_IP (at 680H). |
| 1D9H 473         | IA32_DEBUGCTL Thread   | Debug Control (R/W)  
See Table 35-2. |
| 1DDH 477         | MSR_LER_FROM_LIP Thread | Last Exception Record From Linear IP (R)  
Contains a pointer to the last branch instruction that the processor  
executed prior to the last exception that was generated or the last  
interrupt that was handled. |
| 1DEH 478         | MSR_LER_TO_LIP Thread  | Last Exception Record To Linear IP (R)  
This area contains a pointer to the target of the last branch  
instruction that the processor executed prior to the last exception  
that was generated or the last interrupt that was handled. |
| 1F2H 498         | IA32_SMRR_PHYSBASE Core | See Table 35-2. |
| 1F3H 499         | IA32_SMRR_PHYSMASK Core | See Table 35-2. |
| 1FCH 508         | MSR_POWER_CTL Core     | Power Control Register. See http://biosbits.org.  
Reserved. |
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tr>
<td>Hex</td>
<td>Dec</td>
<td>1</td>
<td>Package</td>
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<tr>
<td>200H</td>
<td>512</td>
<td>IA32_MTRR_PHYSBASE0</td>
<td>Thread</td>
</tr>
<tr>
<td>201H</td>
<td>513</td>
<td>IA32_MTRR_PHYSMASK0</td>
<td>Thread</td>
</tr>
<tr>
<td>202H</td>
<td>514</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>Thread</td>
</tr>
<tr>
<td>203H</td>
<td>515</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>Thread</td>
</tr>
<tr>
<td>204H</td>
<td>516</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>Thread</td>
</tr>
<tr>
<td>205H</td>
<td>517</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>Thread</td>
</tr>
<tr>
<td>206H</td>
<td>518</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>Thread</td>
</tr>
<tr>
<td>207H</td>
<td>519</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>Thread</td>
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<td>208H</td>
<td>520</td>
<td>IA32_MTRR_PHYSBASE4</td>
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<td>209H</td>
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<td>Thread</td>
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<td>20AH</td>
<td>522</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>Thread</td>
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<tr>
<td>20BH</td>
<td>523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>Thread</td>
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<tr>
<td>20CH</td>
<td>524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>Thread</td>
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<tr>
<td>20DH</td>
<td>525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>Thread</td>
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<td>20EH</td>
<td>526</td>
<td>IA32_MTRR_PHYSBASE7</td>
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<td>20FH</td>
<td>527</td>
<td>IA32_MTRR_PHYSMASK7</td>
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<td>210H</td>
<td>528</td>
<td>IA32_MTRR_PHYSBASE8</td>
<td>Thread</td>
</tr>
<tr>
<td>211H</td>
<td>529</td>
<td>IA32_MTRR_PHYSMASK8</td>
<td>Thread</td>
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<td>212H</td>
<td>530</td>
<td>IA32_MTRR_PHYSBASE9</td>
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<td>213H</td>
<td>531</td>
<td>IA32_MTRR_PHYSMASK9</td>
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<tr>
<td>250H</td>
<td>592</td>
<td>IA32_MTRR_FIX64K_00000</td>
<td>Thread</td>
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<tr>
<td>258H</td>
<td>600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>Thread</td>
</tr>
<tr>
<td>259H</td>
<td>601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>Thread</td>
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<td>268H</td>
<td>616</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>Thread</td>
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<tr>
<td>269H</td>
<td>617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>Thread</td>
</tr>
<tr>
<td>26AH</td>
<td>618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>Thread</td>
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<td>Thread</td>
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<tr>
<td>26CH</td>
<td>620</td>
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<td>26DH</td>
<td>621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>Thread</td>
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Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

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<th>Scope</th>
<th>Bit Description</th>
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<td>26EH 622</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<tr>
<td>26FH 623</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<td>277H 631</td>
<td>IA32_PAT</td>
<td>Thread</td>
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</tr>
<tr>
<td>280H 640</td>
<td>IA32_MC0_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>281H 641</td>
<td>IA32_MC1_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
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<td>282H 642</td>
<td>IA32_MC2_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
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<td>283H 643</td>
<td>IA32_MC3_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
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<td>284H 644</td>
<td>IA32_MC4_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>285H 645</td>
<td>IA32_MC5_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
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<td>286H 646</td>
<td>IA32_MC6_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>287H 647</td>
<td>IA32_MC7_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
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<td>288H 648</td>
<td>IA32_MC8_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>Thread</td>
<td>Default Memory Types (R/W)</td>
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<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>309H 777</td>
<td>IA32_FIXED_CTR0</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 0 (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>30AH 778</td>
<td>IA32_FIXED_CTR1</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 1 (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>30BH 779</td>
<td>IA32_FIXED_CTR2</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 2 (R/W) See Table 35-2.</td>
</tr>
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<td>345H 837</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>Thread</td>
<td>See Table 35-2. See Section 17.4.1, “IA32_DEBUGCTL MSR:”</td>
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<tr>
<td>5:0</td>
<td>LBR Format. See Table 35-2.</td>
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<tr>
<td>6</td>
<td>PEBS Record Format.</td>
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</tr>
<tr>
<td>7</td>
<td>PEBSSaveArchRegs. See Table 35-2.</td>
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</tr>
<tr>
<td>11:8</td>
<td>PEBS_REC_FORMAT. See Table 35-2.</td>
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</tr>
<tr>
<td>12</td>
<td>SMM_FREEZE. See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:13</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38DH 909</td>
<td>IA32_FIXED_CTR_CTRL</td>
<td>Thread</td>
<td>Fixed-Function-Counter Control Register (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>38EH 910</td>
<td>IA32_PERF_GLOBAL_STAUS</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>38EH 910</td>
<td>MSR_PERF_GLOBAL_STAUS</td>
<td>Thread</td>
<td>(RO)</td>
</tr>
<tr>
<td>61</td>
<td>UNC_Ovf</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Uncore overflowed if 1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
</tbody>
</table>
## Model-Specific Registers (MSRs)

Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>390H 912</td>
<td>MSR_PERF_GLOBAL_OVF_CTRL</td>
<td>Thread</td>
<td>(R/W)</td>
</tr>
<tr>
<td></td>
<td>61</td>
<td></td>
<td>CLR_UNC_Ovf</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Set 1 to clear UNC_Ovf.</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEBS_ENABLE</td>
<td>Thread</td>
<td>See Section 18.7.1.1, “Precise Event Based Sampling (PEBS).”</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Enable PEBS on IA32_PMC0. (R/W)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>Enable PEBS on IA32_PMC1. (R/W)</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>Enable PEBS on IA32_PMC2. (R/W)</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>Enable PEBS on IA32_PMC3. (R/W)</td>
</tr>
<tr>
<td></td>
<td>31:4</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td></td>
<td>Enable Load Latency on IA32_PMC0. (R/W)</td>
</tr>
<tr>
<td></td>
<td>33</td>
<td></td>
<td>Enable Load Latency on IA32_PMC1. (R/W)</td>
</tr>
<tr>
<td></td>
<td>34</td>
<td></td>
<td>Enable Load Latency on IA32_PMC2. (R/W)</td>
</tr>
<tr>
<td></td>
<td>35</td>
<td></td>
<td>Enable Load Latency on IA32_PMC3. (R/W)</td>
</tr>
<tr>
<td></td>
<td>63:36</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>3F6H 1014</td>
<td>MSR_PEBS_LD_LAT</td>
<td>Thread</td>
<td>See Section 18.7.1.2, “Load Latency Performance Monitoring Facility.”</td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td></td>
<td>Minimum threshold latency value of tagged load operation that will be counted. (R/W)</td>
</tr>
<tr>
<td></td>
<td>63:36</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>3F8H 1016</td>
<td>MSR_PKG_C3_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Package C3 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value since last reset that this package is in processor-specific C3 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>3F9H 1017</td>
<td>MSR_PKG_C6_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Package C6 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value since last reset that this package is in processor-specific C6 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>3FAH 1018</td>
<td>MSR_PKG_C7_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Package C7 Residency Counter. (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Value since last reset that this package is in processor-specific C7 states. Count at the same frequency as the TSC.</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3FCH 1020</td>
<td>MSR_CORE_C3_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 CORE C3 Residency Counter. (R/O) Value since last reset that this core is in processor-specific C3 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>3FDH 1021</td>
<td>MSR_CORE_C6_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:0 CORE C6 Residency Counter. (R/O) Value since last reset that this core is in processor-specific C6 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>400H 1024</td>
<td>IA32_MC0_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>401H 1025</td>
<td>IA32_MC0_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCi_ADDR MSRs.&quot; The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>403H 1027</td>
<td>MSR_MC0_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCi_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>406H 1030</td>
<td>IA32_MC1_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCi_ADDR MSRs.&quot; The IA32_MC1_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC1_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>407H 1031</td>
<td>MSR_MC1_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCi_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>40AH 1034</td>
<td>IA32_MC2_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCi_ADDR MSRs.&quot; The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>408H 1035</td>
<td>MSR_MC2_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCi_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>40CH 1036</td>
<td>MSR_MC3_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>40DH 1037</td>
<td>MSR_MC3_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>40EH 1038</td>
<td>MSR_MC3_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The MSR_MC4_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the MSR_MC4_STATUS register is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When not implemented in the processor, all reads and writes to this MSR will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>40FH 1039</td>
<td>MSR_MC3_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>410H 1040</td>
<td>MSR_MC4_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>411H 1041</td>
<td>MSR_MC4_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>412H 1042</td>
<td>MSR_MC4_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The MSR_MC3_ADDR register is either not implemented or contains no address if</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the ADDRV flag in the MSR_MC3_STATUS register is clear.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When not implemented in the processor, all reads and writes to this MSR will</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>cause a general-protection exception.</td>
</tr>
<tr>
<td>413H 1043</td>
<td>MSR_MC4_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>414H 1044</td>
<td>MSR_MC5_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>415H 1045</td>
<td>MSR_MC5_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>416H 1046</td>
<td>MSR_MC5_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>417H 1047</td>
<td>MSR_MC5_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>418H 1048</td>
<td>MSR_MC6_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>419H 1049</td>
<td>MSR_MC6_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs.&quot; and Chapter 16.</td>
</tr>
<tr>
<td>41AH 1050</td>
<td>MSR_MC6_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>41BH 1051</td>
<td>MSR_MC6_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>41CH 1052</td>
<td>MSR_MC7_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>41DH 1053</td>
<td>MSR_MC7_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs.&quot; and Chapter 16.</td>
</tr>
<tr>
<td>41EH 1054</td>
<td>MSR_MC7_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>41FH 1055</td>
<td>MSR_MC7_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>420H 1056</td>
<td>MSR_MC8_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>421H 1057</td>
<td>MSR_MC8_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs.&quot; and Chapter 16.</td>
</tr>
<tr>
<td>422H 1058</td>
<td>MSR_MC8_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>423H 1059</td>
<td>MSR_MC8_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>480H 1152</td>
<td>IA32_VMX_BASIC</td>
<td>Thread</td>
<td>Reporting Register of Basic VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.1, “Basic VMX Information.”</td>
</tr>
<tr>
<td>481H 1153</td>
<td>IA32_VMX_PINBASED_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>482H 1154</td>
<td>IA32_VMX_PROCBASED_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O) See Appendix A.3, &quot;VM-Execution Controls.&quot;</td>
</tr>
<tr>
<td>483H 1155</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of VM-exit Controls (R/O) See Table 35-2. See Appendix A.4, &quot;VM-Exit Controls.&quot;</td>
</tr>
<tr>
<td>484H 1156</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of VM-entry Controls (R/O) See Table 35-2. See Appendix A.5, &quot;VM-Entry Controls.&quot;</td>
</tr>
<tr>
<td>485H 1157</td>
<td>IA32_VMX_MISC</td>
<td>Thread</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O) See Table 35-2. See Appendix A.6, &quot;Miscellaneous Data.&quot;</td>
</tr>
<tr>
<td>486H 1158</td>
<td>IA32_VMX_CR0_FIXED0</td>
<td>Thread</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O) See Table 35-2. See Appendix A.7, &quot;VMX-Fixed Bits in CR0.&quot;</td>
</tr>
<tr>
<td>487H 1159</td>
<td>IA32_VMX_CR0_FIXED1</td>
<td>Thread</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O) See Table 35-2. See Appendix A.7, &quot;VMX-Fixed Bits in CR0.&quot;</td>
</tr>
<tr>
<td>488H 1160</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Thread</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O) See Table 35-2. See Appendix A.8, &quot;VMX-Fixed Bits in CR4.&quot;</td>
</tr>
<tr>
<td>489H 1161</td>
<td>IA32_VMX_CR4_FIXED1</td>
<td>Thread</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 1 (R/O) See Table 35-2. See Appendix A.8, &quot;VMX-Fixed Bits in CR4.&quot;</td>
</tr>
<tr>
<td>48AH 1162</td>
<td>IA32_VMX_VMCS_ENUM</td>
<td>Thread</td>
<td>Capability Reporting Register of VMCS Field Enumeration (R/O). See Table 35-2. See Appendix A.9, &quot;VMCS Enumeration.&quot;</td>
</tr>
<tr>
<td>48BH 1163</td>
<td>IA32_VMX_PROCBASED_CTLS2</td>
<td>Thread</td>
<td>Capability Reporting Register of Secondary Processor-based VM-execution Controls (R/O) See Appendix A.3, &quot;VM-Execution Controls.&quot;</td>
</tr>
<tr>
<td>600H 1536</td>
<td>IA32_DS_AREA</td>
<td>Thread</td>
<td>DS Save Area (R/W) See Table 35-2. See Section 18.12.4, &quot;Debug Store (DS) Mechanism.&quot;</td>
</tr>
<tr>
<td>680H 1664</td>
<td>MSR_LASTBRANCH_0_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 0 From IP (R/W) One of sixteen pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction for one of the last sixteen branches, exceptions, or interrupts taken by the processor. See also: • Last Branch Record Stack TOS at 1C9H • Section 17.6.1, &quot;LBR Stack.&quot;</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 681H 1665        | MSR_LASTBRANCH_1_FROM_IP       | Thread   | Last Branch Record 1 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 682H 1666        | MSR_LASTBRANCH_2_FROM_IP       | Thread   | Last Branch Record 2 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 683H 1667        | MSR_LASTBRANCH_3_FROM_IP       | Thread   | Last Branch Record 3 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 684H 1668        | MSR_LASTBRANCH_4_FROM_IP       | Thread   | Last Branch Record 4 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 685H 1669        | MSR_LASTBRANCH_5_FROM_IP       | Thread   | Last Branch Record 5 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 686H 1670        | MSR_LASTBRANCH_6_FROM_IP       | Thread   | Last Branch Record 6 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 687H 1671        | MSR_LASTBRANCH_7_FROM_IP       | Thread   | Last Branch Record 7 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 688H 1672        | MSR_LASTBRANCH_8_FROM_IP       | Thread   | Last Branch Record 8 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 689H 1673        | MSR_LASTBRANCH_9_FROM_IP       | Thread   | Last Branch Record 9 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68AH 1674        | MSR_LASTBRANCH_10_FROM_IP      | Thread   | Last Branch Record 10 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68BH 1675        | MSR_LASTBRANCH_11_FROM_IP      | Thread   | Last Branch Record 11 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68CH 1676        | MSR_LASTBRANCH_12_FROM_IP      | Thread   | Last Branch Record 12 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68DH 1677        | MSR_LASTBRANCH_13_FROM_IP      | Thread   | Last Branch Record 13 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68EH 1678        | MSR_LASTBRANCH_14_FROM_IP      | Thread   | Last Branch Record 14 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 68FH 1679        | MSR_LASTBRANCH_15_FROM_IP      | Thread   | Last Branch Record 15 From IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_FROM_IP.                                    |
| 6C0H 1728        | MSR_LASTBRANCH_0_TO_IP         | Thread   | Last Branch Record 0 To IP (R/W)
|                  |                                |          | One of sixteen pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the destination instruction for one of the last sixteen branches, exceptions, or interrupts taken by the processor. |
| 6C1H 1729        | MSR_LASTBRANCH_1_TO_IP         | Thread   | Last Branch Record 1 To IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_TO_IP.                                     |
| 6C2H 1730        | MSR_LASTBRANCH_2_TO_IP         | Thread   | Last Branch Record 2 To IP (R/W)
|                  |                                |          | See description of MSR_LASTBRANCH_0_TO_IP.                                     |
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6C3H 1731</td>
<td>MSR_LASTBRANCH_3_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 3 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C4H 1732</td>
<td>MSR_LASTBRANCH_4_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 4 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C5H 1733</td>
<td>MSR_LASTBRANCH_5_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 5 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C6H 1734</td>
<td>MSR_LASTBRANCH_6_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 6 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C7H 1735</td>
<td>MSR_LASTBRANCH_7_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 7 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C8H 1736</td>
<td>MSR_LASTBRANCH_8_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 8 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C9H 1737</td>
<td>MSR_LASTBRANCH_9_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 9 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CAH 1738</td>
<td>MSR_LASTBRANCH_10_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 10 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CBH 1739</td>
<td>MSR_LASTBRANCH_11_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 11 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CCH 1740</td>
<td>MSR_LASTBRANCH_12_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 12 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CDH 1741</td>
<td>MSR_LASTBRANCH_13_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 13 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CEH 1742</td>
<td>MSR_LASTBRANCH_14_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 14 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CFH 1743</td>
<td>MSR_LASTBRANCH_15_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 15 To IP (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>802H 2050</td>
<td>IA32_X2APIC_APICID</td>
<td>Thread</td>
<td>x2APIC ID register (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See x2APIC Specification.</td>
</tr>
<tr>
<td>803H 2051</td>
<td>IA32_X2APIC_VERSION</td>
<td>Thread</td>
<td>x2APIC Version register (R/O)</td>
</tr>
<tr>
<td>808H 2056</td>
<td>IA32_X2APIC_TPR</td>
<td>Thread</td>
<td>x2APIC Task Priority register (R/W)</td>
</tr>
<tr>
<td>80AH 2058</td>
<td>IA32_X2APIC_PPR</td>
<td>Thread</td>
<td>x2APIC Processor Priority register (R/O)</td>
</tr>
<tr>
<td>80BH 2059</td>
<td>IA32_X2APIC_EOI</td>
<td>Thread</td>
<td>x2APIC EOI register (W/O)</td>
</tr>
<tr>
<td>80DH 2061</td>
<td>IA32_X2APIC_LDR</td>
<td>Thread</td>
<td>x2APIC Logical Destination register (R/O)</td>
</tr>
<tr>
<td>80FH 2063</td>
<td>IA32_X2APIC_SIVR</td>
<td>Thread</td>
<td>x2APIC Spurious Interrupt Vector register (R/W)</td>
</tr>
<tr>
<td>810H 2064</td>
<td>IA32_X2APIC_ISR0</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [31:0] (R/W)</td>
</tr>
<tr>
<td>811H 2065</td>
<td>IA32_X2APIC_ISR1</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>812H 2066</td>
<td>IA32_X2APIC_ISR2</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [95:64] (R/O)</td>
</tr>
<tr>
<td>813H 2067</td>
<td>IA32_X2APIC_ISR3</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [127:96] (R/O)</td>
</tr>
</tbody>
</table>
### Table 35-11. MSRs in Processors Based on Intel® Microarchitecture Code Name Nehalem (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>814H</td>
<td>2068</td>
<td>IA32_X2APIC_ISR4</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>815H</td>
<td>2069</td>
<td>IA32_X2APIC_ISR5</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>816H</td>
<td>2070</td>
<td>IA32_X2APIC_ISR6</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>817H</td>
<td>2071</td>
<td>IA32_X2APIC_ISR7</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [255:224] (R/O)</td>
</tr>
<tr>
<td>818H</td>
<td>2072</td>
<td>IA32_X2APIC_TMR0</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [31:0] (R/O)</td>
</tr>
<tr>
<td>819H</td>
<td>2073</td>
<td>IA32_X2APIC_TMR1</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>81AH</td>
<td>2074</td>
<td>IA32_X2APIC_TMR2</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [95:64] (R/O)</td>
</tr>
<tr>
<td>81BH</td>
<td>2075</td>
<td>IA32_X2APIC_TMR3</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [127:96] (R/O)</td>
</tr>
<tr>
<td>81CH</td>
<td>2076</td>
<td>IA32_X2APIC_TMR4</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>81DH</td>
<td>2077</td>
<td>IA32_X2APIC_TMR5</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>81EH</td>
<td>2078</td>
<td>IA32_X2APIC_TMR6</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>81FH</td>
<td>2079</td>
<td>IA32_X2APIC_TMR7</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [255:224] (R/O)</td>
</tr>
<tr>
<td>820H</td>
<td>2080</td>
<td>IA32_X2APIC_IRR0</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [31:0] (R/O)</td>
</tr>
<tr>
<td>821H</td>
<td>2081</td>
<td>IA32_X2APIC_IRR1</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>822H</td>
<td>2082</td>
<td>IA32_X2APIC_IRR2</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [95:64] (R/O)</td>
</tr>
<tr>
<td>823H</td>
<td>2083</td>
<td>IA32_X2APIC_IRR3</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [127:96] (R/O)</td>
</tr>
<tr>
<td>824H</td>
<td>2084</td>
<td>IA32_X2APIC_IRR4</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>825H</td>
<td>2085</td>
<td>IA32_X2APIC_IRR5</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>826H</td>
<td>2086</td>
<td>IA32_X2APIC_IRR6</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>827H</td>
<td>2087</td>
<td>IA32_X2APIC_IRR7</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [255:224] (R/O)</td>
</tr>
<tr>
<td>828H</td>
<td>2088</td>
<td>IA32_X2APIC_ESR</td>
<td>Thread</td>
<td>x2APIC Error Status register (R/W)</td>
</tr>
<tr>
<td>829H</td>
<td>2089</td>
<td>IA32_X2APIC_LVT_CMI</td>
<td>Thread</td>
<td>x2APIC LVT Corrected Machine Check Interrupt register (R/W)</td>
</tr>
<tr>
<td>830H</td>
<td>2096</td>
<td>IA32_X2APIC_ICR</td>
<td>Thread</td>
<td>x2APIC Interrupt Command register (R/W)</td>
</tr>
<tr>
<td>832H</td>
<td>2098</td>
<td>IA32_X2APIC_LVT_TIMER</td>
<td>Thread</td>
<td>x2APIC LVT Timer Interrupt register (R/W)</td>
</tr>
<tr>
<td>833H</td>
<td>2099</td>
<td>IA32_X2APIC_LVT_THERMAL</td>
<td>Thread</td>
<td>x2APIC LVT Thermal Sensor Interrupt register (R/W)</td>
</tr>
<tr>
<td>834H</td>
<td>2100</td>
<td>IA32_X2APIC_LVT_PMI</td>
<td>Thread</td>
<td>x2APIC LVT Performance Monitor register (R/W)</td>
</tr>
<tr>
<td>835H</td>
<td>2101</td>
<td>IA32_X2APIC_LVT_LINT0</td>
<td>Thread</td>
<td>x2APIC LVT LINT0 register (R/W)</td>
</tr>
<tr>
<td>836H</td>
<td>2102</td>
<td>IA32_X2APIC_LVT_LINT1</td>
<td>Thread</td>
<td>x2APIC LVT LINT1 register (R/W)</td>
</tr>
<tr>
<td>837H</td>
<td>2103</td>
<td>IA32_X2APIC_LVT_ERROR</td>
<td>Thread</td>
<td>x2APIC LVT Error register (R/W)</td>
</tr>
<tr>
<td>838H</td>
<td>2104</td>
<td>IA32_X2APIC_INIT_COUNT</td>
<td>Thread</td>
<td>x2APIC Initial Count register (R/W)</td>
</tr>
<tr>
<td>839H</td>
<td>2105</td>
<td>IA32_X2APIC_CUR_COUNT</td>
<td>Thread</td>
<td>x2APIC Current Count register (R/O)</td>
</tr>
<tr>
<td>83EH</td>
<td>2110</td>
<td>IA32_X2APIC_DIV_CONF</td>
<td>Thread</td>
<td>x2APIC Divide Configuration register (R/W)</td>
</tr>
<tr>
<td>83FH</td>
<td>2111</td>
<td>IA32_X2APIC_SELF_IPI</td>
<td>Thread</td>
<td>x2APIC Self IPI register (W/O)</td>
</tr>
<tr>
<td>C000_</td>
<td>0080H</td>
<td>IA32_EFER</td>
<td>Thread</td>
<td>Extended Feature Enables</td>
</tr>
</tbody>
</table>

See Table 35-2.
35.5.1 Additional MSRs in the Intel® Xeon® Processor 5500 and 3400 Series

Intel Xeon Processor 5500 and 3400 series support additional model-specific registers listed in Table 35-12. These MSRs also apply to Intel Core i7 and i5 processor family CPUID signature with DisplayFamily_DisplayModel of 06_1AH, 06_1EH and 06_1FH, see Table 35-1.

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C000_0081H</td>
<td>IA32_STAR</td>
<td>Thread</td>
<td>System Call Target Address (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0082H</td>
<td>IA32_LSTAR</td>
<td>Thread</td>
<td>IA-32e Mode System Call Target Address (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0084H</td>
<td>IA32_FMASK</td>
<td>Thread</td>
<td>System Call Flag Mask (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0100H</td>
<td>IA32_FS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of FS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0101H</td>
<td>IA32_GS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of GS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0102H</td>
<td>IA32_KERNEL_GSBASE</td>
<td>Thread</td>
<td>Swap Target of BASE Address of GS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000_0103H</td>
<td>IA32_TSC_AUX</td>
<td>Thread</td>
<td>AUXILIARY TSC Signature. (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2 and Section 17.14.2, “IA32_TSC_AUX Register and RDTSCP Support.”</td>
</tr>
</tbody>
</table>

Table 35-12. Additional MSRs in Intel® Xeon® Processor 5500 and 3400 Series

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Actual maximum turbo frequency is multiplied by 133.33MHz. (not available to model 06_2EH)</td>
</tr>
<tr>
<td>7:0</td>
<td>Maximum Turbo Ratio Limit 1C (R/O)</td>
<td></td>
<td>Maximum Turbo mode ratio limit with 1 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Maximum Turbo Ratio Limit 2C (R/O)</td>
<td></td>
<td>Maximum Turbo mode ratio limit with 2 cores active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Maximum Turbo Ratio Limit 3C (R/O)</td>
<td></td>
<td>Maximum Turbo mode ratio limit with 3 cores active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Maximum Turbo Ratio Limit 4C (R/O)</td>
<td></td>
<td>Maximum Turbo mode ratio limit with 4 cores active.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>301H 769</td>
<td>MSR_GQ_SNOOP_MESF</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>From M to S (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>From E to S (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>From S to S (R/W)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-12. Additional MSRs in Intel® Xeon® Processor 5500 and 3400 Series (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>From F to S (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>From M to I (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>From E to I (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>From S to I (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>From F to I (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>391H</td>
<td>MSR_UNCORE_PERF_GLOBAL_CTRL Package See Section 18.7.2.1, “Uncore Performance Monitoring Management Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>392H</td>
<td>MSR_UNCORE_PERF_GLOBAL_STATUS Package See Section 18.7.2.1, “Uncore Performance Monitoring Management Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>393H</td>
<td>MSR_UNCORE_PERF_GLOBAL_OVF_CTRL Package See Section 18.7.2.1, “Uncore Performance Monitoring Management Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>394H</td>
<td>MSR_UNCORE_FIXED_CTRL Package See Section 18.7.2.1, “Uncore Performance Monitoring Management Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>395H</td>
<td>MSR_UNCORE_FIXED_CTRL Package See Section 18.7.2.1, “Uncore Performance Monitoring Management Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>396H</td>
<td>MSR_UNCORE_ADDR_OPCODE_MATCH Package See Section 18.7.2.3, “Uncore Address/Opcode Match MSR.”</td>
<td></td>
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<tr>
<td>3B0H</td>
<td>MSR_UNCORE_PMC0 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3B1H</td>
<td>MSR_UNCORE_PMC1 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3B2H</td>
<td>MSR_UNCORE_PMC2 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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<td></td>
</tr>
<tr>
<td>3B3H</td>
<td>MSR_UNCORE_PMC3 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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<tr>
<td>3B4H</td>
<td>MSR_UNCORE_PMC4 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
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</tr>
<tr>
<td>3B5H</td>
<td>MSR_UNCORE_PMC5 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
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<tr>
<td>3B6H</td>
<td>MSR_UNCORE_PMC6 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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<tr>
<td>3B7H</td>
<td>MSR_UNCORE_PMC7 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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<tr>
<td>3C0H</td>
<td>MSR_UNCORE_PERF_EVTSEL0 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
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</tr>
<tr>
<td>3C1H</td>
<td>MSR_UNCORE_PERF_EVTSEL1 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
<td></td>
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</tr>
<tr>
<td>3C2H</td>
<td>MSR_UNCORE_PERF_EVTSEL2 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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</tr>
<tr>
<td>3C3H</td>
<td>MSR_UNCORE_PERF_EVTSEL3 Package See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
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</table>
35.5.2 Additional MSRs in the Intel® Xeon® Processor 7500 Series

Intel Xeon Processor 7500 series support MSRs listed in Table 35-11 (except MSR address 1ADH) and additional model-specific registers listed in Table 35-13. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2EH.

Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C4H 948</td>
<td>MSR_UNCORE_PERFEVTSEL4</td>
<td>Package</td>
<td>See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
</tr>
<tr>
<td>3C5H 949</td>
<td>MSR_UNCORE_PERFEVTSEL5</td>
<td>Package</td>
<td>See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
</tr>
<tr>
<td>3C6H 950</td>
<td>MSR_UNCORE_PERFEVTSEL6</td>
<td>Package</td>
<td>See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
</tr>
<tr>
<td>3C7H 951</td>
<td>MSR_UNCORE_PERFEVTSEL7</td>
<td>Package</td>
<td>See Section 18.7.2.2, “Uncore Performance Event Configuration Facility.”</td>
</tr>
</tbody>
</table>
| 1ADH 429         | MSR_TURBO_RATIO_LIMIT            | Package  | Reserved
  Attempt to read/write will cause #UD. |
| 289H 649         | IA32_MC9_CTL2                    | Package  | See Table 35-2.                                               |
| 28AH 650         | IA32_MC10_CTL2                   | Package  | See Table 35-2.                                               |
| 28BH 651         | IA32_MC11_CTL2                   | Package  | See Table 35-2.                                               |
| 28CH 652         | IA32_MC12_CTL2                   | Package  | See Table 35-2.                                               |
| 28DH 653         | IA32_MC13_CTL2                   | Package  | See Table 35-2.                                               |
| 28EH 654         | IA32_MC14_CTL2                   | Package  | See Table 35-2.                                               |
| 28FH 655         | IA32_MC15_CTL2                   | Package  | See Table 35-2.                                               |
| 290H 656         | IA32_MC16_CTL2                   | Package  | See Table 35-2.                                               |
| 291H 657         | IA32_MC17_CTL2                   | Package  | See Table 35-2.                                               |
| 292H 658         | IA32_MC18_CTL2                   | Package  | See Table 35-2.                                               |
| 293H 659         | IA32_MC19_CTL2                   | Package  | See Table 35-2.                                               |
| 294H 660         | IA32_MC20_CTL2                   | Package  | See Table 35-2.                                               |
| 295H 661         | IA32_MC21_CTL2                   | Package  | See Table 35-2.                                               |
| 394H 816         | MSR_W_PMON_FIXED_CTR             | Package  | Uncore W-box perfmon fixed counter                              |
| 395H 817         | MSR_W_PMON_FIXED_CTR_CTL         | Package  | Uncore U-box perfmon fixed counter control MSR                 |
| 424H 1060        | MSR_MC9_CTL                      | Package  | See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”                     |
| 425H 1061        | MSR_MC9_STATUS                   | Package  | See Section 15.3.2.2, “IA32_MCI_STATUS MSRS,” and Chapter 16.  |
| 426H 1062        | MSR_MC9_ADDR                     | Package  | See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”                     |
## Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>427H 1063</td>
<td>MSR_MC9_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>428H 1064</td>
<td>MSR_MC10_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>429H 1065</td>
<td>MSR_MC10_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>42AH 1066</td>
<td>MSR_MC10_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>42BH 1067</td>
<td>MSR_MC10_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>42CH 1068</td>
<td>MSR_MC11_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>42DH 1069</td>
<td>MSR_MC11_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>42EH 1070</td>
<td>MSR_MC11_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>42FH 1071</td>
<td>MSR_MC11_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>430H 1072</td>
<td>MSR_MC12_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>431H 1073</td>
<td>MSR_MC12_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>432H 1074</td>
<td>MSR_MC12_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>433H 1075</td>
<td>MSR_MC12_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>434H 1076</td>
<td>MSR_MC13_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>435H 1077</td>
<td>MSR_MC13_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>436H 1078</td>
<td>MSR_MC13_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>437H 1079</td>
<td>MSR_MC13_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>438H 1080</td>
<td>MSR_MC14_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>439H 1081</td>
<td>MSR_MC14_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>43AH 1082</td>
<td>MSR_MC14_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>43BH 1083</td>
<td>MSR_MC14_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>43CH 1084</td>
<td>MSR_MC15_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>43DH 1085</td>
<td>MSR_MC15_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>43EH 1086</td>
<td>MSR_MC15_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>43FH 1087</td>
<td>MSR_MC15_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>440H 1088</td>
<td>MSR_MC16_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>441H 1089</td>
<td>MSR_MC16_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>442H 1090</td>
<td>MSR_MC16_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>443H 1091</td>
<td>MSR_MC16_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>448H 1096</td>
<td>MSR_MC18_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>449H 1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>44AH 1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>44BH 1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>--------------------------------</td>
<td>------------------</td>
<td>------------------------------------------------------</td>
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<tr>
<td>Hex, Dec</td>
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<tr>
<td>44CH 1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>44DH 1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRS,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>44EH 1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>44FH 1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>450H 1104</td>
<td>MSR_MC20_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MG_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>451H 1105</td>
<td>MSR_MC20_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MG_STATUS MSRS,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>452H 1106</td>
<td>MSR_MC20_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MG_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>453H 1107</td>
<td>MSR_MC20_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MG_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>454H 1108</td>
<td>MSR_MC21_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MG_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>455H 1109</td>
<td>MSR_MC21_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, &quot;IA32_MG_STATUS MSRS,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>456H 1110</td>
<td>MSR_MC21_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, &quot;IA32_MG_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>457H 1111</td>
<td>MSR_MC21_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, &quot;IA32_MG_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>C00H 3072</td>
<td>MSR_U_PMON_GLOBAL_CTRL</td>
<td>Package</td>
<td>Uncore U-box perfmon global control MSR.</td>
</tr>
<tr>
<td>C01H 3073</td>
<td>MSR_U_PMON_GLOBAL_STATUS</td>
<td>Package</td>
<td>Uncore U-box perfmon global status MSR.</td>
</tr>
<tr>
<td>C02H 3074</td>
<td>MSR_U_PMON_GLOBAL_OVF_CTRL</td>
<td>Package</td>
<td>Uncore U-box perfmon global overflow control MSR.</td>
</tr>
<tr>
<td>C10H 3088</td>
<td>MSR_U_PMON_EVNT_SEL</td>
<td>Package</td>
<td>Uncore U-box perfmon event select MSR.</td>
</tr>
<tr>
<td>C11H 3089</td>
<td>MSR_U_PMON_CTR</td>
<td>Package</td>
<td>Uncore U-box perfmon counter MSR.</td>
</tr>
<tr>
<td>C20H 3104</td>
<td>MSR_B0_PMON_BOX_CTRL</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon local box control MSR.</td>
</tr>
<tr>
<td>C21H 3105</td>
<td>MSR_B0_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon local box status MSR.</td>
</tr>
<tr>
<td>C22H 3106</td>
<td>MSR_B0_PMON_BOX_OVF_CTRL</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon local box overflow control MSR.</td>
</tr>
<tr>
<td>C30H 3120</td>
<td>MSR_B0_PMON_EVNT_SEL0</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>C31H 3121</td>
<td>MSR_B0_PMON_CTR0</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>C32H 3122</td>
<td>MSR_B0_PMON_EVNT_SEL1</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>C33H 3123</td>
<td>MSR_B0_PMON_CTR1</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>C34H 3124</td>
<td>MSR_B0_PMON_EVNT_SEL2</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>C35H 3125</td>
<td>MSR_B0_PMON_CTR2</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>C36H 3126</td>
<td>MSR_B0_PMON_EVNT_SEL3</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>C37H 3127</td>
<td>MSR_B0_PMON_CTR3</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon counter MSR.</td>
</tr>
</tbody>
</table>
### Model-Specific Registers (MSRs)

**Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
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<td>MSR_S0_PMON_BOX_CTRL</td>
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<tr>
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<td>MSR_B1_PMON_EVNT_SEL3</td>
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<tr>
<td>C77H 3191</td>
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### Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

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<td>Package</td>
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<td>CA5H 3237</td>
<td>MSR_M0_PMON_DSP</td>
<td>Package</td>
<td>Uncore M-box 0 perfmon DSP unit select MSR.</td>
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<tr>
<td>CA6H 3238</td>
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<td>Package</td>
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<td>CA9H 3241</td>
<td>MSR_M0_PMON_PGT</td>
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<td>Uncore M-box 0 perfmon PGT unit select MSR.</td>
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<tr>
<td>CAAH 3242</td>
<td>MSR_M0_PMON_PLD</td>
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<tr>
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<td>MSR_M0_PMON_CTR1</td>
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<td>MSR_M0_PMON_EVNT_SEL2</td>
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<td>CB5H 3253</td>
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### Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

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<th>Register Address</th>
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<th>Bit Description</th>
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<tr>
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### Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

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### Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

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<tr>
<td>E08H 3592</td>
<td>MSR_RO_PMON_IPERFO_P4</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon IPERFO unit Port 4 select MSR.</td>
</tr>
<tr>
<td>E09H 3593</td>
<td>MSR_RO_PMON_IPERFO_P5</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon IPERFO unit Port 5 select MSR.</td>
</tr>
<tr>
<td>E0AH 3594</td>
<td>MSR_RO_PMON_IPERFO_P6</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon IPERFO unit Port 6 select MSR.</td>
</tr>
<tr>
<td>E0BH 3595</td>
<td>MSR_RO_PMON_IPERFO_P7</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon IPERFO unit Port 7 select MSR.</td>
</tr>
<tr>
<td>E0CH 3596</td>
<td>MSR_RO_PMON_QLX_P0</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon QLX unit Port 0 select MSR.</td>
</tr>
<tr>
<td>E0DH 3597</td>
<td>MSR_RO_PMON_QLX_P1</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon QLX unit Port 1 select MSR.</td>
</tr>
<tr>
<td>E0EH 3598</td>
<td>MSR_RO_PMON_QLX_P2</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon QLX unit Port 2 select MSR.</td>
</tr>
<tr>
<td>E0FH 3599</td>
<td>MSR_RO_PMON_QLX_P3</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon QLX unit Port 3 select MSR.</td>
</tr>
<tr>
<td>E10H 3600</td>
<td>MSR_RO_PMON_EVNT_SEL0</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event event select MSR.</td>
</tr>
<tr>
<td>E11H 3601</td>
<td>MSR_RO_PMON_CTR0</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
</tbody>
</table>
### Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E12H 3602</td>
<td>MSR_R0_PMON_EVNT_SEL1</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E13H 3603</td>
<td>MSR_R0_PMON_CTR1</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E14H 3604</td>
<td>MSR_R0_PMON_EVNT_SEL2</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E15H 3605</td>
<td>MSR_R0_PMON_CTR2</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E16H 3606</td>
<td>MSR_R0_PMON_EVNT_SEL3</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E17H 3607</td>
<td>MSR_R0_PMON_CTR3</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E18H 3608</td>
<td>MSR_R0_PMON_EVNT_SEL4</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E19H 3609</td>
<td>MSR_R0_PMON_CTR4</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E1AH 3610</td>
<td>MSR_R0_PMON_EVNT_SEL5</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E1BH 3611</td>
<td>MSR_R0_PMON_CTR5</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E1CH 3612</td>
<td>MSR_R0_PMON_EVNT_SEL6</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E1DH 3613</td>
<td>MSR_R0_PMON_CTR6</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E1EH 3614</td>
<td>MSR_R0_PMON_EVNT_SEL7</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon event select MSR.</td>
</tr>
<tr>
<td>E1FH 3615</td>
<td>MSR_R0_PMON_CTR7</td>
<td>Package</td>
<td>Uncore R-box 0 perfmon counter MSR.</td>
</tr>
<tr>
<td>E20H 3616</td>
<td>MSR_R1_PMON_BOX_CTRL</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon local box control MSR.</td>
</tr>
<tr>
<td>E21H 3617</td>
<td>MSR_R1_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon local box status MSR.</td>
</tr>
<tr>
<td>E22H 3618</td>
<td>MSR_R1_PMON_BOX_OVF_CTRL</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon local box overflow control MSR.</td>
</tr>
<tr>
<td>E24H 3620</td>
<td>MSR_R1_PMON_IPERF1_P8</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 8 select MSR.</td>
</tr>
<tr>
<td>E25H 3621</td>
<td>MSR_R1_PMON_IPERF1_P9</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 9 select MSR.</td>
</tr>
<tr>
<td>E26H 3622</td>
<td>MSR_R1_PMON_IPERF1_P10</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 10 select MSR.</td>
</tr>
<tr>
<td>E27H 3623</td>
<td>MSR_R1_PMON_IPERF1_P11</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 11 select MSR.</td>
</tr>
<tr>
<td>E28H 3624</td>
<td>MSR_R1_PMON_IPERF1_P12</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 12 select MSR.</td>
</tr>
<tr>
<td>E29H 3625</td>
<td>MSR_R1_PMON_IPERF1_P13</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 13 select MSR.</td>
</tr>
<tr>
<td>E2AH 3626</td>
<td>MSR_R1_PMON_IPERF1_P14</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 14 select MSR.</td>
</tr>
<tr>
<td>E2BH 3627</td>
<td>MSR_R1_PMON_IPERF1_P15</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon IPERF1 unit Port 15 select MSR.</td>
</tr>
</tbody>
</table>
## Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2CH 3628</td>
<td>MSR_R1_PMON_QLX_P4</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon QLX unit Port 4 select MSR.</td>
</tr>
<tr>
<td>E2DH 3629</td>
<td>MSR_R1_PMON_QLX_P5</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon QLX unit Port 5 select MSR.</td>
</tr>
<tr>
<td>E2EH 3630</td>
<td>MSR_R1_PMON_QLX_P6</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon QLX unit Port 6 select MSR.</td>
</tr>
<tr>
<td>E2FH 3631</td>
<td>MSR_R1_PMON_QLX_P7</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon QLX unit Port 7 select MSR.</td>
</tr>
<tr>
<td>E30H 3632</td>
<td>MSR_R1_PMON_EVT_SEL8</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E31H 3633</td>
<td>MSR_R1_PMON_CTR8</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E32H 3634</td>
<td>MSR_R1_PMON_EVT_SEL9</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E33H 3635</td>
<td>MSR_R1_PMON_CTR9</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E34H 3636</td>
<td>MSR_R1_PMON_EVT_SEL10</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E35H 3637</td>
<td>MSR_R1_PMON_CTR10</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E36H 3638</td>
<td>MSR_R1_PMON_EVT_SEL11</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E37H 3639</td>
<td>MSR_R1_PMON_CTR11</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E38H 3640</td>
<td>MSR_R1_PMON_EVT_SEL12</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E39H 3641</td>
<td>MSR_R1_PMON_CTR12</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E3AH 3642</td>
<td>MSR_R1_PMON_EVT_SEL13</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E3BH 3643</td>
<td>MSR_R1_PMON_CTR13</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E3CH 3644</td>
<td>MSR_R1_PMON_EVT_SEL14</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E3DH 3645</td>
<td>MSR_R1_PMON_CTR14</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E3EH 3646</td>
<td>MSR_R1_PMON_EVT_SEL15</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon event select MSR.</td>
</tr>
<tr>
<td>E3FH 3647</td>
<td>MSR_R1_PMON_CTR15</td>
<td>Package</td>
<td>Uncore R-box 1 perfmon counter MSR.</td>
</tr>
<tr>
<td>E45H 3653</td>
<td>MSR_B0_PMON_MATCH</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon local box match MSR.</td>
</tr>
<tr>
<td>E46H 3654</td>
<td>MSR_B0_PMON_MASK</td>
<td>Package</td>
<td>Uncore B-box 0 perfmon local box mask MSR.</td>
</tr>
<tr>
<td>E49H 3657</td>
<td>MSR_S0_PMON_MATCH</td>
<td>Package</td>
<td>Uncore S-box 0 perfmon local box mask MSR.</td>
</tr>
<tr>
<td>E4AH 3658</td>
<td>MSR_S0_PMON_MASK</td>
<td>Package</td>
<td>Uncore S-box 0 perfmon local box mask MSR.</td>
</tr>
<tr>
<td>E4DH 3661</td>
<td>MSR_B1_PMON_MATCH</td>
<td>Package</td>
<td>Uncore B-box 1 perfmon local box match MSR.</td>
</tr>
<tr>
<td>E4EH 3662</td>
<td>MSR_B1_PMON_MASK</td>
<td>Package</td>
<td>Uncore B-box 1 perfmon local box mask MSR.</td>
</tr>
<tr>
<td>E54H 3668</td>
<td>MSR_MO_PMON_MM_CONFIG</td>
<td>Package</td>
<td>Uncore M-box 0 perfmon local box address match/mask config MSR.</td>
</tr>
<tr>
<td>E55H 3669</td>
<td>MSR_MO_PMON_ADDR_MATCH</td>
<td>Package</td>
<td>Uncore M-box 0 perfmon local box address match MSR.</td>
</tr>
</tbody>
</table>
35.6 MSRS IN THE INTEL® XEON® PROCESSOR 5600 SERIES (BASED ON INTEL® MICROARCHITECTURE CODE NAME WESTMERE)

Intel® Xeon® Processor 5600 Series (based on Intel® microarchitecture code name Westmere) supports the MSR interfaces listed in Table 35-11, Table 35-12, plus additional MSR listed in Table 35-14. These MSRs apply to Intel Core i7, i5 and i3 processor family with CPUID signature DisplayFamily_DisplayModel of 06_25H and 06_2CH, see Table 35-1.

Table 35-13. Additional MSRs in Intel® Xeon® Processor 7500 Series (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E56H 3670</td>
<td>MSR_M0_PMON_ADDR_Mask</td>
<td>Package</td>
<td>Uncore M-box 0 perfmon local box address mask MSR.</td>
</tr>
<tr>
<td>E59H 3673</td>
<td>MSR_S1_PMON_MATCH</td>
<td>Package</td>
<td>Uncore S-box 1 perfmon local box match MSR.</td>
</tr>
<tr>
<td>E5AH 3674</td>
<td>MSR_S1_PMON_MASK</td>
<td>Package</td>
<td>Uncore S-box 1 perfmon local box mask MSR.</td>
</tr>
<tr>
<td>E5CH 3676</td>
<td>MSR_M1_PMON_MM_CONFIG</td>
<td>Package</td>
<td>Uncore M-box 1 perfmon local box address match/mask config MSR.</td>
</tr>
<tr>
<td>E5DH 3677</td>
<td>MSR_M1_PMON_ADDR_MATCH</td>
<td>Package</td>
<td>Uncore M-box 1 perfmon local box address match MSR.</td>
</tr>
<tr>
<td>E5EH 3678</td>
<td>MSR_M1_PMON_ADDR_MASK</td>
<td>Package</td>
<td>Uncore M-box 1 perfmon local box address mask MSR.</td>
</tr>
<tr>
<td>3B5H 965</td>
<td>MSR_UNCORE_PMC5</td>
<td>Package</td>
<td>See Section 18.7.2.2, &quot;Uncore Performance Event Configuration Facility.&quot;</td>
</tr>
</tbody>
</table>

Table 35-14. Additional MSRs Supported by Intel Processors (Based on Intel® Microarchitecture Code Name Westmere)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13CH 52</td>
<td>MSR_FEATURE_CONFIG</td>
<td>Core</td>
<td>AES Configuration (RW-L)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Privileged post-BIOS agent must provide a #GP handler to handle unsuccessful read of this MSR.</td>
</tr>
<tr>
<td>1:0</td>
<td></td>
<td></td>
<td>AES Configuration (RW-L)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Upon a successful read of this MSR, the configuration of AES instruction set availability is as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11b: AES instructions are not available until next RESET. otherwise, AES instructions are available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note, AES instruction set is not available if read is unsuccessful. If the configuration is not 01b, AES instruction can be mis-configured if a privileged agent unintentionally writes 11b.</td>
</tr>
<tr>
<td>63:2</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>1A7H 423</td>
<td>MSR_OFFCORE_RSP_1</td>
<td>Thread</td>
<td>Offcore Response Event Select Register (R/W)</td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rw if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
</tbody>
</table>
35.7 MSRS IN THE INTEL® XEON® PROCESSOR E7 FAMILY (BASED ON INTEL® MICROARCHITECTURE CODE NAME WESTMERE)

Intel® Xeon® Processor E7 Family (based on Intel® microarchitecture code name Westmere) supports the MSR interfaces listed in Table 35-11 (except MSR address 1ADH), Table 35-12, plus additional MSR listed in Table 35-15. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2FH.

Table 35-15. Additional MSRs Supported by Intel® Xeon® Processor E7 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13CH 52</td>
<td>MSR_FEATURE_CONFIG</td>
<td>Core</td>
<td>AES Configuration (Rw-L)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Privileged post-BIOS agent must provide a #GP handler to handle unsuccessful read of this MSR.</td>
</tr>
<tr>
<td>1:0</td>
<td></td>
<td></td>
<td>AES Configuration (Rw-L)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Upon a successful read of this MSR, the configuration of AES instruction set availability is as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11b: AES instructions are not available until next RESET.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>otherwise, AES instructions are available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note, AES instruction set is not available if read is unsuccessful. If the configuration is not 01b, AES instruction can be mis-configured if a privileged agent unintentionally writes 11b.</td>
</tr>
<tr>
<td>63:2</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>1A7H 423</td>
<td>MSR_OFFCORE_RSP_1</td>
<td>Thread</td>
<td>Offcore Response Event Select Register (R/w)</td>
</tr>
</tbody>
</table>
### Table 35-15. Additional MSRs Supported by Intel® Xeon® Processor E7 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ADH</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Attempt to read/write will cause #UD.</td>
</tr>
<tr>
<td>1B0H</td>
<td>IA32_ENERGY_PERF_BIAS</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>F40H</td>
<td>MSR_C8_PMON_BOX_CTRL</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon local box control MSR.</td>
</tr>
<tr>
<td>F41H</td>
<td>MSR_C8_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon local box status MSR.</td>
</tr>
<tr>
<td>F42H</td>
<td>MSR_C8_PMON_BOX_OVF_CTRL</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon local box overflow control MSR.</td>
</tr>
<tr>
<td>F50H</td>
<td>MSR_C8_PMON_EVNT_SEL0</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F51H</td>
<td>MSR_C8_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter MSR.</td>
</tr>
<tr>
<td>F52H</td>
<td>MSR_C8_PMON_EVNT_SEL1</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F53H</td>
<td>MSR_C8_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter MSR.</td>
</tr>
<tr>
<td>F54H</td>
<td>MSR_C8_PMON_EVNT_SEL2</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F55H</td>
<td>MSR_C8_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter MSR.</td>
</tr>
<tr>
<td>F56H</td>
<td>MSR_C8_PMON_EVNT_SEL3</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F57H</td>
<td>MSR_C8_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter MSR.</td>
</tr>
<tr>
<td>F58H</td>
<td>MSR_C8_PMON_EVNT_SEL4</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F59H</td>
<td>MSR_C8_PMON_CTR4</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter MSR.</td>
</tr>
<tr>
<td>F5AH</td>
<td>MSR_C8_PMON_EVNT_SEL5</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon event select MSR.</td>
</tr>
<tr>
<td>F5BH</td>
<td>MSR_C9_PMON_BOX_CTRL</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon local box control MSR.</td>
</tr>
<tr>
<td>FC0H</td>
<td>MSR_C9_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon local box status MSR.</td>
</tr>
<tr>
<td>FC1H</td>
<td>MSR_C9_PMON_BOX_OVF_CTRL</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon local box overflow control MSR.</td>
</tr>
<tr>
<td>FC2H</td>
<td>MSR_C9_PMON_EVNT_SEL0</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FD0H</td>
<td>MSR_C9_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
<tr>
<td>FD1H</td>
<td>MSR_C9_PMON_EVNT_SEL1</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FD2H</td>
<td>MSR_C9_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
</tbody>
</table>
Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDH 4052</td>
<td>MSR_C9_PMON_EVNT_SEL2</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FD5H 4053</td>
<td>MSR_C9_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
<tr>
<td>FD6H 4054</td>
<td>MSR_C9_PMON_EVNT_SEL3</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FD7H 4055</td>
<td>MSR_C9_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
<tr>
<td>FD8H 4056</td>
<td>MSR_C9_PMON_EVNT_SEL4</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FD9H 4057</td>
<td>MSR_C9_PMON_CTR4</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
<tr>
<td>FDAH 4058</td>
<td>MSR_C9_PMON_EVNT_SEL5</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select MSR.</td>
</tr>
<tr>
<td>FDBH 4059</td>
<td>MSR_C9_PMON_CTR5</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter MSR.</td>
</tr>
</tbody>
</table>

35.8 MSRS IN INTEL® PROCESSOR FAMILY BASED ON INTEL® MICROARCHITECTURE CODE NAME SANDY BRIDGE

Table 35-16 lists model-specific registers (MSRs) that are common to Intel® processor family based on Intel microarchitecture code name Sandy Bridge. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2AH, 06_2DH, see Table 35-1. Additional MSRs specific to 06_2AH are listed in Table 35-17.
<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3AH 58</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Thread</td>
<td>Control Features in Intel 64 Processor (R/W) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Lock (R/WL)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>Enable VMX inside SMX operation (R/WL)</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>Enable VMX outside SMX operation (R/WL)</td>
</tr>
<tr>
<td></td>
<td>14:8</td>
<td></td>
<td>SENTER local functions enables (R/WL)</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td>SENTER global functions enable (R/WL)</td>
</tr>
<tr>
<td>79H 121</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>Core</td>
<td>BIOS Update Trigger Register (W) See Table 35-2.</td>
</tr>
<tr>
<td>8BH 139</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>Thread</td>
<td>BIOS Update Signature ID (RO) See Table 35-2.</td>
</tr>
<tr>
<td>C1H 193</td>
<td>IA32_PMC0</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td>C2H 194</td>
<td>IA32_PMC1</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td>C3H 195</td>
<td>IA32_PMC2</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td>C4H 196</td>
<td>IA32_PMC3</td>
<td>Thread</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td>C5H 197</td>
<td>IA32_PMC4</td>
<td>Core</td>
<td>Performance Counter Register (if core not shared by threads)</td>
</tr>
<tr>
<td>C6H 198</td>
<td>IA32_PMC5</td>
<td>Core</td>
<td>Performance Counter Register (if core not shared by threads)</td>
</tr>
<tr>
<td>C7H 199</td>
<td>IA32_PMC6</td>
<td>Core</td>
<td>Performance Counter Register (if core not shared by threads)</td>
</tr>
<tr>
<td>C8H 200</td>
<td>IA32_PMC7</td>
<td>Core</td>
<td>Performance Counter Register (if core not shared by threads)</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
<td></td>
<td>Maximum Non-Turbo Ratio (R/O) The is the ratio of the frequency that invariant TSC runs at. Frequency = ratio * 100 MHz.</td>
</tr>
<tr>
<td></td>
<td>27:16</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>28</td>
<td></td>
<td>Programmable Ratio Limit for Turbo Mode (R/O) When set to 1, indicates that Programmable Ratio Limits for Turbo mode is enabled, and when set to 0, indicates Programmable Ratio Limits for Turbo mode is disabled.</td>
</tr>
<tr>
<td></td>
<td>29</td>
<td></td>
<td>Programmable TDP Limit for Turbo Mode (R/O) When set to 1, indicates that TDP Limits for Turbo mode are programmable, and when set to 0, indicates TDP Limit for Turbo mode is not programmable.</td>
</tr>
<tr>
<td></td>
<td>39:30</td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
Table 35-16. MSRs Supported by Intel® Processors
based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>47:40</td>
<td>Package</td>
<td>Maximum Efficiency Ratio (R/O)</td>
<td>The is the minimum ratio (maximum efficiency) that the processor can operate, in units of 100MHz.</td>
</tr>
<tr>
<td>63:48</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>E2H 226</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>2:0</td>
<td>Package</td>
<td>Package C-State Limit (R/W)</td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power), for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 000b: C0/C1 (no package C-state support) 001b: C2 010b: C6 no retention 011b: C6 retention 100b: C7 101b: C7s 111: No package C-state limit. Note: This field cannot be used to limit package C-state to C3.</td>
</tr>
<tr>
<td>9:3</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td>When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWAIT instructions</td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/W/O)</td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
<td></td>
</tr>
<tr>
<td>24:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>C3 state auto demotion enable (R/W)</td>
<td>When set, the processor will conditionally demote C6/C7 requests to C3 based on uncore auto-demote information.</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C1 state auto demotion enable (R/W)</td>
<td>When set, the processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information.</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Enable C3 undemotion (R/W)</td>
<td>When set, enables undemotion from demoted C3.</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Enable C1 undemotion (R/W)</td>
<td>When set, enables undemotion from demoted C1.</td>
<td></td>
</tr>
<tr>
<td>63:29</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-16. MSRs Supported by Intel® Processors
based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4H 228</td>
<td>MSR_PMG_IO_CAPTURE_BASE</td>
<td>Core</td>
<td>Power Management IO Redirection in C-state (R/W)</td>
</tr>
<tr>
<td>15:0</td>
<td>LVL_2 Base Address (R/W)</td>
<td></td>
<td>Specifies the base address visible to software for IO redirection. If</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IO MWAIT redirection is enabled, reads to this address will be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>consumed by the power management logic and decoded to MWAIT</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>instructions. When IO port address redirection is enabled, this is the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IO port address reported to the OS/software.</td>
</tr>
<tr>
<td>18:16</td>
<td>C-state Range (R/W)</td>
<td></td>
<td>Specifies the encoding value of the maximum C-State code name to be</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>included when IO read to MWAIT redirection is enabled by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MSR_PKG_CST_CONFIG_CONTROL[bit10]:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b - C3 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b - C6 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b - C7 is the max C-State to include</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:19 Reserved.</td>
</tr>
<tr>
<td>E7H 231</td>
<td>IA32_MPERF</td>
<td>Thread</td>
<td>Maximum Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>E8H 232</td>
<td>IA32_APERF</td>
<td>Thread</td>
<td>Actual Performance Frequency Clock Count (RW)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>13CH 52</td>
<td>MSR_FEATURE_CONFIG</td>
<td>Core</td>
<td>AES Configuration (Rw-L)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Privileged post-BIOS agent must provide a #GP handler to handle</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>unsuccessful read of this MSR.</td>
</tr>
<tr>
<td>1:0</td>
<td>AES Configuration (Rw-L)</td>
<td></td>
<td>Upon a successful read of this MSR, the configuration of AES</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>instruction set availability is as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11b: AES instructions are not available until next RESET.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>otherwise, AES instructions are available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note, AES instruction set is not available if read is unsuccessful. If</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the configuration is not 01b, AES instruction can be mis-configured</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>if a privileged agent unintentionally writes 11b.</td>
</tr>
<tr>
<td>63:2</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>174H 372</td>
<td>IA32_SYSENDER_CS</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H 373</td>
<td>IA32_SYSENDER_ESP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H 374</td>
<td>IA32_SYSENDER_EIP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS</td>
<td>Thread</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex</strong></td>
<td><strong>Dec</strong></td>
<td><strong>Register Name</strong></td>
<td><strong>Scope</strong></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>RIPV</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>EIPV</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>MCIP</td>
</tr>
<tr>
<td>63:3</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>186H</td>
<td>390</td>
<td>IA32_PERFEVTSEL0</td>
<td>Thread</td>
</tr>
<tr>
<td>187H</td>
<td>391</td>
<td>IA32_PERFEVTSEL1</td>
<td>Thread</td>
</tr>
<tr>
<td>188H</td>
<td>392</td>
<td>IA32_PERFEVTSEL2</td>
<td>Thread</td>
</tr>
<tr>
<td>189H</td>
<td>393</td>
<td>IA32_PERFEVTSEL3</td>
<td>Thread</td>
</tr>
<tr>
<td>18AH</td>
<td>394</td>
<td>IA32_PERFEVTSEL4</td>
<td>Core</td>
</tr>
<tr>
<td>188H</td>
<td>395</td>
<td>IA32_PERFEVTSEL5</td>
<td>Core</td>
</tr>
<tr>
<td>18CH</td>
<td>396</td>
<td>IA32_PERFEVTSEL6</td>
<td>Core</td>
</tr>
<tr>
<td>18DH</td>
<td>397</td>
<td>IA32_PERFEVTSEL7</td>
<td>Core</td>
</tr>
<tr>
<td>198H</td>
<td>408</td>
<td>IA32_PERF_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>198H</td>
<td>408</td>
<td>MSR_PERF_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>199H</td>
<td>409</td>
<td>IA32_PERF_CTL</td>
<td>Thread</td>
</tr>
</tbody>
</table>
### Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Thread</td>
<td>Clock Modulation (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IA32_CLOCK_MODULATION MSR was originally named</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IA32_THERM_CONTROL MSR.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3:0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>On demand Clock Modulation Duty Cycle (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>In 6.25% increment</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>On demand Clock Modulation Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Core</td>
<td>Thermal Interrupt Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Core</td>
<td>Thermal Monitor Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Thermal status (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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<td>Thermal status log (R/W/CO)</td>
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<td>PROTCHOT # or FORCEPR# status (RO)</td>
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<td>See Table 35-2</td>
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<td>PROTCHOT # or FORCEPR# log (R/W/CO)</td>
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<td>Critical Temperature status (RO)</td>
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<td>Critical Temperature status log (R/W/CO)</td>
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<td>Thermal threshold #1 status (RO)</td>
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<td>See Table 35-2</td>
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<td>Thermal threshold #1 log (R/W/CO)</td>
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<td>Thermal threshold #2 status (RO)</td>
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<td>Thermal threshold #2 log (R/W/CO)</td>
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<td>Power Limitation status (RO)</td>
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<td>See Table 35-2</td>
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<td>Power Limitation log (R/W/CO)</td>
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<td>22:16</td>
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<td>Digital Readout (RO)</td>
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Table 35-16. MSRs Supported by Intel® Processors
Based on Intel® microarchitecture code name Sandy Bridge (Contd.)

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<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tr>
<td>0x1A0 416</td>
<td>IA32_MISC_ENABLE</td>
<td></td>
<td><strong>Enable Misc. Processor Features (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
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<td>0</td>
<td>Thread</td>
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<td><strong>Fast-Strings Enable</strong></td>
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<td>6:1</td>
<td>Thread</td>
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<td>Thread</td>
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<td><strong>Performance Monitoring Available (R)</strong></td>
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<td>See Table 35-2</td>
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<td>Thread</td>
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<tr>
<td>11</td>
<td>Thread</td>
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<td><strong>Branch Trace Storage Unavailable (RO)</strong></td>
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<td></td>
<td>See Table 35-2</td>
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<td>Thread</td>
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<td><strong>Precise Event Based Sampling Unavailable (RO)</strong></td>
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<td>Package</td>
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</tr>
<tr>
<td>16</td>
<td>Package</td>
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<td><strong>Enhanced Intel SpeedStep Technology Enable (R/W)</strong></td>
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<td>See Table 35-2</td>
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<td>18</td>
<td>Thread</td>
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<td><strong>ENABLE MONITOR FSM. (R/W)</strong></td>
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<td>See Table 35-2</td>
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<td>21:19</td>
<td>Thread</td>
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<tr>
<td>22</td>
<td>Thread</td>
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<td><strong>Limit CPUID Maxval (R/W)</strong></td>
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<td></td>
<td></td>
<td>See Table 35-2</td>
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<tr>
<td>23</td>
<td>Thread</td>
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<td><strong>xTPR Message Disable (R/W)</strong></td>
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<tr>
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<td>See Table 35-2</td>
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<td>33:24</td>
<td>Thread</td>
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<td>Reserved.</td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td></td>
<td><strong>XD Bit Disable (R/W)</strong></td>
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<td>See Table 35-2</td>
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<td>37:35</td>
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Table 35-16. MSRs Supported by Intel® Processors
based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
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<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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</thead>
<tbody>
<tr>
<td>38</td>
<td>Turbo Mode Disable (R/W)</td>
<td>Package</td>
<td>When set to 1 on processors that support Intel Turbo Boost Technology, the turbo mode feature is disabled and the IDA_Enable feature flag will be clear (CPUID.06H: EAX[1]=0). When set to a 0 on processors that support IDA, CPUID.06H: EAX[1] reports the processor’s support of turbo mode is enabled. <strong>Note:</strong> the power-on default value is used by BIOS to detect hardware support of turbo mode. If power-on default value is 1, turbo mode is available in the processor. If power-on default value is 0, turbo mode is not available.</td>
</tr>
<tr>
<td>63:39</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A2H 418</td>
<td>MSR_TEMPERATURE_TARGET</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Temperature Target (R)</td>
<td></td>
<td>The minimum temperature at which PROCHOT# will be asserted. The value is degree C.</td>
</tr>
<tr>
<td>63:24</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A4H 420</td>
<td>MSR_MISC_FEATURE_CONTROL</td>
<td>Miscellaneous Feature Control (R/W)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>L2 Hardware Prefetcher Disable (R/W)</td>
<td>Core</td>
<td>If 1, disables the L2 hardware prefetcher, which fetches additional lines of code or data into the L2 cache.</td>
</tr>
<tr>
<td>1</td>
<td>L2 Adjacent Cache Line Prefetcher Disable (R/W)</td>
<td>Core</td>
<td>If 1, disables the adjacent cache line prefetcher, which fetches the cache line that comprises a cache line pair (128 bytes).</td>
</tr>
<tr>
<td>2</td>
<td>DCU Hardware Prefetcher Disable (R/W)</td>
<td>Core</td>
<td>If 1, disables the L1 data cache prefetcher, which fetches the next cache line into L1 data cache.</td>
</tr>
<tr>
<td>3</td>
<td>DCU IP Prefetcher Disable (R/W)</td>
<td>Core</td>
<td>If 1, disables the L1 data cache IP prefetcher, which uses sequential load history (based on Instruction Pointer of previous loads) to determine whether to prefetch additional lines.</td>
</tr>
<tr>
<td>63:4</td>
<td>Reserved.</td>
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</tr>
<tr>
<td>1A6H 422</td>
<td>MSR_OFFCORE_RSP_0</td>
<td>Thread</td>
<td>Offcore Response Event Select Register (R/W)</td>
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<tr>
<td>1A7H 422</td>
<td>MSR_OFFCORE_RSP_1</td>
<td>Thread</td>
<td>Offcore Response Event Select Register (R/W)</td>
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<tr>
<td>1AAH 426</td>
<td>MSR_MISC_PWR_MGMT</td>
<td>Thread</td>
<td>See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
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<td>1B0H 432</td>
<td>IA32_ENERGY_PERF_BIAS</td>
<td>Package</td>
<td>See Table 35-2.</td>
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<tr>
<td>1B1H 433</td>
<td>IA32_PACKAGE_THERM_STATUS</td>
<td>Package</td>
<td>See Table 35-2.</td>
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<tr>
<td>1B2H 434</td>
<td>IA32_PACKAGE_THERM_INTERRUPT</td>
<td>Package</td>
<td>See Table 35-2.</td>
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### Table 35-16. MSRs Supported by Intel® Processors
**based on Intel® microarchitecture code name Sandy Bridge (Contd.)**

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<tr>
<td>1C8H 456</td>
<td>MSR_LBR_SELECT</td>
<td>Thread</td>
<td>Last Branch Record Filtering Select Register (R/W)</td>
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<td>See Section 17.6.2, “Filtering of Last Branch Records.”</td>
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<td>CPL_EQ_0</td>
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<td>CPL_NEQ_0</td>
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<td>2</td>
<td>JCC</td>
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<td>3</td>
<td>NEAR_REL_CALL</td>
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<td>4</td>
<td>NEAR_IND_CALL</td>
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<td>5</td>
<td>NEAR_RET</td>
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<td>NEAR_IND_JMP</td>
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<td>NEAR_REL_JMP</td>
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<td>8</td>
<td>FAR_BRANCH</td>
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<td>63:9</td>
<td>Reserved.</td>
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<tr>
<td>1C9H 457</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Thread</td>
<td>Last Branch Record Stack TOS (R/W)</td>
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<tr>
<td></td>
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<td></td>
<td>Contains an index (bits 0-3) that points to the MSR</td>
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<td></td>
<td></td>
<td></td>
<td>containing the most recent branch record.</td>
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<td>See MSR_LASTBRANCH_0_FROM_IP (at 680H).</td>
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<td>1D9H 473</td>
<td>IA32_DEBUGCTL</td>
<td>Thread</td>
<td>Debug Control (R/W)</td>
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<td>LBR: Last Branch Record</td>
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<td>BTF</td>
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<td>6</td>
<td>TR: Branch Trace</td>
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<td>7</td>
<td>BTS: Log Branch Trace Message to BTS buffer</td>
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<td>BTINT</td>
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<td>BTS_OFF_OS</td>
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<td>BTS_OFF_USER</td>
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<td>FREEZE_LBR_ON_PMI</td>
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<td>FREEZE_PERFMON_ON_PMI</td>
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<td>ENABLE_UNCORE_PMI</td>
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<td>FREEZE_WHILE_SMM</td>
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<td>63:15</td>
<td>Reserved.</td>
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<td>1DDH 477</td>
<td>MSR_LER_FROM_LIP</td>
<td>Thread</td>
<td>Last Exception Record From Linear IP (R)</td>
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<td></td>
<td>Contains a pointer to the last branch instruction that</td>
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<tr>
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<td></td>
<td></td>
<td>the processor executed prior to the last exception that</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>was generated or the last interrupt that was handled.</td>
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Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
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<td>1DEH 478</td>
<td>MSR_LER_TO_LIP</td>
<td>Thread</td>
<td>Last Exception Record To Linear IP (R)</td>
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<tr>
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<td></td>
<td>This area contains a pointer to the target of the last branch instruction that</td>
</tr>
<tr>
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<td></td>
<td>the processor executed prior to the last exception that was generated or the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>last interrupt that was handled.</td>
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<td>1F2H 498</td>
<td>IA32_SMRR_PHYSBASE</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1F3H 499</td>
<td>IA32_SMRR_PHYSMASK</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1FCH 508</td>
<td>MSR_POWER_CTL</td>
<td>Core</td>
<td>See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
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<td>IA32_MTRR_PHYSBASE0</td>
<td>Thread</td>
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<td>IA32_MTRR_PHYSBASE1</td>
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<td>IA32_MTRR_PHYSBASE2</td>
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<td>IA32_MTRR_PHYSMASK2</td>
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<td>IA32_MTRR_PHYSBASE3</td>
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<td>IA32_MTRR_PHYSMASK3</td>
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<td>IA32_MTRR_PHYSBASE4</td>
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<td>IA32_MTRR_PHYSMASK4</td>
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<td>20AH 522</td>
<td>IA32_MTRR_PHYSBASE5</td>
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<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>Thread</td>
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<td>IA32_MTRR_PHYSBASE6</td>
<td>Thread</td>
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<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
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<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>Thread</td>
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<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>Thread</td>
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<td>210H 528</td>
<td>IA32_MTRR_PHYSBASE8</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<td>211H 529</td>
<td>IA32_MTRR_PHYSMASK8</td>
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<td>212H 530</td>
<td>IA32_MTRR_PHYSBASE9</td>
<td>Thread</td>
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<td>213H 531</td>
<td>IA32_MTRR_PHYSMASK9</td>
<td>Thread</td>
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<td>250H 592</td>
<td>IA32_MTRR_FIX64K_0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>269H 617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26AH 618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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### Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>26BH</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26CH</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26DH</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26EH</td>
<td>IA32_MTRR_FIX4K_F0000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26FH</td>
<td>IA32_MTRR_FIX4K_F8000</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>277H</td>
<td>IA32_PAT</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>280H</td>
<td>IA32_MC0_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>281H</td>
<td>IA32_MC1_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>282H</td>
<td>IA32_MC2_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>283H</td>
<td>IA32_MC3_CTL2</td>
<td>Core</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>284H</td>
<td>MSR_MC4_CTL2</td>
<td>Package</td>
<td>Always 0 (CMCI not supported).</td>
</tr>
<tr>
<td>2FFH</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>Thread</td>
<td>Default Memory Types (R/W)</td>
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<td></td>
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<td>See Table 35-2.</td>
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<tr>
<td>309H</td>
<td>IA32_FIXED_CTR0</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
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<tr>
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<td>See Table 35-2.</td>
</tr>
<tr>
<td>30AH</td>
<td>IA32_FIXED_CTR1</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 1 (R/W)</td>
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<tr>
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<td>See Table 35-2.</td>
</tr>
<tr>
<td>30BH</td>
<td>IA32_FIXED_CTR2</td>
<td>Thread</td>
<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
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<tr>
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<td></td>
<td>See Table 35-2.</td>
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<tr>
<td>345H</td>
<td>IA32_PERF_CAPABILITIES</td>
<td>Thread</td>
<td>See Table 35-2. Section 17.4.1, “IA32_DEBUGCTL MSR.”</td>
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<tr>
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<td></td>
<td></td>
<td>5:0 LBR Format.</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>6 PEBS Record Format.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7 PEBS_SaveArchRegs.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11:8 PEBS_REC_FORMAT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>12 SMM_FREEZE.</td>
</tr>
<tr>
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<td></td>
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<td>63:13 Reserved.</td>
</tr>
<tr>
<td>380H</td>
<td>IA32_FIXED_CTR_CTRL</td>
<td>Thread</td>
<td>Fixed-Function-Counter Control Register (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>38EH</td>
<td>IA32_PERF_GLOBAL_STATUS</td>
<td></td>
<td>See Table 35-2. Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thread</td>
<td>Ovf_PMC0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thread</td>
<td>Ovf_PMC1</td>
</tr>
<tr>
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<td></td>
<td>Thread</td>
<td>Ovf_PMC2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Thread</td>
<td>Ovf_PMC3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Core</td>
<td>Ovf_PMC4 (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Core</td>
<td>Ovf_PMC5 (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
</tr>
</tbody>
</table>
### Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
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<tr>
<td>6</td>
<td>Core</td>
<td>Ovf_PMC6 (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
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<tr>
<td>7</td>
<td>Core</td>
<td>Ovf_PMC7 (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
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<tr>
<td>31:8</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Ovf_FixedCtr0</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Ovf_FixedCtr1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Ovf_FixedCtr2</td>
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</tr>
<tr>
<td>60:35</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>61</td>
<td>Thread</td>
<td>Ovf_Uncore</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Thread</td>
<td>Ovf_BufDSSAVE</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Thread</td>
<td>CondChgd</td>
<td></td>
</tr>
<tr>
<td>38FH 911</td>
<td>IA32_PERF_GLOBAL_CTRL</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, &quot;Global Counter Control Facilities.&quot;</td>
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<tr>
<td>32</td>
<td>Thread</td>
<td>Set 1 to enable PMC0 to count</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Set 1 to enable PMC1 to count</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Set 1 to enable PMC2 to count</td>
<td></td>
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<tr>
<td>35</td>
<td>Thread</td>
<td>Set 1 to enable PMC3 to count</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Core</td>
<td>Set 1 to enable PMC4 to count (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
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</tr>
<tr>
<td>5</td>
<td>Core</td>
<td>Set 1 to enable PMC5 to count (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
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</tr>
<tr>
<td>6</td>
<td>Core</td>
<td>Set 1 to enable PMC6 to count (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
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<td>Core</td>
<td>Set 1 to enable PMC7 to count (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
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<tr>
<td>31:8</td>
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<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Set 1 to enable FixedCtr0 to count</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Set 1 to enable FixedCtr1 to count</td>
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<td>34</td>
<td>Thread</td>
<td>Set 1 to enable FixedCtr2 to count</td>
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<tr>
<td>63:35</td>
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<td></td>
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</tr>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
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<td>See Table 35-2. See Section 18.4.2, &quot;Global Counter Control Facilities.&quot;</td>
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<td>Thread</td>
<td>Set 1 to clear Ovf_PMC0</td>
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<tr>
<td>1</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC1</td>
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<tr>
<td>2</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC2</td>
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<tr>
<td>3</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Core</td>
<td>Set 1 to clear Ovf_PMC4 (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
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<tr>
<td>5</td>
<td>Core</td>
<td>Set 1 to clear Ovf_PMC5 (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
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<tr>
<td>6</td>
<td>Core</td>
<td>Set 1 to clear Ovf_PMC6 (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
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<tr>
<td>7</td>
<td>Core</td>
<td>Set 1 to clear Ovf_PMC7 (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_FixedCtr0</td>
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</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------------------</td>
<td>--------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Set 1</td>
<td>to clear Ovf_FixedCtr1</td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Set 1</td>
<td>to clear Ovf_FixedCtr2</td>
</tr>
<tr>
<td>60:35</td>
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</tr>
<tr>
<td>61</td>
<td>Thread</td>
<td>Set 1</td>
<td>to clear Ovf_Uncore</td>
</tr>
<tr>
<td>62</td>
<td>Thread</td>
<td>Set 1</td>
<td>to clear Ovf_BufDSSAVE</td>
</tr>
<tr>
<td>63</td>
<td>Thread</td>
<td>Set 1</td>
<td>to clear CondChgd</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEBS_ENABLE</td>
<td>Thread</td>
<td>See Section 18.7.1.1, “Precise Event Based Sampling (PEBS).”</td>
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<tr>
<td>0</td>
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<td></td>
<td>Enable PEBS on IA32_PMC0. (R/W)</td>
</tr>
<tr>
<td>1</td>
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<td>Enable PEBS on IA32_PMC1. (R/W)</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Enable PEBS on IA32_PMC2. (R/W)</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>Enable PEBS on IA32_PMC3. (R/W)</td>
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<td>31:4</td>
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<td>Reserved.</td>
</tr>
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<td>32</td>
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<td>Enable Load Latency on IA32_PMC0. (R/W)</td>
</tr>
<tr>
<td>33</td>
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<td>Enable Load Latency on IA32_PMC1. (R/W)</td>
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<td>34</td>
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<td></td>
<td>Enable Load Latency on IA32_PMC2. (R/W)</td>
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<td>35</td>
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<td></td>
<td>Enable Load Latency on IA32_PMC3. (R/W)</td>
</tr>
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<td>62:36</td>
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<td>Reserved.</td>
</tr>
<tr>
<td>63</td>
<td></td>
<td></td>
<td>Enable Precise Store. (R/W)</td>
</tr>
<tr>
<td>3F6H 1014</td>
<td>MSR_PEBS_LD_LAT</td>
<td>Thread</td>
<td>see See Section 18.7.1.2, “Load Latency Performance Monitoring Facility.”</td>
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<tr>
<td>15:0</td>
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<td></td>
<td>Minimum threshold latency value of tagged load operation that will be counted. (R/W)</td>
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<tr>
<td>63:36</td>
<td></td>
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<td>Reserved.</td>
</tr>
<tr>
<td>3F8H 1016</td>
<td>MSR_PKG_C3_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Package C3 Residency Counter. (R/O) Value since last reset that this package is in processor-specific C3 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>3F9H 1017</td>
<td>MSR_PKG_C6_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td>Package C6 Residency Counter. (R/O) Value since last reset that this package is in processor-specific C6 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>3FAH 1018</td>
<td>MSR_PKG_C7_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
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### Table 35-16. MSRs Supported by Intel® Processors (Contd.)

<table>
<thead>
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<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tbody>
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<td>Package C7 Residency Counter. (R/O)</td>
<td>Value since last reset that this package is in processor-specific C7 states. Count at the same frequency as the TSC.</td>
<td></td>
</tr>
<tr>
<td>3FCH 1020</td>
<td>MSR_CORE_C3_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
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<td>CORE C3 Residency Counter. (R/O)</td>
<td>Value since last reset that this core is in processor-specific C3 states. Count at the same frequency as the TSC.</td>
<td></td>
</tr>
<tr>
<td>3FDH 1021</td>
<td>MSR_CORE_C6_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>63:0</td>
<td>CORE C6 Residency Counter. (R/O)</td>
<td>Value since last reset that this core is in processor-specific C6 states. Count at the same frequency as the TSC.</td>
<td></td>
</tr>
<tr>
<td>3FEH 1022</td>
<td>MSR_CORE_C7_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>63:0</td>
<td>CORE C7 Residency Counter. (R/O)</td>
<td>Value since last reset that this core is in processor-specific C7 states. Count at the same frequency as the TSC.</td>
<td></td>
</tr>
<tr>
<td>400H 1024</td>
<td>IA32_MC0_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>401H 1025</td>
<td>IA32_MC0_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>403H 1027</td>
<td>IA32_MC0_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>406H 1030</td>
<td>IA32_MC1_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>407H 1031</td>
<td>IA32_MC1_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>40AH 1034</td>
<td>IA32_MC2_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>40BH 1035</td>
<td>IA32_MC2_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
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<tr>
<td>40CH 1036</td>
<td>IA32_MC3_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
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<td>40DH 1037</td>
<td>IA32_MC3_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, &quot;IA32_MCI_STATUS MSRs,&quot; and Chapter 16.</td>
</tr>
<tr>
<td>40EH 1038</td>
<td>IA32_MC3_ADDR</td>
<td>Core</td>
<td>See Section 15.3.2.3, &quot;IA32_MCI_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>40FH 1039</td>
<td>IA32_MC3_MISC</td>
<td>Core</td>
<td>See Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;</td>
</tr>
<tr>
<td>410H 1040</td>
<td>MSR_MC4_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>0</td>
<td>PCU Hardware Error (R/W)</td>
<td>When set, enables signaling of PCU hardware detected errors.</td>
<td></td>
</tr>
</tbody>
</table>
### Model-Specific Registers (MSRs)

#### Table 35-16. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PCU Controller Error (R/W)</td>
<td>Core</td>
<td>When set, enables signaling of PCU controller detected errors</td>
</tr>
<tr>
<td>2</td>
<td>PCU Firmware Error (R/W)</td>
<td>Core</td>
<td>When set, enables signaling of PCU firmware detected errors</td>
</tr>
<tr>
<td>63:2</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>411H 1041</td>
<td>IA32_MC4_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRS,” and Chapter 16.</td>
</tr>
<tr>
<td>480H 1152</td>
<td>IA32_VMX_BASIC</td>
<td>Thread</td>
<td>Reporting Register of Basic VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.1, “Basic VMX Information.”</td>
</tr>
<tr>
<td>481H 1153</td>
<td>IA32_VMX_PINBASED}_${_}$CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>482H 1154</td>
<td>IA32_VMX_PROCBASED_${_}$CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.3, “VM-Execution Controls.”</td>
</tr>
<tr>
<td>483H 1155</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of VM-exit Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See Appendix A.4, “VM-Exit Controls.”</td>
</tr>
<tr>
<td>484H 1156</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Thread</td>
<td>Capability Reporting Register of VM-entry Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.5, “VM-Entry Controls.”</td>
</tr>
<tr>
<td>485H 1157</td>
<td>IA32_VMX_MISC</td>
<td>Thread</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.6, “Miscellaneous Data.”</td>
</tr>
<tr>
<td>486H 1158</td>
<td>IA32_VMX_CRO_FIXED0</td>
<td>Thread</td>
<td>Capability Reporting Register of CRO Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CRO.”</td>
</tr>
<tr>
<td>487H 1159</td>
<td>IA32_VMX_CRO_FIXED1</td>
<td>Thread</td>
<td>Capability Reporting Register of CRO Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.7, “VMX-Fixed Bits in CRO.”</td>
</tr>
<tr>
<td>488H 1160</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Thread</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.8, “VMX-Fixed Bits in CR4.”</td>
</tr>
<tr>
<td>489H 1161</td>
<td>IA32_VMX_CR4_FIXED1</td>
<td>Thread</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 1 (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.8, “VMX-Fixed Bits in CR4.”</td>
</tr>
<tr>
<td>48AH 1162</td>
<td>IA32_VMX_VMCS_ENUM</td>
<td>Thread</td>
<td>Capability Reporting Register of VMCS Field Enumeration (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Appendix A.9, “VMCS Enumeration.”</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------</td>
<td>-----------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 48BH             | IA32_VMX_PROCBASED_CTLS2 | Thread   | Capability Reporting Register of Secondary Processor-based VM-execution Controls (R/O)  
See Appendix A.3, "VM-Execution Controls." |
| 48CH             | IA32_VMX_EPT_VPID_ENUM | Thread   | Capability Reporting Register of EPT and VPID (R/O)  
See Table 35-2 |
| 48DH             | IA32_VMX_TRUE_PINBASED_CTLS | Thread   | Capability Reporting Register of Pin-based VM-execution Flex Controls (R/O)  
See Table 35-2 |
| 48EH             | IA32_VMX_TRUE_PROCBASED_CTLS | Thread   | Capability Reporting Register of Primary Processor-based VM-execution Flex Controls (R/O)  
See Table 35-2 |
| 48FH             | IA32_VMX_TRUE_EXIT_CTLS | Thread   | Capability Reporting Register of VM-exit Flex Controls (R/O)  
See Table 35-2 |
| 490H             | IA32_VMX_TRUE_ENTRY_CTLS | Thread   | Capability Reporting Register of VM-entry Flex Controls (R/O)  
See Table 35-2 |
| 4C1H             | IA32_A_PMC0 | Thread   | See Table 35-2. |
| 4C2H             | IA32_A_PMC1 | Thread   | See Table 35-2. |
| 4C3H             | IA32_A_PMC2 | Thread   | See Table 35-2. |
| 4C4H             | IA32_A_PMC3 | Thread   | See Table 35-2. |
| 4C5H             | IA32_A_PMC4 | Core     | See Table 35-2. |
| 4C6H             | IA32_A_PMC5 | Core     | See Table 35-2. |
| 4C7H             | IA32_A_PMC6 | Core     | See Table 35-2. |
| 4C8H             | IA32_A_PMC7 | Core     | See Table 35-2. |
| 600H             | IA32_DS_AREA | Thread   | DS Save Area (R/W)  
See Table 35-2.  
| 606H             | MSR_RAPL_POWER_UNIT | Package | Unit Multipliers used in RAPL Interfaces (R/O)  
See Section 14.9.1, “RAPL Interfaces.” |
| 60AH             | MSR_PKGC3_IRTL | Package | Package C3 Interrupt Response Limit (R/W)  
Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.  
Interrupt response time limit (R/W)  
Specifies the limit that should be used to decide if the package should be put into a package C3 state. |

See Table 35-2.
### Table 35-16. MSRs Supported by Intel® Processors
based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:10</td>
<td>Time Unit (R/W)</td>
<td></td>
<td>Specifies the encoding value of time unit of the interrupt response</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>time limit. The following time unit encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: 1 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: 32 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: 1024 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011b: 32768 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100b: 1048576 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101b: 33554432 ns</td>
</tr>
<tr>
<td>14:13</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Valid (R/W)</td>
<td></td>
<td>Indicates whether the values in bits 12:0 are valid and can be used</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>by the processor for package C-state management.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60BH 1547</td>
<td>MSR_PKG_C6_IRTL</td>
<td>Package</td>
<td>Package C6 Interrupt Response Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This MSR defines the budget allocated for the package to exit from</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>C6 to a C0 state, where interrupt request can be delivered to the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>core and serviced. Additional core-exit latency may be applicable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>depending on the actual C-state the core is in.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>9:0</td>
<td>Interrupt response time limit (R/W)</td>
<td></td>
<td>Specifies the limit that should be used to decide if the package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>should be put into a package C6 state.</td>
</tr>
<tr>
<td>12:10</td>
<td>Time Unit (R/W)</td>
<td></td>
<td>Specifies the encoding value of time unit of the interrupt response</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>time limit. The following time unit encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: 1 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: 32 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: 1024 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011b: 32768 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100b: 1048576 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101b: 33554432 ns</td>
</tr>
<tr>
<td>14:13</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Valid (R/W)</td>
<td></td>
<td>Indicates whether the values in bits 12:0 are valid and can be used</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>by the processor for package C-state management.</td>
</tr>
<tr>
<td>60DH 1549</td>
<td>MSR_PKG_C2_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
</tbody>
</table>
### Table 35-16. MSRs Supported by Intel® Processors

**based on Intel® microarchitecture code name Sandy Bridge (Contd.)**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex Dec</strong></td>
<td><strong>Register Name</strong></td>
<td><strong>Scope</strong></td>
<td><strong>Bit Description</strong></td>
</tr>
<tr>
<td>63:0</td>
<td>Package C2 Residency Counter. (R/O) Value since last reset that this package is in processor-specific C2 states. Count at the same frequency as the TSC.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>638H 1592</td>
<td>MSR_PP0_POWER_LIMIT</td>
<td>Package</td>
<td>PP0 RAPL Power Limit Control (R/W) See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>639H 1593</td>
<td>MSR_PP0_ENERGY_STATUS</td>
<td>Package</td>
<td>PP0 Energy Status (R/O) See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
</tbody>
</table>
| 680H 1664        | MSR_LASTBRANCH_0_FROM_IP | Thread | Last Branch Record 0 From IP (R/W) One of sixteen pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction. See also:
- Last Branch Record Stack TOS at 1C9H
- Section 17.6.1, “LBR Stack.” |
| 681H 1665        | MSR_LASTBRANCH_1_FROM_IP | Thread | Last Branch Record 1 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 682H 1666        | MSR_LASTBRANCH_2_FROM_IP | Thread | Last Branch Record 2 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 683H 1667        | MSR_LASTBRANCH_3_FROM_IP | Thread | Last Branch Record 3 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 684H 1668        | MSR_LASTBRANCH_4_FROM_IP | Thread | Last Branch Record 4 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 685H 1669        | MSR_LASTBRANCH_5_FROM_IP | Thread | Last Branch Record 5 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 686H 1670        | MSR_LASTBRANCH_6_FROM_IP | Thread | Last Branch Record 6 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 687H 1671        | MSR_LASTBRANCH_7_FROM_IP | Thread | Last Branch Record 7 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 688H 1672        | MSR_LASTBRANCH_8_FROM_IP | Thread | Last Branch Record 8 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 689H 1673        | MSR_LASTBRANCH_9_FROM_IP | Thread | Last Branch Record 9 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 68AH 1674        | MSR_LASTBRANCH_10_FROM_IP | Thread | Last Branch Record 10 From IP (R/W) See description of MSR_LASTBRANCH_0_FROM_IP. |
### Table 35-16. MSRs Supported by Intel® Processors

Based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>68BH 1675</td>
<td>MSR_LASTBRANCH_11_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 11 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>68CH 1676</td>
<td>MSR_LASTBRANCH_12_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 12 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>68DH 1677</td>
<td>MSR_LASTBRANCH_13_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 13 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>68EH 1678</td>
<td>MSR_LASTBRANCH_14_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 14 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>68FH 1679</td>
<td>MSR_LASTBRANCH_15_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 15 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>6COH 1728</td>
<td>MSR_LASTBRANCH_0_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 0 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of sixteen pairs of last branch record registers on the last branch record stack. This part of the stack contains pointers to the destination instruction.</td>
</tr>
<tr>
<td>6C1H 1729</td>
<td>MSR_LASTBRANCH_1_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 1 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C2H 1730</td>
<td>MSR_LASTBRANCH_2_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 2 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C3H 1731</td>
<td>MSR_LASTBRANCH_3_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 3 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C4H 1732</td>
<td>MSR_LASTBRANCH_4_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 4 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C5H 1733</td>
<td>MSR_LASTBRANCH_5_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 5 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C6H 1734</td>
<td>MSR_LASTBRANCH_6_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 6 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C7H 1735</td>
<td>MSR_LASTBRANCH_7_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 7 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C8H 1736</td>
<td>MSR_LASTBRANCH_8_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 8 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6C9H 1737</td>
<td>MSR_LASTBRANCH_9_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 9 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CAH 1738</td>
<td>MSR_LASTBRANCH_10_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 10 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CBH 1739</td>
<td>MSR_LASTBRANCH_11_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 11 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CCH 1740</td>
<td>MSR_LASTBRANCH_12_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 12 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
</tbody>
</table>
### Table 35-17. MSRs Supported by Intel® Processors based on Intel® microarchitecture code name Sandy Bridge (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6CDH</td>
<td>1741</td>
<td>MSR_LASTBRANCH_13_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 13 To IP (R/W) See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CEH</td>
<td>1742</td>
<td>MSR_LASTBRANCH_14_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 14 To IP (R/W) See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6CFH</td>
<td>1743</td>
<td>MSR_LASTBRANCH_15_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 15 To IP (R/W) See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6E0H</td>
<td>1760</td>
<td>IA32_TSC_DEADLINE</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>802H</td>
<td>83FH</td>
<td>X2APIC MSRs</td>
<td>Thread</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0080H</td>
<td>IA32_EFER</td>
<td>Thread</td>
<td>Extended Feature Enables</td>
</tr>
<tr>
<td>C000</td>
<td>0081H</td>
<td>IA32_STAR</td>
<td>Thread</td>
<td>System Call Target Address (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0082H</td>
<td>IA32_LSTAR</td>
<td>Thread</td>
<td>IA-32e Mode System Call Target Address (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0084H</td>
<td>IA32_FMASK</td>
<td>Thread</td>
<td>System Call Flag Mask (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0100H</td>
<td>IA32_FS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of FS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0101H</td>
<td>IA32_GS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0102H</td>
<td>IA32_KERNEL_GSBASE</td>
<td>Thread</td>
<td>Swap Target of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000</td>
<td>0103H</td>
<td>IA32_TSC_AUX</td>
<td>Thread</td>
<td>AUXILIARY TSC Signature (R/W) See Table 35-2 and Section 17.14.2, “IA32_TSC_AUX Register and RDTSCP Support.”</td>
</tr>
</tbody>
</table>

### 35.8.1 MSRs In 2nd Generation Intel® Core™ Processor Family (Based on Intel® Microarchitecture Code Name Sandy Bridge)

Table 35-17 lists model-specific registers (MSRs) that are specific to the 2nd generation Intel® Core™ processor family (based on Intel microarchitecture code name Sandy Bridge). These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2AH, see Table 35-1.
<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RW if MSR_PLATFORM_INFO[28] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum Ratio Limit for 1C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum Ratio Limit for 2C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum Ratio Limit for 3C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum Ratio Limit for 4C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:32 Reserved.</td>
</tr>
<tr>
<td>391H 913</td>
<td>MSR_UNC_PERF_GLOBAL_CTRL</td>
<td>Package</td>
<td>Uncore PMU global control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Core 0 select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 Core 1 select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 Core 2 select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 Core 3 select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>18:4 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>29 Enable all uncore counters</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>30 Enable wake on PMI</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31 Enable Freezing counter when overflow</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:32 Reserved.</td>
</tr>
<tr>
<td>392H 914</td>
<td>MSR_UNC_PERF_GLOBAL_STATUS</td>
<td>Package</td>
<td>Uncore PMU main status</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Fixed counter overflowed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 An ARB counter overflowed</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 A CBox counter overflowed (on any slice)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:4 Reserved.</td>
</tr>
<tr>
<td>394H 916</td>
<td>MSR_UNC_PERF_FIXED_CTRL</td>
<td>Package</td>
<td>Uncore fixed counter control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>19:0 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 Enable overflow propagation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>21 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>22 Enable counting</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:23 Reserved.</td>
</tr>
</tbody>
</table>
Table 35-17. MSRs Supported by 2nd Generation Intel® Core™ Processors (Intel® microarchitecture code name Sandy Bridge) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>395H 917</td>
<td>MSR_UNC_PERF_FIXED_CTR</td>
<td>Package</td>
<td>Uncore fixed counter</td>
</tr>
<tr>
<td></td>
<td>47:0 Current count</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:48 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>396H 918</td>
<td>MSR_UNC_CBO_CONFIG</td>
<td>Package</td>
<td>Uncore C-Box configuration information (R/O)</td>
</tr>
<tr>
<td></td>
<td>3:0 Encoded number of C-Box, derive value by “-1”</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:4 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3B0H 946</td>
<td>MSR_UNC_ARB_PERFCTR0</td>
<td>Package</td>
<td>Uncore Arb unit, performance counter 0</td>
</tr>
<tr>
<td>3B1H 947</td>
<td>MSR_UNC_ARB_PERFCTR1</td>
<td>Package</td>
<td>Uncore Arb unit, performance counter 1</td>
</tr>
<tr>
<td>3B2H 944</td>
<td>MSR_UNC_ARB_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore Arb unit, counter 0 event select MSR</td>
</tr>
<tr>
<td>3B3H 945</td>
<td>MSR_UNC_ARB_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore Arb unit, counter 1 event select MSR</td>
</tr>
<tr>
<td>60CH 1548</td>
<td>MSR_PKGC7_IRTL</td>
<td>Package</td>
<td><strong>Package C7 Interrupt Response Limit (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This MSR defines the budget allocated for the package to exit from C7 to a C0 state, where interrupt request can be delivered to the core and serviced. Additional core-exit latency may be applicable depending on the actual C-state the core is in. Note: C-state values are processor specific C-state code names, unrelated to MwAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td>9:0 Interrupt response time limit (R/W)</td>
<td></td>
<td>Specifies the limit that should be used to decide if the package should be put into a package C7 state.</td>
</tr>
<tr>
<td></td>
<td>12:10 Time Unit (R/W)</td>
<td></td>
<td>Specifies the encoding value of time unit of the interrupt response time limit. The following time unit encodings are supported: 000b: 1 ns 001b: 32 ns 010b: 1024 ns 011b: 32768 ns 100b: 1048576 ns 101b: 33554432 ns</td>
</tr>
<tr>
<td></td>
<td>14:13 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15 Valid (R/W)</td>
<td></td>
<td>Indicates whether the values in bits 12:0 are valid and can be used by the processor for package C-state management.</td>
</tr>
<tr>
<td></td>
<td>63:16 Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 35-17. MSRs Supported by 2nd Generation Intel® Core™ Processors (Intel® microarchitecture code name Sandy Bridge) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td>MSR_PP0_POLICY</td>
<td>Package</td>
<td>PP0 Balance Policy (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>63AH 1594</td>
<td>MSR_PP1_POWER_LIMIT</td>
<td>Package</td>
<td>PP1 RAPL Power Limit Control (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>640H 1600</td>
<td>MSR_PP1_ENERGY_STATUS</td>
<td>Package</td>
<td>PP1 Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>641H 1601</td>
<td>MSR_PP1_POLICY</td>
<td>Package</td>
<td>PP1 Balance Policy (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>700H 1792</td>
<td>MSR_UNC_CBO_0_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 0, counter 0 event select MSR</td>
</tr>
<tr>
<td>701H 1793</td>
<td>MSR_UNC_CBO_0_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 0, counter 1 event select MSR</td>
</tr>
<tr>
<td>706H 1798</td>
<td>MSR_UNC_CBO_0_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 0, performance counter 0</td>
</tr>
<tr>
<td>707H 1799</td>
<td>MSR_UNC_CBO_0_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 0, performance counter 1</td>
</tr>
<tr>
<td>710H 1808</td>
<td>MSR_UNC_CBO_1_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 1, counter 0 event select MSR</td>
</tr>
<tr>
<td>711H 1809</td>
<td>MSR_UNC_CBO_1_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 1, counter 1 event select MSR</td>
</tr>
<tr>
<td>716H 1814</td>
<td>MSR_UNC_CBO_1_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 1, performance counter 0</td>
</tr>
<tr>
<td>717H 1815</td>
<td>MSR_UNC_CBO_1_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 1, performance counter 1</td>
</tr>
<tr>
<td>720H 1824</td>
<td>MSR_UNC_CBO_2_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 2, counter 0 event select MSR</td>
</tr>
<tr>
<td>721H 1824</td>
<td>MSR_UNC_CBO_2_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 2, counter 1 event select MSR</td>
</tr>
<tr>
<td>726H 1830</td>
<td>MSR_UNC_CBO_2_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 2, performance counter 0</td>
</tr>
<tr>
<td>727H 1831</td>
<td>MSR_UNC_CBO_2_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 2, performance counter 1</td>
</tr>
<tr>
<td>730H 1840</td>
<td>MSR_UNC_CBO_3_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 3, counter 0 event select MSR</td>
</tr>
<tr>
<td>731H 1841</td>
<td>MSR_UNC_CBO_3_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 3, counter 1 event select MSR.</td>
</tr>
<tr>
<td>736H 1846</td>
<td>MSR_UNC_CBO_3_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 3, performance counter 0.</td>
</tr>
<tr>
<td>737H 1847</td>
<td>MSR_UNC_CBO_3_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 3, performance counter 1.</td>
</tr>
</tbody>
</table>
### 35.8.2 MSRs In Intel® Xeon® Processor E5 Family (Based on Intel® Microarchitecture Code Name Sandy Bridge)

Table 35-18 lists additional model-specific registers (MSRs) that are specific to the Intel® Xeon® Processor E5 Family (based on Intel® microarchitecture code name Sandy Bridge). These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2DH, and also supports MSRs listed in Table 35-16 and Table 35-19.

**Table 35-18. Selected MSRs Supported by Intel® Xeon® Processors E5 Family (based on Sandy Bridge microarchitecture)**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17FH 383</td>
<td>MSR_ERROR_CONTROL</td>
<td>Package</td>
<td><strong>MC Bank Error Configuration (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 MemError Log Enable (R/W) When set, enables IMC status bank to log additional info in bits 36:32.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:2 Reserved.</td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit of Turbo Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0, RW if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7:0 Package Maximum Ratio Limit for 1C Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15:8 Package Maximum Ratio Limit for 2C Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>23:16 Package Maximum Ratio Limit for 3C Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>31:24 Package Maximum Ratio Limit for 4C Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>39:32 Package Maximum Ratio Limit for 5C Maximum turbo ratio limit of 5 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>47:40 Package Maximum Ratio Limit for 6C Maximum turbo ratio limit of 6 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>55:48 Package Maximum Ratio Limit for 7C Maximum turbo ratio limit of 7 core active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:56 Package Maximum Ratio Limit for 8C Maximum turbo ratio limit of 8 core active.</td>
</tr>
<tr>
<td>285H 645</td>
<td>IA32_MC5_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>286H 646</td>
<td>IA32_MC6_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>287H 647</td>
<td>IA32_MC7_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>288H 648</td>
<td>IA32_MC8_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>289H 649</td>
<td>IA32_MC9_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28AH 650</td>
<td>IA32_MC10_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28BH 651</td>
<td>IA32_MC11_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28CH 652</td>
<td>IA32_MC12_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>------------------------</td>
<td>------------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>28DH 653</td>
<td>IA32_MC13_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28EH 654</td>
<td>IA32_MC14_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28FH 655</td>
<td>IA32_MC15_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>290H 656</td>
<td>IA32_MC16_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>291H 657</td>
<td>IA32_MC17_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>292H 658</td>
<td>IA32_MC18_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>293H 659</td>
<td>IA32_MC19_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>39CH 924</td>
<td>MSR_PEBS_NUM_ALT</td>
<td>Package</td>
<td>ENABLE_PEBS_NUM_ALT (RW) Write 1 to enable alternate PEBS counting logic for specific events requiring additional configuration, see Table 19-9</td>
</tr>
<tr>
<td>414H 1044</td>
<td>MSR_MC5_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>415H 1045</td>
<td>MSR_MC5_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>416H 1046</td>
<td>MSR_MC5_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>417H 1047</td>
<td>MSR_MC5_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>418H 1048</td>
<td>MSR_MC6_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>419H 1049</td>
<td>MSR_MC6_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>41AH 1050</td>
<td>MSR_MC6_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>41BH 1051</td>
<td>MSR_MC6_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>41CH 1052</td>
<td>MSR_MC7_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>41DH 1053</td>
<td>MSR_MC7_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>41EH 1054</td>
<td>MSR_MC7_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>41FH 1055</td>
<td>MSR_MC7_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>420H 1056</td>
<td>MSR_MC8_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>421H 1057</td>
<td>MSR_MC8_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>422H 1058</td>
<td>MSR_MC8_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>423H 1059</td>
<td>MSR_MC8_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>424H 1060</td>
<td>MSR_MC9_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>425H 1061</td>
<td>MSR_MC9_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>426H 1062</td>
<td>MSR_MC9_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>427H 1063</td>
<td>MSR_MC9_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>428H 1064</td>
<td>MSR_MC10_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>429H 1065</td>
<td>MSR_MC10_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>42AH 1066</td>
<td>MSR_MC10_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.”</td>
</tr>
<tr>
<td>42BH 1067</td>
<td>MSR_MC10_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
</tbody>
</table>
### Table 35-18. Selected MSRs Supported by Intel® Xeon® Processors E5 Family (based on Sandy Bridge microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>42CH 1068</td>
<td>MSR_MC11_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>42DH 1069</td>
<td>MSR_MC11_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>42EH 1070</td>
<td>MSR_MC11_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>42FH 1071</td>
<td>MSR_MC11_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>430H 1072</td>
<td>MSR_MC12_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>431H 1073</td>
<td>MSR_MC12_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>432H 1074</td>
<td>MSR_MC12_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>433H 1075</td>
<td>MSR_MC12_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>434H 1076</td>
<td>MSR_MC13_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>435H 1077</td>
<td>MSR_MC13_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>436H 1078</td>
<td>MSR_MC13_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>437H 1079</td>
<td>MSR_MC13_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>438H 1080</td>
<td>MSR_MC14_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>439H 1081</td>
<td>MSR_MC14_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>43AH 1082</td>
<td>MSR_MC14_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>43BH 1083</td>
<td>MSR_MC14_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>43CH 1084</td>
<td>MSR_MC15_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>43DH 1085</td>
<td>MSR_MC15_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>43EH 1086</td>
<td>MSR_MC15_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>43FH 1087</td>
<td>MSR_MC15_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>440H 1088</td>
<td>MSR_MC16_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>441H 1089</td>
<td>MSR_MC16_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>442H 1090</td>
<td>MSR_MC16_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>443H 1091</td>
<td>MSR_MC16_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>448H 1096</td>
<td>MSR_MC18_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>449H 1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>44AH 1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>44BH 1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
<tr>
<td>44CH 1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>44DH 1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs,” and Chapter 16.</td>
</tr>
<tr>
<td>44EH 1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
</tr>
<tr>
<td>44FH 1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.”</td>
</tr>
</tbody>
</table>
35.8.3 Additional Uncore PMU MSRs in the Intel® Xeon® Processor E5 Family

Intel Xeon Processor E5 family is based on the Sandy Bridge microarchitecture. The MSR-based uncore PMU interfaces are listed in Table 35-19. For complete detail of the uncore PMU, refer to Intel Xeon Processor E5 Product Family Uncore Performance Monitoring Guide. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_2DH

Table 35-19. Uncore PMU MSRs in Intel® Xeon® Processor E5 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>613H</td>
<td>MSR_PKG_PERF_STATUS</td>
<td>Package</td>
<td>Package RAPL Perf Status (R/O)</td>
</tr>
<tr>
<td>618H</td>
<td>MSR_DRAM_POWER_LIMIT</td>
<td>Package</td>
<td>DRAM RAPL Power Limit Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>619H</td>
<td>MSR_DRAM_ENERGY_STATUS</td>
<td>Package</td>
<td>DRAM Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>618H</td>
<td>MSR_DRAM_PERF_STATUS</td>
<td>Package</td>
<td>DRAM Performance Throttling Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>61CH</td>
<td>MSR_DRAM_POWER_INFO</td>
<td>Package</td>
<td>DRAM RAPL Parameters (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
</tbody>
</table>
### Table 35-19. Uncore PMU MSRs in Intel® Xeon® Processor E5 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D11H</td>
<td>MSR_C0_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon event select for C-box 0 counter 1.</td>
</tr>
<tr>
<td>D12H</td>
<td>MSR_C0_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon event select for C-box 0 counter 2.</td>
</tr>
<tr>
<td>D13H</td>
<td>MSR_C0_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon event select for C-box 0 counter 3.</td>
</tr>
<tr>
<td>D14H</td>
<td>MSR_C0_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon box wide filter.</td>
</tr>
<tr>
<td>D16H</td>
<td>MSR_C0_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon counter 0.</td>
</tr>
<tr>
<td>D17H</td>
<td>MSR_C0_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon counter 1.</td>
</tr>
<tr>
<td>D18H</td>
<td>MSR_C0_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon counter 2.</td>
</tr>
<tr>
<td>D19H</td>
<td>MSR_C0_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 0 perfmon counter 3.</td>
</tr>
<tr>
<td>D24H</td>
<td>MSR_C1_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon local box wide control.</td>
</tr>
<tr>
<td>D30H</td>
<td>MSR_C1_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon event select for C-box 1 counter 0.</td>
</tr>
<tr>
<td>D31H</td>
<td>MSR_C1_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon event select for C-box 1 counter 1.</td>
</tr>
<tr>
<td>D32H</td>
<td>MSR_C1_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon event select for C-box 1 counter 2.</td>
</tr>
<tr>
<td>D33H</td>
<td>MSR_C1_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon event select for C-box 1 counter 3.</td>
</tr>
<tr>
<td>D34H</td>
<td>MSR_C1_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon box wide filter.</td>
</tr>
<tr>
<td>D36H</td>
<td>MSR_C1_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon counter 0.</td>
</tr>
<tr>
<td>D37H</td>
<td>MSR_C1_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon counter 1.</td>
</tr>
<tr>
<td>D38H</td>
<td>MSR_C1_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon counter 2.</td>
</tr>
<tr>
<td>D39H</td>
<td>MSR_C1_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 1 perfmon counter 3.</td>
</tr>
<tr>
<td>D44H</td>
<td>MSR_C2_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon local box wide control.</td>
</tr>
<tr>
<td>D50H</td>
<td>MSR_C2_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon event select for C-box 2 counter 0.</td>
</tr>
<tr>
<td>D51H</td>
<td>MSR_C2_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon event select for C-box 2 counter 1.</td>
</tr>
<tr>
<td>D52H</td>
<td>MSR_C2_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon event select for C-box 2 counter 2.</td>
</tr>
<tr>
<td>D53H</td>
<td>MSR_C2_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon event select for C-box 2 counter 3.</td>
</tr>
<tr>
<td>D54H</td>
<td>MSR_C2_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon box wide filter.</td>
</tr>
<tr>
<td>D56H</td>
<td>MSR_C2_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon counter 0.</td>
</tr>
<tr>
<td>D57H</td>
<td>MSR_C2_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon counter 1.</td>
</tr>
<tr>
<td>D58H</td>
<td>MSR_C2_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon counter 2.</td>
</tr>
<tr>
<td>D59H</td>
<td>MSR_C2_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 2 perfmon counter 3.</td>
</tr>
<tr>
<td>D64H</td>
<td>MSR_C3_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon local box wide control.</td>
</tr>
<tr>
<td>D70H</td>
<td>MSR_C3_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon event select for C-box 3 counter 0.</td>
</tr>
<tr>
<td>D71H</td>
<td>MSR_C3_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon event select for C-box 3 counter 1.</td>
</tr>
<tr>
<td>D72H</td>
<td>MSR_C3_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon event select for C-box 3 counter 2.</td>
</tr>
<tr>
<td>D73H</td>
<td>MSR_C3_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon event select for C-box 3 counter 3.</td>
</tr>
<tr>
<td>D74H</td>
<td>MSR_C3_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon box wide filter.</td>
</tr>
<tr>
<td>D76H</td>
<td>MSR_C3_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon counter 0.</td>
</tr>
<tr>
<td>D77H</td>
<td>MSR_C3_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon counter 1.</td>
</tr>
<tr>
<td>D78H</td>
<td>MSR_C3_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon counter 2.</td>
</tr>
</tbody>
</table>
### Table 35-19. Uncore PMU MSRs in Intel® Xeon® Processor E5 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D79H</td>
<td>MSR_C3_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 3 perfmon counter 3.</td>
</tr>
<tr>
<td>D84H</td>
<td>MSR_C4_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon local box wide control.</td>
</tr>
<tr>
<td>D90H</td>
<td>MSR_C4_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon event select for C-box 4 counter 0.</td>
</tr>
<tr>
<td>D91H</td>
<td>MSR_C4_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon event select for C-box 4 counter 1.</td>
</tr>
<tr>
<td>D92H</td>
<td>MSR_C4_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon event select for C-box 4 counter 2.</td>
</tr>
<tr>
<td>D93H</td>
<td>MSR_C4_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon event select for C-box 4 counter 3.</td>
</tr>
<tr>
<td>D94H</td>
<td>MSR_C4_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon box wide filter.</td>
</tr>
<tr>
<td>D96H</td>
<td>MSR_C4_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon counter 0.</td>
</tr>
<tr>
<td>D97H</td>
<td>MSR_C4_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon counter 1.</td>
</tr>
<tr>
<td>D98H</td>
<td>MSR_C4_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon counter 2.</td>
</tr>
<tr>
<td>D99H</td>
<td>MSR_C4_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 4 perfmon counter 3.</td>
</tr>
<tr>
<td>DA4H</td>
<td>MSR_C5_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon local box wide control.</td>
</tr>
<tr>
<td>DB0H</td>
<td>MSR_C5_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon event select for C-box 5 counter 0.</td>
</tr>
<tr>
<td>DB1H</td>
<td>MSR_C5_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon event select for C-box 5 counter 1.</td>
</tr>
<tr>
<td>DB2H</td>
<td>MSR_C5_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon event select for C-box 5 counter 2.</td>
</tr>
<tr>
<td>DB3H</td>
<td>MSR_C5_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon event select for C-box 5 counter 3.</td>
</tr>
<tr>
<td>DB4H</td>
<td>MSR_C5_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon box wide filter.</td>
</tr>
<tr>
<td>DB6H</td>
<td>MSR_C5_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon counter 0.</td>
</tr>
<tr>
<td>DB7H</td>
<td>MSR_C5_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon counter 1.</td>
</tr>
<tr>
<td>DB8H</td>
<td>MSR_C5_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon counter 2.</td>
</tr>
<tr>
<td>DB9H</td>
<td>MSR_C5_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 5 perfmon counter 3.</td>
</tr>
<tr>
<td>DC4H</td>
<td>MSR_C6_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon local box wide control.</td>
</tr>
<tr>
<td>DD0H</td>
<td>MSR_C6_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon event select for C-box 6 counter 0.</td>
</tr>
<tr>
<td>DD1H</td>
<td>MSR_C6_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon event select for C-box 6 counter 1.</td>
</tr>
<tr>
<td>DD2H</td>
<td>MSR_C6_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon event select for C-box 6 counter 2.</td>
</tr>
<tr>
<td>DD3H</td>
<td>MSR_C6_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon event select for C-box 6 counter 3.</td>
</tr>
<tr>
<td>DD4H</td>
<td>MSR_C6_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon box wide filter.</td>
</tr>
<tr>
<td>DD6H</td>
<td>MSR_C6_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon counter 0.</td>
</tr>
<tr>
<td>DD7H</td>
<td>MSR_C6_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon counter 1.</td>
</tr>
<tr>
<td>DD8H</td>
<td>MSR_C6_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon counter 2.</td>
</tr>
<tr>
<td>DD9H</td>
<td>MSR_C6_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 6 perfmon counter 3.</td>
</tr>
<tr>
<td>DE4H</td>
<td>MSR_C7_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon local box wide control.</td>
</tr>
<tr>
<td>DF0H</td>
<td>MSR_C7_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon event select for C-box 7 counter 0.</td>
</tr>
<tr>
<td>DF1H</td>
<td>MSR_C7_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon event select for C-box 7 counter 1.</td>
</tr>
<tr>
<td>DF2H</td>
<td>MSR_C7_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon event select for C-box 7 counter 2.</td>
</tr>
<tr>
<td>DF3H</td>
<td>MSR_C7_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon event select for C-box 7 counter 3.</td>
</tr>
<tr>
<td>DF4H</td>
<td>MSR_C7_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon box wide filter.</td>
</tr>
</tbody>
</table>
The 3rd generation Intel® Core™ processor family and Intel® Xeon® processor E3-1200v2 product family (based on Intel microarchitecture code name Ivy Bridge) supports the MSR interfaces listed in Table 35-16, Table 35-17 and Table 35-20. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3AH.

### Table 35-20. Additional MSRs Supported by 3rd Generation Intel® Core™ Processors (based on Intel® microarchitecture code name Ivy Bridge)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF6H</td>
<td>MSR_C7_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 0.</td>
</tr>
<tr>
<td>DF7H</td>
<td>MSR_C7_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 1.</td>
</tr>
<tr>
<td>DF8H</td>
<td>MSR_C7_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 2.</td>
</tr>
<tr>
<td>DF9H</td>
<td>MSR_C7_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 3.</td>
</tr>
</tbody>
</table>

**Table 35-19. Uncore PMU MSRs in Intel® Xeon® Processor E5 Family (Contd.)**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF6H</td>
<td>MSR_C7_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 0.</td>
</tr>
<tr>
<td>DF7H</td>
<td>MSR_C7_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 1.</td>
</tr>
<tr>
<td>DF8H</td>
<td>MSR_C7_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 2.</td>
</tr>
<tr>
<td>DF9H</td>
<td>MSR_C7_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 7 perfmon counter 3.</td>
</tr>
</tbody>
</table>

**35.9 MSRS IN THE 3RD GENERATION INTEL® CORE™ PROCESSOR FAMILY (BASED ON INTEL® MICROARCHITECTURE CODE NAME IVY BRIDGE)**

The 3rd generation Intel® Core™ processor family and Intel® Xeon® processor E3-1200v2 product family (based on Intel microarchitecture code name Ivy Bridge) supports the MSR interfaces listed in Table 35-16, Table 35-17 and Table 35-20. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3AH.
### Table 35-20. Additional MSRs Supported by 3rd Generation Intel® Core™ Processors (based on Intel® microarchitecture code name Ivy Bridge) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>47:40</td>
<td>Package</td>
<td>Maximum Efficiency Ratio (R/O)</td>
<td>The is the minimum ratio (maximum efficiency) that the processor can operate, in units of 100MHz.</td>
</tr>
<tr>
<td>55:48</td>
<td>Package</td>
<td>Minimum Operating Ratio (R/O)</td>
<td>Contains the minimum supported operating ratio in units of 100 MHz.</td>
</tr>
<tr>
<td>63:56</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_- CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>2:0</td>
<td>Package</td>
<td>Package C-State Limit (R/W)</td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The following C-state code name encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: C0/C1 (no package C-state support)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: C2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: C6 no retention</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011b: C6 retention</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100b: C7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101b: C7s</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>111: No package C-state limit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: This field cannot be used to limit package C-state to C3.</td>
</tr>
<tr>
<td>9:3</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td>When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWAIT instructions</td>
</tr>
<tr>
<td>14:11</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>CFG Lock (R/W)</td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
</tr>
<tr>
<td>24:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>C3 state auto demotion enable (R/W)</td>
<td>When set, the processor will conditionally demote C6/C7 requests to C3 based on uncore auto-demote information.</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>C1 state auto demotion enable (R/W)</td>
<td>When set, the processor will conditionally demote C3/C6/C7 requests to C1 based on uncore auto-demote information.</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>Enable C3 undemotion (R/W)</td>
<td>When set, enables undemotion from demoted C3.</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------</td>
<td>-------------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>28</td>
<td>Enable C1 undemotion (R/W)</td>
<td>Package</td>
<td>When set, enables undemotion from demoted C1.</td>
</tr>
<tr>
<td>63:29</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64H 1608</td>
<td>MSR_CONFIG_TDP_NOMINAL</td>
<td>Package</td>
<td>Base TDP Ratio (R/O)</td>
</tr>
<tr>
<td>7:0</td>
<td>Config_TDP_Base</td>
<td></td>
<td>Base TDP level ratio to be used for this specific processor (in units of 100 MHz).</td>
</tr>
<tr>
<td>63:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64H 1609</td>
<td>MSR_CONFIG_TDP_LEVEL1</td>
<td>Package</td>
<td>ConfigTDP Level 1 ratio and power level (R/O)</td>
</tr>
<tr>
<td>14:0</td>
<td>PKG_TDP_LVL1</td>
<td></td>
<td>Power setting for ConfigTDP Level 1.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Config_TDP_LVL1_Ratio</td>
<td></td>
<td>ConfigTDP level 1 ratio to be used for this specific processor.</td>
</tr>
<tr>
<td>31:24</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46:32</td>
<td>PKG_MAX_PWR_LVL1</td>
<td></td>
<td>Max Power setting allowed for ConfigTDP Level 1.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62:48</td>
<td>PKG_MIN_PWR_LVL1</td>
<td></td>
<td>MIN Power setting allowed for ConfigTDP Level 1.</td>
</tr>
<tr>
<td>63</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64H 1610</td>
<td>MSR_CONFIG_TDP_LEVEL2</td>
<td>Package</td>
<td>ConfigTDP Level 2 ratio and power level (R/O)</td>
</tr>
<tr>
<td>14:0</td>
<td>PKG_TDP_LVL2</td>
<td></td>
<td>Power setting for ConfigTDP Level 2.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Config_TDP_LVL2_Ratio</td>
<td></td>
<td>ConfigTDP level 2 ratio to be used for this specific processor.</td>
</tr>
<tr>
<td>31:24</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>46:32</td>
<td>PKG_MAX_PWR_LVL2</td>
<td></td>
<td>Max Power setting allowed for ConfigTDP Level 2.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62:48</td>
<td>PKG_MIN_PWR_LVL2</td>
<td></td>
<td>MIN Power setting allowed for ConfigTDP Level 2.</td>
</tr>
<tr>
<td>63</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64H 1611</td>
<td>MSR_CONFIG_TDP_CONTROL</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td>1:0</td>
<td>TDP_LEVEL (R/W/L)</td>
<td></td>
<td>System BIOS can program this field.</td>
</tr>
<tr>
<td>30:2</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

Table 35-20. Additional MSRs Supported by 3rd Generation Intel® Core™ Processors (based on Intel® microarchitecture code name Ivy Bridge) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4EH</td>
<td>MSR_PPIN_CTL</td>
<td>Package</td>
<td>Protected Processor Inventory Number Enable Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>LockOut (R/WO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Set 1 to prevent further writes to MSR_PPIN_CTL. Writing 1 to MSR_PPINCTL[bit 0] is permitted only if MSR_PPIN_CTL[bit 1] is clear. Default is 0.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BIOS should provide an opt-in menu to enable the user to turn on MSR_PPIN_CTL[bit 1] for privileged inventory initialization agent to access MSR_PPIN. After reading MSR_PPIN, the privileged inventory initialization agent should write '01b' to MSR_PPIN_CTL to disable further access to MSR_PPIN and prevent unauthorized modification to MSR_PPIN_CTL.</td>
</tr>
</tbody>
</table>

35.9.1 MSRs In Intel® Xeon® Processor E5 v2 Product Family (Based on Ivy Bridge-E Microarchitecture)

Table 35-21 lists model-specific registers (MSRs) that are specific to the Intel® Xeon® Processor E5 v2 Product Family (based on Ivy Bridge-E microarchitecture). These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3EH, see Table 35-1. These processors supports the MSR interfaces listed in Table 35-16, and Table 35-21.

Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Config_TDP_Lock (RW/L)</td>
<td>Package</td>
<td>When this bit is set, the content of this register is locked until a reset.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64CH</td>
<td>MSR_TURBO_ACTIVATION_RATIO</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td>7:0</td>
<td>MAX_NON_TURBO_RATIO (RW/L)</td>
<td></td>
<td>System BIOS can program this field.</td>
</tr>
<tr>
<td>30:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>TURBO_ACTIVATION_RATIO_Lock (RW/L)</td>
<td>Package</td>
<td>When this bit is set, the content of this register is locked until a reset.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-17 for other MSR definitions applicable to processors with CPUID signature 06_3AH.
### Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex</strong></td>
<td><strong>Dec</strong></td>
<td><strong>Register Name</strong></td>
<td><strong>Scope</strong></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Enable_PPIN (R/w)</td>
<td><strong>Enable_PPIN (R/w)</strong></td>
</tr>
<tr>
<td>63:2</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>4FH 79</td>
<td>MSR_PPIN</td>
<td>Package</td>
<td><strong>Protected Processor Inventory Number (R/O)</strong></td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td><strong>Protected Processor Inventory Number (R/O)</strong></td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>15:8</td>
<td></td>
<td><strong>Maximum Non-Turbo Ratio (R/O)</strong></td>
<td>The is the ratio of the frequency that invariant TSC runs at. Frequency = ratio * 100 MHz.</td>
</tr>
<tr>
<td>22:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
<td><strong>PPIN_CAP (R/O)</strong></td>
<td>When set to 1, indicates that Protected Processor Inventory Number (PPIN) capability can be enabled for privileged system inventory agent to read PPIN from MSR_PPIN. When set to 0, PPIN capability is not supported. An attempt to access MSR_PPIN_CTL or MSR_PPIN will cause #GP.</td>
</tr>
<tr>
<td>27:24</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
<td><strong>Programmable Ratio Limit for Turbo Mode (R/O)</strong></td>
<td>When set to 1, indicates that Programmable Ratio Limits for Turbo mode is enabled, and when set to 0, indicates Programmable Ratio Limits for Turbo mode is disabled.</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td><strong>Programmable TDP Limit for Turbo Mode (R/O)</strong></td>
<td>When set to 1, indicates that TDP Limits for Turbo mode are programmable, and when set to 0, indicates TDP Limit for Turbo mode is not programmable.</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td><strong>Programmable TJ OFFSET (R/O)</strong></td>
<td>When set to 1, indicates that MSR_TEMPERATURE_TARGET.[27:24] is valid and writable to specify an temperature offset.</td>
</tr>
<tr>
<td>39:30</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>47:40</td>
<td></td>
<td><strong>Maximum Efficiency Ratio (R/O)</strong></td>
<td>The is the minimum ratio (maximum efficiency) that the processor can operates, in units of 100MHz.</td>
</tr>
</tbody>
</table>
### Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_ CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>2:0</td>
<td>Package C-State Limit (R/W)</td>
<td></td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power), for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 000b: C0/C1 (no package C-state support) 001b: C2 010b: C6 no retention 011b: C6 retention 100b: C7 101b: C7s 111: No package C-state limit. Note: This field cannot be used to limit package C-state to C3.</td>
</tr>
<tr>
<td>9:3</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td></td>
<td>When set, will map IO_read instructions sent to IO register specified by MSR_PMG_IO_CAPTURE_BASE to MWAIT instructions</td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/W)</td>
<td></td>
<td>When set, lock bits 15:0 of this register until next reset.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>Global Machine Check Capability (R/O)</td>
</tr>
<tr>
<td>7:0</td>
<td>Count</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>MCG_CTL_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MCG_EXT_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MCP_CMCI_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>MCG_TES_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:12</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>MCG_EXT_CNT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>MCG_SER_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>MCG_ELOG_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:27</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------------</td>
<td>--------------</td>
<td>----------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>17FH 383</td>
<td>MSR_ERROR_CONTROL</td>
<td>Package</td>
<td>MC Bank Error Configuration (R/W)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>MemError Log Enable (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, enables IMC status bank to log additional info in bits 36:32.</td>
</tr>
<tr>
<td></td>
<td>63:2</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1A2H 418</td>
<td>MSR_TEMPERATURE_TARGET</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td>23:16</td>
<td>Temperature Target (RO)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The minimum temperature at which PROCHOT# will be asserted. The value is degree C.</td>
</tr>
<tr>
<td></td>
<td>27:24</td>
<td>TCC Activation Offset (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies a temperature offset in degrees C from the temperature target (bits 23:16). PROCHOT# will assert at the offset target temperature. Write is permitted only MSR_PLATFORM_INFO.[30] is set.</td>
</tr>
<tr>
<td></td>
<td>63:28</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1AEH 430</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td>Package</td>
<td>Maximum Ratio Limit for 9C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 9 core active.</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
<td>Package</td>
<td>Maximum Ratio Limit for 10C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 10 core active.</td>
</tr>
<tr>
<td></td>
<td>23:16</td>
<td>Package</td>
<td>Maximum Ratio Limit for 11C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 11 core active.</td>
</tr>
<tr>
<td></td>
<td>31:24</td>
<td>Package</td>
<td>Maximum Ratio Limit for 12C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 12 core active.</td>
</tr>
<tr>
<td></td>
<td>63:32</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>285H 645</td>
<td>IA32_MC5_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>286H 646</td>
<td>IA32_MC6_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>287H 647</td>
<td>IA32_MC7_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>288H 648</td>
<td>IA32_MC8_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>289H 649</td>
<td>IA32_MC9_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28AH 650</td>
<td>IA32_MC10_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28BH 651</td>
<td>IA32_MC11_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28CH 652</td>
<td>IA32_MC12_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28DH 653</td>
<td>IA32_MC13_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>28EH 654</td>
<td>IA32_MC14_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28FH 655</td>
<td>IA32_MC15_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>290H 656</td>
<td>IA32_MC16_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>291H 657</td>
<td>IA32_MC17_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>292H 658</td>
<td>IA32_MC18_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>293H 659</td>
<td>IA32_MC19_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>294H 660</td>
<td>IA32_MC20_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>295H 661</td>
<td>IA32_MC21_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>296H 662</td>
<td>IA32_MC22_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>297H 663</td>
<td>IA32_MC23_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>298H 664</td>
<td>IA32_MC24_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>29AH 666</td>
<td>IA32_MC26_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>29BH 667</td>
<td>IA32_MC27_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>29CH 668</td>
<td>IA32_MC28_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>414H 1044</td>
<td>MSR_MC5_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>415H 1045</td>
<td>MSR_MC5_STATUS</td>
<td>Package</td>
<td>Bank MC5 reports MC error from the Intel QPI module.</td>
</tr>
<tr>
<td>416H 1046</td>
<td>MSR_MC5_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>417H 1047</td>
<td>MSR_MC5_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>418H 1048</td>
<td>MSR_MC6_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>419H 1049</td>
<td>MSR_MC6_STATUS</td>
<td>Package</td>
<td>Bank MC6 reports MC error from the integrated I/O module.</td>
</tr>
<tr>
<td>41AH 1050</td>
<td>MSR_MC6_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41BH 1051</td>
<td>MSR_MC6_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41CH 1052</td>
<td>MSR_MC7_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>41DH 1053</td>
<td>MSR_MC7_STATUS</td>
<td>Package</td>
<td>Banks MC7 and MC 8 report MC error from the two home agents.</td>
</tr>
<tr>
<td>41EH 1054</td>
<td>MSR_MC7_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41FH 1055</td>
<td>MSR_MC7_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>420H 1056</td>
<td>MSR_MC8_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>421H 1057</td>
<td>MSR_MC8_STATUS</td>
<td>Package</td>
<td>Banks MC7 and MC 8 report MC error from the two home agents.</td>
</tr>
<tr>
<td>422H 1058</td>
<td>MSR_MC8_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>423H 1059</td>
<td>MSR_MC8_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>424H 1060</td>
<td>MSR_MC9_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>425H 1061</td>
<td>MSR_MC9_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>426H 1062</td>
<td>MSR_MC9_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>427H 1063</td>
<td>MSR_MC9_MISC</td>
<td>Package</td>
<td></td>
</tr>
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</table>
Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture) (Contd.)

<table>
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<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>428H 1064</td>
<td>MSR_MC10_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>429H 1065</td>
<td>MSR_MC10_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42AH 1066</td>
<td>MSR_MC10_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42BH 1067</td>
<td>MSR_MC10_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42CH 1068</td>
<td>MSR_MC11_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>42DH 1069</td>
<td>MSR_MC11_STATUS</td>
<td>Package</td>
<td>Bank MC11 reports MC error from a specific channel of the integrated memory controller.</td>
</tr>
<tr>
<td>42EH 1070</td>
<td>MSR_MC11_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42FH 1071</td>
<td>MSR_MC11_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>430H 1072</td>
<td>MSR_MC12_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>431H 1073</td>
<td>MSR_MC12_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>432H 1074</td>
<td>MSR_MC12_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>433H 1075</td>
<td>MSR_MC12_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>434H 1076</td>
<td>MSR_MC13_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>435H 1077</td>
<td>MSR_MC13_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>436H 1078</td>
<td>MSR_MC13_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>437H 1079</td>
<td>MSR_MC13_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>438H 1080</td>
<td>MSR_MC14_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>439H 1081</td>
<td>MSR_MC14_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43AH 1082</td>
<td>MSR_MC14_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43BH 1083</td>
<td>MSR_MC14_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43CH 1084</td>
<td>MSR_MC15_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>43DH 1085</td>
<td>MSR_MC15_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43EH 1086</td>
<td>MSR_MC15_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43FH 1087</td>
<td>MSR_MC15_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>440H 1088</td>
<td>MSR_MC16_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>441H 1089</td>
<td>MSR_MC16_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>442H 1090</td>
<td>MSR_MC16_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>443H 1091</td>
<td>MSR_MC16_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Bank MC17 reports MC error from a specific CBo (core broadcast) and its corresponding slice of L3.</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
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</tr>
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Table 35-21. MSRs Supported by Intel® Xeon® Processors E5 v2 Product Family (based on Ivy Bridge-E microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
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<td>MSR_MC18_CTL</td>
<td>Package</td>
</tr>
<tr>
<td>448H</td>
<td>1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>44AH</td>
<td>1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>44BH</td>
<td>1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>44CH</td>
<td>1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
</tr>
<tr>
<td>44DH</td>
<td>1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>44EH</td>
<td>1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>44FH</td>
<td>1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>450H</td>
<td>1104</td>
<td>MSR_MC20_CTL</td>
<td>Package</td>
</tr>
<tr>
<td>451H</td>
<td>1105</td>
<td>MSR_MC20_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>452H</td>
<td>1106</td>
<td>MSR_MC20_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>453H</td>
<td>1107</td>
<td>MSR_MC20_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>454H</td>
<td>1108</td>
<td>MSR_MC21_CTL</td>
<td>Package</td>
</tr>
<tr>
<td>455H</td>
<td>1109</td>
<td>MSR_MC21_STATUS</td>
<td>Package</td>
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<tr>
<td>456H</td>
<td>1110</td>
<td>MSR_MC21_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>457H</td>
<td>1111</td>
<td>MSR_MC21_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>458H</td>
<td>1112</td>
<td>MSR_MC22_CTL</td>
<td>Package</td>
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<tr>
<td>459H</td>
<td>1113</td>
<td>MSR_MC22_STATUS</td>
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<td>Package</td>
</tr>
<tr>
<td>45BH</td>
<td>1115</td>
<td>MSR_MC22_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>45CH</td>
<td>1116</td>
<td>MSR_MC23_CTL</td>
<td>Package</td>
</tr>
<tr>
<td>45DH</td>
<td>1117</td>
<td>MSR_MC23_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>45EH</td>
<td>1118</td>
<td>MSR_MC23_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>45FH</td>
<td>1119</td>
<td>MSR_MC23_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>460H</td>
<td>1120</td>
<td>MSR_MC24_CTL</td>
<td>Package</td>
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<tr>
<td>461H</td>
<td>1121</td>
<td>MSR_MC24_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>462H</td>
<td>1122</td>
<td>MSR_MC24_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>463H</td>
<td>1123</td>
<td>MSR_MC24_MISC</td>
<td>Package</td>
</tr>
<tr>
<td>464H</td>
<td>1124</td>
<td>MSR_MC25_CTL</td>
<td>Package</td>
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<tr>
<td>465H</td>
<td>1125</td>
<td>MSR_MC25_STATUS</td>
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<tr>
<td>466H</td>
<td>1126</td>
<td>MSR_MC25_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>467H</td>
<td>1127</td>
<td>MSR_MC25_MISC</td>
<td>Package</td>
</tr>
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</table>
35.9.2 Additional MSRs Supported by Intel® Xeon® Processor E7 v2 Family

Intel® Xeon® processor E7 v2 family (based on Ivy Bridge-E microarchitecture) with CPUID DisplayFamily_DisplayModel signature 06_3EH supports the MSR interfaces listed in Table 35-16, Table 35-21, and Table 35-22.

Table 35-22. Additional MSRs Supported by Intel® Xeon® Processor E7 v2 Family with DisplayFamily_DisplayModel Signature 06_3EH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3AH</td>
<td>58</td>
<td>Thread</td>
<td>Control Features in Intel 64 Processor (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Lock (R/wL)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>Enable VMX inside SMX operation (R/wL)</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>Enable VMX outside SMX operation (R/wL)</td>
</tr>
</tbody>
</table>
Table 35-22. Additional MSRs Supported by Intel® Xeon® Processor E7 v2 Family with DisplayFamily_DisplayModel Signature 06_3EH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14:8</td>
<td>SENTER local functions enables (R/WL)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>SENTER global functions enable (R/WL)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>179H</td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>Global Machine Check Capability (R/O)</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td></td>
<td>Count</td>
</tr>
<tr>
<td>8</td>
<td>MCG_Ctl_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MCG_EXT_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MCP_CMCI_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>MCG_TES_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:12</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>MCG_EXT_CNT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>MCG_SER_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:25</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17AH</td>
<td>IA32_MCG_STATUS</td>
<td>Thread</td>
<td>(R/W0)</td>
</tr>
<tr>
<td>0</td>
<td>RIPV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EIPV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>MCIP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>LMCE signaled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:4</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1AEH</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rw if MSR_PLATFORM_INFO[28] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 9C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 9 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 10C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 10 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 11C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 11 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 12C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 12 core active.</td>
</tr>
<tr>
<td>39:32</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 13C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 13 core active.</td>
</tr>
<tr>
<td>47:40</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 14C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 14 core active.</td>
</tr>
<tr>
<td>55:48</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 15C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 15 core active.</td>
</tr>
<tr>
<td>62:56</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
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Table 35-22. Additional MSRs Supported by Intel® Xeon® Processor E7 v2 Family with DisplayFamily_DisplayModel Signature 06_3EH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Semaphore for Turbo Ratio Limit Configuration</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>If 1, the processor uses override configuration specified in MSR_TURBO_RATIO_LIMIT and MSR_TURBO_RATIO_LIMIT1. If 0, the processor uses factory-set configuration (Default).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29DH 669</td>
<td>IA32_MC29_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>29EH 670</td>
<td>IA32_MC30_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>29FH 671</td>
<td>IA32_MC31_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEB_S_ENABLE</td>
<td>Thread</td>
<td>See Section 18.7.1.1, “Precise Event Based Sampling (PEBS).”</td>
</tr>
<tr>
<td>3F1H 1009</td>
<td>MSR_PEB_S_ENABLE</td>
<td>Thread</td>
<td>0 Enable PEBS on IA32_PMC0. (R/W)</td>
</tr>
<tr>
<td></td>
<td>1 Enable PEBS on IA32_PMC1. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 Enable PEBS on IA32_PMC2. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3 Enable PEBS on IA32_PMC3. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>31:4 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>32 Enable Load Latency on IA32_PMC0. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>33 Enable Load Latency on IA32_PMC1. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>34 Enable Load Latency on IA32_PMC2. (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>35 Enable Load Latency on IA32_PMC3. (R/W)</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>63:36 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41BH 1051</td>
<td>IA32_MC6_MISC</td>
<td>Package</td>
<td>Misc MAC information of Integrated I/O. (R/O) see Section 15.3.2.4</td>
</tr>
<tr>
<td></td>
<td>5:0 Recoverable Address LSB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8:6 Address Mode</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15:9 Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>31:16 PCI Express Requestor ID</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>39:32 PCI Express Segment Number</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>63:32 Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>474H 1140</td>
<td>MSR_MC29_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>475H 1141</td>
<td>MSR_MC29_STATUS</td>
<td>Package</td>
<td>Bank MC29 reports MC error from a specific CBo (core broadcast) and its corresponding slice of L3.</td>
</tr>
<tr>
<td>476H 1142</td>
<td>MSR_MC29_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>477H 1143</td>
<td>MSR_MC29_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>478H 1144</td>
<td>MSR_MC30_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”</td>
</tr>
<tr>
<td>479H 1145</td>
<td>MSR_MC30_STATUS</td>
<td>Package</td>
<td>Bank MC30 reports MC error from a specific CBo (core broadcast) and its corresponding slice of L3.</td>
</tr>
<tr>
<td>47AH 1146</td>
<td>MSR_MC30_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>47BH 1147</td>
<td>MSR_MC30_MISC</td>
<td>Package</td>
<td></td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

35.9.3  Additional Uncore PMU MSRs in the Intel® Xeon® Processor E5 v2 and E7 v2 Families

Intel Xeon Processor E5 v2 and E7 v2 families are based on the Ivy Bridge-E microarchitecture. The MSR-based uncore PMU interfaces are listed in Table 35-19 and Table 35-23. For complete detail of the uncore PMU, refer to Intel Xeon Processor E5 v2 Product Family Uncore Performance Monitoring Guide. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3EH.

Table 35-22. Additional MSRs Supported by Intel® Xeon® Processor E7 v2 Family with DisplayFamily_DisplayModel Signature 06_3EH

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
</tr>
</thead>
<tbody>
<tr>
<td>47CH</td>
<td>1148</td>
</tr>
<tr>
<td>47DH</td>
<td>1149</td>
</tr>
<tr>
<td>47EH</td>
<td>1150</td>
</tr>
<tr>
<td>47FH</td>
<td>1147</td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-21 for other MSR definitions applicable to Intel Xeon processor E7 v2 with CPUID signature 06_3AH.

NOTES:
1. An override configuration lower than the factory-set configuration is always supported. An override configuration higher than the factory-set configuration is dependent on features specific to the processor and the platform.

Table 35-23. Uncore PMU MSRs in Intel® Xeon® Processor E5 v2 and E7 v2 Families

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
</tr>
</thead>
<tbody>
<tr>
<td>C00H</td>
<td></td>
</tr>
<tr>
<td>C01H</td>
<td></td>
</tr>
<tr>
<td>C06H</td>
<td></td>
</tr>
<tr>
<td>C15H</td>
<td></td>
</tr>
<tr>
<td>C35H</td>
<td></td>
</tr>
<tr>
<td>D1AH</td>
<td></td>
</tr>
<tr>
<td>D3AH</td>
<td></td>
</tr>
<tr>
<td>D5AH</td>
<td></td>
</tr>
<tr>
<td>D7AH</td>
<td></td>
</tr>
<tr>
<td>D9AH</td>
<td></td>
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<tr>
<td>DBAH</td>
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<tr>
<td>DDAH</td>
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<tr>
<td>DFAH</td>
<td></td>
</tr>
<tr>
<td>E04H</td>
<td></td>
</tr>
<tr>
<td>E10H</td>
<td></td>
</tr>
<tr>
<td>E11H</td>
<td></td>
</tr>
<tr>
<td>E12H</td>
<td></td>
</tr>
<tr>
<td>E13H</td>
<td></td>
</tr>
</tbody>
</table>

See Section 15.3.2.1, "IA32_MCI_CTL MSRs." through Section 15.3.2.4, "IA32_MCI_MISC MSRs."
Bank MC31 reports MC error from a specific CBo (core broadcast) and its corresponding slice of L3.
<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E14H</td>
<td>MSR_C8_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon box wide filter.</td>
</tr>
<tr>
<td>E16H</td>
<td>MSR_C8_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter 0.</td>
</tr>
<tr>
<td>E17H</td>
<td>MSR_C8_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter 1.</td>
</tr>
<tr>
<td>E18H</td>
<td>MSR_C8_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter 2.</td>
</tr>
<tr>
<td>E19H</td>
<td>MSR_C8_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon counter 3.</td>
</tr>
<tr>
<td>E1AH</td>
<td>MSR_C8_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 8 perfmon box wide filter1.</td>
</tr>
<tr>
<td>E24H</td>
<td>MSR_C9_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon local box wide control.</td>
</tr>
<tr>
<td>E30H</td>
<td>MSR_C9_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select for C-box 9 counter 0.</td>
</tr>
<tr>
<td>E31H</td>
<td>MSR_C9_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select for C-box 9 counter 1.</td>
</tr>
<tr>
<td>E32H</td>
<td>MSR_C9_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select for C-box 9 counter 2.</td>
</tr>
<tr>
<td>E33H</td>
<td>MSR_C9_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon event select for C-box 9 counter 3.</td>
</tr>
<tr>
<td>E34H</td>
<td>MSR_C9_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon box wide filter.</td>
</tr>
<tr>
<td>E36H</td>
<td>MSR_C9_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter 0.</td>
</tr>
<tr>
<td>E37H</td>
<td>MSR_C9_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter 1.</td>
</tr>
<tr>
<td>E38H</td>
<td>MSR_C9_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter 2.</td>
</tr>
<tr>
<td>E39H</td>
<td>MSR_C9_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon counter 3.</td>
</tr>
<tr>
<td>E3AH</td>
<td>MSR_C9_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 9 perfmon box wide filter1.</td>
</tr>
<tr>
<td>E44H</td>
<td>MSR_C10_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon local box wide control.</td>
</tr>
<tr>
<td>E50H</td>
<td>MSR_C10_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon event select for C-box 10 counter 0.</td>
</tr>
<tr>
<td>E51H</td>
<td>MSR_C10_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon event select for C-box 10 counter 1.</td>
</tr>
<tr>
<td>E52H</td>
<td>MSR_C10_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon event select for C-box 10 counter 2.</td>
</tr>
<tr>
<td>E53H</td>
<td>MSR_C10_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon event select for C-box 10 counter 3.</td>
</tr>
<tr>
<td>E54H</td>
<td>MSR_C10_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon box wide filter.</td>
</tr>
<tr>
<td>E56H</td>
<td>MSR_C10_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon counter 0.</td>
</tr>
<tr>
<td>E57H</td>
<td>MSR_C10_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon counter 1.</td>
</tr>
<tr>
<td>E58H</td>
<td>MSR_C10_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon counter 2.</td>
</tr>
<tr>
<td>E59H</td>
<td>MSR_C10_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon counter 3.</td>
</tr>
<tr>
<td>E5AH</td>
<td>MSR_C10_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 10 perfmon box wide filter1.</td>
</tr>
<tr>
<td>E64H</td>
<td>MSR_C11_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon local box wide control.</td>
</tr>
<tr>
<td>E70H</td>
<td>MSR_C11_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon event select for C-box 11 counter 0.</td>
</tr>
<tr>
<td>E71H</td>
<td>MSR_C11_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon event select for C-box 11 counter 1.</td>
</tr>
<tr>
<td>E72H</td>
<td>MSR_C11_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon event select for C-box 11 counter 2.</td>
</tr>
<tr>
<td>E73H</td>
<td>MSR_C11_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon event select for C-box 11 counter 3.</td>
</tr>
<tr>
<td>E74H</td>
<td>MSR_C11_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon box wide filter.</td>
</tr>
<tr>
<td>E76H</td>
<td>MSR_C11_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon counter 0.</td>
</tr>
<tr>
<td>E77H</td>
<td>MSR_C11_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon counter 1.</td>
</tr>
<tr>
<td>E78H</td>
<td>MSR_C11_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon counter 2.</td>
</tr>
</tbody>
</table>
### Table 35-23. Uncore PMU MSRs in Intel® Xeon® Processor E5 v2 and E7 v2 Families (Contd.)

<table>
<thead>
<tr>
<th>Hex Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E79H</td>
<td>MSR_C11_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon counter 3.</td>
</tr>
<tr>
<td>E7AH</td>
<td>MSR_C11_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 11 perfmon box wide filter1.</td>
</tr>
<tr>
<td>E84H</td>
<td>MSR_C12_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon local box wide control.</td>
</tr>
<tr>
<td>E90H</td>
<td>MSR_C12_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon event select for C-box 12 counter 0.</td>
</tr>
<tr>
<td>E91H</td>
<td>MSR_C12_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon event select for C-box 12 counter 1.</td>
</tr>
<tr>
<td>E92H</td>
<td>MSR_C12_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon event select for C-box 12 counter 2.</td>
</tr>
<tr>
<td>E93H</td>
<td>MSR_C12_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon event select for C-box 12 counter 3.</td>
</tr>
<tr>
<td>E94H</td>
<td>MSR_C12_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon box wide filter.</td>
</tr>
<tr>
<td>E96H</td>
<td>MSR_C12_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon counter 0.</td>
</tr>
<tr>
<td>E97H</td>
<td>MSR_C12_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon counter 1.</td>
</tr>
<tr>
<td>E98H</td>
<td>MSR_C12_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon counter 2.</td>
</tr>
<tr>
<td>E99H</td>
<td>MSR_C12_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon counter 3.</td>
</tr>
<tr>
<td>E9AH</td>
<td>MSR_C12_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 12 perfmon box wide filter1.</td>
</tr>
<tr>
<td>EA4H</td>
<td>MSR_C13_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon local box wide control.</td>
</tr>
<tr>
<td>EB0H</td>
<td>MSR_C13_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon event select for C-box 13 counter 0.</td>
</tr>
<tr>
<td>EB1H</td>
<td>MSR_C13_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon event select for C-box 13 counter 1.</td>
</tr>
<tr>
<td>EB2H</td>
<td>MSR_C13_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon event select for C-box 13 counter 2.</td>
</tr>
<tr>
<td>EB3H</td>
<td>MSR_C13_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon event select for C-box 13 counter 3.</td>
</tr>
<tr>
<td>EB4H</td>
<td>MSR_C13_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon box wide filter.</td>
</tr>
<tr>
<td>EB6H</td>
<td>MSR_C13_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon counter 0.</td>
</tr>
<tr>
<td>EB7H</td>
<td>MSR_C13_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon counter 1.</td>
</tr>
<tr>
<td>EB8H</td>
<td>MSR_C13_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon counter 2.</td>
</tr>
<tr>
<td>EB9H</td>
<td>MSR_C13_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon counter 3.</td>
</tr>
<tr>
<td>EBAH</td>
<td>MSR_C13_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 13 perfmon box wide filter1.</td>
</tr>
<tr>
<td>EC4H</td>
<td>MSR_C14_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon local box wide control.</td>
</tr>
<tr>
<td>ED0H</td>
<td>MSR_C14_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon event select for C-box 14 counter 0.</td>
</tr>
<tr>
<td>ED1H</td>
<td>MSR_C14_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon event select for C-box 14 counter 1.</td>
</tr>
<tr>
<td>ED2H</td>
<td>MSR_C14_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon event select for C-box 14 counter 2.</td>
</tr>
<tr>
<td>ED3H</td>
<td>MSR_C14_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon event select for C-box 14 counter 3.</td>
</tr>
<tr>
<td>ED4H</td>
<td>MSR_C14_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon box wide filter.</td>
</tr>
<tr>
<td>ED6H</td>
<td>MSR_C14_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon counter 0.</td>
</tr>
<tr>
<td>ED7H</td>
<td>MSR_C14_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon counter 1.</td>
</tr>
<tr>
<td>ED8H</td>
<td>MSR_C14_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon counter 2.</td>
</tr>
<tr>
<td>ED9H</td>
<td>MSR_C14_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon counter 3.</td>
</tr>
<tr>
<td>EDAH</td>
<td>MSR_C14_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 14 perfmon box wide filter1.</td>
</tr>
</tbody>
</table>
35.10 MSRS IN THE 4TH GENERATION INTEL® CORE™ PROCESSORS (BASED ON HASWELL MICROARCHITECTURE)

The 4th generation Intel® Core™ processor family and Intel® Xeon® processor E3-1200v3 product family (based on Haswell microarchitecture), with CPUID DisplayFamily_DisplayModel signature 06_3CH/06_45H/06_46H, support the MSR interfaces listed in Table 35-16, Table 35-17, and Table 35-24. For an MSR listed in Table 35-16 that also appears in Table 35-24, Table 35-24 supercede Table 35-16.

The MSRs listed in Table 35-24 also apply to processors based on Haswell-E microarchitecture (see Section 35.11).

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex  Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3BH 59</td>
<td>IA32_TSC_ADJUST</td>
<td>THREAD</td>
<td>Per-Logical-Processor TSC ADJUST (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>CEH 206</td>
<td>MSRPLATFORM_INFO</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
<td>Package</td>
<td>Maximum Non-Turbo Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The is the ratio of the frequency that invariant TSC runs at.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Frequency = ratio * 100 MHz.</td>
</tr>
<tr>
<td></td>
<td>27:16</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>28</td>
<td>Package</td>
<td>Programmable Ratio Limit for Turbo Mode (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1, indicates that Programmable Ratio Limits for Turbo mode is enabled, and when set to 0, indicates Programmable Ratio Limits for Turbo mode is disabled.</td>
</tr>
<tr>
<td></td>
<td>29</td>
<td>Package</td>
<td>Programmable TDP Limit for Turbo Mode (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1, indicates that TDP Limits for Turbo mode are programmable, and when set to 0, indicates TDP Limit for Turbo mode is not programmable.</td>
</tr>
<tr>
<td></td>
<td>31:30</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>32</td>
<td>Package</td>
<td>Low Power Mode Support (LPM) (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to 1, indicates that LPM is supported, and when set to 0, indicates LPM is not supported.</td>
</tr>
<tr>
<td></td>
<td>34:33</td>
<td>Package</td>
<td>Number of ConfigTDP Levels (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>00: Only Base TDP level available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01: One additional TDP level available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>02: Two additional TDP level available.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11: Reserved.</td>
</tr>
<tr>
<td></td>
<td>39:35</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>47:40</td>
<td>Package</td>
<td>Maximum Efficiency Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The is the minimum ratio (maximum efficiency) that the processor can operates, in units of 100MHz.</td>
</tr>
<tr>
<td></td>
<td>55:48</td>
<td>Package</td>
<td>Minimum Operating Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains the minimum supported operating ratio in units of 100 MHz.</td>
</tr>
<tr>
<td></td>
<td>63:56</td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
**Table 35-24. Additional MSRs Supported by Processors based on the Haswell or Haswell-E microarchitectures**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0</td>
<td>THREAD</td>
<td>Performance Event Select for Counter 0 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Supports all fields described in Table 35-2 and the fields below.</td>
</tr>
<tr>
<td>32</td>
<td>IN_TX: see Section 18.11.5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IN_TX (bit 32) is set, AnyThread (bit 21) should be cleared to prevent incorrect results</td>
<td></td>
<td></td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1</td>
<td>THREAD</td>
<td>Performance Event Select for Counter 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Supports all fields described in Table 35-2 and the fields below.</td>
</tr>
<tr>
<td>32</td>
<td>IN_TX: see Section 18.11.5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IN_TX (bit 32) is set, AnyThread (bit 21) should be cleared to prevent incorrect results</td>
<td></td>
<td></td>
</tr>
<tr>
<td>188H 392</td>
<td>IA32_PERFEVTSEL2</td>
<td>THREAD</td>
<td>Performance Event Select for Counter 2 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Supports all fields described in Table 35-2 and the fields below.</td>
</tr>
<tr>
<td>32</td>
<td>IN_TX: see Section 18.11.5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IN_TX (bit 32) is set, AnyThread (bit 21) should be cleared to prevent incorrect results</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>IN_TXCP: see Section 18.11.5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IN_TXCP=1 &amp; IN_TX=1 and in sampling, spurious PMI may occur and transactions may continuously abort near overflow conditions. Software should favor using IN_TXCP for counting over sampling. If sampling, software should use large “sample-after” value after clearing the counter configured to use IN_TXCP and also always reset the counter even when no overflow condition was reported.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>189H 393</td>
<td>IA32_PERFEVTSEL3</td>
<td>THREAD</td>
<td>Performance Event Select for Counter 3 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Supports all fields described in Table 35-2 and the fields below.</td>
</tr>
<tr>
<td>32</td>
<td>IN_TX: see Section 18.11.5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When IN_TX (bit 32) is set, AnyThread (bit 21) should be cleared to prevent incorrect results</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1C8H 456</td>
<td>MSR_LBR_SELECT</td>
<td>Thread</td>
<td>Last Branch Record Filtering Select Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CPL_EQ_0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-24. Additional MSRs Supported by Processors based on the Haswell or Haswell-E microarchitectures

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1D9H</td>
<td>IA32_DEBUGCTL</td>
<td>Thread</td>
<td>Debug Control (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>LBR: Last Branch Record</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>BTF</td>
</tr>
<tr>
<td></td>
<td>5:2</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td></td>
<td>TR: Branch Trace</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td></td>
<td>BTS: Log Branch Trace Message to BTS buffer</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td></td>
<td>BTINT</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td></td>
<td>BTS_OFF_OS</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td></td>
<td>BTS_OFF_USER</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td></td>
<td>FREEZE_LBR_ON_PMI</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td></td>
<td>FREEZE_PERFMON_ON_PMI</td>
</tr>
<tr>
<td></td>
<td>13</td>
<td></td>
<td>ENABLE_UNCORE_PMI</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td></td>
<td>FREEZE_WHILE_SMM</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td>RTM_DEBUG</td>
</tr>
<tr>
<td></td>
<td>63:15</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>491H</td>
<td>IA32_VMX_VMFUNC</td>
<td>THREAD</td>
<td>Capability Reporting Register of VM-function Controls (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>60BH</td>
<td>MSR_PKGC_IRTL1</td>
<td>Package</td>
<td>Package C6/C7 Interrupt Response Limit 1 (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This MSR defines the interrupt response time limit used by the processor to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>manage transition to package C6 or C7 state. The latency programmed in this</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>register is for the shorter-latency sub C-states used by an MWAIT hint to C6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>or C7 state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td></td>
<td>9:0</td>
<td></td>
<td>Interrupt response time limit (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the limit that should be used to decide if the package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>should be put into a package C6 or C7 state.</td>
</tr>
<tr>
<td></td>
<td>12:10</td>
<td></td>
<td>Time Unit (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the encoding value of time unit of the interrupt response time limit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The following time unit encodings are supported:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>000b: 1 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>001b: 32 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>010b: 1024 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>011b: 32768 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>100b: 1048576 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>101b: 33554432 ns</td>
</tr>
<tr>
<td></td>
<td>14:13</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td>Valid (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Indicates whether the values in bits 12:0 are valid and can be used by the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>processor for package C-state management.</td>
</tr>
</tbody>
</table>
### Table 35-24. Additional MSRs Supported by Processors based on the Haswell or Haswell-E microarchitectures

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>60CH 1548</td>
<td>MSR_PKG_IRTL2</td>
<td>Package</td>
<td>Package C6/C7 Interrupt Response Limit 2 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This MSR defines the interrupt response time limit used by the processor to manage transition to package C6 or C7 state. The latency programmed in this register is for the longer-latency sub C-states used by an MWAIT hint to C6 or C7 state. Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>9:0</td>
<td></td>
<td>Interrupt response time limit (R/W)</td>
<td>Specifies the limit that should be used to decide if the package should be put into a package C6 or C7 state.</td>
</tr>
<tr>
<td>12:10</td>
<td></td>
<td>Time Unit (R/W)</td>
<td>Specifies the encoding value of time unit of the interrupt response time limit. The following time unit encodings are supported: 000b: 1 ns 001b: 32 ns 010b: 1024 ns 011b: 32768 ns 100b: 1048576 ns 101b: 33554432 ns</td>
</tr>
<tr>
<td>14:13</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>Valid (R/W)</td>
<td>Indicates whether the values in bits 12:0 are valid and can be used by the processor for package C-state management.</td>
</tr>
<tr>
<td>63:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>613H 1555</td>
<td>MSR_PKG_PERF_STATUS</td>
<td>Package</td>
<td>PKG Perf Status (R/O) See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>648H 1608</td>
<td>MSR_CONFIG_TDP NOMINAL</td>
<td>Package</td>
<td>Base TDP Ratio (R/O)</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>Config_TDP_Base</td>
<td>Base TDP level ratio to be used for this specific processor (in units of 100 MHz).</td>
</tr>
<tr>
<td>63:8</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>649H 1609</td>
<td>MSR_CONFIG_TDP_LEVEL1</td>
<td>Package</td>
<td>ConfigTDP Level 1 ratio and power level (R/O)</td>
</tr>
<tr>
<td>14:0</td>
<td></td>
<td>PKG_TDP_LVL1</td>
<td>Power setting for ConfigTDP Level 1.</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td></td>
<td>Config_TDP_LVL1_Ratio</td>
<td>ConfigTDP level 1 ratio to be used for this specific processor.</td>
</tr>
</tbody>
</table>
### Table 35-24. Additional MSRs Supported by Processors based on the Haswell or Haswell-E microarchitectures

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>46:32</td>
<td>PKG_MAX_PWR_LVL1</td>
<td>Max Power setting allowed for ConfigTDP Level 1.</td>
<td></td>
</tr>
<tr>
<td>62:47</td>
<td>PKG_MIN_PWR_LVL1</td>
<td>MIN Power setting allowed for ConfigTDP Level 1.</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>64AH 1610</td>
<td>MSR_CONFIG_TDP_LEVEL2</td>
<td>Package</td>
<td>ConfigTDP Level 2 ratio and power level (R/O)</td>
</tr>
<tr>
<td>14:0</td>
<td>PKG_TDP_LVL2</td>
<td>Power setting for ConfigTDP Level 2.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Config_TDP_LVL2_Ratio</td>
<td>ConfigTDP level 2 ratio to be used for this specific processor.</td>
<td></td>
</tr>
<tr>
<td>31:24</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>46:32</td>
<td>PKG_MAX_PWR_LVL2</td>
<td>Max Power setting allowed for ConfigTDP Level 2.</td>
<td></td>
</tr>
<tr>
<td>62:47</td>
<td>PKG_MIN_PWR_LVL2</td>
<td>MIN Power setting allowed for ConfigTDP Level 2.</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>64BH 1611</td>
<td>MSR_CONFIG_TDP_CONTROL</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td>1:0</td>
<td>TDP_LEVEL (RW/L)</td>
<td>System BIOS can program this field.</td>
<td></td>
</tr>
<tr>
<td>30:2</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Config_TDP_Lock (RW/L)</td>
<td>When this bit is set, the content of this register is locked until a reset.</td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>64CH 1612</td>
<td>MSR_TURBO_ACTIVATION_RATIO</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td>7:0</td>
<td>MAX_NON_TURBO_RATIO (RW/L)</td>
<td>System BIOS can program this field.</td>
<td></td>
</tr>
<tr>
<td>30:8</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>TURBO_ACTIVATION_RATIO_Lock (RW/L)</td>
<td>When this bit is set, the content of this register is locked until a reset.</td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>C80H 3200</td>
<td>IA32_DEBUG_FEATURE</td>
<td>Package</td>
<td>Silicon Debug Feature Control (R/W) See Table 35-2.</td>
</tr>
</tbody>
</table>

See Table 35-2.
35.10.1  MSRs in 4th Generation Intel® Core™ Processor Family (based on Haswell Microarchitecture)

Table 35-25 lists model-specific registers (MSRs) that are specific to 4th generation Intel® Core™ processor family and Intel® Xeon® processor E3-1200 v3 product family (based on Haswell microarchitecture). These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3CH/06_45H/06_46H, see Table 35-1.

Table 35-25.  MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONTROL</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-states. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3:0 Package C-State Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 0000b: C0/C1 (no package C-state support) 0001b: C2 0010b: C3 0011b: C6 0100b: C7 0101b: C7s Package C states C7 are not available to processor with signature 06_3CH</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9:4 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 I/O MWAIT Redirection Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14:11 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15 CFG Lock (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>24:16 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25 C3 State Auto Demotion Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>26 C1 State Auto Demotion Enable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>27 Enable C3 Undemotion (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>28 Enable C1 Undemotion (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:29 Reserved</td>
</tr>
<tr>
<td>17DH 390</td>
<td>MSR_SMM_MCA_CAP</td>
<td>THREAD</td>
<td>Enhanced SMM Capabilities (SMM-RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reports SMM capability Enhancement. Accessible only while in SMM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>57:0 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>58 SMM_Code_Access_Chk (SMM-RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If set to 1 indicates that the SMM code access restriction is supported and the MSR_SMM_FEATURE_CONTROL is supported.</td>
</tr>
</tbody>
</table>
### Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>59</td>
<td>Long_Flow_Indication (SMM-RO)</td>
<td></td>
<td>If set to 1 indicates that the SMM long flow indicator is supported and the MSR_SMM_DELAYED is supported.</td>
</tr>
<tr>
<td>63:60</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RW if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Maximum Ratio Limit for 1C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Maximum Ratio Limit for 2C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Maximum Ratio Limit for 3C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Maximum Ratio Limit for 4C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>391H 913</td>
<td>MSR_UNC_PERF_GLOBAL_CTRL</td>
<td>Package</td>
<td>Uncore PMU global control</td>
</tr>
<tr>
<td>0</td>
<td>Core 0 select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Core 1 select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Core 2 select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Core 3 select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>Enable all uncore counters</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Enable wake on PMI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Enable Freezing counter when overflow</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>392H 914</td>
<td>MSR_UNC_PERF_GLOBAL_STATUS</td>
<td>Package</td>
<td>Uncore PMU main status</td>
</tr>
<tr>
<td>0</td>
<td>Fixed counter overflowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>An ARB counter overflowed</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>A CBox counter overflowed (on any slice)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>394H 916</td>
<td>MSR_UNC_PERF_FIXED_CTRL</td>
<td>Package</td>
<td>Uncore fixed counter control (R/W)</td>
</tr>
<tr>
<td>19:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Enable overflow propagation</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
<td>Enable counting</td>
</tr>
<tr>
<td>63:23</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>395H 917</td>
<td>MSR_UNC_PERF_FIXED_CTR</td>
<td>Package</td>
<td>Uncore fixed counter</td>
</tr>
<tr>
<td>47:0</td>
<td></td>
<td></td>
<td>Current count</td>
</tr>
<tr>
<td>63:48</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>396H 918</td>
<td>MSR_UNC_CBO_CONFIG</td>
<td>Package</td>
<td>Uncore C-Box configuration information (R/O)</td>
</tr>
<tr>
<td>3:0</td>
<td></td>
<td></td>
<td>Encoded number of C-Box, derive value by “-1”</td>
</tr>
<tr>
<td>63:4</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>3B0H 946</td>
<td>MSR_UNC_ARB_PERFCTR0</td>
<td>Package</td>
<td>Uncore Arb unit, performance counter 0</td>
</tr>
<tr>
<td>3B1H 947</td>
<td>MSR_UNC_ARB_PERFCTR1</td>
<td>Package</td>
<td>Uncore Arb unit, performance counter 1</td>
</tr>
<tr>
<td>3B2H 944</td>
<td>MSR_UNC_ARB_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore Arb unit, counter 0 event select MSR</td>
</tr>
<tr>
<td>3B3H 945</td>
<td>MSR_UNC_ARB_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore Arb unit, counter 1 event select MSR</td>
</tr>
<tr>
<td>391H 913</td>
<td>MSR_UNC_PERF_GLOBAL_CTRL</td>
<td>Package</td>
<td>Uncore PMU global control</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Core 0 select</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Core 1 select</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Core 2 select</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>Core 3 select</td>
</tr>
<tr>
<td>18:4</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
<td>Enable all uncore counters</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td>Enable wake on PMI</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
<td>Enable Freezing counter when overflow</td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>395H 917</td>
<td>MSR_UNC_PERF_FIXED_CTR</td>
<td>Package</td>
<td>Uncore fixed counter</td>
</tr>
<tr>
<td>47:0</td>
<td></td>
<td></td>
<td>Current count</td>
</tr>
<tr>
<td>63:48</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>3B3H 945</td>
<td>MSR_UNC_ARB_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore Arb unit, counter 1 event select MSR</td>
</tr>
<tr>
<td>4E0H 1248</td>
<td>MSR_SMM_FEATURE_CONTROL</td>
<td>Package</td>
<td>Enhanced SMM Feature Control (SMM-Rw)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reports SMM capability Enhancement. Accessible only while in SMM.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Lock (SMM-Rwo)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set to ‘1’ locks this register from further changes</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
</tbody>
</table>
### Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td>Scope Bit</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>SMM_Code_Chk_En (SMM-RW)</td>
<td>Package</td>
<td>This control bit is available only if MSR_SMM_MCA_CAP[58] == 1. When set to ‘0’ (default) none of the logical processors are prevented from executing SMM code outside the ranges defined by the SMRR. When set to ‘1’ any logical processor in the package that attempts to execute SMM code not within the ranges defined by the SMRR will assert an unrecoverable MCE.</td>
</tr>
<tr>
<td>63:3</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>4E2H 1250</td>
<td>MSR_SMM_DELAYED</td>
<td>Package</td>
<td>SMM Delayed (SMM-RO) Reports the interruptible state of all logical processors in the package. Available only while in SMM and MSR_SMM_MCA_CAP[LONG_FLOW_INDICATION] == 1.</td>
</tr>
<tr>
<td>N-1:0</td>
<td>LOG_PROC_STATE (SMM-RO)</td>
<td>Package</td>
<td>Each bit represents a logical processor of its state in a long flow of internal operation which delays servicing an interrupt. The corresponding bit will be set at the start of long events such as: Microcode Update Load, C6, WBINVD, Ratio Change, Throttle. The bit is automatically cleared at the end of each long event. The reset value of this field is 0. Only bit positions below N = CPUID.(EAX=0BH, ECX=PKG_LVL):EBX[15:0] can be updated.</td>
</tr>
<tr>
<td>63:N</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>4E3H 1251</td>
<td>MSR_SMM_BLOCKED</td>
<td>Package</td>
<td>SMM Blocked (SMM-RO) Reports the blocked state of all logical processors in the package. Available only while in SMM.</td>
</tr>
<tr>
<td>N-1:0</td>
<td>LOG_PROC_STATE (SMM-RO)</td>
<td>Package</td>
<td>Each bit represents a logical processor of its blocked state to service an SMI. The corresponding bit will be set if the logical processor is in one of the following states: Wait For SIPI or SENTER Sleep. The reset value of this field is OFFFFH. Only bit positions below N = CPUID.(EAX=0BH, ECX=PKG_LVL):EBX[15:0] can be updated.</td>
</tr>
<tr>
<td>63:N</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>606H 1542</td>
<td>MSR_RAPL_POWER_UNIT</td>
<td>Package</td>
<td>Unit Multipliers used in RAPL Interfaces (R/O) Power Units See Section 14.9.1, “RAPL Interfaces.” Energy Status Units Energy related information (in Joules) is based on the multiplier, $1/2^\text{ESU}$; where ESU is an unsigned integer represented by bits 12:8. Default value is 0EH (or 61 micro-joules)</td>
</tr>
<tr>
<td>3:0</td>
<td>Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:4</td>
<td>Package</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>12:8</td>
<td>Package</td>
<td>Energy Status Units</td>
<td></td>
</tr>
<tr>
<td>15:13</td>
<td>Package</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19:16</td>
<td>Time Units</td>
<td>Package</td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
</tr>
<tr>
<td>63:20</td>
<td>PP1 RAPL Power Limit Control (R/W)</td>
<td>Package</td>
<td>See Section 14.9.4, “PP0/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>640H 1600</td>
<td>MSR_PP1_POWER_LIMIT</td>
<td>Package</td>
<td>PP1 Energy Status (R/O)</td>
</tr>
<tr>
<td>641H 1601</td>
<td>MSR_PP1_ENERGY_STATUS</td>
<td>Package</td>
<td>PP1 Balance Policy (R/W)</td>
</tr>
<tr>
<td>642H 1602</td>
<td>MSR_PP1_POLICY</td>
<td>Package</td>
<td>Indicator of Frequency Clipping in Processor Cores (R/W) (frequency refers to processor core frequency)</td>
</tr>
<tr>
<td>690H 1680</td>
<td>MSR_CORE_PERF_LIMIT_REASONS</td>
<td>Package</td>
<td>PROCCHOT Status (R0) When set, processor core frequency is reduced below the operating system request due to assertion of external PROCCHOT.</td>
</tr>
<tr>
<td>0</td>
<td>PROCHOT Status (R0)</td>
<td></td>
<td>When set, processor core frequency is reduced below the operating system request due to assertion of external PROCCHOT.</td>
</tr>
<tr>
<td>1</td>
<td>Thermal Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a thermal event.</td>
</tr>
<tr>
<td>3:2</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Graphics Driver Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to Processor Graphics driver override.</td>
</tr>
<tr>
<td>5</td>
<td>Autonomous Utilization-Based Frequency Control Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request because the processor has detected that utilization is low.</td>
</tr>
<tr>
<td>6</td>
<td>VR Therm Alert Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a thermal alert from the Voltage Regulator.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Electrical Design Point Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to electrical design point constraints (e.g. maximum electrical current consumption).</td>
</tr>
<tr>
<td>9</td>
<td>Core Power Limiting Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to domain-level power limiting.</td>
</tr>
<tr>
<td>10</td>
<td>Package-Level Power Limiting PL1 Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to package-level power limiting PL1.</td>
</tr>
<tr>
<td>11</td>
<td>Package-Level PL2 Power Limiting Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to package-level power limiting PL2.</td>
</tr>
</tbody>
</table>
Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>Max Turbo Limit Status (RO)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to multi-core turbo limits.</td>
</tr>
<tr>
<td>13</td>
<td>Turbo Transition Attenuation Status (RO)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to Turbo transition attenuation. This prevents performance degradation due to frequent operating ratio changes.</td>
</tr>
<tr>
<td>15:14</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PROCHOT Log</td>
<td></td>
<td>When set, indicates that the PROCHOT Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>17</td>
<td>Thermal Log</td>
<td></td>
<td>When set, indicates that the Thermal Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>19:18</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Graphics Driver Log</td>
<td></td>
<td>When set, indicates that the Graphics Driver Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>21</td>
<td>Autonomous Utilization-Based Frequency Control Log</td>
<td></td>
<td>When set, indicates that the Autonomous Utilization-Based Frequency Control Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>22</td>
<td>VR Therm Alert Log</td>
<td></td>
<td>When set, indicates that the VR Therm Alert Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Electrical Design Point Log</td>
<td></td>
<td>When set, indicates that the EDP Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>25</td>
<td>Core Power Limiting Log</td>
<td></td>
<td>When set, indicates that the Core Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
</tbody>
</table>
### Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>Package-Level PL1 Power Limiting Log</td>
<td>Package</td>
<td>When set, indicates that the Package Level PL1 Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>27</td>
<td>Package-Level PL2 Power Limiting Log</td>
<td>Package</td>
<td>When set, indicates that the Package Level PL2 Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>28</td>
<td>Max Turbo Limit Log</td>
<td>Package</td>
<td>When set, indicates that the Max Turbo Limit Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>29</td>
<td>Turbo Transition Attenuation Log</td>
<td>Package</td>
<td>When set, indicates that the Turbo Transition Attenuation Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>63:30</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6B0H 1712</td>
<td>MSR_GRAPHICS_PERF_LIMIT_REASONS</td>
<td>Package</td>
<td>Indicator of Frequency Clipping in the Processor Graphics (R/W) (frequency refers to processor graphics frequency)</td>
</tr>
<tr>
<td>0</td>
<td>PROCHOT Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request due to assertion of external PROCHOT.</td>
</tr>
<tr>
<td>1</td>
<td>Thermal Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request due to a thermal event.</td>
</tr>
<tr>
<td>3:2</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Graphics Driver Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request due to Processor Graphics driver override.</td>
</tr>
<tr>
<td>5</td>
<td>Autonomous Utilization-Based Frequency Control Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request because the processor has detected that utilization is low</td>
</tr>
<tr>
<td>6</td>
<td>VR Therm Alert Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request due to a thermal alert from the Voltage Regulator.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Electrical Design Point Status (R0)</td>
<td>Package</td>
<td>When set, frequency is reduced below the operating system request due to electrical design point constraints (e.g. maximum electrical current consumption).</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------------------------------------------</td>
<td>----------------------------------------------------------------------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>9</td>
<td>Graphics Power Limiting Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to domain-level power limiting.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Package-Level Power Limiting PL1 Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to package-level power limiting PL1.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Package-Level PL2 Power Limiting Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to package-level power limiting PL2.</td>
<td></td>
</tr>
<tr>
<td>15:12</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PROCHOT Log</td>
<td>When set, indicates that the PROCHOT Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Thermal Log</td>
<td>When set, indicates that the Thermal Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>19:18</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Graphics Driver Log</td>
<td>When set, indicates that the Graphics Driver Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Autonomous Utilization-Based Frequency Control Log</td>
<td>When set, indicates that the Autonomous Utilization-Based Frequency Control Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>VR Therm Alert Log</td>
<td>When set, indicates that the VR Therm Alert Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Electrical Design Point Log</td>
<td>When set, indicates that the EDP Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>Core Power Limiting Log</td>
<td>When set, indicates that the Core Power Limiting Status bit has asserted since the log bit was last cleared.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------</td>
<td>----------------</td>
<td>---------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td></td>
<td><strong>Package-Level PL1 Power Limiting Log</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the Package Level PL1 Power Limiting Status bit has</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td></td>
<td><strong>Package-Level PL2 Power Limiting Log</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the Package Level PL2 Power Limiting Status bit has</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
<td><strong>Max Turbo Limit Log</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the Max Turbo Limit Status bit has asserts since the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
<td><strong>Turbo Transition Attenuation Log</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, indicates that the Turbo Transition Attenuation Status bit has</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>63:30</td>
<td></td>
<td></td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>6B1H 1713</td>
<td>MSR_RING_PERF_LIMIT_REASONS</td>
<td>Package</td>
<td><strong>Indicator of Frequency Clipping in the Ring Interconnect (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(frequency refers to ring interconnect in the uncore)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td><strong>PROCHOT Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>assertion of external PROCHOT.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td><strong>Thermal Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>thermal event.</td>
</tr>
<tr>
<td>5:2</td>
<td></td>
<td></td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td><strong>VR Therm Alert Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>thermal alert from the Voltage Regulator.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td><strong>Electrical Design Point Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>electrical design point constraints (e.g. maximum electrical current consumption).</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td><strong>Reserved.</strong></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td><strong>Package-Level Power Limiting PL1 Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>package-level power limiting PL1.</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td><strong>Package-Level PL2 Power Limiting Status (R0)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>package-level power limiting PL2.</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------------------------------------------</td>
<td>------------------------------------------------</td>
<td>-----------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>16</td>
<td>PROCHOT Log</td>
<td>When set, indicates that the PROCHOT Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Thermal Log</td>
<td>When set, indicates that the Thermal Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>19:18</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Graphics Driver Log</td>
<td>When set, indicates that the Graphics Driver Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Autonomous Utilization-Based Frequency Control Log</td>
<td>When set, indicates that the Autonomous Utilization-Based Frequency Control Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>VR Therm Alert Log</td>
<td>When set, indicates that the VR Therm Alert Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Electrical Design Point Log</td>
<td>When set, indicates that the EDP Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>Core Power Limiting Log</td>
<td>When set, indicates that the Core Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Package-Level PL1 Power Limiting Log</td>
<td>When set, indicates that the Package Level PL1 Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Package-Level PL2 Power Limiting Log</td>
<td>When set, indicates that the Package Level PL2 Power Limiting Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Max Turbo Limit Log</td>
<td>When set, indicates that the Max Turbo Limit Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
</tbody>
</table>
## 35.10.2 Additional Residency MSRs Supported in 4th Generation Intel® Core™ Processors

The 4th generation Intel® Core™ processor family (based on Haswell microarchitecture) with CPUID DisplayFamily_DisplayModel signature 06_45H supports the MSR interfaces listed in Table 35-16, Table 35-17, Table 35-20, Table 35-24, Table 35-25, and Table 35-26.

### Table 35-25. MSRs Supported by 4th Generation Intel® Core™ Processors (Haswell microarchitecture) (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>29</td>
<td>Turbo Transition Attenuation Log</td>
<td>When set, indicates that the Turbo Transition Attenuation Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>63:30</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>700H 1792</td>
<td>MSR_UNC_CBO_0_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 0, counter 0 event select MSR</td>
</tr>
<tr>
<td>701H 1793</td>
<td>MSR_UNC_CBO_0_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 0, counter 1 event select MSR</td>
</tr>
<tr>
<td>706H 1798</td>
<td>MSR_UNC_CBO_0_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 0, performance counter 0</td>
</tr>
<tr>
<td>707H 1799</td>
<td>MSR_UNC_CBO_0_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 0, performance counter 1</td>
</tr>
<tr>
<td>710H 1808</td>
<td>MSR_UNC_CBO_1_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 1, counter 0 event select MSR</td>
</tr>
<tr>
<td>711H 1809</td>
<td>MSR_UNC_CBO_1_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 1, counter 1 event select MSR</td>
</tr>
<tr>
<td>716H 1814</td>
<td>MSR_UNC_CBO_1_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 1, performance counter 0</td>
</tr>
<tr>
<td>717H 1815</td>
<td>MSR_UNC_CBO_1_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 1, performance counter 1</td>
</tr>
<tr>
<td>720H 1824</td>
<td>MSR_UNC_CBO_2_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 2, counter 0 event select MSR</td>
</tr>
<tr>
<td>721H 1824</td>
<td>MSR_UNC_CBO_2_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 2, counter 1 event select MSR</td>
</tr>
<tr>
<td>726H 1830</td>
<td>MSR_UNC_CBO_2_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 2, performance counter 0</td>
</tr>
<tr>
<td>727H 1831</td>
<td>MSR_UNC_CBO_2_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 2, performance counter 1</td>
</tr>
<tr>
<td>730H 1840</td>
<td>MSR_UNC_CBO_3_PERFEVTSEL0</td>
<td>Package</td>
<td>Uncore C-Box 3, counter 0 event select MSR</td>
</tr>
<tr>
<td>731H 1841</td>
<td>MSR_UNC_CBO_3_PERFEVTSEL1</td>
<td>Package</td>
<td>Uncore C-Box 3, counter 1 event select MSR.</td>
</tr>
<tr>
<td>736H 1846</td>
<td>MSR_UNC_CBO_3_PERFCTR0</td>
<td>Package</td>
<td>Uncore C-Box 3, performance counter 0.</td>
</tr>
<tr>
<td>737H 1847</td>
<td>MSR_UNC_CBO_3_PERFCTR1</td>
<td>Package</td>
<td>Uncore C-Box 3, performance counter 1.</td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-17, Table 35-20, Table 35-24 for other MSR definitions applicable to processors with CPUID signatures 063CH, 06_46H.
## Table 35-26. Additional Residency MSRs Supported by 4th Generation Intel® Core™ Processors with DisplayFamily_DisplayModel Signature 06_45H

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-states. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>3:0</td>
<td></td>
<td></td>
<td>Package C-State Limit (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 0000b: C0/C1 (no package C-state support) 0001b: C2 0010b: C3 0011b: C6 0100b: C7 0101b: C7s 0110b: C8 0111b: C9 1000b: C10</td>
</tr>
<tr>
<td>9:4</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>10</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/WO)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24:16</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>25</td>
<td>C3 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C1 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Enable C3 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Enable C1 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:29</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>630H 1584</td>
<td>MSR_PKG_C8_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. Package C8 Residency Counter (R/O) Value since last reset that this package is in processor-specific C8 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>59:0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:60</td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>631H 1585</td>
<td>MSR_PKG_C9_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States. Package C9 Residency Counter (R/O) Value since last reset that this package is in processor-specific C9 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>59:0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
35.11 MSRS IN INTEL® XEON® PROCESSOR E5 V3 AND E7 V3 PRODUCT FAMILY

Intel® Xeon® processor E5 v3 family and Intel® Xeon® processor E7 v3 family are based on Haswell-E microarchitecture (CPUID DisplayFamily_DisplayModel = 06_3F). These processors supports the MSR interfaces listed in Table 35-16, Table 35-17, Table 35-24, and Table 35-25.

Table 35-26. Additional Residency MSRs Supported by 4th Generation Intel® Core™ Processors with DisplayFamily_DisplayModel Signature 06_45H

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:60</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>632H 1586</td>
<td>MSR_PKG_C10_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>59:0</td>
<td>Package C10 Residency Counter (R/O)</td>
<td></td>
<td>Value since last reset that this package is in processor-specific C10 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>63:60</td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-17, Table 35-24, Table 35-25 for other MSR definitions applicable to processors with CPUID signature 06_45H.

Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-states. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>2:0</td>
<td>Package C-State Limit (R/W)</td>
<td></td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 000b: C0/C1 (no package C-state support) 001b: C2 010b: C6 (non-retention) 011b: C6 (retention) 111b: No Package C state limits. All C states supported by the processor are available.</td>
</tr>
<tr>
<td>9:3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>I/O MWAIT Redirection Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/WO)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24:16</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>C3 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>C1 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>26</td>
<td></td>
<td>Enable C3 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>27</td>
<td></td>
<td>Enable C1 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>28</td>
<td></td>
<td>Package C State Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>29</td>
<td></td>
<td>Package C State UnDemotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>63:31</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>179H</td>
<td>377</td>
<td></td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>Global Machine Check Capability (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td></td>
<td>Count</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8</td>
<td></td>
<td>MCG_CTL_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>9</td>
<td></td>
<td>MCG_EXT_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>10</td>
<td></td>
<td>MCP_CMCI_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>11</td>
<td></td>
<td>MCG_TES_P</td>
<td></td>
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</tr>
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<td>15:12</td>
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<td>Reserved</td>
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</tr>
<tr>
<td></td>
<td>23:16</td>
<td></td>
<td>MCG_EXT_CNT</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>24</td>
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<td>MCG_SER_P</td>
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</tr>
<tr>
<td></td>
<td>25</td>
<td></td>
<td>MCG_EM_P</td>
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<tr>
<td></td>
<td>26</td>
<td></td>
<td>MCG_ELOG_P</td>
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<td></td>
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<tr>
<td></td>
<td>63:27</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17DH</td>
<td>390</td>
<td></td>
<td>MSR_SMM_MCA_CAP</td>
<td>THREAD</td>
<td>Enhanced SMM Capabilities (SMM-RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reports SMM capability Enhancement. Accessible only while in SMM.</td>
</tr>
<tr>
<td></td>
<td>57:0</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>58</td>
<td></td>
<td>SMM_Code_Access_Chk (SMM-RO)</td>
<td></td>
<td>If set to 1 indicates that the SMM code access restriction is supported and a host-space interface available to SMM handler.</td>
</tr>
<tr>
<td></td>
<td>59</td>
<td></td>
<td>Long_Flow_Indication (SMM-RO)</td>
<td></td>
<td>If set to 1 indicates that the SMM long flow indicator is supported and a host-space interface available to SMM handler.</td>
</tr>
<tr>
<td></td>
<td>63:60</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17FH</td>
<td>383</td>
<td></td>
<td>MSR_ERROR_CONTROL</td>
<td>Package</td>
<td>MC Bank Error Configuration (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>MemError Log Enable (R/W)</td>
<td></td>
<td>When set, enables IMC status bank to log additional info in bits 36:32.</td>
</tr>
<tr>
<td></td>
<td>63:2</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1ADH</td>
<td>429</td>
<td></td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0, Rw if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
</tbody>
</table>
### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 1C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 2C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 3C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 4C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td>39:32</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 5C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 5 core active.</td>
</tr>
<tr>
<td>47:40</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 6C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 6 core active.</td>
</tr>
<tr>
<td>55:48</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 7C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 7 core active.</td>
</tr>
<tr>
<td>63:56</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 8C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 8 core active.</td>
</tr>
<tr>
<td>1AEH</td>
<td>MSR_TURBO_RATIO_LIMIT1</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit of Turbo Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rw if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 9C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 9 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 10C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 10 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 11C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 11 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 12C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 12 core active.</td>
</tr>
<tr>
<td>39:32</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 13C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 13 core active.</td>
</tr>
<tr>
<td>47:40</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 14C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 14 core active.</td>
</tr>
<tr>
<td>55:48</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 15C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 15 core active.</td>
</tr>
<tr>
<td>63:56</td>
<td>Package</td>
<td></td>
<td><strong>Maximum Ratio Limit for 16C</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit of 16 core active.</td>
</tr>
<tr>
<td>1AFH</td>
<td>MSR_TURBO_RATIO_LIMIT2</td>
<td>Package</td>
<td><strong>Maximum Ratio Limit of Turbo Mode</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Rw if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
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### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
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<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
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<td>Maximum Ratio Limit for 17C</td>
</tr>
<tr>
<td>7:0</td>
<td>Package</td>
<td></td>
<td>Maximum turbo ratio limit of 17 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for 18C</td>
</tr>
<tr>
<td>62:16</td>
<td>Package</td>
<td></td>
<td>Maximum turbo ratio limit of 18 core active.</td>
</tr>
<tr>
<td>63</td>
<td>Package</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>414H</td>
<td>1044</td>
<td>MSR_MC5_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>415H</td>
<td>1045</td>
<td>MSR_MC5_STATUS</td>
<td>Bank MC5 reports MC error from the Intel QPI 0 module.</td>
</tr>
<tr>
<td>416H</td>
<td>1046</td>
<td>MSR_MC5_ADDR</td>
<td></td>
</tr>
<tr>
<td>417H</td>
<td>1047</td>
<td>MSR_MC5_MISC</td>
<td></td>
</tr>
<tr>
<td>418H</td>
<td>1048</td>
<td>MSR_MC6_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>419H</td>
<td>1049</td>
<td>MSR_MC6_STATUS</td>
<td>Bank MC6 reports MC error from the integrated I/O module.</td>
</tr>
<tr>
<td>41AH</td>
<td>1050</td>
<td>MSR_MC6_ADDR</td>
<td></td>
</tr>
<tr>
<td>41BH</td>
<td>1051</td>
<td>MSR_MC6_MISC</td>
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</tr>
<tr>
<td>41CH</td>
<td>1052</td>
<td>MSR_MC7_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>41DH</td>
<td>1053</td>
<td>MSR_MC7_STATUS</td>
<td>Bank MC7 reports MC error from the home agent HA 0.</td>
</tr>
<tr>
<td>41EH</td>
<td>1054</td>
<td>MSR_MC7_ADDR</td>
<td></td>
</tr>
<tr>
<td>41FH</td>
<td>1055</td>
<td>MSR_MC7_MISC</td>
<td></td>
</tr>
<tr>
<td>420H</td>
<td>1056</td>
<td>MSR_MC8_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>421H</td>
<td>1057</td>
<td>MSR_MC8_STATUS</td>
<td>Bank MC8 reports MC error from the home agent HA 1.</td>
</tr>
<tr>
<td>422H</td>
<td>1058</td>
<td>MSR_MC8_ADDR</td>
<td></td>
</tr>
<tr>
<td>423H</td>
<td>1059</td>
<td>MSR_MC8_MISC</td>
<td></td>
</tr>
<tr>
<td>424H</td>
<td>1060</td>
<td>MSR_MC9_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>425H</td>
<td>1061</td>
<td>MSR_MC9_STATUS</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>426H</td>
<td>1062</td>
<td>MSR_MC9_ADDR</td>
<td></td>
</tr>
<tr>
<td>427H</td>
<td>1063</td>
<td>MSR_MC9_MISC</td>
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</tr>
<tr>
<td>428H</td>
<td>1064</td>
<td>MSR_MC10_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>429H</td>
<td>1065</td>
<td>MSR_MC10_STATUS</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>42AH</td>
<td>1066</td>
<td>MSR_MC10_ADDR</td>
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</tr>
<tr>
<td>42BH</td>
<td>1067</td>
<td>MSR_MC10_MISC</td>
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</tr>
<tr>
<td>42CH</td>
<td>1068</td>
<td>MSR_MC11_CTL</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>42DH</td>
<td>1069</td>
<td>MSR_MC11_STATUS</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>42EH</td>
<td>1070</td>
<td>MSR_MC11_ADDR</td>
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</tr>
<tr>
<td>42FH</td>
<td>1071</td>
<td>MSR_MC11_MISC</td>
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</tr>
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</table>
### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
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<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>430H 1072</td>
<td>MSR_MC12_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>431H 1073</td>
<td>MSR_MC12_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>432H 1074</td>
<td>MSR_MC12_ADDR</td>
<td>Package</td>
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</tr>
<tr>
<td>433H 1075</td>
<td>MSR_MC12_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>434H 1076</td>
<td>MSR_MC13_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>435H 1077</td>
<td>MSR_MC13_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>436H 1078</td>
<td>MSR_MC13_ADDR</td>
<td>Package</td>
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<tr>
<td>437H 1079</td>
<td>MSR_MC13_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>438H 1080</td>
<td>MSR_MC14_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>439H 1081</td>
<td>MSR_MC14_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>43AH 1082</td>
<td>MSR_MC14_ADDR</td>
<td>Package</td>
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</tr>
<tr>
<td>43BH 1083</td>
<td>MSR_MC14_MISC</td>
<td>Package</td>
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</tr>
<tr>
<td>43CH 1084</td>
<td>MSR_MC15_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>43DH 1085</td>
<td>MSR_MC15_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>43EH 1086</td>
<td>MSR_MC15_ADDR</td>
<td>Package</td>
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</tr>
<tr>
<td>43FH 1087</td>
<td>MSR_MC15_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>440H 1088</td>
<td>MSR_MC16_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>441H 1089</td>
<td>MSR_MC16_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>442H 1090</td>
<td>MSR_MC16_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>443H 1091</td>
<td>MSR_MC16_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td>Bank MC17 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo0, CBo3, CBo6, CBo9, CBo12, CBo15.</td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
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</tr>
<tr>
<td>448H 1096</td>
<td>MSR_MC18_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>449H 1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
<td>Bank MC18 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo1, CBo4, CBo7, CBo10, CBo13, CBo16.</td>
</tr>
<tr>
<td>44AH 1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44BH 1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44CH 1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>44DH 1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
<td>Bank MC19 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo2, CBo5, CBo8, CBo11, CBo14, CBo17.</td>
</tr>
<tr>
<td>44EH 1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44FH 1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>450H 1104</td>
<td>MSR_MC20_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, &quot;IA32_MCI_CTL MSRs.&quot; through Section 15.3.2.4, &quot;IA32_MCI_MISC MSRs.&quot;.</td>
</tr>
<tr>
<td>451H 1105</td>
<td>MSR_MC20_STATUS</td>
<td>Package</td>
<td>Bank MC20 reports MC error from the Intel QPI 1 module.</td>
</tr>
<tr>
<td>452H 1106</td>
<td>MSR_MC20_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>453H 1107</td>
<td>MSR_MC20_MISC</td>
<td>Package</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>454H 1108</td>
<td>MSR_MC21_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.” through Section 15.3.2.4, “IA32_MCi_MISC MSRs.”. Bank MC21 reports MC error from the Intel QPI 2 module.</td>
</tr>
<tr>
<td>455H 1109</td>
<td>MSR_MC21_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>456H 1110</td>
<td>MSR_MC21_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>457H 1111</td>
<td>MSR_MC21_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>606H 1542</td>
<td>MSR_RAPL_POWER_UNIT</td>
<td>Package</td>
<td>Unit Multipliers used in RAPL Interfaces (R/O)</td>
</tr>
<tr>
<td></td>
<td>3:0</td>
<td>Package</td>
<td>Power Units</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
</tr>
<tr>
<td></td>
<td>7:4</td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>12:8</td>
<td>Package</td>
<td>Energy Status Units</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Energy related information (in joules) is based on the multiplier, 1/2^ESU; where ESU is an unsigned integer represented by bits 12:8. Default value is 0EH (or 61 micro-joules)</td>
</tr>
<tr>
<td></td>
<td>15:13</td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>19:16</td>
<td>Package</td>
<td>Time Units</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
</tr>
<tr>
<td></td>
<td>63:20</td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td>618H 1560</td>
<td>MSR_DRAM_POWER_LIMIT</td>
<td>Package</td>
<td>DRAM RAPL Power Limit Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>619H 1561</td>
<td>MSR_DRAM_ENERGY_STATUS</td>
<td>Package</td>
<td>DRAM Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>618H 1563</td>
<td>MSR_DRAM_PERF_STATUS</td>
<td>Package</td>
<td>DRAM Performance Throttling Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>61CH 1564</td>
<td>MSR_DRAM_POWER_INFO</td>
<td>Package</td>
<td>DRAM RAPL Parameters (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>690H 1680</td>
<td>MSR_CORE_PERF_LIMIT_REASONS</td>
<td>Package</td>
<td>Indicator of Frequency Clipping in Processor Cores (R/W) (frequency refers to processor core frequency)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>PROCHOT Status (R0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, processor core frequency is reduced below the operating system request due to assertion of external PROCHOT.</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>Thermal Status (R0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a thermal event.</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>Power Budget Management Status (R0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to PBM limit</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>Platform Configuration Services Status (R0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to PCS limit</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
<td>Reserved.</td>
</tr>
</tbody>
</table>
### Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>Autonomous Utilization-Based Frequency Control Status (R0)</td>
<td>When set, frequency is reduced below the operating system request because the processor has detected that utilization is low</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VR Therm Alert Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to a thermal alert from the Voltage Regulator.</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Electrical Design Point Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to electrical design point constraints (e.g. maximum electrical current consumption).</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Multi-Core Turbo Status (R0)</td>
<td>When set, frequency is reduced below the operating system request due to Multi-Core Turbo limits</td>
<td></td>
</tr>
<tr>
<td>12:11</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Core Frequency P1 Status (R0)</td>
<td>When set, frequency is reduced below max non-turbo P1</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Core Max n-core Turbo Frequency Limiting Status (R0)</td>
<td>When set, frequency is reduced below max n-core turbo frequency</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Core Frequency Limiting Status (R0)</td>
<td>When set, frequency is reduced below the operating system request.</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>PROCHOT Log</td>
<td>When set, indicates that the PROCHOT Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Thermal Log</td>
<td>When set, indicates that the Thermal Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Power Budget Management Log</td>
<td>When set, indicates that the PBM Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Platform Configuration Services Log</td>
<td>When set, indicates that the PCS Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Scope</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>--------------</td>
<td>-------</td>
<td>-----------------</td>
</tr>
<tr>
<td>C8DH 3213</td>
<td>IA32_QM_EVTSEL</td>
<td>THREAD</td>
<td>Monitoring Event Select Register (R/W).</td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td></td>
<td>if CPUID.(EAX=07H, ECX=0):EBX.PQM[bit 12] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>EventID (RW)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Event encoding:</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0: no monitoring</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x1: L3 occupancy monitoring</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>all other encoding reserved.</td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>41:32</td>
<td></td>
<td>RMID (RW)</td>
<td></td>
</tr>
</tbody>
</table>

Table 35-27. Additional MSRs Supported by Intel® Xeon® Processor E5 v3 Family

- **21**: Autonomous Utilization-Based Frequency Control Log
  - When set, indicates that the AUBFC Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **22**: VR Therm Alert Log
  - When set, indicates that the VR Therm Alert Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **23**: Reserved.

- **24**: Electrical Design Point Log
  - When set, indicates that the EDP Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **25**: Reserved.

- **26**: Multi-Core Turbo Log
  - When set, indicates that the Multi-Core Turbo Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **28:27**: Reserved.

- **29**: Core Frequency P1 Log
  - When set, indicates that the Core Frequency P1 Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **30**: Core Max n-core Turbo Frequency Limiting Log
  - When set, indicates that the Core Max n-core Turbo Frequency Limiting Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.

- **31**: Core Frequency Limiting Log
  - When set, indicates that the Core Frequency Limiting Status bit has asserted since the log bit was last cleared.
  - This log bit will remain set until cleared by software writing 0.
### 35.11.1 Additional Uncore PMU MSRs in the Intel® Xeon® Processor E5 v3 Family

Intel Xeon Processor E5 v3 and E7 v3 family are based on the Haswell-E microarchitecture. The MSR-based uncore PMU interfaces are listed in Table 35-28. For complete detail of the uncore PMU, refer to Intel Xeon Processor E5 v3 Product Family Uncore Performance Monitoring Guide. These processors have a CPUID signature with DisplayFamily_DisplayModel of 06_3FH.

#### Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>700H</td>
<td>MSR_PMON_GLOBAL_CTL</td>
<td>Package</td>
<td>Uncore perfmon per-socket global control.</td>
</tr>
<tr>
<td>701H</td>
<td>MSR_PMON_GLOBAL_STATUS</td>
<td>Package</td>
<td>Uncore perfmon per-socket global status.</td>
</tr>
<tr>
<td>702H</td>
<td>MSR_PMON_GLOBAL_CONFIG</td>
<td>Package</td>
<td>Uncore perfmon per-socket global configuration.</td>
</tr>
<tr>
<td>703H</td>
<td>MSR_U_PMON_UCLK_FIXED_CTL</td>
<td>Package</td>
<td>Uncore U-box UCLK fixed counter control</td>
</tr>
<tr>
<td>704H</td>
<td>MSR_U_PMON_UCLK_FIXED_CTR</td>
<td>Package</td>
<td>Uncore U-box UCLK fixed counter</td>
</tr>
<tr>
<td>705H</td>
<td>MSR_U_PMON_EVTSEL0</td>
<td>Package</td>
<td>Uncore U-box perfmon event select for U-box counter 0.</td>
</tr>
<tr>
<td>706H</td>
<td>MSR_U_PMON_EVTSEL1</td>
<td>Package</td>
<td>Uncore U-box perfmon event select for U-box counter 1.</td>
</tr>
<tr>
<td>708H</td>
<td>MSR_U_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore U-box perfmon U-box wide status.</td>
</tr>
<tr>
<td>709H</td>
<td>MSR_U_PMON_CTR0</td>
<td>Package</td>
<td>Uncore U-box perfmon counter 0</td>
</tr>
<tr>
<td>70AH</td>
<td>MSR_U_PMON_CTR1</td>
<td>Package</td>
<td>Uncore U-box perfmon counter 1</td>
</tr>
<tr>
<td>710H</td>
<td>MSR_PCU_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore PCU perfmon for PCU-box-wide control</td>
</tr>
<tr>
<td>711H</td>
<td>MSR_PCU_PMON_EVTSEL0</td>
<td>Package</td>
<td>Uncore PCU perfmon event select for PCU counter 0.</td>
</tr>
<tr>
<td>712H</td>
<td>MSR_PCU_PMON_EVTSEL1</td>
<td>Package</td>
<td>Uncore PCU perfmon event select for PCU counter 1.</td>
</tr>
</tbody>
</table>
Table 35-28. Uncore PMUs in Intel® Xeon® Processor E5 v3 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>713H</td>
<td>MSR_PCU_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore PCU perfmon event select for PCU counter 2.</td>
</tr>
<tr>
<td>714H</td>
<td>MSR_PCU_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore PCU perfmon event select for PCU counter 3.</td>
</tr>
<tr>
<td>715H</td>
<td>MSR_PCU_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore PCU perfmon box-wide filter.</td>
</tr>
<tr>
<td>716H</td>
<td>MSR_PCU_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore PCU perfmon box wide status.</td>
</tr>
<tr>
<td>717H</td>
<td>MSR_PCU_PMON_CTR0</td>
<td>Package</td>
<td>Uncore PCU perfmon counter 0.</td>
</tr>
<tr>
<td>718H</td>
<td>MSR_PCU_PMON_CTR1</td>
<td>Package</td>
<td>Uncore PCU perfmon counter 1.</td>
</tr>
<tr>
<td>719H</td>
<td>MSR_PCU_PMON_CTR2</td>
<td>Package</td>
<td>Uncore PCU perfmon counter 2.</td>
</tr>
<tr>
<td>71AH</td>
<td>MSR_PCU_PMON_CTR3</td>
<td>Package</td>
<td>Uncore PCU perfmon counter 3.</td>
</tr>
<tr>
<td>720H</td>
<td>MSR_S0_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon for SBo 0 box-wide control</td>
</tr>
<tr>
<td>721H</td>
<td>MSR_S0_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon event select for SBo 0 counter 0.</td>
</tr>
<tr>
<td>722H</td>
<td>MSR_S0_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon event select for SBo 0 counter 1.</td>
</tr>
<tr>
<td>723H</td>
<td>MSR_S0_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon event select for SBo 0 counter 2.</td>
</tr>
<tr>
<td>724H</td>
<td>MSR_S0_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon event select for SBo 0 counter 3.</td>
</tr>
<tr>
<td>725H</td>
<td>MSR_S0_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon box-wide filter.</td>
</tr>
<tr>
<td>726H</td>
<td>MSR_S0_PMON_CTR0</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon counter 0.</td>
</tr>
<tr>
<td>727H</td>
<td>MSR_S0_PMON_CTR1</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon counter 1.</td>
</tr>
<tr>
<td>728H</td>
<td>MSR_S0_PMON_CTR2</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon counter 2.</td>
</tr>
<tr>
<td>729H</td>
<td>MSR_S0_PMON_CTR3</td>
<td>Package</td>
<td>Uncore SBo 0 perfmon counter 3.</td>
</tr>
<tr>
<td>72AH</td>
<td>MSR_S1_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon for SBo 1 box-wide control</td>
</tr>
<tr>
<td>72BH</td>
<td>MSR_S1_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon event select for SBo 1 counter 0.</td>
</tr>
<tr>
<td>72CH</td>
<td>MSR_S1_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon event select for SBo 1 counter 1.</td>
</tr>
<tr>
<td>72DH</td>
<td>MSR_S1_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon event select for SBo 1 counter 2.</td>
</tr>
<tr>
<td>72EH</td>
<td>MSR_S1_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon event select for SBo 1 counter 3.</td>
</tr>
<tr>
<td>72FH</td>
<td>MSR_S1_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon box-wide filter.</td>
</tr>
<tr>
<td>730H</td>
<td>MSR_S1_PMON_CTR0</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon counter 0.</td>
</tr>
<tr>
<td>731H</td>
<td>MSR_S1_PMON_CTR1</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon counter 1.</td>
</tr>
<tr>
<td>732H</td>
<td>MSR_S1_PMON_CTR2</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon counter 2.</td>
</tr>
<tr>
<td>733H</td>
<td>MSR_S1_PMON_CTR3</td>
<td>Package</td>
<td>Uncore SBo 1 perfmon counter 3.</td>
</tr>
<tr>
<td>734H</td>
<td>MSR_S2_PMON_BOX_CTL</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon for SBo 2 box-wide control</td>
</tr>
<tr>
<td>735H</td>
<td>MSR_S2_PMON_EVNTSEL0</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon event select for SBo 2 counter 0.</td>
</tr>
<tr>
<td>736H</td>
<td>MSR_S2_PMON_EVNTSEL1</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon event select for SBo 2 counter 1.</td>
</tr>
<tr>
<td>737H</td>
<td>MSR_S2_PMON_EVNTSEL2</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon event select for SBo 2 counter 2.</td>
</tr>
<tr>
<td>738H</td>
<td>MSR_S2_PMON_EVNTSEL3</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon event select for SBo 2 counter 3.</td>
</tr>
<tr>
<td>739H</td>
<td>MSR_S2_PMON_BOX_FILTER</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon box-wide filter.</td>
</tr>
<tr>
<td>73AH</td>
<td>MSR_S2_PMON_CTR0</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon counter 0.</td>
</tr>
<tr>
<td>73BH</td>
<td>MSR_S2_PMON_CTR1</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon counter 1.</td>
</tr>
<tr>
<td>73CH</td>
<td>MSR_S2_PMON_CTR2</td>
<td>Package</td>
<td>Uncore SBo 2 perfmon counter 2.</td>
</tr>
</tbody>
</table>
### Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
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### Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family (Contd.)

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Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family (Contd.)

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### Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family (Contd.)

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### Table 35-28. Uncore PMUs in Intel® Xeon® Processor E5 v3 Family (Contd.)

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<tr>
<td>F15H</td>
<td>MSR_C17_PMON_BOX_FILTER0</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon box wide filter0.</td>
</tr>
<tr>
<td>F16H</td>
<td>MSR_C17_PMON_BOX_FILTER1</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon box wide filter1.</td>
</tr>
</tbody>
</table>
35.12 MSRS IN INTEL® CORE™ M PROCESSORS AND 5TH GENERATION INTEL CORE PROCESSORS

The Intel® Core™ M-5xxx processors and 5th generation Intel® Core™ Processors, and Intel® Xeon® Processor E3-1200 v4 family are based on the Broadwell microarchitecture. The Intel® Core™ M-5xxx processors and 5th generation Intel® Core™ Processors have CPUID DisplayFamily_DisplayModel signature 06_3DH. Intel® Xeon® Processor E3-1200 v4 family and the 5th generation Intel® Core™ Processors have CPUID DisplayFamily_DisplayModel signature 06_47H. Processors with signatures 06_3DH and 06_47H support the MSR interfaces listed in Table 35-16, Table 35-17, Table 35-20, Table 35-24, Table 35-25, Table 35-29, and Table 35-30. For an MSR listed in Table 35-30 that also appears in the model-specific tables of prior generations, Table 35-30 supercede prior generation tables.

Table 35-29 lists MSRs that are common to processors based on the Broadwell microarchitectures (including CPUID signatures 06_3DH, 06_47H, 06_4FH, and 06_56H).

Table 35-28. Uncore PMU MSRs in Intel® Xeon® Processor E5 v3 Family (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F17H</td>
<td>MSR_C17_PMON_BOX_STATUS</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon box wide status.</td>
</tr>
<tr>
<td>F18H</td>
<td>MSR_C17_PMON_CTR0</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon counter 0.</td>
</tr>
<tr>
<td>F19H</td>
<td>MSR_C17_PMON_CTR1</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon counter 1.</td>
</tr>
<tr>
<td>F1AH</td>
<td>MSR_C17_PMON_CTR2</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon counter 2.</td>
</tr>
<tr>
<td>F1BH</td>
<td>MSR_C17_PMON_CTR3</td>
<td>Package</td>
<td>Uncore C-box 17 perfmon counter 3.</td>
</tr>
</tbody>
</table>

Table 35-29. Additional MSRs Common to Processors Based the Broadwell Microarchitectures

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>38EH</td>
<td>IA32_PERF_GLOBAL_STATUS</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>0</td>
<td>Ovf_PMC0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Ovf_PMC1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Ovf_PMC2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Ovf_PMC3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Ovf_FixedCtr0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Ovf_FixedCtr1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Ovf_FixedCtr2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>54:35</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Trace_ToPA_PMI. See Section 36.2.4.2, “Table of Physical Addresses (ToPA).”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60:56</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Ovf_Uncore</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Ovf_BufDSSAVE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>CondChgd</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Model-Specific Registers (MSRs)

### Table 35-29. Additional MSRs Common to Processors Based the Broadwell Microarchitectures

<table>
<thead>
<tr>
<th>Register Address Hex</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>390H 912</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.4.2, “Global Counter Control Facilities.”</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_PMC0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_PMC1</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_PMC2</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_PMC3</td>
</tr>
<tr>
<td>31:4</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_FixedCtr0</td>
</tr>
<tr>
<td>33</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_FixedCtr1</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_FixedCtr2</td>
</tr>
<tr>
<td>54:35</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>55</td>
<td></td>
<td></td>
<td>Set 1 to clear Trace_ToPA_PMI. See Section 36.2.4.2, “Table of Physical Addresses (ToPA).”</td>
</tr>
<tr>
<td>60:56</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_Uncore</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
<td>Set 1 to clear Ovf_BufDSSAVE</td>
</tr>
<tr>
<td>63</td>
<td></td>
<td></td>
<td>Set 1 to clear CondChgd</td>
</tr>
<tr>
<td>560H 1376</td>
<td>IA32_RTIT_OUTPUT_BASE</td>
<td>THREAD</td>
<td>Trace Output Base Register (R/W)</td>
</tr>
<tr>
<td>6:0</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>MAXPHYADDR1-7</td>
<td></td>
<td></td>
<td>Base physical address.</td>
</tr>
<tr>
<td>63:MAXPHYADDR</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>561H 1377</td>
<td>IA32_RTIT_OUTPUT_MASK_PTRS</td>
<td>THREAD</td>
<td>Trace Output Mask Pointers Register (R/W)</td>
</tr>
<tr>
<td>6:0</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>31:7</td>
<td></td>
<td></td>
<td>MaskOrTableOffset</td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td></td>
<td>Output Offset.</td>
</tr>
<tr>
<td>570H 1392</td>
<td>IA32_RTIT_CTL</td>
<td>Thread</td>
<td>Trace Control Register (R/W)</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>TraceEn</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Reserved, MBZ.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>OS</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>User</td>
</tr>
<tr>
<td>6:4</td>
<td></td>
<td></td>
<td>Reserved, MBZ</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>CR3 filter</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>ToPA; writing 0 will #GP if also setting TraceEn</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td>Reserved, MBZ</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td>TSCEn</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td></td>
<td>DisRETC</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
<td>Reserved, MBZ</td>
</tr>
</tbody>
</table>
Table 35-29. Additional MSRs Common to Processors Based the Broadwell Microarchitectures

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13</td>
<td>Reserved; writing 0 will #GP if also setting TraceEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:14</td>
<td>Reserved, MBZ.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>571H 1393</td>
<td>IA32_RTIT_STATUS</td>
<td>Thread</td>
<td>Tracing Status Register (R/W)</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, writes ignored.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ContextEn, writes ignored.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TriggerEn, writes ignored.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Error (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Stopped</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:6</td>
<td>Reserved, MBZ.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>572H 1394</td>
<td>IA32_RTIT_CR3_MATCH</td>
<td>THREAD</td>
<td>Trace Filter CR3 Match Register (R/W)</td>
</tr>
<tr>
<td>4:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:5</td>
<td>CR3[63:5] value to match</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. MAXPHYADDR is reported by CPUID.80000008H:EAX[7:0].

Table 35-30 lists MSRs that are specific to Intel Core M processors and 5th Generation Intel Core Processors.

Table 35-30. Additional MSRs Supported by Intel® Core™ M Processors and 5th Generation Intel® Core™ Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONFIG_CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWait extension C-state parameters or ACPI C-states. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
</tbody>
</table>
### Table 35-30. Additional MSRs Supported by Intel® Core™ M Processors and 5th Generation Intel® Core™ Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3:0</td>
<td>Package C-State Limit (R/W)</td>
<td>Package</td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 0000b: C0/C1 (no package C-state support) 0001b: C2 0010b: C3 0011b: C6 0100b: C7 0101b: C7s 0110b: C8 0111b: C9 1000b: C10</td>
</tr>
<tr>
<td>9:4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>I/O MWait Redirection Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/W/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24:16</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>C3 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C1 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Enable C3 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Enable C1 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>Enable Package C-State Auto-demotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Enable Package C-State Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:31</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode R0 if MSR_PLATFORM_INFO[28] = 0, Rw if MSR_PLATFORM_INFO[28] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Package</td>
<td>Maximum Ratio Limit for 1C</td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td>Maximum Ratio Limit for 2C</td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Package</td>
<td>Maximum Ratio Limit for 3C</td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Package</td>
<td>Maximum Ratio Limit for 4C</td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td>39:32</td>
<td>Package</td>
<td>Maximum Ratio Limit for 5C</td>
<td>Maximum turbo ratio limit of 5 core active.</td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

35.13 MSRS IN NEXT GENERATION INTEL® XEON® PROCESSORS

The MSRs listed in Table 35-31 are available and common to Intel® Xeon® Processor D product Family (CPUID DisplayFamily_DisplayModel = 06_56H) and to next generation of Intel Xeon processors (CPUID DisplayFamily_DisplayModel = 06_4FH). They are based on the Broadwell microarchitecture.

See Section 35.13.1 for lists of tables of MSRs that are supported by Intel® Xeon® Processor D Family.

### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSR_PPIN_CTL</td>
<td>Package</td>
<td>Maximum Ratio Limit for 6C</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Maximum turbo ratio limit of 6core active.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:2</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>MSR_PPIN</td>
<td>Package</td>
<td>Protected Processor Inventory Number (R/O)</td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>15:8</td>
<td></td>
<td>Maximum Non-Turbo Ratio (R/O)</td>
</tr>
<tr>
<td>22:16</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>PPIN_CAP (R/O)</td>
</tr>
<tr>
<td>27:24</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td>Programmable Ratio Limit for Turbo Mode (R/O)</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>Programmable TDP Limit for Turbo Mode (R/O)</td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-17, Table 35-20, Table 35-24, Table 35-25, Table 35-29 for other MSR definitions applicable to processors with CPUID signature 06_3DH.

See Table 35-30, Additional MSRs Supported by Intel® Core™ M Processors and 5th Generation Intel® Core™ Processors.
### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>Package</td>
<td>Programmable TJ OFFSET (R/O)</td>
<td>See Table 35-21.</td>
</tr>
<tr>
<td>39:30</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47:40</td>
<td>Package</td>
<td>Maximum Efficiency Ratio (R/O)</td>
<td>See Table 35-21.</td>
</tr>
<tr>
<td>63:48</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_ CONTROL</td>
<td>Core</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWait extension C-state parameters or ACPI C-states. See <a href="http://biosbits.org">http://biosbits.org</a>.</td>
</tr>
<tr>
<td>2:0</td>
<td>Package</td>
<td>Package C-State Limit (R/W)</td>
<td>Specifies the lowest processor-specific C-state code name (consuming the least power) for the package. The default is set as factory-configured package C-state limit. The following C-state code name encodings are supported: 000b: C0/C1 (no package C-state support) 001b: C2 010b: C6 (non-retention) 011b: C6 (retention) 111b: No Package C state limits. All C states supported by the processor are available.</td>
</tr>
<tr>
<td>9:3</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>I/O MWait Redirection Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>CFG Lock (R/W/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Automatic C-State Conversion Enable (R/W)</td>
<td></td>
<td>If 1, the processor will convert HALT or MWait(C1) to MWait(C6)</td>
</tr>
<tr>
<td>24:17</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>C3 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>C1 State Auto Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Enable C3 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>Enable C1 Undemotion (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>Package C State Demotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Package C State UnDemotion Enable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:31</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>Thread</td>
<td>Global Machine Check Capability (R/O)</td>
</tr>
<tr>
<td>7:0</td>
<td>Count</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>MCG_CTL_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MCG_EXT_P</td>
<td></td>
<td></td>
</tr>
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</table>
Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MCP_CMCI_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>MCG_TES_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:12</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>MCG_EXT_CNT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>MCG_SER_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>MCG_EM_P</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:27</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17DH 390</td>
<td>MSR_SMM_MCA_CAP THREAD</td>
<td></td>
<td>Enhanced SMM Capabilities (SMM-RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Reports SMM capability Enhancement. Accessible only while in SMM.</td>
</tr>
<tr>
<td>57:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>SMM_Code_Access_Chk (SMM-RO)</td>
<td></td>
<td>If set to 1 indicates that the SMM code access restriction is supported and a host-space interface available to SMM handler.</td>
</tr>
<tr>
<td>59</td>
<td>Long_Flow_Indication (SMM-RO)</td>
<td></td>
<td>If set to 1 indicates that the SMM long flow indicator is supported and a host-space interface available to SMM handler.</td>
</tr>
<tr>
<td>63:60</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS Core</td>
<td></td>
<td>Thermal Monitor Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>0</td>
<td>Thermal status (RO)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>1</td>
<td>Thermal status log (R/WC0)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>2</td>
<td>PROTOCHOT # or FORCEPR# status (RO)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>3</td>
<td>PROTOCHOT # or FORCEPR# log (R/WC0)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>4</td>
<td>Critical Temperature status (RO)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>5</td>
<td>Critical Temperature status log (R/WC0)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>6</td>
<td>Thermal threshold #1 status (RO)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>7</td>
<td>Thermal threshold #1 log (R/WC0)</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8</td>
<td>Thermal threshold #2 status (RO)</td>
<td></td>
<td>See Table 35-2.</td>
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### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Thermal threshold #2 log (R/W/C0) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Power Limitation status (RO) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Power Limitation log (R/W/C0) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Current Limit status (RO) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Current Limit log (R/W/C0) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Cross Domain Limit status (RO) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Cross Domain Limit log (R/W/C0) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26:23</td>
<td>Reserved.</td>
<td></td>
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</tr>
<tr>
<td>30:27</td>
<td>Resolution in degrees Celsius (RO) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Reading Valid (RO) See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A2H 418</td>
<td>MSR_TEMPERATURE_TARGET Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Temperature Target (RO) See Table 35-21.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27:24</td>
<td>TCC Activation Offset (R/W) See Table 35-21.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:28</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT Package</td>
<td>Maximum Ratio Limit of Turbo Mode RO if MSR_PLATFORM_INFO[28] = 0, Rw if MSR_PLATFORM_INFO[28] = 1</td>
<td>Maximum Ratio Limit for 1C</td>
</tr>
<tr>
<td>7:0</td>
<td>Package</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td>Maximum Ratio Limit for 2C</td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Package</td>
<td>Maximum Ratio Limit for 3C</td>
<td></td>
</tr>
<tr>
<td>31:24</td>
<td>Package</td>
<td>Maximum Ratio Limit for 4C</td>
<td></td>
</tr>
<tr>
<td>39:32</td>
<td>Package</td>
<td>Maximum Ratio Limit for 5C</td>
<td></td>
</tr>
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</table>
### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tbody>
<tr>
<td>47:40</td>
<td>Package</td>
<td>Maximum Ratio Limit for 6C</td>
<td></td>
</tr>
<tr>
<td>55:48</td>
<td>Package</td>
<td>Maximum Ratio Limit for 7C</td>
<td></td>
</tr>
<tr>
<td>63:56</td>
<td>Package</td>
<td>Maximum Ratio Limit for 8C</td>
<td></td>
</tr>
<tr>
<td>1AEH 430</td>
<td>MSR_TURBO_RATIO_LIMIT1 Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO[28] = 0, Rw if MSR_PLATFORM_INFO[28] = 1</td>
<td></td>
</tr>
<tr>
<td>7:0 Package</td>
<td>Maximum Ratio Limit for 9C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:8 Package</td>
<td>Maximum Ratio Limit for 10C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16 Package</td>
<td>Maximum Ratio Limit for 11C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:24 Package</td>
<td>Maximum Ratio Limit for 12C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39:32 Package</td>
<td>Maximum Ratio Limit for 13C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47:40 Package</td>
<td>Maximum Ratio Limit for 14C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55:48 Package</td>
<td>Maximum Ratio Limit for 15C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:56 Package</td>
<td>Maximum Ratio Limit for 16C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>606H 1542</td>
<td>MSR_RAPL_POWER_UNIT Package</td>
<td>Unit Multipliers used in RAPL Interfaces (R/O)</td>
<td></td>
</tr>
<tr>
<td>3:0 Package</td>
<td>Power Units</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:4 Package</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12:8 Package</td>
<td>Energy Status Units</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Energy related information (in Joules) is based on the multiplier, 1/2^ESU; where ESU is an unsigned integer represented by bits 12:8. Default value is 0EH (or 61 micro-joules)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:13 Package</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19:16 Package</td>
<td>Time Units</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:20 Package</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>618H 1560</td>
<td>MSR_DRAM_POWER_LIMIT Package</td>
<td>DRAM RAPL Power Limit Control (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
<td></td>
<td></td>
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<tr>
<td>619H 1561</td>
<td>MSR_DRAM_ENERGY_STATUS Package</td>
<td>DRAM Energy Status (R/O)</td>
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</tr>
<tr>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
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<tr>
<td>61CH 1564</td>
<td>MSR_DRAM_POWER_INFO Package</td>
<td>DRAM RAPL Parameters (R/W)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>690H 1680</td>
<td>MSR_CORE_PERF_LIMIT_REAONS Package</td>
<td>Indicator of Frequency Clipping in Processor Cores (R/W) (frequency refers to processor core frequency)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>PROCHOT Status (R0)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When set, processor core frequency is reduced below the operating system request due to assertion of external PROCHOT.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Thermal Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a thermal event.</td>
</tr>
<tr>
<td>2</td>
<td>Power Budget Management Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to PBM limit</td>
</tr>
<tr>
<td>3</td>
<td>Platform Configuration Services Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to PCS limit</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Autonomous Utilization-Based Frequency Control Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request because the processor has detected that utilization is low</td>
</tr>
<tr>
<td>6</td>
<td>VR Therm Alert Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to a thermal alert from the Voltage Regulator.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Electrical Design Point Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to electrical design point constraints (e.g. maximum electrical current consumption).</td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Multi-Core Turbo Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request due to Multi-Core Turbo limits</td>
</tr>
<tr>
<td>12:11</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Core Frequency P1 Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below max non-turbo P1</td>
</tr>
<tr>
<td>14</td>
<td>Core Max n-core Turbo Frequency Limiting Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below max n-core turbo frequency</td>
</tr>
<tr>
<td>15</td>
<td>Core Frequency Limiting Status (R0)</td>
<td></td>
<td>When set, frequency is reduced below the operating system request.</td>
</tr>
<tr>
<td>16</td>
<td>PROCHOT Log</td>
<td></td>
<td>When set, indicates that the PROCHOT Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>17</td>
<td>Thermal Log</td>
<td></td>
<td>When set, indicates that the Thermal Status bit has asserted since the log bit was last cleared. This log bit will remain set until cleared by software writing 0.</td>
</tr>
</tbody>
</table>
### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

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<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>Power Budget Management Log</td>
<td></td>
<td>When set, indicates that the PBM Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>19</td>
<td>Platform Configuration Services Log</td>
<td></td>
<td>When set, indicates that the PCS Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Autonomous Utilization-Based Frequency Control Log</td>
<td></td>
<td>When set, indicates that the AUBFC Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>22</td>
<td>VR Therm Alert Log</td>
<td></td>
<td>When set, indicates that the VR Therm Alert Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>Electrical Design Point Log</td>
<td></td>
<td>When set, indicates that the EDP Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>25</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Multi-Core Turbo Log</td>
<td></td>
<td>When set, indicates that the Multi-Core Turbo Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>28:27</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>Core Frequency P1 Log</td>
<td></td>
<td>When set, indicates that the Core Frequency P1 Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>30</td>
<td>Core Max n-core Turbo Frequency Limiting Log</td>
<td></td>
<td>When set, indicates that the Core Max n-core Turbo Frequency Limiting Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>31</td>
<td>Core Frequency Limiting Log</td>
<td></td>
<td>When set, indicates that the Core Frequency Limiting Status bit has asserted since the log bit was last cleared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This log bit will remain set until cleared by software writing 0.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
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<td>Register Address</td>
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<td>Scope</td>
<td>Bit Description</td>
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<td>------------------</td>
<td>-----------------------</td>
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<td>-------------------------------------------------------------------------------</td>
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<tr>
<td>770H 1904</td>
<td>IA32_PM_ENABLE</td>
<td>Package</td>
<td>See Section 14.4.2, “Enabling HWP”</td>
</tr>
<tr>
<td>771H 1905</td>
<td>IA32_HWP_CAPABILITIES</td>
<td>Thread</td>
<td>See Section 14.4.3, “HWP Performance Range and Dynamic Capabilities”</td>
</tr>
<tr>
<td>774H 1908</td>
<td>IA32_HWP_REQUEST</td>
<td>Thread</td>
<td>See Section 14.4.4, “Managing HWP”</td>
</tr>
<tr>
<td>777H 1911</td>
<td>IA32_HWP&gt;Status</td>
<td>Thread</td>
<td>See Section 14.4.5, “HWP Feedback”</td>
</tr>
<tr>
<td>C8DH 3213</td>
<td>IA32_QM_EVTSEL</td>
<td>THREAD</td>
<td>Monitoring Event Select Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>if CPUID.(EAX=07H, ECX=0):EBX.PQM[bit 12] = 1</td>
</tr>
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<td>7:0</td>
<td>EventID (R/W)</td>
<td></td>
<td>Event encoding:</td>
</tr>
<tr>
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<td>0x00: no monitoring</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x01: L3 occupancy</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x02: Total memory bandwidth</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>0x03: Local memory bandwidth</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>All other encoding reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>41:32</td>
<td>RMID (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:42</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C8FH 3215</td>
<td>IA32_PQR_ASSOC</td>
<td>THREAD</td>
<td>Resource Association Register (R/W)</td>
</tr>
<tr>
<td>9:0</td>
<td>RMID</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:10</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>51:32</td>
<td>COS (R/W).</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:52</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C90H 3216</td>
<td>IA32_L3_QOS_MASK_0</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 0 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=0</td>
</tr>
<tr>
<td>0:19</td>
<td>CBM: Bit vector of available L3 ways for COS 0 enforcement</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:20</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C91H 3217</td>
<td>IA32_L3_QOS_MASK_1</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=1</td>
</tr>
<tr>
<td>0:19</td>
<td>CBM: Bit vector of available L3 ways for COS 1 enforcement</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:20</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-31. Additional MSRs Common to Intel® Xeon® Processor D and Next Generation Intel Xeon Processors Based on the Broadwell Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C92H 3218</td>
<td>IA32_L3_QOS_MASK_2</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 2 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 2 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td>C93H 3219</td>
<td>IA32_L3_QOS_MASK_3</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 3 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 3 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 4 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td>C95H 3221</td>
<td>IA32_L3_QOS_MASK_5</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 5 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 5 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td>C96H 3222</td>
<td>IA32_L3_QOS_MASK_6</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 6 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 6 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td>C97H 3223</td>
<td>IA32_L3_QOS_MASK_7</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 7 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=7</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 7 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td>C98H 3224</td>
<td>IA32_L3_QOS_MASK_8</td>
<td>Package</td>
<td>L3 Class Of Service Mask - COS 8 (R/W). if CPUID.(EAX=10H, ECX=1):EDX.COS_MAX[15:0] &gt;=8</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 8 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 9 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0:19 CBM: Bit vector of available L3 ways for COS 10 enforcement</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:20 Reserved</td>
</tr>
</tbody>
</table>
35.13.1 Additional MSRs Supported in the Intel® Xeon® Processor D Product Family

The MSRs listed in Table 35-32 are available to Intel® Xeon® Processor D Product Family (CPUID DisplayFamily_DisplayModel = 06_56H). The Intel® Xeon® processor D product family is based on the Broadwell microarchitecture and supports the MSR interfaces listed in Table 35-16, Table 35-24, Table 35-29, Table 35-31, and Table 35-32.

Table 35-32. Additional MSRs Supported by Intel® Xeon® Processor D with DisplayFamily_DisplayModel 06_56H

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1ACH</td>
<td>MSR_TURBO_RATIO_LIMIT3</td>
<td>Package</td>
<td>Config Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RW if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>62:0</td>
<td>Package</td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

Semaphore for Turbo Ratio Limit Configuration
If 1, the processor uses override configuration specified in MSR_TURBO_RATIO_LIMIT, MSR_TURBO_RATIO_LIMIT1.
If 0, the processor uses factory-set configuration (Default).

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>286H 646</td>
<td>IA32_MC6_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>287H 647</td>
<td>IA32_MC7_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>289H 649</td>
<td>IA32_MC9_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>28AH 650</td>
<td>IA32_MC10_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>291H 657</td>
<td>IA32_MC17_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>292H 658</td>
<td>IA32_MC18_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>293H 659</td>
<td>IA32_MC19_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>418H 1048</td>
<td>MSR_MC6_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>419H 1049</td>
<td>MSR_MC6_STATUS</td>
<td>Package</td>
<td>Bank MC6 reports MC error from the integrated I/O module.</td>
</tr>
<tr>
<td>41AH 1050</td>
<td>MSR_MC6_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41BH 1051</td>
<td>MSR_MC6_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41CH 1052</td>
<td>MSR_MC7_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>41DH 1053</td>
<td>MSR_MC7_STATUS</td>
<td>Package</td>
<td>Bank MC7 reports MC error from the home agent HA 0.</td>
</tr>
<tr>
<td>41EH 1054</td>
<td>MSR_MC7_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41FH 1055</td>
<td>MSR_MC7_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>424H 1060</td>
<td>MSR_MC9_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>425H 1061</td>
<td>MSR_MC9_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 10 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>426H 1062</td>
<td>MSR_MC9_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>427H 1063</td>
<td>MSR_MC9_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>428H 1064</td>
<td>MSR_MC10_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>429H 1065</td>
<td>MSR_MC10_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 10 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>42AH 1066</td>
<td>MSR_MC10_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42BH 1067</td>
<td>MSR_MC10_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td>Bank MC17 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo0, CBo3, CBo6, CBo9, CBo12, CBo15.</td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>448H 1096</td>
<td>MSR_MC18_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MC1_CTL MSRs.” through Section 15.3.2.4, “IA32_MC1_MISC MSRs.”.</td>
</tr>
<tr>
<td>449H 1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
<td>Bank MC18 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo1, CBo4, CBo7, CBo10, CBo13, CBo16.</td>
</tr>
<tr>
<td>44AH 1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44BH 1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
<td></td>
</tr>
</tbody>
</table>
### 35.13.2 Additional MSRs Supported in the Next Generation Intel® Xeon® Processors

The MSRs listed in Table 35-32 are available to the next generation Intel® Xeon® Processor Family (CPUID DisplayFamily_DisplayModel = 06_4FH). The next generation Intel® Xeon® processor family is based on the Broadwell microarchitecture and supports the MSR interfaces listed in Table 35-16, Table 35-17, Table 35-24, Table 35-29, Table 35-31, and Table 35-33.

### Table 35-32. Additional MSRs Supported by Intel® Xeon® Processor D with DisplayFamily_DisplayModel 06_56H

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>44CH</td>
<td>1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>44DH</td>
<td>1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
</tr>
<tr>
<td>44EH</td>
<td>1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
</tr>
<tr>
<td>44FH</td>
<td>1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-24, Table 35-29, and Table 35-31 for other MSR definitions applicable to processors with CPUID signature 06_56H.

### Notes:
1. An override configuration lower than the factory-set configuration is always supported. An override configuration higher than the factory-set configuration is dependent on features specific to the processor and the platform.

### Table 35-33. Additional MSRs Supported by Intel® Xeon® Processors with DisplayFamily_DisplayModel 06_4FH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1ACH</td>
<td>428</td>
<td>MSR_TURBO_RATIO_LIMIT3</td>
<td>Package</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Config Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO.[28] = 0, Rw if MSR_PLATFORM_INFO.[28] = 1</td>
</tr>
<tr>
<td>285H</td>
<td>645</td>
<td>IA32_MC5_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>286H</td>
<td>646</td>
<td>IA32_MC6_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>287H</td>
<td>647</td>
<td>IA32_MC7_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>288H</td>
<td>648</td>
<td>IA32_MC8_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>289H</td>
<td>649</td>
<td>IA32_MC9_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28AH</td>
<td>650</td>
<td>IA32_MC10_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28BH</td>
<td>651</td>
<td>IA32_MC11_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28CH</td>
<td>652</td>
<td>IA32_MC12_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28DH</td>
<td>653</td>
<td>IA32_MC13_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28EH</td>
<td>654</td>
<td>IA32_MC14_CTL2</td>
<td>Package</td>
</tr>
<tr>
<td>28FH</td>
<td>655</td>
<td>IA32_MC15_CTL2</td>
<td>Package</td>
</tr>
</tbody>
</table>
Table 35-33. Additional MSRs Supported by Intel® Xeon® Processors with DisplayFamily_DisplayModel 06_4FH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>290H 656</td>
<td>IA32_MC16_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>291H 657</td>
<td>IA32_MC17_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>292H 658</td>
<td>IA32_MC18_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>293H 659</td>
<td>IA32_MC19_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>294H 660</td>
<td>IA32_MC20_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>295H 661</td>
<td>IA32_MC21_CTL2</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>414H 1044</td>
<td>MSR_MC5_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>415H 1045</td>
<td>MSR_MC5_STATUS</td>
<td>Package</td>
<td>Bank MC5 reports MC error from the Intel QPI 0 module.</td>
</tr>
<tr>
<td>416H 1046</td>
<td>MSR_MC5_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>417H 1047</td>
<td>MSR_MC5_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>418H 1048</td>
<td>MSR_MC6_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>419H 1049</td>
<td>MSR_MC6_STATUS</td>
<td>Package</td>
<td>Bank MC6 reports MC error from the integrated I/O module.</td>
</tr>
<tr>
<td>41AH 1050</td>
<td>MSR_MC6_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41BH 1051</td>
<td>MSR_MC6_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41CH 1052</td>
<td>MSR_MC7_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>41DH 1053</td>
<td>MSR_MC7_STATUS</td>
<td>Package</td>
<td>Bank MC7 reports MC error from the home agent HA 0.</td>
</tr>
<tr>
<td>41EH 1054</td>
<td>MSR_MC7_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>41FH 1055</td>
<td>MSR_MC7_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>420H 1056</td>
<td>MSR_MC8_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>421H 1057</td>
<td>MSR_MC8_STATUS</td>
<td>Package</td>
<td>Bank MC8 reports MC error from the home agent HA 1.</td>
</tr>
<tr>
<td>422H 1058</td>
<td>MSR_MC8_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>423H 1059</td>
<td>MSR_MC8_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>424H 1060</td>
<td>MSR_MC9_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>425H 1061</td>
<td>MSR_MC9_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>426H 1062</td>
<td>MSR_MC9_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>427H 1063</td>
<td>MSR_MC9_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>428H 1064</td>
<td>MSR_MC10_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>429H 1065</td>
<td>MSR_MC10_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>42AH 1066</td>
<td>MSR_MC10_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42BH 1067</td>
<td>MSR_MC10_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42CH 1068</td>
<td>MSR_MC11_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”.</td>
</tr>
<tr>
<td>42DH 1069</td>
<td>MSR_MC11_STATUS</td>
<td>Package</td>
<td>Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>42EH 1070</td>
<td>MSR_MC11_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>42FH 1071</td>
<td>MSR_MC11_MISC</td>
<td>Package</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-33. Additional MSRs Supported by Intel® Xeon® Processors with DisplayFamily_DisplayModel 06_4FH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>430H 1072</td>
<td>MSR_MC12_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>431H 1073</td>
<td>MSR_MC12_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>432H 1074</td>
<td>MSR_MC12_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>433H 1075</td>
<td>MSR_MC12_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>434H 1076</td>
<td>MSR_MC13_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>435H 1077</td>
<td>MSR_MC13_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>436H 1078</td>
<td>MSR_MC13_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>437H 1079</td>
<td>MSR_MC13_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>438H 1080</td>
<td>MSR_MC14_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>439H 1081</td>
<td>MSR_MC14_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43AH 1082</td>
<td>MSR_MC14_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43BH 1083</td>
<td>MSR_MC14_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43CH 1084</td>
<td>MSR_MC15_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>43DH 1085</td>
<td>MSR_MC15_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43EH 1086</td>
<td>MSR_MC15_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>43FH 1087</td>
<td>MSR_MC15_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>440H 1088</td>
<td>MSR_MC16_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Banks MC9 through MC 16 report MC error from each channel of the integrated memory controllers.</td>
</tr>
<tr>
<td>441H 1089</td>
<td>MSR_MC16_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>442H 1090</td>
<td>MSR_MC16_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>443H 1091</td>
<td>MSR_MC16_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>444H 1092</td>
<td>MSR_MC17_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Bank MC17 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo0, CBo3, CBo6, CBo9, CBo12, CBo15.</td>
</tr>
<tr>
<td>445H 1093</td>
<td>MSR_MC17_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>446H 1094</td>
<td>MSR_MC17_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>447H 1095</td>
<td>MSR_MC17_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>448H 1096</td>
<td>MSR_MC18_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Bank MC18 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo1, CBo4, CBo7, CBo10, CBo13, CBo16.</td>
</tr>
<tr>
<td>449H 1097</td>
<td>MSR_MC18_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44AH 1098</td>
<td>MSR_MC18_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44BH 1099</td>
<td>MSR_MC18_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44CH 1100</td>
<td>MSR_MC19_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Bank MC19 reports MC error from the following pair of CBo/L3 Slices (if the pair is present): CBo2, CBo5, CBo8, CBo11, CBo14, CBo17.</td>
</tr>
<tr>
<td>44DH 1101</td>
<td>MSR_MC19_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44EH 1102</td>
<td>MSR_MC19_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>44FH 1103</td>
<td>MSR_MC19_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>450H 1104</td>
<td>MSR_MC20_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.” through Section 15.3.2.4, “IA32_MCI_MISC MSRs.”. Bank MC20 reports MC error from the Intel QPI 1 module.</td>
</tr>
<tr>
<td>451H 1105</td>
<td>MSR_MC20_STATUS</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>452H 1106</td>
<td>MSR_MC20_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>453H 1107</td>
<td>MSR_MC20_MISC</td>
<td>Package</td>
<td></td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

35.14 MSRS IN THE 6TH GENERATION INTEL® CORE™ PROCE S SORS

The 6th generation Intel® Core™ processor family is based on the Skylake microarchitecture. They have CPUID DisplayFamily_DisplayModel signatures of 06_4EH and 06_5EH, supports the MSR interfaces listed in Table 35-16, Table 35-17, Table 35-20, Table 35-24, Table 35-30, and Table 35-34. For an MSR listed in Table 35-34 that also appears in the model-specific tables of prior generations, Table 35-34 supercede prior generation tables.

The notation of “Platform” in the Scope column (with respect to MSR_PLATFORM_ENERGY_COUNTER and MSR_PLATFORM_POWER_LIMIT) is limited to the power-delivery domain and the specifics of the power delivery integration may vary by platform vendor’s implementation.

NOTES:
1. An override configuration lower than the factory-set configuration is always supported. An override configuration higher than the factory-set configuration is dependent on features specific to the processor and the platform.

### Table 35-33. Additional MSRs Supported by Intel® Xeon® Processors with DisplayFamily_DisplayModel 06_4FH

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>454H 1108</td>
<td>MSR_MC21_CTL</td>
<td>Package</td>
<td>See Section 15.3.2.1, “IA32_MIC_CTL MSRs.” through Section 15.3.2.4, “IA32_MIC_MISC MSRs.”.</td>
</tr>
<tr>
<td>455H 1109</td>
<td>MSR_MC21_STATUS</td>
<td>Package</td>
<td>Bank MC21 reports MC error from the Intel QPI 2 module.</td>
</tr>
<tr>
<td>456H 1110</td>
<td>MSR_MC21_ADDR</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>457H 1111</td>
<td>MSR_MC21_MISC</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>630H 1584</td>
<td>MSR_PKG_C8_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>59:0</td>
<td>Package C8 Residency Counter. (R/O)</td>
<td></td>
<td>Value since last reset that this package is in processor-specific C8 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>63:60</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>631H 1585</td>
<td>MSR_PKG_C9_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>59:0</td>
<td>Package C9 Residency Counter. (R/O)</td>
<td></td>
<td>Value since last reset that this package is in processor-specific C9 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>63:60</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>632H 1586</td>
<td>MSR_PKG_C10_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>59:0</td>
<td>Package C10 Residency Counter. (R/O)</td>
<td></td>
<td>Value since last reset that this package is in processor-specific C10 states. Count at the same frequency as the TSC.</td>
</tr>
<tr>
<td>63:60</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C81H 3201</td>
<td>IA32_L3_QOS_CFG</td>
<td>Package</td>
<td>Cache Allocation Technology Configuration (R/W)</td>
</tr>
<tr>
<td>0</td>
<td>CAT Enable. Set 1 to enable Cache Allocation Technology</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:1</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

See Table 35-16, Table 35-17, Table 35-24, and Table 35-25 for other MSR definitions applicable to processors with CPUID signature 06_45H.
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex 58</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Thread</td>
<td>Control Features in Intel 64 Processor (R/W) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Lock (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 Enable VMX inside SMX operation (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 Enable VMX outside SMX operation (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>14:8 SENTER local functions enables (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>15 SENTER global functions enable (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>18 SGX global functions enable (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>20 LMCE_ON (R/WL)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63:21 Reserved.</td>
</tr>
<tr>
<td>254</td>
<td>IA32_MTRR_CAP</td>
<td>Thread</td>
<td>MTRR Capality (RO, Architectural). See Table 35-2</td>
</tr>
<tr>
<td>412</td>
<td>IA32_THERM_STATUS</td>
<td>Core</td>
<td>Thermal Monitor Status (R/W) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 Thermal status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 Thermal status log (R/WC0) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2 PROTCHOT # or FORCEPR# status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3 PROTCHOT # or FORCEPR# log (R/WC0) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4 Critical Temperature status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5 Critical Temperature status log (R/WC0) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>6 Thermal threshold #1 status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7 Thermal threshold #1 log (R/WC0) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>8 Thermal threshold #2 status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9 Thermal threshold #2 log (R/WC0) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10 Power Limitation status (RO) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11 Power Limitation log (R/WC0) See Table 35-2.</td>
</tr>
</tbody>
</table>
Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Current Limit status (RO)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>13</td>
<td>Current Limit log (R/WC0)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>14</td>
<td>Cross Domain Limit status (RO)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>15</td>
<td>Cross Domain Limit log (R/WC0)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26:23</td>
<td>Reserved.</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>30:27</td>
<td>Resolution in degrees Celsius (RO)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>31</td>
<td>Reading Valid (RO)</td>
<td>Package</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RO if MSR_PLATFORM_INFO[28] = 0,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RW if MSR_PLATFORM_INFO[28] = 1</td>
</tr>
<tr>
<td>7:0</td>
<td>Maximum Ratio Limit for 1C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 1 core active.</td>
</tr>
<tr>
<td>15:8</td>
<td>Maximum Ratio Limit for 2C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 2 core active.</td>
</tr>
<tr>
<td>23:16</td>
<td>Maximum Ratio Limit for 3C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 3 core active.</td>
</tr>
<tr>
<td>31:24</td>
<td>Maximum Ratio Limit for 4C</td>
<td>Package</td>
<td>Maximum turbo ratio limit of 4 core active.</td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>1C9H 457</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Thread</td>
<td>Last Branch Record Stack TOS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains an index (bits 0-4) that points to the MSR containing the most recent branch record.</td>
</tr>
<tr>
<td>300H 768</td>
<td>MSR_SGXOWNER0</td>
<td>Package</td>
<td>Lower 64 Bit OwnerEpoch Component of SGX Key (RO).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Low 64 bits of an 128-bit external entropy value for key derivation of an enclave.</td>
</tr>
<tr>
<td>301H 768</td>
<td>MSR_SGXOWNER1</td>
<td>Package</td>
<td>Upper 64 Bit OwnerEpoch Component of SGX Key (RO).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Upper 64 bits of an 128-bit external entropy value for key derivation of an enclave.</td>
</tr>
<tr>
<td>38EH 910</td>
<td>IA32_PERF_GLOBAL_STAUS</td>
<td>Package</td>
<td>See Table 35-2. See Section 18.2.2.3, “Full-Width Writes to Performance Counter Registers.”</td>
</tr>
</tbody>
</table>
Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Thread</td>
<td>Ovf_PMC0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Thread</td>
<td>Ovf_PMC1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Thread</td>
<td>Ovf_PMC2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Thread</td>
<td>Ovf_PMC3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Thread</td>
<td>Ovf_PMC4 (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Thread</td>
<td>Ovf_PMC5 (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Thread</td>
<td>Ovf_PMC6 (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Thread</td>
<td>Ovf_PMC7 (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td>Thread</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Ovf_FixedCtr0</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Ovf_FixedCtr1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Ovf_FixedCtr2</td>
<td></td>
</tr>
<tr>
<td>54:35</td>
<td>Thread</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Thread</td>
<td>Trace_ToPA_PMI.</td>
<td></td>
</tr>
<tr>
<td>57:56</td>
<td>Thread</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Thread</td>
<td>LBR_Frz.</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Thread</td>
<td>CTR_Frz.</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Thread</td>
<td>ASCL</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Thread</td>
<td>Ovf_Uncore</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Thread</td>
<td>Ovf_BufDSSAVE</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Thread</td>
<td>CondChgd</td>
<td></td>
</tr>
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</table>

390H 912 IA32_PERF_GLOBAL_STAT

US_RESET See Table 35-2. See Section 18.2.2.3, “Full-Width Writes to Performance Counter Registers.”

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC4 (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC5 (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC6 (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_PMC7 (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td>Thread</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_FixedCtr0</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_FixedCtr1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_FixedCtr2</td>
<td></td>
</tr>
<tr>
<td>54:35</td>
<td>Thread</td>
<td>Reserved.</td>
<td></td>
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</table>
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>55</td>
<td>Thread</td>
<td>Set 1 to clear Trace_ToPA_PMI.</td>
<td></td>
</tr>
<tr>
<td>57:56</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Thread</td>
<td>Set 1 to clear LBR_Frz.</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Thread</td>
<td>Set 1 to clear CTR_Frz.</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Thread</td>
<td>Set 1 to clear ASCI.</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_Uncore</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Thread</td>
<td>Set 1 to clear Ovf_BufDSSAVE</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Thread</td>
<td>Set 1 to clear CondChgd</td>
<td></td>
</tr>
<tr>
<td>IA32_PERF_GLOBAL_STAT_US_SET 391H 913</td>
<td>Thread</td>
<td>See Table 35-2. See Section 18.2.2.2.3, “Full-Width Writes to Performance Counter Registers.”</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC0 = 1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC1 = 1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC2 = 1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC3 = 1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC4 = 1 (if CPUID.0AH:EAX[15:8] &gt; 4)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC5 = 1 (if CPUID.0AH:EAX[15:8] &gt; 5)</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC6 = 1 (if CPUID.0AH:EAX[15:8] &gt; 6)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_PMC7 = 1 (if CPUID.0AH:EAX[15:8] &gt; 7)</td>
<td></td>
</tr>
<tr>
<td>31:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_FixedCtr0 = 1</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_FixedCtr1 = 1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_FixedCtr2 = 1</td>
<td></td>
</tr>
<tr>
<td>54:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>Thread</td>
<td>Set 1 to cause Trace_ToPA_PMI = 1</td>
<td></td>
</tr>
<tr>
<td>57:56</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Thread</td>
<td>Set 1 to cause LBR_Frz = 1</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>Thread</td>
<td>Set 1 to cause CTR_Frz = 1</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Thread</td>
<td>Set 1 to cause ASCI = 1</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_Uncore</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Thread</td>
<td>Set 1 to cause Ovf_BufDSSAVE</td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IA32_PERF_GLOBAL_INUSE 392H 913</td>
<td>Thread</td>
<td>See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>MSR_PEBS_FRONTEND 3F7H 1015</td>
<td>Thread</td>
<td>FrontEnd Precise Event Condition Select (R/W)</td>
<td></td>
</tr>
<tr>
<td>2:0</td>
<td>Event Code Select</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Event Code Select High</td>
<td></td>
<td></td>
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</table>
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tbody>
<tr>
<td><strong>Hex Dec</strong></td>
<td><strong>Register Name</strong></td>
<td><strong>Scope</strong></td>
<td><strong>Bit Description</strong></td>
</tr>
<tr>
<td>7:5</td>
<td>Reserved.</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>19:8</td>
<td>IDQ_Bubble_Length Specifier</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22:20</td>
<td>IDQ_Bubble_Width Specifier</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:23</td>
<td>Reserved.</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td><strong>500H 1280</strong></td>
<td>IA32_SGX_SVN_STATUS</td>
<td>Thread</td>
<td>Status and SVN Threshold of SGX Support for ACM (RO).</td>
</tr>
<tr>
<td>0</td>
<td>Lock. See Section 42.12.3, “Interactions with Authenticated Code Modules (ACMs)”</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15:1</td>
<td>Reserved.</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>SGX_SVN_SINIT. See Section 42.12.3, “Interactions with Authenticated Code Modules (ACMs)”</td>
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</tr>
<tr>
<td>63:24</td>
<td>Reserved.</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td><strong>560H 1376</strong></td>
<td>IA32_RTIT_OUTPUT_BASE</td>
<td>Thread</td>
<td>Trace Output Base Register (R/W). See Table 35-2.</td>
</tr>
<tr>
<td><strong>561H 1377</strong></td>
<td>IA32_RTIT_OUTPUT_MASK_PTRS</td>
<td>Thread</td>
<td>Trace Output Mask Pointers Register (R/W). See Table 35-2.</td>
</tr>
<tr>
<td><strong>570H 1392</strong></td>
<td>IA32_RTIT_CTL</td>
<td>Thread</td>
<td>Trace Control Register (R/W)</td>
</tr>
<tr>
<td>0</td>
<td>TraceEn</td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td>CYCEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>OS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>User</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6:4</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>CR3 filter</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>ToPA; writing 0 will #GP if also setting TraceEn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>MTCEn</td>
<td></td>
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</tr>
<tr>
<td>10</td>
<td>TSCEn</td>
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</tr>
<tr>
<td>11</td>
<td>DisRETC</td>
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<td></td>
</tr>
<tr>
<td>12</td>
<td>Reserved, MBZ</td>
<td></td>
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</tr>
<tr>
<td>13</td>
<td>BranchEn</td>
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<tr>
<td>17:14</td>
<td>MTCFreq</td>
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<td>18</td>
<td>Reserved, MBZ</td>
<td></td>
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<td>22:19</td>
<td>CYCThresh</td>
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<tr>
<td>23</td>
<td>Reserved, MBZ</td>
<td></td>
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</tr>
<tr>
<td>27:24</td>
<td>PSBFreq</td>
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<td>31:28</td>
<td>Reserved, MBZ</td>
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<td></td>
</tr>
<tr>
<td>35:32</td>
<td>ADDR0_CFG</td>
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<tr>
<td>39:36</td>
<td>ADDR1_CFG</td>
<td></td>
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</tr>
<tr>
<td>63:40</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>571H 1393</strong></td>
<td>IA32_RTIT_STATUS</td>
<td>Thread</td>
<td>Tracing Status Register (R/W)</td>
</tr>
</tbody>
</table>
Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>FilterEn, writes ignored.</td>
<td>Thread</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>ContextEn, writes ignored.</td>
<td>Thread</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>TriggerEn, writes ignored.</td>
<td>Thread</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Error (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Stopped</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:6</td>
<td>Reserved. MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>48:32</td>
<td>PacketByteCnt</td>
<td>Thread</td>
<td></td>
</tr>
<tr>
<td>63:49</td>
<td>Reserved, MBZ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>572H 1394</td>
<td>IA32_RTIT_CR3.Match</td>
<td>Thread</td>
<td>Trace Filter CR3 Match Register (R/W)</td>
</tr>
<tr>
<td>4:0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:5</td>
<td>CR3[63:5] value to match</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64DH 1613</td>
<td>MSR_PLATFORM_ENERGY_COUNTER</td>
<td>Platform*</td>
<td>Platform Energy Counter. (R/O).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This MSR is valid only if both platform vendor hardware implementation and BIOS enablement support it. This MSR will read 0 if not valid.</td>
</tr>
<tr>
<td>31:0</td>
<td>Total energy consumed by all devices in the platform that receive power from integrated power delivery mechanism, Included platform devices are processor cores, SOC, memory, add-on or peripheral devices that get powered directly from the platform power delivery means. The energy units are specified in the MSR_RAPL_POWER_UNIT.Energy_Status.Unit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:32</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>64EH 1614</td>
<td>MSR_PPERF</td>
<td>Thread</td>
<td>Productive Performance Count. (R/O).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Hardware's view of workload scalability. See Section 14.4.5.1</td>
</tr>
<tr>
<td>652H 1618</td>
<td>MSR_PKG_HDC_CONFIG</td>
<td>Package</td>
<td>HDC Configuration (R/W).</td>
</tr>
<tr>
<td>2:0</td>
<td>PKG_Cx_Monitor.</td>
<td>Core</td>
<td>Configures Package Cx state threshold for MSR_PKG_HDC.Deep_RESIDENCY</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:3</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>653H 1619</td>
<td>MSR_CORE_HDC.RESIDENCY</td>
<td>Core</td>
<td>Core HDC Idle Residency. (R/O).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Core_Cx_Duty_Cycle_Cnt.</td>
</tr>
<tr>
<td>655H 1621</td>
<td>MSR_PKG_HDC_SHALLOW.RESIDENCY</td>
<td>Package</td>
<td>Accumulate the cycles the package was in C2 state and at least one logical processor was in forced idle. (R/O).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Pkg_C2_Duty_Cycle_Cnt.</td>
</tr>
<tr>
<td>656H 1622</td>
<td>MSR_PKG_HDC.DEEP.RESIDENCY</td>
<td>Package</td>
<td>Package Cx HDC Idle Residency. (R/O).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Pkg_Cx_Duty_Cycle_Cnt.</td>
</tr>
</tbody>
</table>
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>658H 1624</td>
<td>MSR_WEIGHTED_CORE_C0</td>
<td>Package</td>
<td>Core-count Weighted C0 Residency. (R/O).</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Increment at the same rate as the TSC. The increment each cycle is weighted by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the number of processor cores in the package that reside in C0. If N cores are</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>simultaneously in C0, then each cycle the counter increments by N.</td>
</tr>
<tr>
<td>659H 1625</td>
<td>MSR_ANY_CORE_C0</td>
<td>Package</td>
<td>Any Core C0 Residency. (R/O)</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Increment at the same rate as the TSC. The increment each cycle is one if any</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>processor core in the package is in C0.</td>
</tr>
<tr>
<td>65AH 1626</td>
<td>MSR_ANY_GFXE_C0</td>
<td>Package</td>
<td>Any Graphics Engine C0 Residency. (R/O)</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Increment at the same rate as the TSC. The increment each cycle is one if any</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>processor graphic device's compute engines are in C0.</td>
</tr>
<tr>
<td>65BH 1627</td>
<td>MSR_CORE_GFXE_OVERLAP_C0</td>
<td>Package</td>
<td>Core and Graphics Engine Overlapped C0 Residency. (R/O)</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td>Increment at the same rate as the TSC. The increment each cycle is one if at</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>least one compute engine of the processor graphics is in C0 and at least one</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>processor core in the package is also in C0.</td>
</tr>
<tr>
<td>65CH 1628</td>
<td>MSR_PLATFORM_POWER_LIMIT</td>
<td>Platform*</td>
<td><strong>Platform Power Limit Control (R/W-L)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows platform BIOS to limit power consumption of the platform devices to the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>specified values. The Long Duration power consumption is specified via</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Platform_Power_Limit_1 and Platform_Power_Limit_1_Time. The Short Duration</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>power consumption limit is specified via the Platform_Power_Limit_2 with</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>duration chosen by the processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The processor implements an exponential-weighted algorithm in the placement of</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>the time windows.</td>
</tr>
<tr>
<td></td>
<td>14:0</td>
<td></td>
<td>Platform Power Limit #1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Average Power limit value which the platform must not exceed over a time window</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>as specified by Power_Limit_1_TIME field.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>The default value is the Thermal Design Power (TDP) and varies with product</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>skus. The unit is specified in MSR_RAPLPOWER_UNIT.</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td></td>
<td>Enable Platform Power Limit #1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, enables the processor to apply control policy such that the platform</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>power does not exceed Platform Power limit #1 over the time window specified by</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Power Limit #1 Time Window.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td></td>
<td>Platform Clamping Limitation #1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>When set, allows the processor to go below the OS requested P states in order</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>to maintain the power below specified Platform Power Limit #1 value.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This bit is writeable only when CPUID (EAX=6):EAX[4] is set.</td>
</tr>
</tbody>
</table>
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 23:17            |               | Time Window for Platform Power Limit #1. Specifies the duration of the time window over which Platform Power Limit 1 value should be maintained for sustained long duration. This field is made up of two numbers from the following equation:
|                  |               | Time Window = (float) \((1+(X/4))*(2^Y)\), where: X = POWER_LIMIT_1_TIME[23:22] Y = POWER_LIMIT_1_TIME[21:17]. The maximum allowed value in this field is defined in MSR_PKG_POWER_INFO[PKG_MAX_WIN]. The default value is ODH, The unit is specified in MSR_RAPLPOWER_UNIT[Time Unit]. |
| 31:24            |               | Reserved |
| 46:32            |               | Platform Power Limit #2. Average Power limit value which the platform must not exceed over the Short Duration time window chosen by the processor. The recommended default value is 1.25 times the Long Duration Power Limit (i.e. Platform Power Limit # 1) |
| 47               |               | Enable Platform Power Limit #2. When set, enables the processor to apply control policy such that the platform power does not exceed Platform Power limit #2 over the Short Duration time window. |
| 48               |               | Platform Clamping Limitation #2. When set, allows the processor to go below the OS requested P states in order to maintain the power below specified Platform Power Limit #2 value. |
| 62:49            |               | Reserved |
| 63               |               | Lock. Setting this bit will lock all other bits of this MSR until system RESET. |
| 690H 1680        | MSR_LASTBRANCH_16_FROM_IP | Thread | Last Branch Record 16 From IP (R/w) One of 32 triplets of last branch record registers on the last branch record stack. This part of the stack contains pointers to the source instruction. See also:
|                  |               |       | • Last Branch Record Stack TOS at 1C9H • Section 17.9 |
| 691H 1681        | MSR_LASTBRANCH_17_FROM_IP | Thread | Last Branch Record 17 From IP (R/w) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 692H 1682        | MSR_LASTBRANCH_18_FROM_IP | Thread | Last Branch Record 18 From IP (R/w) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 693H 1683        | MSR_LASTBRANCH_19_FROM_IP | Thread | Last Branch Record 19 From IP (R/w) See description of MSR_LASTBRANCH_0_FROM_IP. |
| 694H 1684        | MSR_LASTBRANCH_20_FROM_IP | Thread | Last Branch Record 20 From IP (R/w) See description of MSR_LASTBRANCH_0_FROM_IP. |
Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>695H 1685</td>
<td>MSR_LASTBRANCH_21_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 21 From IP (R/W)</td>
</tr>
<tr>
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<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>696H 1686</td>
<td>MSR_LASTBRANCH_22_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 22 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>697H 1687</td>
<td>MSR_LASTBRANCH_23_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 23 From IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>698H 1688</td>
<td>MSR_LASTBRANCH_24_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 24 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>699H 1689</td>
<td>MSR_LASTBRANCH_25_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 25 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69AH 1690</td>
<td>MSR_LASTBRANCH_26_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 26 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69BH 1691</td>
<td>MSR_LASTBRANCH_27_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 27 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69CH 1692</td>
<td>MSR_LASTBRANCH_28_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 28 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69DH 1693</td>
<td>MSR_LASTBRANCH_29_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 29 From IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69EH 1694</td>
<td>MSR_LASTBRANCH_30_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 30 From IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>69FH 1695</td>
<td>MSR_LASTBRANCH_31_FROM_IP</td>
<td>Thread</td>
<td>Last Branch Record 31 From IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0_FROM_IP.</td>
</tr>
<tr>
<td>6DOH 1744</td>
<td>MSR_LASTBRANCH_16_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 16 To IP (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of 32 triplets of last branch record registers on the last branch record stack. This part of the stack contains pointers to the destination instruction. See also:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Last Branch Record Stack TOS at 1C9H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Section 17.9</td>
</tr>
<tr>
<td>6D1H 1745</td>
<td>MSR_LASTBRANCH_17_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 17 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D2H 1746</td>
<td>MSR_LASTBRANCH_18_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 18 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D3H 1747</td>
<td>MSR_LASTBRANCH_19_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 19 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D4H 1748</td>
<td>MSR_LASTBRANCH_20_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 20 To IP (R/W)</td>
</tr>
<tr>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D5H 1749</td>
<td>MSR_LASTBRANCH_21_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 21 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
</tbody>
</table>
### Table 35-34. Additional MSRs Supported by 6th Generation Intel® Core™ Processors Based on Skylake Microarchitecture

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6D6H 1750</td>
<td>MSR_LASTBRANCH_22_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 22 To IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D7H 1751</td>
<td>MSR_LASTBRANCH_23_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 23 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D8H 1752</td>
<td>MSR_LASTBRANCH_24_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 24 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6D9H 1753</td>
<td>MSR_LASTBRANCH_25_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 25 To IP (R/W)</td>
</tr>
<tr>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DAH 1754</td>
<td>MSR_LASTBRANCH_26_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 26 To IP (R/W)</td>
</tr>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DBH 1755</td>
<td>MSR_LASTBRANCH_27_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 27 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DCH 1756</td>
<td>MSR_LASTBRANCH_28_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 28 To IP (R/W)</td>
</tr>
<tr>
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<td></td>
<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DDH 1757</td>
<td>MSR_LASTBRANCH_29_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 29 To IP (R/W)</td>
</tr>
<tr>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DEH 1758</td>
<td>MSR_LASTBRANCH_30_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 30 To IP (R/W)</td>
</tr>
<tr>
<td></td>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>6DFH 1759</td>
<td>MSR_LASTBRANCH_31_TO_IP</td>
<td>Thread</td>
<td>Last Branch Record 31 To IP (R/W)</td>
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<tr>
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<td>See description of MSR_LASTBRANCH_0_TO_IP.</td>
</tr>
<tr>
<td>770H 1904</td>
<td>IA32_PM_ENABLE</td>
<td>Package</td>
<td>See Section 14.4.2, “Enabling HWP”</td>
</tr>
<tr>
<td>771H 1905</td>
<td>IA32_HWP_CAPABILITIES</td>
<td>Thread</td>
<td>See Section 14.4.3, “HWP Performance Range and Dynamic Capabilities”</td>
</tr>
<tr>
<td>772H 1906</td>
<td>IA32_HWP_REQUEST_PKG</td>
<td>Package</td>
<td>See Section 14.4.4, “Managing HWP”</td>
</tr>
<tr>
<td>773H 1907</td>
<td>IA32_HWP_INTERRUPT</td>
<td>Thread</td>
<td>See Section 14.4.6, “HWP Notifications”</td>
</tr>
<tr>
<td>774H 1908</td>
<td>IA32_HWP_REQUEST</td>
<td>Thread</td>
<td>See Section 14.4.4, “Managing HWP”</td>
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<tr>
<td></td>
<td>7:0</td>
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<td>Minimum Performance (R/W).</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
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<td>Maximum Performance (R/W).</td>
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<tr>
<td></td>
<td>23:16</td>
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<td>Desired Performance (R/W).</td>
</tr>
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<td>31:24</td>
<td></td>
<td>Energy/Performance Preference (R/W).</td>
</tr>
<tr>
<td></td>
<td>41:32</td>
<td></td>
<td>Activity Window (R/W).</td>
</tr>
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<td></td>
<td>42</td>
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<td>Package Control (R/W).</td>
</tr>
<tr>
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<td>63:43</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>777H 1911</td>
<td>IA32_HWP_STATUS</td>
<td>Thread</td>
<td>See Section 14.4.5, “HWP Feedback”</td>
</tr>
<tr>
<td>DB0H 3504</td>
<td>IA32_PKG_HDC_CTL</td>
<td>Package</td>
<td>See Section 14.5.2, “Package level Enabling HDC”</td>
</tr>
<tr>
<td>DB1H 3505</td>
<td>IA32_PM_CTL1</td>
<td>Thread</td>
<td>See Section 14.5.3, “Logical-Processor Level HDC Control”</td>
</tr>
<tr>
<td>DB2H 3506</td>
<td>IA32_THREADSTALL</td>
<td>Thread</td>
<td>See Section 14.5.4.1, “IA32_THREADSTALL”</td>
</tr>
</tbody>
</table>
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<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCOH 3520</td>
<td>MSR_LBR_INFO_0</td>
<td>Thread</td>
<td>Last Branch Record 0 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of 32 triplet of last branch record registers on the last branch record stack. This part of the stack contains flag, TSX-related and elapsed cycle information. See also:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- Last Branch Record Stack TOS at 1C9H</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>- Section 17.6.1, “LBR Stack.”</td>
</tr>
<tr>
<td>DC1H 3521</td>
<td>MSR_LBR_INFO_1</td>
<td>Thread</td>
<td>Last Branch Record 1 Additional Information (R/w)</td>
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<tr>
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<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DC2H 3522</td>
<td>MSR_LBR_INFO_2</td>
<td>Thread</td>
<td>Last Branch Record 2 Additional Information (R/w)</td>
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<td>See description of MSR_LBR_INFO_0.</td>
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<tr>
<td>DC3H 3523</td>
<td>MSR_LBR_INFO_3</td>
<td>Thread</td>
<td>Last Branch Record 3 Additional Information (R/w)</td>
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<td>See description of MSR_LBR_INFO_0.</td>
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<tr>
<td>DC4H 3524</td>
<td>MSR_LBR_INFO_4</td>
<td>Thread</td>
<td>Last Branch Record 4 Additional Information (R/w)</td>
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<tr>
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<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DC5H 3525</td>
<td>MSR_LBR_INFO_5</td>
<td>Thread</td>
<td>Last Branch Record 5 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCGH 3526</td>
<td>MSR_LBR_INFO_6</td>
<td>Thread</td>
<td>Last Branch Record 6 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DC7H 3527</td>
<td>MSR_LBR_INFO_7</td>
<td>Thread</td>
<td>Last Branch Record 7 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DC8H 3528</td>
<td>MSR_LBR_INFO_8</td>
<td>Thread</td>
<td>Last Branch Record 8 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DC9H 3529</td>
<td>MSR_LBR_INFO_9</td>
<td>Thread</td>
<td>Last Branch Record 9 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCAH 3530</td>
<td>MSR_LBR_INFO_10</td>
<td>Thread</td>
<td>Last Branch Record 10 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCBH 3531</td>
<td>MSR_LBR_INFO_11</td>
<td>Thread</td>
<td>Last Branch Record 11 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCCH 3532</td>
<td>MSR_LBR_INFO_12</td>
<td>Thread</td>
<td>Last Branch Record 12 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCDH 3533</td>
<td>MSR_LBR_INFO_13</td>
<td>Thread</td>
<td>Last Branch Record 13 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCEH 3534</td>
<td>MSR_LBR_INFO_14</td>
<td>Thread</td>
<td>Last Branch Record 14 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DCFH 3535</td>
<td>MSR_LBR_INFO_15</td>
<td>Thread</td>
<td>Last Branch Record 15 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
<tr>
<td>DDOH 3536</td>
<td>MSR_LBR_INFO_16</td>
<td>Thread</td>
<td>Last Branch Record 16 Additional Information (R/w)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LBR_INFO_0.</td>
</tr>
</tbody>
</table>
The next generation Intel® Xeon Phi™ processor family, with CPUID DisplayFamily_DisplayModel signature 06_57H, supports the MSR interfaces listed in Table 35-35. These processors are based on the Knights Landing microarchitecture. Some MSRs are shared between a pair of processor cores, the scope is marked as module.
### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H</td>
<td>IA32_P5_MC_ADDR</td>
<td>Module</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H</td>
<td>IA32_P5_MC_TYPE</td>
<td>Module</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>6H</td>
<td>IA32_MONITOR_FILTER_SIZE</td>
<td>Thread</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination.” and Table 35-2</td>
</tr>
<tr>
<td>10H</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>Thread</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H</td>
<td>IA32_PLATFORM_ID</td>
<td>Package</td>
<td>Platform ID (R) See Table 35-2.</td>
</tr>
<tr>
<td>1BH</td>
<td>IA32_APIC_BASE</td>
<td>Thread</td>
<td>See Section 10.4.4, “Local APIC Status and Location,” and Table 35-2.</td>
</tr>
<tr>
<td>34H</td>
<td>MSR_SMI_COUNT</td>
<td>Thread</td>
<td>SMI Counter (R/O)</td>
</tr>
<tr>
<td></td>
<td>31:0</td>
<td></td>
<td>SMI Count (R/O)</td>
</tr>
<tr>
<td></td>
<td>63:32</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>3AH</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Thread</td>
<td>Control Features in Intel 64Processor (R/W) See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td>Lock (R/WL)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>Enable VMX outside SMX operation (R/WL)</td>
</tr>
<tr>
<td>3BH</td>
<td>IA32_TSC_ADJUST</td>
<td>THREAD</td>
<td>Per-Logical-Processor TSC ADJUST (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>79H</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>Core</td>
<td>BIOS Update Trigger Register (W) See Table 35-2.</td>
</tr>
<tr>
<td>8BH</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>THREAD</td>
<td>BIOS Update Signature ID (RO) See Table 35-2.</td>
</tr>
<tr>
<td>C1H</td>
<td>IA32_PMC0</td>
<td>THREAD</td>
<td>Performance counter register See Table 35-2.</td>
</tr>
<tr>
<td>C2H</td>
<td>IA32_PMC1</td>
<td>THREAD</td>
<td>Performance Counter Register See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>15:8</td>
<td>Package</td>
<td>Maximum Non-Turbo Ratio (R/O) The is the ratio of the frequency that invariant TSC runs at. Frequency = ratio * 100 MHz.</td>
</tr>
<tr>
<td></td>
<td>27:16</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>28</td>
<td>Package</td>
<td>Programmable Ratio Limit for Turbo Mode (R/O) When set to 1, indicates that Programmable Ratio Limits for Turbo mode is enabled, and when set to 0, indicates Programmable Ratio Limits for Turbo mode is disabled.</td>
</tr>
</tbody>
</table>
### MODEL-SPECIFIC REGISTERS (MSRS)

#### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>29</td>
<td>Package</td>
<td>Programmable TDP Limit for Turbo Mode (R/O) When set to 1, indicates that TDP Limits for Turbo mode are programmable, and when set to 0, indicates TDP Limit for Turbo mode is not programmable.</td>
<td></td>
</tr>
<tr>
<td>39:30</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>47:40</td>
<td>Package</td>
<td>Maximum Efficiency Ratio (R/O) The is the minimum ratio (maximum efficiency) that the processor can operates, in units of 100MHz.</td>
<td></td>
</tr>
<tr>
<td>63:48</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>E2H 226</td>
<td>MSR_PKG_CST_CONFIG_CONTROL</td>
<td>Module</td>
<td>C-State Configuration Control (R/W)</td>
</tr>
<tr>
<td>2:0</td>
<td>Package</td>
<td>Package C-State Limit (R/w) The following C-state code name encodings are supported: 000b: C0/C1 001b: C2 010b: C6 No Retention 011b: C6 Retention 111b: No limit</td>
<td></td>
</tr>
<tr>
<td>9:3</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>I/O MWait Redirection Enable (R/w)</td>
<td></td>
</tr>
<tr>
<td>14:11</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>CFG Lock (R/W/O)</td>
<td></td>
</tr>
<tr>
<td>63:16</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>E4H 228</td>
<td>MSR_PMG_IO_CAPTURE_BASE</td>
<td>Module</td>
<td>Power Management IO Redirection in C-state (R/W)</td>
</tr>
<tr>
<td>15:0</td>
<td>LVL_2 Base Address (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18:16</td>
<td></td>
<td>C-state Range (R/w) Specifies the encoding value of the maximum C-State code name to be included when IO read to MWait redirection is enabled by MSR_PKG_CST_CONFIG_CONTROL[bit10]: 100b - C4 is the max C-State to include 110b - C6 is the max C-State to include</td>
<td></td>
</tr>
<tr>
<td>63:19</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>E7H 231</td>
<td>IA32_MPERF</td>
<td>Thread</td>
<td>Maximum Performance Frequency Clock Count (RW) See Table 35-2.</td>
</tr>
<tr>
<td>E8H 232</td>
<td>IA32_APERF</td>
<td>Thread</td>
<td>Actual Performance Frequency Clock Count (RW) See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>Core</td>
<td>Memory Type Range Register (R) See Table 35-2.</td>
</tr>
</tbody>
</table>
Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with
DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>13CH</td>
<td>MSR_FEATURE_CONFIG</td>
<td>Core</td>
<td>AES Configuration (RW-L) Privileged post-BIOS agent must provide a #GP handler to handle unsuccessful read of this MSR.</td>
</tr>
</tbody>
</table>
| 1:0     |                         |           | AES Configuration (RW-L) Upon a successful read of this MSR, the configuration of AES instruction set availability is as follows:
|         |                         |           | 11b: AES instructions are not available until next RESET. otherwise, AES instructions are available. |
|         |                         |           | Note, AES instruction set is not available if read is unsuccessful. If the configuration is not 01b, AES instruction can be mis-configured if a privileged agent unintentionally writes 11b. |
| 63:2    |                         | Reserved. |                                                                                  |
| 174H    | IA32_SYSENTER_CS        | Thread    | See Table 35-2.                                                                 |
| 175H    | IA32_SYSENTER_ESP       | Thread    | See Table 35-2.                                                                 |
| 176H    | IA32_SYSENTER_EIP       | Thread    | See Table 35-2.                                                                 |
| 179H    | IA32_MCG_CAP            | Thread    | See Table 35-2.                                                                 |
| 17AH    | IA32_MCG_STATUS         | Thread    | See Table 35-2.                                                                 |
| 186H    | IA32_PERFEVTSEL0        | Thread    | Performance Monitoring Event Select Register (R/W) See Table 35-2.                 |
| 7:0     | Event Select            |           |                                                                                  |
| 15:8    | UMask                   |           |                                                                                  |
| 16      | USR                     |           |                                                                                  |
| 17      | OS                      |           |                                                                                  |
| 18      | Edge                    |           |                                                                                  |
| 19      | PC                      |           |                                                                                  |
| 20      | INT                     |           |                                                                                  |
| 21      | AnyThread               |           |                                                                                  |
| 22      | EN                      |           |                                                                                  |
| 23      | INV                     |           |                                                                                  |
| 31:24   | CMASK                   |           |                                                                                  |
| 63:32   | Reserved.               |           |                                                                                  |
| 187H    | IA32_PERFEVTSEL1        | Thread    | See Table 35-2.                                                                 |
| 198H    | IA32_PERF_STATUS        | Package   | See Table 35-2.                                                                 |
| 199H    | IA32_PERF_CTL           | Thread    | See Table 35-2.                                                                 |
| 19AH    | IA32_CLOCK_MODULATION   | Thread    | Clock Modulation (R/W) See Table 35-2.                                           |
| 19BH    | IA32_THERM_INTERRUPT    | Module    | Thermal Interrupt Control (R/W) See Table 35-2.                                   |
### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 19CH       | 412 | IA32_THERM_STATUS | Module    | Thermal Monitor Status (R/W)  
See Table 35-2.                                                                 |
| 22:16      |     | Digital Readout   | (RO)      |                                                                                 |
| 26:23      |     |                   |           |                                                                                 |
| 30:27      |     | Resolution in    |           |                                                                                 |
| 31         |     | degrees Celsius, | (RO)      |                                                                                 |
| 63:32      |     | Reading Valid     | (RO)      |                                                                                 |
| 1A0H       | 416 | IA32_MISC_ENABLE  | Thread    | Enable Misc. Processor Features (R/W)  
Allows a variety of processor functions to be enabled and disabled. |
| 0          |     | Fast-Strings      |           |                                                                                 |
| 2:1        |     | Reserved.         |           |                                                                                 |
| 3          |     | Automatic Thermal |           |                                                                                 |
| 6:4        |     | Control Circuit   |           |                                                                                 |
| 7          |     | Performance       |           |                                                                                 |
| 10:8       |     | Monitoring        |           |                                                                                 |
| 11         |     | Branch Trace      |           |                                                                                 |
| 12         |     | Precise Event     |           |                                                                                 |
| 15:13      |     | Maxval            |           |                                                                                 |
| 16         |     | Enhanced Intel    |           |                                                                                 |
| 18         |     | SpeedStep         |           |                                                                                 |
| 21:19      |     | Enable Monitor    |           |                                                                                 |
| 22         |     | Limit CPUID       |           |                                                                                 |
| 23         |     | xTPR Message      |           |                                                                                 |
| 33:24      |     | Reserved.         |           |                                                                                 |
### Model-Specific Registers (MSRs)

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>34</td>
<td>XD Bit Disable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>37:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Turbo Mode Disable (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:39</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A2H 418</td>
<td>MSR_TEMPERATURE_TARGET</td>
<td>Package</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:16</td>
<td>Temperature Target (R)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29:24</td>
<td>Target Offset (R/W)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:30</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A6H 422</td>
<td>MSR_OFFCORE_RSP_0</td>
<td>Shared</td>
<td>Offcore Response Event Select Register (R/W)</td>
</tr>
<tr>
<td>1A7H 423</td>
<td>MSR_OFFCORE_RSP_1</td>
<td>Shared</td>
<td>Offcore Response Event Select Register (R/W)</td>
</tr>
<tr>
<td>1ADH 429</td>
<td>MSR_TURBO_RATIO_LIMIT</td>
<td>Package</td>
<td>Maximum Ratio Limit of Turbo Mode for Groups of Cores (RW)</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7:1</td>
<td>Package</td>
<td></td>
<td>Maximum Number of Cores in Group 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Number active processor cores which operates under the maximum ratio limit for group 0.</td>
</tr>
<tr>
<td>15:8</td>
<td>Package</td>
<td></td>
<td>Maximum Ratio Limit for Group 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Maximum turbo ratio limit when the number of active cores are not more than the group 0 maximum core count.</td>
</tr>
<tr>
<td>20:16</td>
<td>Package</td>
<td></td>
<td>Number of Incremental Cores Added to Group 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Group 1, which includes the specified number of additional cores plus the cores in group 0, operates under the group 1 turbo max ratio limit = “group 0 Max ratio limit” - “group ratio delta for group 1”.</td>
</tr>
<tr>
<td>23:21</td>
<td>Package</td>
<td></td>
<td>Group Ratio Delta for Group 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit to Group 0.</td>
</tr>
<tr>
<td>28:24</td>
<td>Package</td>
<td></td>
<td>Number of Incremental Cores Added to Group 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Group 2, which includes the specified number of additional cores plus all the cores in group 1, operates under the group 2 turbo max ratio limit = “group 1 Max ratio limit” - “group ratio delta for group 2”.</td>
</tr>
<tr>
<td>31:29</td>
<td>Package</td>
<td></td>
<td>Group Ratio Delta for Group 2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit for Group 1.</td>
</tr>
<tr>
<td>36:32</td>
<td>Package</td>
<td></td>
<td>Number of Incremental Cores Added to Group 3</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Group 3, which includes the specified number of additional cores plus all the cores in group 2, operates under the group 3 turbo max ratio limit = “group 2 Max ratio limit” - “group ratio delta for group 3”.</td>
</tr>
</tbody>
</table>
### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>39:37</td>
<td>Group Ratio Delta for Group 3</td>
<td>Package</td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit for Group 2.</td>
</tr>
<tr>
<td>44:40</td>
<td>Number of Incremental Cores Added to Group 4</td>
<td>Package</td>
<td>Group 4, which includes the specified number of additional cores plus all the cores in group 3, operates under the group 4 turbo max ratio limit = “group 3 Max ratio limit” - “group ratio delta for group 4”.</td>
</tr>
<tr>
<td>47:45</td>
<td>Group Ratio Delta for Group 4</td>
<td>Package</td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit for Group 3.</td>
</tr>
<tr>
<td>52:48</td>
<td>Number of Incremental Cores Added to Group 5</td>
<td>Package</td>
<td>Group 5, which includes the specified number of additional cores plus all the cores in group 4, operates under the group 5 turbo max ratio limit = “group 4 Max ratio limit” - “group ratio delta for group 5”.</td>
</tr>
<tr>
<td>55:53</td>
<td>Group Ratio Delta for Group 5</td>
<td>Package</td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit for Group 4.</td>
</tr>
<tr>
<td>60:56</td>
<td>Number of Incremental Cores Added to Group 6</td>
<td>Package</td>
<td>Group 6, which includes the specified number of additional cores plus all the cores in group 5, operates under the group 6 turbo max ratio limit = “group 5 Max ratio limit” - “group ratio delta for group 6”.</td>
</tr>
<tr>
<td>63:61</td>
<td>Group Ratio Delta for Group 6</td>
<td>Package</td>
<td>An unsigned integer specifying the ratio decrement relative to the Max ratio limit for Group 5.</td>
</tr>
<tr>
<td>1B0H</td>
<td>IA32_ENERGY_PERF_BIAS</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<td>1B1H</td>
<td>IA32_PACKAGE_THERM_STATUS</td>
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<td>IA32_PACKAGE_THERM_INTERRUPT</td>
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<td>MSR_LBR_SELECT</td>
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<td>Last Branch Record Filtering Select Register (R/W)</td>
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<td>1C9H</td>
<td>MSR_LASTBRANCH_TOS</td>
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<td>Last Branch Record Stack TOS (R/W)</td>
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<td>IA32_DEBUGCTL</td>
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<td>Debug Control (R/W)</td>
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<td>1DDH</td>
<td>MSR_LER_FROM_LIP</td>
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<td>Last Exception Record From Linear IP (R)</td>
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<td>1DEH</td>
<td>MSR_LER_TO_LIP</td>
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<td>Last Exception Record To Linear IP (R)</td>
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<td>IA32_SMRR_PHYSBASE</td>
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<td>IA32_SMRR_PHYSMASK</td>
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### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

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<tr>
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<th>Scope</th>
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<td>202H</td>
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<td>IA32_MTRR_FIX16K_80000</td>
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<td>Default Memory Types (R/W)</td>
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<td>Fixed-Function Performance Counter Register 0 (R/W)</td>
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<td>Fixed-Function Performance Counter Register 2 (R/W)</td>
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<td>345H</td>
<td>IA32_PERF_CAPABILITIES</td>
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<td>See Table 35-2. See Section 17.4.1, “IA32_DEBUGCTL MSR.”</td>
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<td>380H</td>
<td>IA32_FIXED_CTR_CTRL</td>
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<td>Fixed-Function-Counter Control Register (R/W)</td>
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Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

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<th>Address</th>
<th>Register Name</th>
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<td>38EH</td>
<td>IA32_PERF_GLOBAL_STATUS</td>
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<td>IA32_PERF_GLOBAL_CTRL</td>
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<td>390H</td>
<td>IA32_PERF_GLOBAL_OVF_CTRL</td>
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<td>3F1H</td>
<td>MSR_PEBS_ENABLE</td>
<td>Thread</td>
<td>See Table 35-2.</td>
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<tr>
<td>3F8H</td>
<td>MSR_PKG_C3_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
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<tr>
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<td>63:0 Package C3 Residency Counter. (R/O)</td>
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<tr>
<td>3F9H</td>
<td>MSR_PKG_C6_RESIDENCY</td>
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<td>63:0 Package C6 Residency Counter. (R/O)</td>
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<tr>
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<td>MSR_PKG_C7_RESIDENCY</td>
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<td>63:0 Package C7 Residency Counter. (R/O)</td>
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<tr>
<td>3FCH</td>
<td>MSR_MC0_RESIDENCY</td>
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<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
</tr>
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<td>63:0 Module C0 Residency Counter. (R/O)</td>
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<td>3FDH</td>
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<td>63:0 Module C6 Residency Counter. (R/O)</td>
</tr>
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<td>3FFH</td>
<td>MSR_CORE_C6_RESIDENCY</td>
<td>Core</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to Mwait extension C-state parameters or ACPI C-States.</td>
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<td>63:0 CORE C6 Residency Counter. (R/O)</td>
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<tr>
<td>400H</td>
<td>IA32_MC0_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
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<tr>
<td>401H</td>
<td>IA32_MC0_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
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<td>402H</td>
<td>IA32_MC0_ADDR</td>
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<td>404H</td>
<td>IA32_MC1_CTL</td>
<td>Core</td>
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<tr>
<td>408H</td>
<td>IA32_MC2_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
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<tr>
<td>409H</td>
<td>IA32_MC2_STATUS</td>
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<td>IA32_MC2_ADDR</td>
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<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
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<tr>
<td>40CH</td>
<td>MSR_MC3_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
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<td>40DH</td>
<td>MSR_MC3_STATUS</td>
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<td>40EH</td>
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<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”</td>
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<tr>
<td>410H</td>
<td>MSR_MC4_CTL</td>
<td>Core</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
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<td>411H</td>
<td>MSR_MC4_STATUS</td>
<td>Core</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
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</table>
| 412H    | MSR_MC4_ADDR | Core | See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”

The MSR_MC4_ADDR register is either not implemented or contains no address if the ADDRv flag in the MSR_MC4_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.
Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
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<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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</thead>
<tbody>
<tr>
<td>414H</td>
<td>MSR_MC5_CTL</td>
<td>Package</td>
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<td>MSR_MC5_ADDR</td>
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<td>See Section 15.3.2.3, “IA32_MC_ADDR MSRs.”</td>
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<td>IA32_VMX_BASIC</td>
<td>Core</td>
<td>Reporting Register of Basic VMX Capabilities (R/O)</td>
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<td>481H</td>
<td>IA32_VMX_PINBASED_CTL</td>
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<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O)</td>
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<td>482H</td>
<td>IA32_VMX_PROCBASED_CTL</td>
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<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O)</td>
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<td>Capability Reporting Register of VM-exit Controls (R/O)</td>
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<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O)</td>
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<tr>
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<td>IA32_VMX_CR0_FIXED1</td>
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<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O)</td>
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<td>IA32_VMX_VMCS_ENUM</td>
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<td>IA32_VMX_EPT_VPID_ENUM</td>
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<td>Capability Reporting Register of EPT and VPID (R/O)</td>
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<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
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<tr>
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<td>IA32_VMX_FMFUNC</td>
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<td>Capability Reporting Register of VM-function Controls (R/O)</td>
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<td>IA32_A_PMC1</td>
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<td>600H</td>
<td>IA32_DS_AREA</td>
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<td>DS Save Area (R/W)</td>
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<td>MSR_RAPL_POWER_UNIT</td>
<td>Package</td>
<td>Unit Multipliers used in RAPL Interfaces (R/O)</td>
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<td>Power Units</td>
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<td>Reserved</td>
</tr>
<tr>
<td>12:8</td>
<td></td>
<td>Package</td>
<td>Energy Status Units</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Energy related information (in Joules) is based on the multiplier, 1/2^ESU, where ESU is an unsigned integer represented by bits 12:8. Default value is 0EH (or 61 micro-joules)</td>
</tr>
<tr>
<td>15:13</td>
<td></td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td>19:16</td>
<td></td>
<td>Package</td>
<td>Time Units</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.1, “RAPL Interfaces.”</td>
</tr>
<tr>
<td>63:20</td>
<td></td>
<td>Package</td>
<td>Reserved</td>
</tr>
<tr>
<td>60DH</td>
<td>MSR_PKG_C2_RESIDENCY</td>
<td>Package</td>
<td>Note: C-state values are processor specific C-state code names, unrelated to MWAIT extension C-state parameters or ACPI C-States.</td>
</tr>
<tr>
<td>610H</td>
<td>MSR_PKG_POWER_LIMIT</td>
<td>Package</td>
<td>PKG RAPL Power Limit Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>611H</td>
<td>MSR_PKG_ENERGY_STATUS</td>
<td>Package</td>
<td>PKG Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>613H</td>
<td>MSR_PKG_PERF_STATUS</td>
<td>Package</td>
<td>PKG Perf Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>614H</td>
<td>MSR_PKG_POWER_INFO</td>
<td>Package</td>
<td>PKG RAPL Parameters (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.3, “Package RAPL Domain.”</td>
</tr>
<tr>
<td>618H</td>
<td>MSR_DRAM_POWER_LIMIT</td>
<td>Package</td>
<td>DRAM RAPL Power Limit Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>619H</td>
<td>MSR_DRAM_ENERGY_STATUS</td>
<td>Package</td>
<td>DRAM Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>618H</td>
<td>MSR_DRAM_PERF_STATUS</td>
<td>Package</td>
<td>DRAM Performance Throttling Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
<tr>
<td>61CH</td>
<td>MSR_DRAM_POWER_INFO</td>
<td>Package</td>
<td>DRAM RAPL Parameters (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.5, “DRAM RAPL Domain.”</td>
</tr>
</tbody>
</table>
### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>638H</td>
<td>MSR_PP0_POWER_LIMIT</td>
<td>Package</td>
<td>PPO RAPL Power Limit Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PPO/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>639H</td>
<td>MSR_PP0_ENERGY_STATUS</td>
<td>Package</td>
<td>PPO Energy Status (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Section 14.9.4, “PPO/PP1 RAPL Domains.”</td>
</tr>
<tr>
<td>648H</td>
<td>MSR_CONFIG_TDP_NOMINAL</td>
<td>Package</td>
<td>Base TDP Ratio (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-20</td>
</tr>
<tr>
<td>649H</td>
<td>MSR_CONFIG_TDP_LEVEL1</td>
<td>Package</td>
<td>ConfigTDP Level 1 ratio and power level (R/O). See Table 35-20</td>
</tr>
<tr>
<td>64AH</td>
<td>MSR_CONFIG_TDP_LEVEL2</td>
<td>Package</td>
<td>ConfigTDP Level 2 ratio and power level (R/O). See Table 35-20</td>
</tr>
<tr>
<td>64BH</td>
<td>MSR_CONFIG_TDP_CONTROL</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-20</td>
</tr>
<tr>
<td>64CH</td>
<td>MSR_TURBO_ACTIVATION_RATIO</td>
<td>Package</td>
<td>ConfigTDP Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-20</td>
</tr>
<tr>
<td>690H</td>
<td>MSR_CORE_PERF_LIMIT_REASONS</td>
<td>Package</td>
<td>Indicator of Frequency Clipping in Processor Cores (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(frequency refers to processor core frequency)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>Package</td>
<td>PROCHOT Status (R0)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Package</td>
<td>Thermal Status (R0)</td>
</tr>
<tr>
<td></td>
<td>5:2</td>
<td>Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>Package</td>
<td>VR Therm Alert Status (R0)</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>Package</td>
<td>Electrical Design Point Status (R0)</td>
</tr>
<tr>
<td></td>
<td>63:9</td>
<td>Package</td>
<td>Reserved.</td>
</tr>
<tr>
<td>6E0H</td>
<td>IA32_TSC_DEADLINE</td>
<td>Core</td>
<td>TSC Target of Local APIC’s TSC Deadline Mode (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2</td>
</tr>
<tr>
<td>802H</td>
<td>IA32_X2APIC_APCID</td>
<td>Thread</td>
<td>x2APIC ID register (R/O)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See x2APIC Specification.</td>
</tr>
<tr>
<td>803H</td>
<td>IA32_X2APIC_VERSION</td>
<td>Thread</td>
<td>x2APIC Version register (R/O)</td>
</tr>
<tr>
<td>808H</td>
<td>IA32_X2APIC_TPR</td>
<td>Thread</td>
<td>x2APIC Task Priority register (R/W)</td>
</tr>
<tr>
<td>80AH</td>
<td>IA32_X2APIC_PPR</td>
<td>Thread</td>
<td>x2APIC Processor Priority register (R/O)</td>
</tr>
<tr>
<td>80BH</td>
<td>IA32_X2APIC_EOI</td>
<td>Thread</td>
<td>x2APIC EOI register (W/O)</td>
</tr>
<tr>
<td>800H</td>
<td>IA32_X2APIC_LDR</td>
<td>Thread</td>
<td>x2APIC Logical Destination register (R/O)</td>
</tr>
<tr>
<td>80FH</td>
<td>IA32_X2APIC_SIVR</td>
<td>Thread</td>
<td>x2APIC Spurious Interrupt Vector register (R/W)</td>
</tr>
<tr>
<td>810H</td>
<td>IA32_X2APIC_ISR0</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [31:0] (R/O)</td>
</tr>
<tr>
<td>811H</td>
<td>IA32_X2APIC_ISR1</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>812H</td>
<td>IA32_X2APIC_ISR2</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [35:64] (R/O)</td>
</tr>
<tr>
<td>813H</td>
<td>IA32_X2APIC_ISR3</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [127:96] (R/O)</td>
</tr>
<tr>
<td>814H</td>
<td>IA32_X2APIC_ISR4</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>815H</td>
<td>IA32_X2APIC_ISR5</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>816H</td>
<td>IA32_X2APIC_ISR6</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>817H</td>
<td>IA32_X2APIC_ISR7</td>
<td>Thread</td>
<td>x2APIC In-Service register bits [255:224] (R/O)</td>
</tr>
</tbody>
</table>
### Table 35-35. Selected MSRs Supported by Next Generation Intel® Xeon Phi™ Processors with DisplayFamily_DisplayModel Signature 06_57H

<table>
<thead>
<tr>
<th>Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>818H 2072</td>
<td>IA32_X2APIC_TMR0</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [31:0] (R/O)</td>
</tr>
<tr>
<td>819H 2073</td>
<td>IA32_X2APIC_TMR1</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>81AH 2074</td>
<td>IA32_X2APIC_TMR2</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [95:64] (R/O)</td>
</tr>
<tr>
<td>81BH 2075</td>
<td>IA32_X2APIC_TMR3</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [127:96] (R/O)</td>
</tr>
<tr>
<td>81CH 2076</td>
<td>IA32_X2APIC_TMR4</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>81DH 2077</td>
<td>IA32_X2APIC_TMR5</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>81EH 2078</td>
<td>IA32_X2APIC_TMR6</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>81FH 2079</td>
<td>IA32_X2APIC_TMR7</td>
<td>Thread</td>
<td>x2APIC Trigger Mode register bits [255:224] (R/O)</td>
</tr>
<tr>
<td>820H 2080</td>
<td>IA32_X2APIC_IRR0</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [31:0] (R/O)</td>
</tr>
<tr>
<td>821H 2081</td>
<td>IA32_X2APIC_IRR1</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [63:32] (R/O)</td>
</tr>
<tr>
<td>822H 2082</td>
<td>IA32_X2APIC_IRR2</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [95:64] (R/O)</td>
</tr>
<tr>
<td>823H 2083</td>
<td>IA32_X2APIC_IRR3</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [127:96] (R/O)</td>
</tr>
<tr>
<td>824H 2084</td>
<td>IA32_X2APIC_IRR4</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [159:128] (R/O)</td>
</tr>
<tr>
<td>825H 2085</td>
<td>IA32_X2APIC_IRR5</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [191:160] (R/O)</td>
</tr>
<tr>
<td>826H 2086</td>
<td>IA32_X2APIC_IRR6</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [223:192] (R/O)</td>
</tr>
<tr>
<td>827H 2087</td>
<td>IA32_X2APIC_IRR7</td>
<td>Thread</td>
<td>x2APIC Interrupt Request register bits [255:224] (R/O)</td>
</tr>
<tr>
<td>828H 2088</td>
<td>IA32_X2APIC_ESR</td>
<td>Thread</td>
<td>x2APIC Error Status register (R/W)</td>
</tr>
<tr>
<td>82FH 2095</td>
<td>IA32_X2APIC_LVT_CMCI</td>
<td>Thread</td>
<td>x2APIC LVT Corrected Machine Check Interrupt register (R/w)</td>
</tr>
<tr>
<td>830H 2096</td>
<td>IA32_X2APIC_ICR</td>
<td>Thread</td>
<td>x2APIC Interrupt Command register (R/w)</td>
</tr>
<tr>
<td>832H 2098</td>
<td>IA32_X2APIC_LVT_TIMER</td>
<td>Thread</td>
<td>x2APIC LVT Timer Interrupt register (R/W)</td>
</tr>
<tr>
<td>833H 2099</td>
<td>IA32_X2APIC_LVT_THERMAL</td>
<td>Thread</td>
<td>x2APIC LVT Thermal Sensor Interrupt register (R/W)</td>
</tr>
<tr>
<td>834H 2100</td>
<td>IA32_X2APIC_LVT_PMI</td>
<td>Thread</td>
<td>x2APIC LVT Performance Monitor register (R/W)</td>
</tr>
<tr>
<td>835H 2101</td>
<td>IA32_X2APIC_LVT_LINT0</td>
<td>Thread</td>
<td>x2APIC LVT LINT0 register (R/W)</td>
</tr>
<tr>
<td>836H 2102</td>
<td>IA32_X2APIC_LVT_LINT1</td>
<td>Thread</td>
<td>x2APIC LVT LINT1 register (R/W)</td>
</tr>
<tr>
<td>837H 2103</td>
<td>IA32_X2APIC_LVT_ERROR</td>
<td>Thread</td>
<td>x2APIC LVT Error register (R/W)</td>
</tr>
<tr>
<td>838H 2104</td>
<td>IA32_X2APIC_INIT_COUNT</td>
<td>Thread</td>
<td>x2APIC Initial Count register (R/W)</td>
</tr>
<tr>
<td>839H 2105</td>
<td>IA32_X2APIC_CUR_COUNT</td>
<td>Thread</td>
<td>x2APIC Current Count register (R/O)</td>
</tr>
<tr>
<td>83EH 2110</td>
<td>IA32_X2APIC_DIV_CONF</td>
<td>Thread</td>
<td>x2APIC Divide Configuration register (R/W)</td>
</tr>
<tr>
<td>83FH 2111</td>
<td>IA32_X2APIC_SELF_IPI</td>
<td>Thread</td>
<td>x2APIC Self IPI register (w/O)</td>
</tr>
<tr>
<td>C000_0080H</td>
<td>IA32_EFER</td>
<td>Thread</td>
<td>Extended Feature Enables</td>
</tr>
<tr>
<td>C000_0081H</td>
<td>IA32_STAR</td>
<td>Thread</td>
<td>System Call Target Address (R/w)</td>
</tr>
<tr>
<td>C000_0082H</td>
<td>IA32_LSTAR</td>
<td>Thread</td>
<td>IA-32e Mode System Call Target Address (R/w)</td>
</tr>
<tr>
<td>C000_0084H</td>
<td>IA32_FMASK</td>
<td>Thread</td>
<td>System Call Flag Mask (R/W)</td>
</tr>
</tbody>
</table>

See Table 35-2.
MODEL-SPECIFIC REGISTERS (MSRS)

35.16 MSRS IN THE PENTIUM® 4 AND INTEL® XEON® PROCESSORS

Table 35-36 lists MSRs (architectural and model-specific) that are defined across processor generations based on Intel NetBurst microarchitecture. The processor can be identified by its CPUID signatures of DisplayFamily encoding of 0FH, see Table 35-1.

- MSRs with an “IA32_” prefix are designated as “architectural.” This means that the functions of these MSRs and their addresses remain the same for succeeding families of IA-32 processors.
- MSRs with an “MSR_” prefix are model specific with respect to address functionalities. The column “Model Availability” lists the model encoding value(s) within the Pentium 4 and Intel Xeon processor family at the specified register address. The model encoding value of a processor can be queried using CPUID. See “CPUID—CPU Identification” in Chapter 3 of the Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 2A.

### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Scope</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C000_0100H</td>
<td>IA32_FS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of FS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0101H</td>
<td>IA32_GS_BASE</td>
<td>Thread</td>
<td>Map of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0102H</td>
<td>IA32_KERNEL_GSBASE</td>
<td>Thread</td>
<td>Swap Target of BASE Address of GS (R/W) See Table 35-2.</td>
</tr>
<tr>
<td>C000_0103H</td>
<td>IA32_TSC_AUX</td>
<td>Thread</td>
<td>AUXILIARY TSC Signature. (R/W) See Table 35-2.</td>
</tr>
</tbody>
</table>

35.16 MSRS IN THE PENTIUM® 4 AND INTEL® XEON® PROCESSORS

Table 35-36 lists MSRs (architectural and model-specific) that are defined across processor generations based on Intel NetBurst microarchitecture. The processor can be identified by its CPUID signatures of DisplayFamily encoding of 0FH, see Table 35-1.

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### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td>Fields and Flags</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0H</td>
<td>0</td>
<td>IA32_P5_MC_ADDR</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
</tr>
<tr>
<td>1H</td>
<td>1</td>
<td>IA32_P5_MC_TYPE</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
</tr>
<tr>
<td>6H</td>
<td>6</td>
<td>IA32_MONITOR_FILTER_LINE_SIZE</td>
<td>3, 4, 6</td>
<td>Shared</td>
</tr>
<tr>
<td>10H</td>
<td>16</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17H</td>
<td>23</td>
<td>IA32_PLATFORM_ID</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On earlier processors, only the lower 32 bits are writable. On any write to the lower 32 bits, the upper 32 bits are cleared. For processor family 0FH, models 3 and 4: all 64 bits are writable.

The operating system can use this MSR to determine “slot” information for the processor and the proper microcode update to load.
<table>
<thead>
<tr>
<th>Hex</th>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/ Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1BH</td>
<td>IA32_APIC_BASE</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td></td>
<td>APIC Location and Status (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2. See Section 10.4.4, “Local APIC Status and Location.”</td>
</tr>
<tr>
<td>2AH</td>
<td>MSR_EBC_HARD_POWERON</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>Processor Hard Power-On Configuration (R/W) Enables and disables processor features; (R) indicates current processor configuration.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output Tri-state Enabled (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates whether tri-state output is enabled (1) or disabled (0) as set by the strapping of SMI#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Execute BIST (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates whether the execution of the BIST is enabled (1) or disabled (0) as set by the strapping of INIT#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>In Order Queue Depth (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates whether the in order queue depth for the system bus is 1 (1) or up to 12 (0) as set by the strapping of A7#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>MCERR# Observation Disabled (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates whether MCERR# observation is enabled (0) or disabled (1) as determined by the strapping of A9#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BINIT# Observation Enabled (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Indicates whether BINIT# observation is enabled (0) or disabled (1) as determined by the strapping of A10#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>6:5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>APIC Cluster ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains the logical APIC cluster ID value as set by the strapping of A12# and A11#. The logical cluster ID value is written into the field on the deassertion of RESET#; the field is set to 1 when the address bus signal is asserted.</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex  Dec</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Bus Park Disable (R)</td>
<td></td>
<td></td>
<td>Indicates whether bus park is enabled (0) or disabled (1) as set by the strapping of A15#. The value in this bit is written on the deassertion of RESET#; the bit is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>11:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13:12</td>
<td>Agent ID (R)</td>
<td></td>
<td></td>
<td>Contains the logical agent ID value as set by the strapping of BR[3:0]. The logical ID value is written into the field on the deassertion of RESET#; the field is set to 1 when the address bus signal is asserted.</td>
</tr>
<tr>
<td>63:14</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2BH 43</td>
<td>MSR_EBC_SOFT_POWERON</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Processor Soft Power-On Configuration (R/W) Enables and disables processor features.</td>
</tr>
<tr>
<td>0</td>
<td>RCNT/SCNT On Request Encoding Enable (R/W)</td>
<td></td>
<td></td>
<td>Controls the driving of RCNT/SCNT on the request encoding. Set to enable (1); clear to disabled (0, default).</td>
</tr>
<tr>
<td>1</td>
<td>Data Error Checking Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable system data bus parity checking; clear to enable parity checking.</td>
</tr>
<tr>
<td>2</td>
<td>Response Error Checking Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable (default); clear to enable.</td>
</tr>
<tr>
<td>3</td>
<td>Address/Request Error Checking Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable (default); clear to enable.</td>
</tr>
<tr>
<td>4</td>
<td>Initiator MCERR# Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable MCERR# driving for initiator bus requests (default); clear to enable.</td>
</tr>
<tr>
<td>5</td>
<td>Internal MCERR# Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable MCERR# driving for initiator internal errors (default); clear to enable.</td>
</tr>
<tr>
<td>6</td>
<td>BINIT# Driver Disable (R/W)</td>
<td></td>
<td></td>
<td>Set to disable BINIT# driver (default); clear to enable driver.</td>
</tr>
<tr>
<td>63:7</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique&lt;sup&gt;1&lt;/sup&gt;</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2CH 44</td>
<td>MSR_EBC_FREQUENCY_ID</td>
<td>2,3, 4, 6</td>
<td>Shared</td>
<td>Processor Frequency Configuration&lt;br&gt;The bit field layout of this MSR varies according to the MODEL value in the CPUID version information. The following bit field layout applies to Pentium 4 and Xeon Processors with MODEL encoding equal or greater than 2.&lt;br&gt;(R) The field indicates the current processor frequency configuration.</td>
</tr>
<tr>
<td>15:0</td>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>18:16</td>
<td>Scalable Bus Speed (R/W)</td>
<td></td>
<td></td>
<td>Scalable Bus Speed&lt;br&gt;Indicates the intended scalable bus speed:&lt;br&gt;Encoding Scalable Bus Speed&lt;br&gt;000B 100 MHz (Model 2)&lt;br&gt;000B 266 MHz (Model 3 or 4)&lt;br&gt;001B 133 MHz&lt;br&gt;010B 200 MHz&lt;br&gt;011B 166 MHz&lt;br&gt;100B 333 MHz (Model 6)&lt;br&gt;133.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 001B.&lt;br&gt;166.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 011B.</td>
</tr>
<tr>
<td>23:19</td>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>31:24</td>
<td>Core Clock Frequency to System Bus Frequency Ratio (R)</td>
<td></td>
<td></td>
<td>Core Clock Frequency to System Bus Frequency Ratio (R)&lt;br&gt;The processor core clock frequency to system bus frequency ratio observed at the de-assertion of the reset pin.</td>
</tr>
<tr>
<td>63:25</td>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>2CH 44</td>
<td>MSR_EBC_FREQUENCY_ID</td>
<td>0, 1</td>
<td>Shared</td>
<td>Processor Frequency Configuration (R)&lt;br&gt;The bit field layout of this MSR varies according to the MODEL value of the CPUID version information. This bit field layout applies to Pentium 4 and Xeon Processors with MODEL encoding less than 2.&lt;br&gt;Indicates current processor frequency configuration.</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>20:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23:21</td>
<td>Scalable Bus Speed (R/W)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Indicates the intended scalable bus speed:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Encoding Scalable Bus Speed</td>
<td>000B 100 MHz</td>
<td>All others values reserved.</td>
<td></td>
</tr>
<tr>
<td>63:24</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3AH 58</td>
<td>IA32_FEATURE_CONTROL</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Control Features in IA-32 Processor (R/W)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>(If CPUID.01H:ECX.[bit 5])</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>79H 121</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>BIOS Update Trigger Register (W)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8BH 139</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>BIOS Update Signature ID (R/w)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>9BH 155</td>
<td>IA32_SMM_MONITOR_CTL</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>SMM Monitor Configuration (R/W)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>FEH 254</td>
<td>IA32_MTRRCAP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>MTRR Information</td>
</tr>
<tr>
<td></td>
<td>See Section 11.11.1, “MTRR Feature Identification.”</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>174H 372</td>
<td>IA32_SYSENTER_CS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>CS register target for CPL 0 code (R/W)</td>
</tr>
<tr>
<td></td>
<td>See Section 35-2</td>
<td></td>
<td></td>
<td>See Section 35-2.</td>
</tr>
<tr>
<td></td>
<td>See Section 5.8.7, “Performing Fast Calls to System Procedures with the SYSENTER and SYSEXIT Instructions.”</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>175H 373</td>
<td>IA32_SYSENTER_ESP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Stack pointer for CPL 0 stack (R/W)</td>
</tr>
<tr>
<td></td>
<td>See Section 35-2</td>
<td></td>
<td></td>
<td>See Section 35-2.</td>
</tr>
<tr>
<td></td>
<td>See Section 5.8.7, “Performing Fast Calls to System Procedures with the SYSENTER and SYSEXIT Instructions.”</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>176H 374</td>
<td>IA32_SYSENTER_EIP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>CPL 0 code entry point (R/W)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td></td>
<td>See Section 5.8.7, “Performing Fast Calls to System Procedures with the SYSENTER and SYSEXIT Instructions.”</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>179H 377</td>
<td>IA32_MCG_CAP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check Capabilities (R)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Section 15.3.1.1, “IA32_MCG_CAP MSR.”</td>
</tr>
<tr>
<td>17AH 378</td>
<td>IA32_MCG_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check Status. (R)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Section 15.3.1.2, “IA32_MCG_STATUS MSR.”</td>
</tr>
<tr>
<td>17BH 379</td>
<td>IA32_MCG_CTL</td>
<td></td>
<td></td>
<td>Machine Check Feature Enable (R/w)</td>
</tr>
<tr>
<td></td>
<td>See Table 35-2</td>
<td></td>
<td></td>
<td>See Section 15.3.1.3, “IA32_MCG_CTL MSR.”</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>180H 384</td>
<td>MSR_MCG_RAX</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EAX/RAX Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>181H 385</td>
<td>MSR_MCG_RBX</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EBX/RBX Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>182H 386</td>
<td>MSR_MCG_RCX</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check ECX/RCX Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>183H 387</td>
<td>MSR_MCG_RDX</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EDX/RDX Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>184H 388</td>
<td>MSR_MCG_RSI</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check ESI/RSI Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>185H 389</td>
<td>MSR_MCG_RDI</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EDI/RDI Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>186H 390</td>
<td>MSR_MCG_RBP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EBP/RBP Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>187H 391</td>
<td>MSR_MCG_RSP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check ESP/RSP Save State</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>188H 392</td>
<td>MSR_MCG_RFLAGS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EFLAGS/RFLAGS Save State</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>189H 393</td>
<td>MSR_MCG_RIP</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check EIP/RIP Save State</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td></td>
<td>Contains register state at time of machine check error. When in non-64-bit modes at the time of the error, bits 63-32 do not contain valid data.</td>
</tr>
<tr>
<td>18AH 394</td>
<td>MSR_MCG_MISC</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check Miscellaneous</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td>DS</td>
</tr>
<tr>
<td></td>
<td>63:1</td>
<td></td>
<td></td>
<td>When set, the bit indicates that a page assist or page fault occurred during DS normal operation. The processors response is to shut down. The bit is used as an aid for debugging DS handling code. It is the responsibility of the user (BIOS or operating system) to clear this bit for normal operation.</td>
</tr>
<tr>
<td>18BH-18FH</td>
<td>MSR_MCG_RESERVED1 - MSR_MCG_RESERVED5</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Reserved.</td>
</tr>
<tr>
<td>190H 400</td>
<td>MSR_MCG_R8</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check R8</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td></td>
<td>Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.</td>
</tr>
<tr>
<td>191H 401</td>
<td>MSR_MCG_R9</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Machine Check R9D/R9</td>
</tr>
<tr>
<td></td>
<td>63:0</td>
<td></td>
<td></td>
<td>Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 192H | 402 | MSR_MCG_R10 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R10
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”

Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.

| 193H | 403 | MSR_MCG_R11 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R11
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”

Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.

| 194H | 404 | MSR_MCG_R12 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R12
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”

Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.

| 195H | 405 | MSR_MCG_R13 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R13
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”

Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.

| 196H | 406 | MSR_MCG_R14 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R14
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”

Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.

| 197H | 407 | MSR_MCG_R15 | 0, 1, 2, 3, 4, 6 | Unique | Machine Check R15
See Section 15.3.2.6, “IA32_MCG Extended Machine Check State MSRs.”
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td>Fields and Flags</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:0</td>
<td></td>
<td></td>
<td></td>
<td>Registers R8-15 (and the associated state-save MSRs) exist only in Intel 64 processors. These registers contain valid information only when the processor is operating in 64-bit mode at the time of the error.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Thermal Monitor Control (R/W) See Table 35-2. See Section 14.7.3, “Software Controlled Clock Modulation.”</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>Thermal Interrupt Control (R/W) See Section 14.7.2, “Thermal Monitor,” and see Table 35-2.</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Thermal Monitor Status (R/W) See Section 14.7.2, “Thermal Monitor,” and see Table 35-2.</td>
</tr>
<tr>
<td>19DH 413</td>
<td>MSR_THERM2_CTL</td>
<td></td>
<td>Shared</td>
<td>Thermal Monitor 2 Control. For Family F, Model 3 processors: When read, specifies the value of the target TM2 transition last written. When set, it sets the next target value for TM2 transition. For Family F, Model 4 and Model 6 processors: When read, specifies the value of the target TM2 transition last written. Writes may cause #GP exceptions.</td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Enable Miscellaneous Processor Features (R/W) Fast-Strings Enable. See Table 35-2. Reserved. x87 FPU Fopcode Compatibility Mode Enable Thermal Monitor 1 Enable See Section 14.7.2, “Thermal Monitor,” and see Table 35-2. Split-Lock Disable When set, the bit causes an #AC exception to be issued instead of a split-lock cycle. Operating systems that set this bit must align system structures to avoid split-lock scenarios. When the bit is clear (default), normal split-locks are issued to the bus.</td>
</tr>
</tbody>
</table>
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
<td>This debug feature is specific to the Pentium 4 processor.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>6</td>
<td>Third-Level Cache Disable (R/w)</td>
<td></td>
<td></td>
<td>When set, the third-level cache is disabled; when clear (default) the third-level cache is enabled. This flag is reserved for processors that do not have a third-level cache. Note that the bit controls only the third-level cache; and only if overall caching is enabled through the CD flag of control register CR0, the page-level cache controls, and/or the MTRRs. See Section 11.5.4, &quot;Disabling and Enabling the L3 Cache.&quot;</td>
</tr>
<tr>
<td>7</td>
<td>Performance Monitoring Available (R)</td>
<td>See Table 35-2.</td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8</td>
<td>Suppress Lock Enable</td>
<td></td>
<td></td>
<td>When set, assertion of LOCK on the bus is suppressed during a Split Lock access. When clear (default), LOCK is not suppressed.</td>
</tr>
<tr>
<td>9</td>
<td>Prefetch Queue Disable</td>
<td></td>
<td></td>
<td>When set, disables the prefetch queue. When clear (default), enables the prefetch queue.</td>
</tr>
<tr>
<td>10</td>
<td>FERR# Interrupt Reporting Enable (R/w)</td>
<td></td>
<td></td>
<td>When set, interrupt reporting through the FERR# pin is enabled; when clear, this interrupt reporting function is disabled. When this flag is set and the processor is in the stop-clock state (STPCLK# is asserted), asserting the FERR# pin signals to the processor that an interrupt (such as, INIT#, BINIT#, INTR, NMI, SMI#, or RESET#) is pending and that the processor should return to normal operation to handle the interrupt. This flag does not affect the normal operation of the FERR# pin (to indicate an unmasked floating-point error) when the STPCLK# pin is not asserted.</td>
</tr>
<tr>
<td>11</td>
<td>Branch Trace Storage Unavailable (BTS_UNAVILABLE) (R)</td>
<td>See Table 35-2.</td>
<td></td>
<td>When set, the processor does not support branch trace storage (BTS); when clear, BTS is supported.</td>
</tr>
</tbody>
</table>
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name Fields and Flags</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>PEBS_UNAVILABLE: Precise Event Based Sampling Unavailable (R)</td>
<td>See Table 35-2.</td>
<td>When set, the processor does not support precise event-based sampling (PEBS); when clear, PEBS is supported.</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>TM2 Enable (R/w)</td>
<td>When this bit is set (1) and the thermal sensor indicates that the die temperature is at the predetermined threshold, the Thermal Monitor 2 mechanism is engaged. TM2 will reduce the bus to core ratio and voltage according to the value last written to MSR_THERM2_CTL bits 15:0. When this bit is clear (0, default), the processor does not change the VID signals or the bus to core ratio when the processor enters a thermal managed state. If the TM2 feature flag (ECX[8]) is not set to 1 after executing CPUID with EAX = 1, then this feature is not supported and BIOS must not alter the contents of this bit location. The processor is operating out of spec if both this bit and the TM1 bit are set to disabled states.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:14</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>ENABLE MONITOR FSM (R/w)</td>
<td>See Table 35-2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Adjacent Cache Line Prefetch Disable (R/w)</td>
<td>When set to 1, the processor fetches the cache line of the 128-byte sector containing currently required data. When set to 0, the processor fetches both cache lines in the sector. Single processor platforms should not set this bit. Server platforms should set or clear this bit based on platform performance observed in validation and testing. BIOS may contain a setup option that controls the setting of this bit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:20</td>
<td>Reserved.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>Limit CPUID MAXVAL (R/w)</td>
<td>See Table 35-2. Setting this can cause unexpected behavior to software that depends on the availability of CPUID leaves greater than 3.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>xTPR Message Disable (R/w)</td>
<td>See Table 35-2.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**L1 Data Cache Context Mode (R/W)**
When set, the L1 data cache is placed in shared mode; when clear (default), the cache is placed in adaptive mode. This bit is only enabled for IA-32 processors that support Intel Hyper-Threading Technology. See Section 11.5.6, “L1 Data Cache Context Mode.”
When L1 is running in adaptive mode and CR3s are identical, data in L1 is shared across logical processors. Otherwise, L1 is not shared and cache use is competitive.
If the Context ID feature flag (ECX[10]) is set to 0 after executing CPUID with EAX = 1, the ability to switch modes is not supported. BIOS must not alter the contents of IA32_MISC_ENABLE[24].

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Available/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td></td>
<td></td>
<td>L1 Data Cache Context Mode (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(When set, the L1 data cache is placed in shared mode; when clear, the cache is placed in adaptive mode. This bit is only enabled for IA-32 processors that support Intel Hyper-Threading Technology. See Section 11.5.6, “L1 Data Cache Context Mode.”)</td>
</tr>
<tr>
<td>33:25</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
<td>Unique</td>
<td>XD Bit Disable (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(See Table 35-2.)</td>
<td></td>
</tr>
<tr>
<td>63:35</td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
</tbody>
</table>

**MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)**

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1A1H 417</td>
<td>MSR_PLATFORM_BRV</td>
<td>3, 4, 6</td>
<td>Shared</td>
<td>Platform Feature Requirements (R)</td>
</tr>
<tr>
<td>17:0</td>
<td></td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td></td>
<td>PLATFORM Requirements</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(When set to 1, indicates the processor has specific platform requirements. The details of the platform requirements are listed in the respective data sheets of the processor.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>63:19</td>
<td></td>
<td></td>
<td>Reserved.</td>
<td></td>
</tr>
</tbody>
</table>

| 1D7H 471         | MSR_LER_FROM_LIP | 0, 1, 2, 3, 4, 6   | Unique | Last Exception Record From Linear IP (R) |
| 31:0             |               |                    | From Linear IP |
|                  |               | (Linear address of the last branch instruction.) | Std  |
| 63:32            |               |                    | Reserved. |                  |

| 1D7H 471         | 63:0           | Unique             | From Linear IP |
|                  |               | (Linear address of the last branch instruction (if IA-32e mode is active).) |

| 1D8H 472         | MSR_LER_TO_LIP | 0, 1, 2, 3, 4, 6   | Unique | Last Exception Record To Linear IP (R) |
|                  |               |                    | From Linear IP |
|                  |               | (Linear address of the last branch instruction.) |

See Section 17.10.3, “Last Exception Records.”
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors  (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
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<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 1D8H 472         | 63:0                           | Unique             |               | From Linear IP  
Linear address of the target of the last branch instruction. |
|                  | 63:32                          |                    |               | Reserved.      |
| 1D9H 473         | MSR_DEBUGCTLA                  | 0, 1, 2, 3, 4, 6   | Unique        | Debug Control (R/w) 
Controls how several debug features are used. Bit definitions are discussed in the referenced section. See Section 17.10.1, “MSR_DEBUGCTLA MSR.” |
| 1DAH 474         | MSR_LASTBRANCH_TOS             | 0, 1, 2, 3, 4, 6   | Unique        | Last Branch Record Stack TOS (R/W) 
Contains an index (0-3 or 0-15) that points to the top of the last branch record stack (that is, that points the index of the MSR containing the most recent branch record). See Section 17.10.2, “LBR Stack for Processors Based on Intel NetBurst® Microarchitecture”; and addresses 1DBH-1DEH and 680H-68FH. |
| 1DBH 475         | MSR_LASTBRANCH_0               | 0, 1, 2            | Unique        | Last Branch Record 0 (R/W) 
One of four last branch record registers on the last branch record stack. It contains pointers to the source and destination instruction for one of the last four branches, exceptions, or interrupts that the processor took. MSR_LASTBRANCH_0 through MSR_LASTBRANCH_3 at 1DBH-1DEH are available only on family 0FH, models 0H-02H. They have been replaced by the MSRs at 680H-68FH and 6C0H-6CFH. See Section 17.9, “Last Branch, Call Stack, Interrupt, and Exception Recording for Processors based on Skylake Microarchitecture.” |
| 1DDH 477         | MSR_LASTBRANCH_2               | 0, 1, 2            | Unique        | Last Branch Record 2 
See description of the MSR_LASTBRANCH_0 MSR at 1DBH. |
| 1DEH 478         | MSR_LASTBRANCH_3               | 0, 1, 2            | Unique        | Last Branch Record 3 
See description of the MSR_LASTBRANCH_0 MSR at 1DBH. |
| 200H 512         | IA32_MTRR_PHYSBASE0             | 0, 1, 2, 3, 4, 6   | Shared        | Variable Range Base MTRR 
See Section 11.11.2.3, “Variable Range MTRRs.” |
| 201H 513         | IA32_MTRR_PHYSMASK0            | 0, 1, 2, 3, 4, 6   | Shared        | Variable Range Mask MTRR 
See Section 11.11.2.3, “Variable Range MTRRs.” |
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

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</tr>
</thead>
<tbody>
<tr>
<td>202H 514</td>
<td>IA32_MTRR_PHYSBASE1</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>203H 515</td>
<td>IA32_MTRR_PHYSMASK1</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>204H 516</td>
<td>IA32_MTRR_PHYSBASE2</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>205H 517</td>
<td>IA32_MTRR_PHYSMASK2</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>206H 518</td>
<td>IA32_MTRR_PHYSBASE3</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>207H 519</td>
<td>IA32_MTRR_PHYSMASK3</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>208H 520</td>
<td>IA32_MTRR_PHYSBASE4</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>209H 521</td>
<td>IA32_MTRR_PHYSMASK4</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20AH 522</td>
<td>IA32_MTRR_PHYSBASE5</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20BH 523</td>
<td>IA32_MTRR_PHYSMASK5</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20CH 524</td>
<td>IA32_MTRR_PHYSBASE6</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20DH 525</td>
<td>IA32_MTRR_PHYSMASK6</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20EH 526</td>
<td>IA32_MTRR_PHYSBASE7</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>20FH 527</td>
<td>IA32_MTRR_PHYSMASK7</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Variable Range Mask MTRR See Section 11.11.2.3, “Variable Range MTRRs.”</td>
</tr>
<tr>
<td>250H 592</td>
<td>IA32_MTRR_FIX64K_00000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR See Section 11.11.2.2, “Fixed Range MTRRs.”</td>
</tr>
<tr>
<td>258H 600</td>
<td>IA32_MTRR_FIX16K_80000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR See Section 11.11.2.2, “Fixed Range MTRRs.”</td>
</tr>
<tr>
<td>259H 601</td>
<td>IA32_MTRR_FIX16K_A0000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR See Section 11.11.2.2, “Fixed Range MTRRs.”</td>
</tr>
<tr>
<td>268H 616</td>
<td>IA32_MTRR_FIX4K_C0000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR See Section 11.11.2.2, “Fixed Range MTRRs.”</td>
</tr>
<tr>
<td>269H 617</td>
<td>IA32_MTRR_FIX4K_C8000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR See Section 11.11.2.2, “Fixed Range MTRRs.”</td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Fields and Flags</td>
<td>Model Availability</td>
<td>Shared/Unique</td>
</tr>
<tr>
<td>-----------------</td>
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<td>------------------</td>
<td>-------------------</td>
<td>--------------</td>
</tr>
<tr>
<td>26AH 618</td>
<td>IA32_MTRR_FIX4K_D0000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR</td>
</tr>
<tr>
<td>26BH 619</td>
<td>IA32_MTRR_FIX4K_D8000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR</td>
</tr>
<tr>
<td>26CH 620</td>
<td>IA32_MTRR_FIX4K_E0000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Fixed Range MTRR</td>
</tr>
<tr>
<td>26DH 621</td>
<td>IA32_MTRR_FIX4K_E8000</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
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### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

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### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

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<tr>
<td>3CAH 970</td>
<td>MSR_ALF_ESCR0 0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
<td></td>
</tr>
</tbody>
</table>
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B7H 3CBH 971</td>
<td>MSR_ALF_ESCR1</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>CCH 3CCH 972</td>
<td>MSR_CRU_ESCR2</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>CDD 3CDH 973</td>
<td>MSR_CRU_ESCR3</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>E0H 3E0H 992</td>
<td>MSR_CRU_ESCR4</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>E1H 3E1H 993</td>
<td>MSR_CRU_ESCR5</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>08H 3F0H 1008</td>
<td>MSR_TC_PRECISE_EVENT</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 18.12.1, “ESCR MSRs.”</td>
</tr>
<tr>
<td>09H 3F1H 1009</td>
<td>MSR_PEBS_ENABLE</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>Precise Event-Based Sampling (PEBS) (R/W) Controls the enabling of precise event sampling and replay tagging.</td>
</tr>
<tr>
<td>FFH 3F2H 1010</td>
<td>MSR_PEBS_MATRIX_VERT</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Table 19-26.</td>
</tr>
<tr>
<td>100H 400H</td>
<td>IA32_MCI_CTL</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCI_CTL MSRs.”</td>
</tr>
<tr>
<td>101H 401H</td>
<td>IA32_MCI_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCI_STATUS MSRs.”</td>
</tr>
</tbody>
</table>
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

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<th>Register Name</th>
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<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>403H 1027</td>
<td>IA32_MC0_MISC</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.” The IA32_MC0_MISC MSR is either not implemented or does not contain additional information if the MISCV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>406H 1030</td>
<td>IA32_MC1_ADDR</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC1_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC1_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>407H 1031</td>
<td>IA32_MC1_MISC</td>
<td></td>
<td>Shared</td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.” The IA32_MC1_MISC MSR is either not implemented or does not contain additional information if the MISCV flag in the IA32_MC1_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRS.”</td>
</tr>
<tr>
<td>40AH 1034</td>
<td>IA32_MC2_ADDR</td>
<td>0, 1, 2, 3, 4, 6</td>
<td></td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
</tbody>
</table>
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

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<tr>
<th>Register Address</th>
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<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>408H 1035</td>
<td>IA32_MC2_MISC</td>
<td></td>
<td></td>
<td></td>
<td>See Section 15.3.2.4, “IA32_MC2_MISC MSRs.” The IA32_MC2_MISC MSR is either not implemented or does not contain additional information if the MISCV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>40CH 1036</td>
<td>IA32_MC3_CTL</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>40DH 1037</td>
<td>IA32_MC3_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.”</td>
</tr>
<tr>
<td>40EH 1038</td>
<td>IA32_MC3_ADDR</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>40FH 1039</td>
<td>IA32_MC3_MISC</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.” The IA32_MC3_MISC MSR is either not implemented or does not contain additional information if the MISCV flag in the IA32_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>410H 1040</td>
<td>IA32_MC4_CTL</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.1, “IA32_MCi_CTL MSRs.”</td>
</tr>
<tr>
<td>411H 1041</td>
<td>IA32_MC4_STATUS</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Shared</td>
<td></td>
<td>See Section 15.3.2.2, “IA32_MCi_STATUS MSRs.”</td>
</tr>
<tr>
<td>412H 1042</td>
<td>IA32_MC4_ADDR</td>
<td></td>
<td></td>
<td></td>
<td>See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.” The IA32_MC4_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC4_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>413H 1043</td>
<td>IA32_MC4_MISC</td>
<td></td>
<td></td>
<td></td>
<td>See Section 15.3.2.4, “IA32_MCi_MISC MSRs.” The IA32_MC4_MISC MSR is either not implemented or does not contain additional information if the MISCV flag in the IA32_MC4_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
</tbody>
</table>
### Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
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<tr>
<th>Register Address</th>
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<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| 480H 1152        | IA32_VMX_BASIC                  | 3, 4, 6            | Unique        | Reporting Register of Basic VMX Capabilities (R/O)  
|                  |                                 |                    |               | See Table 35-2.  
|                  |                                 |                    |               | See Appendix A.1, “Basic VMX Information.” |
| 481H 1153        | IA32_VMX_PINBASED_CTLs          | 3, 4, 6            | Unique        | Capability Reporting Register of Pin-based  
|                  |                                 |                    |               | VM-execution Controls (R/O)  
|                  |                                 |                    |               | See Table 35-2.  
|                  |                                 |                    |               | See Appendix A.3, “VM-Execution Controls.” |
| 482H 1154        | IA32_VMX_PROCBASED_CTLs         | 3, 4, 6            | Unique        | Capability Reporting Register of Primary  
|                  |                                 |                    |               | Processor-based VM-execution Controls (R/O)  
|                  |                                 |                    |               | See Appendix A.3, “VM-Execution Controls,” and  
|                  |                                 |                    |               | see Table 35-2. |
| 483H 1155        | IA32_VMX_EXIT_CTLs              | 3, 4, 6            | Unique        | Capability Reporting Register of VM-exit  
|                  |                                 |                    |               | Controls (R/O)  
|                  |                                 |                    |               | See Appendix A.4, “VM-Exit Controls,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 484H 1156        | IA32_VMX_ENTRY_CTLs             | 3, 4, 6            | Unique        | Capability Reporting Register of VM-entry  
|                  |                                 |                    |               | Controls (R/O)  
|                  |                                 |                    |               | See Appendix A.5, “VM-Entry Controls,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 485H 1157        | IA32_VMX_MISC                   | 3, 4, 6            | Unique        | Reporting Register of Miscellaneous VMX  
|                  |                                 |                    |               | Capabilities (R/O)  
|                  |                                 |                    |               | See Appendix A.6, “Miscellaneous Data,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 486H 1158        | IA32_VMX_CRO_FIXED0             | 3, 4, 6            | Unique        | Capability Reporting Register of CR0 Bits Fixed  
|                  |                                 |                    |               | to 0 (R/O)  
|                  |                                 |                    |               | See Appendix A.7, “VMX-Fixed Bits in CR0,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 487H 1159        | IA32_VMX_CRO_FIXED1             | 3, 4, 6            | Unique        | Capability Reporting Register of CR0 Bits Fixed  
|                  |                                 |                    |               | to 1 (R/O)  
|                  |                                 |                    |               | See Appendix A.7, “VMX-Fixed Bits in CR0,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 488H 1160        | IA32_VMX_CR4_FIXED0             | 3, 4, 6            | Unique        | Capability Reporting Register of CR4 Bits Fixed  
|                  |                                 |                    |               | to 0 (R/O)  
|                  |                                 |                    |               | See Appendix A.8, “VMX-Fixed Bits in CR4,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 489H 1161        | IA32_VMX_CR4_FIXED1             | 3, 4, 6            | Unique        | Capability Reporting Register of CR4 Bits Fixed  
|                  |                                 |                    |               | to 1 (R/O)  
|                  |                                 |                    |               | See Appendix A.8, “VMX-Fixed Bits in CR4,” and see  
|                  |                                 |                    |               | Table 35-2. |
| 48AH 1162        | IA32_VMX_VMCS_ENUM              | 3, 4, 6            | Unique        | Capability Reporting Register of VMCS Field  
|                  |                                 |                    |               | Enumeration (R/O)  
|                  |                                 |                    |               | See Appendix A.9, “VMCS Enumeration,” and see  
<p>|                  |                                 |                    |               | Table 35-2. |</p>
<table>
<thead>
<tr>
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<th>Register Name</th>
<th>Model Availability</th>
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<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>48BH 1163</td>
<td>IA32_VMX_PROCBASED_CTL2</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Capability Reporting Register of Secondary Processor-based VM-execution Controls (R/O) See Appendix A.3, “VM-Execution Controls,” and see Table 35-2.</td>
</tr>
<tr>
<td>600H 1536</td>
<td>IA32_DS_AREA</td>
<td>0, 1, 2, 3, 4, 6</td>
<td>Unique</td>
<td>DS Save Area (R/W) See Table 35-2. See Section 18.12.4, “Debug Store (DS) Mechanism.”</td>
</tr>
<tr>
<td>680H 1664</td>
<td>MSR_LASTBRANCH_0_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 0 (R/W) One of 16 pairs of last branch record registers on the last branch record stack (680H-68FH). This part of the stack contains pointers to the source instruction for one of the last 16 branches, exceptions, or interrupts taken by the processor. The MSRs at 680H-68FH, 6C0H-6CfH are not available in processor releases before family 0FH, model 03H. These MSRs replace MSRs previously located at 1DBH-1DEH which performed the same function for early releases. See Section 17.9, “Last Branch, Call Stack, Interrupt, and Exception Recording for Processors based on Skylake Microarchitecture.”</td>
</tr>
<tr>
<td>681H 1665</td>
<td>MSR_LASTBRANCH_1_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 1 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>682H 1666</td>
<td>MSR_LASTBRANCH_2_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 2 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>683H 1667</td>
<td>MSR_LASTBRANCH_3_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 3 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>684H 1668</td>
<td>MSR_LASTBRANCH_4_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 4 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>685H 1669</td>
<td>MSR_LASTBRANCH_5_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 5 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>686H 1670</td>
<td>MSR_LASTBRANCH_6_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 6 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>687H 1671</td>
<td>MSR_LASTBRANCH_7_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 7 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>688H 1672</td>
<td>MSR_LASTBRANCH_8_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 8 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>689H 1673</td>
<td>MSR_LASTBRANCH_9_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 9 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
<tr>
<td>68AH 1674</td>
<td>MSR_LASTBRANCH_10_FROM_IP</td>
<td>3, 4, 6</td>
<td>Unique</td>
<td>Last Branch Record 10 See description of MSR_LASTBRANCH_0 at 680H.</td>
</tr>
</tbody>
</table>
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<tr>
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<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 68BH 1675        | MSR_LASTBRANCH_11_FROM_IP     | 3, 4, 6           | Unique        | Last Branch Record 11  
See description of MSR_LASTBRANCH_0 at 680H. |
| 68CH 1676        | MSR_LASTBRANCH_12_FROM_IP     | 3, 4, 6           | Unique        | Last Branch Record 12  
See description of MSR_LASTBRANCH_0 at 680H. |
| 68DH 1677        | MSR_LASTBRANCH_13_FROM_IP     | 3, 4, 6           | Unique        | Last Branch Record 13  
See description of MSR_LASTBRANCH_0 at 680H. |
| 68EH 1678        | MSR_LASTBRANCH_14_FROM_IP     | 3, 4, 6           | Unique        | Last Branch Record 14  
See description of MSR_LASTBRANCH_0 at 680H. |
| 68FH 1679        | MSR_LASTBRANCH_15_FROM_IP     | 3, 4, 6           | Unique        | Last Branch Record 15  
See description of MSR_LASTBRANCH_0 at 680H. |
| 6COH 1728        | MSR_LASTBRANCH_0_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 0 (R/W)  
One of 16 pairs of last branch record registers on the last branch record stack (6COH-6CFH). This part of the stack contains pointers to the destination instruction for one of the last 16 branches, exceptions, or interrupts that the processor took.  
See Section 17.9, “Last Branch, Call Stack, Interrupt, and Exception Recording for Processors based on Skylake Microarchitecture.” |
| 6C1H 1729        | MSR_LASTBRANCH_1_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 1  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C2H 1730        | MSR_LASTBRANCH_2_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 2  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C3H 1731        | MSR_LASTBRANCH_3_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 3  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C4H 1732        | MSR_LASTBRANCH_4_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 4  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C5H 1733        | MSR_LASTBRANCH_5_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 5  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C6H 1734        | MSR_LASTBRANCH_6_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 6  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C7H 1735        | MSR_LASTBRANCH_7_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 7  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C8H 1736        | MSR_LASTBRANCH_8_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 8  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6C9H 1737        | MSR_LASTBRANCH_9_TO_IP        | 3, 4, 6           | Unique        | Last Branch Record 9  
See description of MSR_LASTBRANCH_0 at 6COH. |
| 6CAH 1738        | MSR_LASTBRANCH_10_TO_IP       | 3, 4, 6           | Unique        | Last Branch Record 10  
See description of MSR_LASTBRANCH_0 at 6COH. |
Table 35-36. MSRs in the Pentium® 4 and Intel® Xeon® Processors (Contd.)

<table>
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<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique¹</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 6CBH 1739 | MSR-LASTBRANCH_11_TO_IP | 3, 4, 6 | Unique | Last Branch Record 11  
See description of MSR-LASTBRANCH_0 at 6COH. |
| 6CCH 1740 | MSR-LASTBRANCH_12_TO_IP | 3, 4, 6 | Unique | Last Branch Record 12  
See description of MSR-LASTBRANCH_0 at 6COH. |
| 6CDH 1741 | MSR-LASTBRANCH_13_TO_IP | 3, 4, 6 | Unique | Last Branch Record 13  
See description of MSR-LASTBRANCH_0 at 6COH. |
| 6CEH 1742 | MSR-LASTBRANCH_14_TO_IP | 3, 4, 6 | Unique | Last Branch Record 14  
See description of MSR-LASTBRANCH_0 at 6COH. |
| C000_ 0080H | IA32_EFER | 3, 4, 6 | Unique | Extended Feature Enables  
See Table 35-2. |
| C000_ 0081H | IA32_STAR | 3, 4, 6 | Unique | System Call Target Address (R/W)  
See Table 35-2. |
| C000_ 0082H | IA32_LSTAR | 3, 4, 6 | Unique | IA-32e Mode System Call Target Address (R/W)  
See Table 35-2. |
| C000_ 0084H | IA32_FMASK | 3, 4, 6 | Unique | System Call Flag Mask (R/W)  
See Table 35-2. |
| C000_ 0100H | IA32_FS_BASE | 3, 4, 6 | Unique | Map of BASE Address of FS (R/W)  
See Table 35-2. |
| C000_ 0101H | IA32_GS_BASE | 3, 4, 6 | Unique | Map of BASE Address of GS (R/W)  
See Table 35-2. |
| C000_ 0102H | IA32_KERNEL_GSBASE | 3, 4, 6 | Unique | Swap Target of BASE Address of GS (R/W)  
See Table 35-2. |

¹. For HT-enabled processors, there may be more than one logical processors per physical unit. If an MSR is Shared, this means that one MSR is shared between logical processors. If an MSR is unique, this means that each logical processor has its own MSR.

### 35.16.1 MSRs Unique to Intel® Xeon® Processor MP with L3 Cache

The MSRs listed in Table 35-37 apply to Intel® Xeon® Processor MP with up to 8MB level three cache. These processors can be detected by enumerating the deterministic cache parameter leaf of CPUID instruction (with EAX = 4 as input) to detect the presence of the third level cache, and with CPUID reporting family encoding 0FH, model encoding 3 or 4 (see CPUID instruction for more details).
The MSRs listed in Table 35-38 apply to Intel® Xeon® Processor 7100 series. These processors can be detected by enumerating the deterministic cache parameter leaf of CPUID instruction (with EAX = 4 as input) to detect the presence of the third level cache, and with CPUID reporting family encoding 0FH, model encoding 6 (See CPUID instruction for more details.). The performance monitoring MSRs listed in Table 35-38 are shared between logical processors in the same core, but are replicated for each core.

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>107CCH</td>
<td>MSR_IFSB_BUSQ0</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB BUSQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache.”</td>
</tr>
<tr>
<td>107CDH</td>
<td>MSR_IFSB_BUSQ1</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB BUSQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107CEH</td>
<td>MSR_IFSB_SNPQ0</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB SNPQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache.”</td>
</tr>
<tr>
<td>107CFH</td>
<td>MSR_IFSB_SNPQ1</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB SNPQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107D0H</td>
<td>MSR_EFSB_DRDY0</td>
<td>3, 4</td>
<td>Shared</td>
<td>EFSB DRDY Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache” for details.</td>
</tr>
<tr>
<td>107D1H</td>
<td>MSR_EFSB_DRDY1</td>
<td>3, 4</td>
<td>Shared</td>
<td>EFSB DRDY Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107D2H</td>
<td>MSR_IFSB_CTL6</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB Latency Event Control Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache” for details.</td>
</tr>
<tr>
<td>107D3H</td>
<td>MSR_IFSB_CNTR7</td>
<td>3, 4</td>
<td>Shared</td>
<td>IFSB Latency Event Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache.”</td>
</tr>
</tbody>
</table>
MODEL-SPECIFIC REGISTERS (MSRS)

35.17 MSRS IN INTEL® CORE™ SOLO AND INTEL® CORE™ DUO PROCESSORS

Model-specific registers (MSRs) for Intel Core Solo, Intel Core Duo processors, and Dual-core Intel Xeon processor LV are listed in Table 35-39. The column “Shared/Unique” applies to Intel Core Duo processor. “Unique” means each processor core has a separate MSR, or a bit field in an MSR governs only a core independently. “Shared” means the MSR or the bit field in an MSR address governs the operation of both processor cores.

Table 35-38. MSRs Unique to Intel® Xeon® Processor 7100 Series

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Model Availability</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>107CCH</td>
<td>MSR_EMON_L3_CTR_CTL0</td>
<td>6</td>
<td>Shared</td>
<td>GBUSQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache.”</td>
</tr>
<tr>
<td>107CDH</td>
<td>MSR_EMON_L3_CTR_CTL1</td>
<td>6</td>
<td>Shared</td>
<td>GBUSQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107CEH</td>
<td>MSR_EMON_L3_CTR_CTL2</td>
<td>6</td>
<td>Shared</td>
<td>GSNPQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache.”</td>
</tr>
<tr>
<td>107CFH</td>
<td>MSR_EMON_L3_CTR_CTL3</td>
<td>6</td>
<td>Shared</td>
<td>GSNPQ Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107D0H</td>
<td>MSR_EMON_L3_CTR_CTL4</td>
<td>6</td>
<td>Shared</td>
<td>FSB Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Section 18.17, “Performance Monitoring on 64-bit Intel Xeon Processor MP with Up to 8-MByte L3 Cache” for details.</td>
</tr>
<tr>
<td>107D1H</td>
<td>MSR_EMON_L3_CTR_CTL5</td>
<td>6</td>
<td>Shared</td>
<td>FSB Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107D2H</td>
<td>MSR_EMON_L3_CTR_CTL6</td>
<td>6</td>
<td>Shared</td>
<td>FSB Event Control and Counter Register (R/W)</td>
</tr>
<tr>
<td>107D3H</td>
<td>MSR_EMON_L3_CTR_CTL7</td>
<td>6</td>
<td>Shared</td>
<td>FSB Event Control and Counter Register (R/W)</td>
</tr>
</tbody>
</table>

Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H 0</td>
<td>P5_MC_ADDR</td>
<td>Unique</td>
<td>See Section 35.20, “MSRs in Pentium Processors,” and see Table 35-2.</td>
</tr>
<tr>
<td>1H 1</td>
<td>P5_MC_TYPE</td>
<td>Unique</td>
<td>See Section 35.20, “MSRs in Pentium Processors,” and see Table 35-2.</td>
</tr>
<tr>
<td>6H 6</td>
<td>IA32_MONITOR_FILTER_SIZE</td>
<td>Unique</td>
<td>See Section 8.10.5, “Monitor/Mwait Address Range Determination,” and see Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>10H</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>Unique</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H</td>
<td>IA32_PLATFORM_ID</td>
<td>Shared</td>
<td>Platform ID (R) See Table 35-2. The operating system can use this MSR to determine “slot” information for the processor and the proper microcode update to load.</td>
</tr>
<tr>
<td>1BH</td>
<td>IA32_APIC_BASE</td>
<td>Unique</td>
<td>See Section 10.4.4, “Local APIC Status and Location,” and see Table 35-2.</td>
</tr>
<tr>
<td>2AH</td>
<td>MSR_EBL_CR_POWERON</td>
<td>Shared</td>
<td>Processor Hard Power-On Configuration (R/W) Enables and disables processor features; (R) indicates current processor configuration.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Data Error Checking Enable (R/W) 1 = Enabled; 0 = Disabled Note: Not all processor implements R/W.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Response Error Checking Enable (R/W) 1 = Enabled; 0 = Disabled Note: Not all processor implements R/W.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>MCERR# Drive Enable (R/W) 1 = Enabled; 0 = Disabled Note: Not all processor implements R/W.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Address Parity Enable (R/W) 1 = Enabled; 0 = Disabled Note: Not all processor implements R/W.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6:5</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>BINIT# Driver Enable (R/W) 1 = Enabled; 0 = Disabled Note: Not all processor implements R/W.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Output Tri-state Enabled (R/O) 1 = Enabled; 0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Execute BIST (R/O)   1 = Enabled; 0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>MCERR# Observation Enabled (R/O) 1 = Enabled; 0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>BINIT# Observation Enabled (R/O) 1 = Enabled; 0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>1 MByte Power on Reset Vector (R/O) 1 = 1 MByte; 0 = 4 GBytes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17:16</td>
<td>APIC Cluster ID (R/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>System Bus Frequency (R/O)</td>
<td></td>
<td>0 = 100 MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Reserved</td>
</tr>
<tr>
<td>19</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21:20</td>
<td>Symmetric Arbitration ID (R/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26:22</td>
<td>Clock Frequency Ratio (R/O)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3AH</td>
<td>IA32_FEATURE_CONTROL</td>
<td>Unique</td>
<td>Control Features in IA-32 Processor (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>40H</td>
<td>MSR_LASTBRANCH_0</td>
<td>Unique</td>
<td>Last Branch Record 0 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>One of 8 last branch record registers on the last branch record stack: bits 31-0 hold the ‘from’ address and bits 63-32 hold the ‘to’ address. See also:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Last Branch Record Stack TOS at 1C9H</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors).”</td>
</tr>
<tr>
<td>41H</td>
<td>MSR_LASTBRANCH_1</td>
<td>Unique</td>
<td>Last Branch Record 1 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>42H</td>
<td>MSR_LASTBRANCH_2</td>
<td>Unique</td>
<td>Last Branch Record 2 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>43H</td>
<td>MSR_LASTBRANCH_3</td>
<td>Unique</td>
<td>Last Branch Record 3 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>44H</td>
<td>MSR_LASTBRANCH_4</td>
<td>Unique</td>
<td>Last Branch Record 4 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>45H</td>
<td>MSR_LASTBRANCH_5</td>
<td>Unique</td>
<td>Last Branch Record 5 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>46H</td>
<td>MSR_LASTBRANCH_6</td>
<td>Unique</td>
<td>Last Branch Record 6 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>47H</td>
<td>MSR_LASTBRANCH_7</td>
<td>Unique</td>
<td>Last Branch Record 7 (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See description of MSR_LASTBRANCH_0.</td>
</tr>
<tr>
<td>79H</td>
<td>IA32_BIOS_UPDT_TRIG</td>
<td>Unique</td>
<td>BIOS Update Trigger Register (W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>8BH</td>
<td>IA32_BIOS_SIGN_ID</td>
<td>Unique</td>
<td>BIOS Update Signature ID (RO)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C1H</td>
<td>IA32_PMC0</td>
<td>Unique</td>
<td>Performance counter register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>C2H</td>
<td>IA32_PMC1</td>
<td>Unique</td>
<td>Performance counter register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
</tbody>
</table>
### Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDH</td>
<td>205</td>
<td>MSR_FSB_FREQ</td>
<td>Shared</td>
<td><strong>Scaleable Bus Speed (RO)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This field indicates the scaleable bus clock speed:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2:0 • 101B: 100 MHz (FSB 400)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 001B: 133 MHz (FSB 533)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• 011B: 167 MHz (FSB 667)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>133.33 MHz should be utilized if performing calculation with System Bus Speed when encoding is 101B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>166.67 MHz should be utilized if performing calculation with System Bus Speed when encoding is 001B.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:3 Reserved.</td>
</tr>
<tr>
<td>E7H</td>
<td>231</td>
<td>IA32_MPERF</td>
<td>Unique</td>
<td><strong>Maximum Performance Frequency Clock Count. (RW)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>E8H</td>
<td>232</td>
<td>IA32_APERF</td>
<td>Unique</td>
<td><strong>Actual Performance Frequency Clock Count. (RW)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>FEH</td>
<td>254</td>
<td>IA32_MTRRCAP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>11EH</td>
<td>281</td>
<td>MSR_BBL_CR_CTL3</td>
<td>Shared</td>
<td><strong>L2 Hardware Enabled (RO)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = If the L2 is hardware-enabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = Indicates if the L2 is hardware-disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>7:1 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>L2 Enabled (R/W)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = L2 cache has been initialized</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = Disabled (default)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Until this bit is set the processor will not respond to the WBINVD instruction or the assertion of the FLUSH# input.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>22:9 Reserved.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>L2 Not Present (RO)</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0 = L2 Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1 = L2 Not Present</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>63:24 Reserved.</td>
</tr>
<tr>
<td>174H</td>
<td>372</td>
<td>IA32_SYSENTER_CS</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>175H</td>
<td>373</td>
<td>IA32_SYSENTER_ESP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>176H</td>
<td>374</td>
<td>IA32_SYSENTER_EIP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>179H</td>
<td>377</td>
<td>IA32_MCG_CAP</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>17AH</td>
<td>378</td>
<td>IA32_MCG_STATUS</td>
<td>Unique</td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>RIPV</td>
<td></td>
<td>When set, this bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) can be used to restart the program. If this bit is cleared, the program cannot be reliably restarted.</td>
</tr>
<tr>
<td>1</td>
<td>EIPV</td>
<td></td>
<td>When set, this bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) is directly associated with the error.</td>
</tr>
<tr>
<td>2</td>
<td>MCIP</td>
<td></td>
<td>When set, this bit indicates that a machine check has been generated. If a second machine check is detected while this bit is still set, the processor enters a shutdown state. Software should write this bit to 0 after processing a machine check exception.</td>
</tr>
<tr>
<td>63:3</td>
<td></td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>186H 390</td>
<td>IA32_PERFEVTSEL0</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>187H 391</td>
<td>IA32_PERFEVTSEL1</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>Shared</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Unique</td>
<td>Clock Modulation (R/W)</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Unique</td>
<td>Thermal Interrupt Control (R/W)</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Unique</td>
<td>Thermal Monitor Status (R/W)</td>
</tr>
<tr>
<td>19DH 413</td>
<td>MSR_THERM2_CTL</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>15:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>TM_SELECT</td>
<td>(R/W)</td>
<td>Mode of automatic thermal monitor:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 = Thermal Monitor 1 (thermally-initiated on-die modulation of the stop-clock duty cycle)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 = Thermal Monitor 2 (thermally-initiated frequency transitions)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If bit 3 of the IA32_MISC_ENABLE register is cleared, TM_SELECT has no effect. Neither TM1 nor TM2 will be enabled.</td>
</tr>
<tr>
<td>63:16</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td></td>
<td>Enable Miscellaneous Processor Features (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td>2:0</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Unique</td>
<td>Automatic Thermal Control Circuit Enable (R/W) See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>6:4</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Shared</td>
<td>Performance Monitoring Available (R) See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>9:8</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Shared</td>
<td>FERR# Multiplexing Enable (R/W) 1 = FERR# asserted by the processor to indicate a pending break event within the processor 0 = Indicates compatible FERR# signaling behavior This bit must be set to 1 to support XAPIC interrupt model usage.</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Shared</td>
<td>Branch Trace Storage Unavailable (RO) See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>Shared</td>
<td>TM2 Enable (R/w) When this bit is set (1) and the thermal sensor indicates that the die temperature is at the pre-determined threshold, the Thermal Monitor 2 mechanism is engaged. TM2 will reduce the bus to core ratio and voltage according to the value last written to MSR_THERM2_CTL bits 15:0. When this bit is clear (0, default), the processor does not change the VID signals or the bus to core ratio when the processor enters a thermal managed state. If the TM2 feature flag (ECX[8]) is not set to 1 after executing CPUID with EAX = 1, then this feature is not supported and BIOS must not alter the contents of this bit location. The processor is operating out of spec if both this bit and the TM1 bit are set to disabled states.</td>
<td></td>
</tr>
<tr>
<td>15:14</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>Shared</td>
<td>Enhanced Intel SpeedStep Technology Enable (R/w) 1 = Enhanced Intel SpeedStep Technology enabled</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Shared</td>
<td>ENABLE MONITOR FSM (R/w) See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>Shared</td>
<td>Limit CPUID Maxval (R/w) See Table 35-2. Setting this bit may cause behavior in software that depends on the availability of CPUID leaves greater than 3.</td>
<td></td>
</tr>
<tr>
<td>33:23</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Shared</td>
<td>XD Bit Disable (R/w) See Table 35-2.</td>
<td></td>
</tr>
<tr>
<td>63:35</td>
<td>Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Shared/Unique</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------</td>
<td>---------------</td>
<td>--------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1C9H 457</td>
<td>MSR_LASTBRANCH_TOS</td>
<td>Unique</td>
<td>Last Branch Record Stack TOS (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains an index (bits 0-3) that points to the MSR containing the most recent branch record.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>See MSR_LASTBRANCH_0_FROM_IP (at 40H).</td>
</tr>
<tr>
<td>1D9H 473</td>
<td>IA32_DEBUGCTL</td>
<td>Unique</td>
<td>Debug Control (R/W)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Controls how several debug features are used. Bit definitions are discussed in the referenced section.</td>
</tr>
<tr>
<td>1DDH 477</td>
<td>MSR_LER_FROM_LIP</td>
<td>Unique</td>
<td>Last Exception Record From Linear IP (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Contains a pointer to the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>1DEH 478</td>
<td>MSR_LER_TO_LIP</td>
<td>Unique</td>
<td>Last Exception Record To Linear IP (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This area contains a pointer to the target of the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.</td>
</tr>
<tr>
<td>1E0H 480</td>
<td>ROB_CR_BKUPTMPDR6</td>
<td>Unique</td>
<td>Fast String Enable bit. (Default, enabled)</td>
</tr>
<tr>
<td></td>
<td>1:0 Reserved.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>200H 512</td>
<td>MTRRphysBase0</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>201H 513</td>
<td>MTRRphysMask0</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>202H 514</td>
<td>MTRRphysBase1</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>203H 515</td>
<td>MTRRphysMask1</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>204H 516</td>
<td>MTRRphysBase2</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>205H 517</td>
<td>MTRRphysMask2</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>206H 518</td>
<td>MTRRphysBase3</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>207H 519</td>
<td>MTRRphysMask3</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>208H 520</td>
<td>MTRRphysBase4</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>209H 521</td>
<td>MTRRphysMask4</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20AH 522</td>
<td>MTRRphysBase5</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20BH 523</td>
<td>MTRRphysMask5</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20CH 524</td>
<td>MTRRphysBase6</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20DH 525</td>
<td>MTRRphysMask6</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20EH 526</td>
<td>MTRRphysBase7</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>20FH 527</td>
<td>MTRRphysMask7</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>250H 592</td>
<td>MTRRfix64K_00000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>258H 600</td>
<td>MTRRfix16K_80000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>259H 601</td>
<td>MTRRfix16K_A0000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>268H 616</td>
<td>MTRRfix4K_C0000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>Hex Address</td>
<td>Register Name</td>
<td>Shared/Unique</td>
<td>Bit Description</td>
</tr>
<tr>
<td>-------------</td>
<td>----------------------</td>
<td>---------------</td>
<td>----------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>269H 617</td>
<td>MTRRfix4K_C8000</td>
<td>Unique</td>
<td>Default Memory Types (R/W)</td>
</tr>
<tr>
<td>26AH 618</td>
<td>MTRRfix4K_D0000</td>
<td>Unique</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>26BH 619</td>
<td>MTRRfix4K_D8000</td>
<td>Unique</td>
<td>See Section 11.11.2.1, &quot;IA32_MTRR_DEF_TYPE MSR.&quot;</td>
</tr>
<tr>
<td>26CH 620</td>
<td>MTRRfix4K_E0000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>26DH 621</td>
<td>MTRRfix4K_E8000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>26EH 622</td>
<td>MTRRfix4K_F0000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>26FH 623</td>
<td>MTRRfix4K_F8000</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>2FFH 767</td>
<td>IA32_MTRR_DEF_TYPE</td>
<td>Unique</td>
<td>Default Memory Types (R/W)</td>
</tr>
<tr>
<td>400H 1024</td>
<td>IA32_MC0_CTL</td>
<td>Unique</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>401H 1025</td>
<td>IA32_MC0_STATUS</td>
<td>Unique</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>402H 1026</td>
<td>IA32_MC0_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, &quot;IA32_MCi_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>404H 1028</td>
<td>IA32_MC1_CTL</td>
<td>Unique</td>
<td>The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>405H 1029</td>
<td>IA32_MC1_STATUS</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>406H 1030</td>
<td>IA32_MC1_ADDR</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>408H 1032</td>
<td>IA32_MC2_CTL</td>
<td>Unique</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>409H 1033</td>
<td>IA32_MC2_STATUS</td>
<td>Unique</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
<tr>
<td>40AH 1034</td>
<td>IA32_MC2_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, &quot;IA32_MCi_ADDR MSRs.&quot;</td>
</tr>
<tr>
<td>40CH 1036</td>
<td>MSR_MC4_CTL</td>
<td>Unique</td>
<td>The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>40DH 1037</td>
<td>MSR_MC4_STATUS</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>40EH 1038</td>
<td>MSR_MC4_ADDR</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>410H 1040</td>
<td>MSR_MC3_CTL</td>
<td>Unique</td>
<td>See Section 15.3.2.1, &quot;IA32_MCi_CTL MSRs.&quot;</td>
</tr>
<tr>
<td>411H 1041</td>
<td>MSR_MC3_STATUS</td>
<td>Unique</td>
<td>See Section 15.3.2.2, &quot;IA32_MCi_STATUS MSRs.&quot;</td>
</tr>
</tbody>
</table>
The MSR_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.

### Table 35-39. MSRs in Intel® Core™ Solo, Intel® Core™ Duo Processors, and Dual-Core Intel® Xeon® Processor LV

<table>
<thead>
<tr>
<th>Hex</th>
<th>Dec</th>
<th>Register Name</th>
<th>Shared/Unique</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>412H</td>
<td>1042</td>
<td>MSR_MC3_ADDR</td>
<td>Unique</td>
<td>See Section 15.3.2.3, “IA32_MCI_ADDR MSRs.” The MSR_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception.</td>
</tr>
<tr>
<td>413H</td>
<td>1043</td>
<td>MSR_MC3_MISC</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>414H</td>
<td>1044</td>
<td>MSR_MC5_CTL</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>415H</td>
<td>1045</td>
<td>MSR_MC5_STATUS</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>416H</td>
<td>1046</td>
<td>MSR_MC5_ADDR</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>417H</td>
<td>1047</td>
<td>MSR_MC5_MISC</td>
<td>Unique</td>
<td></td>
</tr>
<tr>
<td>480H</td>
<td>1152</td>
<td>IA32_VMX_BASIC</td>
<td>Unique</td>
<td>Reporting Register of Basic VMX Capabilities (R/O) See Table 35-2. See Appendix A.1, “Basic VMX Information” (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>481H</td>
<td>1153</td>
<td>IA32_VMX_PINBASED_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of Pin-based VM-execution Controls (R/O) See Appendix A.3, &quot;VM-Execution Controls&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>482H</td>
<td>1154</td>
<td>IA32_VMX_PROCBASED_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of Primary Processor-based VM-execution Controls (R/O) See Appendix A.3, &quot;VM-Execution Controls&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>483H</td>
<td>1155</td>
<td>IA32_VMX_EXIT_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of VM-exit Controls (R/O) See Appendix A.4, &quot;VM-Exit Controls&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>484H</td>
<td>1156</td>
<td>IA32_VMX_ENTRY_CTLS</td>
<td>Unique</td>
<td>Capability Reporting Register of VM-entry Controls (R/O) See Appendix A.5, &quot;VM-Entry Controls&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>485H</td>
<td>1157</td>
<td>IA32_VMX_MISC</td>
<td>Unique</td>
<td>Reporting Register of Miscellaneous VMX Capabilities (R/O) See Appendix A.6, &quot;Miscellaneous Data&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>486H</td>
<td>1158</td>
<td>IA32_VMX_CR0_FIXED0</td>
<td>Unique</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 0 (R/O) See Appendix A.7, &quot;VMX-Fixed Bits in CR0&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>487H</td>
<td>1159</td>
<td>IA32_VMX_CR0_FIXED1</td>
<td>Unique</td>
<td>Capability Reporting Register of CR0 Bits Fixed to 1 (R/O) See Appendix A.7, &quot;VMX-Fixed Bits in CR0&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
<tr>
<td>488H</td>
<td>1160</td>
<td>IA32_VMX_CR4_FIXED0</td>
<td>Unique</td>
<td>Capability Reporting Register of CR4 Bits Fixed to 0 (R/O) See Appendix A.8, &quot;VMX-Fixed Bits in CR4&quot; (If CPUID.01H:ECX.[bit 9])</td>
</tr>
</tbody>
</table>
### 35.18 MSRS IN THE PENTIUM M PROCESSOR

Model-specific registers (MSRs) for the Pentium M processor are similar to those described in Section 35.19 for P6 family processors. The following table describes new MSRs and MSRs whose behavior has changed on the Pentium M processor.

#### Table 35-40. MSRs in Pentium M Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex Dec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0H 0</td>
<td>P5_MC_ADDR</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H 1</td>
<td>P5_MC_TYPE</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>10H 16</td>
<td>IA32_TIME_STAMP_COUNTER</td>
<td>See Section 17.14, “Time-Stamp Counter,” and see Table 35-2.</td>
</tr>
<tr>
<td>17H 23</td>
<td>IA32_PLATFORM_ID</td>
<td>Platform ID (R)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The operating system can use this MSR to determine “slot” information for the processor and the proper microcode update to load.</td>
</tr>
<tr>
<td>Hex</td>
<td>Dec</td>
<td>Register Address</td>
</tr>
<tr>
<td>-----</td>
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<tr>
<td>2AH</td>
<td>42</td>
<td>MSR_EBL_CR_POWERON</td>
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<td></td>
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</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------------</td>
<td>------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
</tbody>
</table>
| 18               | System Bus Frequency (R/O) | 0 = 100 MHz  
1 = Reserved  
Always 0 on the Pentium M processor. |
| 19               | Reserved.         |                                                                                                                                           |
| 21: 20           | Symmetric Arbitration ID (R/O) | Always 00B on the Pentium M processor.                                                                                                      |
| 26:22            | Clock Frequency Ratio (R/O) |                                                                                                                                           |
| 40H 64           | MSR_LASTBRANCH_0  | Last Branch Record 0 (R/W)  
One of 8 last branch record registers on the last branch record stack: bits 31-0 hold the ‘from’ address and bits 63-32 hold the to address.  
See also:  
• Last Branch Record Stack TOS at 1C9H  
• Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors)” |
| 41H 65           | MSR_LASTBRANCH_1  | Last Branch Record 1 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 42H 66           | MSR_LASTBRANCH_2  | Last Branch Record 2 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 43H 67           | MSR_LASTBRANCH_3  | Last Branch Record 3 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 44H 68           | MSR_LASTBRANCH_4  | Last Branch Record 4 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 45H 69           | MSR_LASTBRANCH_5  | Last Branch Record 5 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 46H 70           | MSR_LASTBRANCH_6  | Last Branch Record 6 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 47H 71           | MSR_LASTBRANCH_7  | Last Branch Record 7 (R/W)  
See description of MSR_LASTBRANCH_0. |
| 119H 281         | MSR_BBL_CR_CTL    | 63:0 Reserved.                                                                                                                                     |
| 11EH 281         | MSR_BBL_CR_CTL3   | 0 L2 Hardware Enabled (RO)  
1 = If the L2 is hardware-enabled  
0 = Indicates if the L2 is hardware-disabled  
4:1 Reserved. |
### Table 35-40. MSRs in Pentium M Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 5                | Ecc Check Enable (RO) | This bit enables ECC checking on the cache data bus. ECC is always generated on write cycles.  
0 = Disabled (default)  
1 = Enabled  
For the Pentium M processor, ECC checking on the cache data bus is always enabled. |
| 7:6              | Reserved.         |                                                                                  |
| 8                | L2 Enabled (R/W)   | 1 = L2 cache has been initialized  
0 = Disabled (default)  
Until this bit is set the processor will not respond to the WBINVD instruction or the assertion of the FLUSH# input. |
| 22:9             | Reserved.         |                                                                                  |
| 23               | L2 Not Present (RO) | 0 = L2 Present  
1 = L2 Not Present |
| 63:24            | Reserved.         |                                                                                  |
| 179H 377         | IA32_MCG_CAP      | 7:0  
Count (RO)  
Indicates the number of hardware unit error reporting banks available in the processor. |
| 8                | IA32_MCG_CTL Present (RO) | 1 = Indicates that the processor implements the MSR_MCG_CTL register found at MSR 17BH.  
0 = Not supported. |
| 17AH 378         | IA32_MCG_STATUS   | 0  
RIPV  
When set, this bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) can be used to restart the program. If this bit is cleared, the program cannot be reliably restarted. |
|                  |                   | 1  
EIPV  
When set, this bit indicates that the instruction addressed by the instruction pointer pushed on the stack (when the machine check was generated) is directly associated with the error. |
|                  |                   | 2  
MCIP  
When set, this bit indicates that a machine check has been generated. If a second machine check is detected while this bit is still set, the processor enters a shutdown state. Software should write this bit to 0 after processing a machine check exception. |
|                  |                   | 63:3  
Reserved. |
### Table 35-40. MSRs in Pentium M Processors (Contd.)

<table>
<thead>
<tr>
<th>Hex Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>198H 408</td>
<td>IA32_PERF_STATUS</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>199H 409</td>
<td>IA32_PERF_CTL</td>
<td>See Table 35-2.</td>
</tr>
<tr>
<td>19AH 410</td>
<td>IA32_CLOCK_MODULATION</td>
<td>Clock Modulation (R/w). See Table 35-2. See Section 14.7.3, “Software Controlled Clock Modulation.”</td>
</tr>
<tr>
<td>19BH 411</td>
<td>IA32_THERM_INTERRUPT</td>
<td>Thermal Interrupt Control (R/w) See Table 35-2. See Section 14.7.2, “Thermal Monitor.”</td>
</tr>
<tr>
<td>19CH 412</td>
<td>IA32_THERM_STATUS</td>
<td>Thermal Monitor Status (R/w) See Table 35-2. See Section 14.7.2, “Thermal Monitor.”</td>
</tr>
<tr>
<td>19DH 413</td>
<td>MSR_THERM2_CTL</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>15:0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>TM_SELECT (R/w) Mode of automatic thermal monitor: 0 = Thermal Monitor 1 (thermally-initiated on-die modulation of the stop-clock duty cycle) 1 = Thermal Monitor 2 (thermally-initiated frequency transitions) If bit 3 of the IA32_MISC_ENABLE register is cleared, TM_SELECT has no effect. Neither TM1 nor TM2 will be enabled.</td>
</tr>
<tr>
<td></td>
<td>63:16</td>
<td>Reserved.</td>
</tr>
<tr>
<td>1A0H 416</td>
<td>IA32_MISC_ENABLE</td>
<td>Enable Miscellaneous Processor Features (R/w) Allows a variety of processor functions to be enabled and disabled.</td>
</tr>
<tr>
<td></td>
<td>2:0</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>Automatic Thermal Control Circuit Enable (R/w) 1 = Setting this bit enables the thermal control circuit (TCC) portion of the Intel Thermal Monitor feature. This allows processor clocks to be automatically modulated based on the processor's thermal sensor operation. 0 = Disabled (default). The automatic thermal control circuit enable bit determines if the thermal control circuit (TCC) will be activated when the processor's internal thermal sensor determines the processor is about to exceed its maximum operating temperature. When the TCC is activated and TM1 is enabled, the processor's clocks will be forced to a 50% duty cycle. BIOS must enable this feature. The bit should not be confused with the on-demand thermal control circuit enable bit.</td>
</tr>
<tr>
<td></td>
<td>6:4</td>
<td>Reserved.</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>Performance Monitoring Available (R) 1 = Performance monitoring enabled 0 = Performance monitoring disabled</td>
</tr>
</tbody>
</table>
### Table 35-40. MSRs in Pentium M Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:8</td>
<td>Reserved.</td>
<td></td>
</tr>
</tbody>
</table>
| 10               | **FERR# Multiplexing Enable (R/W)** | 1 = FERR# asserted by the processor to indicate a pending break event within the processor  
0 = Indicates compatible FERR# signaling behavior  
This bit must be set to 1 to support XAPIC interrupt model usage. |
| 12               | **Branch Trace Storage Unavailable (RO)** | 1 = Processor doesn't support branch trace storage (BTS)  
0 = BTS is supported |
| 15:13            | Reserved.     |                 |
| 16               | **Enhanced Intel SpeedStep Technology Enable (R/W)** | 1 = Enhanced Intel SpeedStep Technology enabled.  
On the Pentium M processor, this bit may be configured to be read-only. |
| 22:17            | Reserved.     |                 |
| 23               | **xTPR Message Disable (R/W)** | When set to 1, xTPR messages are disabled. xTPR messages are optional messages that allow the processor to inform the chipset of its priority.  
The default is processor specific. |
| 1C9H 457         | MSR_LASTBRANCH_TOS | **Last Branch Record Stack TOS (R/W)**  
Contains an index (bits 0-3) that points to the MSR containing the most recent branch record. See also:  
• MSR_LASTBRANCH_0_FROM_IP (at 40H)  
• Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors)” |
| 1D9H 473         | MSR_DEBUGCTLB | **Debug Control (R/W)**  
Controls how several debug features are used. Bit definitions are discussed in the referenced section.  
See Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors).” |
| 1DDH 477         | MSR_LER_TO_LIP | **Last Exception Record To Linear IP (R)**  
This area contains a pointer to the target of the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.  
See Section 17.12, “Last Branch, Interrupt, and Exception Recording (Pentium M Processors)” and Section 17.13.2, “Last Branch and Last Exception MSRs.” |
### Table 35-40. MSRs in Pentium M Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 1DEH 478         | MSR_LER_FROM_LIP | Last Exception Record From Linear IP (R)  
Contains a pointer to the last branch instruction that the processor executed prior to the last exception that was generated or the last interrupt that was handled.  
See Section 17.12, "Last Branch, Interrupt, and Exception Recording (Pentium M Processors)" and Section 17.13.2, "Last Branch and Last Exception MSRs." |
| 2FFH 767         | IA32_MTRR_DEF_TYPE | Default Memory Types (R/W)  
Sets the memory type for the regions of physical memory that are not mapped by the MTRRs.  
See Section 11.11.2.1, "IA32_MTRR_DEF_TYPE MSR." |
| 400H 1024        | IA32_MC0_CTL    | See Section 15.3.2.1, "IA32_MCi_CTL MSRs." |
| 401H 1025        | IA32_MC0_STATUS | See Section 15.3.2.2, "IA32_MCi_STATUS MSRs." |
| 402H 1026        | IA32_MC0_ADDR   | See Section 14.3.2.3, "IA32_MCi_ADDR MSRs."  
The IA32_MC0_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC0_STATUS register is clear.  
When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception. |
| 404H 1028        | IA32_MC1_CTL    | See Section 15.3.2.1, "IA32_MCi_CTL MSRs." |
| 405H 1029        | IA32_MC1_STATUS | See Section 15.3.2.2, "IA32_MCi_STATUS MSRs." |
| 406H 1030        | IA32_MC1_ADDR   | See Section 14.3.2.3, "IA32_MCi_ADDR MSRs."  
The IA32_MC1_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC1_STATUS register is clear.  
When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception. |
| 408H 1032        | IA32_MC2_CTL    | See Section 15.3.2.1, "IA32_MCi_CTL MSRs." |
| 409H 1033        | IA32_MC2_STATUS | See Chapter 15.3.2.2, "IA32_MCi_STATUS MSRs." |
| 40AH 1034        | IA32_MC2_ADDR   | See Section 14.3.2.3, "IA32_MCi_ADDR MSRs."  
The IA32_MC2_ADDR register is either not implemented or contains no address if the ADDRV flag in the IA32_MC2_STATUS register is clear.  
When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception. |
| 40CH 1036        | MSR_MC4_CTL     | See Section 15.3.2.1, "IA32_MCi_CTL MSRs." |
| 40DH 1037        | MSR_MC4_STATUS  | See Section 15.3.2.2, "IA32_MCi_STATUS MSRs." |
| 40EH 1038        | MSR_MC4_ADDR    | See Section 14.3.2.3, "IA32_MCi_ADDR MSRs."  
The MSR_MC4_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC4_STATUS register is clear.  
When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception. |
| 410H 1040        | MSR_MC3_CTL     | See Section 15.3.2.1, "IA32_MCi_CTL MSRs." |
| 411H 1041        | MSR_MC3_STATUS  | See Section 15.3.2.2, "IA32_MCi_STATUS MSRs." |
The following MSRs are defined for the P6 family processors. The MSRs in this table that are shaded are available only in the Pentium II and Pentium III processors. Beginning with the Pentium 4 processor, some of the MSRs in this list have been designated as “architectural” and have had their names changed. See Table 35-2 for a list of the architectural MSRs.

### Table 35-40. MSRs in Pentium M Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
</table>
| 412H 1042        | MSR_MC3_ADDR      | See Section 15.3.2.3, “IA32_MCi_ADDR MSRs.”  
The MSR_MC3_ADDR register is either not implemented or contains no address if the ADDRV flag in the MSR_MC3_STATUS register is clear. When not implemented in the processor, all reads and writes to this MSR will cause a general-protection exception. |
| 600H 1536        | IA32_DS_AREA      | DS Save Area (R/W)  
Points to the DS buffer management area, which is used to manage the BTS and PEBS buffers. See Section 18.12.4, “Debug Store (DS) Mechanism.” |
| 31:0             | DS Buffer Management Area |  
Linear address of the first byte of the DS buffer management area. |
| 63:32            | Reserved.         |                                                                                  |

### 35.19 MSRS IN THE P6 FAMILY PROCESSORS

The following MSRs are defined for the P6 family processors. The MSRs in this table that are shaded are available only in the Pentium II and Pentium III processors. Beginning with the Pentium 4 processor, some of the MSRs in this list have been designated as “architectural” and have had their names changed. See Table 35-2 for a list of the architectural MSRs.

### Table 35-41. MSRs in the P6 Family Processors

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H 0</td>
<td>P5_MC_ADDR</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>1H 1</td>
<td>P5_MC_TYPE</td>
<td>See Section 35.20, “MSRs in Pentium Processors.”</td>
</tr>
<tr>
<td>10H 16</td>
<td>TSC</td>
<td>See Section 17.14, “Time-Stamp Counter.”</td>
</tr>
</tbody>
</table>
| 17H 23           | IA32_PLATFORM_ID  | Platform ID (R)  
The operating system can use this MSR to determine “slot” information for the processor and the proper microcode update to load. |
| 49:0             | Reserved.         |                                                                                  |
| 52:50            | Platform ID (R)   | Contains information concerning the intended platform for the processor.  
52 51 50  
0 0 0 Processor Flag 0  
0 0 1 Processor Flag 1  
0 1 0 Processor Flag 2  
0 1 1 Processor Flag 3  
1 0 0 Processor Flag 4  
1 0 1 Processor Flag 5  
1 1 0 Processor Flag 6  
1 1 1 Processor Flag 7 |
| 56:53            | L2 Cache Latency Read. |                                                                                  |
| 59:57            | Reserved.         |                                                                                  |
### Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hex</strong></td>
<td><strong>Dec</strong></td>
<td><strong>Register Name</strong></td>
</tr>
<tr>
<td>60</td>
<td></td>
<td>Clock Frequency Ratio Read.</td>
</tr>
<tr>
<td>63:61</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>1BH</td>
<td>27</td>
<td>APIC_BASE</td>
</tr>
<tr>
<td>7:0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Boot Strap Processor indicator Bit</td>
</tr>
<tr>
<td>1 = BSP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:9</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td></td>
<td>APIC Global Enable Bit - Permanent till reset</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31:12</td>
<td></td>
<td>APIC Base Address.</td>
</tr>
<tr>
<td>63:32</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>2AH</td>
<td>42</td>
<td>EBL_CR_POWERON</td>
</tr>
<tr>
<td>(R/W) Enables and disables processor features;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(R) indicates current processor configuration.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Data Error Checking Enable (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Response Error Checking Enable FRCERR Observation Enable (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>AERR# Drive Enable (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>BERR# Enable for Initiator Bus Requests (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>Reserved.</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>BERR# Driver Enable for Initiator Internal Errors (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>BINIT# Driver Enable (R/W)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Output Tri-state Enabled (R)</td>
</tr>
<tr>
<td>1 = Enabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 = Disabled</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>---------------</td>
<td>-----------------</td>
</tr>
<tr>
<td>9</td>
<td>Execute BIST (R)</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>10</td>
<td>AERR# Observation Enabled (R)</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>11</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>BINIT# Observation Enabled (R)</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>13</td>
<td>In Order Queue Depth (R)</td>
<td>1 = 1, 0 = 8</td>
</tr>
<tr>
<td>14</td>
<td>1-MByte Power on Reset Vector (R)</td>
<td>1 = 1MByte, 0 = 4GBytes</td>
</tr>
<tr>
<td>15</td>
<td>FRC Mode Enable (R)</td>
<td>1 = Enabled, 0 = Disabled</td>
</tr>
<tr>
<td>17:16</td>
<td>APIC Cluster ID (R)</td>
<td></td>
</tr>
<tr>
<td>19:18</td>
<td>System Bus Frequency (R)</td>
<td>00 = 66MHz, 10 = 100MHz, 01 = 133MHz, 11 = Reserved</td>
</tr>
<tr>
<td>21:20</td>
<td>Symmetric Arbitration ID (R)</td>
<td></td>
</tr>
<tr>
<td>25:22</td>
<td>Clock Frequency Ratio (R)</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Low Power Mode Enable (R/W)</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>Clock Frequency Ratio</td>
<td></td>
</tr>
<tr>
<td>63:28</td>
<td>Reserved.¹</td>
<td></td>
</tr>
<tr>
<td>33H 51</td>
<td>TEST_CTL</td>
<td>Test Control Register</td>
</tr>
<tr>
<td>29:0</td>
<td>Reserved.</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Streaming Buffer Disable</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Disable LOCK#</td>
<td>Assertion for split locked access.</td>
</tr>
<tr>
<td>79H 121</td>
<td>BIOS_UPDT_TRIG</td>
<td>BIOS Update Trigger Register.</td>
</tr>
<tr>
<td>88H 136</td>
<td>BBL_CR_D0[63:0]</td>
<td>Chunk 0 data register D[63:0]: used to write to and read from the L2</td>
</tr>
<tr>
<td>89H 137</td>
<td>BBL_CR_D1[63:0]</td>
<td>Chunk 1 data register D[63:0]: used to write to and read from the L2</td>
</tr>
<tr>
<td>8AH 138</td>
<td>BBL_CR_D2[63:0]</td>
<td>Chunk 2 data register D[63:0]: used to write to and read from the L2</td>
</tr>
</tbody>
</table>
Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8BH 139</td>
<td>BIOS_SIGN/BBL_CR_D3[63:0]</td>
<td>BIOS Update Signature Register or Chunk 3 data register D[63:0] Used to write to and read from the L2 depending on the usage model.</td>
</tr>
<tr>
<td>C1H 193</td>
<td>PerfCtr0 (PERFCTR0)</td>
<td></td>
</tr>
<tr>
<td>C2H 194</td>
<td>PerfCtr1 (PERFCTR1)</td>
<td></td>
</tr>
<tr>
<td>FEH 254</td>
<td>MTRRcap</td>
<td></td>
</tr>
<tr>
<td>116H 278</td>
<td>BBL_CR_ADDR [63:0]</td>
<td>Address register: used to send specified address (A31-A3) to L2 during cache initialization accesses.</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_ADDR [63:32]</td>
<td>Reserved,</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_ADDR [31:3]</td>
<td>Address bits [35:3]</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_ADDR [2:0]</td>
<td>Reserved Set to 0.</td>
</tr>
<tr>
<td>118H 280</td>
<td>BBL_CR_DECC[63:0]</td>
<td>Data ECC register D[7:0]; used to write ECC and read ECC to/from L2</td>
</tr>
<tr>
<td>119H 281</td>
<td>BBL_CR_CTL</td>
<td>Control register: used to program L2 commands to be issued via cache configuration accesses mechanism. Also receives L2 lookup response</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[63:22]</td>
<td>User supplied ECC</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[21]</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[20:19]</td>
<td>L2 Command</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[18]</td>
<td>Data Read w/ LRU update (RLU)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[17]</td>
<td>Tag Read w/ Data Read (TRR)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[16]</td>
<td>Tag Inquire (TI)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[15:14]</td>
<td>L2 Control Register Read (CR)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[13:12]</td>
<td>L2 Control Register Write (CW)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[11:10]</td>
<td>Tag Write w/ Data Read (TWR)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[9:8]</td>
<td>Tag Write w/ Data Write (TWW)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[7]</td>
<td>Tag Write (Tw)</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[6:5]</td>
<td>State to L2</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_CTL[4:0]</td>
<td>Way to L2</td>
</tr>
<tr>
<td></td>
<td>01100</td>
<td>Way 0 - 00, Way 1 - 01, Way 2 - 10, Way 3 - 11</td>
</tr>
<tr>
<td></td>
<td>01110</td>
<td>Modified - 11, Exclusive - 10, Shared - 01, Invalid - 00</td>
</tr>
<tr>
<td></td>
<td>01111</td>
<td>Way from L2</td>
</tr>
<tr>
<td></td>
<td>00010</td>
<td>State from L2</td>
</tr>
<tr>
<td></td>
<td>00011</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>010 + MESI encode</td>
<td>Reserved</td>
</tr>
<tr>
<td></td>
<td>111 + MESI encode</td>
<td>L2 Hit</td>
</tr>
<tr>
<td></td>
<td>100 + MESI encode</td>
<td>Processor number²</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disable = 1, Enable = 0, Reserved</td>
</tr>
<tr>
<td></td>
<td>11AH 282</td>
<td>Trigger register: used to initiate a cache configuration accesses access, Write only with Data = 0.</td>
</tr>
<tr>
<td></td>
<td>BBL_CR_TRIG</td>
<td>Busy register: indicates when a cache configuration accesses L2 command is in progress. D[0] = 1 = BUSY</td>
</tr>
</tbody>
</table>
### Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>116H 286</td>
<td>BBL_CR_CTL3</td>
<td>Control register 3: used to configure the L2 Cache</td>
</tr>
<tr>
<td>     BBL_CR_CTL3[63:26]</td>
<td>     Reserved</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[25]</td>
<td>     Cache bus fraction (read only)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[24]</td>
<td>     Reserved</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[23]</td>
<td>     L2 Hardware Disable (read only)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[22:20]</td>
<td>     L2 Physical Address Range support</td>
<td></td>
</tr>
<tr>
<td>     111</td>
<td>     64GBytes</td>
<td></td>
</tr>
<tr>
<td>     110</td>
<td>     32GBytes</td>
<td></td>
</tr>
<tr>
<td>     101</td>
<td>     16GBytes</td>
<td></td>
</tr>
<tr>
<td>     100</td>
<td>     8GBytes</td>
<td></td>
</tr>
<tr>
<td>     011</td>
<td>     4GBytes</td>
<td></td>
</tr>
<tr>
<td>     010</td>
<td>     2GBytes</td>
<td></td>
</tr>
<tr>
<td>     001</td>
<td>     1GBytes</td>
<td></td>
</tr>
<tr>
<td>     000</td>
<td>     512MBytes</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[19]</td>
<td>     Reserved</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[18]</td>
<td>     Cache State error checking enable (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[17:13]</td>
<td>     Cache size per bank (read/write)</td>
<td></td>
</tr>
<tr>
<td>     00001</td>
<td>     256KBytes</td>
<td></td>
</tr>
<tr>
<td>     00010</td>
<td>     512KBytes</td>
<td></td>
</tr>
<tr>
<td>     00100</td>
<td>     1MByte</td>
<td></td>
</tr>
<tr>
<td>     01000</td>
<td>     2MByte</td>
<td></td>
</tr>
<tr>
<td>     10000</td>
<td>     4MBytes</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[12:11]</td>
<td>     Number of L2 banks (read only)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[10:9]</td>
<td>     L2 Associativity (read only)</td>
<td></td>
</tr>
<tr>
<td>     0</td>
<td>     Direct Mapped</td>
<td></td>
</tr>
<tr>
<td>     01</td>
<td>     2 Way</td>
<td></td>
</tr>
<tr>
<td>     10</td>
<td>     4 Way</td>
<td></td>
</tr>
<tr>
<td>     11</td>
<td>     Reserved</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[8]</td>
<td>     L2 Enabled (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[7]</td>
<td>     CRTN Parity Check Enable (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[6]</td>
<td>     Address Parity Check Enable (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[5]</td>
<td>     ECC Check Enable (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[4:1]</td>
<td>     L2 Cache Latency (read/write)</td>
<td></td>
</tr>
<tr>
<td>     BBL_CR_CTL3[0]</td>
<td>     L2 Configured (read/write)</td>
<td></td>
</tr>
<tr>
<td>174H 372</td>
<td>SYSENTER_CS_MSR</td>
<td>CS register target for CPL 0 code</td>
</tr>
<tr>
<td>175H 373</td>
<td>SYSENTER_ESP_MSR</td>
<td>Stack pointer for CPL 0 stack</td>
</tr>
<tr>
<td>176H 374</td>
<td>SYSENTER_EIP_MSR</td>
<td>CPL 0 code entry point</td>
</tr>
<tr>
<td>179H 377</td>
<td>MCG_CAP</td>
<td> </td>
</tr>
<tr>
<td>17AH 378</td>
<td>MCG_STATUS</td>
<td> </td>
</tr>
<tr>
<td>Register Address</td>
<td>Register Name</td>
<td>Bit Description</td>
</tr>
<tr>
<td>------------------</td>
<td>------------------------</td>
<td>----------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>17BH 379</td>
<td>MCG_CTL</td>
<td></td>
</tr>
</tbody>
</table>
| 186H 390         | PerfEvtSel0 (EVNTSEL0) | 7:0 Event Select
Refer to Performance Counter section for a list of event encodings. |
|                  |                        | 15:8 UMASK (Unit Mask)
Unit mask register set to 0 to enable all count options. |
|                  |                        | 16 USER
Controls the counting of events at Privilege levels of 1, 2, and 3. |
|                  |                        | 17 OS
Controls the counting of events at Privilege level of 0. |
|                  |                        | 18 E Occurrence/Duration Mode Select
1 = Occurrence
0 = Duration |
|                  |                        | 19 PC
Enabled the signaling of performance counter overflow via BP0 pin |
|                  |                        | 20 INT
Enables the signaling of counter overflow via input to APIC
1 = Enable
0 = Disable |
|                  |                        | 22 ENABLE
Enables the counting of performance events in both counters
1 = Enable
0 = Disable |
|                  |                        | 23 INV
Inverts the result of the CMASK condition
1 = Inverted
0 = Non-Inverted |
|                  |                        | 31:24 CMASK (Counter Mask). |
| 187H 391         | PerfEvtSel1 (EVNTSEL1) | 7:0 Event Select
Refer to Performance Counter section for a list of event encodings. |
|                  |                        | 15:8 UMASK (Unit Mask)
Unit mask register set to 0 to enable all count options. |
### Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hex</td>
<td>Dec</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>USER</td>
<td>Controls the counting of events at Privilege levels of 1, 2, and 3.</td>
</tr>
<tr>
<td>17</td>
<td>OS</td>
<td>Controls the counting of events at Privilege level of 0.</td>
</tr>
<tr>
<td>18</td>
<td>E</td>
<td>Occurrence/Duration Mode Select</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Occurrence</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Duration</td>
</tr>
<tr>
<td>19</td>
<td>PC</td>
<td>Enabled the signaling of performance counter overflow via BPO pin.</td>
</tr>
<tr>
<td>20</td>
<td>INT</td>
<td>Enables the signaling of counter overflow via input to APIC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Disable</td>
</tr>
<tr>
<td>23</td>
<td>INV</td>
<td>Inverts the result of the CMASK condition</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 = Inverted</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 = Non-Inverted</td>
</tr>
<tr>
<td>31:24</td>
<td>CMASK (Counter Mask)</td>
<td></td>
</tr>
<tr>
<td>1D9H 473</td>
<td>DEBUGCTLMSR</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Enable/Disable Last Branch Records</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Branch Trap Flag</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Performance Monitoring/Break Point Pins</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Performance Monitoring/Break Point Pins</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Performance Monitoring/Break Point Pins</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>Performance Monitoring/Break Point Pins</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>Enable/Disable Execution Trace Messages</td>
</tr>
<tr>
<td>31:7</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>1DBH 475</td>
<td>LASTBRANCHFROMIP</td>
<td></td>
</tr>
<tr>
<td>1DCH 476</td>
<td>LASTBRANCHTOIP</td>
<td></td>
</tr>
<tr>
<td>1DH 477</td>
<td>LASTINTFROMIP</td>
<td></td>
</tr>
<tr>
<td>1DEH 478</td>
<td>LASTINTTOIP</td>
<td></td>
</tr>
<tr>
<td>1E0H 480</td>
<td>ROB_CR_BKUPTMPDR6</td>
<td></td>
</tr>
<tr>
<td>1:0</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Fast String Enable bit. Default is enabled</td>
</tr>
<tr>
<td>200H 512</td>
<td>MTRRphysBase0</td>
<td></td>
</tr>
<tr>
<td>201H 513</td>
<td>MTRRphysMask0</td>
<td></td>
</tr>
<tr>
<td>202H 514</td>
<td>MTRRphysBase1</td>
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</tr>
</tbody>
</table>
### Model-Specific Registers (MSRs)

#### Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>203H 515</td>
<td>MTRRphysMask1</td>
<td></td>
</tr>
<tr>
<td>204H 516</td>
<td>MTRRphysBase2</td>
<td></td>
</tr>
<tr>
<td>205H 517</td>
<td>MTRRphysMask2</td>
<td></td>
</tr>
<tr>
<td>206H 518</td>
<td>MTRRphysBase3</td>
<td></td>
</tr>
<tr>
<td>207H 519</td>
<td>MTRRphysMask3</td>
<td></td>
</tr>
<tr>
<td>208H 520</td>
<td>MTRRphysBase4</td>
<td></td>
</tr>
<tr>
<td>209H 521</td>
<td>MTRRphysMask4</td>
<td></td>
</tr>
<tr>
<td>20AH 522</td>
<td>MTRRphysBase5</td>
<td></td>
</tr>
<tr>
<td>20BH 523</td>
<td>MTRRphysMask5</td>
<td></td>
</tr>
<tr>
<td>20CH 524</td>
<td>MTRRphysBase6</td>
<td></td>
</tr>
<tr>
<td>20DH 525</td>
<td>MTRRphysMask6</td>
<td></td>
</tr>
<tr>
<td>20EH 526</td>
<td>MTRRphysBase7</td>
<td></td>
</tr>
<tr>
<td>20FH 527</td>
<td>MTRRphysMask7</td>
<td></td>
</tr>
<tr>
<td>250H 592</td>
<td>MTRRfix64K_00000</td>
<td></td>
</tr>
<tr>
<td>258H 600</td>
<td>MTRRfix16K_80000</td>
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</tr>
<tr>
<td>259H 601</td>
<td>MTRRfix16K_A0000</td>
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</tr>
<tr>
<td>268H 616</td>
<td>MTRRfix4K_C0000</td>
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</tr>
<tr>
<td>269H 617</td>
<td>MTRRfix4K_C8000</td>
<td></td>
</tr>
<tr>
<td>26AH 618</td>
<td>MTRRfix4K_D0000</td>
<td></td>
</tr>
<tr>
<td>26BH 619</td>
<td>MTRRfix4K_D8000</td>
<td></td>
</tr>
<tr>
<td>26CH 620</td>
<td>MTRRfix4K_E0000</td>
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</tr>
<tr>
<td>26DH 621</td>
<td>MTRRfix4K_E8000</td>
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</tr>
<tr>
<td>26EH 622</td>
<td>MTRRfix4K_F0000</td>
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</tr>
<tr>
<td>26FH 623</td>
<td>MTRRfix4K_F8000</td>
<td></td>
</tr>
<tr>
<td>2FFH 767</td>
<td>MTRRdefType</td>
<td>2:0 Default memory type</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>MTRRdefType</td>
<td>10 Fixed MTRR enable</td>
</tr>
<tr>
<td>2FFH 767</td>
<td>MTRRdefType</td>
<td>11 MTRR Enable</td>
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<tr>
<td>400H 1024</td>
<td>MC0_CTL</td>
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</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>15:0 MC_STATUS_MCACOD</td>
</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>31:16 MC_STATUS_MSCOD</td>
</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>57 MC_STATUS_DAM</td>
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<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>58 MC_STATUS_ADDRV</td>
</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>59 MC_STATUS_MISCV</td>
</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>60 MC_STATUS_EN. (Note: For MC0_STATUS only, this bit is hardcoded to 1.)</td>
</tr>
<tr>
<td>401H 1025</td>
<td>MC0_STATUS</td>
<td>61 MC_STATUS_UC</td>
</tr>
</tbody>
</table>
The following MSRs are defined for the Pentium processors. The P5_MC_ADDR, P5_MC_TYPE, and TSC MSRs (named IA32_P5_MC_ADDR, IA32_P5_MC_TYPE, and IA32_TIME_STAMP_COUNTER in the Pentium 4 processor) are architectural; that is, code that accesses these registers will run on Pentium 4 and P6 family processors without generating exceptions (see Section 35.1, "Architectural MSRs"). The CESR, CTR0, and CTR1 MSRs are unique to

### Table 35-41. MSRs in the P6 Family Processors (Contd.)

<table>
<thead>
<tr>
<th>Register Address</th>
<th>Register Name</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>62 63</td>
<td>MC_STATUS_0, MC_STATUS_V</td>
<td></td>
</tr>
<tr>
<td>402H 1026</td>
<td>MC0_ADDR</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
</tr>
<tr>
<td>403H 1027</td>
<td>MC0_MISC</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
</tr>
<tr>
<td>404H 1028</td>
<td>MC1_CTL</td>
<td></td>
</tr>
<tr>
<td>405H 1029</td>
<td>MC1_STATUS</td>
<td>Bit definitions same as MC0_STATUS.</td>
</tr>
<tr>
<td>406H 1030</td>
<td>MC1_ADDR</td>
<td></td>
</tr>
<tr>
<td>407H 1031</td>
<td>MC1_MISC</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
</tr>
<tr>
<td>408H 1032</td>
<td>MC2_CTL</td>
<td></td>
</tr>
<tr>
<td>409H 1033</td>
<td>MC2_STATUS</td>
<td>Bit definitions same as MC0_STATUS.</td>
</tr>
<tr>
<td>40AH 1034</td>
<td>MC2_ADDR</td>
<td></td>
</tr>
<tr>
<td>40BH 1035</td>
<td>MC2_MISC</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
</tr>
<tr>
<td>40CH 1036</td>
<td>MC4_CTL</td>
<td>Bit definitions same as MC0_STATUS, except bits 0, 4, 57, and 61 are hardcoded to 1.</td>
</tr>
<tr>
<td>40DH 1037</td>
<td>MC4_STATUS</td>
<td>Defined in MCA architecture but not implemented in P6 Family processors.</td>
</tr>
<tr>
<td>40EH 1038</td>
<td>MC4_ADDR</td>
<td>Defined in MCA architecture but not implemented in P6 Family processors.</td>
</tr>
<tr>
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<td>MC4_MISC</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
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<tr>
<td>410H 1040</td>
<td>MC3_CTL</td>
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<td>411H 1041</td>
<td>MC3_STATUS</td>
<td>Bit definitions same as MC0_STATUS.</td>
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<tr>
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<td>MC3_ADDR</td>
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</tr>
<tr>
<td>413H 1043</td>
<td>MC3_MISC</td>
<td>Defined in MCA architecture but not implemented in the P6 family processors.</td>
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</table>

### NOTES

1. Bit 0 of this register has been redefined several times, and is no longer used in P6 family processors.
2. The processor number feature may be disabled by setting bit 21 of the BBL_CR_CTL MSR (model-specific register address 119h) to “1”. Once set, bit 21 of the BBL_CR_CTL may not be cleared. This bit is write-once. The processor number feature will be disabled until the processor is reset.
3. The Pentium III processor will prevent FSB frequency overclocking with a new shutdown mechanism. If the FSB frequency selected is greater than the internal FSB frequency the processor will shutdown. If the FSB selected is less than the internal FSB frequency the BIOS may choose to use bit 11 to implement its own shutdown policy.

### 35.20 MSRS IN PENTIUM PROCESSORS

The following MSRs are defined for the Pentium processors. The P5_MC_ADDR, P5_MC_TYPE, and TSC MSRs (named IA32_P5_MC_ADDR, IA32_P5_MC_TYPE, and IA32_TIME_STAMP_COUNTER in the Pentium 4 processor) are architectural; that is, code that accesses these registers will run on Pentium 4 and P6 family processors without generating exceptions (see Section 35.1, "Architectural MSRs"). The CESR, CTR0, and CTR1 MSRs are unique to
Pentium processors; code that accesses these registers will generate exceptions on Pentium 4 and P6 family processors.

### Table 35-42. MSRs in the Pentium Processor

<table>
<thead>
<tr>
<th>Register Address</th>
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<th>Hex</th>
<th>Dec</th>
<th>Bit Description</th>
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</thead>
<tbody>
<tr>
<td>0H</td>
<td>P5_MC_ADDR</td>
<td>0</td>
<td>1</td>
<td>See Section 15.10.2, “Pentium Processor Machine-Check Exception Handling.”</td>
</tr>
<tr>
<td>1H</td>
<td>P5_MC_TYPE</td>
<td>1</td>
<td>16</td>
<td>See Section 15.10.2, “Pentium Processor Machine-Check Exception Handling.”</td>
</tr>
<tr>
<td>10H</td>
<td>TSC</td>
<td>16</td>
<td>16</td>
<td>See Section 17.14, “Time-Stamp Counter.”</td>
</tr>
<tr>
<td>11H</td>
<td>CESR</td>
<td>17</td>
<td>17</td>
<td>See Section 18.20.1, “Control and Event Select Register (CESR).”</td>
</tr>
<tr>
<td>12H</td>
<td>CTR0</td>
<td>18</td>
<td>18</td>
<td>Section 18.20.3, “Events Counted.”</td>
</tr>
<tr>
<td>13H</td>
<td>CTR1</td>
<td>19</td>
<td>19</td>
<td>Section 18.20.3, “Events Counted.”</td>
</tr>
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</table>
### 35.21 MSR INDEX

MSRs of recent processors are indexed here for convenience. IA32 MSRs are excluded from this index.

<table>
<thead>
<tr>
<th>MSR Name and CPUID DisplayFamily_DisplayModel</th>
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<tr>
<td>MSR_ALF_ESCRO 0FH</td>
<td>See Table 35-36</td>
</tr>
<tr>
<td>MSR_ALF_ESCR1 0FH</td>
<td>See Table 35-36</td>
</tr>
<tr>
<td>MSR_ANY_CORE_C0 06_4EH, 06_5EH</td>
<td>See Table 35-34</td>
</tr>
<tr>
<td>MSR_ANY_GFXE_C0 06_4EH, 06_5EH</td>
<td>See Table 35-34</td>
</tr>
<tr>
<td>MSR_B0_PMON_BOX_CTRL 06_2EH</td>
<td>See Table 35-13</td>
</tr>
<tr>
<td>MSR_B0_PMON_BOX_OVF_CTRL 06_2EH</td>
<td>See Table 35-13</td>
</tr>
<tr>
<td>MSR_B0_PMON_BOX_STATUS 06_2EH</td>
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</tr>
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<td>MSR_B0_PMON_MASK 06_2EH</td>
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<td>MSR_B0_PMON_MATCH 06_2EH</td>
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<tr>
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<td>MSR_B1_PMON_BOX_OVF_CTRL 06_2EH</td>
<td>See Table 35-13</td>
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<tr>
<td>MSR Name and CPUID DisplayFamily_DisplayModel</td>
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</table>
### Model-Specific Registers (MSRs)

A table shows MSR names, CPUID display family and model numbers, and locations.

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<thead>
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<th>Location</th>
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<td>MSR_CO_PMON_CTR3</td>
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<td>MSR_C1_PMON_BOX_CTRL</td>
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</tr>
<tr>
<td>MSR_C1_PMON_BOX_FILTER</td>
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See Table 35-19
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See Table 35-19
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See Table 35-19
See Table 35-28
<table>
<thead>
<tr>
<th>MSR Name and CPUID DisplayFamily_DisplayModel</th>
<th>Location</th>
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<td>MSR Name and CPUID DisplayFamily_DisplayModel</td>
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## MODEL-SPECIFIC REGISTERS (MSRS)

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### MODEL-SPECIFIC REGISTERS (MSRs)

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## MODEL-SPECIFIC REGISTERS (MSRS)

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### Model-Specific Registers (MSRs)

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Note: MSR addresses are shown in hexadecimal format (e.g., `06_3EH`).
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### Model-Specific Registers (MSRs)

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## MODEL-SPECIFIC REGISTERS (MSRs)

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<td>06_1AH, 06_1EH, 06_1FH, 06_25H, 06_2CH .................................................. See Table 35-12</td>
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<td>MSR_UNCORE_PMC5</td>
<td>06_1AH, 06_1EH, 06_1FH, 06_25H, 06_2CH .................................................. See Table 35-12</td>
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<tr>
<td>MSR_UNCORE_PMC6</td>
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<tr>
<td>MSR_UNCORE_PMC7</td>
<td>06_1AH, 06_1EH, 06_1FH, 06_25H, 06_2CH .................................................. See Table 35-12</td>
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<td>MSR_UNCORE_PRMRR_BASE</td>
<td>06_4EH, 06_5EH .............................................................. See Table 35-34</td>
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<td>MSR_UNCORE_PRMRR_MASK</td>
<td>06_4EH, 06_5EH .............................................................. See Table 35-34</td>
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<td>MSR_W_PMON_BOX_OVF_CTRL</td>
<td>06_2EH .............................................................. See Table 35-13</td>
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<tr>
<td>MSR_W_PMON_BOX_STATUS</td>
<td>06_2EH .............................................................. See Table 35-13</td>
</tr>
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<td>06_2EH .............................................................. See Table 35-13</td>
</tr>
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<td>MSR_W_PMON_CTR1</td>
<td>06_2EH .............................................................. See Table 35-13</td>
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<td>MSR_W_PMON_CTR2</td>
<td>06_2EH .............................................................. See Table 35-13</td>
</tr>
<tr>
<td>MSR_W_PMON_CTR3</td>
<td>06_2EH .............................................................. See Table 35-13</td>
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<tr>
<td>MSR_W_PMON_EVNT_SEL0</td>
<td>06_2EH .............................................................. See Table 35-13</td>
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<tr>
<td>MSR_W_PMON_EVNT_SEL1</td>
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### Model-Specific Registers (MSRs)

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<thead>
<tr>
<th>MSR Name and CPUID Display</th>
<th>Family</th>
<th>Model</th>
<th>Location</th>
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<td>MSR_W_PMON_EVENT_SEL3</td>
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<tr>
<td>MTRRfix16K_80000</td>
<td>P6</td>
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<tr>
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<td>See Table 35-39, Table 35-41</td>
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<td>P6</td>
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<td>See Table 35-39, Table 35-41</td>
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<td>P6</td>
<td></td>
<td>See Table 35-39, Table 35-41</td>
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<td>See Table 35-39, Table 35-41</td>
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<td>MTRRfix4K_F0000</td>
<td>P6</td>
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<td>See Table 35-39, Table 35-41</td>
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<td>P6</td>
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<td>See Table 35-39, Table 35-41</td>
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<tr>
<td>MSR Name</td>
<td>CPUID DisplayFamily_DisplayModel</td>
<td>Location</td>
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<td>MTRRphysBase1</td>
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<td></td>
</tr>
<tr>
<td>MTRRphysBase2</td>
<td>06_0EH</td>
<td>See Table 35-41</td>
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<td>MTRRphysBase3</td>
<td>06_0EH</td>
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<tr>
<td>MTRRphysBase4</td>
<td>06_0EH</td>
<td>See Table 35-41</td>
<td></td>
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<tr>
<td>MTRRphysBase5</td>
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</tr>
<tr>
<td>MTRRphysBase6</td>
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<td>See Table 35-41</td>
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<td>06_0EH</td>
<td>See Table 35-41</td>
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<tr>
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<td>06_0EH</td>
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<td>06_0EH</td>
<td>See Table 35-41</td>
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<tr>
<td>MTRRphysMask3</td>
<td>06_0EH</td>
<td>See Table 35-41</td>
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</tr>
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<td>MTRRphysMask4</td>
<td>06_0EH</td>
<td>See Table 35-41</td>
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</tr>
<tr>
<td>MSR Name and CPUID DisplayFamily_DisplayModel</td>
<td>Location</td>
<td></td>
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<td>See Table 35-39</td>
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<td>P6 Family ...........................................</td>
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<td></td>
</tr>
<tr>
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<tr>
<td>06_0EH ..............................................</td>
<td>See Table 35-39</td>
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<td>P6 Family ...........................................</td>
<td>See Table 35-41</td>
<td></td>
<td></td>
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<td>See Table 35-39</td>
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<td>P6 Family ...........................................</td>
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<td></td>
</tr>
<tr>
<td>P6 Family ...........................................</td>
<td>See Table 35-41</td>
<td></td>
<td></td>
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</table>
36.1 OVERVIEW

Intel® Processor Trace (Intel® PT) is an extension of Intel® Architecture that captures information about software execution using dedicated hardware facilities that cause only minimal performance perturbation to the software being traced. This information is collected in data packets. The initial implementations of Intel PT offer control flow tracing, which generates a variety of packets to be processed by a software decoder. The packets include timing, program flow information (e.g. branch targets, branch taken/not taken indications) and program-induced mode related information (e.g. Intel TSX state transitions, CR3 changes). These packets may be buffered internally before being sent to the memory subsystem or other output mechanism available in the platform. Debug software can process the trace data and reconstruct the program flow.

36.1.1 Features and Capabilities

Intel PT’s control flow trace generates a variety of packets that, when combined with the binaries of a program by a post-processing tool, can be used to produce an exact execution trace. The packets record flow information such as instruction pointers (IP), indirect branch targets, and directions of conditional branches within contiguous code regions (basic blocks).

In addition, the packets record other contextual, timing, and bookkeeping information that enables both functional and performance debugging of applications. Intel PT has several control and filtering capabilities available to customize the tracing information collected and to append other processor state and timing information to enable debugging. For example, there are modes that allow packets to be filtered based on the current privilege level (CPL) or the value of CR3.

Configuration of the packet generation and filtering capabilities are programmed via a set of MSRs. The MSRs generally follow the naming convention of IA32_RTIT_*. The capability provided by these configuration MSRs are enumerated by CPUID, see Section 36.3. Details of the MSRs for configuring Intel PT are described in Section 36.2.5.

36.1.1.1 Packet Summary

After a tracing tool has enabled and configured the appropriate MSRs, the processor will collect and generate trace information in the following categories of packets (for more details on the packets, see Section 36.4):

- Packets about basic information on program execution: These include:
  - Packet Stream Boundary (PSB) packets: PSB packets act as ‘heartbeats’ that are generated at regular intervals (e.g., every 4K trace packet bytes). These packets allow the packet decoder to find the packet boundaries within the output data stream; a PSB packet should be the first packet that a decoder looks for when beginning to decode a trace.
  - Paging Information Packet (PIP): PIPs record modifications made to the CR3 register. This information, along with information from the operating system on the CR3 value of each process, allows the debugger to attribute linear addresses to their correct application source.
  - Time-Stamp Counter (TSC) packets: TSC packets aid in tracking wall-clock time, and contain some portion of the software-visible time-stamp counter.
  - Core Bus Ratio (CBR) packets: CBR packets contain the core:bus clock ratio.
  - Overflow (OVF) packets: OVF packets are sent when the processor experiences an internal buffer overflow, resulting in packets being dropped. This packet notifies the decoder of the loss and can help the decoder to respond to this situation.

- Packets about control flow information:
  - Taken Not-Taken (TNT) packets: TNT packets track the “direction” of direct conditional branches (taken or not taken).
— **Target IP (TIP)** packets: TIP packets record the target IP of indirect branches, exceptions, interrupts, and other branches or events. These packets can contain the IP, although that IP value may be compressed by eliminating upper bytes that match the last IP. There are various types of TIP packets; they are covered in more detail in Section 36.4.2.2.

— **Flow Update Packets (FUP)**: FUPs provide the source IP addresses for asynchronous events (interrupt and exceptions), as well as other cases where the source address cannot be determined from the binary.

— **MODE** packets: These packets provide the decoder with important processor execution information so that it can properly interpret the dis-assembled binary and trace log. MODE packets have a variety of formats that indicate details such as the execution mode (16-bit, 32-bit, or 64-bit).

### 36.2 INTEL® PROCESSOR TRACE OPERATIONAL MODEL

This section describes the overall Intel Processor Trace mechanism and the essential concepts relevant to how it operates.

#### 36.2.1 Change of Flow Instruction (COFI) Tracing

A basic program block is a section of code where no jumps or branches occur. The instruction pointers (IPs) in this block of code need not be traced, as the processor will execute them from start to end without redirecting code flow. Instructions such as branches, and events such as exceptions or interrupts, can change the program flow. These instructions and events that change program flow are called Change of Flow Instructions (COFI). There are three categories of COFI:

- Direct transfer COFI.
- Indirect transfer COFI.
- Far transfer COFI.

The following subsections describe the COFI events that result in trace packet generation. Table 36-1 lists branch instruction by COFI types. For detailed description of specific instructions, see *Intel® 64 and IA-32 Architectures Software Developer’s Manual*.

<table>
<thead>
<tr>
<th>COFI Type</th>
<th>Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conditional Branch</td>
<td>JA, JAE, JB, JBE, JC, JCXZ&lt; JECXZ, JRCXZ, JE, JG, JGE, JL, JLE, JNA, JNBE,</td>
</tr>
<tr>
<td></td>
<td>JNB, JNC, JNE, JNG, JNGE, JNL, JNLE, JNO, JNP, JNS, JNZ, J0, JP, JPE, JPO,</td>
</tr>
<tr>
<td></td>
<td>JS, JZ, LOOP, LOOPE, LOOPNE, LOOPNZ, LOOPZ</td>
</tr>
<tr>
<td>Unconditional Direct Branch</td>
<td>JMP (E9 xx, EB xx), CALL (E8 xx)</td>
</tr>
<tr>
<td>Indirect Branch</td>
<td>JMP (FF /4), CALL (FF /2)</td>
</tr>
<tr>
<td>Near Ret</td>
<td>RET (C3, C2 xx)</td>
</tr>
<tr>
<td>Far Transfers</td>
<td>INT3, INTn, INTO, IRET, IRETQ, INT, JMP (EA xx, FF /5), CALL (9A xx, FF /3),</td>
</tr>
<tr>
<td></td>
<td>RET (CB, CA xx), SYSCALL, SYSRET, SYSEXIT, VMLAUNCH, VMRESUME</td>
</tr>
</tbody>
</table>

#### 36.2.1.1 Direct Transfer COFI

Direct Transfer COFI are relative branches. This means that their target is an IP whose offset from the current IP is embedded in the instruction bytes. It is not necessary to indicate target of these instructions in the trace output since it can be obtained through the source disassembly. Conditional branches need to indicate only whether the branch is taken or not. Unconditional branches do not need any recording in the trace output. There are two sub-categories:

- **Conditional Branch (Jcc, J*CXZ) and LOOP**

  To track this type of instruction, the processor encodes a single bit (taken or not taken — TNT) to indicate the program flow after the instruction.
Jcc, J*CXZ, and LOOP can be traced with TNT bits. To improve the trace packet output efficiency, the processor will compact several TNT bits into a single packet.

- **Unconditional Direct Jumps**
  
  There is no trace output required for direct unconditional jumps (like JMP near relative or CALL near relative) since they can be directly inferred from the application assembly. Direct unconditional jumps do not generate a TNT bit or a Target IP packet, though TIP.PGD and TIP.PGE packets can be generated by unconditional direct jumps that toggle Intel PT enables (see Section 36.2.3).

### 36.2.1.2 Indirect Transfer COFI

Indirect transfer instructions involve updating the IP from a register or memory location. Since the register or memory contents can vary at any time during execution, there is no way to know the target of the indirect transfer until the register or memory contents are read. As a result, the disassembled code is not sufficient to determine the target of this type of COFI. Therefore, tracing hardware must send out the destination IP in the trace packet for debug software to determine the target address of the COFI. Note that this IP may be a linear or effective address (see Section 36.3.1.1).

An indirect transfer instruction generates a Target IP Packet (TIP) that contains the target address of the branch. There are two sub-categories:

- **Near JMP Indirect and Near Call Indirect**
  
  As previously mentioned, the target of an indirect COFI resides in the contents of either a register or memory location. Therefore, the processor must generate a packet that includes this target address to allow the decoder to determine the program flow.

- **Near RET**
  
  When a CALL instruction executes, it pushes onto the stack the address of the next instruction following the CALL. Upon completion of the call procedure, the RET instruction is often used to pop the return address off of the call stack and redirect code flow back to the instruction following the CALL.

  A RET instruction simply transfers program flow to the address it popped off the stack. Because a called procedure may change the return address on the stack before executing the RET instruction, debug software can be misled if it assumes that code flow will return to the instruction following the last CALL. Therefore, even for near RET, a Target IP Packet may be sent.

  — **RET Compression**
  
  A special case is applied if the target of the RET is consistent with what would be expected from tracking the CALL stack. If it is assured that the decoder has seen the corresponding CALL (with “corresponding” defined as the CALL with matching stack depth), and the RET target is the instruction after that CALL, the RET target may be “compressed”. In this case, only a single TNT bit of “taken” is generated instead of a Target IP Packet. To ensure that the decoder will not be confused in cases of RET compression, only RETs that correspond to CALLs which have been seen since the last PSB packet may be compressed in a given logical processor. For details, see "Indirect Transfer Compression for Returns (RET)” in Section 36.4.2.2.

### 36.2.1.3 Far Transfer COFI

All operations that change the instruction pointer and are not near jumps are “far transfers”. This includes exceptions, interrupts, traps, TSX aborts, and instructions that do far transfers.

All far transfers will produce a Target IP (TIP) packet, which provides the destination IP address. For those far transfers that cannot be inferred from the binary source (e.g., asynchronous events such as exceptions and interrupts), the TIP will be preceded by a Flow Update packet (FUP), which provides the source IP address at which the event was taken. Table 36-25 indicates exactly which IP will be included in the FUP generated by a far transfer.

### 36.2.2 Trace Filtering

Intel Processor Trace provides filtering capabilities, by which the debug/profile tool can control what code is traced.
36.2.2.1 Filtering by Current Privilege Level (CPL)

Intel PT provides the ability to configure a logical processor to generate trace packets only when CPL = 0, when CPL > 0, or regardless of CPL.

CPL filtering ensures that no IPs or other architectural state information associated with the filtered CPL can be seen in the log. For example, if the processor is configured to trace only when CPL > 0, and software executes SYSCALL (changing the CPL to 0), the destination IP of the SYSCALL will be suppressed from the generated packet (see the discussion of TIP.PGD in Section 36.4.2.5).

It should be noted that CPL is always 0 in real-address mode and that CPL is always 3 in virtual-8086 mode. To trace code in these modes, filtering should be configured accordingly.

When software is executing in a non-enabled CPL, ContextEn is cleared. See Section 36.2.3.1 for details.

36.2.2.2 Filtering by CR3

Intel PT supports a CR3-filtering mechanism by which the generation of packets containing architectural states can be enabled or disabled based on the value of CR3. A debugger can use CR3 filtering to trace only a single application without context switching the state of the RTIT MSRs. For the reconstruction of traces from software with multiple threads, debug software may wish to context-switch for the state of the RTIT MSRs (if the operating system does not provide context-switch support) to separate the output for the different threads (see Section 36.3.5, "Context Switch Consideration").

To trace for only a single CR3 value, software can write that value to the IA32_RTIT_CR3_MATCH MSR, and set IA32_RTIT_CTL.CR3Filter. When CR3 value does not match IA32_RTIT_CR3_MATCH and IA32_RTIT_CTL.CR3Filter is 1, ContextEn is forced to 0, and packets containing architectural states will not be generated. Some other packets can be generated when ContextEn is 0; see Section 36.2.3.3 for details. When CR3 does match IA32_RTIT_CR3_MATCH (or when IA32_RTIT_CTL.CR3Filter is 0), CR3 filtering does not force ContextEn to 0 (although it could be 0 due to other filters or modes).

CR3 matches IA32_RTIT_CR3_MATCH if the two registers are identical for bits 63:12, or 63:5 when in PAE paging mode; the lower 5 bits of CR3 and IA32_RTIT_CR3_MATCH are ignored. CR3 filtering is independent of the value of CR0.PG.

When CR3 filtering is in use, PIP packets may still be seen in the log if the processor is configured to trace when CPL = 0 (IA32_RTIT_CTL.OS = 1). If not, no PIP packets will be seen.

36.2.2.3 Filtering by IP

Trace packet generation with configurable filtering by IP is supported if CPUID.(EAX=14H, ECX=0):EBX[bit 2] = 1. Intel PT can be configured to enable the generation of packets containing architectural states only when the processor is executing code within certain IP ranges. If the IP is outside of these ranges, generation of some packets is blocked.

IP filtering is enabled using the ADDRx_CFG fields in the IA32_RTIT_CTL MSR (Section 36.2.5.2), where the digit 'n' is a zero-based number that selects which address range is being configured. Each ADDRx_CFG field configures the use of the register pair IA32_RTIT_ADDRx_A and IA32_RTIT_ADDRx_B (Section 36.2.5.5).

IA32_RTIT_ADDRx_A defines the base and IA32_RTIT_ADDRx_B specifies the limit of the range in which tracing is enabled. Thus each range, referred to as the ADDRx range, is defined by [IA32_RTIT_ADDRx_A, IA32_RTIT_ADDRx_B]. There can be multiple such ranges, software can query CPUID (Section 36.3.1) for the number of ranges supported on a processor.

Default behavior (ADDRx_CFG=0) defines no IP filter range, meaning FilterEn is always set. In this case code at any IP can be traced, though other filters, such as CR3 or CPL, could limit tracing. When ADDRx_CFG is set to enable IP filtering (see Section 36.3.1), tracing will commence when a taken branch or event is seen whose target address is in the ADDRx range.

While inside a tracing region and with FilterEn is set, leaving the tracing region may only be detected once a taken branch or event with a target outside the range is retired. If an ADDRx range is entered or exited by executing the next sequential instruction, rather than by a control flow transfer, FilterEn may not toggle immediately. See Section 36.2.3.5 for more details on FilterEn.

Note that these address range base and limit values are inclusive, such that the range includes the first and last instruction whose first instruction byte is in the ADDRx range.
Depending upon processor implementation, IP filtering may be based on linear or effective address. This can cause different behavior between implementations if CSbase is not equal to zero or in real mode. See Section 36.3.1.1 for details. Software can query CPUID to determine filters are based on linear or effective address (Section 36.3.1). Note that some packets, such as MTC (Section 36.3.7) and other timing packets, do not depend on FilterEn. For details on which packets depend on FilterEn, and hence are impacted by IP filtering, see Section 36.4.1.

**TraceStop**

The ADDRn ranges can also be configured to cause tracing to be disabled upon entry to the specified region. This is intended for cases where unexpected code is executed, and the user wishes to immediately stop generating packets in order to avoid overwriting previously written packets.

The TraceStop mechanism works much the same way that IP filtering does, and uses the same address comparison logic. The TraceStop region base and limit values are programmed into one or more ADDRn ranges, but IA32_RTIT_CTL.ADDRn_CFG is configured with the TraceStop encoding. Like FilterEn, TraceStop is detected when a taken branch or event lands in a TraceStop region.

Further, TraceStop requires that TriggerEn=1 at the beginning of the branch/event, and ContextEn=1 upon completion of the branch/event. When this happens, the CPU will set IA32_RTIT_STATUS.Stopped, thereby clearing TriggerEn and hence disabling packet generation. This may generate a TIP.PGD packet with the target IP of the branch or event that entered the TraceStop region. Finally, a TraceStop packet will be inserted, to indicate that the condition was hit.

If a TraceStop condition is encountered during buffer overflow (Section 36.3.8), it will not be dropped, but will instead be signaled once the overflow has resolved.

Note that a TraceStop event does not guarantee that all internally buffered packets are flushed out of internal buffers. To ensure that this has occurred, the user should clear TraceEn.

To resume tracing after a TraceStop event, the user must first disable Intel PT by clearing IA32_RTIT_CTL.TraceEn before the IA32_RTIT_STATUS.Stopped bit can be cleared. At this point Intel PT can be reconfigured, and tracing resumed.

Note that the IA32_RTIT_STATUS.Stopped bit can also be set using the ToPA STOP bit. See Section 36.2.4.2.

**IP Filtering Example**

The following table gives an example of IP filtering behavior. Assume that IA32_RTIT_ADDRn_A = the IP of RangeBase, and that IA32_RTIT_ADDRn_B = the IP of RangeLimit, while IA32_RTIT_CTL.ADDRn_CFG = 0x1 (enable ADDRn range as a FilterEn range).

<table>
<thead>
<tr>
<th>Code Flow</th>
<th>Packets</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bar:</td>
<td>TIP.PGE(RangeBase)</td>
</tr>
<tr>
<td>jmp RangeBase // jump into filter range</td>
<td>TNT(0)</td>
</tr>
<tr>
<td>RangeBase:</td>
<td>TIP.PGD(RangeLimit+1)</td>
</tr>
<tr>
<td>jcc Foo // not taken</td>
<td></td>
</tr>
<tr>
<td>add eax, 1</td>
<td></td>
</tr>
<tr>
<td>Foo:</td>
<td></td>
</tr>
<tr>
<td>jmp RangeLimit+1 // jump out of filter range</td>
<td></td>
</tr>
<tr>
<td>RangeLimit:</td>
<td></td>
</tr>
<tr>
<td>nop</td>
<td></td>
</tr>
<tr>
<td>jcc Bar</td>
<td></td>
</tr>
</tbody>
</table>

**IP Filtering and TraceStop**

It is possible for the user to configure IP filter range(s) and TraceStop range(s) that overlap. In this case, code executing in the non-overlapping portion of either range will behave as would be expected from that range. Code executing in the overlapping range will get TraceStop behavior.
### 36.2.3 Packet Generation Enable Controls

Intel Processor Trace includes a variety of controls that determine whether a packet is generated. In general, most packets are sent only if Packet Enable (`PacketEn`) is set. PacketEn is an internal state maintained in hardware in response to software configurable enable controls, PacketEn is not visible to software directly. The relationship of PacketEn to the software-visible controls in the configuration MSRs is described in this section.

#### 36.2.3.1 Packet Enable (`PacketEn`)

When `PacketEn` is set, the processor is in the mode that Intel PT is monitoring and all packets can be generated to log what is being executed. `PacketEn` is composed of other states according to this relationship:

```
PacketEn ← TriggerEn AND ContextEn AND FilterEn AND BranchEn
```

These constituent controls are detailed in the following subsections.

`PacketEn` ultimately determines when the processor is tracing. When `PacketEn` is set, all control flow packets are enabled. When `PacketEn` is clear, no control flow packets are generated, though other packets (timing and bookkeeping packets) may still be sent. See Section 36.2.4 for details of `PacketEn` and packet generation.

Note that, on processors that do not support IP filtering (i.e., CPUID.(EAX=14H, ECX=0):EBX.IPFLT_WRSTPRSV[bit 2] = 0), `FilterEn` is treated as always set.

#### 36.2.3.2 Trigger Enable (`TriggerEn`)

`Trigger Enable (TriggerEn)` is the primary indicator that trace packet generation is active. `TriggerEn` is set when IA32_RTIT_CTL.TraceEn is set, and cleared by any of the following conditions:

- TraceEn is cleared by software,
- A TraceStop condition is encountered and IA32_RTIT_STATUS.Stopped is set,
- IA32_RTIT_STATUS.Error is set due to an operational error (see Section 36.3.9).

Software can discover the current `TriggerEn` value by reading the IA32_RTIT_STATUS.TriggerEn bit. When `TriggerEn` is clear, tracing is inactive and no packets are generated.

#### 36.2.3.3 Context Enable (`ContextEn`)

`Context Enable (ContextEn)` indicates whether the processor is in the state or mode that software configured hardware to trace. For example, if execution with CPL = 0 code is not being traced (IA32_RTIT_CTL.OS = 0), then `ContextEn` will be 0 when the processor is in CPL0.

Software can discover the current `ContextEn` value by reading the IA32_RTIT_STATUS.ContextEn bit. `ContextEn` is defined as follows:

```
ContextEn = !((IA32_RTIT_CTL.OS = 0 AND CPL = 0) OR (IA32_RTIT_CTL.USER = 0 AND CPL > 0) OR (IS_IN_A_PRODUCTION_ENCLAVE1) OR (IA32_RTIT_CTL.CR3Filter = 1 AND IA32_RTIT_CR3_MATCH does not match CR3))
```

If the clearing of `ContextEn` causes `PacketEn` to be cleared, a Packet Generation Disable (TIP.PGD) packet is generated, but its IP payload is suppressed. If the setting of `ContextEn` causes `PacketEn` to be set, a Packet Generation Enable (TIP.PGE) packet is generated.

When `ContextEn` is 0, control flow packets (TNT, FUP, TIP.*, MODE.*) are not generated, and no Linear Instruction Pointers (LIPs) are exposed. However, some packets, such as MTC and PSB (see Section 36.4.2.16 and Section 36.4.2.17), may still be generated while `ContextEn` is 0. For details of which packets are generated only when `ContextEn` is set, see Section 36.4.1.

The processor does not update `ContextEn` when `TriggerEn` = 0.

The value of `ContextEn` will toggle only when `TriggerEn` = 1.

---

1. Trace packets generation is disabled in a production enclave, see Section 36.2.6.3. See Intel® Software Guard Extensions Programming Reference about differences between a production enclave and a debug enclave.
36.2.3.4 Branch Enable (BranchEn)

This value is based purely on the IA32_RTIT_CTL.BranchEn value. If BranchEn is not set, then relevant COFI packets (TNT, TIP*, FUP, MODE.*) are suppressed. Other packets related to timing (TSC, TMA, MTC, CYC), as well as PSB, will be generated normally regardless. Further, PIP and VMCS continue to be generated, as indicators of what software is running.

36.2.3.5 Filter Enable (FilterEn)

Filter Enable indicates that the Instruction Pointer (IP) is within the range of IPs that Intel PT is configured to watch. Software can get the state of Filter Enable by a RDMSR of IA32_RTIT_STATUS.FilterEn. For details on configuration and use of IP filtering, see Section 36.2.2.3.

On clearing of FilterEn that also clears PacketEn, a Packet Generation Disable (TIP.PGD) will be generated, but unlike the ContextEn case, the IP payload may not be suppressed. For direct, unconditional branches, as well as for indirect branches (including RETs), the PGD generated by leaving the tracing region and clearing FilterEn will contain the target IP. This means that IPs from outside the configured range can be exposed in the trace, as long as they are within context.

When FilterEn is 0, control flow packets are not generated (e.g., TNT, TIP). However, some packets, such as PIP, MTC, and PSB, may still be generated while FilterEn is clear. For details on packet enable dependencies, see Section 36.4.1.

After TraceEn is set, FilterEn is set to 1 at all times if there is no IP filter range configured by software (IA32_RTIT_CTL.ADDRn_CFG != 1, for all n), or if the processor does not support IP filtering (i.e., CPUID.(EAX=14H, ECX=0):EBX.IPFILT_WRSTPRSV[bit 2] = 0). FilterEn will toggle only when TraceEn=1 and ContextEn=1, and when at least one range is configured for IP filtering.

36.2.4 Trace Output

Intel PT output should be viewed independently from trace content and filtering mechanisms. The options available for trace output can vary across processor generations and platforms.

Trace output is written out using one of the following output schemes, as configured by the ToPA and FabricEn bit fields of IA32_RTIT_CTL (see Section 36.2.5.2):

- A single, contiguous region of physical address space.
- A collection of variable-sized regions of physical memory. These regions are linked together by tables of pointers to those regions, referred to as Table of Physical Addresses (ToPA). The trace output stores bypass the caches and the TLBs, but are not serializing. This is intended to minimize the performance impact of the output.
- A platform-specific trace transport subsystem.

Regardless of the output scheme chosen, Intel PT stores bypass the processor caches by default. This ensures that they don’t consume precious cache space, but they do not have the serializing aspects associated with un-cacheable (UC) stores. Software should avoid using MTRRs to mark any portion of the Intel PT output region as UC, as this may override the behavior described above and force Intel PT stores to UC, thereby incurring severe performance impact.

There is no guarantee that a packet will be written to memory or other trace endpoint after some fixed number of cycles after a packet-producing instruction executes. The only way to assure that all packets generated have reached their endpoint is to clear TraceEn and follow that with a store, fence, or serializing instruction; doing so ensures that all buffered packets are flushed out of the processor.

36.2.4.1 Single Range Output

When IA32_RTIT_CTL.ToPA and IA32_RTIT_CTL.FabricEn bits are clear, trace packet output is sent to a single, contiguous memory (or MMIO if DRAM is not available) range defined by a base address in IA32_RTIT_OUTPUT_BASE (Section 36.2.5.7) and mask value in IA32_RTIT_OUTPUT_MASK_PTRS (Section 36.2.5.8). The current write pointer in this range is also stored in IA32_RTIT_OUTPUT_MASK_PTRS. This output range is circular, meaning that when the writes wrap around the end of the buffer they begin again at the base address.
This output method is best suited for cases where Intel PT output is either:

- Configured to be directed to a sufficiently large contiguous region of DRAM.
- Configured to go to an MMIO debug port, in order to route Intel PT output to a platform-specific trace endpoint (e.g., JTAG). In this scenario, a specific range of addresses is written in a circular manner, and SoC will intercept these writes and direct them to the proper device. Repeated writes to the same address do not overwrite each other, but are accumulated by the debugger, and hence no data is lost by the circular nature of the buffer.

The processor will determine the address to which to write the next trace packet output byte as follows:

\[
\text{OutputBase}_{[63:0]} \leftarrow \text{IA32_RTIT_OUTPUT_BASE}_{[63:0]}
\]

\[
\text{OutputMask}_{[63:0]} \leftarrow \text{ZeroExtend64} (\text{IA32_RTIT_OUTPUT_MASK_PTRS}_{[31:0]})
\]

\[
\text{OutputOffset}_{[63:0]} \leftarrow \text{ZeroExtend64} (\text{IA32_RTIT_OUTPUT_MASK_PTRS}_{[63:32]})
\]

\[
\text{trace_store_phys_addr} \leftarrow (\text{OutputBase} \& \sim \text{OutputMask}) + (\text{OutputOffset} \& \text{OutputMask})
\]

**Single-Range Output Errors**

If the output base and mask are not properly configured by software, an operational error (see Section 36.3.9) will be signaled, and tracing disabled. Error scenarios with single-range output are:

- Mask value is non-contiguous.
  
  \[
  \text{IA32_RTIT_OUTPUT_MASK_PTRS.MaskOrTablePointer} \text{ value has a 0 in a less significant bit position than the most significant bit containing a 1.}
  \]

- Base address and Mask are mis-aligned, and have overlapping bits set.
  
  \[
  \text{IA32_RTIT_OUTPUT_BASE} \& \& \text{IA32_RTIT_OUTPUT_MASK_PTRS.MaskOrTableOffset} > 0.
  \]

- Illegal Output Offset
  
  \[
  \text{IA32_RTIT_OUTPUT_MASK_PTRS.OutputOffset} \text{ is greater than the mask value (IA32_RTIT_OUTPUT_MASK_PTRS.MaskOrTableOffset).}
  \]

Also note that errors can be signaled due to trace packet output overlapping with restricted memory, see Section 36.2.4.4.

**36.2.4.2 Table of Physical Addresses (ToPA)**

When IA32_RTIT_CTL.ToPA is set and IA32_RTIT_CTL.FabricEn is clear, the ToPA output mechanism is utilized. The ToPA mechanism uses a linked list of tables; see Figure 36-1 for an illustrative example. Each entry in the table contains some attribute bits, a pointer to an output region, and the size of the region. The last entry in the table may hold a pointer to the next table. This pointer can either point to the top of the current table (for circular array) or to the base of another table. The table size is not fixed, since the link to the next table can exist at any entry.

The processor treats the various output regions referenced by the ToPA table(s) as a unified buffer. This means that a single packet may span the boundary between one output region and the next.

The ToPA mechanism is controlled by three values maintained by the processor:

- **proc_trace_table_base.**
  
  This is the physical address of the base of the current ToPA table. When tracing is enabled, the processor loads this value from the IA32_RTIT_OUTPUT_BASE MSR. While tracing is enabled, the processor updates the IA32_RTIT_OUTPUT_BASE MSR with changes to proc_trace_table_base, but these updates may not be synchronous to software execution. When tracing is disabled, the processor ensures that the MSR contains the latest value of proc_trace_table_base.

- **proc_trace_table_offset.**
  
  This indicates the entry of the current table that is currently in use. (This entry contains the address of the current output region.) When tracing is enabled, the processor loads this value from bits 31:7 (MaskOrTableOffset) of the IA32_RTIT_OUTPUT_MASK_PTRS. While tracing is enabled, the processor updates IA32_RTIT_OUTPUT_MASK_PTRS.MaskOrTableOffset with changes to proc_trace_table_offset, but these updates may not be synchronous to software execution. When tracing is disabled, the processor ensures that the MSR contains the latest value of proc_trace_table_offset.

- **proc_trace_output_offset.**
  
  This a pointer into the current output region and indicates the location of the next write. When tracing is
enabled, the processor loads this value from bits 63:32 (OutputOffset) of the IA32_RTIT_OUTPUT_MASK_PTRS. While tracing is enabled, the processor updates IA32_RTIT_OUTPUT_MASK_PTRS.OutputOffset with changes to proc_trace_output_offset, but these updates may not be synchronous to software execution. When tracing is disabled, the processor ensures that the MSR contains the latest value of proc_trace_output_offset.

Figure 36-1 provides an illustration (not to scale) of the table and associated pointers.

![Figure 36-1. ToPA Memory Illustration](image)

With the ToPA mechanism, the processor writes packets to the current output region (identified by proc_trace_table_base and the proc_trace_table_offset). The offset within that region to which the next byte will be written is identified by proc_trace_output_offset. When that region is filled with packet output (thus proc_trace_output_offset = RegionSize–1), proc_trace_table_offset is moved to the next ToPA entry, proc_trace_output_offset is set to 0, and packet writes begin filling the new output region specified by proc_trace_table_offset.

As packets are written out, each store derives its physical address as follows:

\[
\text{trace_store_phys_addr} \leftarrow \text{Base address from current ToPA table entry} + \text{proc_trace_output_offset}
\]

Eventually, the regions represented by all entries in the table may become full, and the final entry of the table is reached. An entry can be identified as the final entry because it has either the END or STOP attribute. The END attribute indicates that the address in the entry does not point to another output region, but rather to another ToPA table. The STOP attribute indicates that tracing will be disabled once the corresponding region is filled. See Section 36.2.4.2 for details on STOP.

When an END entry is reached, the processor loads proc_trace_table_base with the base address held in this END entry, thereby moving the current table pointer to this new table. The proc_trace_table_offset is reset to 0, as is the proc_trace_output_offset, and packet writes will resume at the base address indicated in the first entry.

If the table has no STOP or END entry, and trace-packet generation remains enabled, eventually the maximum table size will be reached (proc_trace_table_offset = FFFFFFFFH). In this case, the proc_trace_table_offset and proc_trace_output_offset are reset to 0 (wrapping back to the beginning of the current table) once the last output region is filled.
It is important to note that processor updates to the IA32_RTIT_OUTPUT_BASE and IA32_RTIT_OUTPUT_MASK_PTRS MSRs are asynchronous to instruction execution. Thus, reads of these MSRs while Intel PT is enabled may return stale values. Like all IA32_RTIT_* MSRs, the values of these MSRs should not be trusted or saved unless trace packet generation is first disabled by clearing IA32_RTIT_CTL.TraceEn. This ensures that the output MSR values account for all packets generated to that point, after which the output MSR values will be frozen until tracing resumes. 1

The processor may cache internally any number of entries from the current table or from tables that it references (directly or indirectly). If tracing is enabled, the processor may ignore or delay detection of modifications to these tables. To ensure that table changes are detected by the processor in a predictable manner, software should clear TraceEn before modifying the current table (or tables that it references) and only then re-enable packet generation.

**Single Output Region ToPA Implementation**

The first processor generation to implement Intel PT supports only ToPA configurations with a single ToPA entry followed by an END entry that points back to the first entry (creating one circular output buffer). Such processors enumerate CPUID.(EAX=14H,ECX=0):ECX.MENTRY[bit 1] = 0 and CPUID.(EAX=14H,ECX=0):ECX.TOPAOUT[bit 0] = 1.

If CPUID.(EAX=14H,ECX=0):ECX.MENTRY[bit 1] = 0, ToPA tables can hold only one output entry, which must be followed by an END=1 entry which points back to the base of the table. Hence only one contiguous block can be used as output.

The lone output entry can have INT or STOP set, but nonetheless must be followed by an END entry as described above. Note that, if INT=1, the PMI will actually be delivered before the region is filled.

**ToPA Table Entry Format**

The format of ToPA table entries is shown in Figure 36-2. The size of the address field is determined by the processor’s physical-address width (MAXPHYADDR) in bits, as reported in CPUID.80000008H:EAX[7:0].

![Figure 36-2. Layout of ToPA Table Entry](image)

Table 36-3 describes the details of the ToPA table entry fields. If reserved bits are set to 1, an error is signaled.

**Table 36-3. ToPA Table Entry Fields**

<table>
<thead>
<tr>
<th>ToPA Entry Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Region Base Physical Address</td>
<td>If END=0, this is the base physical address of the output region specified by this entry. Note that all regions must be aligned based on their size. Thus a 2M region must have bits 20:12 clear. If the region is not properly aligned, an operational error will be signaled when the entry is reached. If END=1, this is the 4K-aligned base physical address of the next ToPA table (which may be the base of the current table, or the first table in the linked list if a circular buffer is desired). If the processor supports only a single ToPA output region (see above), this address must be the value currently in the IA32_RTIT_OUTPUT_BASE MSR.</td>
</tr>
</tbody>
</table>

---

1. Although WRMSR is a serializing instruction, the execution of WRMSR that forces packet writes by clearing TraceEn does not itself cause these writes to be globally observed.
Each ToPA entry has a STOP bit. If this bit is set, the processor will set the IA32_RTIT_STATUS.Stopped bit when the corresponding trace output region is filled. This will clear TriggerEn and thereby cease packet generation. See Section 36.2.5.4 for details on IA32_RTIT_STATUS.Stopped. This sequence is known as “ToPA Stop”.

No TIP.PGD packet will be seen in the output when the ToPA stop occurs, since the disable happens only when the region is already full. When this occurs, output ceases after the last byte of the region is filled, which may mean that a packet is cut off in the middle. Any packets remaining in internal buffers are lost and cannot be recovered.

When ToPA stop occurs, the IA32_RTIT_OUTPUT_BASE MSR will hold the base address of the table whose entry had STOP=1. IA32_RTIT_OUTPUT_MASK_PTRS.MaskOrTableOffset will hold the index value for that entry, and the IA32_RTIT_OUTPUT_MASK_PTRS.OutputOffset should be set to the size of the region.

Note that this means the offset pointer is pointing to the next byte after the end of the region, a configuration that would produce an operational error if the configuration remained when tracing is re-enabled with IA32_RTIT_STATUS.Stopped cleared.

ToPA PMI

Each ToPA entry has an INT bit. If this bit is set, the processor will signal a performance-monitoring interrupt (PMI) when the corresponding trace output region is filled. This interrupt is not precise, and it is thus likely that writes to the next region will occur by the time the interrupt is taken.

The following steps should be taken to configure this interrupt:

1. Enable PMI via the LVT Performance Monitor register (at MMIO offset 340H in xAPIC mode; via MSR 834H in x2APIC mode). See Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3B for more details on this register. For ToPA PMI, set all fields to 0, save for the interrupt vector, which can be selected by software.

2. Set up an interrupt handler to service the interrupt vector that a ToPA PMI can raise.

3. Set the interrupt flag by executing STI.

4. Set the INT bit in the ToPA entry of interest and enable packet generation, using the ToPA output option. Thus, TraceEn=ToPA=1 in the IA32_RTIT_CTL MSR.

Once the INT region has been filled with packet output data, the interrupt will be signaled. This PMI can be distinguished from others by checking bit 55 (Trace_ToPA_PMI) of the IA32_PERF_GLOBAL_STATUS MSR (MSR 38EH). Once the ToPA PMI handler has serviced the relevant buffer, writing 1 to bit 55 of the MSR at 390H (IA32_GLOBAL_STATUS_RESET) clears IA32_PERF_GLOBAL_STATUS.Trace_ToPA_PMI.
Intel PT is not frozen on PMI, and thus the interrupt handler will be traced (though filtering can prevent this). The IA32_DEBUGCTL.Freeze_Perfmon_on_PMI setting will be applied on ToPA PMI just as on other PMIs, and hence Perfmon counters are frozen.

Assuming the PMI handler wishes to read any buffered packets for persistent output, software should first disable packet generation by clearing TraceEn. This ensures that all buffered packets are written to memory and avoids tracing of the PMI handler. The configuration MSRs can then be used to determine where tracing has stopped. If packet generation is disabled by the handler, it should then be manually re-enabled before the IRET if continued tracing is desired.

**ToPA PMI and Single Output Region ToPA Implementation**

A processor that supports only a single ToPA output region implementation (such that only one output region is supported; see above) will attempt to signal a ToPA PMI interrupt before the output wraps and overwrites the top of the buffer. To support this functionality, the PMI handler should disable packet generation as soon as possible.

Due to PMI skid, it is possible, in rare cases, that the wrap will have occurred before the PMI is delivered. Software can avoid this by setting the STOP bit in the ToPA entry (see Table 36-3); this will disable tracing once the region is filled, and no wrap will occur. This approach has the downside of disabling packet generation so that some of the instructions that led up to the PMI will not be traced. If the PMI skid is significant enough to cause the region to fill and tracing to be disabled, the PMI handler will need to clear the IA32_RTIT_STATUS.Stopped indication before tracing can resume.

**ToPA PMI and XSAVES/XRSTORS State Handling**

In some cases the ToPA PMI may be taken after completion of an XSAVES instruction that switches Intel PT state, and in such cases any modification of Intel PT MSRs within the PMI handler will not persist when the saved Intel PT context is later restored with XRSTORS. To account for such a scenario, it is recommended that the Intel PT output configuration be modified by altering the ToPA tables themselves, rather than the Intel PT output MSRs.

Table 36-4 depicts a recommended PMI handler algorithm for managing multi-region ToPA output and handling ToPA PMIs that may arrive between XSAVES and XRSTORS. This algorithm is flexible to allow software to choose between adding entries to the current ToPA table, adding a new ToPA table, or using the current ToPA table as a circular buffer. It assumes that the ToPA entry that triggers the PMI is not the last entry in the table, which is the recommended treatment.

<table>
<thead>
<tr>
<th>Pseudo Code Flow</th>
</tr>
</thead>
<tbody>
<tr>
<td>IF (IA32_PERF_GLOBAL_STATUS.ToPA)</td>
</tr>
<tr>
<td>Save IA32_RTIT_CTL value;</td>
</tr>
<tr>
<td>IF (IA32_RTIT_CTL.TraceEN)</td>
</tr>
<tr>
<td>Disable Intel PT by clearing TraceEn;</td>
</tr>
<tr>
<td>FI;</td>
</tr>
<tr>
<td>IF (there is space available to grow the current ToPA table)</td>
</tr>
<tr>
<td>Add one or more ToPA entries after the last entry in the ToPA table;</td>
</tr>
<tr>
<td>Point new ToPA entry address field(s) to new output region base(s);</td>
</tr>
<tr>
<td>ELSE</td>
</tr>
<tr>
<td>Modify an upcoming ToPA entry in the current table to have END=1;</td>
</tr>
<tr>
<td>IF (output should transition to a new ToPA table)</td>
</tr>
<tr>
<td>Point the address of the &quot;END=1&quot; entry of the current table to the new table base;</td>
</tr>
<tr>
<td>ELSE</td>
</tr>
<tr>
<td>/* Continue to use the current ToPA table, make a circular. */</td>
</tr>
<tr>
<td>Point the address of the &quot;END=1&quot; entry to the base of the current table;</td>
</tr>
<tr>
<td>Modify the ToPA entry address fields for filled output regions to point to new, unused output regions;</td>
</tr>
<tr>
<td>/* Filled regions are those with index in the range of 0 to IA32_RTIT_MASK_PTRS.MaskOrTableOffset -1. */</td>
</tr>
<tr>
<td>FI;</td>
</tr>
<tr>
<td>FI;</td>
</tr>
<tr>
<td>Restore saved IA32_RTIT_CTL.value;</td>
</tr>
<tr>
<td>FI;</td>
</tr>
</tbody>
</table>
ToPA Errors
When a malformed ToPA entry is found, an operation error results (see Section 36.3.9). A malformed entry can be any of the following:

1. **ToPA entry reserved bit violation.**
   This describes cases where a bit marked as reserved in Section 36.2.4.2 above is set to 1.

2. **ToPA alignment violation.**
   This includes cases where illegal ToPA entry base address bits are set to 1:
   a. ToPA table base address is not 4KB-aligned. The table base can be from a WRMSR to IA32_RTIT_OUTPUT_BASE, or from a ToPA entry with END=1.
   b. ToPA entry base address is not aligned to the ToPA entry size (e.g., a 2MB region with base address[20:12] not equal to 0).
   c. ToPA entry base address sets upper physical address bits not supported by the processor.

3. **Illegal ToPA Output Offset (if IA32_RTIT_STATUS.Stopped=0).**
   IA32_RTIT_OUTPUT_MASK_PTRS.OutputOffset is greater than or equal to the size of the current ToPA output region size.

4. **ToPA rules violations.**
   These are similar to ToPA entry reserved bit violations; they are cases when a ToPA entry is encountered with illegal field combinations. They include the following:
   a. Setting the STOP or INT bit on an entry with END=1.
   b. Setting the END bit in entry 0 of a ToPA table.
   c. On processors that support only a single ToPA entry (see above), two additional illegal settings apply:
      i) ToPA table entry 1 with END=0.
      ii) ToPA table entry 1 with base address not matching the table base.

In all cases, the error will be logged by setting IA32_RTIT_STATUS.Error, thereby disabling tracing when the problematic ToPA entry is reached (when proc_trace_table_offset points to the entry containing the error). Any packet bytes that are internally buffered when the error is detected may be lost.

Note that operational errors may also be signaled due to attempts to access restricted memory. See Section 36.2.4.4 for details.

A tracing software have a range of flexibility using ToPA to manage the interaction of Intel PT with application buffers, see Section 36.5.

### 36.2.4.3 Trace Transport Subsystem
When IA32_RTIT_CTL.FabricEn is set, the IA32_RTIT_CTL.ToPA bit is ignored, and trace output is written to the trace transport subsystem. The endpoints of this transport are platform-specific, and details of configuration options should refer to the specific platform documentation. The FabricEn bit is available to be set if CPUID(EAX=14H,ECX=0):EBX[bit 3] = 1.

### 36.2.4.4 Restricted Memory Access
Packet output cannot be directed to any regions of memory that are restricted by the platform. In particular, all memory accesses on behalf of packet output are checked against the SMRR regions. If there is any overlap with these regions, trace data collection will not function properly. Exact processor behavior is implementation-dependent; Table 36-5 summarizes several scenarios.
It should also be noted that packet output should not be routed to the 4KB APIC MMIO region, as defined by the IA32_APIC_BASE MSR. For details about the APIC, refer to Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 3A. No error is signaled for this case.

**Modifications to Restricted Memory Regions**

It is recommended that software disable packet generation before modifying the SMRRs to change the scope of the SMRR regions. This is because the processor reserves the right to cache any number of ToPA table entries internally, after checking them against restricted memory ranges. Once cached, the entries will not be checked again, meaning one could potentially route packet output to a newly restricted region. Software can ensure that any cached entries are written to memory by clearing IA32_RTIT_CTL.TraceEn.

### 36.2.5 Enabling and Configuration MSRs

#### 36.2.5.1 General Considerations

Trace packet generation is enabled and configured by a collection of model-specific registers (MSRs), which are detailed below. Some notes on the configuration MSR behavior:

- If Intel Processor Trace is not supported by the processor (see Section 36.3.1), RDMSR or WRMSR of the IA32_RTIT_* MSRs will cause #GP.
- A WRMSR to any of these configuration MSRs that begins and ends with IA32_RTIT_CTL.TraceEn set will #GP fault. Packet generation must be disabled before the configuration MSRs can be changed.

  Note: Software may write the same value back to IA32_RTIT_CTL without #GP, even if TraceEn=1.

- All configuration MSRs for Intel PT are duplicated per logical processor
- For each configuration MSR, any MSR write that attempts to change bits marked reserved, or utilize encodings marked reserved, will cause a #GP fault.
- All configuration MSRs for Intel PT are cleared on a cold RESET.
  - If CPUID.(EAX=14H, ECX=0):EBX.IPFILT_WRSTPRSV[bit 2] = 1, only the TraceEn bit is cleared on warm RESET; though this may have the impact of clearing other bits in IA32_RTIT_STATUS. Other MSR values of the trace configuration MSRs are preserved on warm RESET.
- The semantics of MSR writes to trace configuration MSRs in this chapter generally apply to explicit WRMSR to these registers, using VM-exit or VM-entry MSR load list to these MSRs, XRSTORS with requested feature bit map including XSAVE map component of state_8 (corresponding to IA32_XSS[bit 8]), and the write to IA32_RTIT_CTL.TraceEn by XSAVES (Section 36.3.5.2).

#### 36.2.5.2 IA32_RTIT_CTL MSR

IA32_RTIT_CTL, at address 570H, is the primary enable and control MSR for trace packet generation. Bit positions are listed in Table 36-6.
Table 36-6. IA32_RTIT_CTL MSR

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TraceEn</td>
<td>0</td>
<td>If 1, enables tracing; else tracing is disabled if 0. When this bit transitions from 1 to 0, all buffered packets are flushed out of internal buffers. A further store, fence, or architecturally serializing instruction may be required to ensure that packet data can be observed at the trace endpoint. See Section 36.2.5.3 for details of enabling and disabling packet generation. Note that the processor will clear this bit on #SMI (Section 36.2.5.1) and warm reset. Other MSR bits of IA32_RTIT_CTL (and other trace configuration MSRs) are not impacted by these events.</td>
</tr>
<tr>
<td>1</td>
<td>CYCEn</td>
<td>0</td>
<td>0: Disables CYC Packet (see Section 36.4.2.14). 1: Enables CYC Packet. This bit is reserved if CPUID.(EAX=14H, ECX=0):EBX.CPSB_CAM[bit 1] = 0.</td>
</tr>
<tr>
<td>2</td>
<td>OS</td>
<td>0</td>
<td>0: Packet generation is disabled when CPL = 0. 1: Packet generation may be enabled when CPL = 0.</td>
</tr>
<tr>
<td>3</td>
<td>User</td>
<td>0</td>
<td>0: Packet generation is disabled when CPL &gt; 0. 1: Packet generation may be enabled when CPL &gt; 0.</td>
</tr>
<tr>
<td>5:4</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>6</td>
<td>FabricEn</td>
<td>0</td>
<td>0: Trace output is directed to the memory subsystem, mechanism depends on IA32_RTIT_CTL.ToPA. 1: Trace output is directed to the trace transport subsystem, IA32_RTIT_CTL.ToPA is ignored. This bit is reserved if CPUID.(EAX=14H, ECX=0):ECX[bit 3] = 0.</td>
</tr>
<tr>
<td>7</td>
<td>CR3Filter</td>
<td>0</td>
<td>0: Disables CR3 filtering. 1: Enables CR3 filtering.</td>
</tr>
<tr>
<td>8</td>
<td>ToPA</td>
<td>0</td>
<td>0: Single-range output scheme enabled if CPUID.(EAX=14H, ECX=0):ECX.SNGLRGNOUT[bit 2] = 1 and IA32_RTIT_CTL.FabricEn=0. 1: ToPA output scheme enabled (see Section 36.2.4.2) if CPUID.(EAX=14H, ECX=0):ECX.TOPA[bit 0] = 1, and IA32_RTIT_CTL.FabricEn=0. Note: WRMSR to IA32_RTIT_CTL that sets TraceEn but clears this bit and FabricEn would cause #GP, if CPUID.(EAX=14H, ECX=0):ECX.SNGLRGNOUT[bit 2] = 0. WRMSR to IA32_RTIT_CTL that sets this bit causes #GP, if CPUID.(EAX=14H, ECX=0):ECX.TOPA[bit 0] = 0.</td>
</tr>
<tr>
<td>9</td>
<td>MTCEn</td>
<td>0</td>
<td>0: Disables MTC Packet (see Section 36.4.2.16). 1: Enables MTC Packet. This bit is reserved if CPUID.(EAX=14H, ECX=0):EBX.MTC[bit 3] = 0.</td>
</tr>
<tr>
<td>10</td>
<td>TSCEn</td>
<td>0</td>
<td>0: Disable TSC packets. 1: Enable TSC packets (see Section 36.4.2.11).</td>
</tr>
<tr>
<td>11</td>
<td>DisRETC</td>
<td>0</td>
<td>0: Enable RET compression. 1: Disable RET compression (see Section 36.2.1.2).</td>
</tr>
<tr>
<td>12</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>13</td>
<td>BranchEn</td>
<td>0</td>
<td>0: Disable COFI-based packets. 1: Enable COFI-based packets: FUP, TIP, TIP.PGE, TIP.PGD, TNT, MODE.Exec, MODE.TSX. see Section 36.2.4 for details on BranchEn.</td>
</tr>
</tbody>
</table>
# INTEL® PROCESSOR TRACE

## Table 36-6. IA32_RTIT_CTL MSR

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>17:14</td>
<td>MTCFreq</td>
<td>0</td>
<td>Defines MTC packet Frequency, which is based on the core crystal clock, or Always Running Timer (ART). MTC will be sent each time the selected ART bit toggles. The following Encodings are defined:</td>
</tr>
<tr>
<td>18</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>22:19</td>
<td>CycThresh</td>
<td>0</td>
<td>CYC packet threshold, see Section 36.3.6 for details. CYC packets will be sent with the first eligible packet after N cycles have passed since the last CYC packet. If CycThresh is 0 then N=0, otherwise N is defined as 2^CycThresh. The following Encodings are defined:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Software must use CPUID to query the supported encodings in the processor, see Section 36.3.1. Use of unsupported encodings will result in a #GP fault. This field is reserved if CPUID.(EAX=14H, ECX=0):EBX.MTC[bit 3] = 0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>27:24</td>
<td>PSBFreq</td>
<td>0</td>
<td>Indicates the frequency of PSB packets. PSB packet frequency is based on the number of Intel PT packet bytes output, so this field allows the user to determine the increment of IA32_IA32_RTIT_STATUS.PacketByteCnt that should cause a PSB to be generated. Note that PSB insertion is not precise, but the average output bytes per PSB should approximate the SW selected period. The following Encodings are defined:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Software must use CPUID to query the supported encodings in the processor, see Section 36.3.1. Use of unsupported encodings will result in a #GP fault. This field is reserved if CPUID.(EAX=14H, ECX=0):EBX.CPSB_CAM[bit 1] = 0.</td>
</tr>
<tr>
<td>31:28</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>35:32</td>
<td>ADDRO_CFG</td>
<td>0</td>
<td>Configures the base/limit register pair IA32_RTIT_ADDR0_A/B based on the following encodings:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: ADDRO range unused.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: The [IA32_RTIT_ADDR0_A:IA32_RTIT_ADDR0_B] range defines a FilterEn range. FilterEn will only be set when the IP is within this range, though other FilterEn ranges can additionally be used. See Section 36.2.2.3 for details on IP filtering.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2: The [IA32_RTIT_ADDR0_A:IA32_RTIT_ADDR0_B] range defines a TraceStop range. TraceStop will be asserted if code branches into this range. See 4.2.8 for details on TraceStop.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3..15: Reserved (#GP).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>This field is reserved if CPUID.(EAX=14H, ECX=1):EBX.RANGECNT[2:0] &gt;= 0.</td>
</tr>
</tbody>
</table>
36.2.5.3 Enabling and Disabling Packet Generation with TraceEn

When TraceEn transitions from 0 to 1, Intel Processor Trace is enabled, and a series of packets may be generated. These packets help ensure that the decoder is aware of the state of the processor when the trace begins, and that it can keep track of any timing or state changes that may have occurred while packet generation was disabled. A full PSB+ (see Section 36.4.2.17) will be generated if IA32_RTIT_STATUS.PacketByteCnt=0, and may be generated in other cases as well. Otherwise, timing packets will be generated, including TSC, TMA, and CBR (see Section 36.4.2).

In addition to the packets discussed above, if and when PacketEn (Section 36.2.3.1) transitions from 0 to 1 (which may happen immediately, depending on filtering settings), a TIP.PGE packet (Section 36.4.2.3) will be generated.

When TraceEn is set, the processor may read ToPA entries from memory and cache them internally. For this reason, software should disable packet generation before making modifications to the ToPA tables (or changing the config-
Disabling Packet Generation
Clearing TraceEn causes any packet data buffered within the logical processor to be flushed out, after which the output MSRs (IA32_RTIT_OUTPUT_BASE and IA32_RTIT_OUTPUT_MASK_PTRS) will have stable values. When output is directed to memory, a store, fence, or architecturally serializing instruction may be required to ensure that the packet data is globally observed. No special packets are generated by disabling packet generation, though a TIP.PGD may result if PacketEn=1 at the time of disable.

Other Writes to IA32_RTIT_CTL
Any attempt to modify IA32_RTIT_CTL while TraceEn is set will result in a general-protection fault (#GP) unless the same write also clears TraceEn. However, writes to IA32_RTIT_CTL that do not modify any bits will not cause a #GP, even if TraceEn remains set.

36.2.5.4 IA32_RTIT_STATUS MSR
The IA32_RTIT_STATUS MSR is readable and writable by software, but some bits (ContextEn, TriggerEn) are read-only and cannot be directly modified. The WRMSR instruction ignores these bits in the source operand (attempts to modify these bits are ignored and do not cause WRMSR to fault).
This MSR can only be written when IA32_RTIT_CTL.TraceEn is 0; otherwise WRMSR causes a general-protection fault (#GP). The processor does not modify the value of this MSR while TraceEn is 0 (software can modify it with WRMSR).

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FilterEn</td>
<td>0</td>
<td>This bit is written by the processor, and indicates that tracing is allowed for the current IP, see Section 36.2.3.5. Writes are ignored.</td>
</tr>
<tr>
<td>1</td>
<td>ContextEn</td>
<td>0</td>
<td>The processor sets this bit to indicate that tracing is allowed for the current context. See Section 36.2.3.3. Writes are ignored.</td>
</tr>
<tr>
<td>2</td>
<td>TriggerEn</td>
<td>0</td>
<td>The processor sets this bit to indicate that tracing is enabled. See Section 36.2.3.2. Writes are ignored.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>4</td>
<td>Error</td>
<td>0</td>
<td>The processor sets this bit to indicate that an operational error has been encountered. When this bit is set, TriggerEn is cleared to 0 and packet generation is disabled. For details, see “ToPA Errors” in Section 36.2.4.2. When TraceEn is cleared, software can write this bit. Once it is set, only software can clear it. It is not recommended that software ever set this bit, except in cases where it is restoring a prior saved state.</td>
</tr>
<tr>
<td>5</td>
<td>Stopped</td>
<td>0</td>
<td>The processor sets this bit to indicate that a ToPA Stop condition has been encountered. When this bit is set, TriggerEn is cleared to 0 and packet generation is disabled. For details, see “ToPA STOP” in Section 36.2.4.2. When TraceEn is cleared, software can write this bit. Once it is set, only software can clear it. It is not recommended that software ever set this bit, except in cases where it is restoring a prior saved state.</td>
</tr>
<tr>
<td>31:6</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
<tr>
<td>48:32</td>
<td>PacketByteCnt</td>
<td>0</td>
<td>This field is written by the processor, and holds a count of packet bytes that have been sent out. The processor also uses this field to determine when the next PSB packet should be inserted. Note that the processor may clear or modify this field at any time while IA32_RTIT_CTL.TraceEn=1. It will have a stable value when IA32_RTIT_CTL.TraceEn=0. See Section 36.4.2.17 for details.</td>
</tr>
<tr>
<td>63:49</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
</tbody>
</table>
36.2.5.5 IA32_RTIT_ADDRn_A and IA32_RTIT_ADDRn_B MSRs

The role of the IA32_RTIT_ADDRn_A/B register pairs, for each n, is determined by the corresponding ADDRn_CFG fields in IA32_RTIT_CTL (see Section 36.2.5.2). The number of these register pairs is enumerated by CPUID.(EAX=14H, ECX=1):EAX.RANGECNT[2:0].

- Processors that enumerate support for 1 range support:
  IA32_RTIT_ADDR0_A, IA32_RTIT_ADDR0_B

- Processors that enumerate support for 2 ranges support:
  IA32_RTIT_ADDR0_A, IA32_RTIT_ADDR0_B
  IA32_RTIT_ADDR1_A, IA32_RTIT_ADDR1_B

- Processors that enumerate support for 3 ranges support:
  IA32_RTIT_ADDR0_A, IA32_RTIT_ADDR0_B
  IA32_RTIT_ADDR1_A, IA32_RTIT_ADDR1_B
  IA32_RTIT_ADDR2_A, IA32_RTIT_ADDR2_B

- Processors that enumerate support for 4 ranges support:
  IA32_RTIT_ADDR0_A, IA32_RTIT_ADDR0_B
  IA32_RTIT_ADDR1_A, IA32_RTIT_ADDR1_B
  IA32_RTIT_ADDR2_A, IA32_RTIT_ADDR2_B
  IA32_RTIT_ADDR3_A, IA32_RTIT_ADDR3_B

Each register has a single 64-bit field that holds a linear address value. Writes must ensure that the address is properly sign-extended, otherwise a #GP fault will result.

36.2.5.6 IA32_RTIT_CR3_MATCH MSR

The IA32_RTIT_CR3_MATCH register is compared against CR3 when IA32_RTIT_CTL.CR3Filter is 1. Bits 63:5 hold the CR3 address value to match, bits 4:0 are reserved to 0. For more details on CR3 filtering and the treatment of this register, see Section 36.2.2.2.

This MSR can be written only when IA32_RTIT_CTL.TraceEn is 0; otherwise WRMSR causes a general-protection fault (#GP). IA32_RTIT_CR3_MATCH[4:0] are reserved and must be 0; an attempt to set those bits using WRMSR causes a #GP.

36.2.5.7 IA32_RTIT_OUTPUT_BASE MSR

This MSR is used to configure the trace output destination, when output is directed to memory (IA32_RTIT_CTL.FabricEn = 0). The size of the address field is determined by the maximum physical address width (MAXPHYADDR), as reported by CPUID.80000008H:EAX[7:0].

When the ToPA output scheme is used, the processor may update this MSR when packet generation is enabled, and those updates are asynchronous to instruction execution. Therefore, the values in this MSR should be considered unreliable unless packet generation is disabled (IA32_RTIT_CTL.TraceEn = 0).

Accesses to this MSR are supported only if Intel PT output to memory is supported, hence when either CPUID.(EAX=14H, ECX=0):ECX[bit 0] or CPUID.(EAX=14H, ECX=0):ECX[bit 2] are set. Otherwise WRMSR or RDMSR cause a general-protection fault (#GP). If supported, this MSR can be written only when IA32_RTIT_CTL.TraceEn is 0; otherwise WRMSR causes a general-protection fault (#GP).

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:0</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
</tbody>
</table>
36.2.5.8 IA32_RTIT_OUTPUT_MASK_PTRS MSR

This MSR holds any mask or pointer values needed to indicate where the next byte of trace output should be written. The meaning of the values held in this MSR depend on whether the ToPA output mechanism is in use. See Section 36.2.4.2 for details.

The processor updates this MSR while when packet generation is enabled, and those updates are asynchronous to instruction execution. Therefore, the values in this MSR should be considered unreliable unless packet generation is disabled (IA32_RTIT_CTL.TraceEn = 0).

Accesses to this MSR are supported only if Intel PT output to memory is supported, hence when either CPUID.(EAX=14H, ECX=0):ECX[bit 0] or CPUID.(EAX=14H, ECX=0):ECX[bit 2] are set. Otherwise WRMSR or RDMSR cause a general-protection fault (#GP). If supported, this MSR can be written only when IA32_RTIT_CTL.TraceEn is 0; otherwise WRMSR causes a general-protection fault (#GP).

### Table 36-8. IA32_RTIT_OUTPUT_BASE MSR

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAXPHYADDR-1:7</td>
<td>BasePhysAddr</td>
<td>0</td>
<td>The base physical address. How this address is used depends on the value of IA32_RTIT_CTL.ToPA: 0: This is the base physical address of a single, contiguous physical output region. This could be mapped to DRAM or to MMIO, depending on the value. The base address should be aligned with the size of the region, such that none of the 1s in the mask value (Section 36.2.5.8) overlap with 1s in the base address. If the base is not aligned, an operational error will result (see Section 36.3.9). 1: The base physical address of the current ToPA table. The address must be 4K aligned. Writing an address in which bits 11:7 are non-zero will not cause a #GP, but an operational error will be signaled once TraceEn is set. See “ToPA Errors” in Section 36.2.4.2 as well as Section 36.3.9.</td>
</tr>
<tr>
<td>63:MAXPHYADDR</td>
<td>Reserved</td>
<td>0</td>
<td>Must be 0.</td>
</tr>
</tbody>
</table>

### Table 36-9. IA32_RTIT_OUTPUT_MASK_PTRS MSR

<table>
<thead>
<tr>
<th>Position</th>
<th>Bit Name</th>
<th>At Reset</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6:0</td>
<td>LowerMask</td>
<td>7FH</td>
<td>Forced to 1, writes are ignored.</td>
</tr>
<tr>
<td>31:7</td>
<td>MaskOrTableOffset</td>
<td>0</td>
<td>0: This field holds bits 31:7 of the mask value for the single, contiguous physical output region. The size of this field indicates that regions can be of size 128B up to 4GB. This value (combined with the lower 7 bits, which are reserved to 1) will be ANDed with the OutputOffset field to determine the next write address. All 1s in this field should be consecutive and starting at bit 7, otherwise the region will not be contiguous, and an operational error (Section 36.3.9) will be signaled when TraceEn is set. 1: This field holds bits 27:3 of the offset pointer into the current ToPA table. This value can be added to the IA32_RTIT_OUTPUT_BASE value to produce a pointer to the current ToPA table entry, which itself is a pointer to the current output region. In this scenario, the lower 7 reserved bits are ignored. This field supports tables up to 256 MBytes in size.</td>
</tr>
<tr>
<td>63:32</td>
<td>OutputOffset</td>
<td>0</td>
<td>0: This is bits 31:0 of the offset pointer into the single, contiguous physical output region. This value will be added to the IA32_RTIT_OUTPUT_BASE value to form the physical address at which the next byte of packet output data will be written. This value must be less than or equal to the MaskOrTableOffset field, otherwise an operational error (Section 36.3.9) will be signaled when TraceEn is set. 1: This field holds bits 31:0 of the offset pointer into the current ToPA output region. This value will be added to the output region base field, found in the current ToPA table entry, to form the physical address at which the next byte of trace output data will be written. This value must be less than the ToPA entry size, otherwise an operational error (Section 36.3.9) will be signaled when TraceEn is set.</td>
</tr>
</tbody>
</table>
36.2.6 Interaction of Intel® Processor Trace and Other Processor Features

36.2.6.1 Intel® Transactional Synchronization Extensions (Intel® TSX)

The operation of Intel TSX is described in Chapter 14 of the Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1. For tracing purpose, packet generation does not distinguish between hardware lock elision (HLE) and restricted transactional memory (RTM), but speculative execution does have impacts on the trace output. Specifically, packets are generated as instructions complete, even for instructions in a transactional region that is later aborted. For this reason, debugging software will need indication of the beginning and end of a transactional region; this will allow software to understand when instructions are part of a transactional region and whether that region has been committed.

To enable this, TSX information is included in a MODE packet leaf. The mode bits in the leaf are:

- **InTX**: Set to 1 on an TSX transaction begin, and cleared on transaction commit or abort.
- **TXAbort**: Set to 1 only when InTX transitions from 1 to 0 on an abort. Cleared otherwise.

If BranchEn=1, this MODE packet will be sent each time the transaction status changes. See Table 36-10 for details.

<table>
<thead>
<tr>
<th>TSX Event</th>
<th>Instruction</th>
<th>Packets</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transaction Begin</td>
<td>Either XBEGIN or XACQUIRE lock (the latter if executed transactionally)</td>
<td>MODE(TXAbort=0, InTX=1), FUP(CurrentIP)</td>
</tr>
<tr>
<td>Transaction Commit</td>
<td>Either XEND or XRELEASE lock, if transactional execution ends. This happens only on the outermost commit</td>
<td>MODE(TXAbort=0, InTX=0), FUP(CurrentIP)</td>
</tr>
<tr>
<td>Transaction Abort</td>
<td>XABORT or other transactional abort</td>
<td>MODE(TXAbort=1, InTX=0), FUP(CurrentIP), TIP(TargetIP)</td>
</tr>
<tr>
<td>Other</td>
<td>One of the following:</td>
<td>None. No change to TSX mode bits for these cases.</td>
</tr>
<tr>
<td></td>
<td>• Nested XBEGIN or XACQUIRE lock</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• An outer XACQUIRE lock that doesn’t begin a transaction (InTX not set)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Non-outermost XEND or XRELEASE lock</td>
<td></td>
</tr>
</tbody>
</table>

The CurrentIP listed above is the IP of the associated instruction. The TargetIP is the IP of the next instruction to be executed; for HLE, this is the XACQUIRE lock; for RTM, this is the fallback handler.

Intel PT stores are non-transactional, and thus packet writes are not rolled back on TSX abort.

**TSX and IP Filtering**

A complication with tracking transactions is handling transactions that start or end outside of the tracing region. Transactions can’t span across a change in ContextEn, because CPL changes and CR3 changes each cause aborts. But a transaction can start within the IP filter region and end outside it.

To assist the decoder handling this situation, MODE.TSX packets can be sent even if FilterEn=0, though there will be no FUP attached. Instead, they will merely serve to indicate to the decoder when transactions are active and when they are not. When tracing resumes (due to PacketEn=1), the last MODE.TSX preceding the TIP.PGE will indicate the current transaction status.

**System Management Mode (SMM)**

SMM code has special privileges that non-SMM code does not have. Intel Processor Trace can be used to trace SMM code, but special care is taken to ensure that SMM handler context is not exposed in any non-SMM trace collection. Additionally, packet output from tracing non-SMM code cannot be written into memory space that is either protected by SMRR or used by the SMM handler.

SMM is entered via a system management interrupt (SMI). SMI delivery saves the value of IA32_RTIT_CTL.TraceEn into SMRAM and then clears it, thereby disabling packet generation.
The saving and clearing of IA32_RTIT_CTL.TraceEn ensures two things:

1. All internally buffered packet data is flushed before entering SMM (see Section 36.2.5.2).

2. Packet generation ceases before entering SMM, so any tracing that was configured outside SMM does not continue into SMM. No SMM instruction pointers or other state will be exposed in the non-SMM trace.

When the RSM instruction is executed to return from SMM, the TraceEn value that was saved by SMI delivery is restored, allowing tracing to be resumed. As is done any time packet generation is enabled, ContextEn is re-evaluated, based on the values of CPL, CR3, etc., established by RSM.

Like other interrupts, delivery of an SMI produces a FUP containing the IP of the next instruction to execute. By toggling TraceEn, SMI and RSM can produce TIP.PGD and TIP.PGE packets, respectively, indicating that tracing was disabled or re-enabled. See Table 36.7 for more information about packets entering and leaving SMM.

Although #SMI and RSM change CR3, PIP packets are not generated in these cases. With #SMI tracing is disabled before the CR3 change; with RSM TraceEn is restored after CR3 is written.

TraceEn must be cleared before executing RSM, otherwise it will cause a shutdown. Further, on processors that restrict use of Intel PT with LBRs (see Section 36.3.1.2), any RSM that results in enabling of both will cause a shutdown.

Intel PT can support tracing of System Transfer Monitor operating in SMM, see Section 36.6.

36.2.6.2 Virtual-Machine Extensions (VMX)

Initial implementations of Intel Processor Trace do not support tracing in VMX operation. This is indicated by IA32_VMX_MISC[bit 14] returns 0. Execution of the VMXON instruction clears TraceEn. An attempt to set IA32_RTIT_CTL.TraceEn using WRMSR in VMX operation causes a general-protection fault (#GP).

For processors that Intel Processor Trace supports tracing in VMX operation, IA32_VMX_MISC[bit 14] reports 1 if TraceEn can be set post-VMXON. Details of tracing post-VMXON is described in Section 36.5.

36.2.6.3 Intel Software Guard Extensions (SGX)

SGX provides an application with ability to instantiate a protective container (an enclave) with confidentiality and integrity (see Intel® Software Guard Extensions Programming Reference). On a processor with both Intel PT and SGX enabled, when executing code within a production enclave, no control flow packets are produced by Intel PT. Enclave entry will clear ContextEn, thereby blocking control flow packet generation. A TIP.PGD packet will be generated if PacketEn=1 at the time of the entry.

Upon enclave exit, ContextEn will no longer be forced to 0. If other enables are set at the time, a TIP.PGE may be generated to indicate that tracing is resumed.

During the enclave execution, Intel PT remains enabled, and periodic or timing packets such as PSB, TSC, MTC, or CBR can still be generated. No IPs or other architectural state will be exposed.

For packet generation examples on enclave entry or exit, see Section 36.7.

Debug Enclaves

SGX allows an enclave to be configured with relaxed protection of confidentiality for debug purposes, see Intel® Software Guard Extensions Programming Reference. In a debug enclave, Intel PT continues to function normally. Specifically, ContextEn is not impacted by enclave entry or exit. Hence the generation of ContextEn-dependent packets within a debug enclave is allowed.

36.2.6.4 SENTER/ENTERACCS and ACM

GETSEC[SENDER] and GETSEC[ENTERACCS] instructions clear TraceEn, and it is not restored when those instruction complete. SENTER also causes TraceEn to be cleared on other logical processors when they rendezvous and enter the SENTER sleep state. In these two cases, the disabling of packet generation is not guaranteed to flush internally buffered packets. Some packets may be dropped.

When executing an authenticated code module (ACM), packet generation is silently disabled during ACRAM setup. TraceEn will be cleared, but no TIP.PGD packet is generated. After completion of the module, the TraceEn value will be restored. There will be no TIP.PGE packet, but timing packets, like TSC and CBR, may be produced.
36.2.6.5 Intel® Memory Protection Extensions (Intel® MPX)

Bounds exceptions (#BR) caused by Intel MPX are treated like other exceptions, producing FUP and TIP packets that indicate the source and destination IPs.

36.3 CONFIGURATION AND PROGRAMMING GUIDELINE

36.3.1 Detection of Intel Processor Trace and Capability Enumeration

Processor support for Intel Processor Trace is indicated by CPUID.(EAX=07H,ECX=0H):EBX[bit 25] = 1. CPUID function 14H is dedicated to enumerate the resource and capability of processors that report CPUID.(EAX=07H,ECX=0H):EBX[bit 25] = 1. Different processor generations may have architecturally-defined variation in capabilities. Table 36-11 describes details of the enumerable capabilities that software must use across generations of processors that support Intel Processor Trace.

Table 36-11. CPUID Leaf 14H Enumeration of Intel Processor Trace Capabilities

<table>
<thead>
<tr>
<th>CPUID.(EAX=14H,ECX=0)</th>
<th>Name</th>
<th>Description Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Register</strong></td>
<td><strong>Bits</strong></td>
<td><strong>Name</strong></td>
</tr>
<tr>
<td>EAX</td>
<td>31:0</td>
<td>Maximum valid sub-leaf Index</td>
</tr>
<tr>
<td>EBX</td>
<td>0</td>
<td>CR3 Filtering Support</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>Configurable PSB and Cycle-Accurate Mode Supported</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>IP Filtering and TraceStop supported, and Preserve Intel PT MSRs across warm reset</td>
</tr>
</tbody>
</table>
Table 36-11. CPUID Leaf 14H Enumeration of Intel Processor Trace Capabilities

<table>
<thead>
<tr>
<th>CPUID.(EAX=14H,ECX=0)</th>
<th>Name</th>
<th>Description Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Register</td>
<td>Bits</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>MTC Supported</td>
<td>1: IA32_RTIT_CTL.MTCEn can be set to 1, and MTC packets will be generated. See Section 36.2.5. 0: An attempt to set IA32_RTIT_CTL.MTCEn or IA32_RTIT_CTL.MTCFreq to a non-zero value will #GP fault.</td>
</tr>
<tr>
<td>31:4</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>ToPA Output Supported</td>
<td>1: Tracing can be enabled with IA32_RTIT_CTL.ToPA = 1, hence utilizing the ToPA output scheme (Section 36.2.4.2) IA32_RTIT_OUTPUT_BASE and IA32_RTIT_OUTPUT_MASK_PTRS MSRs can be accessed. 0: Unless CPUID.(EAX=14H, ECX=0):ECX.SNGLRNGOUT[bit 2] = 1, writes to IA32_RTIT_OUTPUT_BASE or IA32_RTIT_OUTPUT_MASK_PTRS. MSRs will #GP fault.</td>
</tr>
<tr>
<td>1</td>
<td>ToPA Tables Allow Multiple Output Entries</td>
<td>1: ToPA tables can hold any number of output entries, up to the maximum allowed by the MaskOrTableOffset field of IA32_RTIT_OUTPUT_MASK_PTRS. 0: ToPA tables can hold only one output entry, which must be followed by an END=1 entry which points back to the base of the table. Further, ToPA PMIs will be delivered before the region is filled. See ToPA PMI in Section 36.2.4.2. If there is more than one output entry before the END entry, or if the END entry has the wrong base address, an operational error will be signaled (see “ToPA Errors” in Section 36.2.4.2).</td>
</tr>
<tr>
<td>2</td>
<td>Single-Range Output Supported</td>
<td>1: Enabling tracing (TraceEn=1) with IA32_RTIT_CTL.ToPA=0 is supported. 0: Unless CPUID.(EAX=14H, ECX=0):ECX.TOPAOUT[bit 0] = 1, writes to IA32_RTIT_OUTPUT_BASE or IA32_RTIT_OUTPUT_MASK_PTRS. MSRs will #GP fault.</td>
</tr>
<tr>
<td>3</td>
<td>Output to Trace Transport Subsystem Supported</td>
<td>1: Setting IA32_RTIT_CTL.FabricEn to 1 is supported. 0: IA32_RTIT_CTL.FabricEn is reserved. Write 1 to IA32_RTIT_CTL.FabricEn will #GP fault.</td>
</tr>
<tr>
<td>30:4</td>
<td></td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>IP Payloads are LIP</td>
<td>1: Generated packets which contain IP payloads have LIP values, which include the CS base component. 0: Generated packets which contain IP payloads have RIP values, which are the offset from CS base.</td>
</tr>
<tr>
<td>EDX</td>
<td>31:0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

If CPUID.(EAX=14H, ECX=0):EAX reports a non-zero value, additional capabilities of Intel Processor Trace are described in the sub-leaves of CPUID leaf 14H.
36.3.1.1 Packet Decoding of RIP versus LIP

FUP, TIP, TIP.PGE, and TIP.PGE packets can contain an instruction pointer (IP) payload. On some processor generations, this payload will be an effective address (RIP), while on others this will be a linear address (LIP). In the former case, the payload is the offset from the current CS base address, while in the latter it is the sum of the offset
and the CS base address (Note that in real mode, the CS base address is the value of CS<<4, while in protected mode the CS base address is the base linear address of the segment indicated by the CS register). Which IP type is in use is indicated by enumeration (see CPUID.(EAX=14H, ECX=0):ECX.LIP[bit 31] in Table 36-11).

For software that executes while the CS base address is 0 (including all software executing in 64-bit mode), the difference is indistinguishable. A trace decoder must account for cases where the CS base address is not 0 and the resolved LIP will not be evident in a trace generated on a CPU that enumerates use of RIP. This is likely to cause problems when attempting to link the trace with the associated binaries.

Note that IP comparison logic, for IP filtering and TraceStop range calculation, is based on the same IP type as these IP packets. For processors that output RIP, the IP comparison mechanism is also based on RIP, and hence on those processors RIP values should be written to IA32_RTIT_ADDRn_[AB] MSRs. This can produce differing behavior if the same trace configuration setting is run on processors reporting different IP types, i.e. CPUID.(EAX=14H, ECX=0):ECX.LIP[bit 31]. Care should be taken to check CPUID when configuring IP filters.

36.3.1.2  Model Specific Capability Restrictions

Some processor generations impose restrictions that prevent use of LBRs/BTS/BTM/LERs when software has enabled tracing with Intel Processor Trace. On these processors, when TraceEn is set, updates of LBR, BTS, BTM, LERs are suspended but the states of the corresponding IA32_DEBUGCTL control fields remained unchanged as if it were still enabled. When TraceEn is cleared, the LBR array is reset, and LBR/BTS/BTM/LERs updates will resume. Further, reads of these registers will return 0, and writes will be dropped.

The list of MSRs whose updates/accesses are restricted follows.

• MSR_LASTBRANCH_x_TO_IP, MSR_LASTBRANCH_x_FROM_IP, MSR_LBR_INFO_x, MSR_LASTBRANCH_TOS
• MSR.Lerp_FROM_IP, MSR.Lerp_TO_IP
• MSR.LBR_SELECT

For processor with CPUID DisplayFamily_DisplayModel signature of 06_3DH, 06_47H, 06_4EH, 06_4FH, 06_56H and 06_5EH, the use of Intel PT and LBRs are mutually exclusive.

36.3.2 Enabling and Configuration of Trace Packet Generation

To configure trace packets, enable packet generation, and capture packets, software starts with using CPUID instruction to detect its feature flag, CPUID.(EAX=07H,ECX=0H):EBX[bit 25] = 1; followed by enumerating the capabilities described in Section 36.3.1.

Based on the capability queried from Section 36.3.1, software must configure a number of model-specific registers. This section describes programming considerations related to those MSRs.

36.3.2.1 Enabling Packet Generation

When configuring and enabling packet generation, the IA32_RTIT_CTL MSR should be written after any other Intel PT MSRs have been written, since writes to the other configuration MSRs cause a general-protection fault (#GP) if TraceEn = 1. If a prior trace collection context is not being restored, then software should first clear IA32_RTIT_STATUS. This is important since the Stopped, and Error fields are writable; clearing the MSR clears any values that may have persisted from prior trace packet collection contexts. See Section 36.2.5.2 for details of packets generated by setting TraceEn to 1.

If setting TraceEn to 1 causes an operational error (see Section 36.3.9), there may be a delay after the WRMSR completes before the error is signaled in the IA32_RTIT_STATUS MSR.

While packet generation is enabled, the values of some configuration MSRs (e.g., IA32_RTIT_STATUS and IA32_RTIT_OUTPUT_*) are transient, and reads may return values that are out of date. Only after packet generation is disabled (by clearing TraceEn) do reads of these MSRs return reliable values.

36.3.2.2 Disabling Packet Generation

After disabling packet generation by clearing IA32_RTIT_CTL, it is advisable to read the IA32_RTIT_STATUS MSR (Section 36.2.5.4):
• If the Error bit is set, an operational error was encountered, and the trace is most likely compromised. Software should check the source of the error (by examining the output MSR values), correct the source of the problem, and then attempt to gather the trace again. For details on operational errors, see Section 36.3.9. Software should clear IA32_RTIT_STATUS.Error before re-enabling packet generation.

• If the Stopped bit is set, software execution encountered an IP TraceStop (see Section 36.2.2.3) or the ToPA Stop condition (see “ToPA STOP” in Section 36.2.4.2) before packet generation was disabled.

36.3.3 Flushing Trace Output

Packets are first buffered internally and then written out asynchronously. To collect packet output for post-processing, a collector needs first to ensure that all packet data has been flushed from internal buffers. Software can ensure this by stopping packet generation by clearing IA32_RTIT_CTL.TraceEn (see “Disabling Packet Generation” in Section 36.2.5.2).

When software clears IA32_RTIT_CTL.TraceEn to flush out internally buffered packets, the logical processor issues an SFENCE operation which ensures that WC trace output stores will be ordered with respect to the next store, or serializing operation. A subsequent read from the same logical processor will see the flushed trace data, while a read from another logical processor should be preceded by a store, fence, or architecturally serializing operation on the tracing logical processor.

When the flush operations complete, the IA32_RTIT_OUTPUT_* MSR values indicate where the trace ended. While TraceEn is set, these MSRs may hold stale values.

36.3.4 Warm Reset

The MSRs software uses to program Intel Processor Trace are cleared after a power-on RESET (or cold RESET). On a warm RESET, the contents of those MSRs can retain their values from before the warm RESET with the exception that IA32_RTIT_CTL.TraceEn will be cleared (which may have the side effect of clearing some bits in IA32_RTIT_STATUS).

36.3.5 Context Switch Consideration

To facilitate construction of instruction execution traces at the granularity of a software process or thread context, software can save and restore the states of the trace configuration MSRs across the process or thread context switch boundary. The principle is the same as saving and restoring the typical architectural processor states across context switches.

36.3.5.1 Manual Trace Configuration Context Switch

The configuration can be saved and restored through a sequence of instructions of RDMSR, management of MSR content and WRMSR. To stop tracing and to ensure that all configuration MSRs contain stable values, software must clear IA32_RTIT_CTL.TraceEn before reading any other trace configuration MSRs. The recommended method for saving trace configuration context manually follows:

1. RDMSR IA32_RTIT_CTL, save value to memory
2. WRMSR IA32_RTIT_CTL with saved value from RDMSR above and TraceEn cleared
3. RDMSR all other configuration MSRs whose values had changed from previous saved value, save changed values to memory

When restoring the trace configuration context, IA32_RTIT_CTL should be restored last:

1. Read saved configuration MSR values, aside from IA32_RTIT_CTL, from memory, and restore them with WRMSR
2. Read saved IA32_RTIT_CTL value from memory, and restore with WRMSR.
36.3.5.2 Trace Configuration Context Switch Using XSAVES/XRSTORS

On processors whose XSAVE feature set supports XSAVES and XRSTORS, the Trace configuration state can be saved using XSAVES and restored by XRSTORS, in conjunction with the bit field associated with supervisory state component in IA32_XSS. See Chapter 13, “Managing State Using the XSAVE Feature Set” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

CPUID leaf ODH enumerates the capabilities of the XSAVE feature set. Within CPUID leaf ODH, the sub-functions related to supervisor state management of the trace configuration MSRs are shown in Table 36-13 and Table 36-14.

### Table 36-13. CPUID Leaf ODH, sub-leaf 1H Enumeration of XSAVE Feature Set

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit(s)</th>
<th>Name</th>
<th>Description Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECX</td>
<td>8</td>
<td>Supervisory Trace Configuration State support in IA32_XSS</td>
<td>If 1, IA32_XSS[bit 8] is supported for supervisor state save/restor using XSAVES/XRSTORS for trace configuration MSR states. Otherwise, IA32_XSS[bit 8] is reserved.</td>
</tr>
<tr>
<td>EBX</td>
<td>31:0</td>
<td>Total size of the XSAVE area</td>
<td>Total size of the XSAVE area containing all states enabled by XCR0</td>
</tr>
</tbody>
</table>

### Table 36-14. CPUID Leaf ODH, sub-leaf 8H Enumeration of XSAVE Feature Set

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit(s)</th>
<th>Name</th>
<th>Description Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>EAX</td>
<td>31:0</td>
<td>Size of Trace Configuration State Save Area</td>
<td>The size in bytes of this component’s save area in the XSAVE area (from the offset specified in EBX)</td>
</tr>
<tr>
<td>EBX</td>
<td>31:0</td>
<td>Offset of Trace Configuration State Save Area</td>
<td>The offset in bytes of this component’s save area from the beginning of the XSAVE area.</td>
</tr>
<tr>
<td>ECX</td>
<td>0</td>
<td>Valid</td>
<td>If 1, sub leaf index is valid and maps to IA32_XSS[bit 8]. Otherwise, sub leaf index is invalid.</td>
</tr>
</tbody>
</table>

The layout of the trace configuration component state in the XSAVE area is shown in Table 36-15.1

### Table 36-15. Memory Layout of the Trace Configuration State Component

<table>
<thead>
<tr>
<th>Offset within Component Area</th>
<th>Field</th>
<th>Offset within Component Area</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>0H</td>
<td>IA32_RTIT_CTL</td>
<td>08H</td>
<td>IA32_RTIT_OUTPUT_BASE</td>
</tr>
<tr>
<td>10H</td>
<td>IA32_RTIT_OUTPUT_MASK_PTRS</td>
<td>18H</td>
<td>IA32_RTIT_STATUS</td>
</tr>
<tr>
<td>20H</td>
<td>IA32_RTIT_CR3_MATCH</td>
<td>28H</td>
<td>IA32_RTIT_ADDR0_A</td>
</tr>
<tr>
<td>30H</td>
<td>IA32_RTIT_ADDR0_B</td>
<td>38H</td>
<td>IA32_RTIT_ADDR1_A</td>
</tr>
<tr>
<td>40H</td>
<td>IA32_RTIT_ADDR1_B</td>
<td>48H-End</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The IA32_XSS MSR is zero coming out of RESET. Once IA32_XSS[bit 8] is set, system software operating at CPL=0 can use XSAVES/XRSTORS with the appropriate requested-feature bitmap (RFBM) to manage supervisor state components in the XSAVE map. See Chapter 13, “Managing State Using the XSAVE Feature Set” of Intel® 64 and IA-32 Architectures Software Developer’s Manual, Volume 1.

1. Table 36-15 documents support for the MSRs defining address ranges 0 and 1. Processors that provide XSAVE support for Intel Processor Trace support only those address ranges.
36.3.6 Cycle-Accurate Mode

Intel PT can be run in a cycle-accurate mode which enables CYC packets (see Section 36.4.2.14) that provide low-level information in the processor core clock domain. This cycle counter data in CYC packets can be used to compute IPC (Instructions Per Cycle), or to track wall-clock time on a fine-grain level.

To enable cycle-accurate mode packet generation, software should set IA32_RTIT_CTL.CYCEn=1. It is recommended that software also set TSCEn=1 anytime cycle-accurate mode is in use. With this, all CYC-eligible packets will be preceded by a CYC packet, the payload of which indicates the number of core clock cycles since the last CYC packet. In cases where multiple CYC-eligible packets are generated in a single cycle, only a single CYC will be generated before the CYC-eligible packets, otherwise each CYC-eligible packet will be preceded by its own CYC. The CYC-eligible packets are:
- TNT, TIP, TIP.PGE, TIP.PGD, MODE.EXEC, MODE.TSX, PIP, VMCS, OVF, MTC, TSC

TSC packets are generated when there is insufficient information to reconstruct wall-clock time, due to tracing being disabled (TriggerEn=0), or power down scenarios like a transition to a deep-sleep MWAIT C-state. In this case, the CYC that is generated along with the TSC will indicate the number of cycles actively tracing (those powered up, with TriggerEn=1) executed between the last CYC packet and the TSC packet. And hence the amount of time spent while tracing is inactive can be inferred from the difference in time between that expected based on the CYC value, and the actual time indicated by the TSC.

Additional CYC packets may be sent stand-alone, so that the processor can ensure that the decoder is aware of the number of cycles that have passed before the internal hardware counter wraps, or is reset due to other micro-architectural condition. There is no guarantee at what intervals these standalone CYC packets will be sent, except that they will be sent before the wrap occurs. An illustration is given below.

Example 36-1. An Illustrative CYC Packet Example

<table>
<thead>
<tr>
<th>Time (cycles)</th>
<th>Instruction Snapshot</th>
<th>Generated Packets</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>call %eax</td>
<td>CYC(?), TIP</td>
<td>?Elapsed cycles from the previous CYC unknown</td>
</tr>
<tr>
<td>x + 2</td>
<td>call %ebx</td>
<td>CYC(2), TIP</td>
<td>1 byte CYC packet; 2 cycles elapsed from the previous CYC</td>
</tr>
<tr>
<td>x + 8</td>
<td>jnz Foo (not taken)</td>
<td>CYC(6)</td>
<td>1 byte CYC packet</td>
</tr>
<tr>
<td>x + 9</td>
<td>ret (compressed)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>x + 12</td>
<td>jnz Bar (taken)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>x + 16</td>
<td>ret (uncompressed)</td>
<td>TNT, CYC(8), TIP</td>
<td>1 byte CYC packet</td>
</tr>
<tr>
<td>x + 4111</td>
<td></td>
<td>CYC(4095)</td>
<td>2 byte CYC packet</td>
</tr>
<tr>
<td>x + 12305</td>
<td></td>
<td>CYC(8194)</td>
<td>3 byte CYC packet</td>
</tr>
<tr>
<td>x + 16332</td>
<td>mov cr3, %ebx</td>
<td>CYC(4027), PIP</td>
<td>2 byte CYC packet</td>
</tr>
</tbody>
</table>

36.3.6.1 Cycle Counter

The cycle counter is implemented in hardware (independent of the time stamp counter or performance monitoring counters), and is a simple incrementing counter that does not saturate, but rather wraps. The size of the counter is implementation specific.

The cycle counter is reset to zero any time that TriggerEn is cleared, and when a CYC packet is sent. The cycle counter will continue to count when ContextEn or FilterEn are cleared, and cycle packets will still be generated. It will not count during sleep states that result in Intel PT logic being powered-down, but will count up to the point where clocks are disabled, and resume counting once they are re-enabled.

36.3.6.2 Cycle Packet Semantics

Cycle-accurate mode adheres to the following protocol:
- All packets that precede a CYC packet represent instructions or events that took place before the CYC time.
- All packets that follow a CYC packet represent instructions or events that took place at the same time as, or after, the CYC time.
The CYC-eligible packet that immediately follows a CYC packet represents an instruction or event that took place at the same time as the CYC time.

These items above give the decoder a means to apply CYC packets to a specific instruction in the assembly stream. Most packets represent a single instruction or event, and hence the CYC packet that precedes each of those packets represents the retirement time of that instruction or event. In the case of TNT packets, up to 6 conditional branches and/or compressed RETs may be contained in the packet. In this case, the preceding CYC packet provides the retirement time of the first branch in the packet. It is possible that multiple branches retired in the same cycle as that first branch in the TNT, but the protocol will not make that obvious. Also note that a MTC packet could be generated in the same cycle as the first JCC in the TNT packet. In this case, the CYC would precede both the MTC and the TNT, and apply to both.

Note that there are times when the cycle counter will stop counting, though cycle-accurate mode is enabled. After any such scenario, a CYC packet followed by TSC packet will be sent. See Section 36.8.3.2 to understand how to interpret the payload values.

### Multi-packet Instructions or Events

Some operations, such as interrupts or task switches, generate multiple packets. In these cases, multiple CYC packets may be sent for the operation, preceding each CYC-eligible packet in the operation. An example, using a task switch on a software interrupt, is shown below.

#### Example 36.2. An Example of CYC in the Presence of Multi-Packet Operations

<table>
<thead>
<tr>
<th>Time (cycles)</th>
<th>Instruction Snapshot</th>
<th>Generated Packets</th>
</tr>
</thead>
<tbody>
<tr>
<td>x</td>
<td>jnz Foo (not taken)</td>
<td>CYC(?)</td>
</tr>
<tr>
<td>x + 2</td>
<td>ret (compressed)</td>
<td></td>
</tr>
<tr>
<td>x + 8</td>
<td>jnz Bar (taken)</td>
<td></td>
</tr>
<tr>
<td>x + 9</td>
<td>jmp %eax</td>
<td>TNT, CYC(9), TIP</td>
</tr>
<tr>
<td>x + 12</td>
<td>jnz Bar (not taken)</td>
<td>CYC(3)</td>
</tr>
<tr>
<td>x + 32</td>
<td>int3 (task gate)</td>
<td>TNT, FUP, CYC(10), PIP, CYC(20), MODE.Exec, TIP</td>
</tr>
</tbody>
</table>

#### 36.3.6.3 Cycle Thresholds

Software can opt to reduce the frequency of cycle packets, a trade-off to save bandwidth and intrusion at the expense of precision. This is done by utilizing a cycle threshold (see Section 36.2.5.2).

IA32_RTIT_CTL.CycThresh indicates to the processor the minimum number of cycles that must pass before the next CYC packet should be sent. If this value is 0, no threshold is used, and CYC packets can be sent every cycle in which a CYC-eligible packet is generated. If this value is greater than 0, the hardware will wait until the associated number of cycles have passed since the last CYC packet before sending another. CPUID provides the threshold options for CycThresh, see Section 36.3.1.

Note that the cycle threshold does not dictate how frequently a CYC packet will be posted, it merely assigns the maximum frequency. If the cycle threshold is 16, a CYC packet can be posted no more frequently than every 16 cycles. However, once that threshold of 16 cycles has passed, it still requires a new CYC-eligible packet to be generated before a CYC will be inserted. Table 36-16 illustrates the threshold behavior.

#### Table 36-16. An Illustrative CYC Packet Example

<table>
<thead>
<tr>
<th>Time (cycles)</th>
<th>Instruction Snapshot</th>
<th>Threshold</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>x</td>
<td>jmp %eax</td>
<td>CYC, TIP</td>
</tr>
<tr>
<td>x + 9</td>
<td>call %ebx</td>
<td>CYC, TIP</td>
</tr>
<tr>
<td>x + 15</td>
<td>call %ecx</td>
<td>CYC, TIP</td>
</tr>
<tr>
<td>x + 30</td>
<td>jmp %edx</td>
<td>CYC, TIP</td>
</tr>
<tr>
<td>x + 38</td>
<td>mov cr3,%eax</td>
<td>CYC, PIP</td>
</tr>
</tbody>
</table>
36.3.7 Decoder Synchronization (PSB+)

The PSB packet (Section 36.4.2.17) serves as a synchronization point for a trace-packet decoder. It is a pattern in the trace log for which the decoder can quickly scan to align packet boundaries. No legal packet combination can result in such a byte sequence. As such, it serves as the starting point for packet decode. To decode a trace log properly, the decoder needs more than simply to be aligned: it needs to know some state and potentially some timing information as well. The decoder should never need to retain any information (e.g., LastIP, call stack, compound packet event) across a PSB; all compound packet events will be completed before a PSB, and any compression state will be reset.

When a PSB packet is generated, it is followed by a PSBEND packet (Section 36.4.2.18). One or more packets may be generated in between those two packets, and these inform the decoder of the current state of the processor. These packets, known collectively as PSB+, should be interpreted as "status only", since they do not imply any change of state at the time of the PSB, nor are they associated directly with any instruction or event. Thus, the normal binding and ordering rules that apply to these packets outside of PSB+ can be ignored when these packets are between a PSB and PSBEND. They inform the decoder of the state of the processor at the time of the PSB.

PSB+ can include:
- Timestamp (TSC), if IA32_RTIT_CTL.TSCEn=1
- Timestamp-MTC Align (TMA), if IA32_RTIT_CTL.TSCEn=1 && IA32_RTIT_CTL.MTCEn=1
- Paging Info Packet (PIP), if ContextEn=1 and IA32_RTIT_CTL.OS=1
  - Includes non-Root (NR) field, if the “Suppress VMX Indications in Guest Traces” VMCS execution control is cleared
- VMCS, if post-VMXON and the “Suppress VMX Indications in Guest Traces” VMCS execution control is cleared
- Core Bus Ratio (CBR)
- MODE.TSX, if ContextEn=1 and BranchEn = 1.
- MODE.Exec, if PacketEn=1.
- Flow Update Packet (FUP), if PacketEn=1.

PSB is generated only when TriggerEn=1; hence PSB+ has the same dependencies. The ordering of packets within PSB+ is not fixed. Timing packets such as CYC and MTC may be generated between PSB and PSBEND, and their meanings are the same as outside PSB+.

Note that an overflow can occur during PSB+, and this could cause the PSBEND packet to be lost. For this reason, the OVF packet should also be viewed as terminating PSB+.

36.3.8 Internal Buffer Overflow

In the rare circumstances when new packets need to be generated but the processor’s dedicated internal buffers are all full, an “internal buffer overflow” occurs. On such an overflow packet generation ceases (as packets would need to enter the processor’s internal buffer) until the overflow resolves. Once resolved, packet generation resumes.

When the buffer overflow is cleared, an OVF packet (Section 36.4.2.16) is generated, and the processor ensures that packets which follow the OVF are not compressed (IP compression or RET compression) against packets that were lost.
If IA32_RTIT_CTL.BranchEn = 1, the OVF packet will be followed by a FUP if the overflow resolves while PacketEn=1. If the overflow resolves while PacketEn = 0 no packet is generated, but a TIP.PGE will naturally be generated later, once PacketEn = 1. The payload of the FUP or TIP.PGE will be the Current IP of the first instruction upon which tracing resumes after the overflow is cleared. Between the OVF and following FUP or TIP.PGE, there may be packets that do not depend on PacketEn, such as timing packets. If the overflow resolves while PacketEn=0, other packets that are not dependent on PacketEn may come before the TIP.PGE.

36.3.8.1 Overflow Impact on Enables

The address comparisons to ADDRn ranges, for IP filtering and TraceStop (Section 36.2.2.3), continue during a buffer overflow, and TriggerEn, ContextEn, and FilterEn may change during a buffer overflow. Like other packets, however, any TIP.PGE or TIP.PGD packets that would have been generated will be lost. Further, IA32_RTIT_STATUS.PacketByteCnt will not increment, since it is only incremented when packets are generated. If a TraceStop event occurs during the buffer overflow, IA32_RTIT_STATUS.Stopped will still be set, tracing will cease as a result. However, the TraceStop packet, and any TIP.PGD that result from the TraceStop, may be dropped.

36.3.8.2 Overflow Impact on Timing Packets

Any timing packets that are generated during a buffer overflow will be dropped. If only a few MTC packets are dropped, a decoder should be able to detect this by noticing that the time value in the first MTC packet after the buffer overflow incremented by more than one. If the buffer overflow lasted long enough that 256 MTC packets are lost (and thus the MTC packet ‘wraps’ its 8-bit CTC value), then the decoder may be unable to properly understand the trace. This is not an expected scenario. No CYC packets are generated during overflow, even if the cycle counter wraps.

Note that, if cycle-accurate mode is enabled, the OVF packet will generate a CYC packet. Because the cycle counter counts during overflows, this CYC packet can provide the duration of the overflow. However, there is a risk that the cycle counter wrapped during the overflow, which could render this CYC misleading.

36.3.9 Operational Errors

Errors are detected as a result of packet output configuration problems, which can include output alignment issues, ToPA reserved bit violations, or overlapping packet output with restricted memory. See “ToPA Errors” in Section 36.2.4.2 for details on ToPA errors, and Section 36.2.4.4 for details on restricted memory errors. Operational errors are only detected and signaled when TraceEn=1.

When an operational error is detected, tracing is disabled and the error is logged. Specifically, IA32_RTIT_STATUS.Error is set, which will cause IA32_RTIT_STATUS.TriggerEn to be 0. This will disable generation of all packets. Some causes of operational errors may lead to packet bytes being dropped.

It should be noted that the timing of error detection may not be predictable. Errors are signaled when the processor encounters the problematic configuration. This could be as soon as packet generation is enabled but could also be later when the problematic entry or field needs to be used.

Once an error is signaled, software should disable packet generation by clearing TraceEn, diagnose and fix the error condition, and clear IA32_RTIT_STATUS.Error. At this point, packet generation can be re-enabled.

36.4 TRACE PACKETS AND DATA TYPES

This section details the data packets generated by Intel Processor Trace. It is useful for developers writing the interpretation code that will decode the data packets and apply it to the traced source code.

36.4.1 Packet Relationships and Ordering

This section introduces the concept of packet “binding”, which involves determining the IP in a binary disassembly at which the change indicated by a given packet applies. Some packets have the associated IP as the payload (FUP,
INTEL® PROCESSOR TRACE

TIP), while for others the decoder need only search for the next instance of a particular instruction (or instructions) to bind the packet (TNT). However, in many cases, the decoder will need to consider the relationship between packets, and to use this packet context to determine how to bind the packet.

Section 36.4.2 below provides detailed descriptions of the packets, including how packets bind to IPs in the disassembly, to other packets, or to nothing at all. Many packets listed are simple to bind, because they are generated in only a few scenarios. Those that require more consideration are typically part of “compound packet events”, such as interrupts, exceptions, and some instructions, where multiple packets are generated by a single operation (instruction or event). These compound packet events frequently begin with a FUP to indicate the source address (if it is not clear from the disassembly), and are concluded by a TIP or TIP.PGD packet that indicates the destination address (if one is provided). In this scenario, the FUP is said to be “coupled” with the TIP packet.

Other packets could be in between the coupled FUP and TIP packet. Timing packets, such as TSC, MTC, CYC, or CBR, could arrive at any time, and hence could intercede in a compound packet event. If an operation changes CR3 or the processor’s mode of execution, a state update packet (i.e., PIP or MODE) is generated. The state changes indicated by these intermediate packets should be applied at the IP of the TIP* packet. A summary of compound packet events is provided in Table 36-17; see Section 36.4.2 for more per-packet details and Section 36.7 for more detailed packet generation examples.

36.4.2 Packet Definitions

The following description of packet definitions are in tabular format. Figure 36-3 explains how to interpret them. Packet bits listed as “RSVD” are not guaranteed to be 0.

<table>
<thead>
<tr>
<th>Event Type</th>
<th>Beginning</th>
<th>Middle</th>
<th>End</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unconditional uncompresed control-flow transfer</td>
<td>FUP or none</td>
<td>Any combination of PIP, VMCS, MODE.Exec, or none</td>
<td>TIP or TIP.PGD</td>
<td>FUP only for asynchronous events. Order of middle packets may vary. PIP/VMCS/MODE only if the operation modifies the state tracked by these respective packets</td>
</tr>
<tr>
<td>TSX Update</td>
<td>MODE.TSX, and (FUP or none)</td>
<td>None</td>
<td>TIP, TIP.PGD, or none</td>
<td>FUP</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>TIP/TIP.PGD only for TSX abort cases</td>
</tr>
<tr>
<td>Overflow</td>
<td>OVF</td>
<td>PSB, PSBEND, or none</td>
<td>FUP or TIP.PGE</td>
<td>FUP if overflow resolves while ContextEn=1, else TIP.PGE.</td>
</tr>
</tbody>
</table>

Table 36-17. Compound Packet Event Summary
36.4.2.1 Taken/Not-taken (TNT) Packet

<table>
<thead>
<tr>
<th>Name</th>
<th>Taken/Not-taken (TNT) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>7</strong></td>
</tr>
<tr>
<td></td>
<td><strong>0</strong></td>
</tr>
<tr>
<td></td>
<td><strong>1</strong></td>
</tr>
</tbody>
</table>

B1…BN represent the last N conditional branch or compressed RET (Section 36.4.2.2) results, such that B1 is oldest and BN is youngest. The short TNT packet can contain from 1 to 6 TNT bits. The long TNT packet can contain up from 1 to 47 TNT bits.
Irrespective of how many TNT bits is in a packet, the last valid TNT bit is followed by a trailing 1, or Stop bit, as shown above. If the TNT packet is not full (fewer than 6 TNT bits for the Short TNT, or fewer than 47 TNT bits for the Long TNT), the Stop bit moves up, and the trailing bits of the packet are filled with 0s. Examples of these “partial TNTs” are shown below.

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>PacketEn</th>
<th>Generation Scenario</th>
<th>Description</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>On a conditional branch or compressed RET, if it fills the TNT. Also, partial TNTs may be generated at any time, as a result of other packets being generated, or certain micro-architectural conditions occurring, before the TNT is full.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Provides the taken/not-taken results for the last 1–N conditional branches (Jcc, J*CXZ, or LOOP) or compressed RETs (Section 36.4.2.2). The TNT payload bits should be interpreted as follows:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1 indicates a taken conditional branch, or a compressed RET</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0 indicates a not-taken conditional branch</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Each valid payload bit (that is, bits between the header bits and the trailing Stop bit) applies to an upcoming conditional branch or RET instruction. Once a decoder consumes a TNT packet with N valid payload bits, these bits should be applied to (and hence provide the destination for) the next N conditional branches or RETs</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 36-18. TNT Packet Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Irrespective of how many TNT bits is in a packet, the last valid TNT bit is followed by a trailing 1, or Stop bit, as shown above. If the TNT packet is not full (fewer than 6 TNT bits for the Short TNT, or fewer than 47 TNT bits for the Long TNT), the Stop bit moves up, and the trailing bits of the packet are filled with 0s. Examples of these “partial TNTs” are shown below.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short TNT</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>B1</td>
<td>B2</td>
<td>B3</td>
<td>B4</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Long TNT</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>B24</td>
<td>B25</td>
<td>B26</td>
<td>B27</td>
<td>B28</td>
<td>B29</td>
<td>B30</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>B16</td>
<td>B17</td>
<td>B18</td>
<td>B19</td>
<td>B20</td>
<td>B21</td>
<td>B22</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>B8</td>
<td>B9</td>
<td>B10</td>
<td>B11</td>
<td>B12</td>
<td>B13</td>
<td>B14</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>1</td>
<td>B1</td>
<td>B2</td>
<td>B3</td>
<td>B4</td>
<td>B5</td>
<td>B6</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
### 36.4.2.2 Target IP (TIP) Packet

#### Table 36-19. IP Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Target IP (TIP) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>IPBytes</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Dependencies</td>
<td></td>
</tr>
<tr>
<td>PacketEn</td>
<td></td>
</tr>
<tr>
<td>Generation Scen-</td>
<td></td>
</tr>
<tr>
<td>ario</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>Indirect branch (including un-compressed RET), far branch, interrupt, exception, INIT,</td>
</tr>
<tr>
<td></td>
<td>SIPI, (VM exit, VM entry,)(^1) TSX abort, (EENTER, EEXIT, ERESUME, AEX)(^2).</td>
</tr>
<tr>
<td>Description</td>
<td></td>
</tr>
<tr>
<td>Provides the target for some control flow transfers</td>
<td></td>
</tr>
<tr>
<td>Application</td>
<td></td>
</tr>
<tr>
<td>Anytime a TIP is encountered, it indicates that control was transferred to the IP provided in the payload.</td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. If IA32_VMX_MISC[bit 14] reports 1.
2. In a debug enclave.

### IP Compression

The IP payload in a TIP. FUP, TIP.PGE, or TIP.PGD packet can vary in size, based on the mode of execution, and the use of IP compression. IP compression is an optional compression technique the processor may choose to employ to reduce bandwidth. With IP compression, the IP to be represented in the payload is compared with the last IP sent out, via any of FUP, TIP, TIP.PGE, or TIP.PGD. If that previous IP had the same upper (most significant) address bytes, those matching bytes may be suppressed in the current packet. The processor maintains an internal state of the “Last IP” that was encoded in trace packets, thus the decoder will need to keep track of the “Last IP” state in software, to match fidelity with packets generated by hardware. “Last IP” is initialized to zero, hence if the first IP in the trace may be compressed if the upper bytes are zeroes.

The “IPBytes” field of the IP packets (FUP, TIP, TIP.PGE, TIP.PGD) serves to indicate how many bytes of payload are provided, and how the decoder should fill in any suppressed bytes. The algorithm for reconstructing the IP for a TIP/FUP packet is shown in the table below.
The processor-internal Last IP state is guaranteed to be reset to zero when a PSB is sent out. This means that the IP that follows the PSB with either be un-compressed (011b or 110b, see Table 36-20), or compressed against zero.

At times, "IPbytes" will have a value of 0. As shown above, this does not mean that the IP payload matches the full address of the last IP, but rather that the IP for this packet was suppressed. This is used for cases where the IP that applies to the packet is out of context. An example is the TIP.PGD sent on a SYSCALL, when tracing only USR code. In that case, no TargetIP will be included in the packet, since that would expose an instruction point at CPL = 0. When the IP payload is suppressed in this manner, Last IP is not cleared, and instead refers to the last IP packet with a non-zero IPBytes field.

On processors that support a maximum linear address size of 32 bits, IP payloads may never exceed 32 bits (IPBytes <= 010b).

Indirect Transfer Compression for Returns (RET)

In addition to IP compression, TIP packets for near return (RET) instructions can also be compressed. If the RET target matches the next IP of the corresponding CALL, then the TIP packet is unneeded, since the decoder can deduce the target IP by maintaining a CALL/RET stack of its own.

A CALL/RET stack can be maintained by the decoder by doing the following:

1. Allocate space to store 64 RET targets.

2. For near CALLs, push the Next IP onto the stack. Once the stack is full, new CALLs will force the oldest entry off the end of the stack, such that only the youngest 64 entries are stored. Note that this excludes zero-length CALLs, which are direct near CALLs with displacement zero (to the next IP). These CALLs typically don’t have matching RETs.

3. For near RETs, pop the top (youngest) entry off the stack. This will be the target of the RET.

In cases where the RET is compressed, the target is guaranteed to match the value produced in 2) above. If the target is not compressed, a TIP packet will be generated with the RET target, which may differ from 2).

The hardware ensure that packets read by the decoder will always have seen the CALL that corresponds to any compressed RET. The processor will never compress a RET across a PSB, a buffer overflow, or scenario where PacketEn=0. This means that a RET whose corresponding CALL executed while PacketEn=0, or before the last PSB, etc., will not be compressed.

If the CALL/RET stack is manipulated or corrupted by software, and thereby causes a RET to transfer control to a target that is inconsistent with the CALL/RET stack, then the RET will not be compressed, and will produce a TIP packet. This can happen, for example, if software executes a PUSH instruction to push a target onto the stack, and a later RET uses this target.

When a RET is compressed, a Taken indication is added to the TNT buffer. Because it sends no TIP packet, it also does not update the internal Last IP value, and thus the decoder should treat it the same way. If the RET is not compressed, it will generate a TIP packet (just like when RET compression is disabled, via IA32_RTIT_CTL.DisRETC). For processors that employ deferred TIPs (Section 36.4.2.3), an uncompressed RET will not be deferred, and hence will force out any accumulated TNTs or TIPs. This serves to avoid ambiguity, and make

<table>
<thead>
<tr>
<th>IPBytes</th>
<th>Uncompressed IP Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>000b</td>
<td>None, IP is out of context</td>
</tr>
<tr>
<td>001b</td>
<td>Last IP[63:16] IP Payload[15:0]</td>
</tr>
<tr>
<td>010b</td>
<td>Last IP[63:32] IP Payload[31:0]</td>
</tr>
<tr>
<td>011b</td>
<td>IP Payload[47] extended IP Payload[47:0]</td>
</tr>
<tr>
<td>100b</td>
<td>Last IP[63:48] IP Payload[47:0]</td>
</tr>
<tr>
<td>101b</td>
<td>Reserved</td>
</tr>
<tr>
<td>110b</td>
<td>IP Payload[63:0]</td>
</tr>
<tr>
<td>111b</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Table 36-20. FUP/TIP IP Reconstruction
clear to the decoder whether the near RET was compressed, and hence a bit in the in-progress TNT should be consumed, or uncompressed, in which case there will be no in-progress TNT and thus a TIP should be consumed. Note that in the unlikely case that a RET executes in a different execution mode than the associated CALL, the decoder will need to model the same behavior with its CALL stack. For instance, if a CALL executes in 64-bit mode, a 64-bit IP value will be pushed onto the software stack. If the corresponding RET executes in 32-bit mode, then only the lower 32 target bits will be popped off of the stack, which may mean that the RET does not go to the CALL’s Next IP. This is architecturally correct behavior, and this RET could be compressed, thus the decoder should match this behavior.

### 36.4.2.3 Deferred TIPs

The processor may opt to defer sending out the TNT when TIPs are generated. Thus, rather than sending a partial TNT followed by a TIP, both packets will be deferred while the TNT accumulates more Jcc/RET results. Any number of TIP packets may be accumulated this way, such that only once the TNT is filled, or once another packet (e.g., FUP) is generated, the TNT will be sent, followed by all the deferred TIP packets, and finally terminated by the other packet(s) that forced out the TNT and TIP packets. Generation of many other packets (see list below) will force out the TNT and any accumulated TIP packets. This is an optional optimization in hardware to reduce the bandwidth consumption, and hence the performance impact, incurred by tracing.

**Table 36-21. TNT Examples with Deferred TIPs**

<table>
<thead>
<tr>
<th>Code Flow</th>
<th>Packets, Non-Deferred TIPS</th>
<th>Packets, Deferred TIPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1000 cmp %rcx, 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1004 jnz Foo // not-taken</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1008 jmp %rdx</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1308 cmp %rcx, 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x130c jnz Bar // not-taken</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1310 cmp %rcx, 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1314 jnz Baz // taken</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1500 cmp %eax, 7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1504 jg Exit // not-taken</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1508 jmp %r15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1100 cmp %rbx, 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1104 jg Start // not-taken</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1108 add %rcx, %eax</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x110c ... // an asynchronous Interrupt arrives</td>
<td></td>
<td></td>
</tr>
<tr>
<td>INTHandler:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Oxcc00 pop %rdx</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The processor may opt to defer sending out the TNT when TIPs are generated. Thus, rather than sending a partial TNT followed by a TIP, both packets will be deferred while the TNT accumulates more Jcc/RET results. Any number of TIP packets may be accumulated this way, such that only once the TNT is filled, or once another packet (e.g., FUP) is generated, the TNT will be sent, followed by all the deferred TIP packets, and finally terminated by the other packet(s) that forced out the TNT and TIP packets. Generation of many other packets (see list below) will force out the TNT and any accumulated TIP packets. This is an optional optimization in hardware to reduce the bandwidth consumption, and hence the performance impact, incurred by tracing.
### 36.4.2.4 Packet Generation Enable (TIP.PGE)

#### Table 36-22. TIP.PGE Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Target IP - Packet Generation Enable (TIP.PGE)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Target IP Byte</td>
</tr>
<tr>
<td>0</td>
<td>IPBytes</td>
</tr>
<tr>
<td>1</td>
<td>TargetIP[7:0]</td>
</tr>
<tr>
<td>2</td>
<td>TargetIP[15:8]</td>
</tr>
<tr>
<td>3</td>
<td>TargetIP[23:16]</td>
</tr>
<tr>
<td>4</td>
<td>TargetIP[31:24]</td>
</tr>
<tr>
<td>5</td>
<td>TargetIP[39:32]</td>
</tr>
<tr>
<td>6</td>
<td>TargetIP[47:40]</td>
</tr>
<tr>
<td>7</td>
<td>TargetIP[55:48]</td>
</tr>
<tr>
<td>8</td>
<td>TargetIP[63:56]</td>
</tr>
</tbody>
</table>

**Dependencies**
PacketEn transitions to 1

**Generation Scenario**
Any branch instruction, control flow transfer, or MOV CR3 that sets PacketEn, a WRMSR that enables packet generation and sets PacketEn

**Description**
Indicates that PacketEn has transitioned to 1. It provides the IP at which the tracing begins. This can occur due to any of the enables that comprise PacketEn transitioning from 0 to 1, as long as all the others are asserted. Examples:

- **TriggerEn**: This is set on software write to set IA32_RTIT_CTL.TraceEn as long as the Stopped and Error bits in IA32_RTIT_STATUS are clear. The IP payload will be the Next IP of the WRMSR.
- **FilterEn**: This is set when software jumps into the tracing region. This region is defined by enabling IP filtering in IA32_RTIT_CTL.ADDRn_CFG, and defining the range in IA32_RTIT_ADDRn_AB[AB], see Section 36.2.2.3. The IP payload will be the target of the branch.
- **ContextEn**: This is set on a CPL change, a CR3 write or any other means of changing ContextEn. The IP payload will be the Next IP of the instruction that changes context if it is not a branch, otherwise it will be the target of the branch.

**Application**
TIP.PGE packets bind to the instruction at the IP given in the payload.
## 36.4.2.5 Packet Generation Disable (TIP.PGD)

### Table 36-23. TIP.PGD Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Target IP - Packet Generation Disable (TIP.PGD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>IPBytes</td>
</tr>
<tr>
<td>1</td>
<td>TargetIP[7:0]</td>
</tr>
<tr>
<td>2</td>
<td>TargetIP[15:8]</td>
</tr>
<tr>
<td>3</td>
<td>TargetIP[23:16]</td>
</tr>
<tr>
<td>4</td>
<td>TargetIP[31:24]</td>
</tr>
<tr>
<td>5</td>
<td>TargetIP[39:32]</td>
</tr>
<tr>
<td>6</td>
<td>TargetIP[47:40]</td>
</tr>
<tr>
<td>7</td>
<td>TargetIP[55:48]</td>
</tr>
<tr>
<td>8</td>
<td>TargetIP[63:56]</td>
</tr>
</tbody>
</table>

### Dependencies

<table>
<thead>
<tr>
<th>PacketEn transitions to 0</th>
<th>Generation Scenario</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Any branch instruction, control flow transfer, or MOV CR3 that clears PacketEn, a WRMSR that disables packet generation and clears PacketEn</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Application

TIP.PGD can be produced by any branch instructions, as well as some non-branch instructions, that clear PacketEn. When produced by a branch, it replaces any TIP or TNT update that the branch would normally produce. In cases where there is an unbound FUP preceding the TIP.PGD, then the TIP.PGD is part of compound operation (i.e., asynchronous event or TSX abort) which cleared PacketEn. For most such cases, the TIP.PGD is simply replacing a TIP, and should be treated the same way. The TIP.PGD may or may not have an IP payload, depending on whether the operation cleared ContextEn. If there is not an associated FUP, the binding will depend on whether there is an IP payload. If there is an IP payload, then the TIP.PGD should be applied to either the next direct branch whose target matches the TIP.PGD payload, or the next branch that would normally generate a TIP or TNT packet. If there is no IP payload, then the TIP.PGD should apply to the next branch or MOV CR3 instruction.
### 36.4.2.6 Flow Update (FUP) Packet

<table>
<thead>
<tr>
<th>Name</th>
<th>Flow Update (FUP) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td><img src="image" alt="Packet Format" /></td>
</tr>
</tbody>
</table>

**Table 36-24. FUP Packet Definition**

<table>
<thead>
<tr>
<th>IP Bytes</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>IPBytes</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>IP[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>IP[15:8]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>IP[23:16]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>IP[31:24]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>IP[39:32]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>IP[47:40]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>IP[55:48]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>IP[63:56]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Dependencies**
TriggerEn & ContextEn.
(Typically depends on BranchEn and FilterEn as well, see Section 36.2.2 for details.)

**Generation Scenario**
Asynchronous Events (interrupts, exceptions, INIT, SIPI, SMI, VM exit¹, #MC), XBEGIN, XEND, XABORT, XACQUIRE, XRELEASE, (EENTRY, EEXIT, ERESUME, EEE, AEX)², INT 0, INT 3, INT n, a WRMSR that disables packet generation.

**Description**
Provides the source address for asynchronous events, and some other instructions. Is never sent alone, always sent with an associated TIP or MODE packet, and potentially others.

**Application**
FUP packets provide the IP to which they bind. However, they are never standalone, but are coupled with other packets.
In TSX cases, the FUP is immediately preceded by a MODE.TSX, which binds to the same IP. A TIP will follow only in the case of TSX aborts, see Section 36.4.2.8 for details.
Otherwise, FUPs are part of compound packet events (see Section 36.4.1). In these compound cases, the FUP provides the source IP for an instruction or event, while a following TIP (or TIP.PGD) uop will provide any destination IP. Other packets may be included in the compound event between the FUP and TIP.

**NOTES:**
1. If IA32_VMX_MISC[bit 14] reports 1.
2. If Intel Software Guard Extensions is supported.
FUP IP Payload

Flow Update Packet gives the source address of an instruction when it is needed. In general, branch instructions do not need a FUP, because the source address is clear from the disassembly. For asynchronous events, however, the source address cannot be inferred from the source, and hence a FUP will be sent. Table 36-25 illustrates cases where FUPs are sent, and which IP can be expected in those cases.

### Table 36-25. FUP Cases and IP Payload

<table>
<thead>
<tr>
<th>Event</th>
<th>Flow Update IP</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>External Interrupt, NMI/SMI, Traps, Machine Check (trap-like), INIT/SIP</td>
<td>Address of next instruction (Next IP) that would have been executed</td>
<td>Functionally, this matches the LBR FROM field value and also the EIP value which is saved onto the stack.</td>
</tr>
<tr>
<td>Exceptions/Faults, Machine check (fault-like)</td>
<td>Address of the instruction which took the exception/fault (Current IP)</td>
<td>This matches the similar functionality of LBR FROM field value and also the EIP value which is saved onto the stack.</td>
</tr>
<tr>
<td>Software Interrupt</td>
<td>Address of the software interrupt instruction (Current IP)</td>
<td>This matches the similar functionality of LBR FROM field value, but does not match the EIP value which is saved onto the stack (Next Linear Instruction Pointer - NLIP).</td>
</tr>
<tr>
<td>EENTER, EEXIT, ERESUME, Enclave Exiting Event (EEE), AEX</td>
<td>Current IP of the instruction</td>
<td>This matches the LBR FROM field value and also the EIP value which is saved onto the stack.</td>
</tr>
<tr>
<td>XACQUIRE</td>
<td>Address of the X* instruction</td>
<td></td>
</tr>
<tr>
<td>XRELEASE, XBEGIN, XEND, XABORT, other transactional abort</td>
<td>Current IP</td>
<td></td>
</tr>
<tr>
<td>#SMI</td>
<td>IP that is saved into SMRAM</td>
<td></td>
</tr>
<tr>
<td>WRMSR that clears TraceEn</td>
<td>Current IP</td>
<td></td>
</tr>
</tbody>
</table>

### NOTES:

1. Information on EENTER, EEXIT, ERESUME, EEE, Asynchronous Enclave eXit (AEX) can be found in *Intel® Software Guard Extensions Programming Reference*. 

On a canonical fault due to sequentially fetching an instruction in non-canonical space (as opposed to jumping to non-canonical space), the IP of the fault (and thus the payload of the FUP) will be a non-canonical address. This is consistent with what is pushed on the stack for such faulting cases.

If there are post-commit task switch faults, the IP value of the FUP will be the original IP when the task switch started. This is the same value as would be seen in the LBR_FROM field. But it is a different value as is saved on the stack or VMCS.
### 36.4.2.7 Paging Information (PIP) Packet

#### Table 36-26. PIP Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Paging Information (PIP) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packet Format</strong></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>CR3[11:5] or 0</td>
</tr>
<tr>
<td>3</td>
<td>CR3[19:12]</td>
</tr>
<tr>
<td>4</td>
<td>CR3[27:20]</td>
</tr>
<tr>
<td>5</td>
<td>CR3[35:28]</td>
</tr>
<tr>
<td>6</td>
<td>CR3[43:36]</td>
</tr>
<tr>
<td>7</td>
<td>CR3[51:44]</td>
</tr>
<tr>
<td><strong>Dependencies</strong></td>
<td>TriggerEn &amp;&amp; ContextEn &amp;&amp; IA32_RTIT_CTL.OS</td>
</tr>
<tr>
<td><strong>Generation Scenario</strong></td>
<td>MOV CR3, Task switch, INIT, SIPI, PSB+; If IA32_VMX_MISC[bit 14] reports 1: VM exit, VM entry</td>
</tr>
</tbody>
</table>
| **Description**       | The CR3 payload shown includes only the address portion of the CR3 value. For PAE paging, CR3[11:5] are thus included. For other page modes (32-bit and IA-32e paging), these bits are 0. This packet holds the CR3 address value. It will be generated on operations that modify CR3:
- MOV CR3 operation
- Task Switch
- INIT and SIPI
- VM exit and VM entry, if VMCS-based controls are clear (see Section 36.5.1)
PIPs are not generated, despite changes to CR3, on SMI and RSM. This is due to the special behavior on these operations, see Section  for details. Note that, for some cases of task switch where CR3 is not modified, no PIP will be produced.
The purpose of the PIP is to indicate to the decoder which application is running, so that it can apply the proper binaries to the linear addresses that are being traced.
The PIP packet contains the new CR3 value when CR3 is written.
On processors that IA32_VMX_MISC[bit 14] reports 0, bit 0 of byte 2 is reserved, and no VM exits or VM entries will be seen in the trace since these processors do not allow TraceEn to be set post-VMXON.
On processors that IA32_VMX_MISC[bit 14] reports 1, PIPs that are generated in VMX non-root operation can be configured via the VMCS execution control to set the NR bit.
The NR bit is clear for PIPs generated in VMX root operation or if the VMCS execution control is configured to suppress VMX indications in Guest Traces.
| **Application**       | The purpose of the PIP packet is to help the decoder uniquely identify what software is running at any given time. When a PIP is encountered, a decoder should do the following:
1) If there was a prior unbound FUP (that is, a FUP not preceded by a packet such as MODE.TSX that consumes it, and it hence pairs with a TIP that has not yet been seen), then this PIP is part of a compound packet event (Section 36.4.1). Find the ending TIP and apply the new CR3/NR values to the TIP payload IP.
2) Otherwise, look for the next MOV CR3, far branch, or VMRESUME/VMLAUNCH in the disassembly, and apply the new CR3 to the next (or target) IP.
For examples of the packets generated by these flows, see Section 36.7. |
36.4.2.8 MODE Packets

MODE packets keep the decoder informed of various processor modes about which it needs to know in order to properly manage the packet output, or to properly disassemble the associated binaries. MODE packets include a header and a mode byte, as shown below.

The MODE Leaf ID indicates which set of mode bits are held in the lower bits.

**MODE.Exec Packet**

<table>
<thead>
<tr>
<th>Name</th>
<th>MODE.Exec Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td></td>
<td>0 1 0 0 1 1 0 0 1</td>
</tr>
<tr>
<td></td>
<td>1 0 0 0 0 0 0 CS.D (CS.L &amp; LMA)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>Far branch, interrupt, exception, (VM exit, VM entry,)[1] if the mode changes. PSB+, and any scenario that can generate a TIP.PGE, such that the mode may have changed since the last MODE.Exec.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PacketEn</td>
<td></td>
</tr>
<tr>
<td>Generation Scenario</td>
<td></td>
</tr>
</tbody>
</table>

| Description                   | Indicates whether software is in 16, 32, or 64-bit mode, by providing the CS.D and (CS.L & IA32_EFER.LMA) values. Essential for the decoder to properly disassemble the associated binary. |

<table>
<thead>
<tr>
<th>CS.D</th>
<th>(CS.L &amp; IA32_EFER.LMA)</th>
<th>Addressing Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 1</td>
<td>N/A</td>
<td></td>
</tr>
<tr>
<td>0 1</td>
<td>64-bit mode</td>
<td></td>
</tr>
<tr>
<td>1 0</td>
<td>32-bit mode</td>
<td></td>
</tr>
<tr>
<td>0 0</td>
<td>16-bit mode</td>
<td></td>
</tr>
</tbody>
</table>

MODE.Exec is sent at the time of a mode change, if PacketEn=1 at the time, or when tracing resumes, if necessary. In the former case, the MODE.Exec packet is generated along with other packets that result from the far transfer operation that changes the mode. In cases where the mode changes while PacketEn=0, the processor will send out a MODE.Exec along with the TIP.PGE when tracing resumes. The processor may opt to suppress the MODE.Exec when tracing resumes if the mode matches that from the last MODE.Exec packet, if there was no PSB in between.

| Application                   | MODE.Exec always immediately precedes a TIP or TIP.PGE. The mode change applies to the IP address in the payload of the next TIP or TIP.PGE. |

**NOTES:**
1. If IA32_VMX_MISC[bit 14] reports 1.
Table 36-29. MODE.TSX Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>MODE.TSX Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td><img src="image" alt="Binary Format" /></td>
</tr>
<tr>
<td>Dependencies</td>
<td>TriggerEn and ContextEn</td>
</tr>
<tr>
<td>Description</td>
<td>Indicates when a TSX transaction (either HLE or RTM) begins, commits, or aborts. Instructions executed transactionally will be “rolled back” if the transaction is aborted.</td>
</tr>
<tr>
<td>TXAbort</td>
<td>0</td>
</tr>
<tr>
<td>InTX</td>
<td>0</td>
</tr>
<tr>
<td>Implication</td>
<td>11</td>
</tr>
<tr>
<td>Application</td>
<td>If PacketEn=1, MODE.TSX always immediately precedes a FUP. If the TXAbort bit is zero, then the mode change applies to the IP address in the payload of the FUP. If TXAbort=1, then the FUP will be followed by a TIP, and the mode change will apply to the IP address in the payload of the TIP. MODE.TSX packets may be generated when PacketEn=0, due to FilterEn=0. In this case, only the last MODE.TSX generated before TIP.PGE need be applied.</td>
</tr>
</tbody>
</table>
36.4.2.9 TraceStop Packet

Table 36-30. TraceStop Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>TraceStop Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Dependencies</td>
<td>TriggerEn &amp;&amp; ContextEn</td>
</tr>
<tr>
<td>Generation Scenario</td>
<td>Taken branch with target in TraceStop IP region, MOV CR3 in TraceStop IP region, or WRMSR that sets TraceEn in TraceStop IP region.</td>
</tr>
<tr>
<td>Description</td>
<td>Indicates when software has entered a user-configured TraceStop region. When the IP matches a TraceStop range while ContextEn and TriggerEn are set, a TraceStop action occurs. This disables tracing by setting IA32_RTIT_STATUS.Stopped, thereby clearing TriggerEn, and causes a TraceStop packet to be generated. The TraceStop action also forces FilterEn to 0. Note that TraceStop may not force a flush of internally buffered packets, and thus trace packet generation should still be manually disabled by clearing IA32_RTIT_CTL.TraceEn before examining output. See Section 36.2.2.3 for more details.</td>
</tr>
<tr>
<td>Application</td>
<td>If TraceStop follows a TIP.PGD (before the next TIP.PGE), then it was triggered either by the instruction that cleared PacketEn, or it was triggered by some later instruction that executed while FilterEn=0. In either case, the TraceStop can be applied at the IP of the TIP.PGD (if any). If TraceStop follows a TIP.PGE (before the next TIP.PGD), it should be applied at the last known IP.</td>
</tr>
</tbody>
</table>

36.4.2.10 Core:Bus Ratio (CBR) Packet

Table 36-31. CBR Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Core:Bus Ratio (CBR) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Dependencies</td>
<td>TriggerEn</td>
</tr>
<tr>
<td>Generation Scenario</td>
<td>After any frequency change, on C-state wake up, PSB+, and after enabling trace packet generation.</td>
</tr>
<tr>
<td>Description</td>
<td>Indicates the corebus ratio of the processor core. Useful for correlating wall-clock time and cycle time.</td>
</tr>
<tr>
<td>Application</td>
<td>All packets following the CBR represent instructions that executed with the new corebus ratio, while all preceding packets (aside from timing packets) represent instructions that executed with the prior ratio. There is not a precise IP provided, to which to bind the CBR packet.</td>
</tr>
</tbody>
</table>
### 36.4.2.11 Timestamp Counter (TSC) Packet

Table 36-32. TSC Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Timestamp Counter (TSC) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td><img src="image" alt="Packet Format" /></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>Sw TSC[7:0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Sw TSC[15:8]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Sw TSC[23:16]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Sw TSC[31:24]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Sw TSC[39:32]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Sw TSC[47:40]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Sw TSC[55:48]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Dependencies

IA32_RTIT_CTL.TSCEn && TriggerEn

### Generation Scenario

Sent after any event that causes the processor clocks or Intel PT timing packets (such as MTC or CYC) to stop. This may include P-state changes, wake from C-state, or clock modulation. Also on transition of TraceEn from 0 to 1.

### Description

When enabled by software, a TSC packet provides the lower 7 bytes of the current TSC value, as returned by the RDTSC instruction. This may be useful for tracking wall-clock time, and synchronizing the packets in the log with other timestamped logs.

### Application

TSC packet provides a wall-clock proxy of the event which generated it (packet generation enable, sleep state wake, etc). In all cases, TSC does not precisely indicate the time of any control flow packets; however, all preceding packets represent instructions that executed before the indicated TSC time, and all subsequent packets represent instructions that executed after it. There is not a precise IP to which to bind the TSC packet.
### 36.4.2.12 Mini Time Counter (MTC) Packet

#### Table 36-33. MTC Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Mini time Counter (MTC) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td><img src="image" alt="Packet Format" /></td>
</tr>
<tr>
<td>Dependencies</td>
<td>IA32_RTIT_CTL.MTCEn &amp; TriggerEn</td>
</tr>
<tr>
<td>Generation Scenario</td>
<td>Periodic, based on the core crystal clock, or Always Running Timer (ART).</td>
</tr>
<tr>
<td>Description</td>
<td>When enabled by software, an MTC packet provides a periodic indication of wall-clock time. The 8-bit CTC (Common Timestamp Copy) payload value is set to ((\text{ART} &gt;&gt; N) &amp; 0xFF). The frequency of the ART is related to the Maximum Non-Turbo frequency, and the ratio can be determined from CPUID leaf 15H, as described in Section 36.8.3. Software can select the threshold (N), which determines the MTC frequency by setting the IA32_RTIT_CTL.MTCFreq field (see Section 36.2.5.2) to a supported value using the lookup enumerated by CPUID (see Section 36.3.1). See Section 36.8.3 for details on how to use the MTC payload to track TSC time. MTC provides 8 bits from the ART, starting with the bit selected by MTCFreq to dictate the frequency of the packet. Whenever that 8-bit range being watched changes, an MTC packet will be sent out with the new value of that 8-bit range. This allows the decoder to keep track of how much wall-clock time has elapsed since the last TSC packet was sent, by keeping track of how many MTC packets were sent and what their value was. The decoder can infer the truncated bits, CTC([N+7:N]), are 0 at the time of the MTC packet. There are cases in which MTC packet can be dropped, due to overflow or other micro-architectural conditions. The decoder should be able to recover from such cases by checking the 8-bit payload of the next MTC packet, to determine how many MTC packets were dropped. It is not expected that &gt;256 consecutive MTC packets should ever be dropped.</td>
</tr>
<tr>
<td>Application</td>
<td>MTC does not precisely indicate the time of any other packet, nor does it bind to any IP. However, all preceding packets represent instructions or events that executed before the indicated ART time, and all subsequent packets represent instructions that executed after, or at the same time as, the ART time.</td>
</tr>
</tbody>
</table>

---

7 6 5 4 3 2 1 0
0 0 1 0 1 1 0 0 1
1 CTC\([N+7:N]\)
## 36.4.2.13 TSC/MTC Alignment (TMA) Packet

**Table 36-34. TMA Packet Definition**

<table>
<thead>
<tr>
<th>Name</th>
<th>TSC/MTC Alignment (TMA) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>CTC[7:0]</td>
</tr>
<tr>
<td>3</td>
<td>CTC[15:8]</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>FastCounter[7:0]</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

| Dependencies | IA32_RTIT_CTL.MTCEn && IA32_RTIT_CTL.TSCEn && TriggerEn |
| Generation Scenario | Sent with any TSC packet. |

**Description**
The TMA packet serves to provide the information needed to allow the decoder to correlate MTC packets with TSC packets. With this packet, when a MTC packet is encountered, the decoder can determine how many timestamp counter ticks have passed since the last TSC or MTC packet. See Section 36.8.3.2 for details on how to make this calculation.

**Application**
TMA is always sent immediately following a TSC packet, and the payload values are consistent with the TSC payload value. Thus the application of TMA matches that of TSC.
36.4.2.14 Cycle Count Packet (CYC) Packet

Table 36-35. Cycle Count Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Cycle Count (CYC) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td>0</td>
<td>Cycle Counter[4:0]</td>
</tr>
<tr>
<td>2</td>
<td>Cycle Counter[18:12]</td>
</tr>
<tr>
<td>...</td>
<td>... (if Exp = 1 in the previous byte)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>IA32_RTIT_CTL.CYCEn &amp;&amp; TriggerEn</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generation Scenario</td>
<td>Can be sent at any time, though a maximum of one CYC packet is sent per core clock cycle. See Section 36.3.6 for CYC-eligible packets.</td>
</tr>
</tbody>
</table>

Description
The Cycle Counter field increments at the same rate as the processor core clock ticks, but with a variable length format (using a trailing EXP bit field) and a range-capped byte length.
If the CYC value is less than 32, a 1-byte CYC will be generated, with Exp=0. If the CYC value is between 32 and 4095 inclusive, a 2-byte CYC will be generated, with byte 0 Exp=1 and byte 1 Exp=0. And so on.
CYC provides the number of core clocks that have passed since the last CYC packet. CYC can be configured to be sent in every cycle in which an eligible packet is generated, or software can opt to use a threshold to limit the number of CYC packets, at the expense of some precision. These settings are configured using the IA32_RTIT_CTL.CycThresh field (see Section 36.2.5.2). For details on Cycle-Accurate Mode, IPC calculation, etc, see Section 36.3.6.
When CycThresh=0, and hence no threshold is in use, then a CYC packet will be generated in any cycle in which any CYC-eligible packet is generated. The CYC packet will precede the other packets generated in the cycle, and provides the precise cycle time of the packets that follow.
In addition to these CYC packets generated with other packets, CYC packets can be sent stand-alone. These packets serve simply to update the decoder with the number of cycles passed, and are used to ensure that a wrap of the processor’s internal cycle counter doesn’t cause cycle information to be lost. These stand-alone CYC packets do not indicate the cycle time of any other packet or operation, and will be followed by another CYC packet before any other CYC-eligible packet is seen.
When CycThresh>0, CYC packets are generated only after a minimum number of cycles have passed since the last CYC packet. Once this threshold has passed, the behavior above resumes, where CYC will either be sent in the next cycle that produces other CYC-eligible packets, or could be sent stand-alone.
When using CYC thresholds, only the cycle time of the operation (instruction or event) that generates the CYC packet is truly known. Other operations simply have their execution time bounded: they completed at or after the last CYC time, and before the next CYC time.

Application
CYC provides the offset cycle time (since the last CYC packet) for the CYC-eligible packet that follows. If another CYC is encountered before the next CYC-eligible packet, the cycle values should be accumulated and applied to the next CYC-eligible packet.
If a CYC packet is generated by a TNT, note that the cycle time provided by the CYC packet applies to the first branch in the TNT packet.
### 36.4.2.15 VMCS Packet

<table>
<thead>
<tr>
<th>Name</th>
<th>VMCS Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>VMCS Base Address [19:12]</td>
</tr>
<tr>
<td>3</td>
<td>VMCS Base Address [27:20]</td>
</tr>
<tr>
<td>4</td>
<td>VMCS Base Address [35:28]</td>
</tr>
<tr>
<td>5</td>
<td>VMCS Base Address [43:36]</td>
</tr>
<tr>
<td>6</td>
<td>VMCS Base Address [51:44]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>TriggerEn &amp;&amp; ContextEn; Also post-VMXON</th>
</tr>
</thead>
<tbody>
<tr>
<td>Generation Scenario</td>
<td>Generated on successful VMPTRLD, and optionally on SMM VM exit and VM entries that return from SMM (see Section 36.5).</td>
</tr>
</tbody>
</table>

### Description
The VMCS packet provides an address related to a VMCS pointer for a decoder to determine the transition of code contexts:

- On a successful VMPTRLD (i.e., a VMPTRLD that doesn’t fault, fail, or VM exit), the VMCS packet contains the address of the current working VMCS pointer of the logical processor that will execute a VM guest context.
- On SMM VM exits, the VMCS packet provides the STM VMCS base address (SMM Transfer VMCS pointer), if VMCS-based controls are clear (see Section 36.5.1). See Section 36.6 on tracing inside and outside STM.
- On VM entries that return from SMM, the VMCS packet provides the current working VMCS pointer of the guest VM (see Section 36.6), if VMCS-based controls are clear (see Section 36.5.1). Root versus Non-Root operation can be distinguished from the PIP.NR bit.

If a VMCS packet is generated before a VMCS has been loaded, or after it has been cleared, the base address value will be all 1s.

VMCS packets will not be seen on processors with IA32_VMX_MISC[bit 14]=0, as these processors do not allow TraceEn to be set post-VMXON.

### Application
The purpose of the VMCS packet is to help the decoder uniquely identify changes in the executing software context in situations that CR3 may not be unique.

When a VMCS is encountered, a decoder should do the following:

- If there was a prior unbound FUP (that is, a FUP not preceded by a packet such as MODE.TSX that consumes it, and it hence pairs with a TIP that has not yet been seen), then this VMCS is part of a compound packet event (Section 36.4.1). Find the ending TIP and apply the new VMCS base pointer value to the TIP payload IP.
- Otherwise, look for the next VMPTRLD, VMRESUME, or VMLAUNCH in the disassembly, and apply the new VMCS base pointer on the next VM entry.

For examples of the packets generated by these flows, see Section 36.7.
**36.4.2.16 Overflow (OVF) Packet**

Table 36-37. OVF Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Overflow (OVF) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packet Format</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>1 1 1 1 1 0 1 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>TriggerEn</th>
<th>Generation Scenario</th>
<th>On resolution of internal buffer overflow</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>OVF simply indicates to the decoder that an internal buffer overflow occurred, and packets were likely lost. If BranchEN= 1, OVF is followed by a FUP or TIP.PGE which will provide the IP at which packet generation resumes. See Section 36.3.8.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application</td>
<td>When an OVF packet is encountered, the decoder should skip to the IP given in the subsequent FUP or TIP.PGE. The cycle counter for the CYC packet will be reset at the time the OVF packet is sent. Software should reset its call stack depth on overflow, since no RET compression is allowed across an overflow. Similarly, any IP compression that follows the OVF is guaranteed to use as a reference LastIP the IP payload of an IP packet that preceded the overflow.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**36.4.2.17 Packet Stream Boundary (PSB) Packet**

Table 36-38. PSB Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Packet Stream Boundary (PSB) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Packet Format</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td></td>
<td>0 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>1 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>2 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>3 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>4 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>5 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>6 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>7 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>8 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>9 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>10 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>11 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>12 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>13 1 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>14 0 0 0 0 1 0</td>
</tr>
<tr>
<td></td>
<td>15 1 0 0 0 1 0</td>
</tr>
</tbody>
</table>
36.4.2.18 PSBEND Packet

<table>
<thead>
<tr>
<th>Name</th>
<th>PSBEND Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
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<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Dependencies | TriggerEn | Generation Scenario | Always follows PSB packet, separated by PSB+ packets
Description | PSBEND is simply a terminator for the series of “status only” (PSB+) packets that follow PSB (Section 36.3.7).
Application | When a PSBEND packet is seen, the decoder should cease to treat packets as “status only”.

Table 36-38. PSB Packet Definition

| Dependencies | TriggerEn | Generation Scenario | Periodic, based on the number of output bytes generated while tracing. PSB is sent when IA32_RTIT_STATUS.PacketByteCnt=0, and each time it crosses the software selected threshold after that. May be sent for other micro-architectural conditions as well. |
|--------------|-----------|----------------------|
| Description  | PSB is a unique pattern in the packet output log, and hence serves as a sync point for the decoder. It is a pattern that the decoder can search for in order to get aligned on packet boundaries. This packet is periodic, based on the number of output bytes, as indicated by IA32_RTIT_STATUS.PacketByteCnt. The period is chosen by software, via IA32_RTIT_CTL.PSBFreq (see Section 36.2.5.2). Note, however, that the PSB period is not precise, it simply reflects the average number of output bytes that should pass between PSBs. The processor will make a best effort to insert PSB as quickly after the selected threshold is reached as possible. The processor also may send extra PSB packets for some micro-architectural conditions. PSB also serves as the leading packet for a set of “status-only” packets collectively known as PSB+ (Section 36.3.7). |
| Application  | When a PSB is seen, the decoder should interpret all following packets as “status only”, until either a PSBEND or OVF packet is encountered. “Status only” implies that the binding and ordering rules to which these packets normally adhere are ignored, and the state they carry can instead be applied to the IP payload in the FUP packet that is included. |
36.4.2.19 Maintenance (MNT) Packet

Table 36-40. MNT Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>Maintenance (MNT) Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
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<tr>
<td></td>
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<td>1</td>
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<td>9</td>
</tr>
<tr>
<td></td>
<td>10</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>TriggerEn</th>
<th>Generation Scenario</th>
<th>Implementation specific</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>This packet is generated by hardware, the payload meaning is model-specific.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application</td>
<td>Unless a decoder has been extended for a particular family/model/stepping to interpret MNT packet payloads, this packet should simply be ignored. It does not bind to any IP.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

36.4.2.20 PAD Packet

Table 36-41. PAD Packet Definition

<table>
<thead>
<tr>
<th>Name</th>
<th>PAD Packet</th>
</tr>
</thead>
<tbody>
<tr>
<td>Packet Format</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
<tr>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Dependencies</th>
<th>TriggerEn</th>
<th>Generation Scenario</th>
<th>Implementation specific</th>
</tr>
</thead>
<tbody>
<tr>
<td>Description</td>
<td>PAD is simply a NOP packet. Processor implementations may choose to add pad packets to improve packet alignment or for implementation-specific reasons.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application</td>
<td>Ignore PAD packets.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

36.5 TRACING POST-VMXON

On processors that IA32_VMX_MISC[bit 14] reports 1, TraceEn can be set post-VMXON. A series of mechanisms exist to allow the VMM to configure tracing based on the desired trace domain, and on the consumer of the trace output. The VMM can configure specific VM execution controls in the VMCS to control what virtualization-specific data are included within the trace packets (see Section 36.5.1 for details). MSR save and load lists can be employed by the VMM to restrict tracing to the desired context (see Section 36.5.2 for details). These configuration options
are summarized in Table 36-42. Table 36-42 covers common Intel PT usages while SMIs are handled by the default SMM treatment. Tracing with SMM Transfer Monitor is described in Section 36.6.

### Table 36-42. Common Usages of Intel PT and VMX

<table>
<thead>
<tr>
<th>Target Domain</th>
<th>Output Consumer</th>
<th>Virtualize Output</th>
<th>Configure VMCS Controls</th>
<th>TraceEN Configuration</th>
<th>Save/Restore MSR states of Trace Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>System-Wide (VMM + VMs)</td>
<td>Host</td>
<td>NA</td>
<td>Default Setting (no suppression)</td>
<td>WRMSR or XRSTORS by Host</td>
<td>NA</td>
</tr>
<tr>
<td>VMM Only</td>
<td>Intel PT Aware VMM</td>
<td>NA</td>
<td>Enable suppression</td>
<td>MSR load list to disable tracing in VM, enable tracing on VM exits</td>
<td>NA</td>
</tr>
<tr>
<td>VM Only</td>
<td>Intel PT Aware VMM</td>
<td>NA</td>
<td>Enable suppression</td>
<td>MSR load list to enable tracing in VM, disable tracing on VM exits</td>
<td>NA</td>
</tr>
<tr>
<td>Intel PT Aware Guest(s)</td>
<td>Per Guest</td>
<td>VMM adds trace output virtualization</td>
<td>Enable suppression</td>
<td>MSR load list to enable tracing in VM, disable tracing on VM exits</td>
<td>VMM Update guest state on XRSTORS-exiting VM exits</td>
</tr>
</tbody>
</table>

#### 36.5.1 VMX-Specific Packets and VMCS Controls

In all of the usages of VMX and Intel PT, the decoder in the host or VMM context can identify the occurrences of VMX transitions with the aid of VMX-specific packets. Packets relevant to VMX fall into the follow two kinds:

- **VMCS Packet**: The VMX transitions of individual VM can be distinguished by a decoder using the base address field in a VMCS packet. The base address field stores the VMCS pointer address of a successful VMPTRLD. A VMCS packet is sent on a successful execution of VMPTRLD. See Section 36.4.2.15 for details.

- **NonRoot (NR) bit field in PIP packet**: PIP packets are generated with each VM entry/exit. The NR bit in a PIP packet is set when in VMX non-Root operation. Thus a transition of the NR bit from 0 to 1 indicates the occurrence of a VM entry, and a transition of 1 to 0 indicates the occurrence of a VM exit.

Processors with IA32_VMX_MISC[bit 14] = 1 also provides VMCS controls that a VMM can configure to prevent VMX-specific information from leaking across virtualization boundaries.

### Table 36-43. VMCS Controls For Intel Processor Trace

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Bit Position</th>
<th>Value</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>Suppress VMX Indications in Guest Traces</td>
<td>Secondary Processor-Based Execution Control</td>
<td>19</td>
<td>0</td>
<td>PIPs generated in non-Root operation will set the PIP.NR bit. PSB+ in non-Root operation will include the VMCS packet, to ensure that the decoder knows which Guest is currently in use.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>PIPs generated in non-Root operation will not set the PIP.NR bit. PSB+ in non-Root operation will not include the VMCS packet.</td>
</tr>
<tr>
<td>Suppress VMX packets on Exit</td>
<td>VM-exit Control</td>
<td>24</td>
<td>0</td>
<td>PIPs are generated on VM exit, with NonRoot=0. On VM exit to SMM, VMCS packets are additionally generated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>No PIP is generated on VM exit, and no VMCS packet is generated on VM exit to SMM.</td>
</tr>
<tr>
<td>Suppress VMX packets on Entry</td>
<td>VM-entry Control</td>
<td>17</td>
<td>0</td>
<td>PIPs are generated on VM entry, with NonRoot=1 if the destination of the entry is non-Root operation. On VM entry to SMM, VMCS packets are additionally generated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>No PIP is generated on VM entry, and no VMCS packet is generated on VM entry to SMM.</td>
</tr>
</tbody>
</table>

The default setting for the VMCS controls that interacts with Intel PT is to enable all VMX-specific packet information. The scenarios that would use the default setting also do not require the VMM to use MSR load list to manage the configuration of turning-on/off of trace packet generation across VM exits.
If IA32_VMX_MISC[bit 14] reports 0, any attempt to set the VMCS control bits in Table 36-43 will result in a failure on guest entry.

### 36.5.2 Managing Trace Packet Generation Across VMX Transitions

In tracing scenarios that collect packets for both VMX root and non-root operations, a host executive can manage the MSRs associated with trace packet generation directly. The states of these MSRs need not be modified using MSR load list or MSR save list across VMX transitions.

For tracing scenarios that collect only packets within either VMX root or non-root operations, the VMM can use the MSR load list and/or MSR save list to toggle IA32_RTIT_CTL.TraceEn.

#### 36.5.2.1 System-Wide Tracing

When a host or VMM configures Intel PT to collect trace packets of the entire system, it can leave the VMCS controls in its default setting to allow VMX-specific packets to provide information across VMX transitions. MSR load list is not used across VM exits or VM entries, nor is VM-exit MSR save list.

The decoder will desire to identify the occurrence of VMX transitions. The packets of interests to a decoder are shown in Table 36-44.

<table>
<thead>
<tr>
<th>Event</th>
<th>Packets</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM exit</td>
<td>FUP(GuestIP)</td>
<td>The FUP indicates at which point in the Guest flow the VM exit occurred. This is important, since VM exit can be an asynchronous event. The IP will match that written into the VMCS.</td>
</tr>
<tr>
<td></td>
<td>PIP(HostCR3, NR=0)</td>
<td>The PIP packet provides the new Host CR3 value, as well as indication that the logical processor is entering VMX Root operation. This allows the decoder to identify the change of executing context from guest to host and load the appropriate set of binaries to continue decode.</td>
</tr>
<tr>
<td></td>
<td>TIP(HostIP)</td>
<td>The TIP indicates the destination IP, the IP of the first instruction to be executed in VMX Root operation. Note, this packet could be preceded by a MODE.Exec packet (Section 36.4.2.8). This is generated only in cases where CS.D or (CS.L &amp; EFER.LMA) change during the transition.</td>
</tr>
<tr>
<td>VM entry</td>
<td>PIP(GuestCR3, NR=1)</td>
<td>The PIP packet provides the new Guest CR3 value, as well as indication that the logical processor is entering VMX non-Root operation. This allows the decoder to identify the change of executing context from host to guest and load the appropriate set of binaries to continue decode.</td>
</tr>
<tr>
<td></td>
<td>TIP(GuestIP)</td>
<td>The TIP indicates the destination IP, the IP of the first instruction to be executed in VMX no-Root operation. This should match the IP value read out from the VMCS. Note, this packet could be preceded by a MODE.Exec packet (Section 36.4.2.8). This is generated only in cases where CS.D or (CS.L &amp; EFER.LMA) change during the transition.</td>
</tr>
</tbody>
</table>

Since the packet suppression controls are cleared, the VMCS packet will be included in all PSB+ for this usage scenario. Thus the decoder can distinguish the execution context of different VMs. Additionally, it will be generated on VMPTRLD. Thus the decoder can distinguish the execution context of different VMs.

When the host VMM configures a system to collect trace packets in this scenario, it should emulate CPUID to report CPUID.(EAX=07H, ECX=0):EBX[bit 26] with 0 to guests, indicating to guests that Intel PT is not available.

### VMX TSC Manipulation

The TSC packets generated while in VMX non-Root operation will include any changes resulting from the use of a VMM’s use of the TSC offsetting or TSC scaling VMCS control (see Chapter 25, “VMX Non-Root Operation”). In this system-wide usage model, the decoder may need to account for the effect of per-VM adjustments in the TSC packets generated in non-Root operation and the absence of TSC adjustments in TSC packets generated in Root operation. The VMM can supply this information to the decoder.
36.5.2.2 Host-Only Tracing

When trace packets in VMX non-root operation are not desired, the VMM can use VM-entry MSR load list with IA32_RTIT_CTL.TraceEn=0 to disable trace packet generation in guests, set IA32_RTIT_CTL.TraceEn=1 via VM-exit MSR load list.

When tracing only the Host, the decoder does not need information about the guests, the VMCS controls for suppressing VMX-specific packets can be set to reduce the packets generated. VMCS packets will still be generated on successful VMPTRLD and in PSB+ generated in the Host, but these will be unused by the decoder.

The packets of interests to a decoder when trace packets are collected for host-only tracing are shown in Table 36-45.

Table 36-45. Packets on VMX Transitions (Host-Only Tracing)

<table>
<thead>
<tr>
<th>Event</th>
<th>Packets</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM exit</td>
<td>TIP.PGE(HostIP)</td>
<td>The TIP.PGE indicates that trace packet generation is enabled and gives the IP of the first instruction to be executed in VMX Root operation. Note, this packet could be preceded by a MODE.Exec packet (Section 36.4.2.8). This is generated only in cases where CS.D or (CS.L &amp; EFER.LMA) change during the transition.</td>
</tr>
<tr>
<td>VM entry</td>
<td>TIP.GD()</td>
<td>The TIP indicates that trace packet generation was disabled. This ensure that all buffered packets are flushed out.</td>
</tr>
</tbody>
</table>

36.5.2.3 Guest-Only Tracing

A VMM can configure trace packet generation while in non-root operation for guests executing normally. This is accomplished by utilizing the MSR load lists across VM exit and VM entry to confine trace packet generation to stay within the guest environment.

For this usage, the VM-entry MSR load list is programmed to turn on trace packet generation. The VM-exit MSR load list is used to clear TraceEn=0 to disable trace packet generation in the host. Further, if it is preferred that the Guest packet stream contain no indication of non-Root execution, the VMM should set 1 to the VMCS controls described in Table 36-43.

36.5.2.4 Virtualization of Guest Output Packet Streams

Each Intel PT aware guest OS can produce one or more output packet streams to destination addresses specified as guest physical address (GPA) using context-switched IA32_RTIT_OUTPUT_BASE within the guest. The processor generates trace packets to the platform physical address specified in IA32_RTIT_OUTPUT_BASE, and those specified in the ToPA tables. Thus, a VMM that supports Intel PT aware guest OS may wish to virtualize the output configurations of IA32_RTIT_OUTPUT_BASE and ToPA for each trace configuration state of all the guests.

36.5.2.5 Emulation of Intel PT Traced State

If a VMM emulates an element of processor state by taking a VM exit on reads and/or writes to that piece of state, and the state element impacts Intel PT packet generation or values, it may be incumbent upon the VMM to insert or modify the output trace data.

If a VM exit is taken on a guest write to CR3 (including ”MOV CR3” as well as task switches), the PIP packet normally generated on the CR3 write will be missing.

To avoid decoder confusion when the guest trace is decoded, the VMM should emulate the missing PIP by writing it into the guest output buffer. If the guest CR3 value is manipulated, the VMM may also need to manipulate the IA32_RTIT_CR3_MATCH value, in order to ensure the trace behavior matches the guest's expectation.

Similarly, if a VMM emulates the TSC value by taking a VM exit on RDTSC, the TSC packets generated in the trace may mismatch the TSC values returned by the VMM on RDTSC. To ensure that the trace can be properly aligned with software logs based on RDTSC, the VMM should either make corresponding modifications to the TSC packet values in the guest trace, or use mechanisms such as TSC offsetting or TSC scaling in place of exiting.
36.5.2.6 TSC Scaling

When TSC scaling is enabled for a guest using Intel PT, the VMM should ensure that the value of Maximum Non-Turbo Ratio[15:8] in MSR_PLATFORM_INFO (MSR 0CEH) and the TSC/“core crystal clock” ratio (EBX/EAX) in CPUID leaf 15H are set in a manner consistent with the resulting TSC rate that will be visible to the VM. This will allow the decoder to properly apply TSC packets, MTC packets (based on the core crystal clock or ART, whose frequency is indicated by CPUID leaf 15H), and CBR packets (which indicate the ratio of the processor frequency to the Max Non-Turbo frequency). Absent this, or separate indication of the scaling factor, the decoder will be unable to properly track time in the trace. See Section 36.8.3 for details on tracking time within an Intel PT trace.

36.5.2.7 Failed VM Entry

The packets generated by a failed VM-entry depend both on the VMCS configuration, as well as on the type of failure. The results to expect are summarized in the table below. Note that packets in italics may or may not be generated, depending on implementation choice, and the point of failure.

<table>
<thead>
<tr>
<th>Usage Model</th>
<th>Entry Configuration</th>
<th>Early Failure (fall through to Next IP)</th>
<th>Late Failure (VM exit)</th>
</tr>
</thead>
<tbody>
<tr>
<td>System-Wide</td>
<td>No MSR load list</td>
<td>TIP (NextIP)</td>
<td>Pip(Guest CR3, NR=1), TraceEn 0-&gt;1 Packets (See Section 36.2.5.3), Pip(HostCR3, NR=0), TIP(HostIP)</td>
</tr>
<tr>
<td>VMM Only</td>
<td>MSR load list</td>
<td>TIP (NextIP)</td>
<td>TraceEn 0-&gt;1 Packets (See Section 36.2.5.3), TIP(HostIP)</td>
</tr>
<tr>
<td>VM Only</td>
<td>MSR load list</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

36.5.2.8 VMX Abort

VMX Abort conditions take the processor into a shutdown state. On a VM exit that leads to VMX abort, some packets (FUP, PIP) may be generated, but any expected TIP, TIP.PGE, or TIP.PGD may be dropped.

36.6 TRACING AND SMM TRANSFER MONITOR (STM)

SMM Transfer Monitor is a VMM that operates inside SMM while in VMX root operation. An STM operates in conjunction with an executive monitor. The latter operates outside SMM and in VMX root operation. Transitions from the executive monitor or its VMMs to the STM are called SMM VM exits. The STM returns from SMM via a VM entry to the VM in non-root operation or the executive monitor in VMX root operation.

Intel PT supports tracing in STM similar to tracing support for post-VMXON as described above in Section 36.7. As a result, on a SMM VM exit resulting from #SMI, TraceEn is not saved and then cleared. Software can save the state of the trace configuration MSRs and clear TraceEN using the MSR load/save lists.

36.7 PACKET GENERATION SCENARIOS

Table 36-47 illustrates the packets generated in various scenarios. In the heading row, PacketEn is abbreviated as PktEn, ContextEn as CntxEn. Note that this assumes that TraceEn=1 in IA32_RTIT_CTL, while TriggerEn=1 and Error=0 in IA32_RTIT_STATUS, unless otherwise specified. Entries that do not matter in packet generation are marked “D.C.”

<table>
<thead>
<tr>
<th>Case</th>
<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>1a</td>
<td>Normal non-jump operation</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td></td>
<td>None</td>
</tr>
<tr>
<td>1b</td>
<td>Normal non-jump operation</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td>None</td>
</tr>
</tbody>
</table>
## Table 36-47. Packet Generation under Different Enable Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>2a</td>
<td>WRMSR/XRSTORS/RSM that changes TraceEn 0 -&gt; 1, with PacketByteCnt &gt;0</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>*TSC if TSCEn=1; TMA if TSCEn=MTCEn=1</td>
<td>TSC?, TMA?, CBR</td>
</tr>
<tr>
<td>2b</td>
<td>WRMSR/XRSTORS/RSM that changes TraceEn 0 -&gt; 1, with PacketByteCnt =0</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>*TSC if TSCEn=1; TMA if TSCEn=MTCEn=1</td>
<td>PSB, PSBEND (see Section 36.4.2.17)</td>
</tr>
<tr>
<td>2d</td>
<td>WRMSR/XRSTORS/RSM that changes TraceEn 0 -&gt; 1, with PacketByteCnt &gt;0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>TSC if TSCEn=1; TMA if TSCEn=MTCEn=1</td>
<td>TSC?, TMA?, CBR, MODE.Exec, TIP,PGE(NLIP)</td>
</tr>
<tr>
<td>2e</td>
<td>WRMSR/XRSTORS/RSM that changes TraceEn 0 -&gt; 1, with PacketByteCnt =0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>MODE.Exec, TIP,PGE(NLIP), PSB, PSBEND (see Section 36.4.2.8, 36.4.2.7, 36.4.2.13, 36.4.2.15, 36.4.2.17)</td>
<td></td>
</tr>
<tr>
<td>3a</td>
<td>WRMSR that changes TraceEn 1 -&gt; 0</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>3b</td>
<td>WRMSR that changes TraceEn 1 -&gt; 0</td>
<td>1</td>
<td>0</td>
<td>D.C.</td>
<td>FUP(CLIP), TIP,PGD()</td>
<td>None</td>
</tr>
<tr>
<td>5a</td>
<td>MOV to CR3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>TraceStop if executed in a TraceStop region</td>
<td>TIP(NewCR3,NR?), TraceStop?</td>
</tr>
<tr>
<td>5f</td>
<td>MOV to CR3</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>TraceStop if executed in a TraceStop region</td>
<td>TIP(NewCR3,NR?), TraceStop?</td>
</tr>
<tr>
<td>5b</td>
<td>MOV to CR3</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*PIP.NR=1 if not in root operation, and “Suppress VMX indications” execution control = 0</td>
<td>PIP(NewCR3, NR?), MODE.Exec?, TIP,PGE(NLIP)</td>
</tr>
<tr>
<td>5c</td>
<td>MOV to CR3</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>None</td>
<td>TIP,PGD()</td>
</tr>
<tr>
<td>5e</td>
<td>MOV to CR3</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*PIP.NR=1 if not in root operation, and “Suppress VMX indications” execution control = 0</td>
<td>PIP(NewCR3, NR?), MODE.Exec?, TIP,PGE(NLIP), TraceStop?</td>
</tr>
<tr>
<td>5d</td>
<td>MOV to CR3</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>*PIP.NR=1 if not in root operation, and “Suppress VMX indications” execution control = 0</td>
<td>PIP(NewCR3, NR?)</td>
</tr>
<tr>
<td>6a</td>
<td>Unconditional direct near jump</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>6b</td>
<td>Unconditional direct near jump</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>TraceStop if BLIP is in a TraceStop region</td>
<td>TIP,PGD(BLIP), TraceStop?</td>
</tr>
<tr>
<td>6c</td>
<td>Unconditional direct near jump</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
<td>MODE.Exec?, TIP,PGE(BLIP)</td>
</tr>
<tr>
<td>6d</td>
<td>Unconditional direct near jump</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>7a</td>
<td>Conditional taken jump or compressed RET that does not fill up the internal TNT buffer</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
### Table 36-47. Packet Generation under Different Enable Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>7b</td>
<td>Conditional taken jump or compressed RET</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
<td>MODE.Exec?, TIP.PGE(BLIP)</td>
</tr>
<tr>
<td>7e</td>
<td>Conditional taken jump or compressed RET, with empty TNT buffer</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>TraceStop if BLIP is in a TraceStop region</td>
<td>TIP.PGD(), TraceStop?</td>
</tr>
<tr>
<td>7f</td>
<td>Conditional taken jump or compressed RET, with non-empty TNT buffer</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>TraceStop if BLIP is in a TraceStop region</td>
<td>TNT, TIP.PGD(), TraceStop?</td>
</tr>
<tr>
<td>7d</td>
<td>Conditional taken jump or compressed RET that fills up the internal TNT buffer</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td>TNT</td>
</tr>
<tr>
<td>8a</td>
<td>Conditional non-taken jump</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td></td>
<td>None</td>
</tr>
<tr>
<td>8d</td>
<td>Conditional not-taken jump that fills up the internal TNT buffer</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td>TNT</td>
</tr>
<tr>
<td>9a</td>
<td>Near indirect jump (JMP, CALL, or uncompressed RET)</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td></td>
<td>None</td>
</tr>
<tr>
<td>9b</td>
<td>Near indirect jump (JMP, CALL, or uncompressed RET)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
<td>MODE.Exec?, TIP.PGE(BLIP)</td>
</tr>
<tr>
<td>9c</td>
<td>Near indirect jump (JMP, CALL, or uncompressed RET)</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>TraceStop if BLIP is in a TraceStop region</td>
<td>TIP.PGD(BLIP), TraceStop?</td>
</tr>
<tr>
<td>9d</td>
<td>Near indirect jump (JMP, CALL, or uncompressed RET)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td></td>
<td>TIP(BLIP)</td>
</tr>
<tr>
<td>10a</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>None</td>
</tr>
<tr>
<td>10f</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *TraceStop if BLIP is in a TraceStop region</td>
<td>PIP(new CR3, NR?), TraceStop?</td>
</tr>
<tr>
<td>10b</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
<td>PIP(new CR3, NR?), MODE.Exec?, TIP.PGE(BLIP)</td>
</tr>
<tr>
<td>10c</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>TIP.PGD()</td>
</tr>
</tbody>
</table>
### Table 36-47. Packet Generation under Different Enable Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>10d</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *TraceStop if BLIP is in a TraceStop region</td>
<td>PIP(new CR3, NR??), TIP.PGD(BLIP), TraceStop?</td>
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<tr>
<td>10e</td>
<td>Far Branch (CALL/JMP/RET)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *MODE.Exec if the operation changes CSL/D or IA32_EFER.LMA</td>
<td>PIP(new CR3, NR??), MODE.Exec?, TIP(BLIP)</td>
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<tr>
<td>11a</td>
<td>HW Interrupt</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>None</td>
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<tr>
<td>11f</td>
<td>HW Interrupt</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *TraceStop if BLIP is in a TraceStop region</td>
<td>PIP(new CR3, NR??), TraceStop?</td>
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<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
<td>PIP(new CR3, NR??), MODE.Exec?, TIP.PGE(BLIP)</td>
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<tr>
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<td>HW Interrupt</td>
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<td>*PIP if CR3 is updated (i.e., task switch), and OS=1; *PIP.NR=1 if destination is not root operation, and “Suppress VMX indications” execution control = 0; *TraceStop if BLIP is in a TraceStop region</td>
<td>FUP(NLIP), PIP(new CR3, NR??), TIP.PGD(BLIP), TraceStop</td>
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<tr>
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<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
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<tr>
<td>11e</td>
<td>HW Interrupt</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
<td>FUP(NLIP), PIP(NewCR3, NR?), MODE.Exec?, TIP(BLIP)</td>
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<td>*PIP.NR=1 if destination is not root operation, and</td>
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<td>“Suppress VMX indications” execution control = 0;</td>
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<td>* MODE.Exec if the operation changes CS.L/D or</td>
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<tr>
<td>12a</td>
<td>SW Interrupt</td>
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<td>0</td>
<td>0</td>
<td>None</td>
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</tr>
<tr>
<td>12f</td>
<td>SW Interrupt</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
<td>PIP(NewCR3, NR?), TraceStop?</td>
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<td>*PIP.NR=1 if destination is not root operation, and</td>
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<td>* MODE.Exec if the mode has changed since the last</td>
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<td>MODE.Exec, or if no</td>
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<td>MODE.Exec since last PSB</td>
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<td>12b</td>
<td>SW Interrupt</td>
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<td>1</td>
<td>1</td>
<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
<td>PIP(NewCR3, NR?), MODE.Exec?, TIP.PGE(BLIP)</td>
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<td>SW Interrupt</td>
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<td>FUP(CLIP), TIP.PGD()</td>
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<td>12d</td>
<td>SW Interrupt</td>
<td>1</td>
<td>0</td>
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<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
<td>FUP(CLIP), PIP(NewCR3, NR?), TIP.PGD(BLIP), TraceStop?</td>
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<tr>
<td>12e</td>
<td>SW Interrupt</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
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<td>*PIP.NR=1 if destination is not root operation, and</td>
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<td>IA32_EFER.LMA</td>
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<tr>
<td>13a</td>
<td>Exception/Fault</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>None</td>
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<th>Operation</th>
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<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
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<tbody>
<tr>
<td>13f</td>
<td>Exception/Fault</td>
<td>0</td>
<td>0</td>
<td>1</td>
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<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
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<td>* PIP.NR=1 if destination is not root operation, and “Suppress VMX indications”</td>
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<td></td>
<td></td>
<td>*TraceStop if BLIP is in a TraceStop region</td>
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<td>13b</td>
<td>Exception/Fault</td>
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<td>1</td>
<td>1</td>
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<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
</tr>
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<td>*MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB</td>
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<td>PIP(NewCR3, NR?)?, MODE.Exec?, TIP.PGE(BLIP)</td>
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<td>Exception/Fault</td>
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<td>0</td>
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<td>FUP(CLIP), TIP.PGD()</td>
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<tr>
<td>13d</td>
<td>Exception/Fault</td>
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<td>1</td>
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<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
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<td>13e</td>
<td>Exception/Fault</td>
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<td>1</td>
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<td>* PIP if CR3 is updated (i.e., task switch), and OS=1</td>
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<td>execution control = 0;</td>
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<td>* MODE.Exec if the operation changes CS.L/D or IA32_EFER.LMA</td>
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<td>FUP(CLIP), PIP(NewCR3, NR?)?, MODE.Exec?, TIP(BLIP)</td>
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<td>SMI (TraceEn cleared)</td>
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<td>D.C.</td>
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<td>SMI (TraceEn cleared)</td>
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<td>0</td>
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<td>FUP(SMRAM,LIP), TIP.PGD()</td>
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<td>14f</td>
<td>SMI (TraceEn cleared)</td>
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<td>NA</td>
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<td>SMI (TraceEn cleared)</td>
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<td>NA</td>
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<td>RSM, TraceEn restored to 0</td>
<td>0</td>
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<td>None</td>
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<td>15b</td>
<td>RSM, TraceEn restored to 1</td>
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<td>D.C.</td>
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<td>RSM, TraceEn restored to 1</td>
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<td>RSM (TraceEn=1, goes to shutdown)</td>
<td>1</td>
<td>0</td>
<td>0</td>
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<td>RSM (TraceEn=1, goes to shutdown)</td>
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<td>RSM (TraceEn=1, goes to shutdown)</td>
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<td>None</td>
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<td>Vmexit</td>
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<td>None</td>
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<td>Vmexit</td>
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<td>*PIP if OF=1, and “Suppress VMX packets on exit” execution control = 0; *TraceStop if VMCSH.LIP is in a TraceStop region</td>
<td>PIP(HostCR3, NR=0)?, TraceStop?</td>
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<td>VM exit, MSR list sets TraceEn=1</td>
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<td>See WRMSR cases for packets on enable. FUP IP is VMCSH.LIP</td>
<td>See WRMSR cases for packets on enable. FUP/TIPPG.IP is VMCSH.LIP</td>
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<td>See WRMSR cases for packets on enable. FUP/TIPPG.IP is VMCSH.LIP</td>
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<td>VM exit</td>
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<td>*PIP if OF=1, and “Suppress VMX packets on exit” execution control = 0; *MODE.Exec if the value is different, since last TIPPGD</td>
<td>PIP(HostCR3, NR=0)?, MODE.Exec?, TIPPGD(VMCSH.LIP)</td>
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<td>*PIP if OF=1, and “Suppress VMX packets on exit” execution control = 0;</td>
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<td>FUP(VMCSG.LIP), PIP(HostCR3, NR=0)?, MODE.Exec, TIP(VMCSH.LIP)</td>
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<td>VM entry</td>
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<td>*PIP if OF=1, and “Suppress VMX packets on entry” execution control = 0; *TraceStop if VMCSg.LIP is in a TraceStop region</td>
<td>PIP(GuestCR3, NR=1)?, TraceStop?</td>
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<td>VM entry, FilterEN 0-&gt;1</td>
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<td>*PIP if OF=1, and “Suppress VMX packets on entry” execution control = 0; *MODE.Exec if the value is different, since last TIP.PGD</td>
<td>PIP(GuestCR3, NR=1)?, MODE.Exec?, TIPPGE(VMCSg.LIP)</td>
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<td>VM entry, ContextEN 0-&gt;1</td>
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<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
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<td>VM entry, MSR list clears TraceEn=0</td>
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<td>PIP(GuestCR3, NR=1)?, TIPP.GD</td>
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<tr>
<td>17h</td>
<td>VM entry</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*PIP if OF=1, and “Suppress VMX packets on entry” execution control = 0; *TraceStop if VMCSg.LIP is in a TraceStop region</td>
<td>PIP(GuestCR3, NR=1)?, TIPP(GD(VMCSg.LIP), TraceStop?)</td>
</tr>
<tr>
<td>17i</td>
<td>VM entry</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>*PIP if OF=1, and “Suppress VMX packets on entry” execution control = 0; *MODE.Exec if the value is different, since last TIP.PGD</td>
<td>PIP(GuestCR3, NR=1)?, MODE.Exec, TIPP(VMCSg.LIP)</td>
</tr>
<tr>
<td>20a</td>
<td>EENTER/ERESUME to non-debug enclave</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>20c</td>
<td>EENTER/ERESUME to non-debug enclave</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>FUP(CLIP), TIPP.GD()</td>
<td>FUP(CLIP), TIPP.GD()</td>
</tr>
<tr>
<td>21a</td>
<td>EEEXIT from non-debug enclave</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>21b</td>
<td>EEEXIT from non-debug enclave</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIPPGE(BLIP)</td>
</tr>
<tr>
<td>22a</td>
<td>AEX/EEE from non-debug enclave</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>22b</td>
<td>AEX/EEE from non-debug enclave</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIPPGE(AEP.LIP)</td>
</tr>
<tr>
<td>23a</td>
<td>EENTER/ERESUME to debug enclave</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>23b</td>
<td>EENTER/ERESUME to debug enclave</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIPPGE(BLIP)</td>
</tr>
<tr>
<td>23c</td>
<td>EENTER/ERESUME to debug enclave</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>23d</td>
<td>EENTER/ERESUME to debug enclave</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*TraceStop if BLIP is in a TraceStop region</td>
<td>FUP(CLIP), TIPP.GD(BLIP), TraceStop?</td>
</tr>
<tr>
<td>23e</td>
<td>EENTER/ERESUME to debug enclave</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>24f</td>
<td>EEEXIT from debug enclave</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>24b</td>
<td>EEEXIT from debug enclave</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIPP.GD(BLIP)</td>
</tr>
<tr>
<td>24d</td>
<td>EEEXIT from debug enclave</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*TraceStop if BLIP is in a TraceStop region</td>
<td>FUP(CLIP), TIPP.GD(BLIP), TraceStop?</td>
</tr>
<tr>
<td>24e</td>
<td>EEEXIT from debug enclave</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>25a</td>
<td>AEX/EEE from debug enclave</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>
### Table 36-47. Packet Generation under Different Enable Conditions

<table>
<thead>
<tr>
<th>Case</th>
<th>Operation</th>
<th>PktEn Before</th>
<th>PktEn After</th>
<th>CntxEn After</th>
<th>Other Dependencies</th>
<th>Packets Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>25b</td>
<td>AEX/EEE from debug enclave</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIP.PGE(AEP.LIP)</td>
</tr>
<tr>
<td>25d</td>
<td>AEX/EEE from debug enclave</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*For AEX, FUP IP could be NLIP, for trap-like events</td>
<td>FUP(CLIP), TIP.PGD(AEP.LIP)</td>
</tr>
<tr>
<td>25e</td>
<td>AEX/EEE from debug enclave</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>*MODE.Exec if the value is different, since last TIP.PGD</td>
<td>FUP(CLIP), MODE.Exec?, TIP(AEP.LIP)</td>
</tr>
<tr>
<td>26a</td>
<td>XBEGIN/XACQUIRE</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>26d</td>
<td>XBEGIN/XACQUIRE that does not set InTX</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>26e</td>
<td>XBEGIN/XACQUIRE that sets InTX</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MODE(InTX=1, TXAbort=0), FUP(CLIP)</td>
<td></td>
</tr>
<tr>
<td>27a</td>
<td>XEND/XRELEASE</td>
<td>0</td>
<td>0</td>
<td>D.C.</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>27d</td>
<td>XEND/XRELEASE that does not clear InTX</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>27e</td>
<td>XEND/XRELEASE that clears InTX</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>MODE(InTX=0, TXAbort=0), FUP(CLIP)</td>
<td></td>
</tr>
<tr>
<td>28a</td>
<td>XABORT(Async XAbort, or other)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>28d</td>
<td>XABORT(Async XAbort, or other)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*TraceStop if BLIP is in a TraceStop region</td>
<td>MODE(InTX=0, TXAbort=1), TraceStop?</td>
</tr>
<tr>
<td>28b</td>
<td>XABORT(Async XAbort, or other)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>MODE(InTX=0, TXAbort=1), TIP.PGE(ResetLIP)</td>
<td></td>
</tr>
<tr>
<td>28c</td>
<td>XABORT(Async XAbort, or other)</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>*TraceStop if BLIP is in a TraceStop region</td>
<td>MODE(InTX=0, TXAbort=1), TIP.PGD(Blip), TraceStop?</td>
</tr>
<tr>
<td>30a</td>
<td>INIT (BSP)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>None</td>
<td></td>
</tr>
<tr>
<td>30b</td>
<td>INIT (BSP)</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>*TraceStop if RESET.LIP is in a TraceStop region</td>
<td>BIP(0), TraceStop?</td>
</tr>
<tr>
<td>30c</td>
<td>INIT (BSP)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>* MODE.Exec if the value is different, since last TIP.PGD</td>
<td>MODE.Exec?, TIP.PGE(ResetLIP)</td>
</tr>
<tr>
<td>30d</td>
<td>INIT (BSP)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>FUP(NLIP), TIP.PGD()</td>
<td></td>
</tr>
<tr>
<td>30e</td>
<td>INIT (BSP)</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>* PIP if OS=1</td>
<td>FUP(NLIP), PIP(0), TIP.PGD, TraceStop?</td>
</tr>
<tr>
<td>30f</td>
<td>INIT (BSP)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>* MODE.Exec if the mode has changed since the last MODE.Exec, or if no MODE.Exec since last PSB, PIP if OS=1</td>
<td>FUP(NLIP), PIP(0), MODE.Exec?, TIP(ResetLIP)</td>
</tr>
<tr>
<td>31a</td>
<td>INIT (AP, goes to wait-for-SIPI)</td>
<td>0</td>
<td>D.C.</td>
<td>D.C.</td>
<td>None</td>
<td></td>
</tr>
</tbody>
</table>
36.8 SOFTWARE CONSIDERATIONS

36.8.1 Tracing SMM Code

Nothing prevents an SMM handler from configuring and enabling packet generation for its own use. As described in Section , SMI will always clear TraceEn, so the SMM handler would have to set TraceEn in order to enable tracing. There are some unique aspects and guidelines involved with tracing SMM code, which follows:

1. SMM should save away the existing values of any configuration MSRs that SMM intends to modify for tracing. This will allow the non-SMM tracing context to be restored before RSM.
2. It is recommended that SMM wait until it sets CSbase to 0 before enabling packet generation, to avoid possible LIP vs RIP confusion.
3. Packet output cannot be directed to SMRR memory, even while tracing in SMM.
4. Before performing RSM, SMM should take care to restore modified configuration MSRs to the values they had immediately after #SMI. This involves first disabling packet generation by clearing TraceEn, then restoring any other configuration MSRs that were modified.
5. RSM
   - Software must ensure that TraceEn=0 at the time of RSM. Trailing RSM is not a supported usage model, and the packets generated by RSM are undefined.
   - For processors on which Intel PT and LBR use are mutually exclusive (see Section 36.3.1.2), any RSM during which TraceEn is restored to 1 will suspend any LBR or BTS logging.

36.8.2 Cooperative Transition of Multiple Trace Collection Agents

A third-party trace-collection tool should take into consideration the fact that it may be deployed on a processor that supports Intel PT but may run under any operating system.
In such a deployment scenario, Intel recommends that tool agents follow similar principles of cooperative transition of single-use hardware resources, similar to how performance monitoring tools handle performance monitoring hardware:

- Respect the "in-use" ownership of an agent who already configured the trace configuration MSRs, see architectural MSRs with the prefix "IA32_RTIT_" in Chapter 35, "Model-Specific Registers (MSRs)", where "in-use" can be determined by reading the "enable bits" in the configuration MSRs.
- Relinquish ownership of the trace configuration MSRs by clearing the "enabled bits" of those configuration MSRs.

### 36.8.3 Tracking Time

This section describes the relationships of several clock counters whose update frequencies reside in different domains that feed into the timing packets. To track time, the decoder also needs to know the regularity or irregularity of the occurrences of various timing packets that store those clock counters.

Intel PT provides time information for three different but related domains:

- **Processor timestamp counter**
  
  This counter increments at the max non-turbo or P1 frequency, and its value is returned on a RDTSC. Its frequency is fixed. The TSC packet holds the lower 7 bytes of the timestamp counter value. The TSC packet occurs occasionally and are much less frequent than the frequency of the time stamp counter. The timestamp counter will continue to increment when the processor is in deep C-States, with the exception of processors reporting CPUID.80000007H:EDX.InvariantTSC[bit 8] =0.

- **Core crystal clock**

  The ratio of the core crystal clock to timestamp counter frequency is known as P, and can calculating CPUID.15H:EBX[31:0] / CPUID.15H:EAX[31:0]. The frequency of the core crystal clock is fixed and lower than that of the timestamp counter. The periodic MTC packet is generated based on software-selected multiples of the crystal clock frequency. The MTC packet is expected to occur more frequently than the TSC packet.

- **Processor core clock**

  The processor core clock frequency can vary due to P-state and thermal conditions. The CYC packet provides elapsed time as measured in processor core clock cycles relative to the last CYC packet.

A decoder can use all or some combination of these packets to track time at different resolutions throughout the trace packets.

### 36.8.3.1 Time Domain Relationships

The three domains are related by the following formula:

\[
\text{TimeStampValue} = (\text{CoreCrystalClockValue} \times P) + \text{AdjustedProcessorCycles} + \text{Software_Offset};
\]

The CoreCrystalClockValue can provide the coarse-grained component of the TSC value. P, or the TSC/"core crystal clock" ratio, can be derived from CPUID leaf 15H, as described in Section 36.8.3.

The AdjustedProcessorCycles component provides the fine-grained distance from the rising edge of the last core crystal clock. Specifically, it is a cycle count in the same frequency as the timestamp counter from the last crystal clock rising edge. The value is adjusted based on the ratio of the processor core clock frequency to the Maximum Non-Turbo (or P1) frequency.

The Software_Offsets component includes software offsets that are factored into the timestamp value, such as IA32_TSC_ADJUST.

### 36.8.3.2 Estimating TSC within Intel PT

For many usages, it may be useful to have an estimated timestamp value for all points in the trace. The formula provided in Section 36.8.3.1 above provides the framework for how such an estimate can be calculated from the various timing packets present in the trace.

The TSC packet provides the precise timestamp value at the time it is generated; however, TSC packets are infrequent, and estimates of the current timestamp value based purely on TSC packets are likely to be very inaccurate
for this reason. In order to get more precise timing information between TSC packets, CYC packets and/or MTC packets should be enabled.

MTC packets provide incremental updates of the CoreCrystalClockValue. On processors that support CPUID leaf 15H, the frequency of the timestamp counter and the core crystal clock is fixed, thus MTC packets provide a means to update the running timestamp estimate. Between two MTC packets A and B, the number of crystal clock cycles passed is calculated from the 8-bit payloads of respective MTC packets:

\[
(CTC_B - CTC_A), \text{ where } CTC_i = MTC_i[15:8] << IA32_RTIT_CTL.MTCFreq \text{ and } i = A, B.
\]

The time from a TSC packet to the subsequent MTC packet can be calculated using the TMA packet that follows the TSC packet. The TMA packet provides both the crystal clock value (lower 16 bits, in the CTC field) and the AdjustedProcessorCycles value (in the FastCounter field) that can be used in the calculation of the corresponding core crystal clock value of the TSC packet.

When the next MTC after a pair of TSC/TMA is seen, the number of crystal clocks passed since the TSC packet can be calculated by subtracting the TMA.CTC value from the time indicated by the MTCNext packet by

\[
CTC_{\text{Delta}}[15:0] = (CTC_{\text{Next}}[15:0] - \text{TMA.CTC}[15:0]), \text{ where } CTC_{\text{Next}} = MTC_{\text{Payload}} << IA32_RTIT_CTL.MTCFreq.
\]

The TMA.FastCounter field provides the fractional component of the TSC packet into the next crystal clock cycle. CYC packets can provide further precision of an estimated timestamp value to many non-timing packets, by providing an indication of the time passed between other timing packets (MTCs or TSCs).

When enabled, CYC packets are sent preceding each CYC-eligible packet, and provide the number of processor core clock cycles that have passed since the last CYC packet. Thus between MTCs and TSCs, the accumulated CYC values can be used to estimate the adjusted_processor_cycles component of the timestamp value. The accumulated CPU cycles will have to be adjusted to account for the difference in frequency between the processor core clock and the P1 frequency. The necessary adjustment can be estimated using the core:bus ratio value given in the CBR packet, by multiplying the accumulated cycle count value by P1/CBRpayload.

A greater level of precision may be achieved by calculating the CPU clock frequency, see Section 36.8.3.4 below for a method to do so using Intel PT packets.

CYCs can be used to estimate time between TSCs even without MTCs, though this will likely result in a reduction in estimated TSC precision.

36.8.3.3 VMX TSC Manipulation

When software executes in non-Root operation, additional offset and scaling factors may be applied to the TSC value. These are optional, but may be enabled via VMCS controls on a per-VM basis. See Chapter 25, "VMX Non-Root Operation" for details on VMX TSC offsetting and TSC scaling.

Like the value returned by RDTSC, TSC packets will include these adjustments, but other timing packets (such as MTC, CYC, and CBR) are not impacted. In order to use the algorithm above to estimate the TSC value when TSC scaling is in use, it will be necessary for software to account for the scaling factor. See Section 36.5.2.6 for details.

36.8.3.4 Calculating Frequency with Intel PT

Because Intel PT can provide both wall-clock time and processor clock cycle time, it can be used to measure the processor core clock frequency. Either TSC or MTC packets can be used to track the wall-clock time. By using CYC packets to count the number of processor core cycles that pass in between a pair of wall-clock time packets, the ratio between processor core clock frequency and TSC frequency can be derived. If the P1 frequency is known, it can be applied to determine the CPU frequency. See Section 36.8.3.1 above for details on the relationship between TSC, MTC, and CYC.