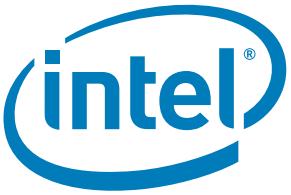
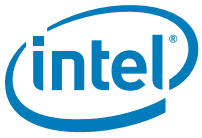


Intel® Xeon® Processor7500 Series Intel® Xeon® Processor E7-8800/4800/2800 Product Families

Thermal and Mechanical Design Guide

April 2011

Reference Number: 323342-002



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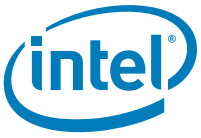
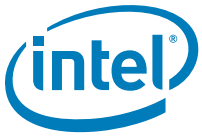


Figures

Tables



Revision History

Document Number	Revision Number	Description	Revision Date
323342	001	• Public release	March 2010
323342	002	• Update Intel® Xeon® processor E7-8800/4800/2800 product families	April 2011

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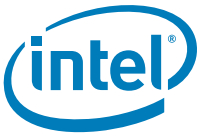
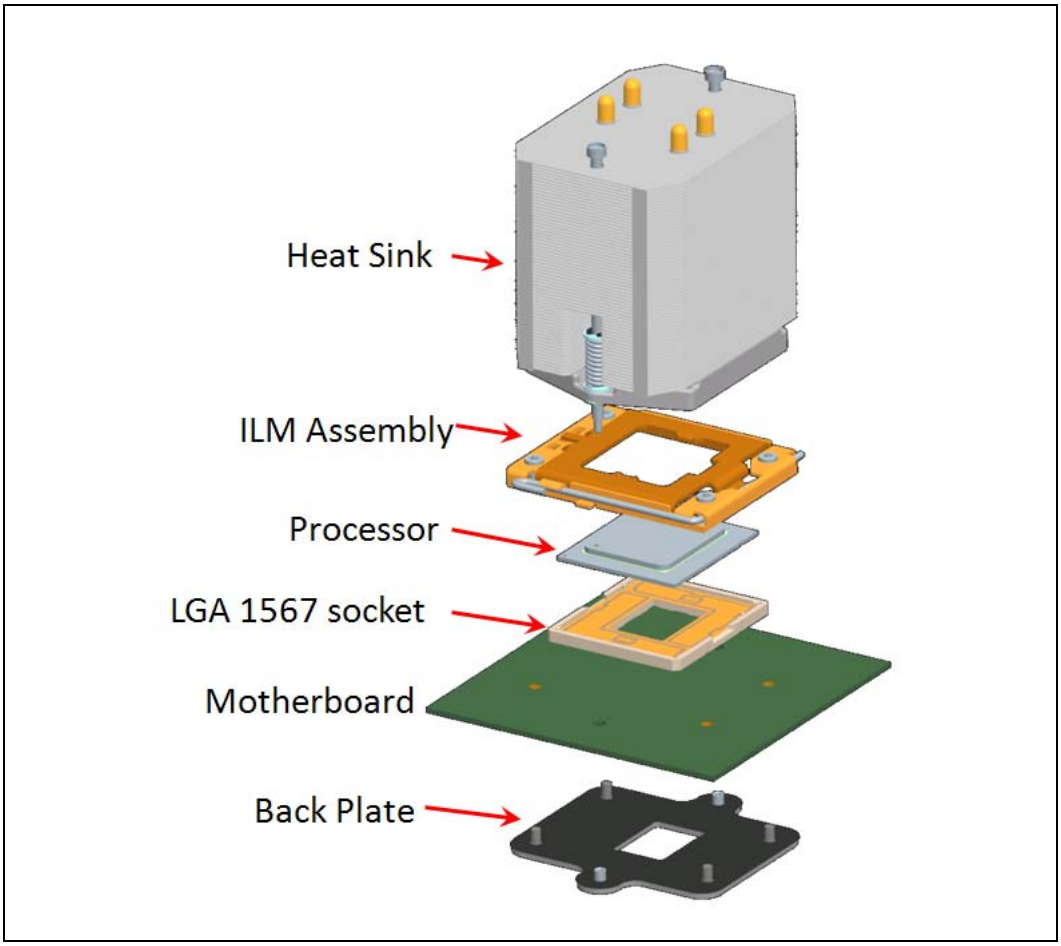


1 Introduction

This document provides guidelines for the design of thermal and mechanical solutions for the Intel® Xeon® processor 7500 series and the Intel® Xeon® processor E7-8800/4800/2800 product families. Both processors are compatible with the LGA1567 Socket (Chapter 2) and the ILM (Chapter 3). Both processors adhere to the same thermal specifications found in the *Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 1* and *Intel® Xeon® Processor 7500 Series Datasheet*, Volume 1 (see Table 1-1, "Reference Documents"). Thermal solutions designed for the Intel Xeon processor 7500 series will also be compatible with Intel Xeon processor E7-8800/4800/2800 product families (Chapter 4). The components described in this document include:

- The processor thermal solution (heatsink) and associated retention hardware
- The LGA1567 socket, Independent Loading Mechanism (ILM) and back plate

Figure 1-1. Socket Stack for the Intel® Xeon® Processor 7500 Series Platform



The goals of this document are:

- To assist board and system thermal mechanical designers

- To assist designers and suppliers of processor heatsinks

Thermal profiles and other processor specifications are provided in *Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 1* and *Intel® Xeon® Processor 7500 Series Datasheet*, Volume 1.

1.1 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1-1. Reference Documents

Document	Doc#	Notes
Intel® Xeon® Processor 7500 Series Datasheet, Volume 1	323340-001	1
Intel® Xeon® Processor 7500 Series Mechanical Model	323530-001	1
Intel® Xeon® Processor 7500 Series Thermal Model	323531-001	1
Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 1 of 2	325119-001	1
Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 2 of 2	325120-001	1
Intel® 7500, 7510, and 7512 Scalable Memory Buffer Thermal/Mechanical Design Guidelines	322828-002	1

Notes:
1. Document numbers indicated in Location column are subject to change. See IBP [http://tigris.intel.com/scripts-edk/viewer/UI_UpdateDesignKits.asp?edkID=7281&ProdID=21201&CatID=0] for the most up-to-date collateral list.

1.2 Definition of Terms

Table 1-2. Terms and Descriptions (Sheet 1 of 2)

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
ILM	Independent Loading Mechanism provides the force needed to seat the 1567-LGA land package onto the socket contacts.
LGA1567 socket	The processor mates with the system board through this surface mount, 1567-land socket.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Ψ_{CA}	Case-to-ambient thermal resistance parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA})$ / Total Package Power. Heat source should always be specified for Ψ measurements.
Ψ_{CS}	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S)$ / Total Package Power.

Table 1-2. Terms and Descriptions (Sheet 2 of 2)

Term	Description
Ψ_{SA}	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as (T_S – T_{LA}) / Total Package Power.
T_{CASE}	The case temperature of the processor, measured at the geometric center of the package substrate (not the IHS).
T_{CASE_MAX}	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	Tcontrol is a static value below TCC activation used as a trigger point for fan speed control.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
T_{LA}	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
T_{SA}	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.

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2 LGA1567 Socket

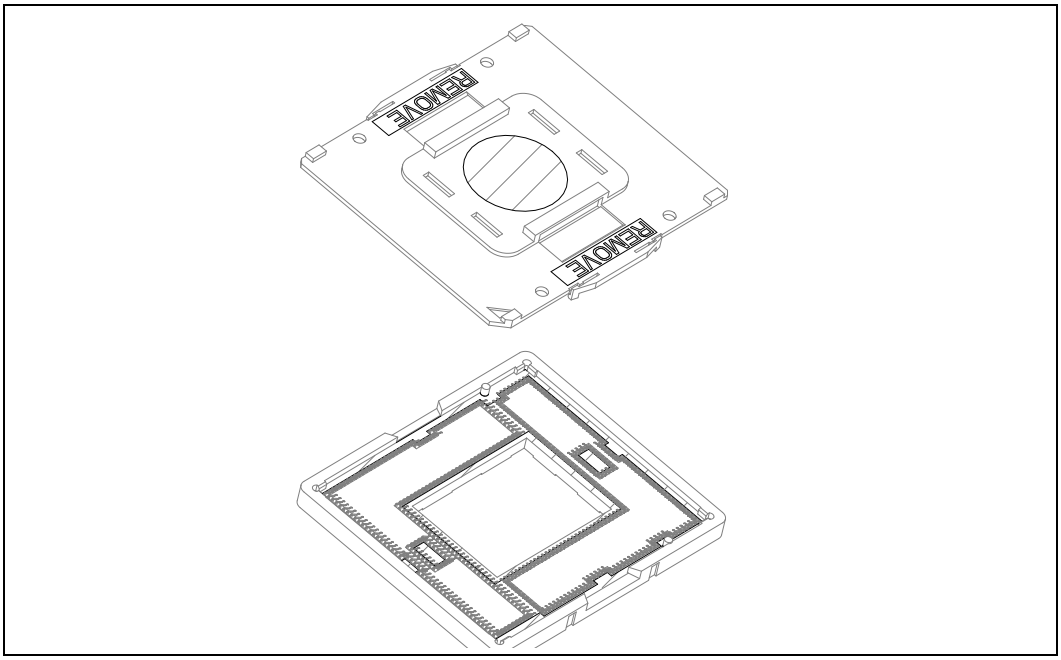
This section describes a surface mount, LGA (Land Grid Array) socket intended for Intel Xeon Processor 7500 Series and Intel Xeon processor E7-8800/4800/2800 product families. The socket provides I/O, power and ground contacts. The socket contains 1567contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The socket has 1567 contacts with 1.016 mm X 1.016 mm pitch (X by Y) in a 52x46 grid with 32x24 grid depopulation in the center of the array and selective depopulation elsewhere.

The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). The design includes a back plate which is integral to having a uniform load on the socket solder joints. Socket loading specifications are listed in Section 2-1.

See Appendix A for LGA1567 Socket supplier information and part numbers.

Figure 2-1. LGA1567 Socket with Pick and Place Cover Removed



2.1 Mechanical Requirements

2.1.1 Attachment to Printed Circuit Board (PCB)

The socket will be attached to the motherboard via its 1567 contact solder balls. There are no additional external methods (that is, screw, extra solder, adhesive, and so on) to attach the socket to the motherboard.

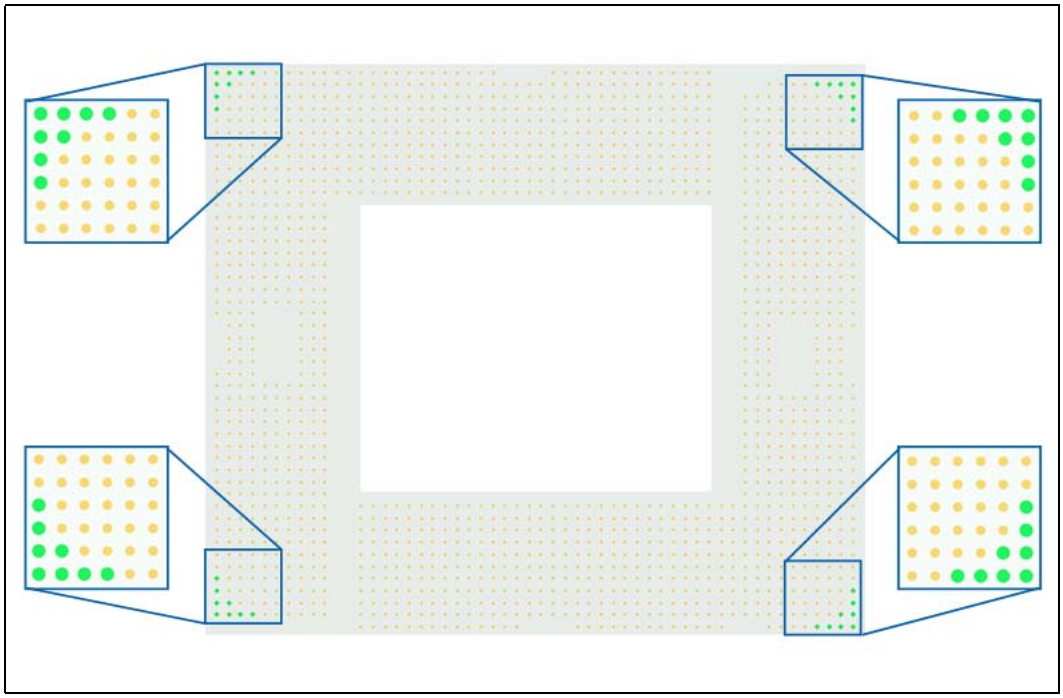
In installed condition, the socket is sandwiched between the processor package and the system board. An independent loading mechanism (ILM) will apply a static compression load, as described in this chapter.

2.1.2 Pad Dimensions

The system board must have a solder pad array matching socket BGA. Recommended solder pads are circular with a diameter of 0.45 mm (18 mils). They can be a combination of metal defined (MD) and solder mask defined (SMD).

Intel recommends that pads under the nCTF joints be solder mask defined (SMD). These are shown as the 8 corner pads at each of the 4 corners (marked in green in Figure 2-2) and should have a 26 mil Cu pad size.

Figure 2-2. Corner Pad Definition on board corresponding to nTCF Solder Balls

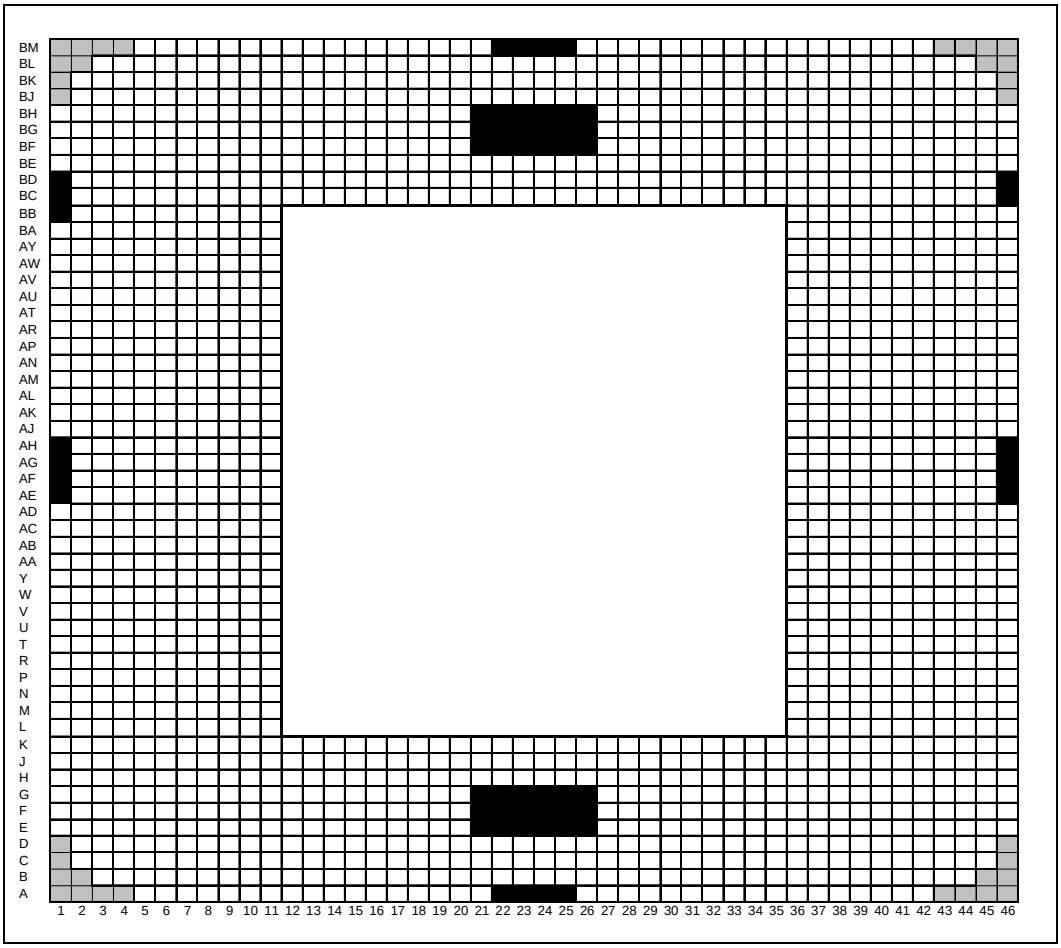


Also see Section 2.1.3.

2.1.3 LGA1567 Socket NCTF Solder Joints

Intel has defined selected solder joints of the socket as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality. Figure 2-3 identifies the NCTF solder joints.

Figure 2-3. LGA1567 Socket Contact Numbering and NCTF Solder Joints (Shown in Gray)



2.1.4 Socket Loading and Deflection Specifications

Table 2-1 provides load and board deflection specifications for the LGA1567 Socket. These mechanical limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 100 °C conditions.

Table 2-1. Socket Loading and Deflection Specifications (Sheet 1 of 2)

Parameter	SI Units			English Units			Notes
	Min	Max	Unit	Min	Max	Unit	
Static Compressive per Contact	15	38	gf	0.53	1.34	ozf	1
Static Pre-Load Compressive	289	623	N	60	140	lbf	2
Static Total Compressive	578	934	N	110	210	lbf	3
Dynamic Compressive		588	N		132	lbf	4

Table 2-1. Socket Loading and Deflection Specifications (Sheet 2 of 2)

Parameter		SI Units			English Units			Notes
		Min	Max	Unit	Min	Max	Unit	
Board Transient Strain								5
Board Deflection under socket solder ball array under Maximum Static Compressive Load	62 mil boards		0.30	mm		0.012	in.	6
	70 mil to 120 mil boards		0.25	mm		0.010	in.	

Notes:
1. The compressive load applied by the package on the LGA contacts to meet electrical performance. This condition must be satisfied throughout the life of the product.
2. The load applied by the ILM onto the socket through the processor package.
3. The total load applied by both the ILM and the heatsink onto the socket through the processor package.
4. Quasi-static equivalent compressive load applied during the mechanical shock from heatsink, calculated using a reference 600g heatsink with a 25G shock input and an amplification factor of 3 (600g x 25G x 3 = 99 lbf). This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this value. Intel reference system shock requirement for this product family is 25G input as measured at the chassis mounting location.
5. Maximum allowable strain below socket BGA corners during transient loading events (i.e., slow displacement events) which might occur during board manufacturing, assembly or testing. See the LGA1567 BFI Strain Guidance Sheet. Contact your CQE for this datasheet.
6. See Section 2.3 for more details. Reference Table 4-3, "Mechanical Parameters".

2.1.5 Clarification of Static Compressive Load Values

The minimum *Static Pre-Load Compressive* value listed in Table 2-1, "Socket Loading and Deflection Specifications" is the force provided by the ILM and should be sufficient for rudimentary continuity testing of the socket and/or board. *This load value will not ensure normal operation throughout the life of the product.* Please see Table 3-2, "ILM Load Specifications".

The minimum *Static Total Compressive* value listed in Table 2-1, "Socket Loading and Deflection Specifications" will ensure socket reliability over the life of the product and that the contact resistance between the processor and the socket contacts meets the values outlined in Table 2-3, "LGA1567 Electrical Requirements".

Please refer to Section 4.2 for a more thorough description of load distribution for the various ILMs and heatsinks.

2.1.6 Critical-to-Function Interfaces

Critical-to-function (CTF) dimensions for motherboard layout and assembled components' interface to the socket are identified in Table 2-2. The CTF values are detailed on the socket drawing, which is provided in Appendix B. All sockets manufactured must meet the specified CTF dimensions. These dimensions will be verified as part of the validation process.

Note: Unless otherwise specified, interpret dimensions and tolerances in accordance with ASME Y14.5M-1994. Dimensions are in millimeters.

Table 2-2. Critical-to-Function Interface Dimensions

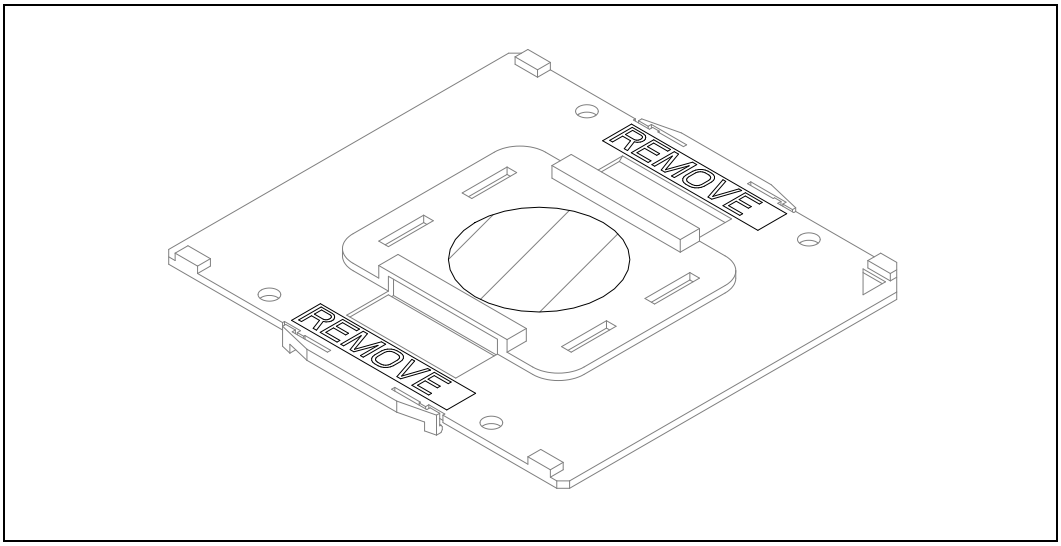
Description	Sheet/Zone
Socket Package Alignment Cavity Length *	D91065 rev 2, Sheet 2, Zone G6 and G7
Socket Package Alignment Cavity Width *	D91065 rev 2, Sheet 2, Zone F5
Socket Height (from Package Seating Plane to MB after Reflow) *	D91065 rev 2, Sheet 2, Zone A3
Seating Plane Co-planarity *	D91065 rev 2, Sheet 2, Zone C4
Through Cavity Length	D91065 rev 2, Sheet 2, Zone D6 and D7
Through Cavity Width	D91065 rev 2, Sheet 2, Zone E8
Through Cavity X-Position	D91065 rev 2, Sheet 2, Zone D6 and D7
Through Cavity Y-Position	D91065 rev 2, Sheet 2, Zone E8
Stand-Off Gap (Solder Ball to Stand-Off)	D91065 rev 2, Sheet 2, Zone C4
Solder Ball Feature Relating True Position	D91065 rev 2, Sheet 2, Zone C1
Solder Ball Co-planarity	D91065 rev 2, Sheet 2, Zone B3
Contact Height Above Seating Plane *	D91065 rev 2, Sheet 2, Zone A4 and A5
Contact True Position *	D91065 rev 2, Sheet 2, Zone C5
Contact Co-Planarity*	D91065 rev 2, Sheet 2, Zone B4 and B5

Note: *Dimensions are to be measured post SMT.

2.1.7 Pick-and-Place and Handling Cover

To facilitate high-volume manufacturing, the socket shall have a detachable cover to support the vacuum type Pick and Place system. The cover could also be used as a protective device to prevent damage to the contact field during motherboard assembly and handling. The cover design shall meet or exceed the applicable requirements of SEMI S8-0999, Safety Guidelines for Ergonomics/Human Factors Engineering of Semiconductor Manufacturing Equipment. The removal and replacement of the cover shall not cause any possible damage to the socket body, contact pins or the cover itself.

Figure 2-4. Pick-and-Place Cover (PnP Cap)



2.1.8 Socket Housing Material

The socket housing material should be of thermoplastic or equivalent, UL 94 V-0 flame rating, temperature rating, and design capable of maintaining structural integrity following a temperature of 260°C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket. The material must have a thermal coefficient of expansion in the XY plane capable of passing reliability tests rated for an expected high-operating temperature, mounted on HTg FR4-type motherboard material. The creep properties of the material must be such that the mechanical integrity of the socket is maintained for the use condition outlined in Chapter 5.

2.1.9 Socket Markings

All markings required in this section must withstand a temperature of 260°C for 40 seconds, which is typical of a reflow/rework profile for solder material used on the socket, as well as any environmental test procedure outlined in Chapter 5, without degrading.

2.1.9.1 Name

LF-LGA1567 (Font type is Helvetica Bold – minimum 6 point (or 2.125 mm)).

Note: This mark shall be stamped or laser marked into the sidewall of the stiffener plate on the actuation lever side.

Manufacturer's insignia (font size at supplier's discretion).

This mark will be molded or laser marked into the top side of the socket housing.

Both socket name and manufacturer's insignia will be visible when first seated on the motherboard.

2.1.9.2 Lot Traceability

Each socket will be marked with a lot identification code to allow traceability of all components, date of manufacture (year and week), and assembly location. The mark must be placed on a surface that is visible after the socket is mounted on the motherboard. In addition, this identification code must be marked on the exterior of the box in which the unit is shipped.

2.1.9.3 Pin 1 Identification

The socket will have markings identifying Pin 1. This marking will be represented by a clearly visible triangular symbol in the location specified.

2.1.10 Solder Ball Characteristics

2.1.10.1 Number of Solder Balls

Total number of solder balls: 1567.

2.1.10.2 Material

Lead free solder alloy having a melting point temperature of 217°C maximum (for example, SnAgCu) and be compatible with Immersions silver surface finish with SnAg/ SnAgCu solder paste.

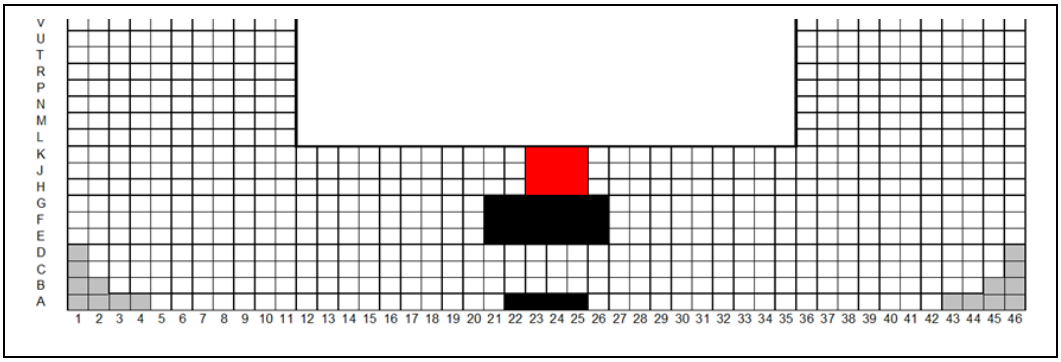
2.2 Maximum Socket Temperature

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

- Via temperature under socket < 96 °C

The recommend via used for temperature measurement is defined by K22 - H25. See Figure 2-5.

Figure 2-5. Recommended vias for Socket temperature measurement (shown in red)



The socket maximum temperature is defined at Thermal Design Current (TDC). In addition, the heatsink performance targets and boundary conditions of Table 4-1 and Table 4-2 must be met to limit power dissipation through the socket. To measure via temperature:

1. Drill a hole through the back plate at the specific via defined above.
2. Thread a T-type thermocouple (36 - 40 gauge) through the hole and glue it into the specific via on the underside of the motherboard.
3. Once the glue dries, reinstall the back plate and measure the temperature.

2.3 Electrical Requirements

LGA1567 electrical requirements (see Table 2-3) are measured from the socket-seating plane of the processor (end of the contacts) to the socket solder ball attach at the motherboard. All specifications are maximum values (unless otherwise stated) for a single socket contact, but includes effects of adjacent contacts where indicated. Socket inductance includes exposed metal from mated contact to the PCB land array.

Reference Appendix F for the methodology used to determine these values.

Table 2-3. LGA1567 Electrical Requirements (Sheet 1 of 2)

Parameter	Value	Notes
Maximum Mutual Capacitance, C	<0.33 pF	The capacitance between two contacts
Dielectric Withstand Voltage	> 360 Volts RMS	
Insulation Resistance	> 800 mΩ	

Table 2-3. LGA1567 Electrical Requirements (Sheet 2 of 2)

Parameter	Value	Notes
Contact Resistance, total at End of Life (EOL), 26 °C.	≤ 15.2 mΩ	The socket contact resistance target is derived from the resistance of each chain minus resistance of shorting bars divided by number contacts within the daisy chain. The bulk resistance of the contact metal body, and interface resistance to the package LGA lands are included. This LLCR target applies with 1% failure rate at 60% confidence interval among all measured chains of the whole population being tested.
Contact Bulk Resistance, at 26 °C	≤ 9.5 mΩ	Resistance of each contact as measured from tip to tip. Interface resistances are excluded. FEA model using minimum conductivity value can be used in lieu of measurement.
Contact Bulk Resistance Increase	≤ 3 mΩ	The bulk resistance increase per contact from 24°C to 100°C
Total Loop Inductance, Loop	<3.9 nH	The inductance calculated or measured for a pair of two adjacent contacts, considering one forward conductor and one return conductor. These values must be satisfied at the worst-case socket contact height (that is, minimum deflection) in assembled configuration
Mated partial mutual inductance, L	< 0.95 nH	The inductance on a contact due to any single neighboring contact.
Differential return loss	< -13 dB	Measurements/simulations conditions: 1. Termination impedance: 90 Ohm, differential 2. Test structure overview will be provided later 3. All details of Frequency domain S parameters specs will be provided in later revision
Differential Insertion loss	< |-0.6 dB|	
Cross-talk	< -25 dB	
Measurement frequency(s) for Contact-to-Contact inductance.	1 GHz	Linear region (usually found at higher frequency ranges)
Measurement frequency(s) for Contact-to-Contact capacitance.	400 MHz	Capacitively dominated region (usually the lowest measurable frequency)

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3 Independent Loading Mechanism (ILM)

The Independent Loading Mechanism (ILM) provides the force needed to seat the 1567-Land LGA package (i.e., processor) onto the socket contacts. The ILM is physically separate from the socket body. The ILM consists of two major components, the ILM cover and the back plate, that will be procured as a set from the enabled vendors. The assembly of the ILM is expected to occur after the socket is surface mounted. The exact assembly location is dependent on manufacturing preference and test flow. See the Manufacturing Advantage Service collateral for this platform for additional guidance.

The ILM has two critical functions:

- Deliver the force to seat the processor onto the socket contacts
- Distribute the resulting load evenly through the socket solder balls

3.1 Allowable Board Thickness

The components described in this document (namely ILM, back plate and heatsink) will support board thickness in the range of 1.8 - 3.0 mm (0.072" - 0.118"). Boards (PCBs) not within this range may require modifications to the back plate and heatsink retention. Please contact the component suppliers for modifications (see Appendix A, "Intel Enabling Component Suppliers").

3.2 Description of ILM Versions

There are two versions (SKUs) of ILM for the Nehalem-EX processor. The first version (as described in Rev 1.0 and previous) has been renamed to **High-Load ILM (HL-ILM)**. The second version of the ILM, called the **Low Profile ILM (LP-ILM)**, has important differences. The Low Profile ILM was developed to eliminate the need for a pedestal on the processor heatsink. An unavoidable trade-off is a reduction in the applied load by the Low Profile ILM. This requires that heatsink solutions implementing the LP-ILM will need to increase the load applied to the top of the IHS. Another requirement for heatsinks implementing the LP-ILM will be two small pockets in the heatsink bottom to clear the fingers which touch the top of the IHS. A summary of these differences is articulated in the following table.

Table 3-1. ILM Comparison Summary (Sheet 1 of 2)

		High Load ILM (HL-ILM)	Low Profile ILM (LP-ILM)
ILM Applied Load F_{ILM}	Min.	80 lbf / 400 N	60 lbf / 289 N
	Max	140 lbf / 623 N	105 lbf / 467 N
Heatsink Applied Load [1] $F_{HEATSINK}$	Min.	30 lbf / 178 N	50 lbf / 289 N
	Max	70 lbf / 311 N	105 lbf / 467 N

Table 3-1. ILM Comparison Summary (Sheet 2 of 2)

		High Load ILM (HL-ILM)	Low Profile ILM (LP-ILM)
Socket Static Total Compressive Load [2] F_{SOCKET}	Min.	110 lbf / 578 N	
	Max	210 lbf / 934 N	
Thermal resistance impact (C/W)		0.022	0 (baseline)
Heatsink required features		2.5mm pedestal	2 pockets (~14x12x2.5mm)

Notes:
1. See Table 4-3, "Mechanical Parameters", for more information on heatsink applied loads for each ILM implementation.
2. See Table 2-1, "Socket Loading and Deflection Specifications", for Static Total Compressive Load values. Socket load is the addition of the ILM and Heatsink applied load according to the equation: $F_{ILM} + F_{HEATSINK} = F_{SOCKET}$

A picture of each ILM version is shown in Figure 3-1 and Figure 3-2.

Both ILM versions will be "build to print" from Intel controlled drawings. See Appendix C for drawings.

See Appendix A, "Intel Enabling Component Suppliers" for ILM supplier information and part numbers.

3.3 ILM Assembly

The ILM is an assembly of a load plate, a frame, and a lever. Four fasteners secure the ILM frame to the backer plate.

All pieces in the ILM assembly, except the frame and fasteners, are fabricated from stainless steel and plated where appropriate. The frame is made from high-strength steel. The fasteners are fabricated from a high-carbon steel. The frame provides the hinge locations for the load lever and load plate.

The ILM design ensures that once installed onto the baseboard and secured to the backer plate, the only features touching the board are the captive fasteners. The nominal gap of the frame to the board is ~1 mm.

When the load plate is closed, compressive load is applied onto the processor package from the top of the IHS at two points. See load plate "dimpled" features shown in Figure 3-1. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the backer plate. Some of the load is passed through the socket body to the board, inducing a slight compression on the solder joints.

Figure 3-1. High Load ILM (HL-ILM) Assembly (shown with PCB and Processor)

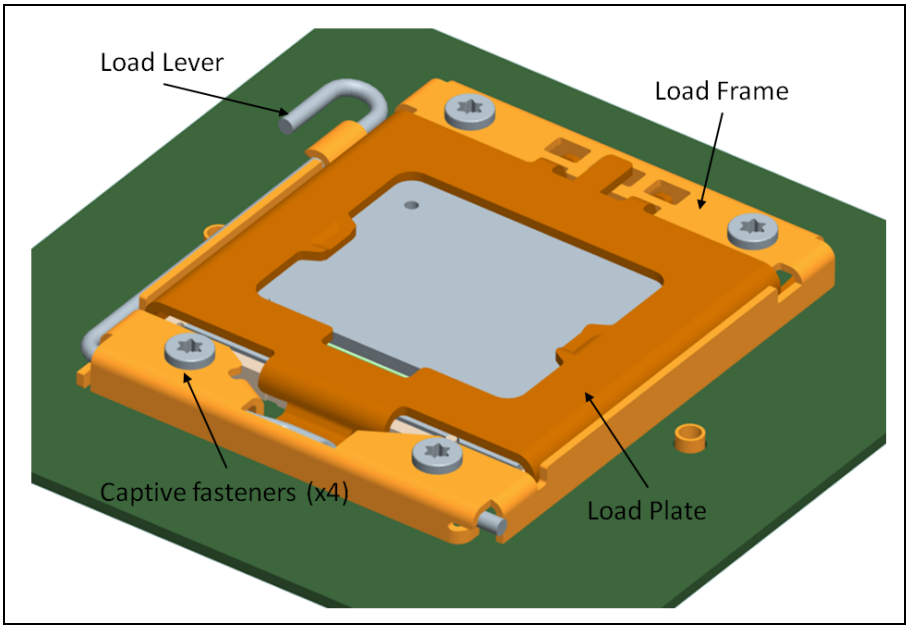
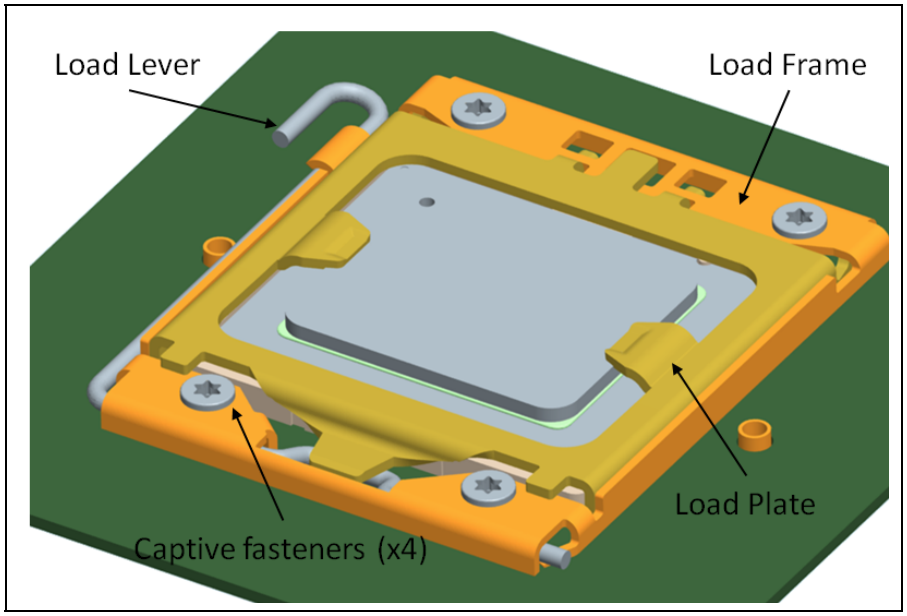


Figure 3-2. Low Profile ILM (LP-ILM) Assembly (shown with PCB and Processor)

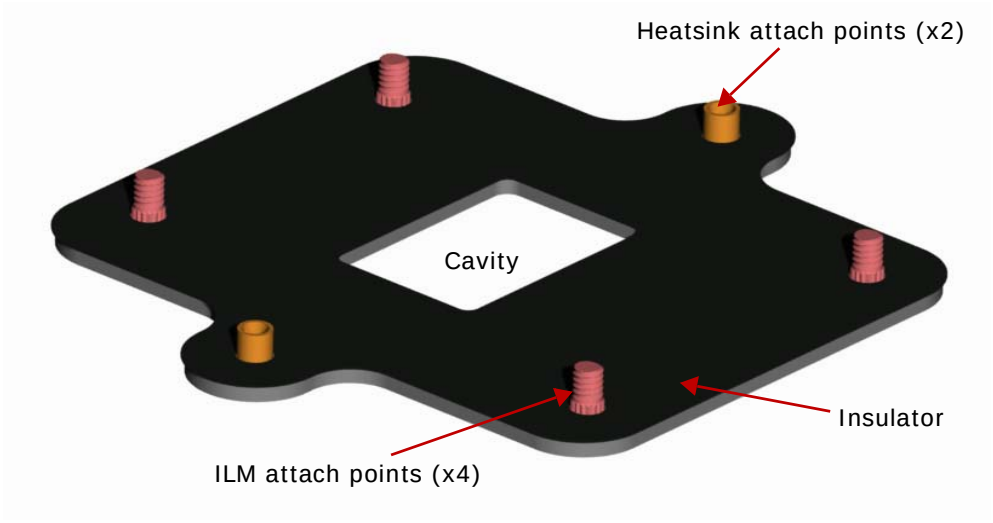


3.4 ILM Back Plate Assembly

The back plate consists of a flat steel back plate with four internally threaded inserts for ILM attach, and two inserts for heatsink attach. The inserts are press fit into the back plate. A cavity is located at the center of the plate to allow access to the baseboard test points and backside capacitors. An insulator is pre-applied to prevent shorting the board.

Both versions of the ILM (the LP-ILM and the HL-ILM) are compatible with this back plate.

Figure 3-3. Back Plate Assembly



3.5 ILM Load Specifications

The HL-ILM is designed to achieve the minimum Socket Static Pre-Load Compressive load specification. The thermal solution (heatsink) should apply additional load to achieve the Socket Static Total Compressive load (see Table 2-1, "Socket Loading and Deflection Specifications"). The heatsink load will be applied to the IHS (Integrated Heat Spreader). The dual-loading approach is represented by the following equation:

$$F_{ILM} + F_{HEATSINK} = F_{SOCKET}$$

The ILM static load targets are given in Table 3-2.

Table 3-2. ILM Load Specifications

Parameter	SI Units (N)		English Units (lbf)		Notes
	Min	Max	Min	Max	
HL-ILM Static Compressive Load	356	623	80	140	Nominal load = 467 N / 105 lbf
LP-ILM Static Compressive Load	267	467	60	105	Nominal load = 334 N / 75 lbf

3.6 ILM Cover

To provide additional protection to during manufacturing and handling, an ILM Cover is available to help mitigate damaging socket contacts. The ILM cover provides protection until a processor is installed.

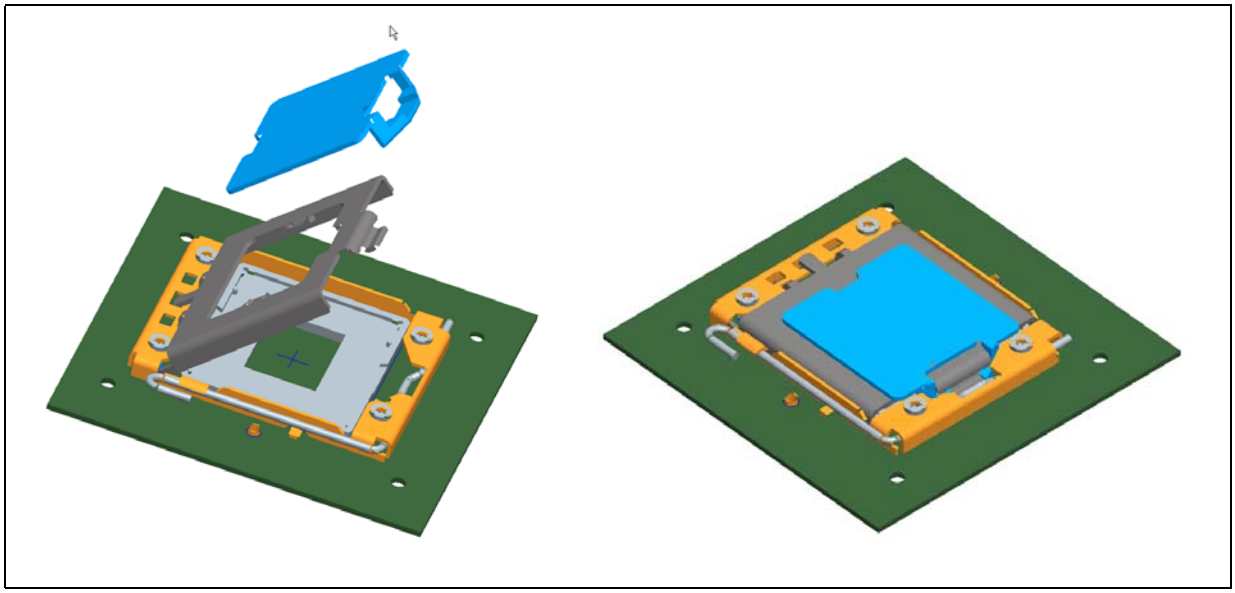
There are several versions developed that snap into the ILM. Please see Table A-2, "LGA1567 Socket and ILM Part Number and Supplier Contact Information" for ordering information.

There is an ILM Cover for each version of ILM.

3.6.1 HL-ILM Cover

The HL-ILM Cover *cannot* coexist with the LGA1567 Pick and Place Cover as shown in Figure 3-4. Meaning that the operator will need to remove the Socket Cap in order to install the ILM Cover. Please see Table A-2, "LGA1567 Socket and ILM Part Number and Supplier Contact Information".

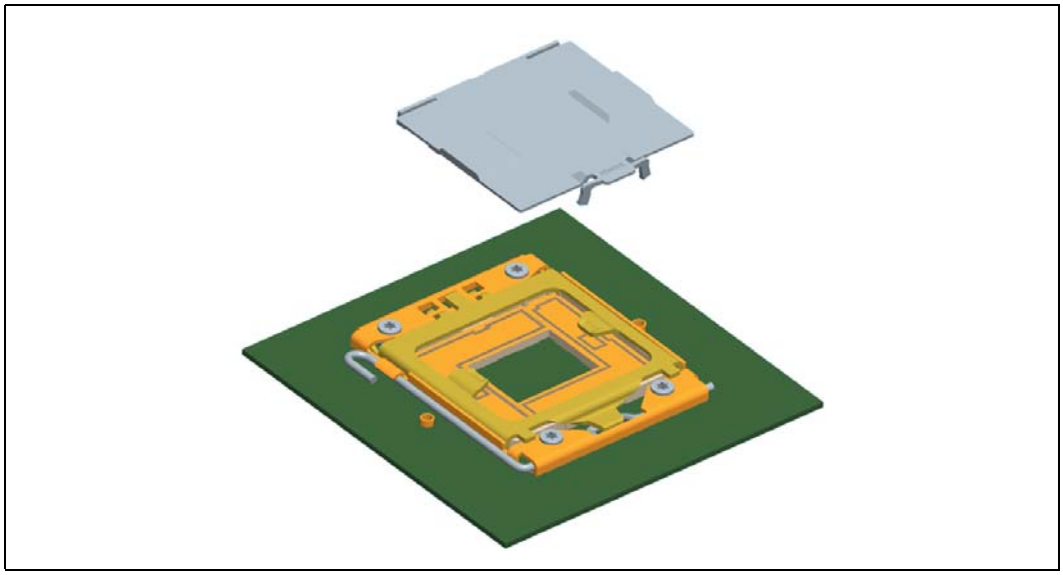
Figure 3-4. HL-ILM Cover assembly onto HL-ILM



3.6.2 LP-ILM Cover

The LP-ILM Cover *cannot* coexist with the LGA1567 Pick and Place Cover as shown in Figure 3-5. In fact, the LGA1567 Pick and Place Cover (Socket Cover) will not physically fit under the LP-ILM load plate once closed. Please see Table A-2, "LGA1567 Socket and ILM Part Number and Supplier Contact Information".

Figure 3-5. LP-ILM Cover Assembly onto LP-ILM



3.7 Components Assembly

The Intel Xeon processor 7500 series thermal mechanical solution assembly begins with surface mounting the LGA1567 socket onto the baseboard. The remaining steps assume the socket is already surface-mounted:

1. Back Plate and ILM Installation:

   The standoff pattern on the backer plate also acts as a key-in feature. Align the backer plate standoff pattern to the baseboard's hole pattern before mating the backer plate to the baseboard.

   Before installing the ILM, be sure that it is already assembled with the lever and the fasteners. The ILM fastener pattern also acts as a key-in feature. Align the ILM fastener pattern to the baseboard hole pattern. Tighten the fasteners with the matching torque driver set to ~8 in-lbf [0.9 N.m]. Verify that the ILM and the backer plate are properly installed. There should be a uniform gap between the ILM and the base board, and virtually no gap between the backer plate and the baseboard.

2. Processor Installation:

   Release the ILM lever to access the LGA1567 socket. Carefully remove the socket cover to avoid damaging the socket contacts. Inspect the socket for contact damage or foreign materials. Orient the processor such that the processor pin1 faces the same direction as the socket pin1. Carefully place the processor on the socket and verify that it is seated properly. Two side protrusions on the socket will prevent the package from resting flat on the socket if the processor is not properly aligned to the socket. Close the ILM cover and secure the lever.

For more detailed installation instructions as well as recommendations on board manufacturing, please download the *Intel® Xeon® Processor 7500 Series-based Platform Manufacturing Advantage Service* document found on http://learn.intel.com (please input code: ME709).

Figure 3-6. Socket and Backer Plate Assembly

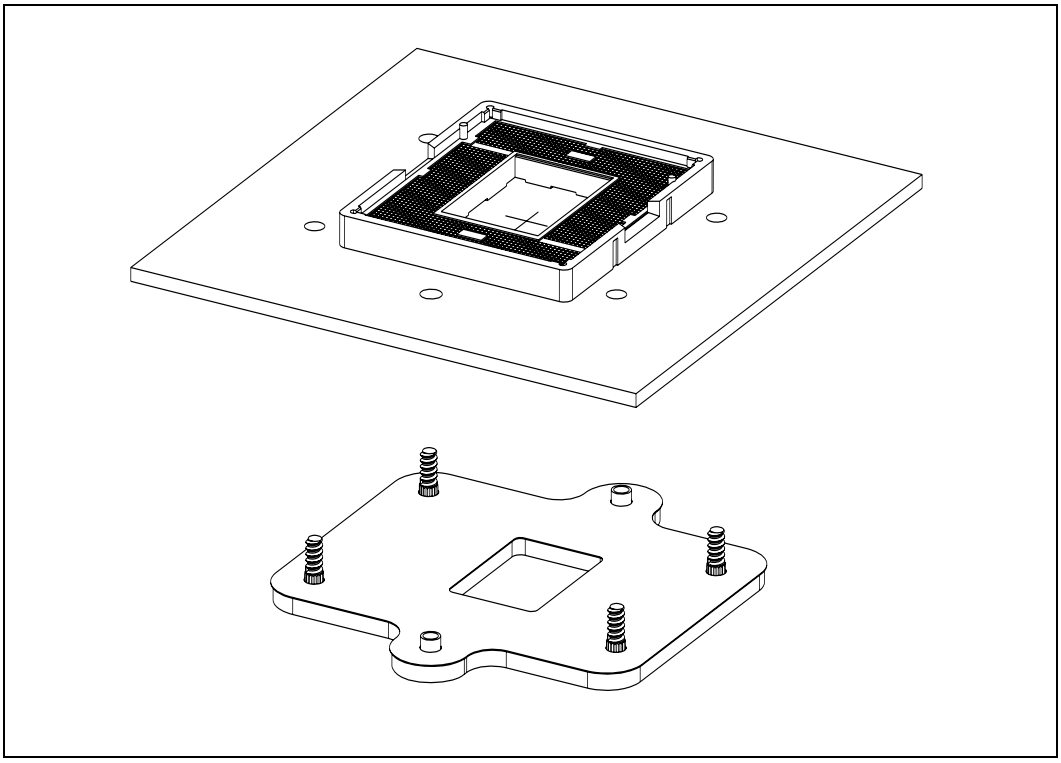
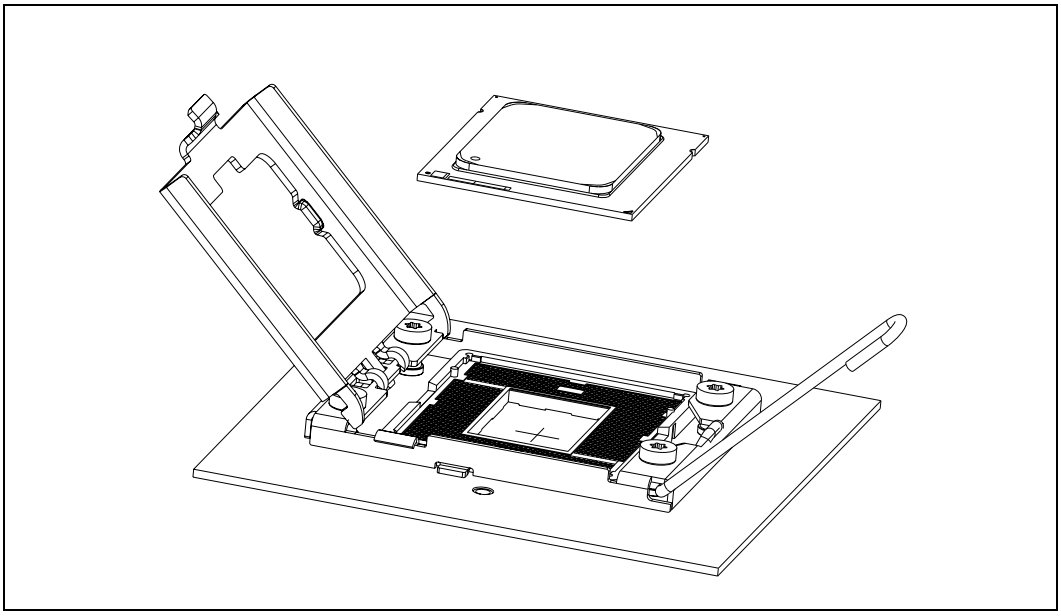


Figure 3-7. ILM and Processor Assembly



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4 Processor Thermal Solutions

This section describes the design guidelines for Intel® Xeon® processor 7500 Series thermal solutions. Also included are the Intel reference heatsink design specifications.

Intel's reference thermal solutions which were designed for the Intel® Xeon® Processor 7500 series will also be compatible with Intel® Xeon® processor E7-8800/ 4800/2800 product families thermal specifications.

4.1 Processor Thermal Targets

Table 4-1 provides thermal boundary conditions and performance targets for both the Intel Xeon Processor 7500 series and the Intel Xeon processor E7-8800/4800/2800 product families. These values should guide thermal solution design.

Table 4-1. Processor Boundary Conditions and Performance Targets

Parameter	Value		
Altitude, system ambient temp	Sea level, 35ºC		
TDP	95W	105W	130W
T_{LA}[1]	42ºC	42ºC	45ºC
Ψ_{CA}[2]	0.255 ºC/W	0.206 ºC/W	0.185 ºC/W
Ψ_{CA_MAX}[3]	0.295 ºC/W	0.210 ºC/W	0.185 ºC/W
Airflow[4]	12.6 CFM @ 0.34" ΔP	28 CFM @ 0.25" ΔP	36 CFM @ 0.20" ΔP
System height (form factor)[5]	1U	2U	4U
Heatsink volumetric[6]	90 x 90 x 26.5mm	90 x 90 x 51mm	100 x 70 x 102.5mm
Heatsink technology[7]	Cu base, Al fins	Cu base, Al fins	Cu/Al base / Al fins / heatpipes

Notes:
1. Local ambient temperature of the air entering the heatsink.
2. Estimated performance for each heatsink based on the form factor, technology, material, and boundary conditions. These estimates are **not** necessarily the thermal performance targets needed to meet processor thermal specifications. Please see *Intel® Xeon® Processor 7500 Series Datasheet, Volume 1* and *Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 1* for processor thermal specifications.
3. Defined as $(T_{CASE\_MAX} - T_{LA})$ / TDP
4. Airflow through the heatsink fins with zero bypass. Max target for pressure drop (ΔP) measured in inches H_2O.
5. Reference system configuration. 1U = 1.75".
6. Dimensions of heatsink do not include socket or processor.
7. Passive heatsinks with Honeywell* PCM45F

4.2 Mechanical Targets

Thermal solutions should be designed to meet the mechanical requirements described in this section.

Keep in mind that the heatsink retention will need to apply additional load in order to achieve the minimum Socket Static Total Compressive load (see Table 2-1, "Socket Loading and Deflection Specifications"). This load should be distributed over the IHS (Integrated Heat Spreader). The dual-loading approach is represented by the following equation.

$$F_{ILM} + F_{HEATSINK} = F_{SOCKET}$$

Values for the Heatsink applied loads are given in Table 4-3.

4.2.1 Package / Socket Stackup Height

Table 4-2 provides the stackup height of a processor and LGA1567 socket with processor fully seated on the socket seating plane.

Table 4-2. Processor and LGA1567 Socket Stackup Height

Integrated Stackup Height (mm) From Top of Board to Top of IHS	7.599 ± 0.50 mm

Notes:
1. This data is provided for information only, and should be derived from: (a) the height of the socket seating plane above the motherboard after reflow, given in Appendix B, "LGA 1567 Socket Mechanical Drawings", (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances that are given in *Intel® Xeon® Processor 7500 Series Datasheet, Volume 1* and *Intel® Xeon® Processor E7-8800/4800/2800 Product Families Datasheet, Volume 1*.

4.2.2 Mechanical Parameters

Table 4-3. Mechanical Parameters

Parameter	SI Units			English Units			Notes
	Min	Max	Unit	Min	Max	Unit	
Thermal Solution Mass (includes retention)			g		1.32	lbm	4
Heatsink Applied Static Compressive Load *(High Load ILM implementation)*	133	311	N	30	70	lbf	2,3
Heatsink Applied Static Compressive Load *(Low Profile ILM implementation)*	222	467	N	50	105	lbf	2,3
Heatsink Applied Dynamic only Compressive load		445	N		100	lbf	2,5,6
Processor Static Compressive Load			N		210	lbf	1
Processor Tensile Load		155	N		35	lbf	1
Processor Torque Load		7.9	N-m		70	lbf-in	1
Processor Shear Load		356	N		80	lbf	1

Notes:
1. In the case of a discrepancy, the most recent datasheets supersede targets listed in the above table.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
3. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
4. This specification applies for either thermal retention solutions that prevent baseboard deflection or for the Intel reference thermal solution.
5. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
6. An experimentally validated test condition used a heatsink mass of acceleration measured on a shock table with a dynamic amplification factor of 3. This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load.

4.3 Intel Reference Design Heat Sink

4.3.1 Allowable Board Thickness

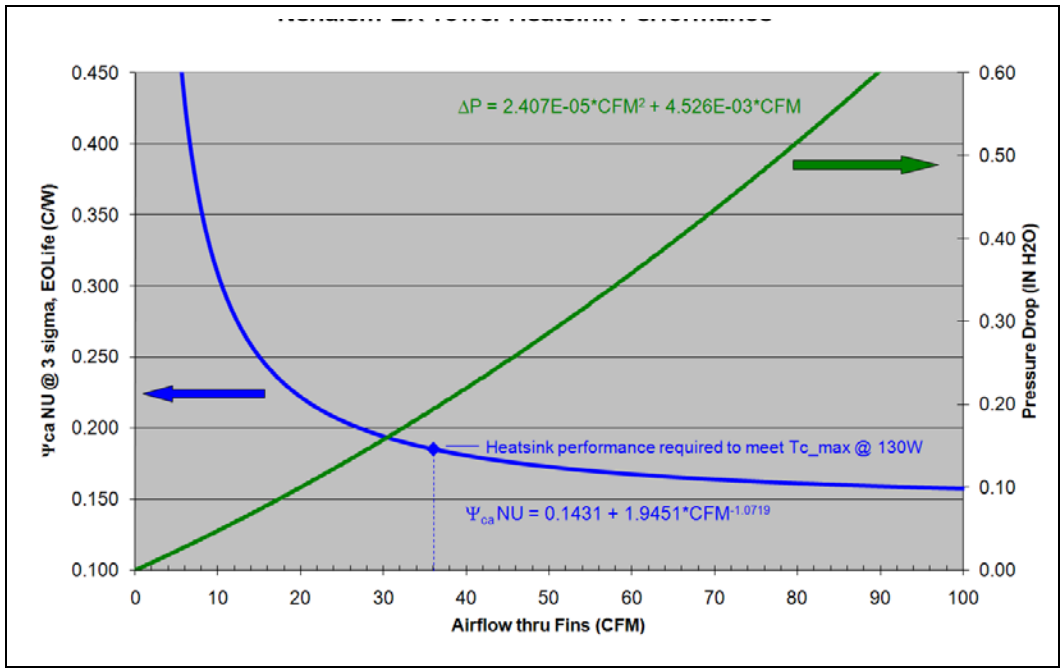
The Tower heat sink described in Section 4.3 will support board thickness in the range of 1.8 - 3.0 mm (0.072" - 0.118"). Boards (PCBs) not within this range may require modifications to the back plate and heatsink retention. Please contact suppliers for modifications (see Appendix A, "Intel Enabling Component Suppliers").

4.3.2 Tower Heatsink Performance

See Appendix D for detailed drawings of the Tower (4U) reference heatsink. Figure 4-1 shows thermal resistance (Ψ_{CA}) and pressure drop (ΔP) for the 4U heatsink versus the airflow provided. Best-fit equations are provided to prevent errors associated with reading the graph. They are:

- $\Delta P = (2.407 \times 10^{-05}) * CFM^2 + (4.526 \times 10^{-03}) * CFM$
- Ψ_{CA} NU = $0.1431 + 1.9451 * CFM^{-1.0719}$

Figure 4-1. Tower Heatsink Performance Curves for 130W



4.3.3 Tower Heatsink Load Range

The Tower Heatsink was thermally validated for the load range of 40 lbf to 70 lbf. This is different than the *Heatsink Applied Static Compressive Load* range listed in Table 4-3, "Mechanical Parameters" (that is, 30 lbf to 70 lbf) and may have a small effect on the heatsink performance.

4.3.4 Thermal Interface Material (TIM)

Honeywell PCM45F material was chosen for the Intel reference design. This material will be pre-applied onto the Tower heatsink pedestal.

The recommended size ensures adequate coverage at the interface between the processor IHS and heatsink pedestal.

Table 4-4. TIM Specification

Parameter	SI Units			English Units			Notes
	Min	Max	Unit	Min	Max	Unit	
TIM Size	24 x 33 by 0.43 thick		mm	0.94 x 1.30 by 0.017 thick		in.	Dimensions applies to Honeywell* PCM45F p/n: 95367
PCM45F Activation Load			N	28		lbf	Load required to meet min. TIM pressure (15 psi)

Refer to the TIM manufacturer's guidelines for specifications and handling instructions.

4.4 Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- **The area of the surface on which the heat transfer takes place –** Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.
- **The conduction path from the heat source to the heatsink fins –** Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it. Refer to Section 4.5 for further information on the TIM between the IHS and the heatsink base.
- **The heat transfer conditions on the surface upon which heat transfer takes place –** Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, T_{LA}, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.

An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface necessary to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is

more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

4.5 Thermal Interface Material (TIM) Considerations

Thermal Interface Material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective cover. Protective tape is not recommended as the TIM could be damaged during its removal step.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured T_{CASE} value of a given processor may increase over time, depending on the type of TIM material.

4.6 Mechanical Considerations

Note: Determining the performance for any thermal/mechanical solution is the responsibility of the customer.

An attachment mechanism must be designed to support the heatsink because there are no features on the LGA1567 socket on which to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the performance of the system, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Refer to Section 4.2.2 for information on trade-offs made with TIM selection. Designs should consider the possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events. The mechanical requirements of the attachment mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attachment mechanism. Their design should provide a means for protecting LGA1567 socket solder joints, as well as preventing package pullout from the socket.

Note: The load applied by the attachment mechanism must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as identified in Table 4-3.

A potential mechanical solution for heavy heatsinks is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

The Intel reference design for the Intel Xeon processor 7500 series uses such a heatsink attachment scheme. Refer to Section 4.4 for further information regarding the Intel reference mechanical solution.

4.7 Structural Considerations

The mass of the tower heatsinks should not exceed 600 g.

From Table 4-3, the Dynamic Compressive Load of 100 lbf max allows for designs that exceed 600 g as long as the mathematical product does not exceed 100 lbf. Example: A heatsink of 1.5 lbm (680 g) x 35G (acceleration) x 1.9 Dynamic Amplification Factor = 100 lbf.

The heatsink limit of 600g and the use of a back plate have eliminated the need for Direct Chassis Attach retention (as used with the previous Intel® Xeon® Processor 5000 Sequence). Direct contact between back plate and chassis pan will help minimize board deflection during shock.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.

4.8 Thermal Design Guidelines

4.8.1 Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a new feature available on certain processor SKUs that opportunistically, and automatically allow the processor to run faster than the marked frequency if all of the following conditions are met:

1. Processor operating at Base Frequency (that is, P1 P-state)
2. Power management not active (i.e., not throttling)
3. Processor operating below its temperature limit (that is, DTS < 0)
4. Processor operating below its power and current limits (that is, < TDP and $< I_{CC\_MAX}$).

Heatsink performance (lower Ψ_{CA} as described in Section 4.8) is one of several factors that can impact the amount of Turbo Mode benefit. Other factors are operating environment, workload and system design.

With Turbo Mode enabled, the processor may run more consistently at higher power levels (but still within TDP), and be more likely to operate above $T_{CONTROL}$, as compared to when Turbo Mode is disabled. This may result in higher acoustics.

Increased IMON accuracy may provide more Turbo Boost benefit on TDP limited applications, as compared to lower Ψ_{CA}, as temperature is not typically the limiter for these workloads. See *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 11.1 Design Guidelines (DocID: 397898)* for more information regarding IMON accuracy.

4.8.2 Absolute Processor Temperature

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature can be misleading.

4.8.3 Thermal Characterization Parameter

The case-to-local ambient Thermal Characterization Parameter (Ψ_{CA}) is defined by:

Equation 4-1. $\Psi_{CA} = (T_{CASE} - T_{LA}) / TDP$

Where:

- T_{CASE} = Processor case temperature (°C). For T_{CASE} specification see *Intel® Xeon® Processor E7- 8800/4800/2800 Product Families Datasheet Volume 1of 2*.
- T_{LA} = Local ambient temperature in chassis at processor (°C).
- **TDP** = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design. TTVs are often used to dissipate TDP. Correction offsets account for differences in temperature distribution between processor and TTV.

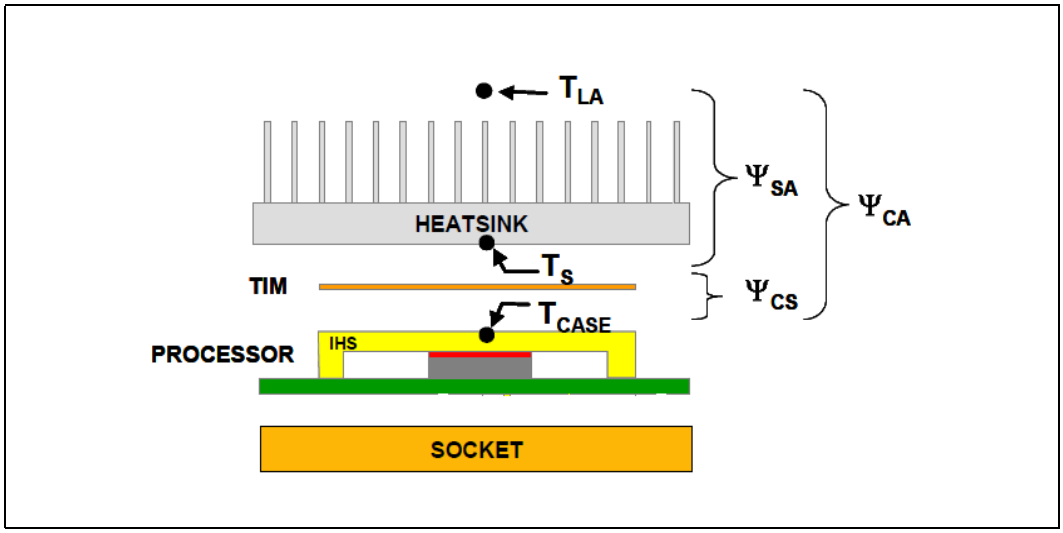
Equation 4-2. $\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$

Where:

- Ψ_{CS} = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.
- Ψ_{SA} = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

Figure 4-2 illustrates the thermal characterization parameters.

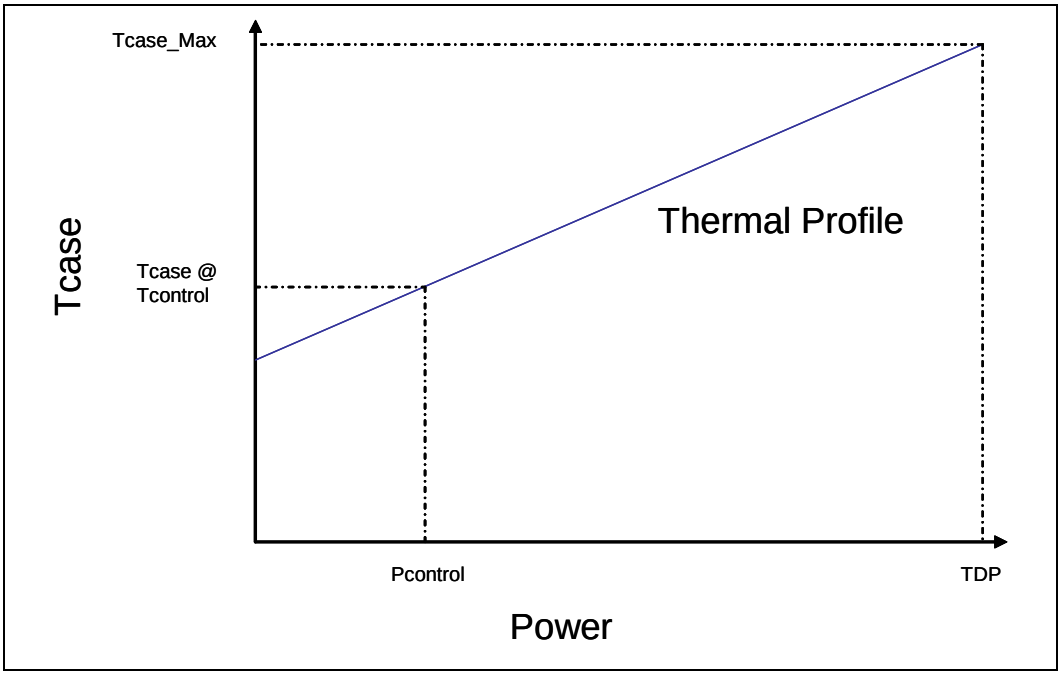
Figure 4-2. Processor Thermal Characterization Parameter Relationships



4.8.4 Fan Speed Control

Fan speed control (FSC) techniques to reduce system-level acoustic noise are a common practice in server designs. The fan speed is one of the parameters that determines the amount of airflow provided to the thermal solution. Additionally, airflow is proportional to a thermal solution's performance, which consequently determines the T_{CASE} of the processor at a given power level. Because the T_{CASE} of a processor is an important parameter in determining the long-term reliability of a processor, the FSC implemented in a system directly correlates to the processor's ability to meet the Thermal Profile. For this purpose, the parameter called $T_{CONTROL}$, as explained in the applicable datasheet, is to be used in FSC designs to ensure that the long-term reliability of the processor is met while keeping the system-level acoustic noise down. Figure 4-3 depicts the relationship between $T_{CONTROL}$ and FSC methodology.

Figure 4-3. $T_{CONTROL}$ and Fan Speed Control



The PECI temperature reading from the processor can be compared to this $T_{CONTROL}$ value. A fan speed control scheme can be implemented as described in Table 4-5 without compromising the long-term reliability of the processor.

Table 4-5. Fan Speed Control, $T_{CONTROL}$ and DTS Relationship

Condition	FSC Scheme
DTS ≤ $T_{CONTROL}$	FSC can adjust fan speed to maintain DTS ≤ $T_{CONTROL}$ (low acoustic region).
DTS >$T_{CONTROL}$	FSC should adjust fan speed to keep T_{CASE} at or below the Thermal Profile specification (increased acoustic region).

There are many different ways of implementing fan speed control, including FSC-based on processor ambient temperature, FSC based on processor Digital Thermal Sensor (DTS) temperature, or a combination of the two. If FSC is based only on the processor ambient temperature, low acoustic targets can be achieved under low ambient temperature conditions. However, the acoustics cannot be optimized based on the behavior of the processor temperature. If FSC is based only on the Digital Thermal Sensor, sustained temperatures above $T_{CONTROL}$ drive fans to maximum RPM. If FSC is based both on the ambient and Digital Thermal Sensor, ambient temperature can be used to scale the fan RPM controlled by the Digital Thermal Sensor. This would result in an optimal acoustic performance. Regardless of which scheme is employed, system designers must ensure that the Thermal Profile specification is met when the processor Digital Thermal Sensor temperature exceeds the T_{CONTOL} value for a given processor.

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5 Quality, Reliability and Ecological Requirements

5.1 Intel Reference Component Validation

Intel tests reference components both individually and as an assembly on mechanical test boards, and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows that a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

5.1.1 Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not been previously submitted to any reliability testing.

The test sequence should always start with a visual inspection after assembly and BIOS/Processor/memory test. The stress test should then be followed by a visual inspection and then by a BIOS/processor/memory test.

5.1.2 Post-Test Pass Criteria

The post-test pass criteria are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/processor/memory test.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.

5.1.3 Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

The testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard
- Processor and memory

- All enabling components, including socket and thermal solution parts

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors.

5.2 Heatsink Test Conditions

The Test Conditions provided in Table 5-1 address processor heatsink failure mechanisms only. Test Conditions, Qualification and Visual Criteria vary by customer; Table 5-1 reflects Intel requirements.

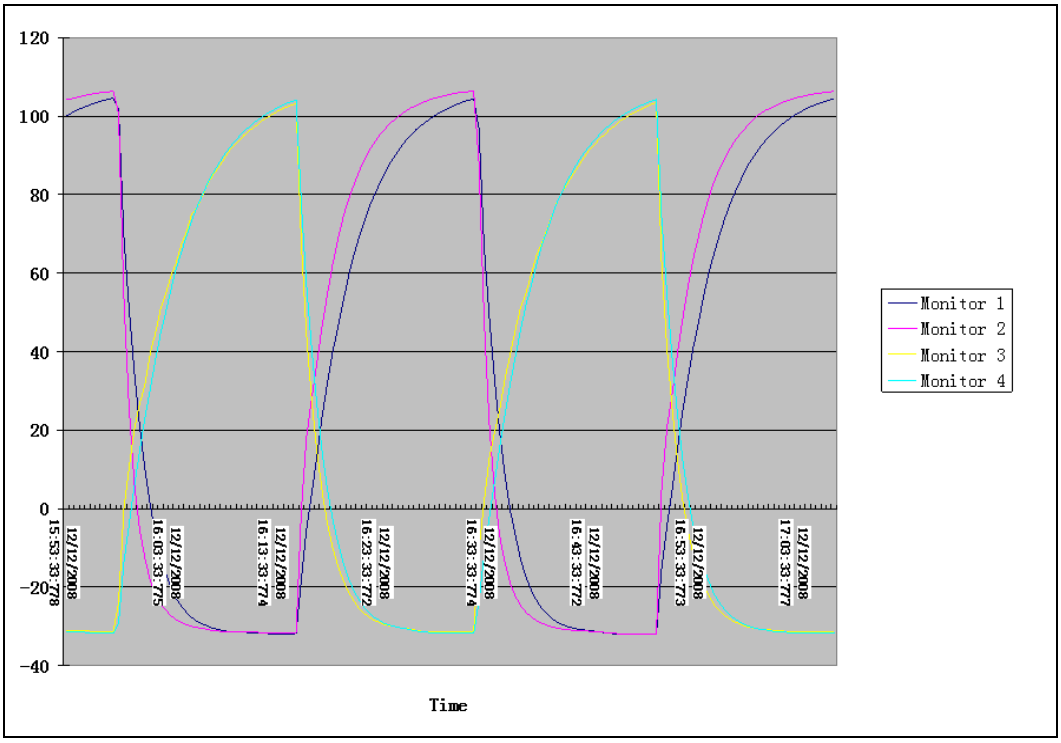
Table 5-1. Tower Heatsink Test Conditions and Qualification Criteria (Sheet 1 of 2)

Assessment	Test Condition	Qualification Criteria	Min Sample Size
1) Humidity	Non-operating, 500 hours, +85C and 85% R.H. 168 hours. 50% to 85% non-condensing at temperatures of 25C to 70C. Ramp rate Humidity ≤ 18% per hour; Temp. ≤ 23C per hour.	No visual defects. As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1 Pressure drop not to exceed value in Table 4-1.	12
2) Board-Level UnPackaged Shock	50G±10%; 170±10% in/sec; 3 drops per face, 6 faces.	No damage to heatsink base or pipe. No visual defects. As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1. Pressure drop not to exceed value in Table 4-1.	12
3) Board-Level UnPackaged Vibration	5 Hz @ 0.01 g2/Hz to 20 Hz @ 0.02 g2/Hz (slope up). 20 Hz to 500 Hz @ 0.02 g2/Hz (flat). Input acceleration is 3.13 g RMS. 10 minutes/axis for all 3 axes on all samples. Random control limit tolerance is ±3 dB.	No damage to heatsink base or pipe. No visual defects. As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1 Pressure drop not to exceed value in Table 4-1	12
4) First Article Inspection	Not Applicable	Meet all dimensions on 5 samples. Meet all CTF dimensions on 32 additional samples with 1.33 Cpk (mean + 4σ). If samples are soft-tooled, a hard tool plan must be defined.	37
5) Shipping Media: Packaged Shock	Drop height determined by weight and may vary by customer; Intel requirement in General Supplier Packaging Spec. 10 drops (6 sides, 3 edges, 1 corner)	No visual defects	1 box
6) Shipping Media: Packaged Vibration	0.015 g2/Hz @ 10-40 Hz, sloping to 0.0015 g2/Hz @ 500 Hz, 1.03 gRMS, 1 hour/axis for 3 axes	No visual defects	1 box
7) Thermal Performance	Using Tower heatsink and Tower airflow from Table 4-1 with Thermal Test Vehicle (TTV) set to 130-W output	As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1 Pressure drop not to exceed value in Table 4-1	30 heatsinks

Table 5-1. Tower Heatsink Test Conditions and Qualification Criteria (Sheet 2 of 2)

Assessment	Test Condition	Qualification Criteria	Min Sample Size
8) Bake	Non-Operating, 110C, 1000 hours Note: Increased duration recommended if using alternative, unqualified TIM.	No visual defects. As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1 Pressure drop not to exceed value in Table 4-1.	12
9) Thermal Cycling	Required for heatpipe designs. Temperature range at pipe in heatsink assembly: -25C to +100C for 500 cycles. Cycle time is 30 minutes per full cycle, divided into half cycle in hot zone and half in cold zone, with minimum 1-min soak at each temperature extreme for each cycle. See Figure 5-1 for example profile.	No visual defects. As verified in wind tunnel: Mean Ψ_{CA} + 3σ + offset not to exceed value in Table 4-1 Pressure drop not to exceed value in Table 4-1.	15
10) Heat Pipe Burst	Continuously raise heat pipe temperature and record the burst/leak temperatures of final formed/shaped/flattened heatpipe, 12 heatpipes minimum.	No failures at minimum of 300C @ 20 minutes	12 pipes
11) Heatsink Mass	Design Target < 500 g	Avg + 3 sigma heatsink mass < 600 g	12
12) Heatsink Load	Design Targets: 0.080" board = 54.3 ± 3.2lbf (F_{min} = 51.1 lbf) 0.118" board = 61.5 ± 4.1 lbf (F_{max} = 65.6lbf)	Heatsink Load Design Targets: 1.8mm (0.072") board > 40 lbf 3.0mm (0.118") board < 70 lbf	12

Figure 5-1. Example Thermal Cycle - Actual Profile Will Vary



5.3 LGA1567 Socket Reliability Testing and Results

Intel has conducted extensive reliability tests on the LGA1567 socket. Test conditions and results are provided in the LGA1567 Socket Validation Report. Contact Intel's enabled socket suppliers, listed in Table A.1, "Intel Enabling Component Suppliers" on page 43, for a copy of these reports.

5.4 Socket Durability Test

The socket must withstand 30 mating cycles. Test per EIA-364, test procedure 09. Measure contact resistance when mated in 1st and 30th cycles. The package must be removed at the end of each de-actuation cycle and reinserted into the socket.

5.5 Ecological Requirement

General requirements: Materials used in this product must comply with customers' Environmental Product Content Specification. The Intel specification is available at:

http://supplier2.intel.com/EHS/Environmental_Product_Content_Specification_9-16-03.doc

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance.

Any plastic component exceeding 25 grams must be recyclable per the European Blue Angel recycling standards.

Particular requirements: Cadmium shall not be used in painting or plating. No Quaternary salt electrolytic capacitors shall be used. Examples of prohibited caps are United Chemi-Con type: LXF, LXY, LXZ. No brominated plastics shall be used. Also, plastics heavier then 25 g must be labeled per ISO 10469 and may not contain halogenated flame retardant compounds.

Chemical Restrictions:

All components (for example: socket, TIM, heatsink) must be 'halogen-free'; that is, they are assembled without the intentional use of halogen in the raw materials and these elements are not intentionally present in the end product.

- IEC 61249-2-21
  - — 900 ppm maximum chlorine
  - — 900 ppm maximum bromine
  - — 1500 ppm maximum total halogens
- IPC-4101B
  - — 900 ppm maximum chlorine
  - — 900 ppm maximum bromine
  - — 1500 ppm maximum total halogens

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A Supplier Information

A.1 Intel Enabling Component Suppliers

Customers can purchase Intel reference thermal solution components from the suppliers listed in Table A-1.

See Appendix D for drawings.

Table A-1. Suppliers for the Processor Heatsink

Component	Description / Part Number	Development Suppliers	Supplier Contact Info
Thermal Interface Material	PCM45F / 95367	Honeywell	Judy Oles (Customer Service) Judy.Oles@Honeywell.com 509-252-8605 Andrew S.K. Ho (APAC) andrew.ho@honeywell.com (852) 9095-4593 Andy Delano (Technical) Andrew.Delano@Honeywell.com 509-252-2224
Processor Heatsink - HL-ILM implementation	Tower Heatsink (with PCM45F) Intel P/N: E45309-007 CCI P/N: 0008053206	Chaun-Choung Technology Corp. (CCI)	Monica Chih 12F, No.123-1, Hsing-De Rd., Sanchung, Taipei, Taiwan, R.O.C. Tel. +886 (2) 2995-2666 x1131 Fax: +886 (2) 2995-8258 monica_chih@ccic.com.tw Sean Wu sean_wu@ccic.com.tw (408) 768-7629

The Intel reference thermal solution has been validated per the criteria outlined in Chapter 5.

Customers can purchase the LGA1567 Socket and ILM components from suppliers listed in Table A-2.

See Appendix B for LGA1567 Socket drawings. See Appendix C for ILM drawings.

Table A-2. LGA1567 Socket and ILM Part Number and Supplier Contact Information (Sheet 1 of 2)

Item	Intel	Foxconn	Lotes	Tyco
High Load ILM (HL-ILM)	E42426-001	PT44L11-4301	ACA-ZIF-084-K01	
High Load ILM Cover (HL-ILM) only	G12449-001	012-1000-5838	ACA-ZIF-103-P01	
High Load ILM Assembly (HL-ILM) (includes E42426-001 and G12449-001)	G14941-001	PT44L21-4311	ACA-ZIF-126-Y01	

Table A-2. LGA1567 Socket and ILM Part Number and Supplier Contact Information (Sheet 2 of 2)

Item	Intel	Foxconn	Lotes	Tyco
Low Profile ILM Assembly (LP-ILM)	E56700-001	PT44L12-4301		
Back Plate	E42477-001	PT44P11-4301	DCA-HSK-149-K01	
LGA1567 Socket	E34291-001	PE156727-5241-01F		2040636-1
Contact Info		Julia Jiang juliaj@usa.foxconn.com Tel. (408) 919-6178 1688 Richard Ave. Santa Clara, CA 95050 USA	Cathy Yang cathy@lotes.com.cn Tel. 86-20-84686519 No.15, Wusyun Street Anle District Keelung City, 20446 Taiwan	Gretchen Troutman gltroutm@tycoelectronics.com Tel. 717-986-5241 PO Box 3608 Harrisburg, PA 17105-3608 USA

Table A-3. Alternate Suppliers with Thermal Solutions Designed for the Intel Xeon Processor 7500 Series

Component	Description / Part Number	Development Suppliers	Supplier Contact Info
Processor Heatsink - LP-ILM implementation	1.5U Aluminum embedded heatpipe Part number: 321879 *(Verified to meet load targets in Table 4-1)*	Aavid Thermalloy	Chris Chapman (USA) 70 Commercial St. Suite 200 Concord, NH 03301 603 223-1728 chapman@aavid.com George Lee (Taiwan) 14F-4, No 79, Hsin Tai Wu Rd., Sec, 1 Hsichin, Taipei Hsien, Taiwan ROC +886 (2) 2698-9888 ext. 603 George.lee@aavid.com.tw
Processor Heatsink - HL-ILM implementation	1U Copper skived Part number Q129 *(Verified to meet load targets in Table 4-1 and thermal targets in Table 4-3)*	Dynatron Corporation (Top Motor/Dynaeon)	Ian Lee 41458 Christy Street Fremont, CA 94538 510-498-8888 x137 ian@dynatron-corp.com Lang Pai 510-498-8888 x138 Lang@dynatron-corp.com
Processor Heatsink - HL-ILM implementation	Tower Heatsink 050234 Rev05 *(Verified to meet load targets in Table 4-1 and thermal targets in Table 4-3)*	Aavid Thermalloy	Chris Chapman (USA) 70 Commercial St. Suite 200 Concord, NH 03301 603 223-1728 chapman@aavid.com George Lee (Taiwan) 14F-4, No 79, Hsin Tai Wu Rd., Sec, 1 Hsichin, Taipei Hsien, Taiwan ROC +886 (2) 2698-9888 ext. 603 George.lee@aavid.com.tw

The Alternate Processor Heatsink Solutions listed in Table A-3 have been verified to meet Intel's requirements except as noted. Customers must evaluate performance against their own product requirements.

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B LGA 1567 Socket Mechanical Drawings

Table B-1 lists the mechanical drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
“LGA 1567 Socket Mechanical Drawing – Sheet 1 of 4”	Figure B-1
“LGA 1567 Socket Mechanical Drawing – Sheet 2 of 4”	Figure B-2
“LGA 1567 Socket Mechanical Drawing – Sheet 3 of 4”	Figure B-3
“LGA 1567 Socket Mechanical Drawing – Sheet 4 of 4”	Figure B-4

Figure B-1. LGA 1567 Socket Mechanical Drawing – Sheet 1 of 4

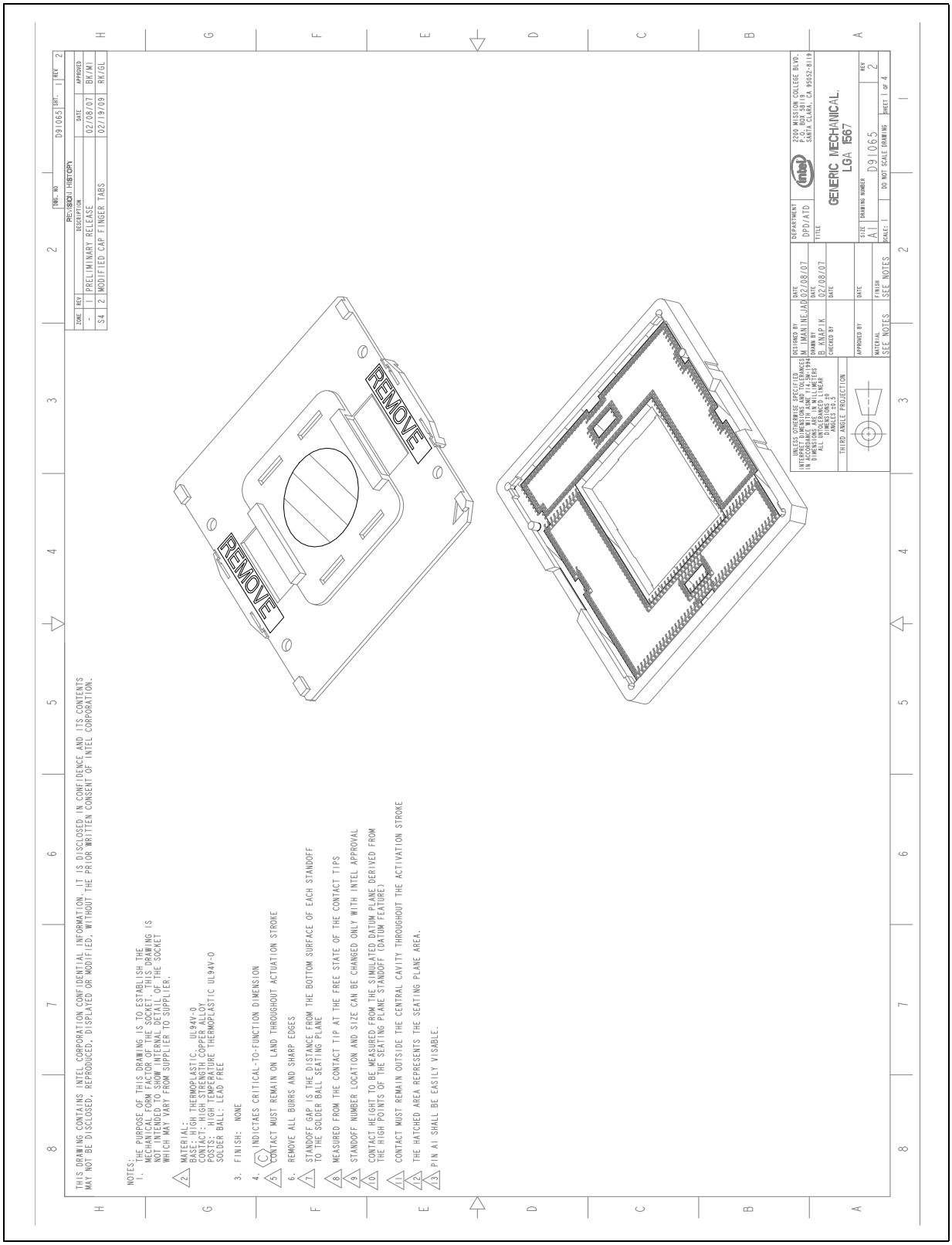


Figure B-2. LGA 1567 Socket Mechanical Drawing – Sheet 2 of 4

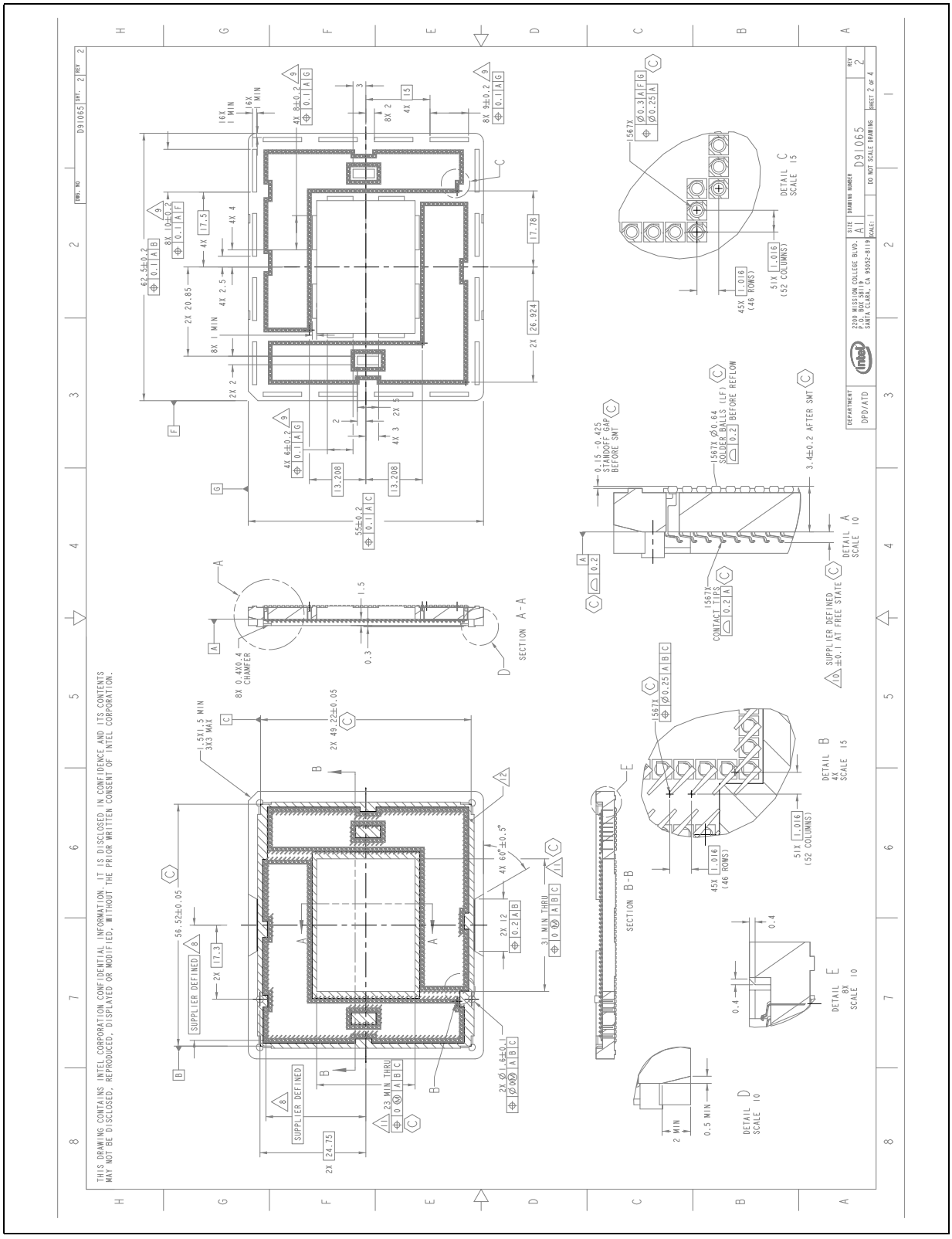


Figure B-3. LGA 1567 Socket Mechanical Drawing – Sheet 3 of 4

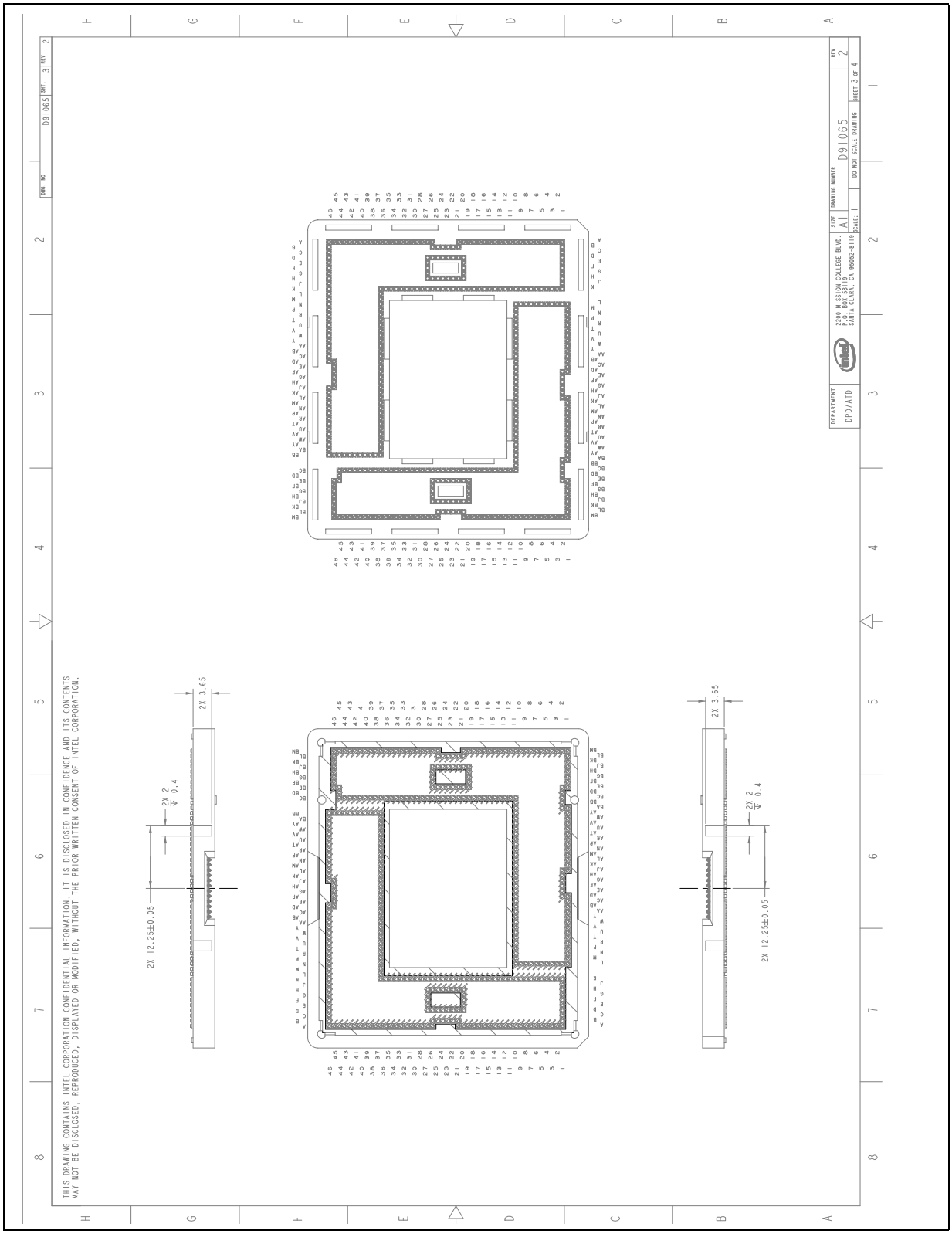
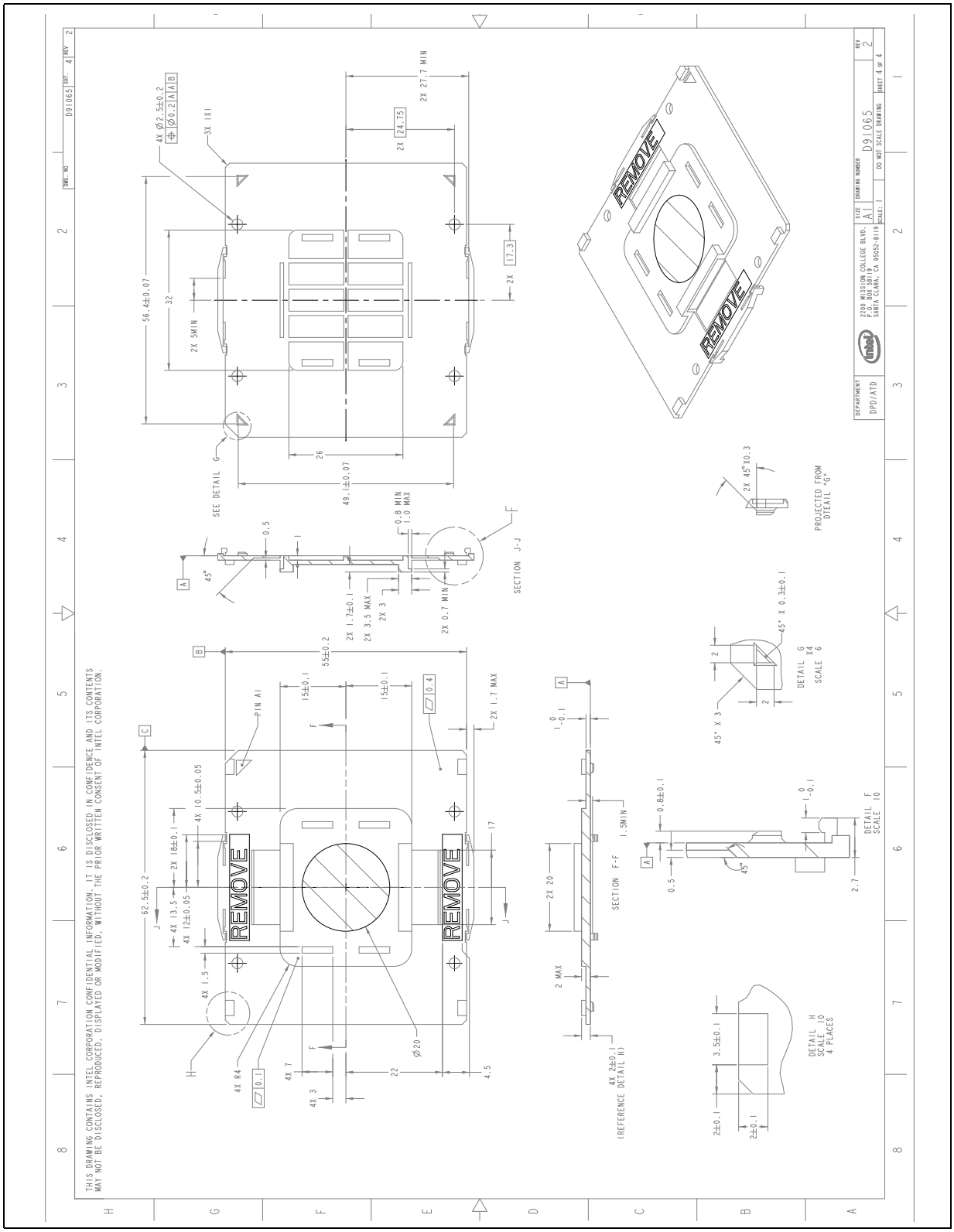


Figure B-4. LGA 1567 Socket Mechanical Drawing – Sheet 4 of 4



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C Independent Loading Assembly (ILM) Drawings and Backplate Assembly Drawings

Table C-1 lists the mechanical drawings included in this appendix.

Table C-1. Mechanical Drawing List

Drawing Description	Figure Number
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 1 of 7”	Figure C-1
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 2 of 7”	Figure C-2
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 3 of 7”	Figure C-3
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 4 of 7”	Figure C-4
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 5 of 7”	Figure C-5
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 6 of 7”	Figure C-6
“High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 7 of 7”	Figure C-7
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 1 of 8”	Figure C-8
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 2 of 8”	Figure C-9
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 3 of 8”	Figure C-10
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 4 of 8”	Figure C-11
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 5 of 8”	Figure C-12
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 6 of 8”	Figure C-13
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 7 of 8”	Figure C-14
“Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 8 of 8”	Figure C-15
“Backplate Assembly Drawing – Sheet 1 of 5”	Figure C-16
“Backplate Assembly Drawing – Sheet 2 of 5”	Figure C-17
“Backplate Assembly Drawing – Sheet 3 of 5”	Figure C-18
“Backplate Assembly Drawing – Sheet 4 of 5”	Figure C-19
“Backplate Assembly Drawing – Sheet 5 of 5”	Figure C-20

Figure C-1. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 1 of 7

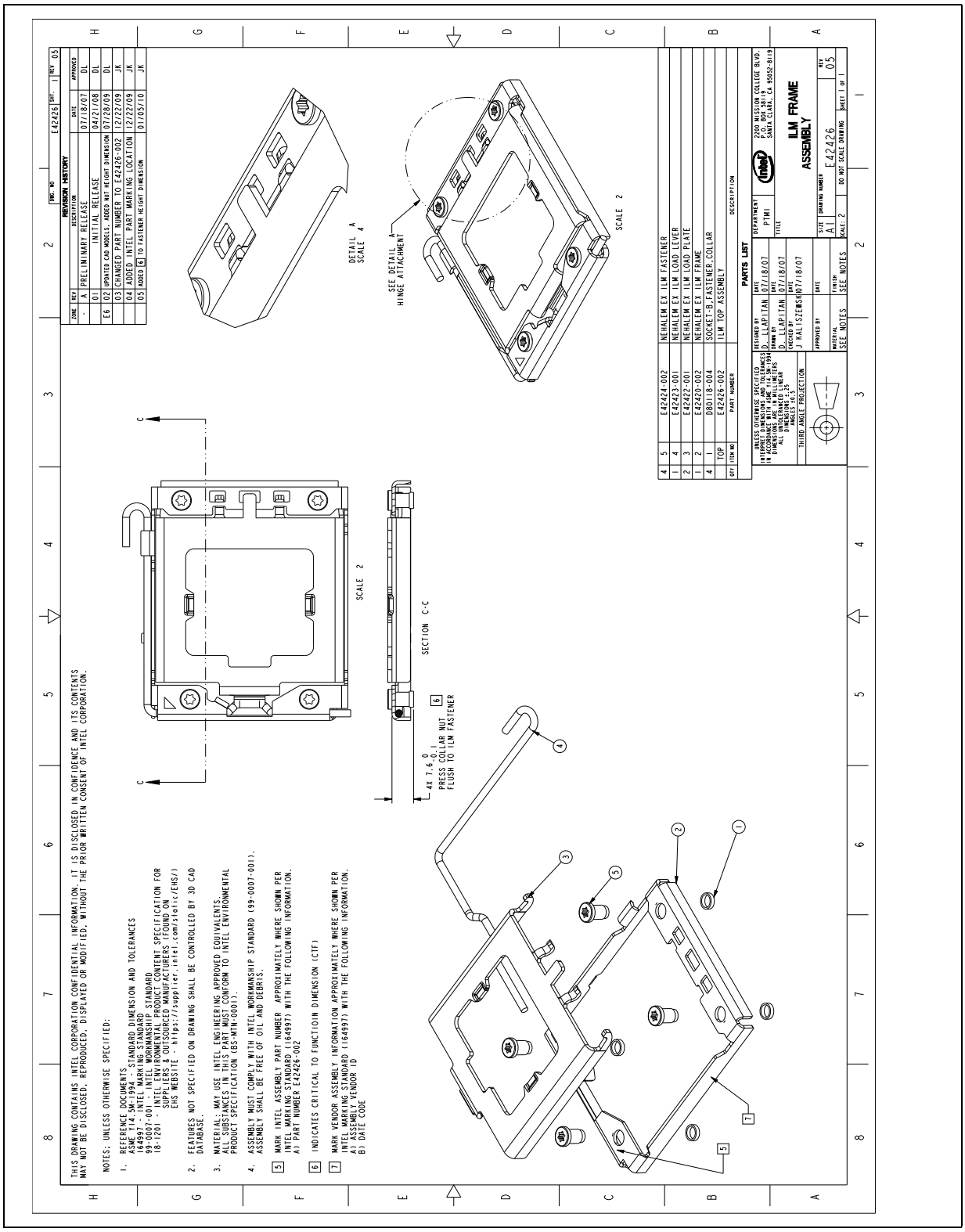

Figure C-2. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 2 of 7

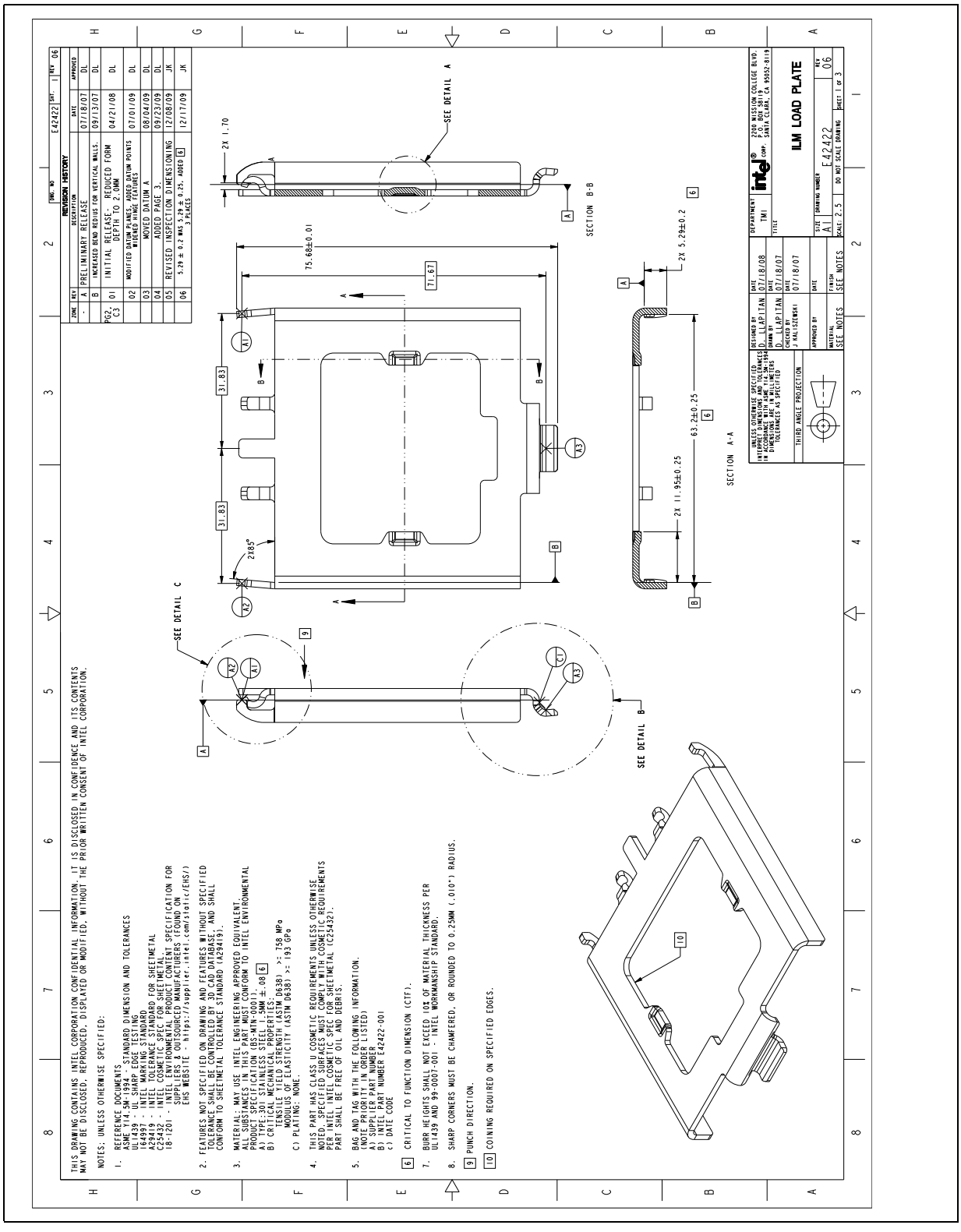

Figure C-3. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 3 of 7

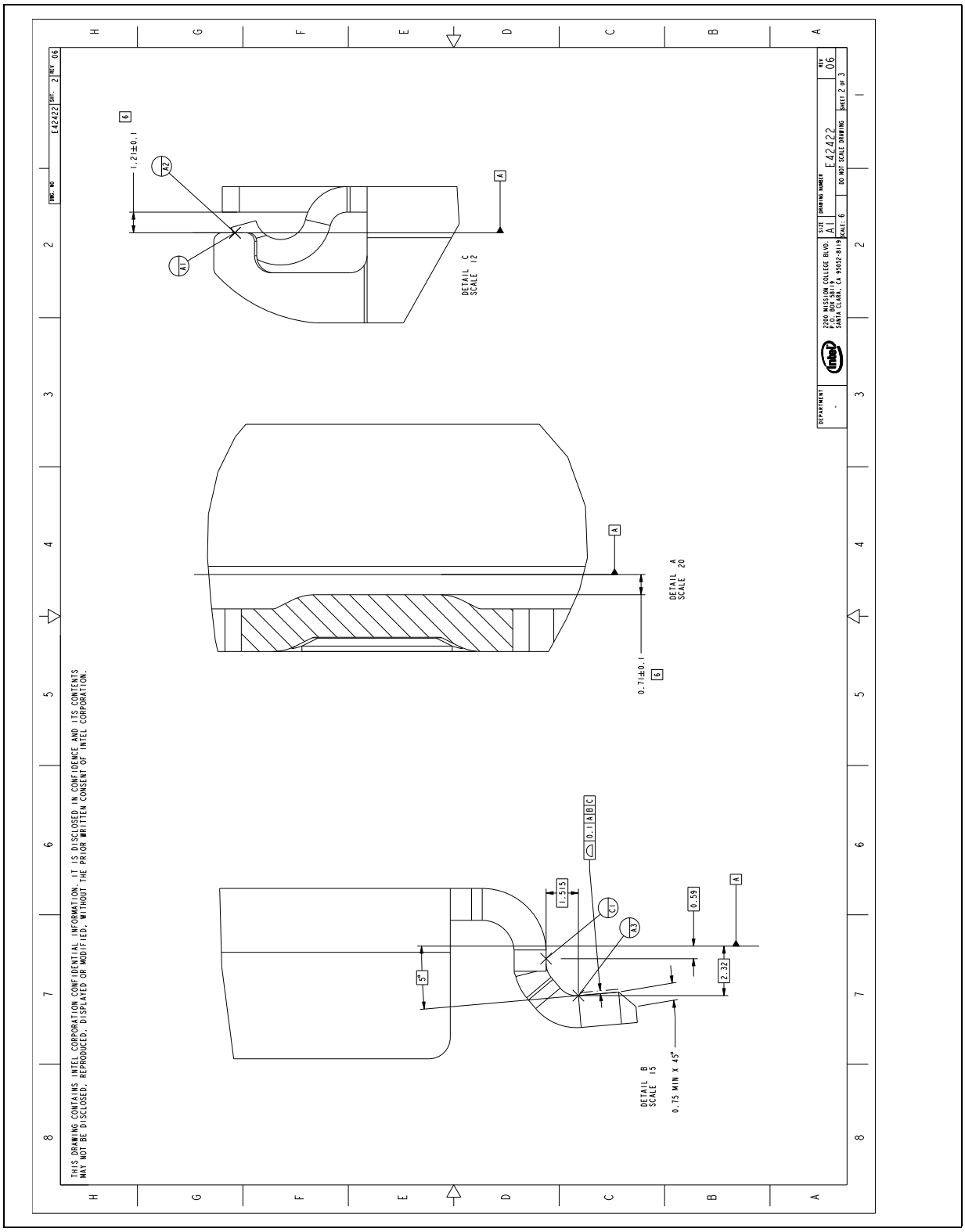

Figure C-4. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 4 of 7

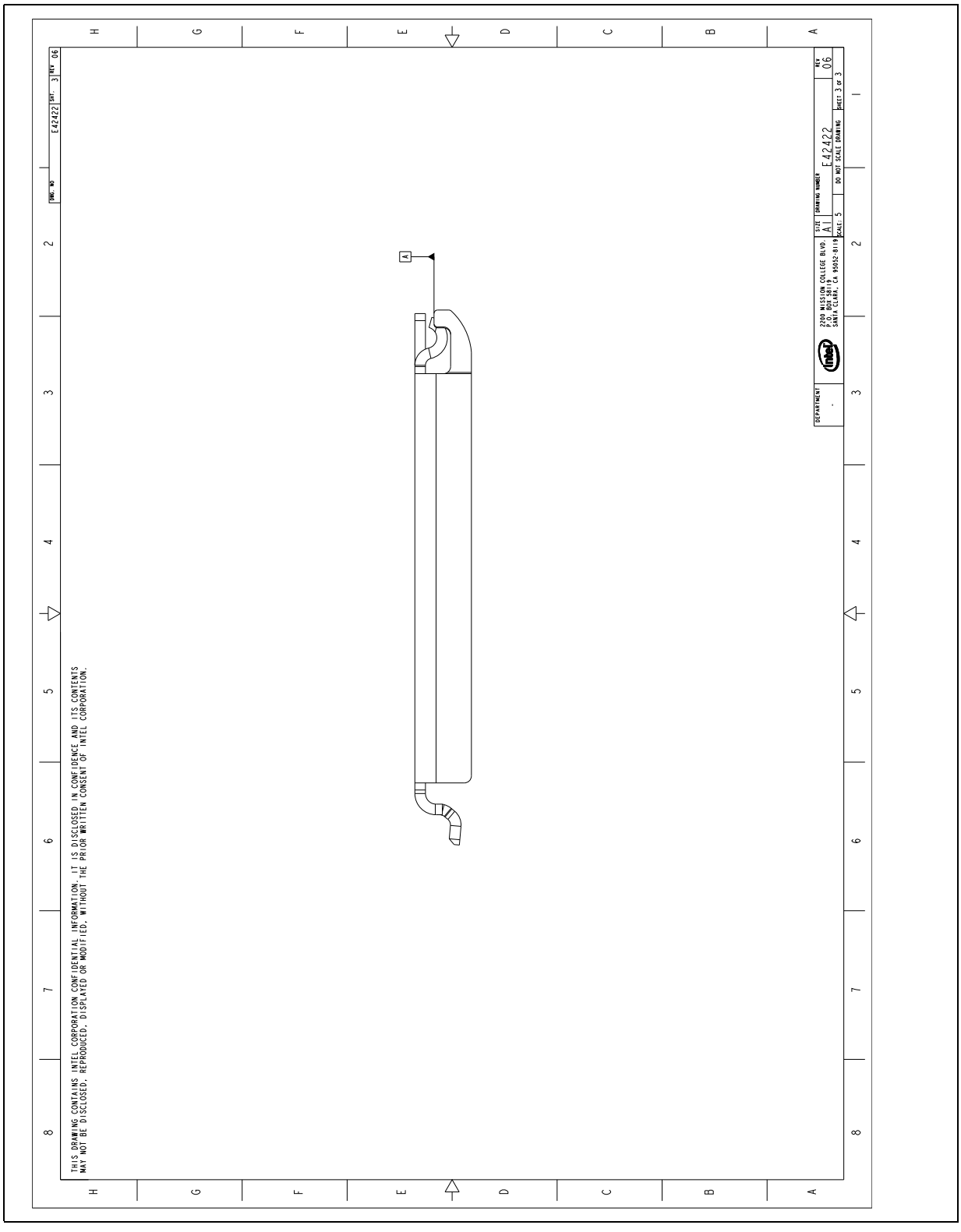

Figure C-5. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 5 of 7

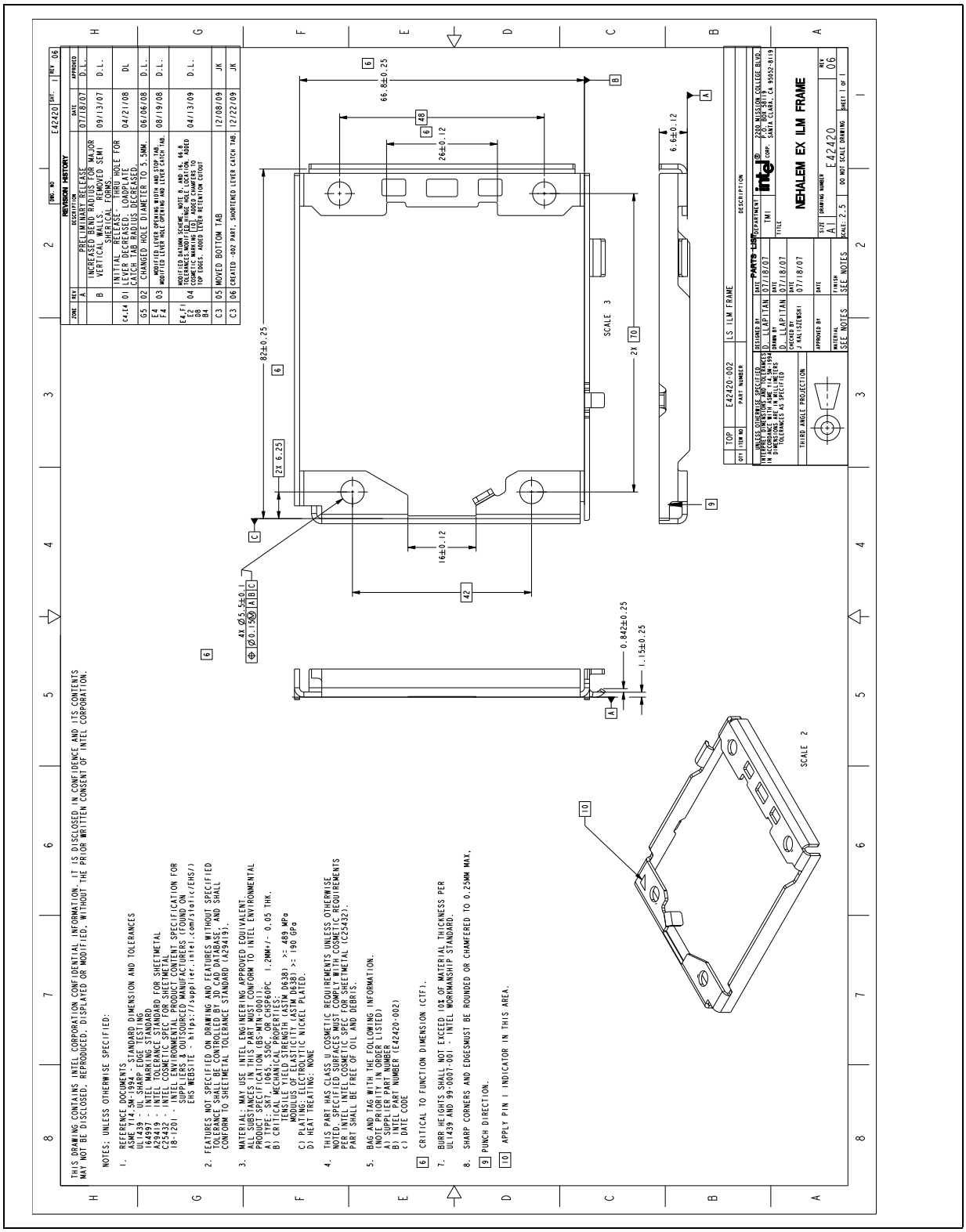

Figure C-6. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 6 of 7

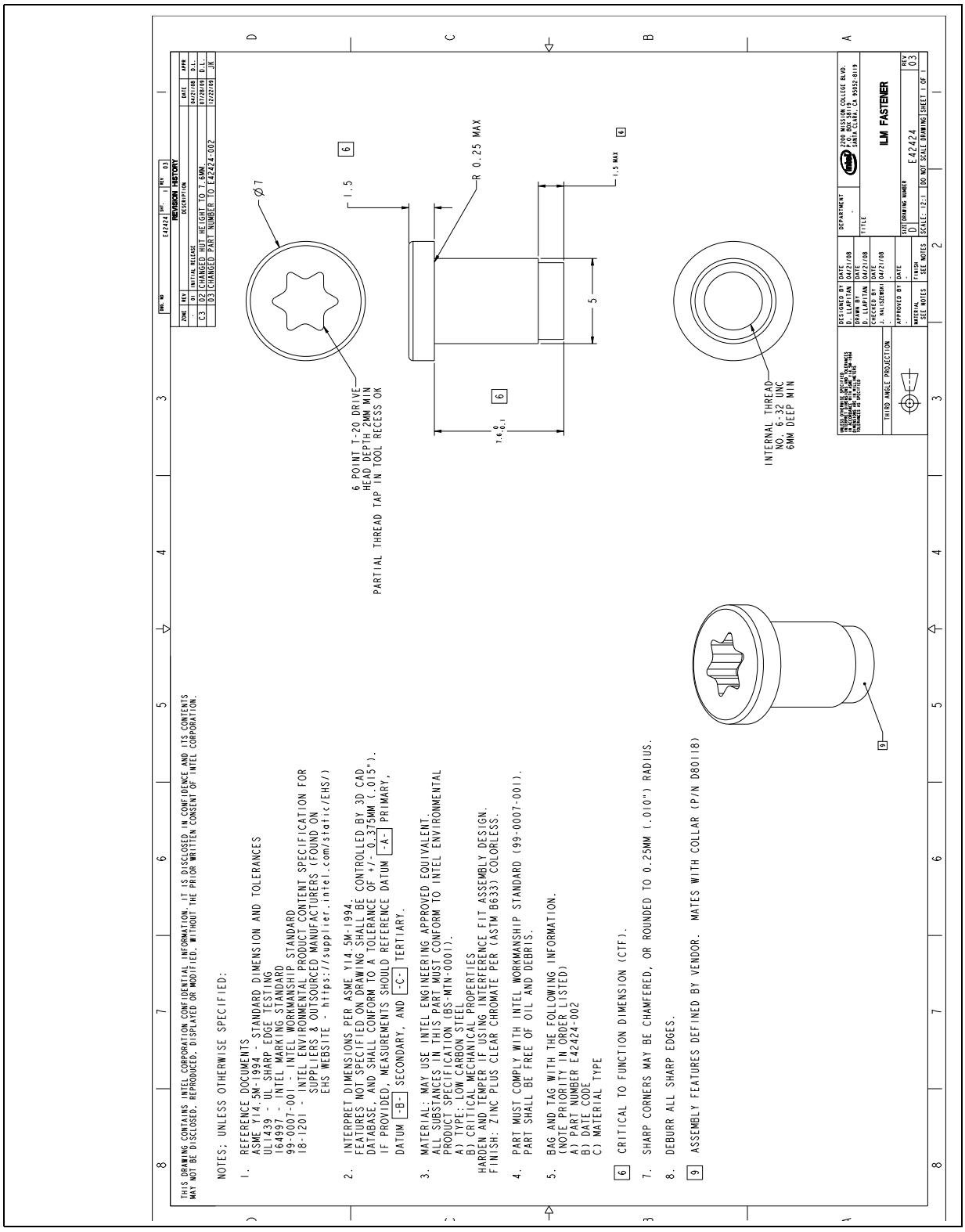

Figure C-7. High-Load Independent Loading Assembly (HL-ILM) Mechanical Drawing – Sheet 7 of 7

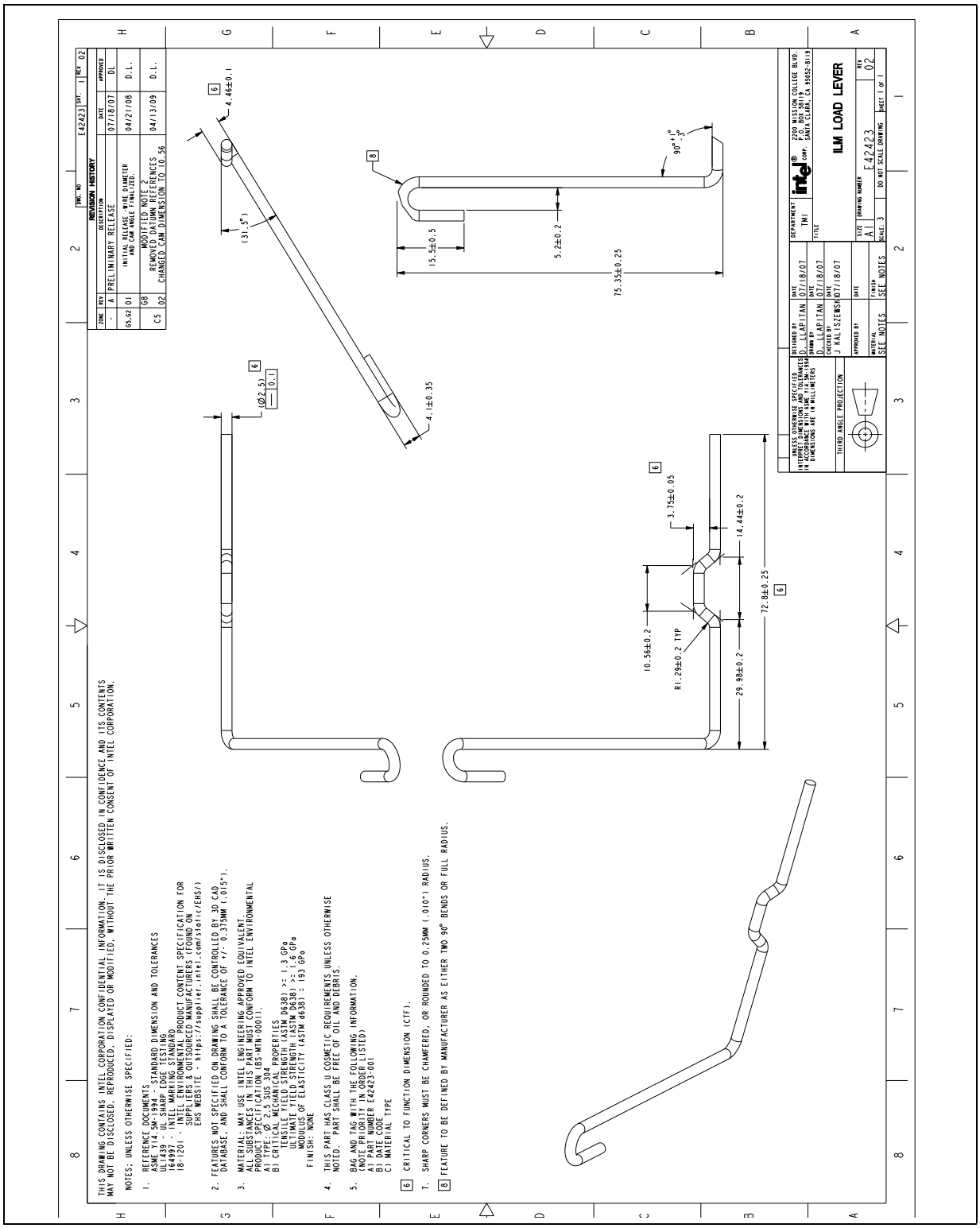

Figure C-8. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 1 of 8

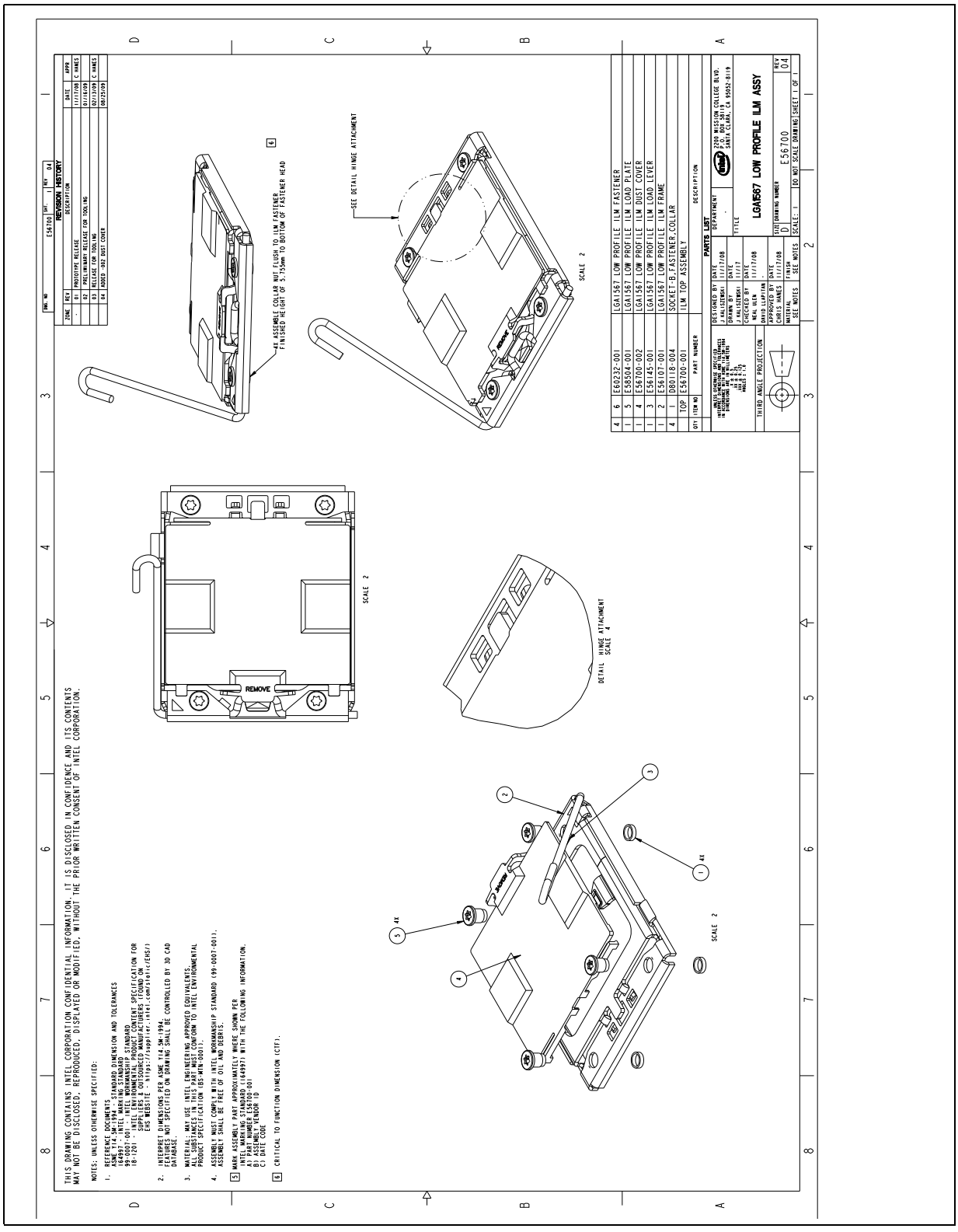

Figure C-9. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 2 of 8

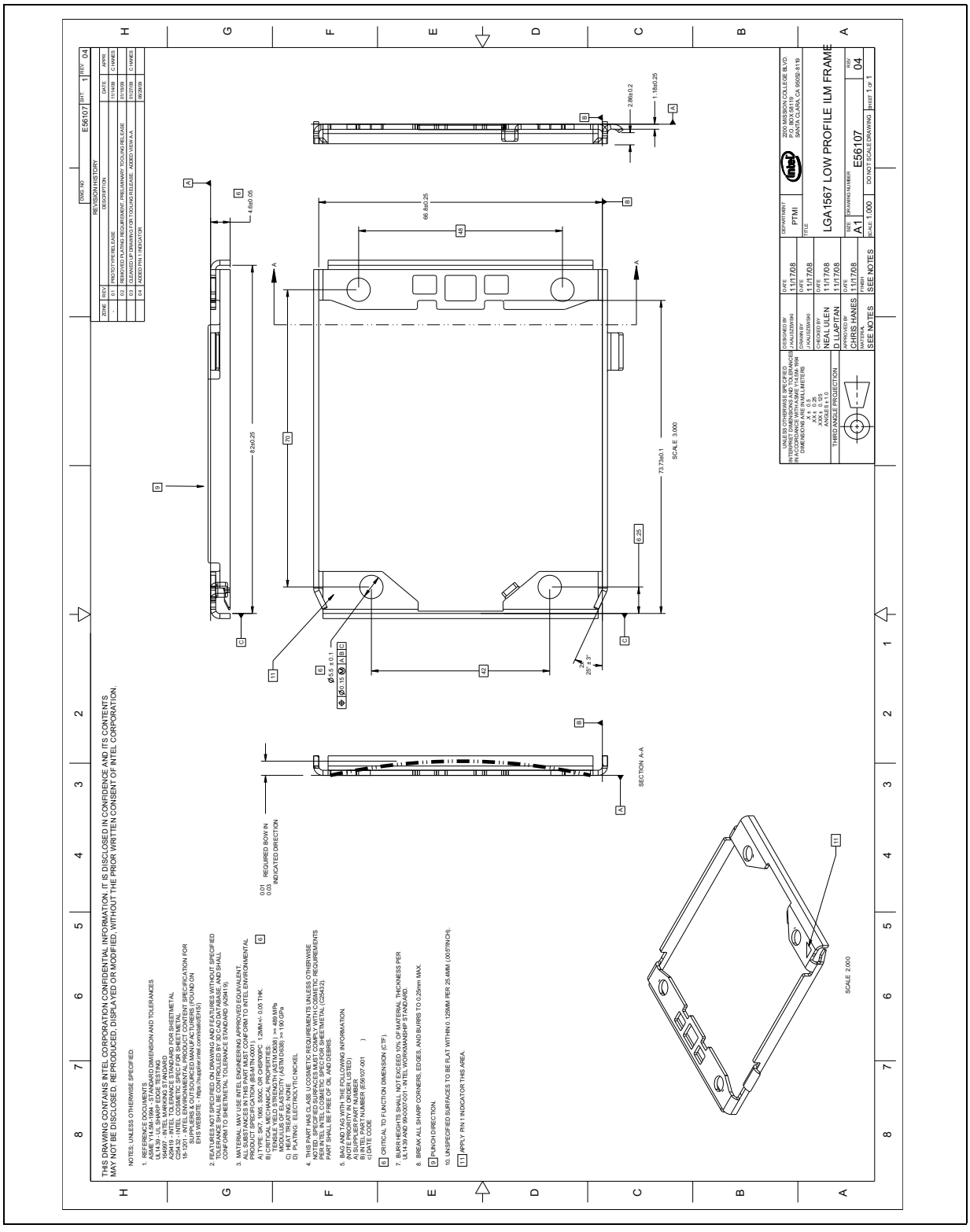

Figure C-10. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 3 of 8

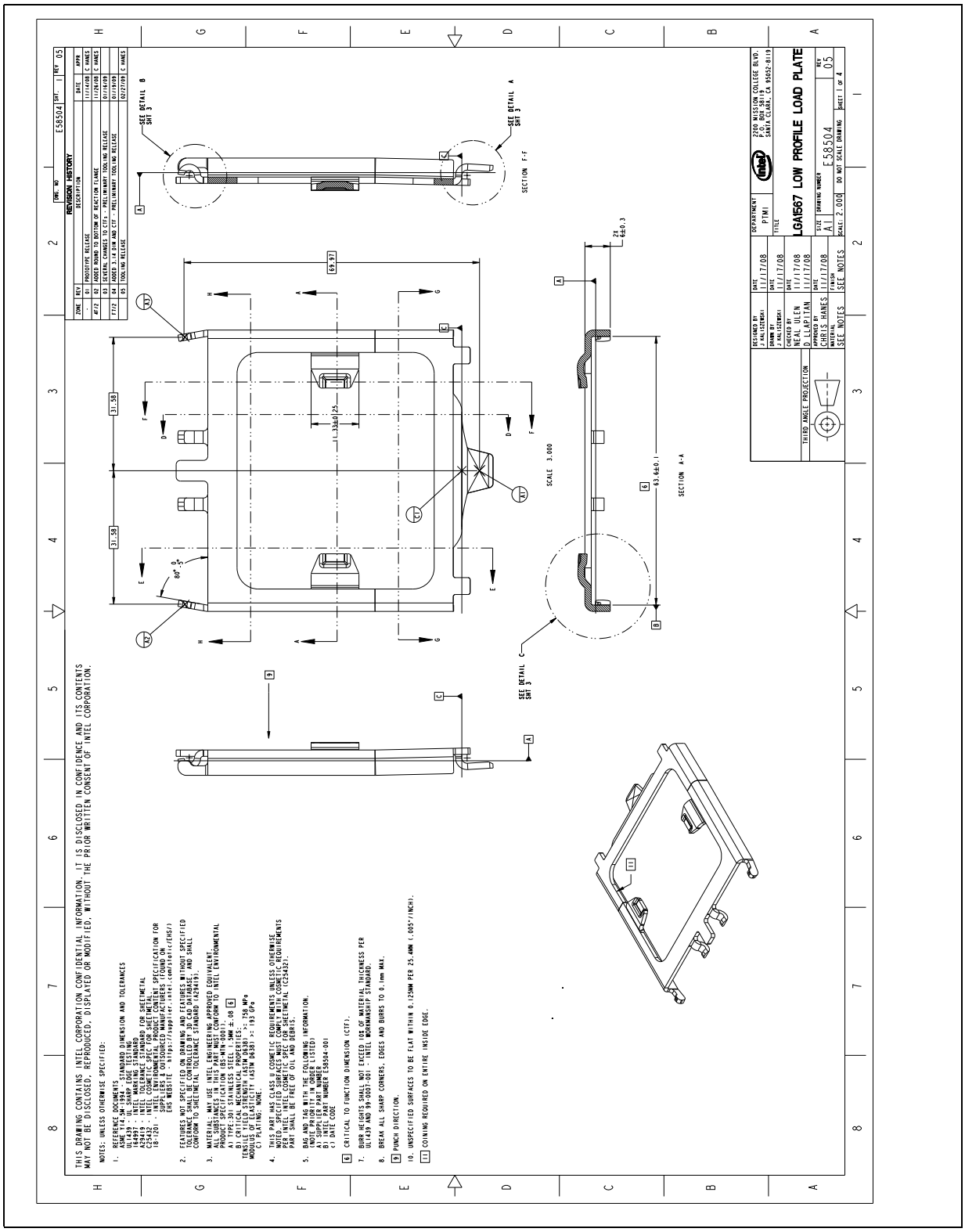

Figure C-11. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 4 of 8

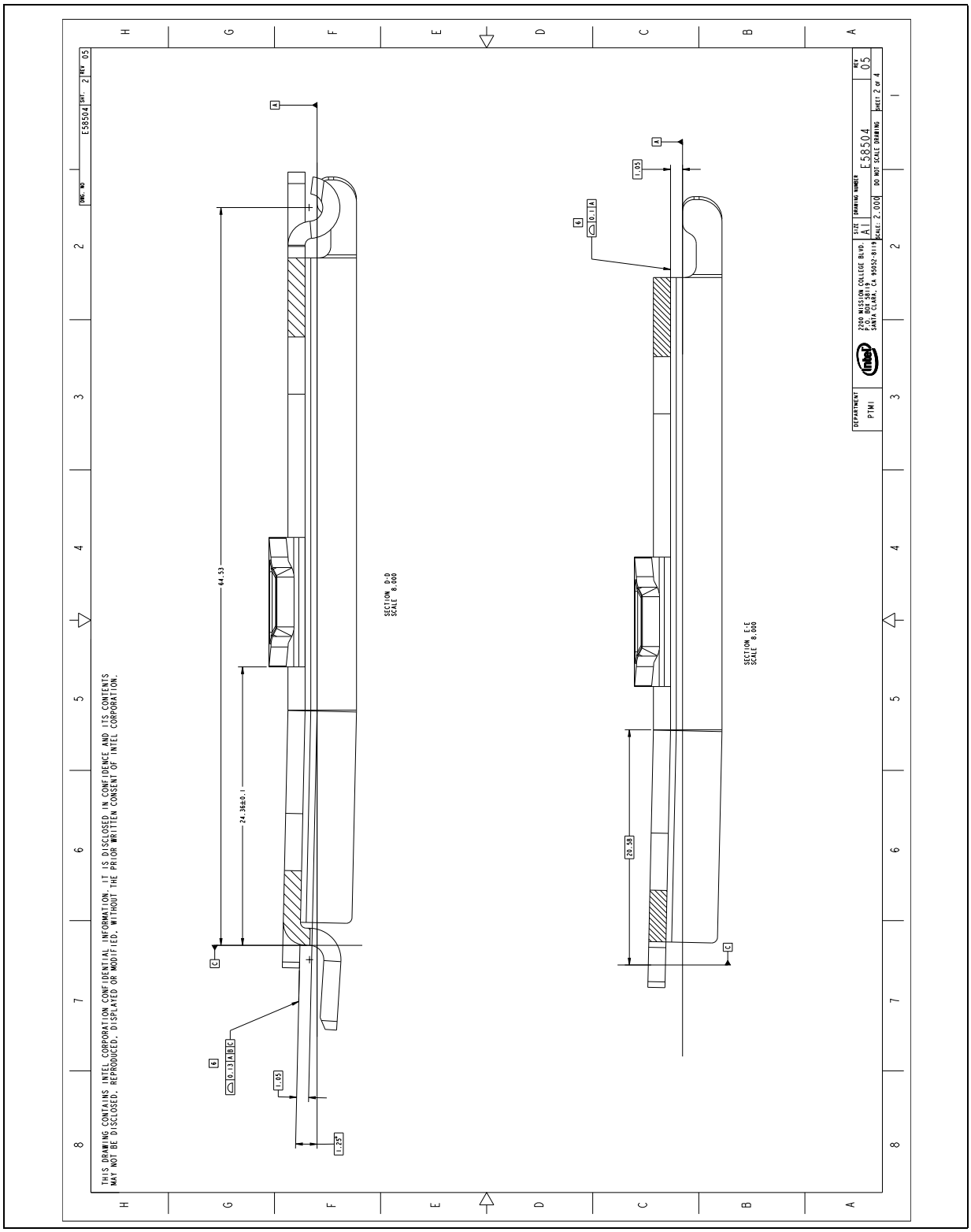

Figure C-12. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 5 of 8

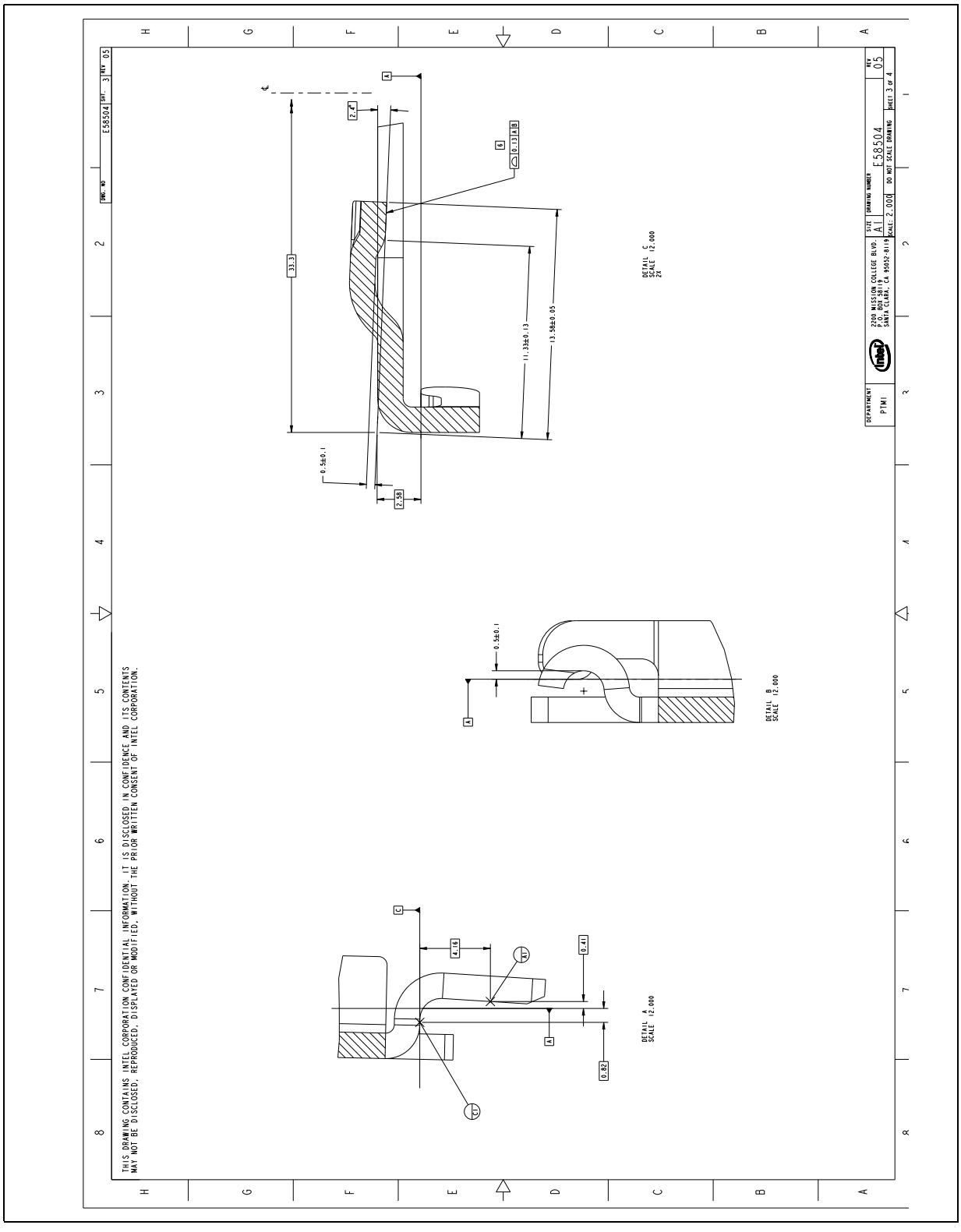

Figure C-13. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 6 of 8

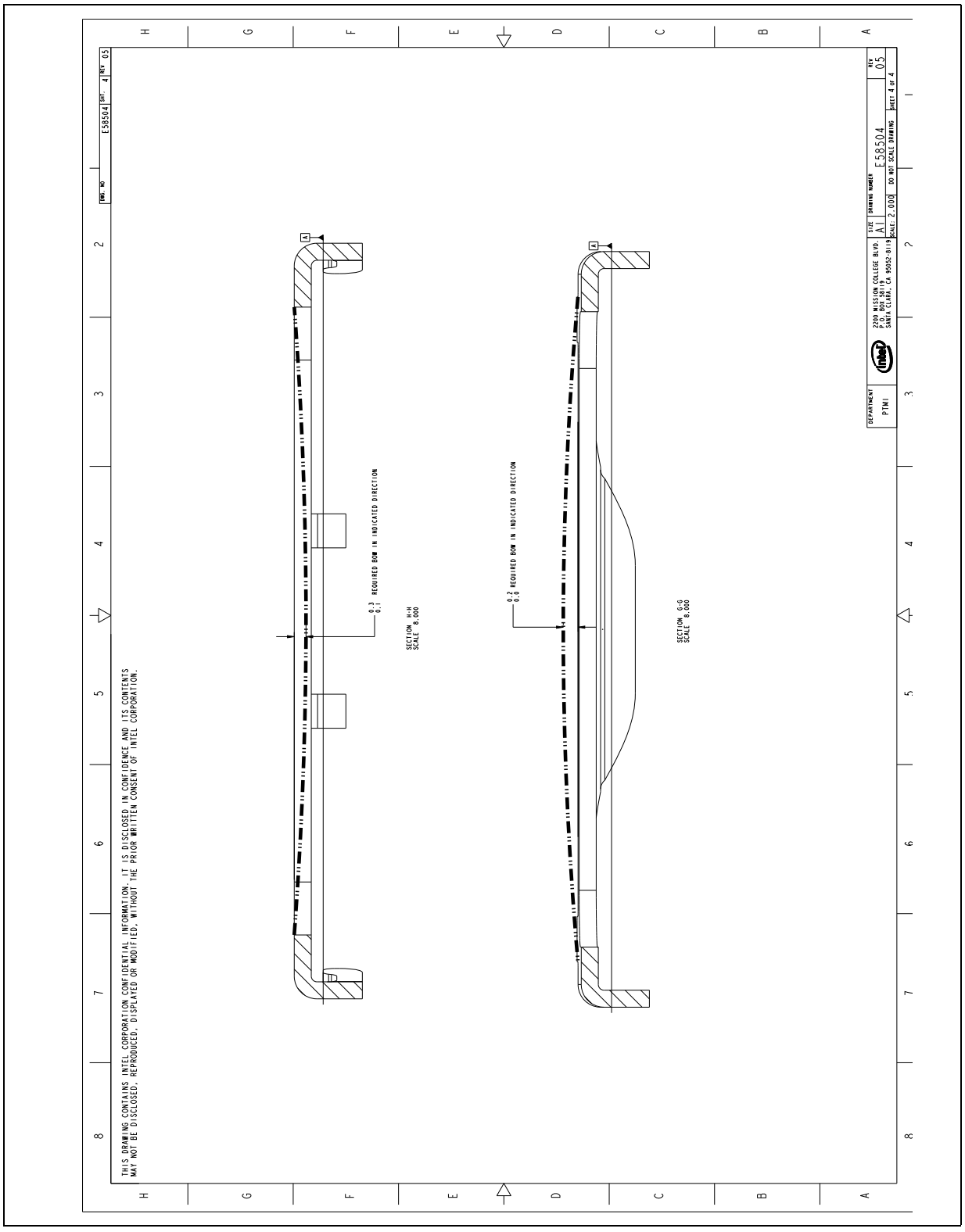

Figure C-14. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 7 of 8

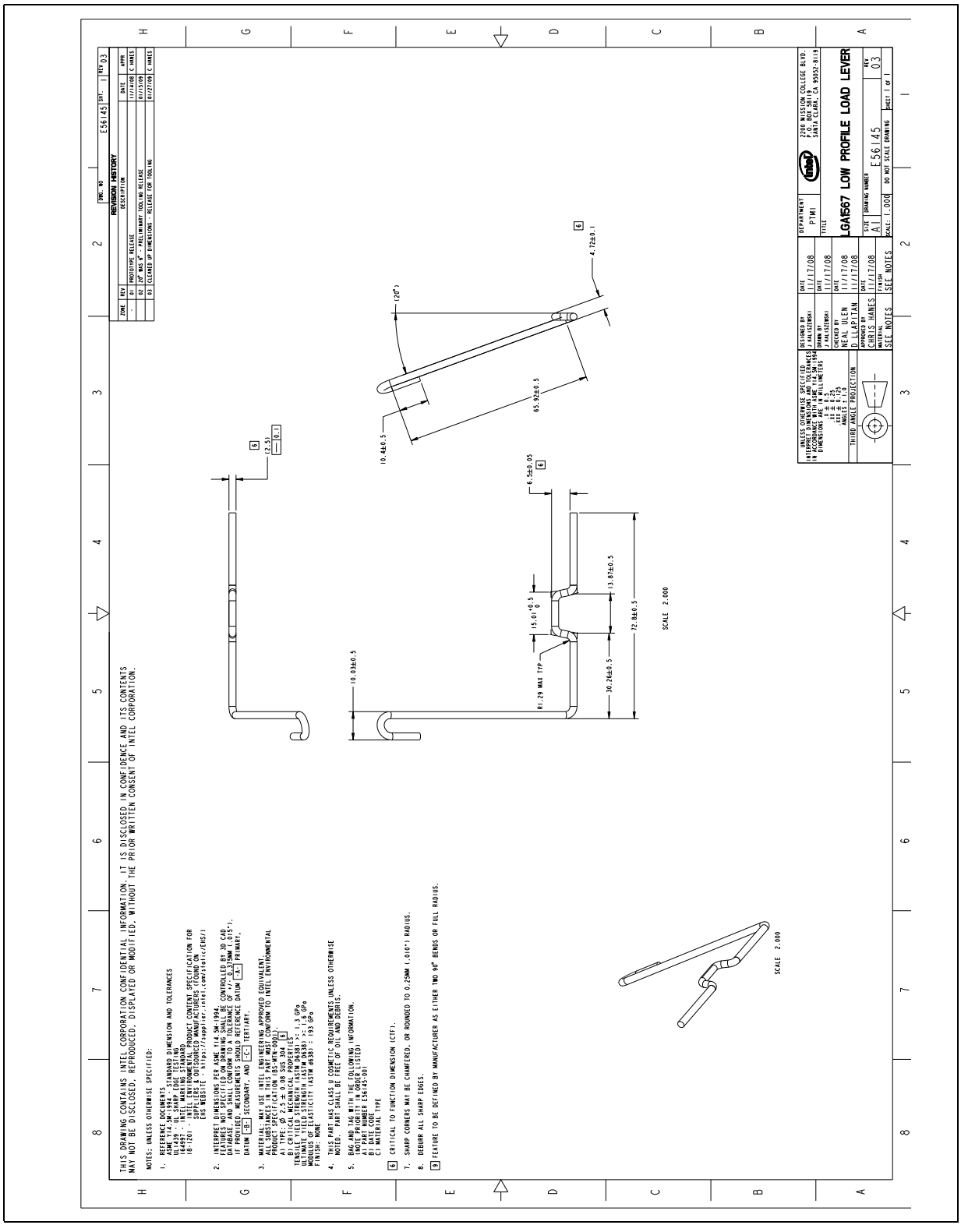

Figure C-15. Low-Profile Independent Loading Assembly (LP-ILM) Mechanical Drawing – Sheet 8 of 8

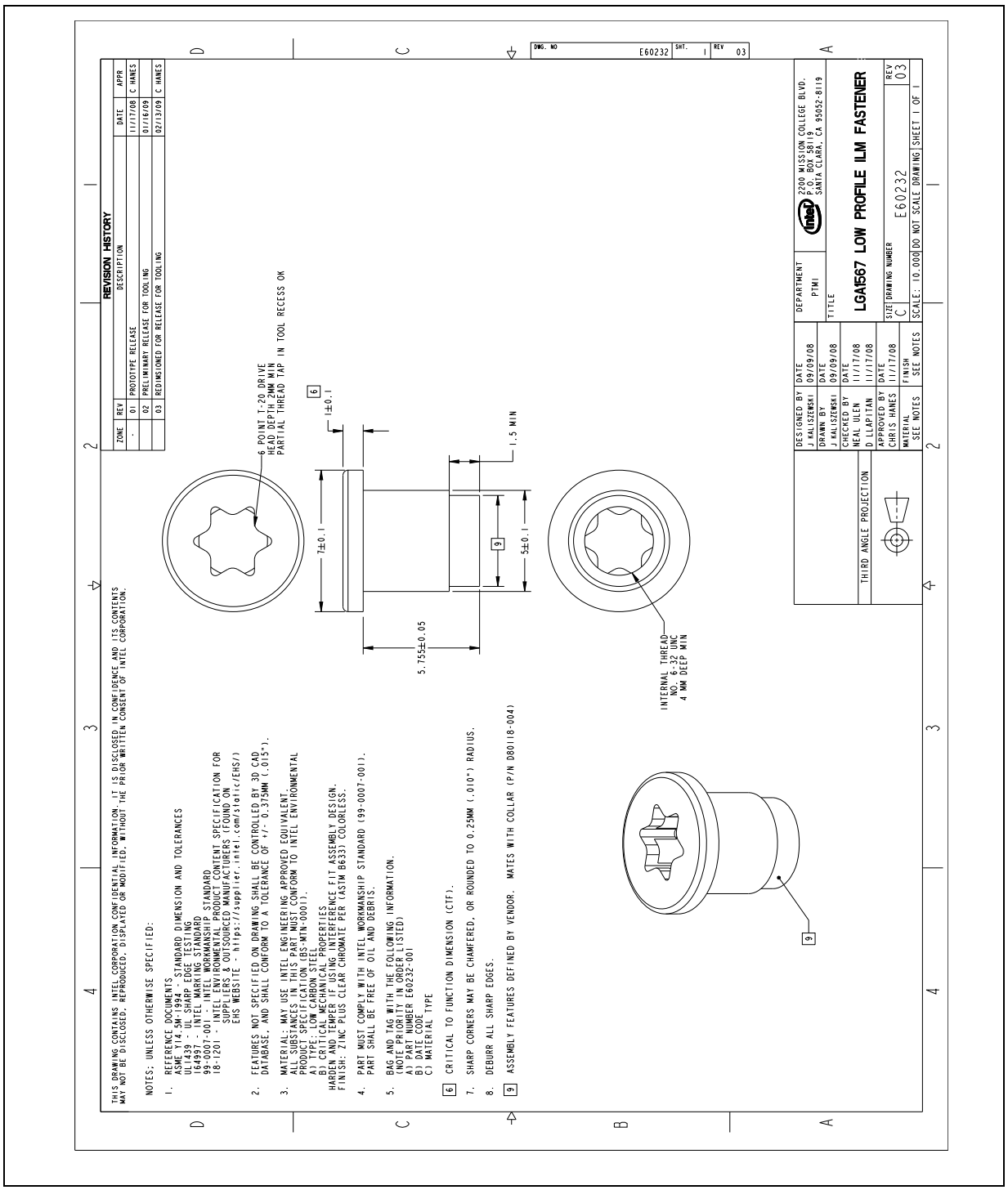

Figure C-16. Backplate Assembly Drawing – Sheet 1 of 5

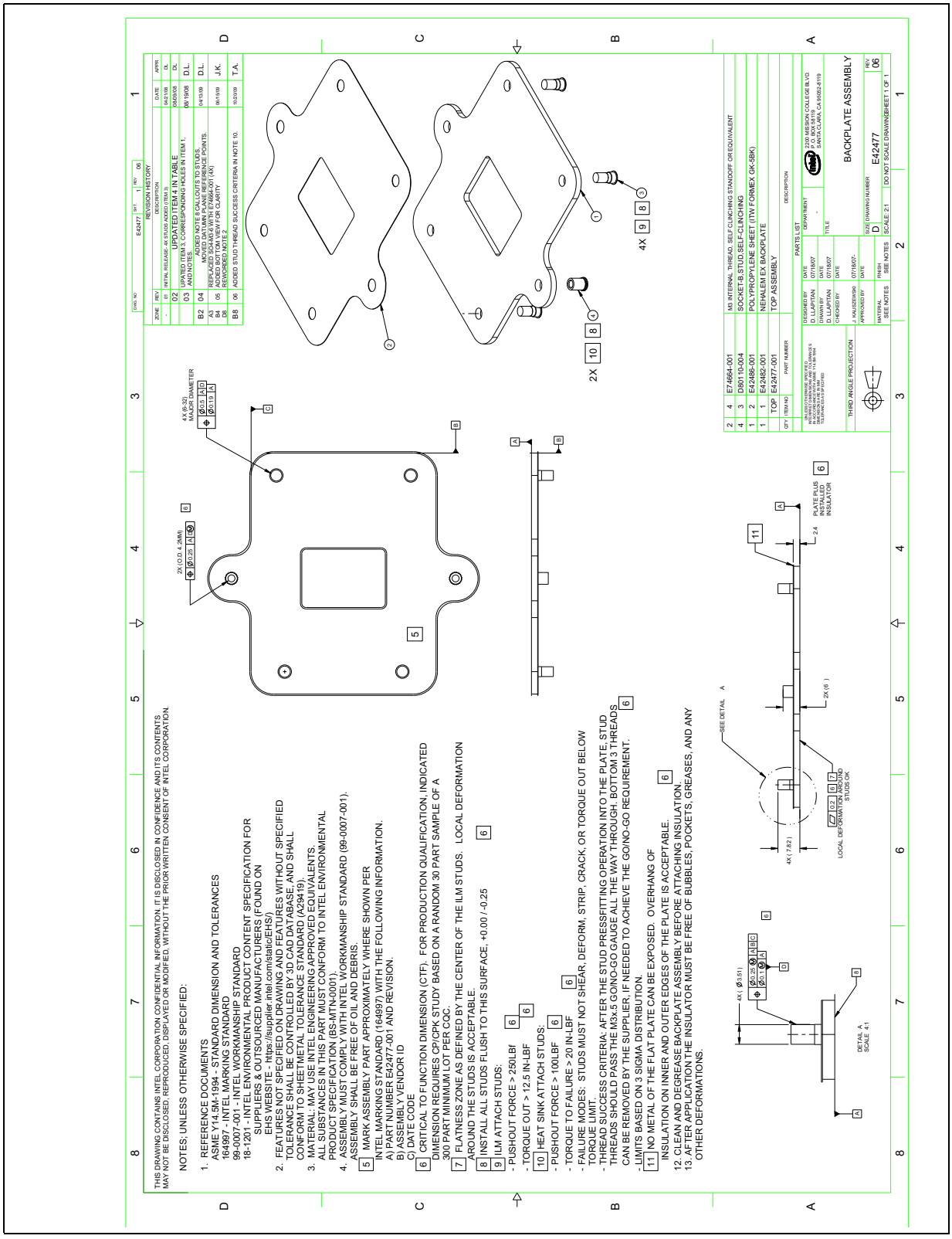

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Figure C-17. Backplate Assembly Drawing – Sheet 2 of 5

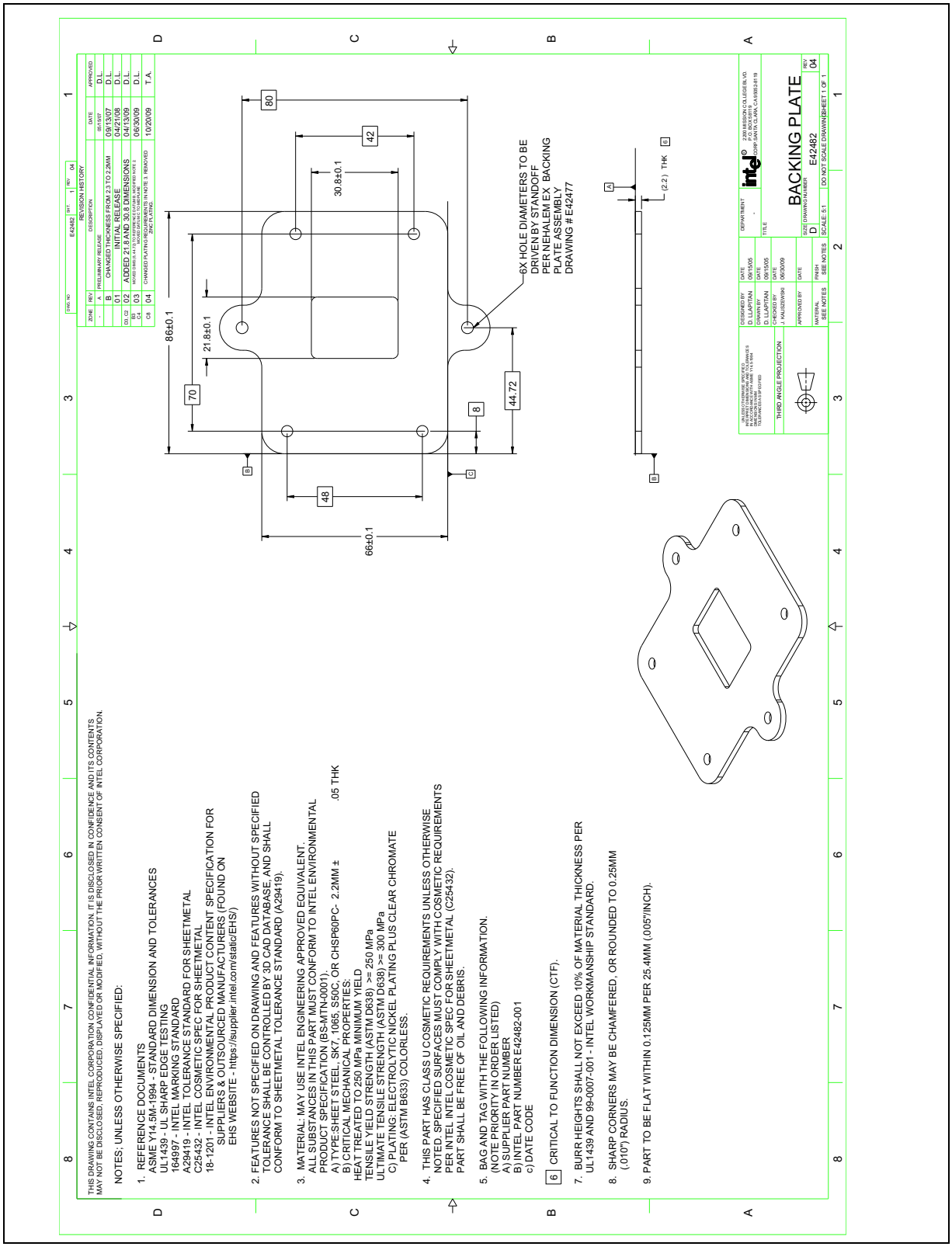


Figure C-18. Backplate Assembly Drawing – Sheet 3 of 5

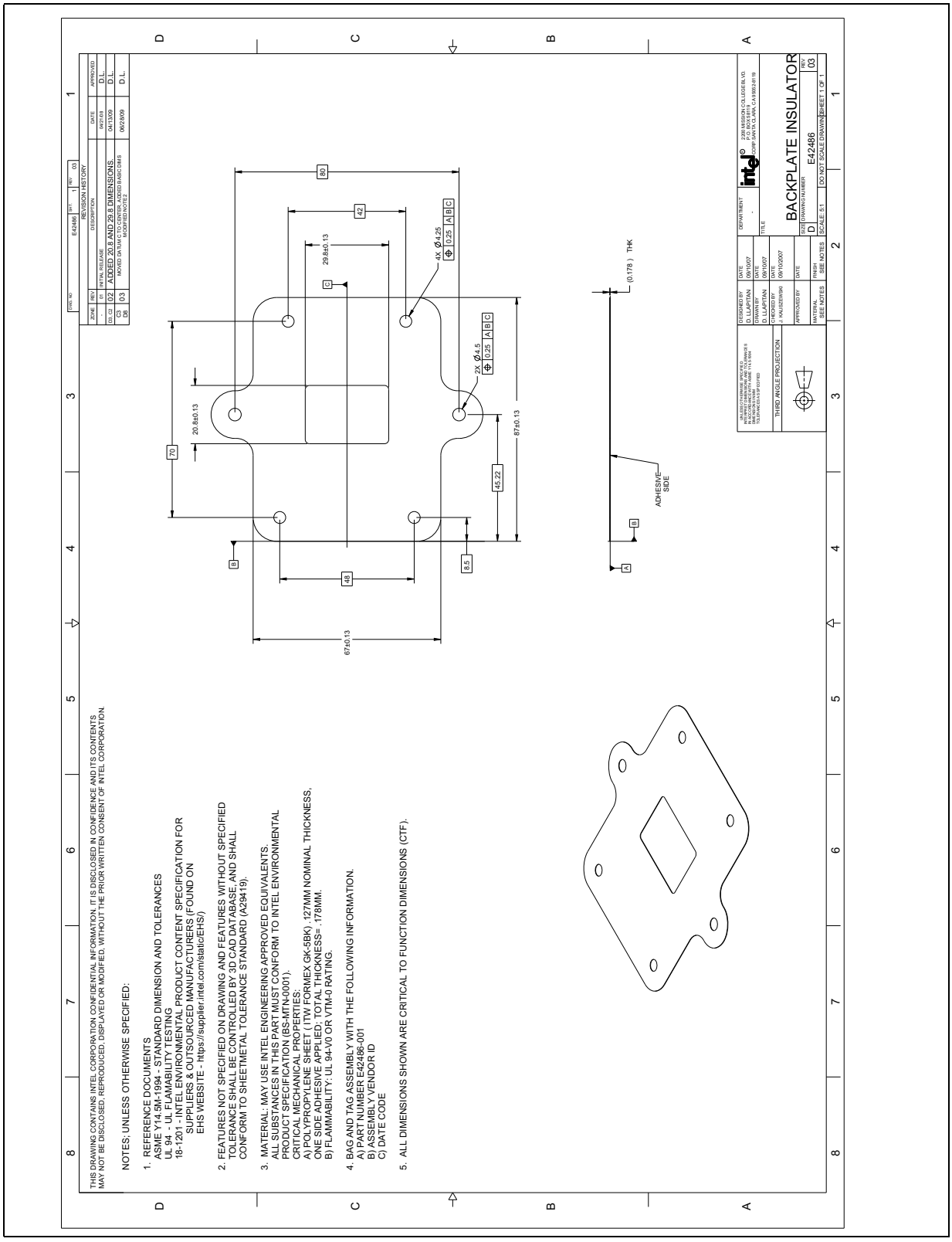


Figure C-19. Backplate Assembly Drawing – Sheet 4 of 5

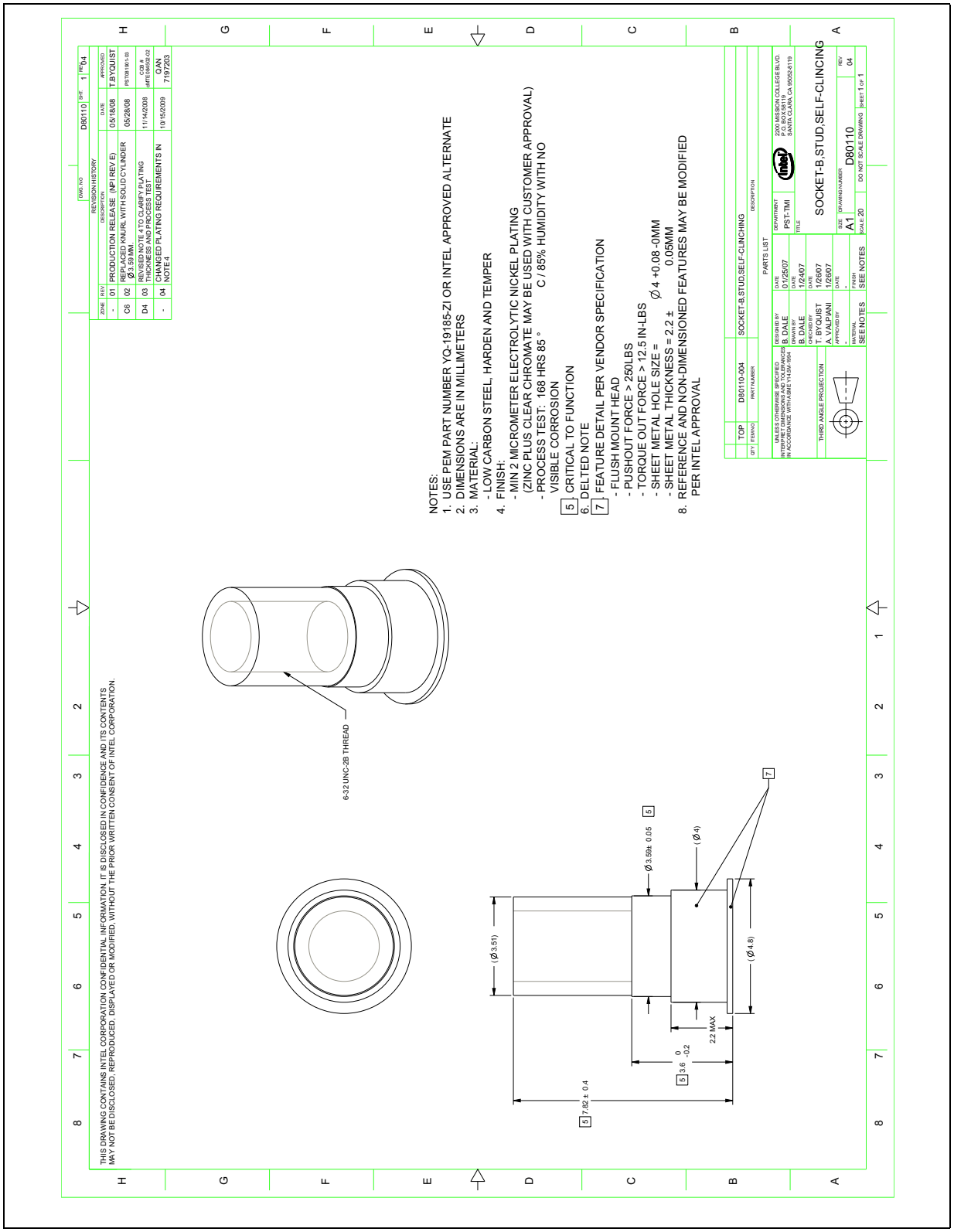
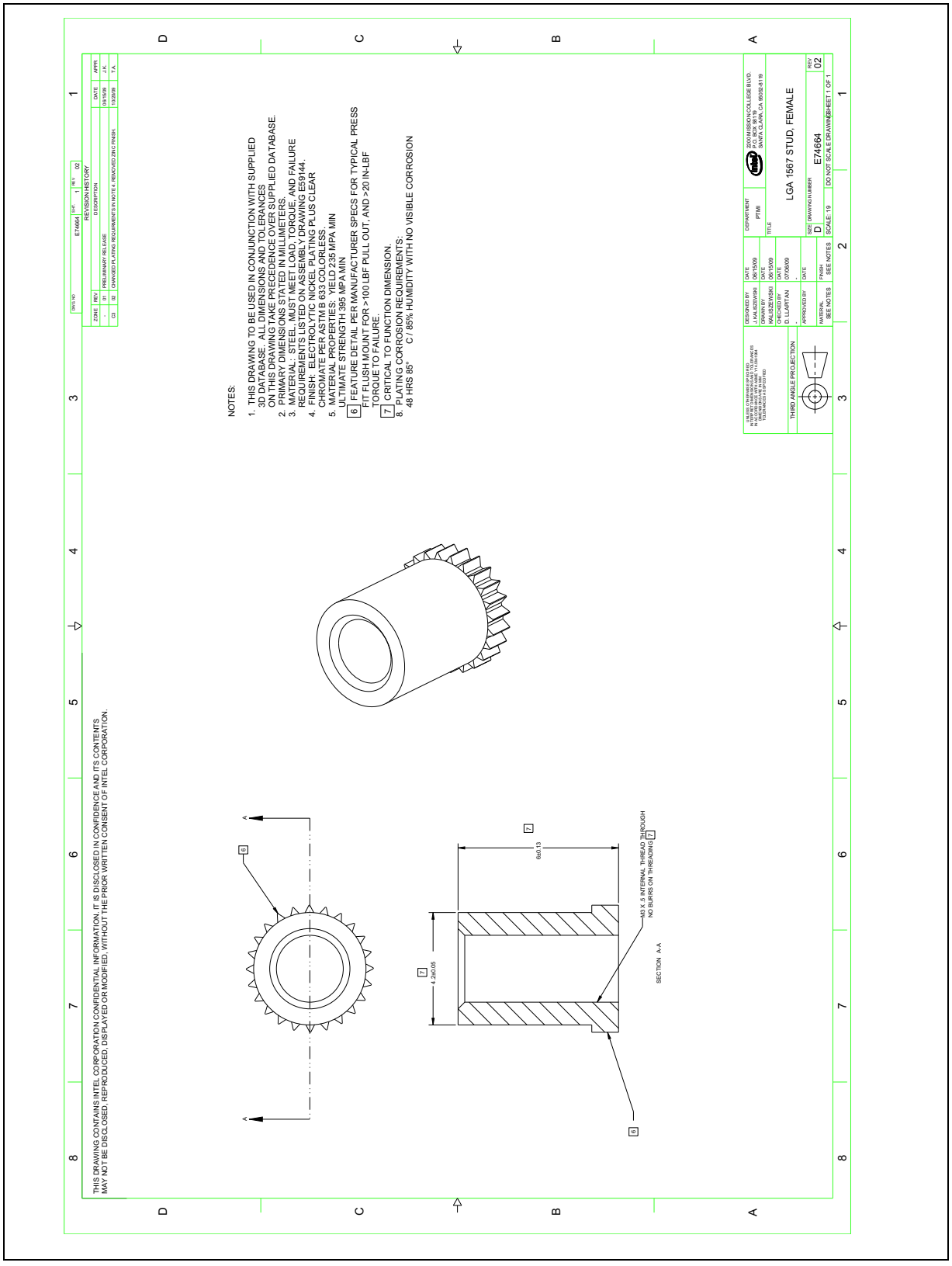


Figure C-20. Backplate Assembly Drawing – Sheet 5 of 5



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D Tower Heatsink Drawings

Table D-1 lists the mechanical drawings included in this appendix.

Table D-1. Mechanical Drawing List

Drawing Description	Figure Number
“Tower Heatsink Drawing – Sheet 1 of 14”	Figure D-1
“Tower Heatsink Drawing – Sheet 2 of 14”	Figure D-2
“Tower Heatsink Drawing – Sheet 3 of 14”	Figure D-3
“Tower Heatsink Drawing – Sheet 4 of 14”	Figure D-4
“Tower Heatsink Drawing – Sheet 5 of 14”	Figure D-5
“Tower Heatsink Drawing – Sheet 6 of 14”	Figure D-6
“Tower Heatsink Drawing – Sheet 7 of 14”	Figure D-7
“Tower Heatsink Drawing – Sheet 8 of 14”	Figure D-8
“Tower Heatsink Drawing – Sheet 9 of 14”	Figure D-9
“Tower Heatsink Drawing – Sheet 10 of 14”	Figure D-10
“Tower Heatsink Drawing – Sheet 11 of 14”	Figure D-11
“Tower Heatsink Drawing – Sheet 12 of 14”	Figure D-12
“Tower Heatsink Drawing – Sheet 13 of 14”	Figure D-13
“Tower Heatsink Drawing – Sheet 14 of 14”	Figure D-14

Figure D-1. Tower Heatsink Drawing – Sheet 1 of 14

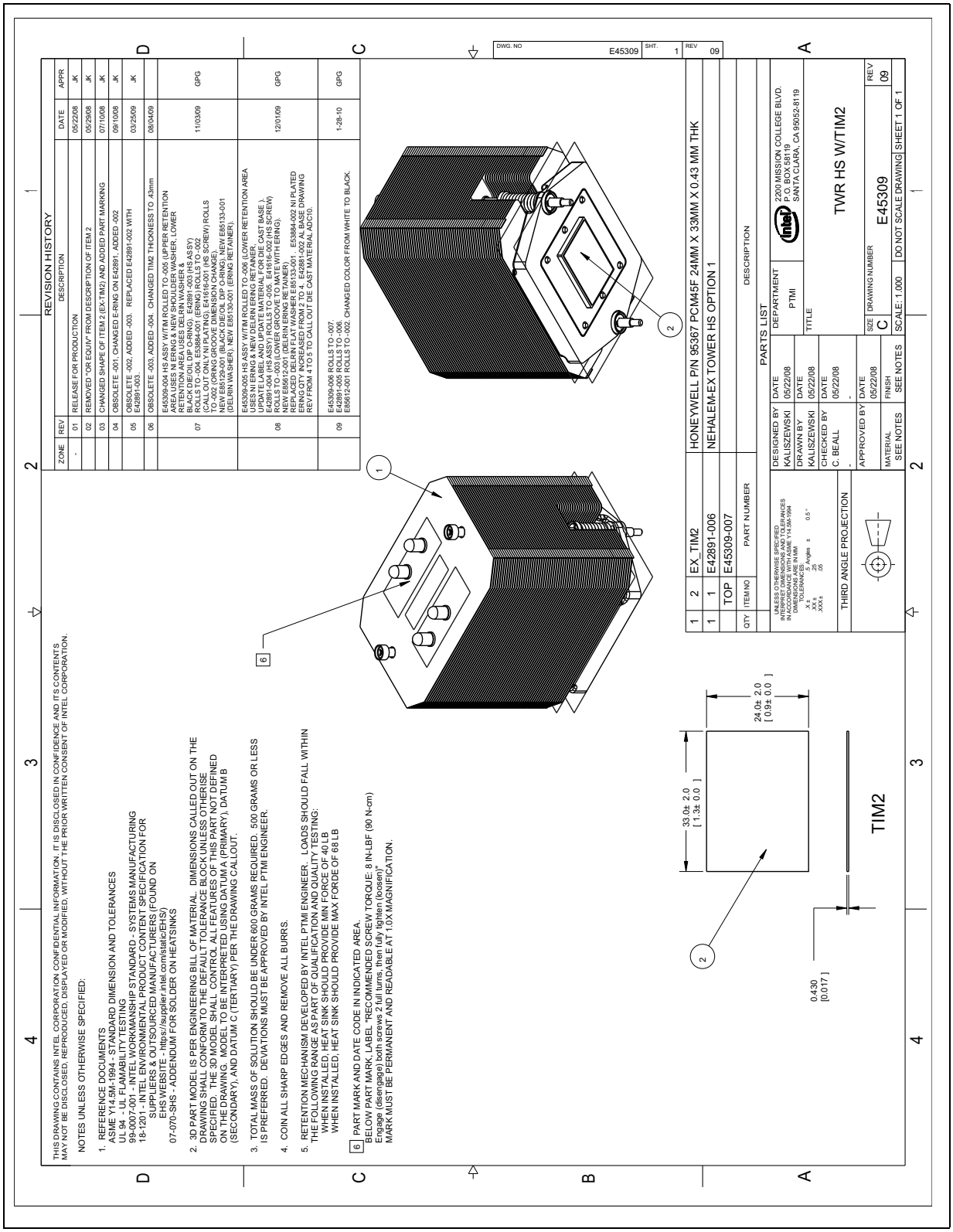


Figure D-2. Tower Heatsink Drawing – Sheet 2 of 14

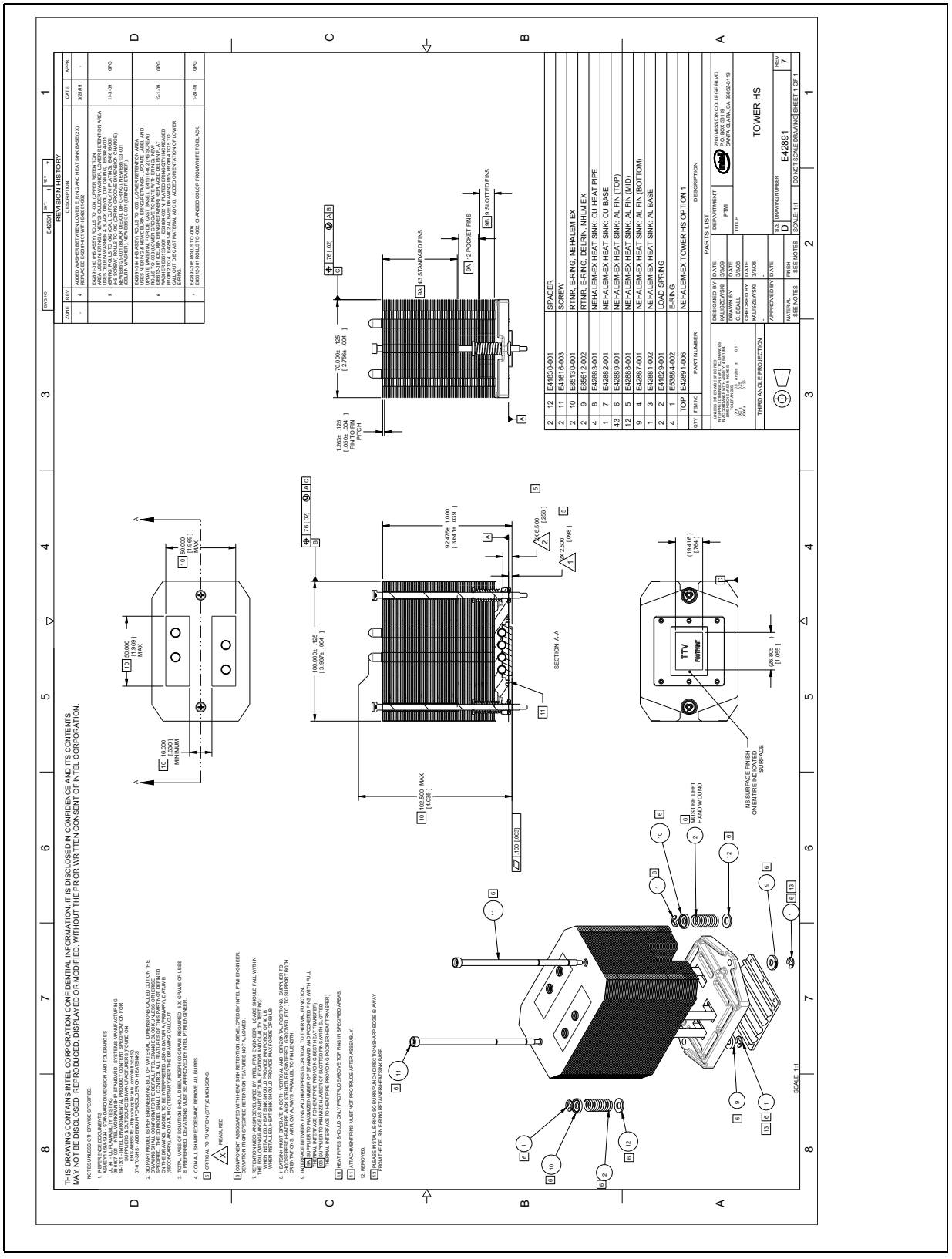


Figure D-3. Tower Heatsink Drawing – Sheet 3 of 14

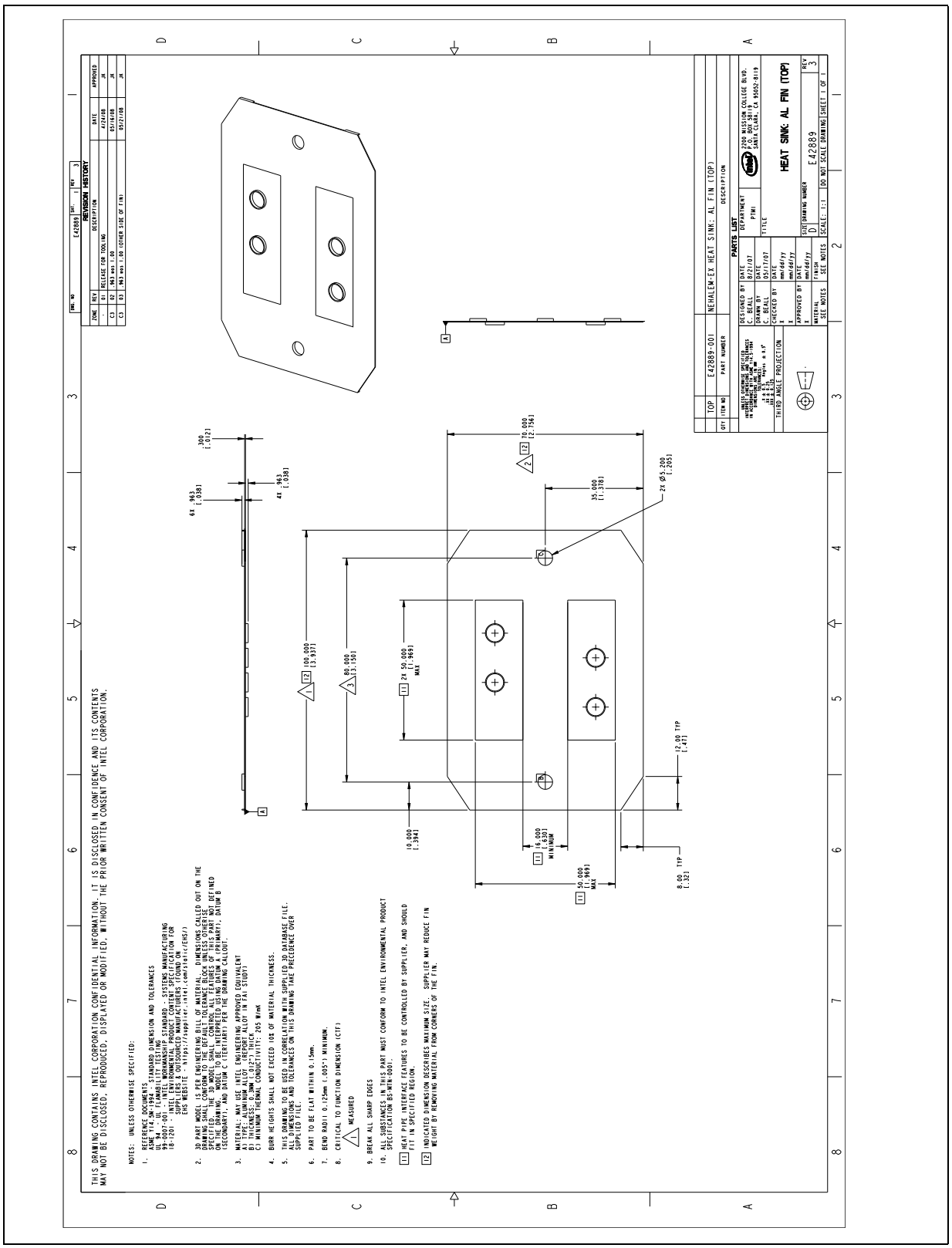


Figure D-4. Tower Heatsink Drawing – Sheet 4 of 14

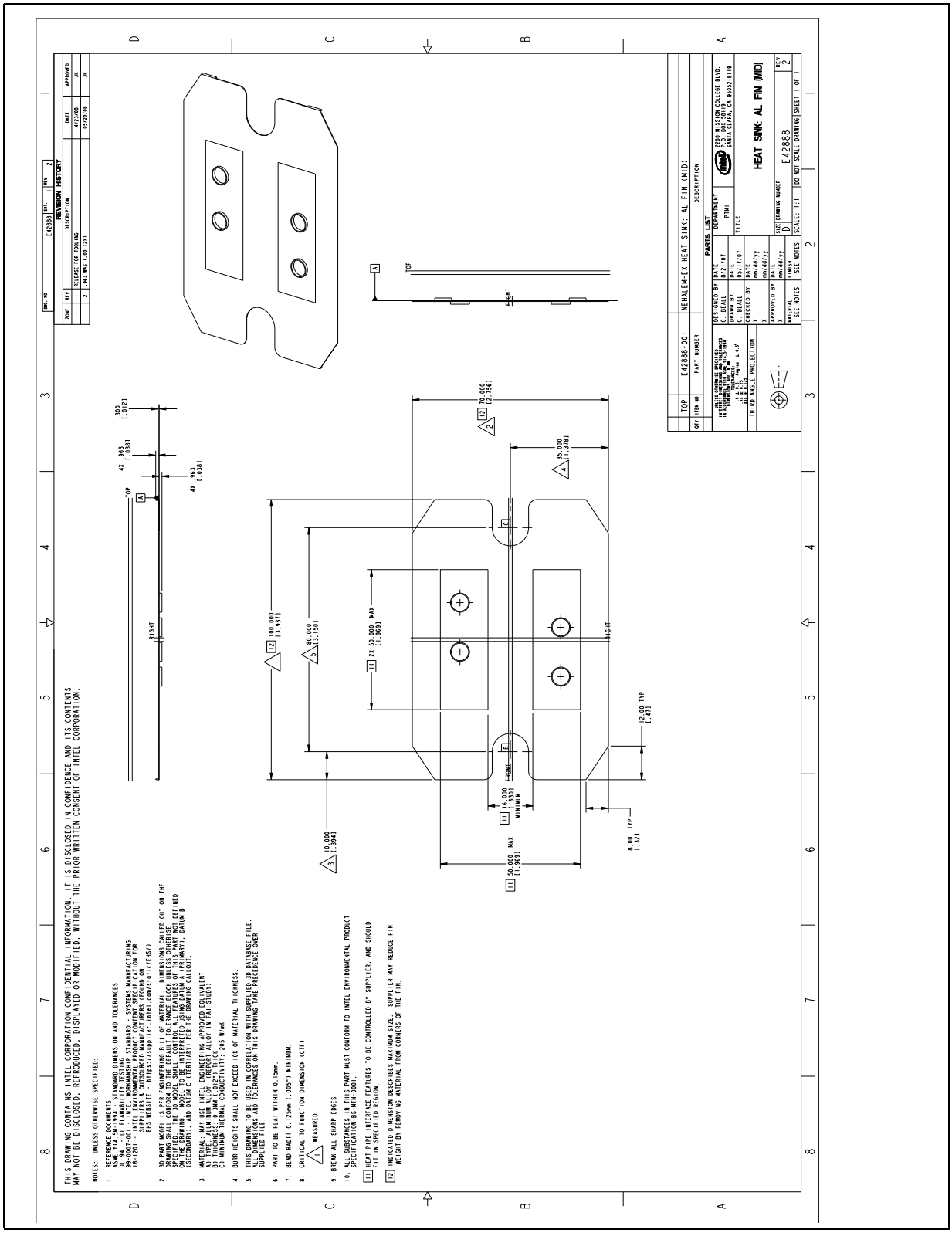


Figure D-5. Tower Heatsink Drawing – Sheet 5 of 14

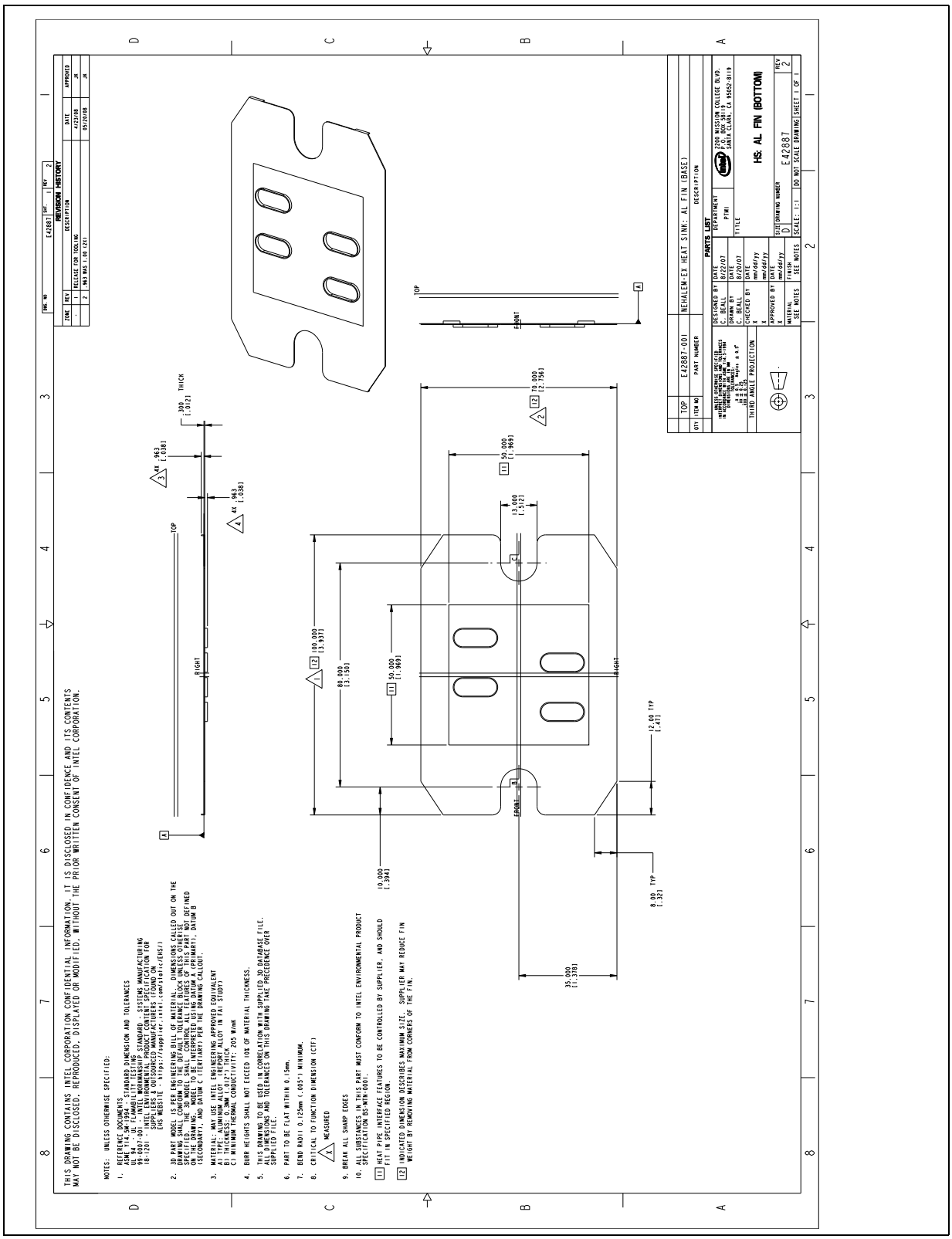


Figure D-6. Tower Heatsink Drawing – Sheet 6 of 14

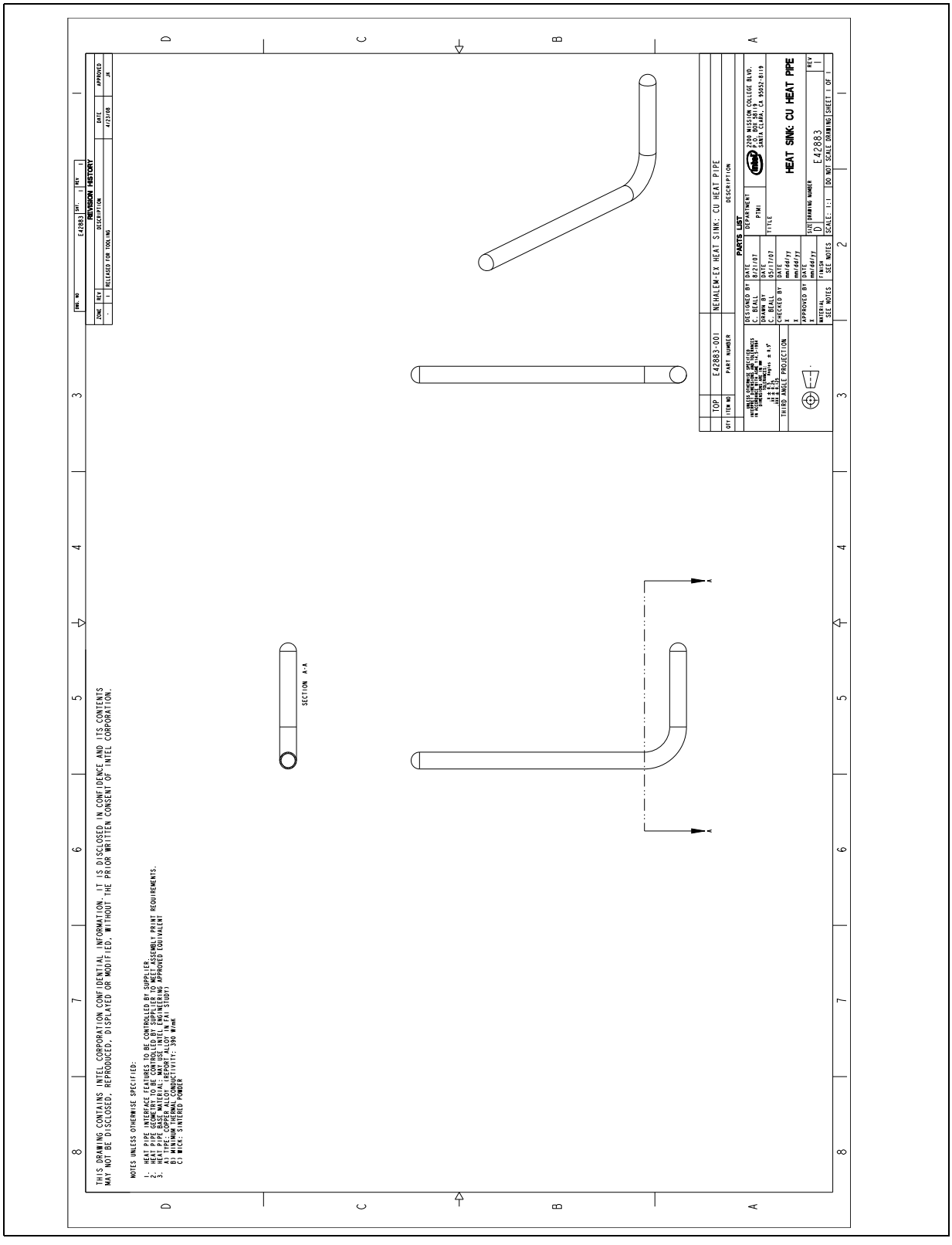


Figure D-7. Tower Heatsink Drawing – Sheet 7 of 14

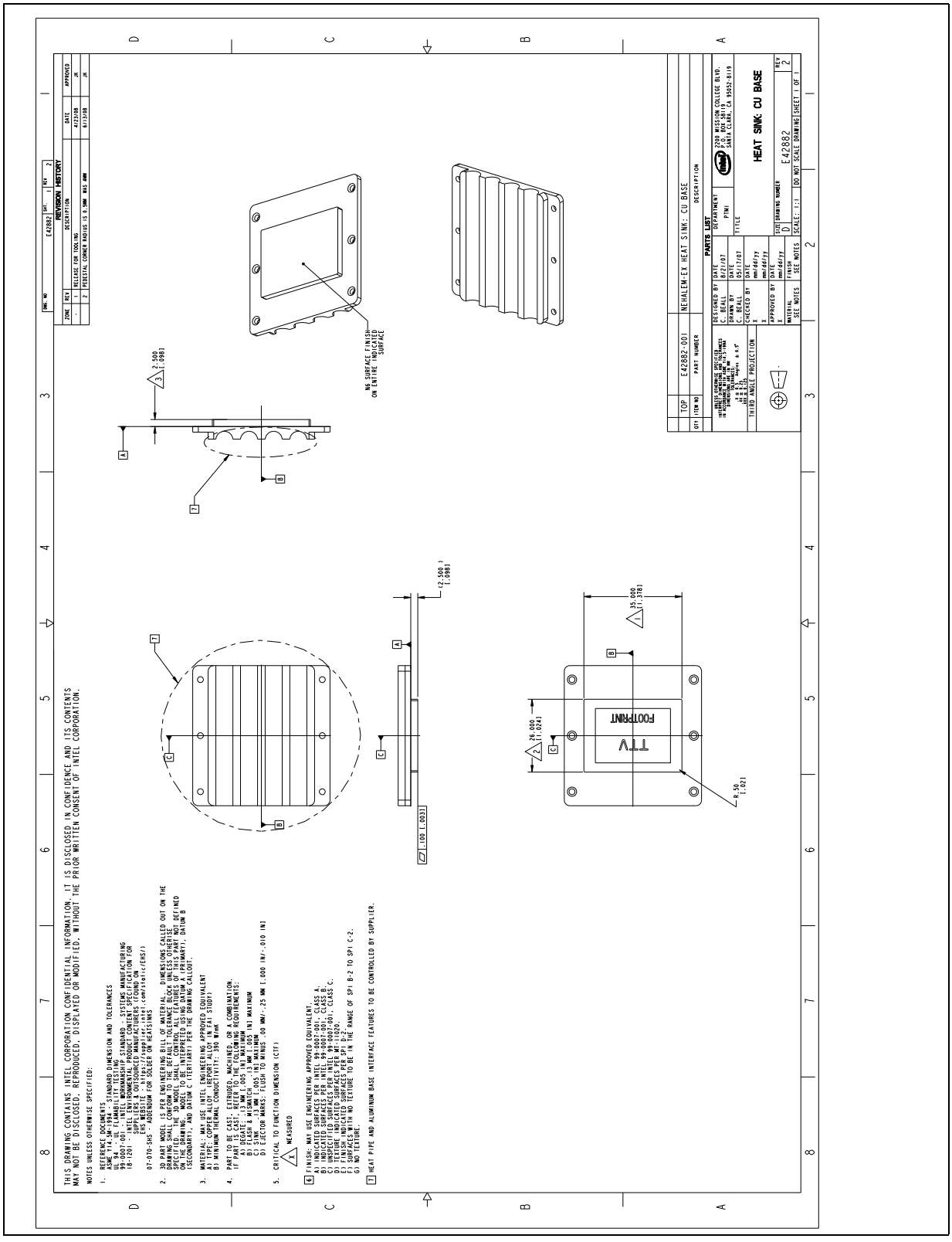


Figure D-8. Tower Heatsink Drawing – Sheet 8 of 14

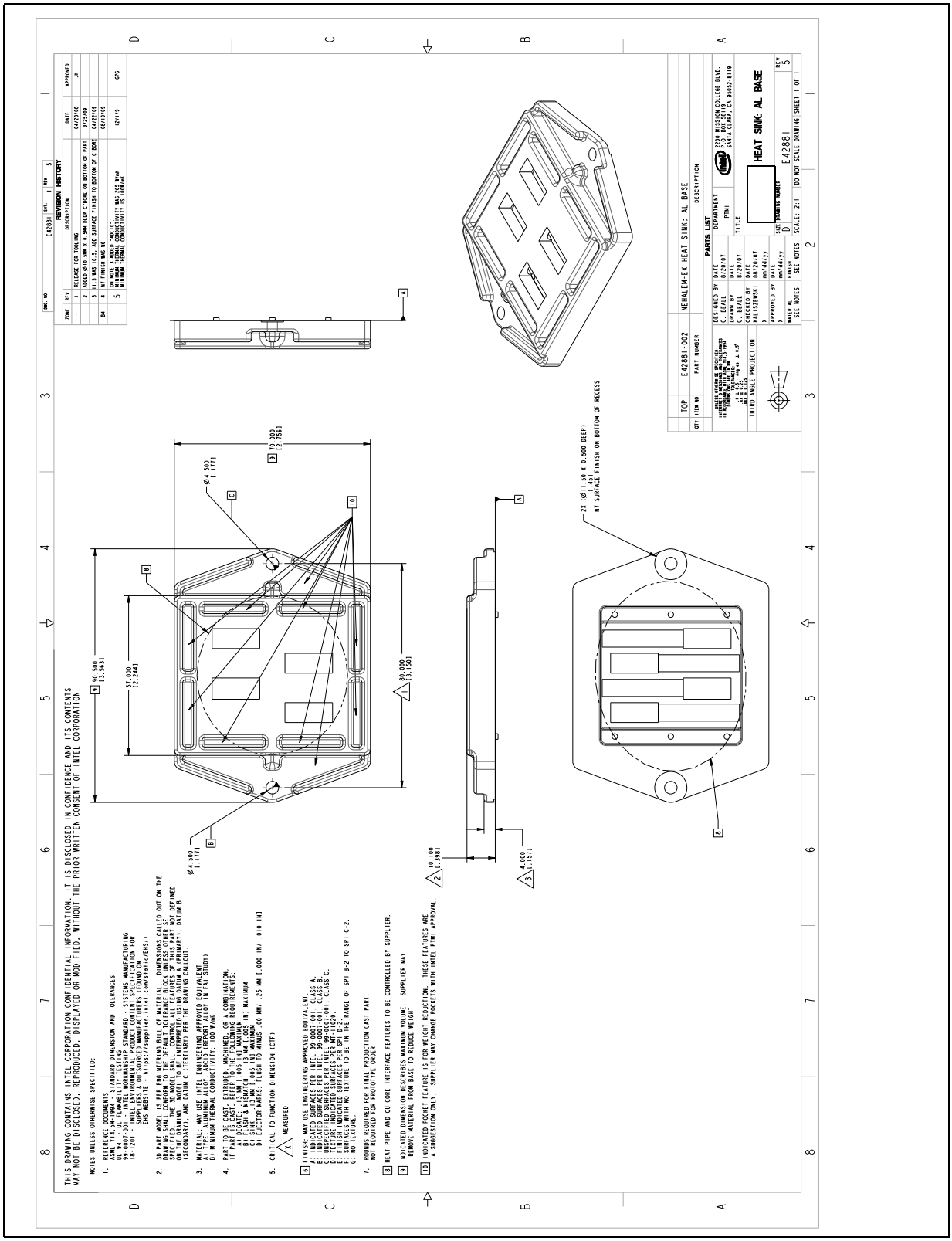


Figure D-9. Tower Heatsink Drawing – Sheet 9 of 14

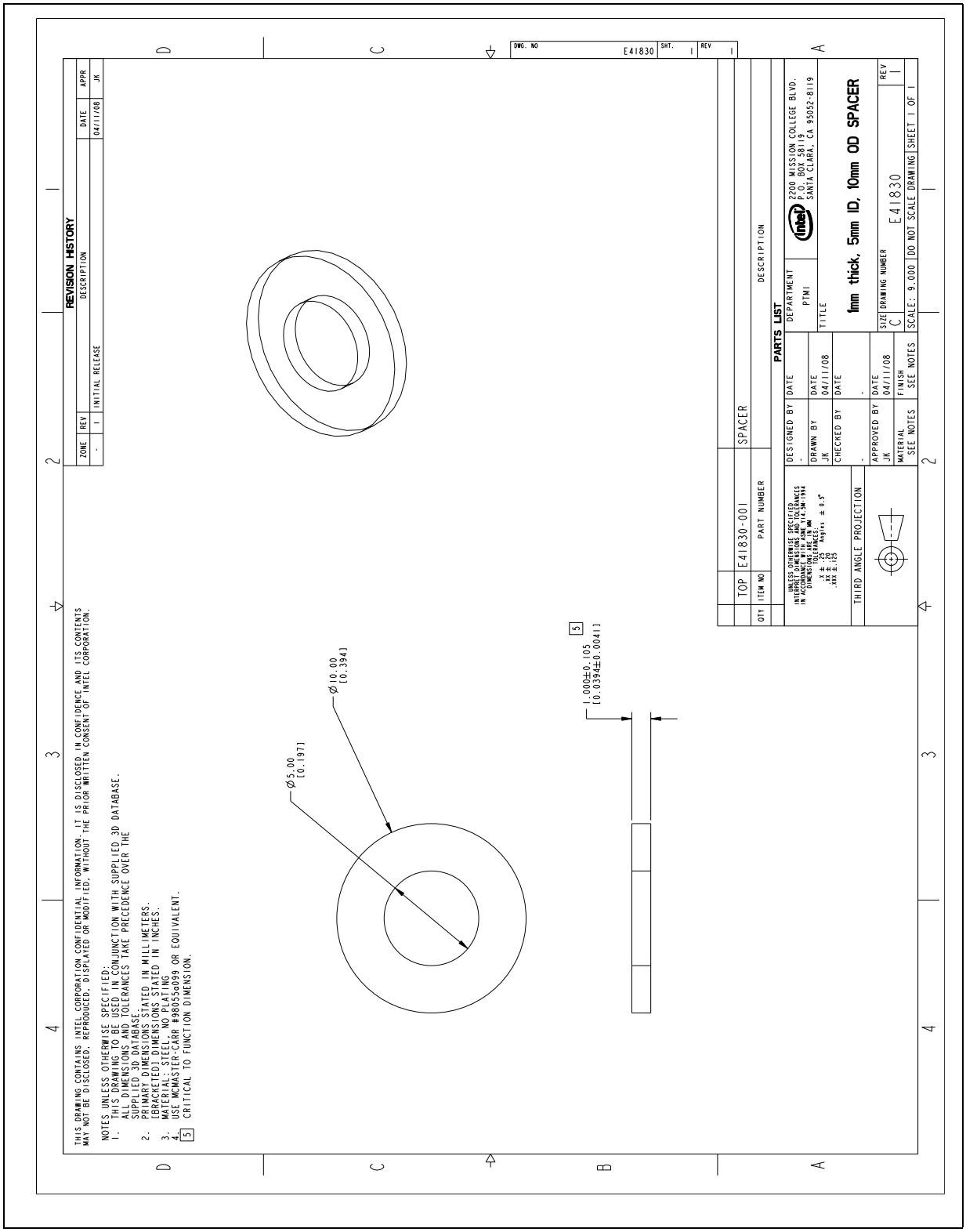


Figure D-10. Tower Heatsink Drawing – Sheet 10 of 14

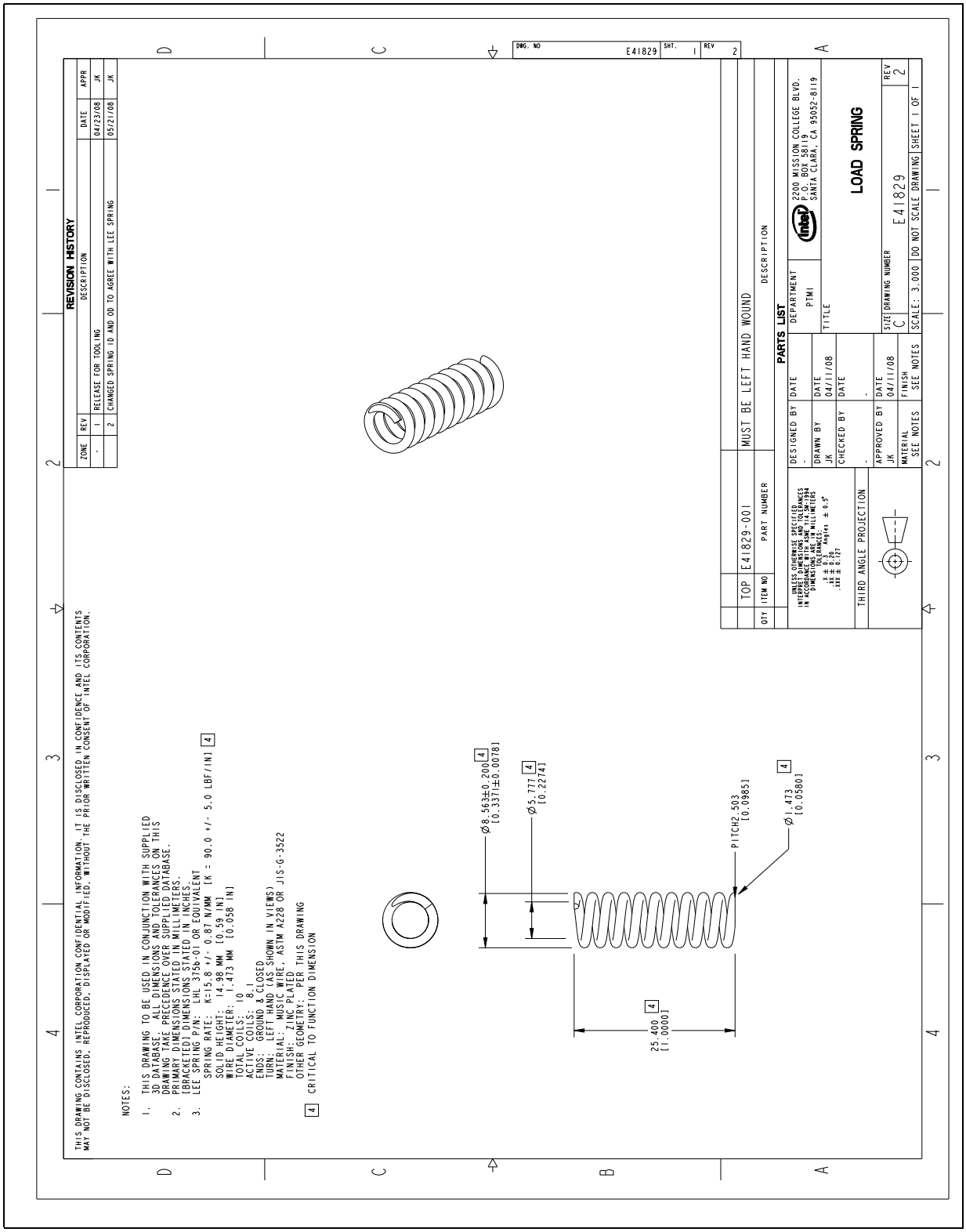


Figure D-11. Tower Heatsink Drawing – Sheet 11 of 14

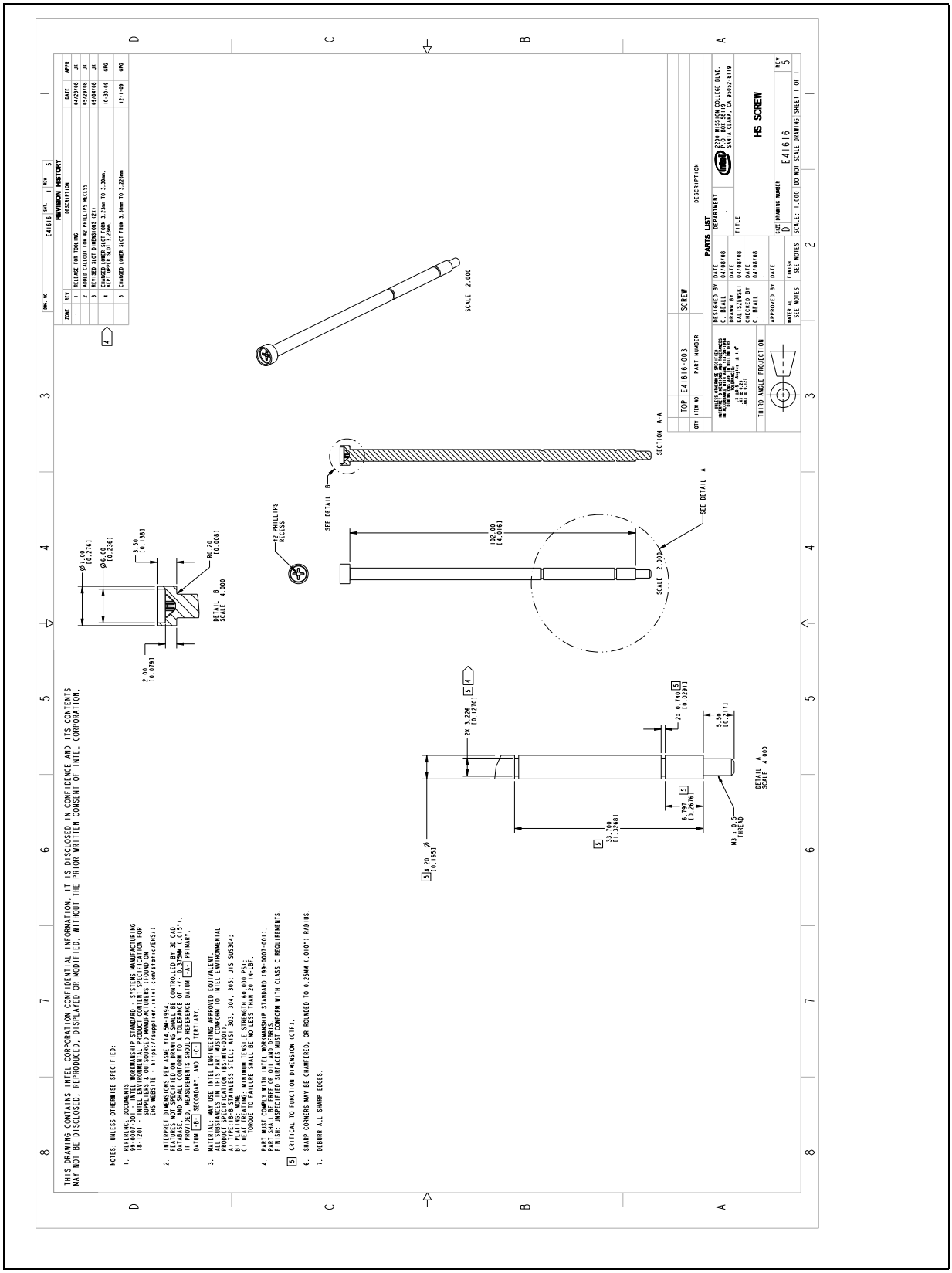


Figure D-12. Tower Heatsink Drawing – Sheet 12 of 14

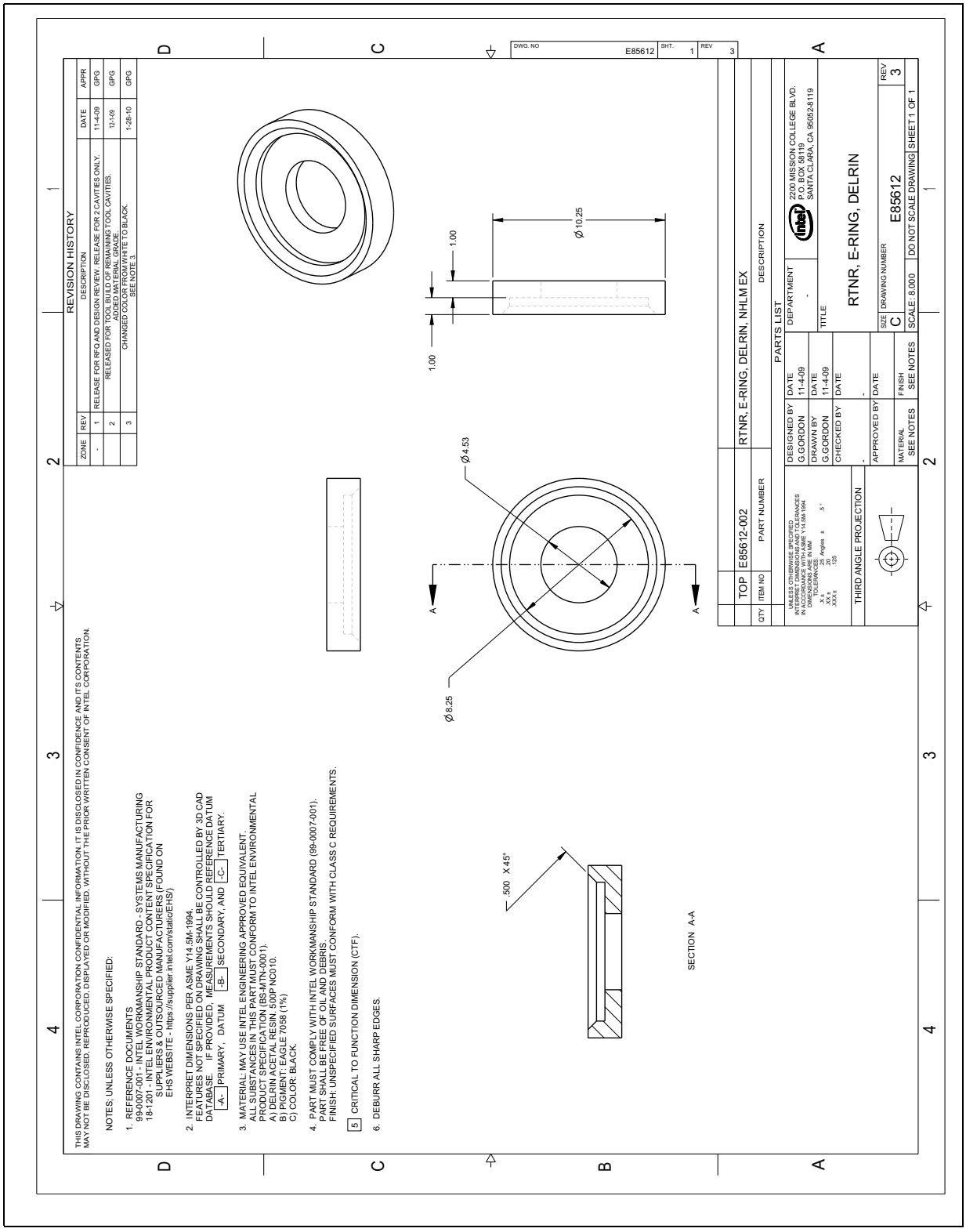


Figure D-13. Tower Heatsink Drawing – Sheet 13 of 14

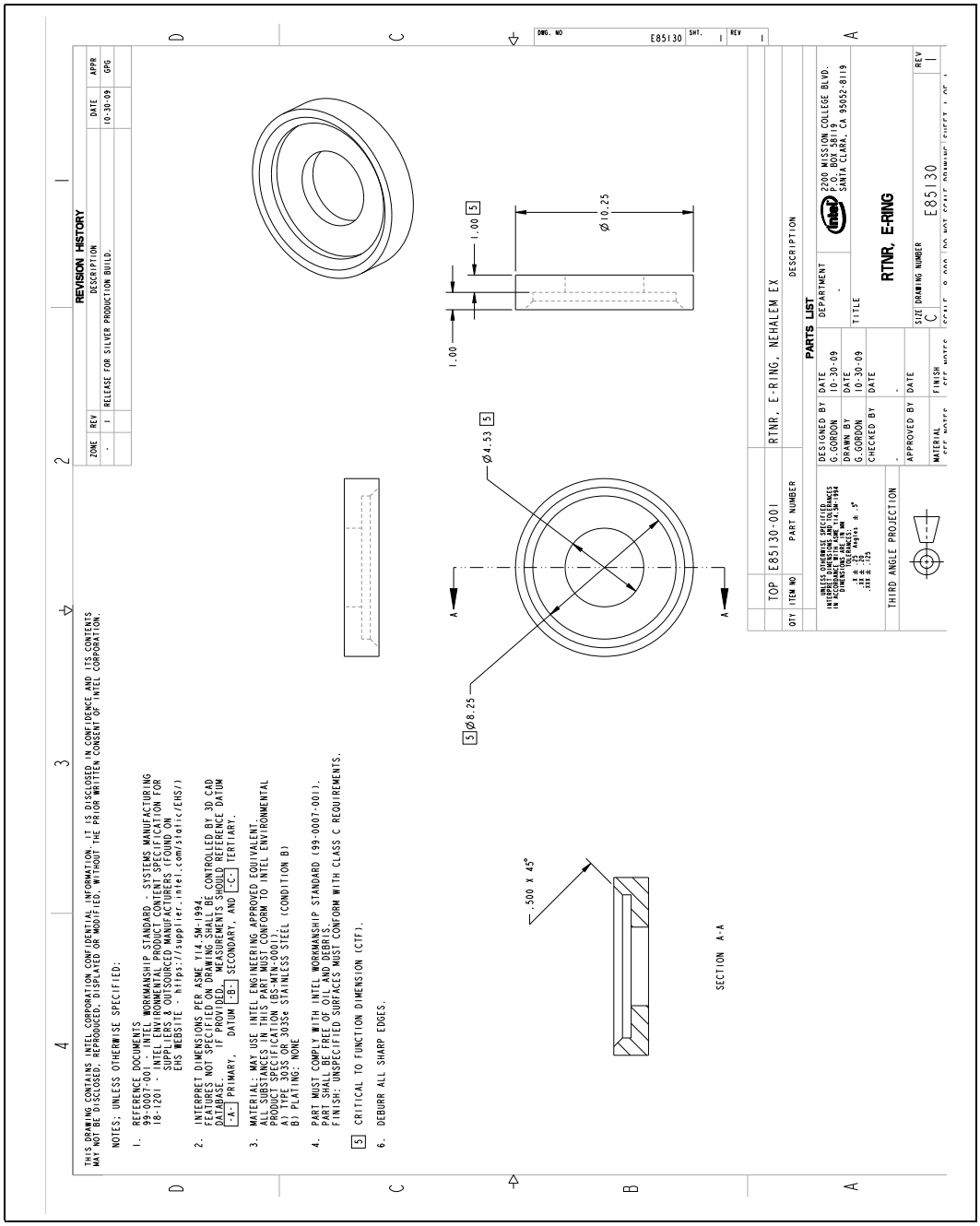
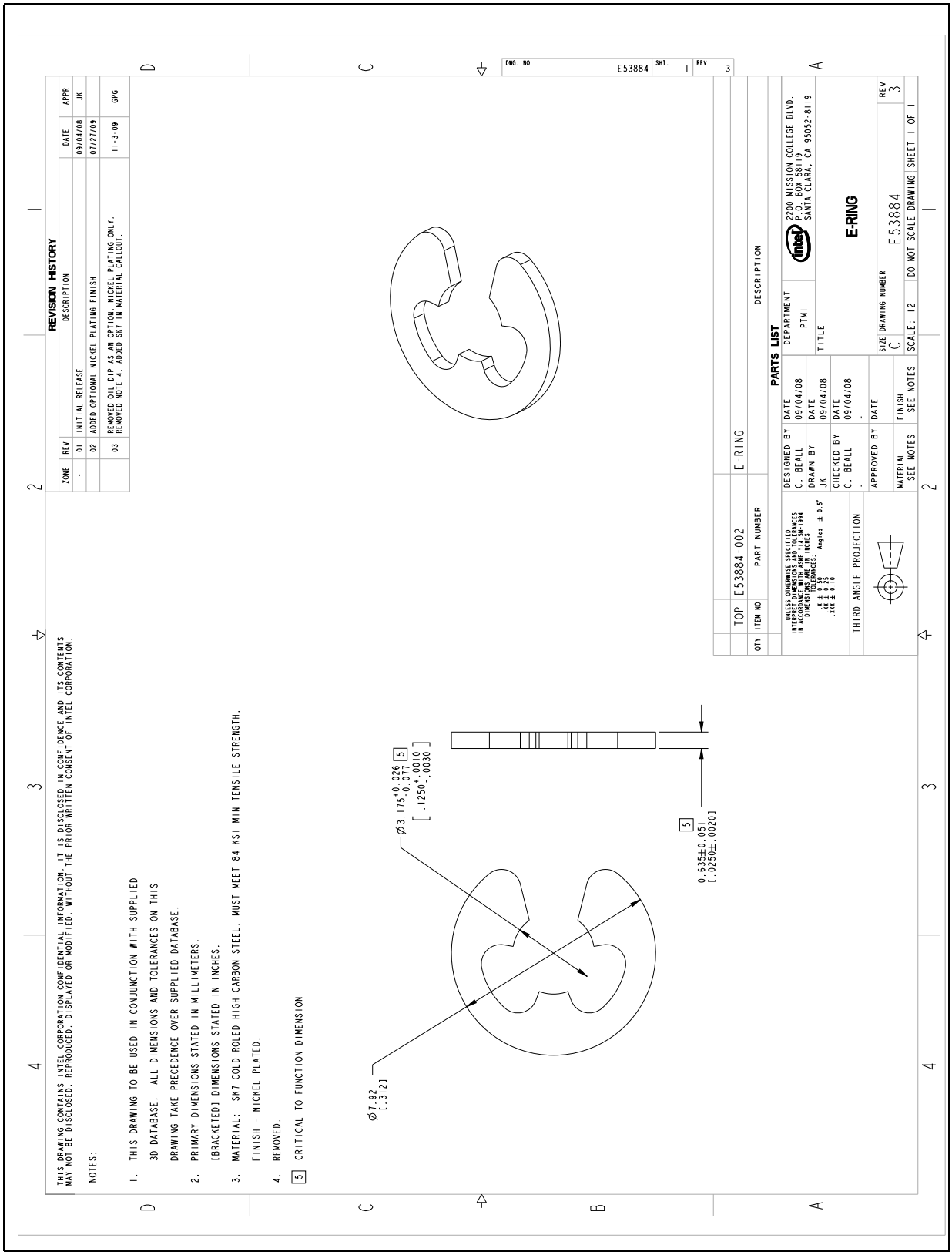


Figure D-14. Tower Heatsink Drawing – Sheet 14 of 14



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E Enabled Component Board Keepout Drawings

Table E-1 lists the mechanical drawings included in this appendix.

Table E-1. Mechanical Drawing List

Drawing Description	Figure Number
"Enabled Component Board Keepout Mechanical Drawing – Sheet 1 of 7"	Figure E-1
"Enabled Component Board Keepout Mechanical Drawing – Sheet 2 of 7"	Figure E-2
"Enabled Component Board Keepout Mechanical Drawing – Sheet 3 of 7"	Figure E-3
"Enabled Component Board Keepout Mechanical Drawing – Sheet 4 of 7"	Figure E-4
"Enabled Component Board Keepout Mechanical Drawing – Sheet 5 of 7"	Figure E-5
"Enabled Component Board Keepout Mechanical Drawing – Sheet 6 of 7"	Figure E-6
"Enabled Component Board Keepout Mechanical Drawing – Sheet 7of 7"	Figure E-7

Figure E-1. Enabled Component Board Keepout Mechanical Drawing – Sheet 1 of 7

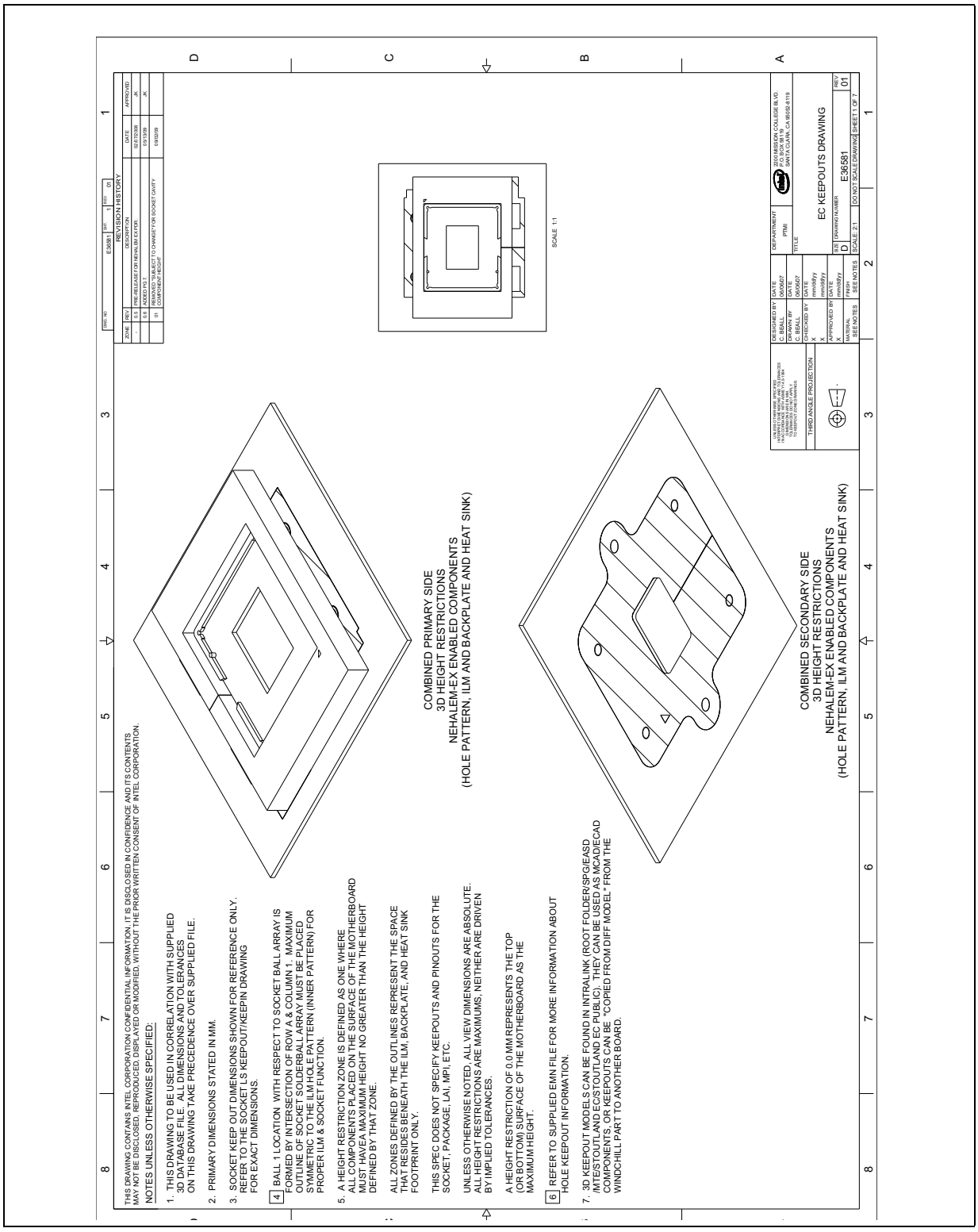


Figure E-2. Enabled Component Board Keepout Mechanical Drawing – Sheet 2 of 7

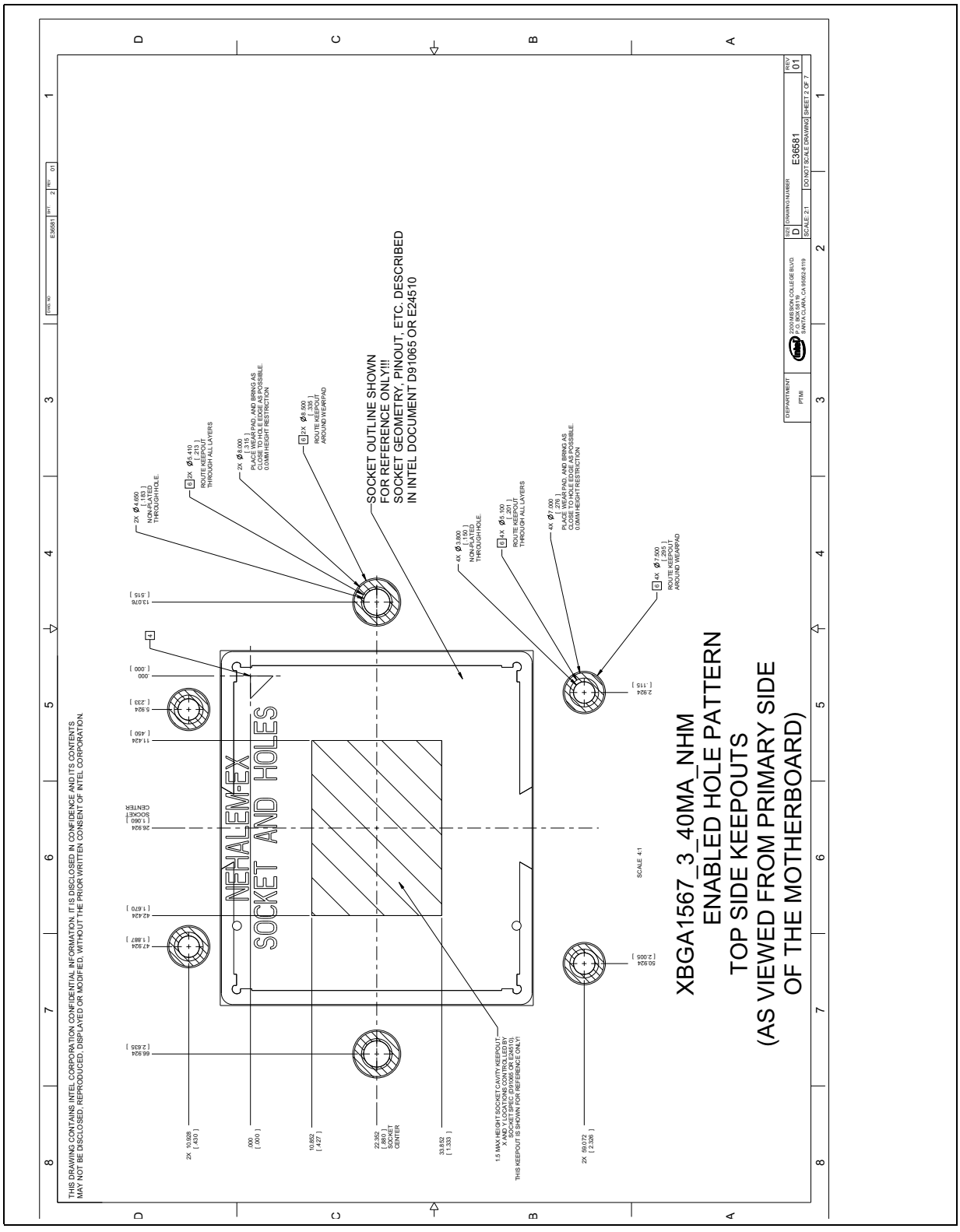


Figure E-3. Enabled Component Board Keepout Mechanical Drawing – Sheet 3 of 7

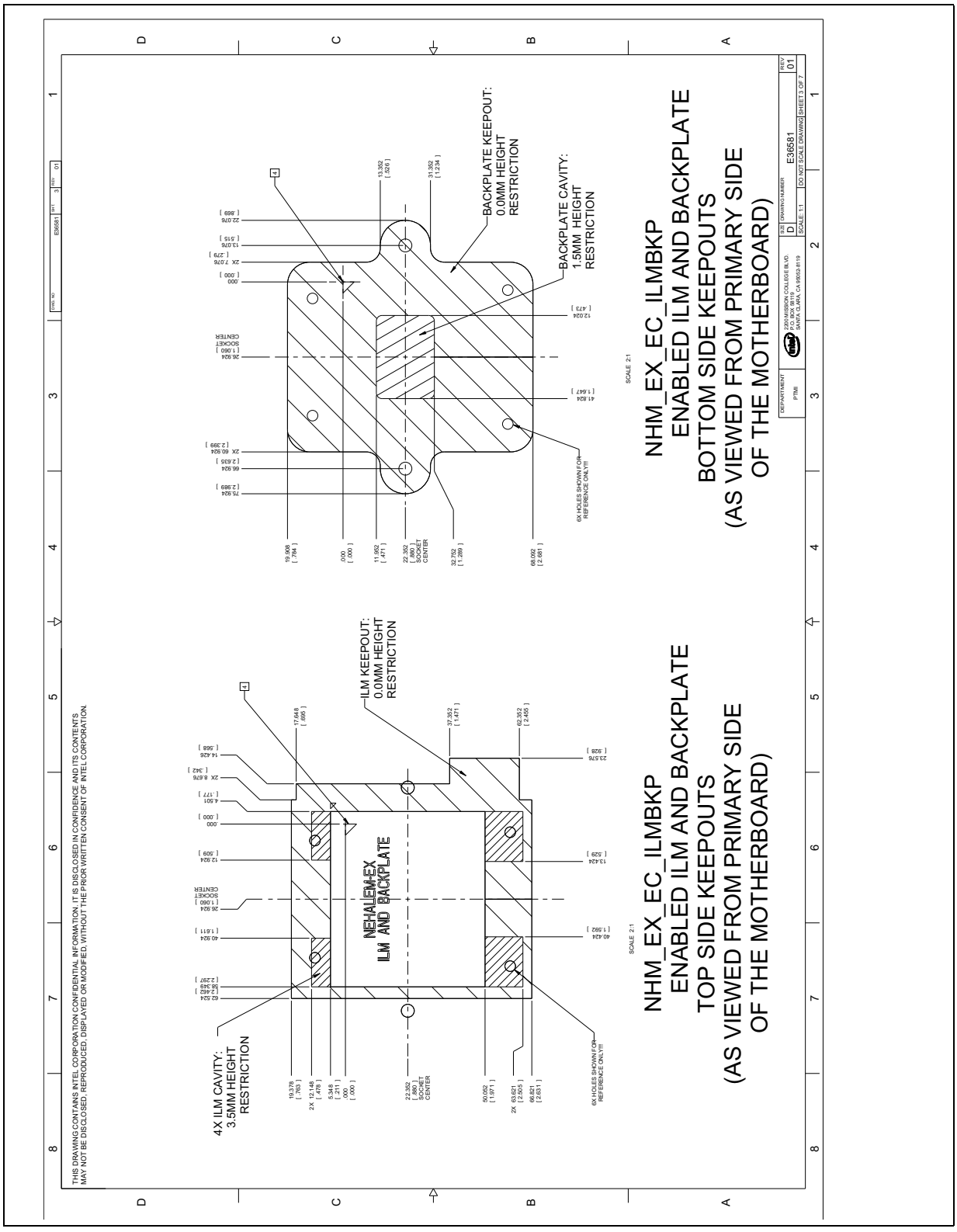


Figure E-4. Enabled Component Board Keepout Mechanical Drawing – Sheet 4 of 7

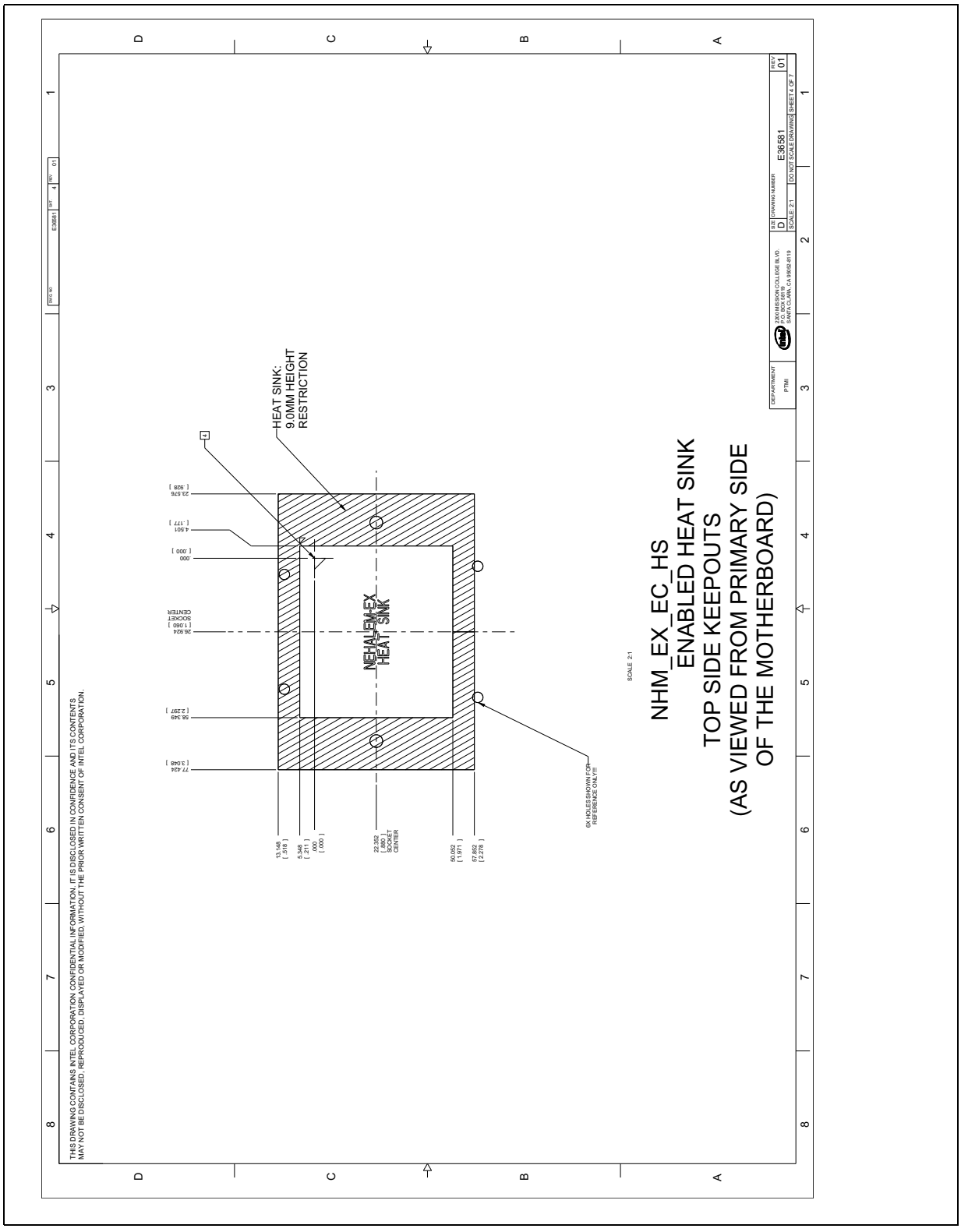


Figure E-5. Enabled Component Board Keepout Mechanical Drawing – Sheet 5 of 7

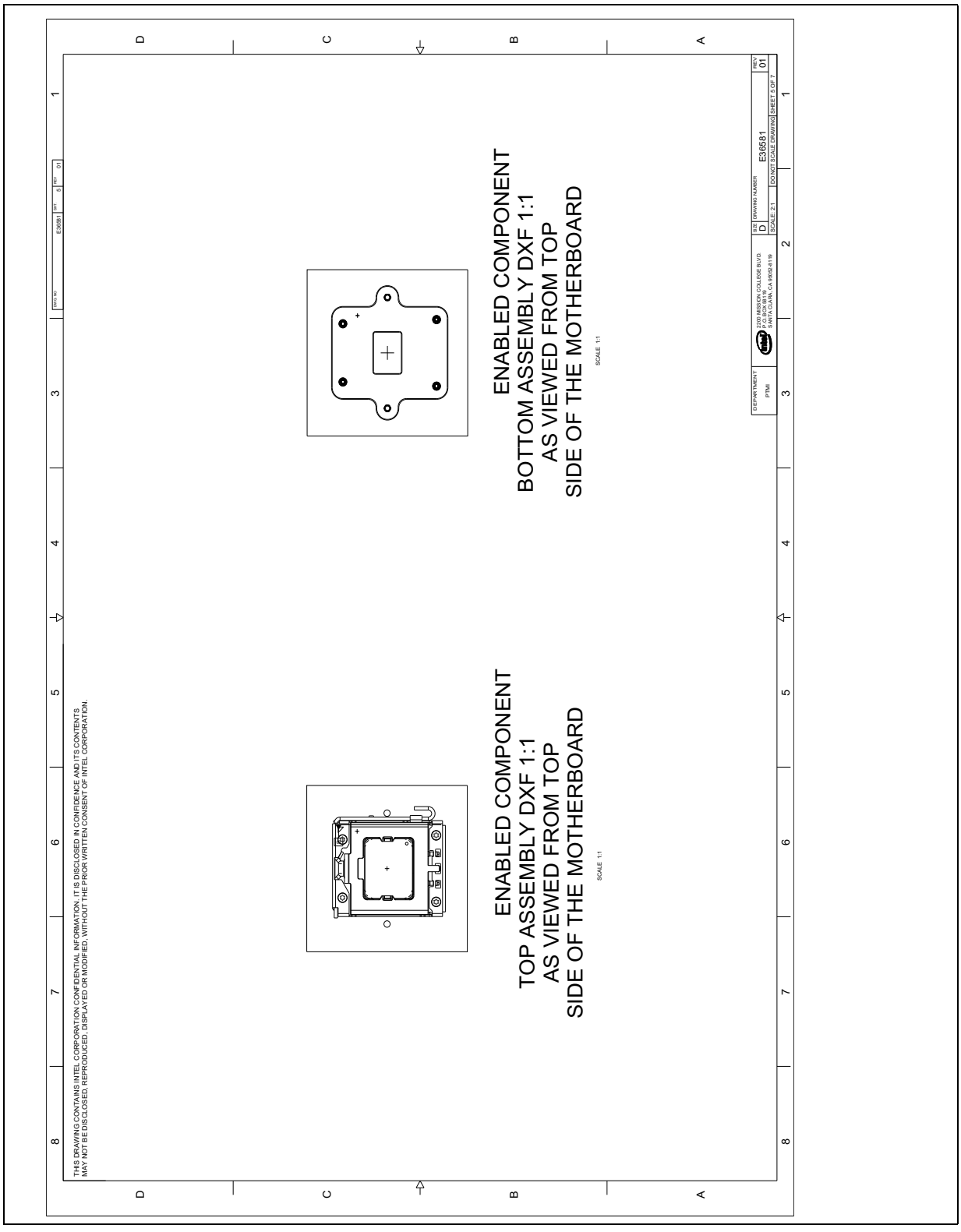


Figure E-6. Enabled Component Board Keepout Mechanical Drawing – Sheet 6 of 7

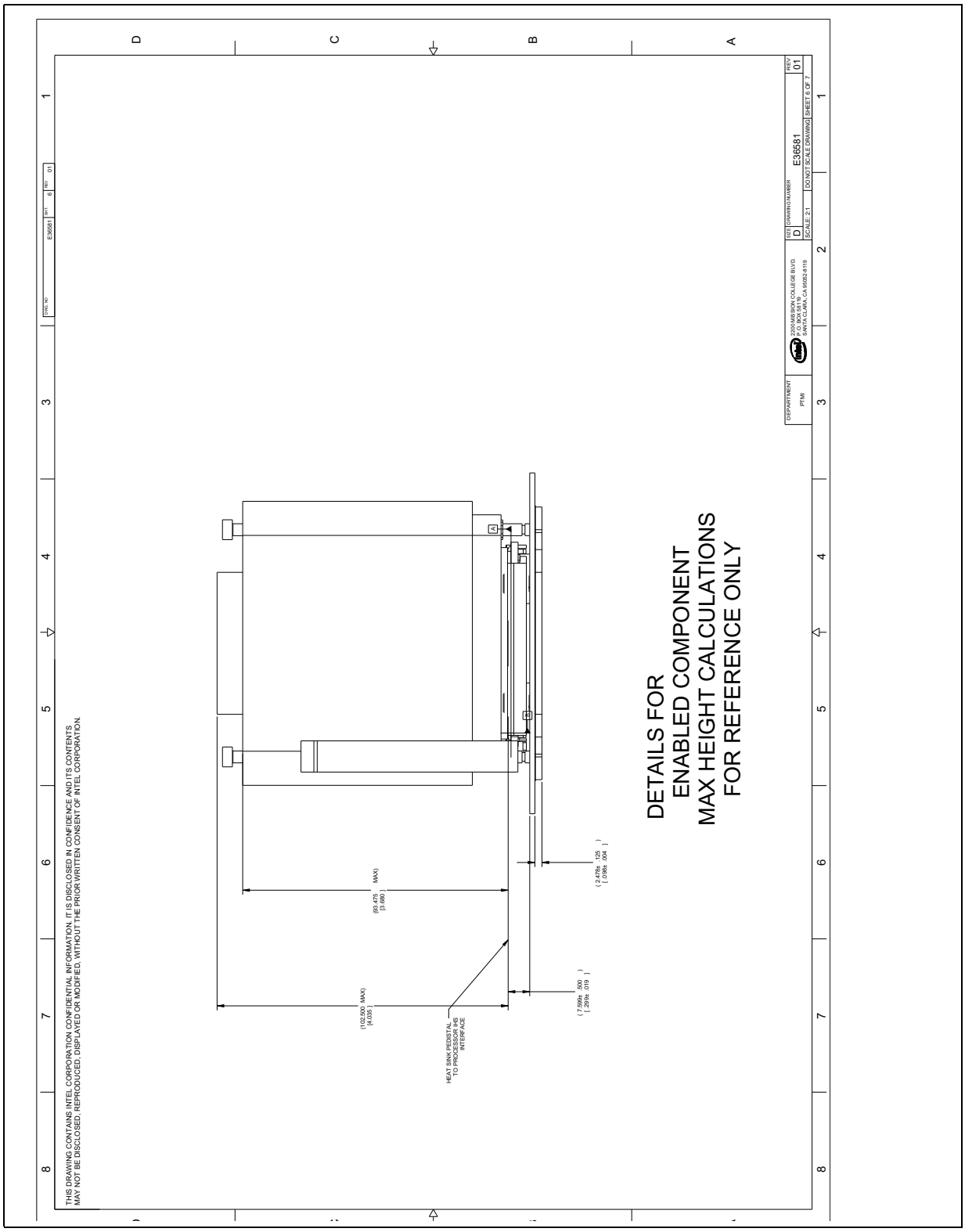
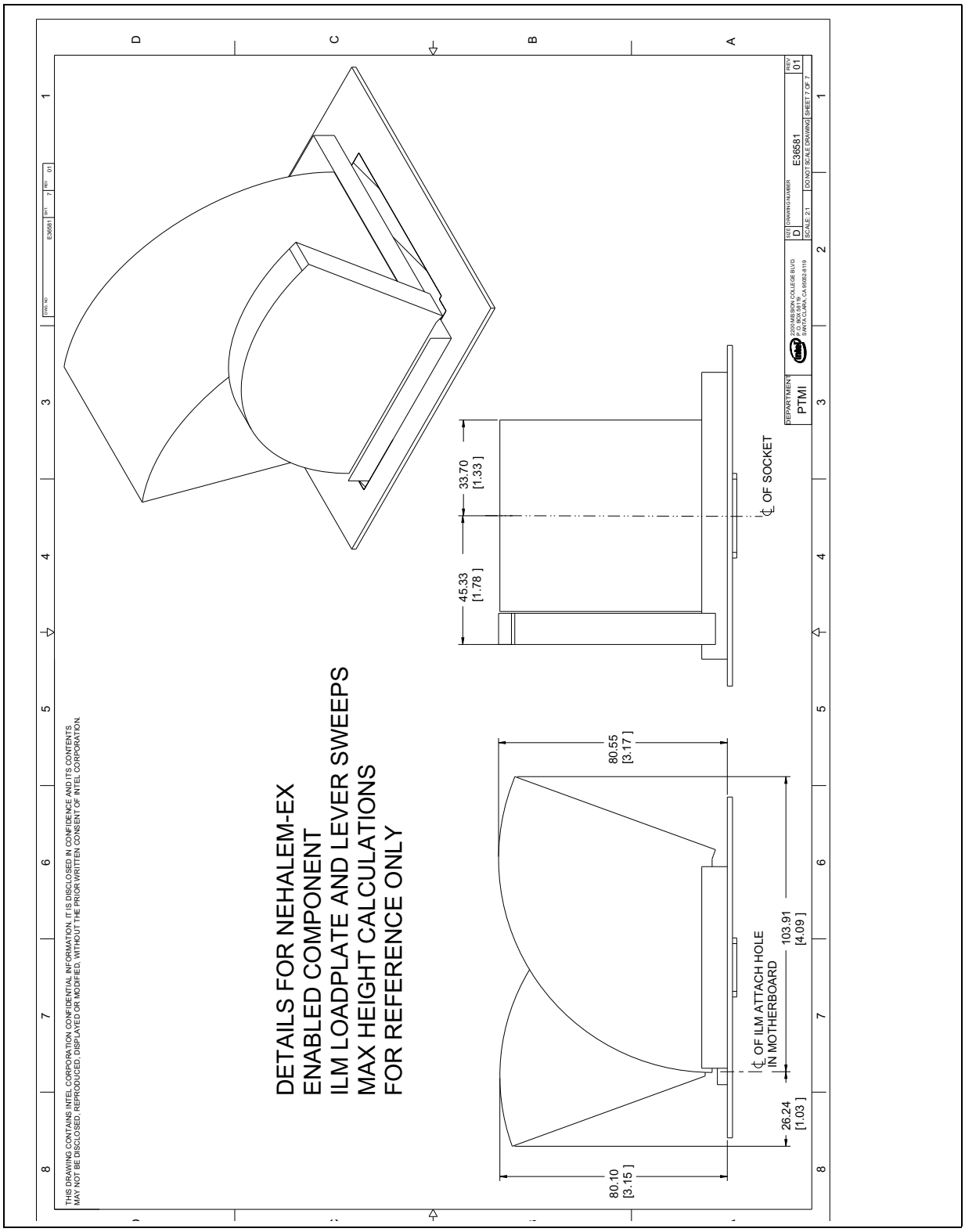


Figure E-7. Enabled Component Board Keepout Mechanical Drawing – Sheet 7of 7



F Electrical Methodology

F.1 Measuring Electrical Resistance of the Jumper

Figure F-1 and Figure F-2 show the proposed methodology for measuring the final electrical resistance. The methodology requires measuring LGA TV flush-mounted directly to the motherboard fixtures, so that the Land shoulder is flush with the motherboard to get the averaged jumper resistance, R_{jumper}. The R_{jumper} should come from a good statistical average of 30 package fixtures flush mounted to a motherboard fixture. The same measurements are then made with a package fixture mounted on a supplier's socket, and both are mounted on a motherboard fixture; this provides the R_{Total}. The resistance requirement, R_{Req}, can be calculated for each chain, as explained later.

Figure F-1. Methodology for Measuring Total Electrical Resistance

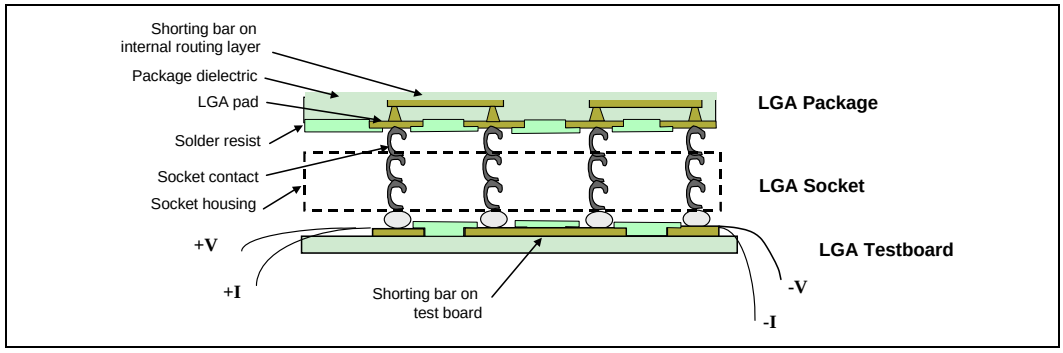


Figure F-2. Methodology for Measuring Electrical Resistance of the Jumper

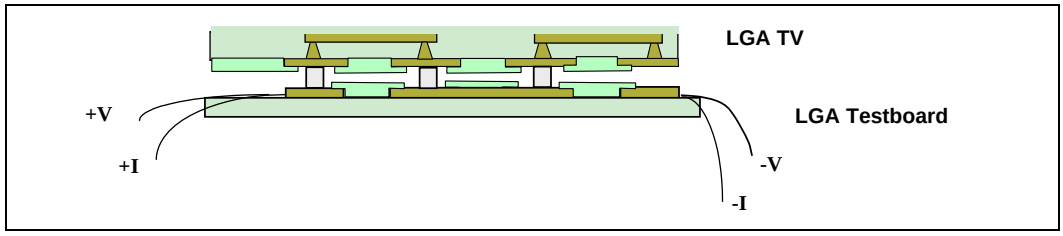


Figure F-3 shows the resistance test fixtures separately and superimposed. The upper figures show the daisy chain pattern of the package and the baseboard. The bottom figure shows the two parts superimposed. There are TBD daisy chain configurations on the resistance test board. Figure F-3 shows these configurations with the number of lands per each chain and netlist. All figures are shown with the view from the top of the package.

F.2 Determining Maximum Electrical Resistance

This section provides a guideline for the instruments used to take the measurements.

Note: The instrument selection should consider the guidelines in EIA 364-23A.

- These measurements use a 4-wire technique, where the instruments provide two separate circuits. One is a precision current source to deliver the test current. The other is a precision voltmeter circuit to measure the voltage drop between the desired points.
- These separate circuits can be contained within one instrument, such as a high-quality micro-ohmmeter, a stand-alone current source and voltmeter, or the circuits of a data acquisition system.
- Measurement accuracy in Ω is specified as ± 0.1% of reading, or ±0.1 mΩ, whichever is greater. The vendor is responsible for demonstrating that their instrument(s) can meet this accuracy.
- Automation of the measurements can be implemented by scanning the chains through the edge or cable test socket using a switch matrix. The matrix can be operated by hand, or through software.
- Measure R_{Total} for each daisy chain of “package + socket + motherboard” unit.
- Measure R_{jumper} for each daisy chain of 30 “package + socket + motherboard” units. Calculate $\overline{R}_{jumper}$ for each daisy change (there are 303 data for each daisy chain).
- For each socket unit, calculate:

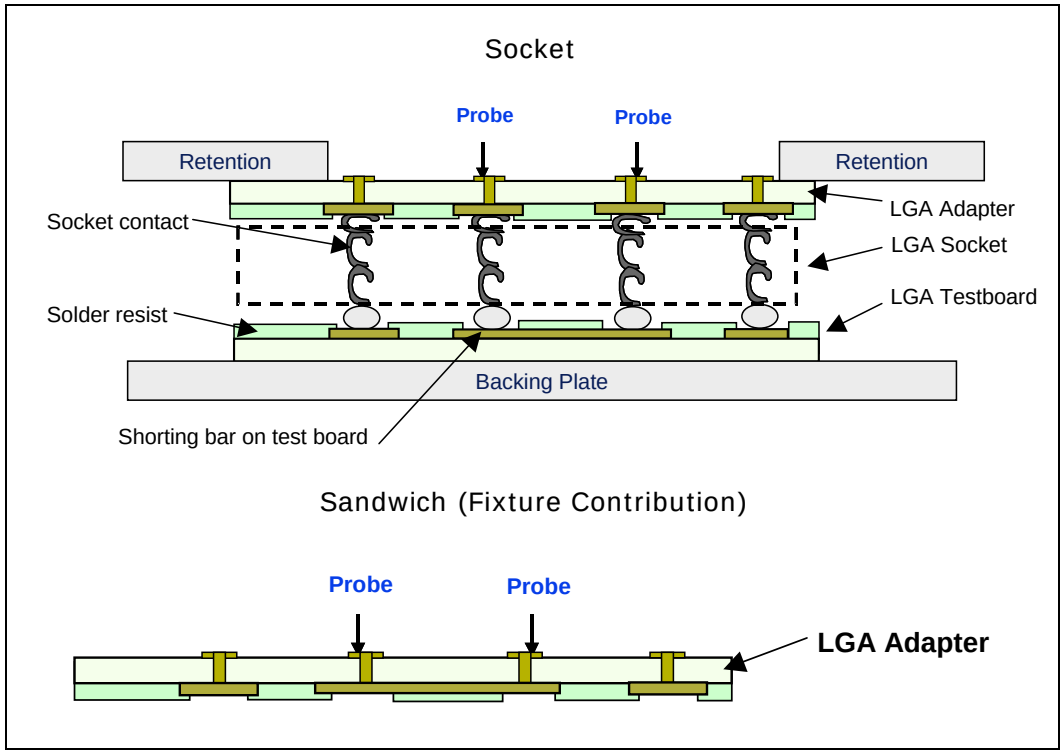
$$R_{Req} = \frac{R_{Total} - \overline{R}_{jumper}}{N}$$

R_{Req} is the average contact resistance for socket pin.

F.3 Inductance

The inductance measurement is completed in two steps. First, the socket is measured in an assembled configuration. A second measurement is made to subtract the fixture contribution. Figure F-3 shows a cross-section of the retention, LGA Adapter, socket, test board, and backing plate assembly. A circuit board, referred to as the LGA adapter, is used to compress the LGA socket leads during test. During test in the assembled configuration, the probes contact the surface of the LGA adapter. The test board contains a ground plane under the shorting bar. The second figure shows the measurement of the unassembled adapter. The measurement of the adapter alone is used to calibrate out the fixture contribution.

Figure F-3. Inductance Measurement Fixture Cross-Section



F.3.1 Design Procedure for Inductance Measurements

The measurement equipment required to perform the validation is:

- HP8753D Vector Network Analyzer* or equivalent.
- Robust Probe Station (GTL4040)* or equivalent.
- Probes: GS1250 and GSG1250 Air-Co-Planar* or equivalent.
- Calibration: Cascade Calibration Substrates* or equivalent.
- Measurement objects: Sockets, motherboards.

F.3.1.1 Measurement Steps

1. Equipment setup:
   a. Cables should be connected to the network analyzer and to the probes using the appropriate torque wrench to ensure consistent data collection every time the measurement is performed.
2. Set VNA:
   a. Bandwidth = 300 KHz – 3 GHz with 801 points.
   b. Averaging Factor = 16.
3. Perform Open/Short/Load calibration:
   a. Calibration should be performed at the start of any measurement session.
   b. Create Calibration Kit if necessary for 1st time.
   c. Do not perform port extension after calibration.

4. Check to ensure calibration successfully performed.
5. Measure the inductance of the socket mounted to the motherboard fixture by probing the locations on the LGA Adapter and socket assembly.
   a. Call this $L_{socket\ assembly}$
   b. Export data into MDS/ADS or (capture data at frequency specified in item 6 of Table 4-1).
6. Measure the inductance of the motherboard fixture by probing on the pads.
   a. Call this $L_{sandwich}$
   b. Measure 30 units.
   c. The test board for 30 units must be chosen from different lots. Use five different lots, six units from each lot.
   d. Export data into MDS/ADS or (capture data at frequency specified in item 6 of Table 4-1).
   e. Calculate $\overline{L}_{sandwich}$
   f. For each socket unit, calculate:

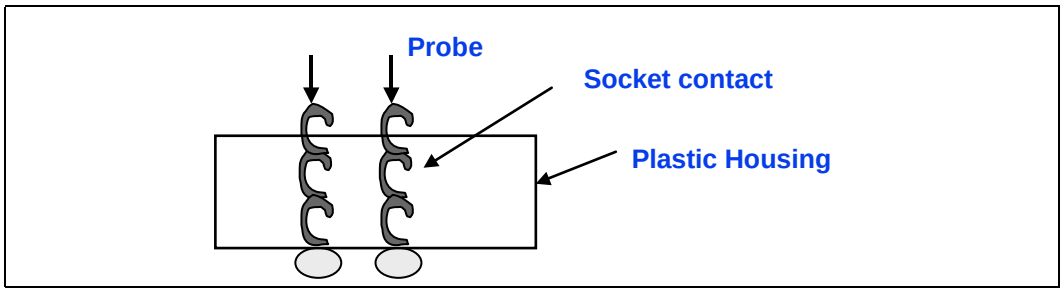
      $$L_{socket} = L_{socket\ assembly} - \overline{L}_{sandwich}$$

      It means $\overline{L}_{sandwich}$ will be subtracted from each $L_{socket\ assembly}$ and the result will be compared with spec value for each individual socket unit.

F.3.2 Correlation of Measurement and Model Data Inductance

To correlate the measurement and model data for loop inductance, one unit of measured socket assembly (socket and shorted test fixture) and one unit of measured sandwich (shorted test fixture) will be chosen for cross-sectioning. Both units will be modeled based on data from cross sectioning using Ansoft 3D*. The sandwich inductance will be subtracted from socket assembly inductance for both measured and modeled data. This procedure results in loop inductance for socket contact. This final result can be compared with the loop inductance from the supplier model for the socket. If there is any difference between them, it will be called the de-embedded correction factor. Adding the test board to the socket and then eliminating the contribution of the fixture creates this correction factor because inductance is not linear.

Figure F-4. Measurement Fixture Cross-Section



F.4 Dielectric Withstand Voltage

No disruptive discharge or leakage greater than 0.5 mA is allowed when subjected to 360 V RMS. The sockets shall be tested according to EIA-364, Test Procedure 20A, Method 1. The sockets shall be tested in fully mated condition. Barometric pressure shall be equivalent to Sea Level. The sample size is 25 contact-to-contact pairs on each of four sockets. The contacts shall be randomly chosen.

F.5 Insulation Resistance

The Insulation Resistance shall be greater than 800 MΩ when subjected to 500 V DC. The sockets shall be tested according to EIA-364, Test Procedure 21. The sockets shall be tested in fully mated condition. The sample size is 25 contact-to-contact pairs on each of 4 sockets. The contacts shall be randomly chosen.

F.6 Contact Current Rating

Measure and record the temperature rise when the socket is subjected to rate current of 0.8 A. The sockets shall be tested according to EIA-364, Test Procedure 70 A, Test Method 1.

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