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Intel® Pentium® 4 Processor and Intel® E7205 Chipset

Platform Design Guide

For Use with Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process

December 2002

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Revision History

Revision	Description	Date
–001	Initial release.	November 2002
-002	Corrected incorrect RCOMP Values from 24.9 Ohms to 32.4 ohms	December 2002

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Introduction 1

The *Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide* describes Intel's design recommendations for systems that are based on the Intel® Pentium® 4 processor with 512-KB L2 cache on 0.13 micron process and the Intel® E7205 chipset. The document provides motherboard design recommendations such as layout and routing guidelines, and addresses other system design issues such as power delivery. For specific design issues (e.g., thermal considerations), refer to the design guides and application notes listed in Section 1.1, "Reference Documentation".

In this document, "processor "and "chipset" refer to the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process and the E7205 chipset. Where a reference is intended to refer to a specific processor, the specific processor is listed.

The *Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide* has been developed to ensure maximum flexibility for board designers, while reducing board design risks. The design information provided in this document falls under one of the two following categories:

- *Design Recommendations.* These are items that are based on Intel's simulations and lab experience, are strongly recommended, and may be necessary to meet timing and signal quality specifications.

- *Design Considerations.* These are suggestions for platform design that provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel and should be used as examples, but may not be applicable to specific designs.

Note: The guidelines recommended in this document are based on experience, simulation, and validation work performed by Intel during development of Pentium 4 processors with 512-KB L2 cache on 0.13 micron process / E7205 chipset-based systems. This work is ongoing, and the recommendations are subject to change.

Platform schematics are included in Appendix A. The schematics are for a specific design implementation, but the core schematics remain the same for most platforms that are based on the chipset. The schematic set provides a reference schematic for each chipset component, as well as common motherboard options. Additional flexibility is possible through other permutations of these options and components.

1.1 Reference Documentation

Item	Location/Number
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Datasheet	298643
Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Thermal Design Guidelines	http://developer.intel.com/design/ Pentium4/guides/
Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Signal Integrity and Usage Guidelines	http://developer.intel.com/design/ Pentium4/devtools/
Intel® Pentium® 4 Processor 478-Pin Socket (mPGA478) Design Guidelines	http://www.intel.com/design/Pentium4/ guides/249890.htm
Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet	249887
Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines	249889
ITP700 Debug Port Design Guide	http://www.intel.com/design/Xeon/ guides/249679.htm
Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet	251937
Intel® E7205 and Intel® E7505 Length Matching Spreadsheet	Note 1
Intel® NetBurst™ Microarchitecture BIOS Writer's Guide	Note 1
Intel® Pentium® 4 Processor VR-Down Design Guidelines	Note 1
Voltage Regulator Module (VRM) 9.1 DC-DC Converter Design Guidelines	http://developer.intel.com/design/ Xeon/guides
PCI Local Bus Specification	http://www.pcisig.com/
PCI-PCI Bridge Specification	http://www.pcisig.com/
PCI Bus Power Management Interface Specification	http://www.pcisig.com/
PCI-X Specification	http://www.pcisig.com/
PCI Local Bus Specification Rev 2.2	http://www.pcisig.com/
Serial ATA Specification Rev 1.0	http://www.serialata.org/cgi-bin/ SerialATA10gold.zip
Sil3112 PCI to Serial ATA Controller Datasheet Rev 0.01	http://www.siliconimage.com/ home.asp
Intel® 82801DB I/O Controller Hub 4 (ICH4) Datasheet	http://www.intel.com/design/chipsets/ datashts/290744.HTM
AP-728 Intel® ICH Family Real Time Clock (RTC) Accuracy and Considerations under Test Conditions	http://www.intel.com/design/chipsets/ applnots/292276.htm
JEDEC DDR SDRAM Unbuffered DIMM Design Specification	www.jedec.org
JEDEC DDR SDRAM Unbuffered DIMM Design Specification Addendum	http://www.intel.com/technology/ memory/ddr/specs/ ddr200_unbuff_dimm_spec_09.htm
JEDEC DDR SDRAM Registered DIMM Design Specification	http://www.intel.com/technology/ memory/ddr/specs/ ddr200_reg_dimm_spec_10.html
DDR200 JEDEC Specification Addendum	http://www.intel.com/technology/ memory/pcsdram/spec/ ddr200_spec_10.htm

Item	Location/Number
82562ET 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet	http://fdbl.intel.com/servlet/ opencontentservlet?OBJID=09000d29 80129c13
CK408 Clock Synthesizer/Driver Specification	Note 1
AC '97 Component Specification, Revision 2.3	http://developer.intel.com/ial/ scalableplatforms/audio/
Communication and Network Riser Specification	http://developer.intel.com/technology/ cnr/index.htm
ATA/ATAPI-6 Standard	http://T13.org
Intel® BGA/OLGA Assembly Development Guide- NDA r1.4	Note 1
Accelerated Graphics Port Interface Specification 3.0, Revision 0.95	http://www.agpforum.org/
Low Pin Count Interface Specification, Revision 1.0	http://developer.intel.com/design/ chipsets/industry/lpc.htm
Universal Serial Bus 2.0 Specification	http://www.usb.org/
Advance Configuration and Power Interface (ACPI) Specification	http://www.teleport.com/~acpi/
Microsoft Windows* Logo Program System and Device Requirements	www.microsoft.com/hwdev/winlogo

NOTES:
1. Contact your Intel representative for the latest version of this item.

1.2   Terminology

This section defines conventions and terminology that is used throughout the design guide.

Term	Description
Aggressor	A network that transmits a coupled signal to another network.
AGTL+	The processor's system buses use a bus technology called AGTL+, or Assisted Gunning Transceiver Logic. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to assist the pull-up resistors during the first clock of a low-to-high voltage transition.
Asynchronous GTL+	Pentium 4 processors with 512-KB L2 cache on 0.13 micron process do not utilize CMOS voltage levels on any signals that connect to the processor. As a result, legacy input signals such as A20M#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#, SLP#, and STPCLK# utilize GTL+ input buffers. Legacy output FERR# and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) utilize GTL+ output buffers. All of these signals follow the same DC requirements as AGTL+ signals, however the outputs are not actively driven high (during a logical 0 to 1 transition) by the processor (the major difference between GTL+ and AGTL+). These signals do not have setup or hold time specifications in relation to HCLKINP/HCLKINN. However, all of the Asynchronous GTL+ signals are required to be asserted for at least two HCLKINs in order for the processor to recognize them.
Bus Agent	A component or group of components that, when combined, represent a single load on the AGTL+ bus.
Crosstalk	The reception on a victim network of a signal imposed by aggressor network(s) through inductive and capacitive coupling between the networks. • Backward Crosstalk - Coupling that creates a signal in a victim network that travels in the opposite direction as the aggressor's signal. • Forward Crosstalk - Coupling that creates a signal in a victim network that travels in the same direction as the aggressor's signal. • Even Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the same direction that the victim is switching. • Odd Mode Crosstalk - Coupling from a signal or multiple aggressors when all the aggressors switch in the opposite direction that the victim is switching.
Flip Chip Ball Grid Array (FCBGA)	Microprocessor packaging using "flip chip" design, where the processor is attached to the substrate face-down for better signal integrity, more efficient heat removal and lower inductance.
Flight Time	Flight time is a term in the timing equation that includes the signal propagation delay, any effects the system has on the Tco of the driver, plus any adjustments to the signal at the receiver needed to guarantee the setup time of the receiver. More precisely, flight time is defined as: • The time difference between a signal at the input pin of a receiving agent crossing the switching voltage (adjusted to meet the receiver manufacturer's conditions required for AC timing specifications; i.e., ringback, etc.) and the output pin of the driving agent crossing the switching voltage when the driver is driving a test load used to specify the driver's AC timings. • Maximum and Minimum Flight Time - Flight time variations are caused by many different parameters. The more obvious causes include variation of the board dielectric constant, changes in load condition, crosstalk, power noise, variation in termination resistance and differences in I/O buffer performance as a function of temperature, voltage, and manufacturing process. Some less obvious causes include effects of Simultaneous Switching Output (SSO) and packaging effects. • Maximum flight time is the largest acceptable flight time a network will experience under all conditions. • Minimum flight time is the smallest acceptable flight time a network will experience under all conditions.

Term	Description
ISI	Inter-symbol interference is the effect of a previous signal (or transition) on the interconnect delay. For example, when a signal is transmitted down a line, and the reflections due to the transition have not completely dissipated, the following data transition launched onto the bus is affected. ISI is dependent upon frequency, time delay of the line, and the reflection coefficient at the driver and receiver. ISI can impact both timing and signal integrity.
Network	The network is the trace of a Printed Circuit Board (PCB) that completes and electrical connection between two or more components.
Overshoot	The maximum voltage observed for a signal at the device pad, measured with respect to VCC_CPU.
Pad	The electrical contact point of a semiconductor die to the package substrate. A pad is only observable in simulations.
Pin	The contact point of a component package to the traces on a substrate, such as the motherboard. Signal quality and timings can be measured at the pin.
Power-Good	"Power-Good" or "PWRGOOD" (an active high signal) indicates that all of the system power supplies and clocks are stable. PWRGOOD should go active a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.
Ringback	The voltage that a signal changes to after reaching its maximum absolute value. Ringback may be caused by reflections, driver oscillations, or other transmission line phenomena.
System Bus	The System Bus is the microprocessor bus of the processor.
Setup Window	The time between the beginning of Setup to Clock (T_{SU_MIN}) and the arrival of a valid clock edge. This window may be different for each type of bus agent in the system.
SSO	Simultaneous Switching Output (SSO) effects are differences in electrical timing parameters and degradation in signal quality caused by multiple signal outputs simultaneously switching voltage levels in the opposite direction from a single signal or in the same direction. These are called odd mode and even mode switching, respectively. This simultaneous switching of multiple outputs creates higher current swings that may cause additional propagation delay ("push-out") or a decrease in propagation delay ("pull-in"). These SSO effects may impact the setup and/or hold times and are not always taken into account by simulations. System timing budgets should include margin for SSO effects.
Stub	The branch from the bus trunk terminating at the pad of an agent.
Trunk	The main connection, excluding interconnect branches, from one end agent pad to the other end agent pad.
Undershoot	The minimum voltage extending below VSS that is observed for a signal at the device pad.
VCC_CPU	VCC_CPU is the core power for the processor. The System Bus is terminated to VCC_CPU.
Victim	A network that receives a coupled crosstalk signal from another network is called the victim network.

1.3 System Overview

The E7205 chipset is designed for use with Pentium 4 processors with 512-KB L2 cache on 0.13 micron process. The architecture of the E7205 chipset provides the performance and feature-set required for single-processor based entry workstation system. Figure 1-1 illustrates an example processor / chipset system configuration for entry workstation platforms.

Figure 1-1. Example Processor / Chipset Based System Configuration
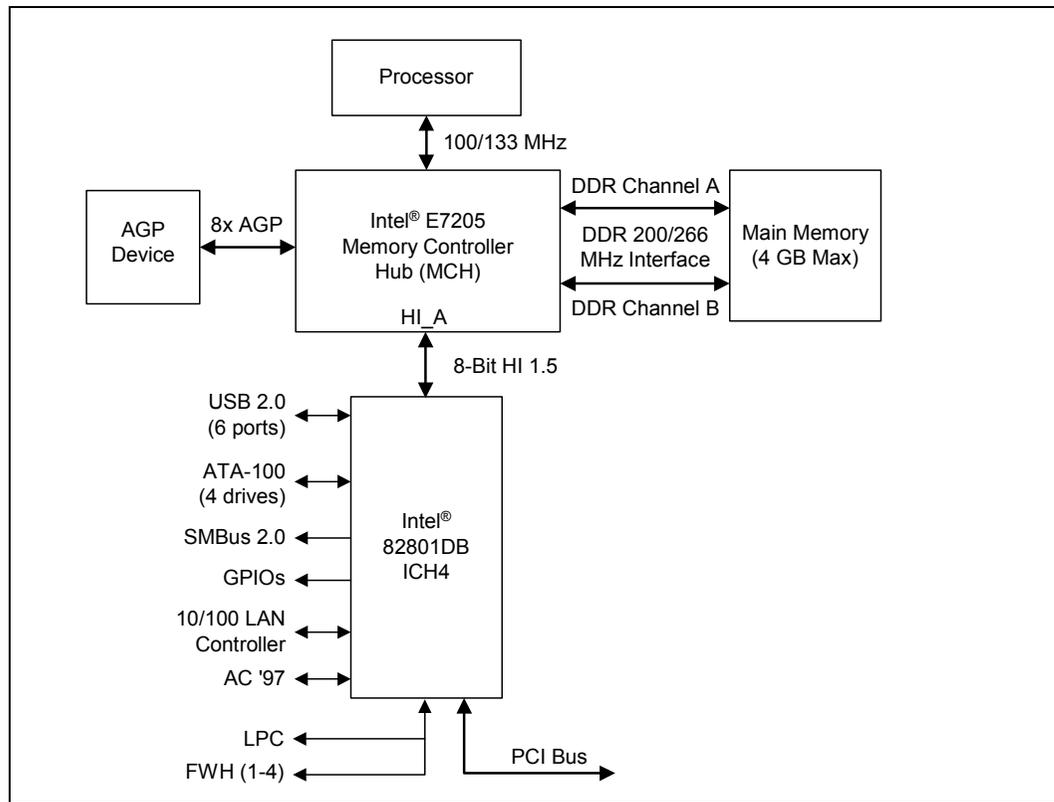
1.3.1 Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process is the next generation of the Pentium 4 processor in the 478-pin package with the Intel® NetBurst™ microarchitecture. The processor delivers performance levels that are significantly higher than previous generations of Intel® IA-32 processors. Table 1-1 describes the basic feature set of the processor.

Table 1-1. Intel® Pentium® 4 Processor Feature Set Overview

Feature	Intel® Pentium® 4 Processor
L2 Cache	512-KB
Data Bus Transfer Rate	4.27 GB/s
Package	mPGA478

The processor includes the following advanced microarchitecture features:

- Advanced Dynamic Execution
- Execution Trace Cache
- Streaming SIMD (single instruction, multiple data) Extensions 2
- Advanced Transfer Cache
- Enhanced floating point and multimedia engine

1.3.2   Intel® E7205 Chipset

The chipset consists of two major components: the Memory Controller (MCH), and the I/O Controller 4 (ICH4). The chipset components communicate via the hub interface (HI).

The MCH is a 1005-ball FC-BGA package and contains the following functionality:

- System Bus Features:
  — Supports single processor at 533 MHz
  — System bus bandwidth of 4.27 GB/s
  — Supports 36-bit system bus addressing model
  — 12 deep in-order queue, 1-deep defer queue
- Memory Bus Features:
  — 144-bit wide, DDR266 (PC2100) memory interface Memory bandwidth of 4.27 GB/s or 3.2 GB/s.
  — Supports non-ECC (x64) and ECC (x72) DDR266 DIMMs using 128-Mb, 256-Mb, and 512-Mb DRAMs
  — Supports a maximum of 4 GB of memory
  — Supports S4EC/D4ED ECC
  — Supports up to 16 simultaneous open pages
- AGP 8X Bus Features
  — Single AGP device
  — AGP interface asynchronously coupled to core
  — AGP 3.0 Specification
  — 8X or 4X at 0.8 V (AGP 3.0) electrical characteristics
  — 4X, 2X, or 1X at 1.5 V (AGP 2.0) electrical characteristics
  — 0.8 V and 1.5 V AGP electrical. No 3.3 V support
  — 32-deep AGP request queue
  — 32-bit upstream address support for inbound AGP and PCI cycles
  — 32-bit downstream address support for outbound PCI and Fast Write cycles
- I/O Features
  — Provides HI1.5 Connection for ICH4
    - HI1.5 = HI1.0 protocols with HI2.0 electrical characteristics
    - 266 MB/s point-to-point connection for ICH4 with parity protection
    - 8-bit wide, 66 MHz base clock, 4X data transfer
    - Parallel termination mode for longer trace lengths
    - 64-bit inbound addressing, 32-bit outbound addressing

1.3.2.1 Intel® I/O Controller Hub 4 (ICH4)

The I/O Controller Hub (ICH4) provides the legacy I/O subsystem for E7205 chipset-based platforms. Additionally, it integrates many advanced I/O functions. The ICH4 includes the following features:

- Provides HI1.5 Connection to MCH
  - 266 MB/s point-to-point connection for ICH4 with parity protection
  - 8-bit wide, 66 MHz base clock, 4X data transfer
  - Parallel termination mode for longer trace lengths
  - 64-bit inbound addressing, 32-bit outbound addressing
- 2-channel Ultra ATA/100 bus master IDE controller
- 3 Universal Host Controller Interface (UHCI) USB host controllers (capabilities for six ports)
- I/O APIC
- SMBus 2.0 controller
- LPC interface
- AC '97 2.3 interface
- PCI 2.2 interface
- Integrated LAN Controller

1.3.3 Processor Support

Table 1-2 provides a summary of the supported processor configurations for the chipset-based platform.

Table 1-2. Supported Processor Configurations

Processor System Bus (MHz)	Installed Memory	Allowable	Comment
400	DDR200	Yes	Validated
400	DDR266	Yes	Validated
533	DDR200	No	Not validated
533	DDR266	Yes	Validated

1.3.4   DIMM Support

Table 1-3 provides a summary of the supported memory configurations for the chipset-based platform.

Table 1-3. DIMM Support Summary

Type	Unbuffered
Dual Channel	1 to 2 pairs of DIMMs (4 rows)

1.3.5   Bandwidth Summary

Table 1-4 describes the clock speed, sample rate, and bandwidth for each interface in the chipset-based platform.

Table 1-4. Platform Bandwidth Summary

Interface	Clock Speed (MHz)	Samples per Clock	Data Width (Bytes)	Bandwidth (MB/s)
System Bus (Data)	133	4	8	4200
System Bus (Address)	133	2	4	1066
DDR Interface	133	2	16	4200
DDR Interface	100	2	16	3200
Hub Interface	66	4	1	266
AGP 8X	66	8	4	2032

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Component Quadrant Layout **2**

The quadrant layout figures below do not show the exact component ball count—only the general quadrant information. Use only the exact ball assignment to conduct a routing analysis. Reference the following documents for ball assignment information:

- *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet*

- *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet*

- *Intel® I/O Controller Hub 4 (ICH4) Datasheet*

Note: All figures in this section show the top view.

2.1 Intel® Pentium® 4 Processor Quadrant Layout

Figure 2-1 illustrates the quadrant layout of the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

Figure 2-1. Intel® Pentium® 4 Processor Quadrant Layout (Top View)
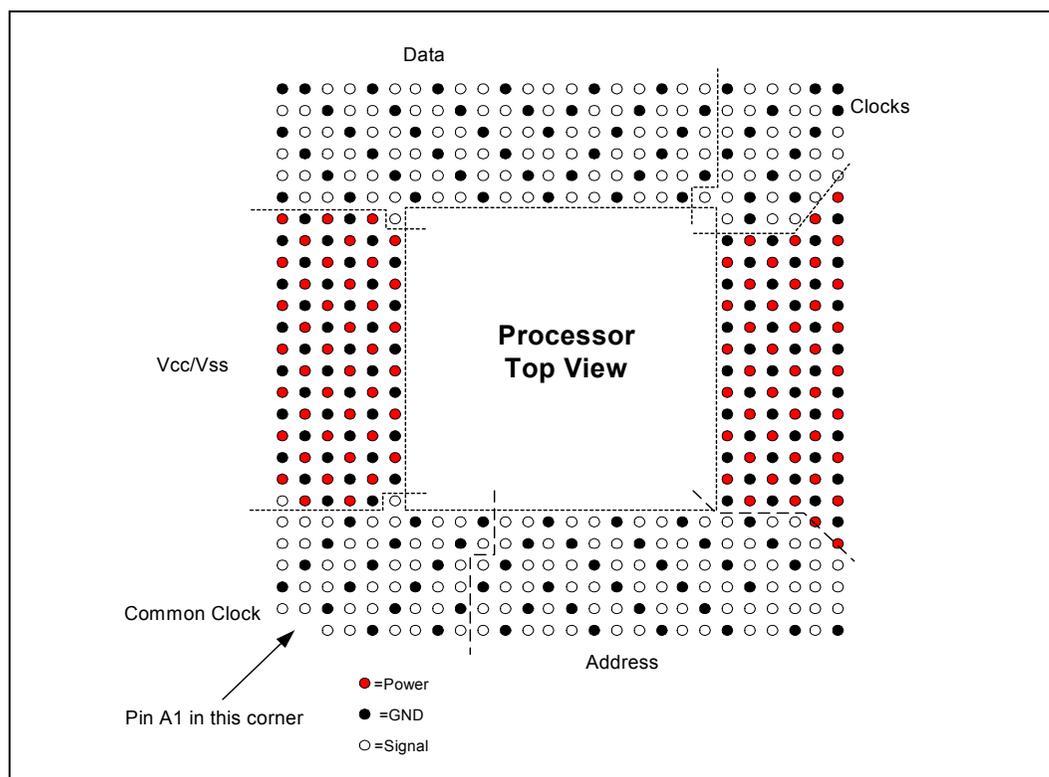
2.2 MCH Quadrant Layout

Figure 2-2 illustrates the quadrant layout for the MCH chipset component.

Figure 2-2. MCH Quadrant Layout (Top View)
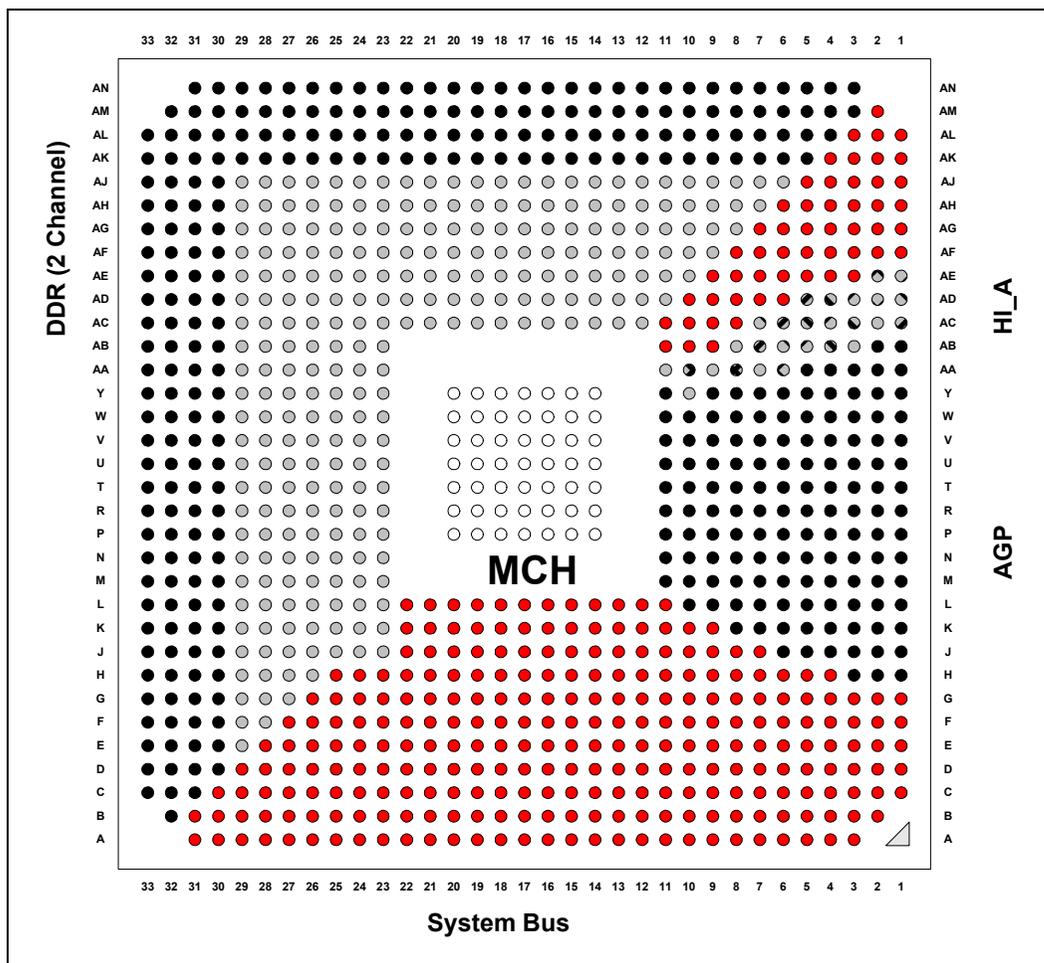
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2.3 Intel® ICH4 Quadrant Layout

Figure 2-3 shows the quadrant layout for the Intel® 82801CA ICH4 chipset component.

Figure 2-3. Intel® ICH4 Quadrant Layout (Top View)
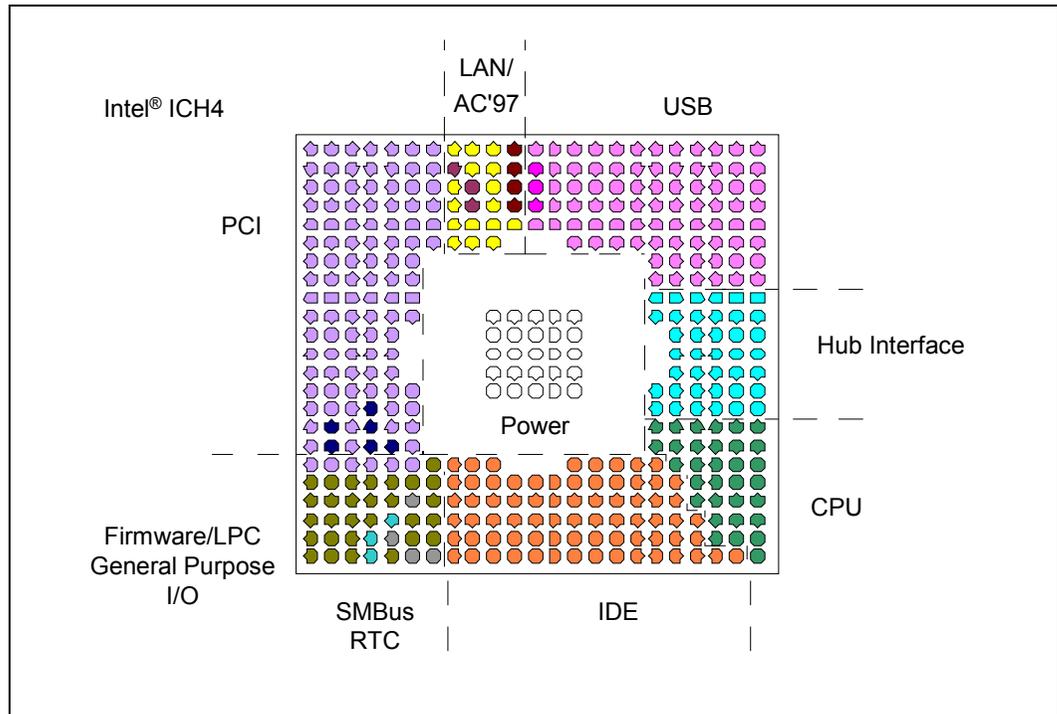
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Platform Stack-Up and Component Placement Overview 3

3.1 Platform Component Placement

Figure 3-1 illustrates the general component placement for the processor/chipset-based customer reference platform. Table 3-1 lists the assumptions used for the component placement.

Table 3-1. Assumptions for System Placement Example

System Configuration	Assumptions		
	Form Factor	Number of PCB Layers	Assembly
Entry Workstation (UP)	ATX (12" x 9.6")	6	Single Sided

Figure 3-1. Intel® Pentium® 4 Processor / Intel® E7205 Chipset-Based System Placement Example
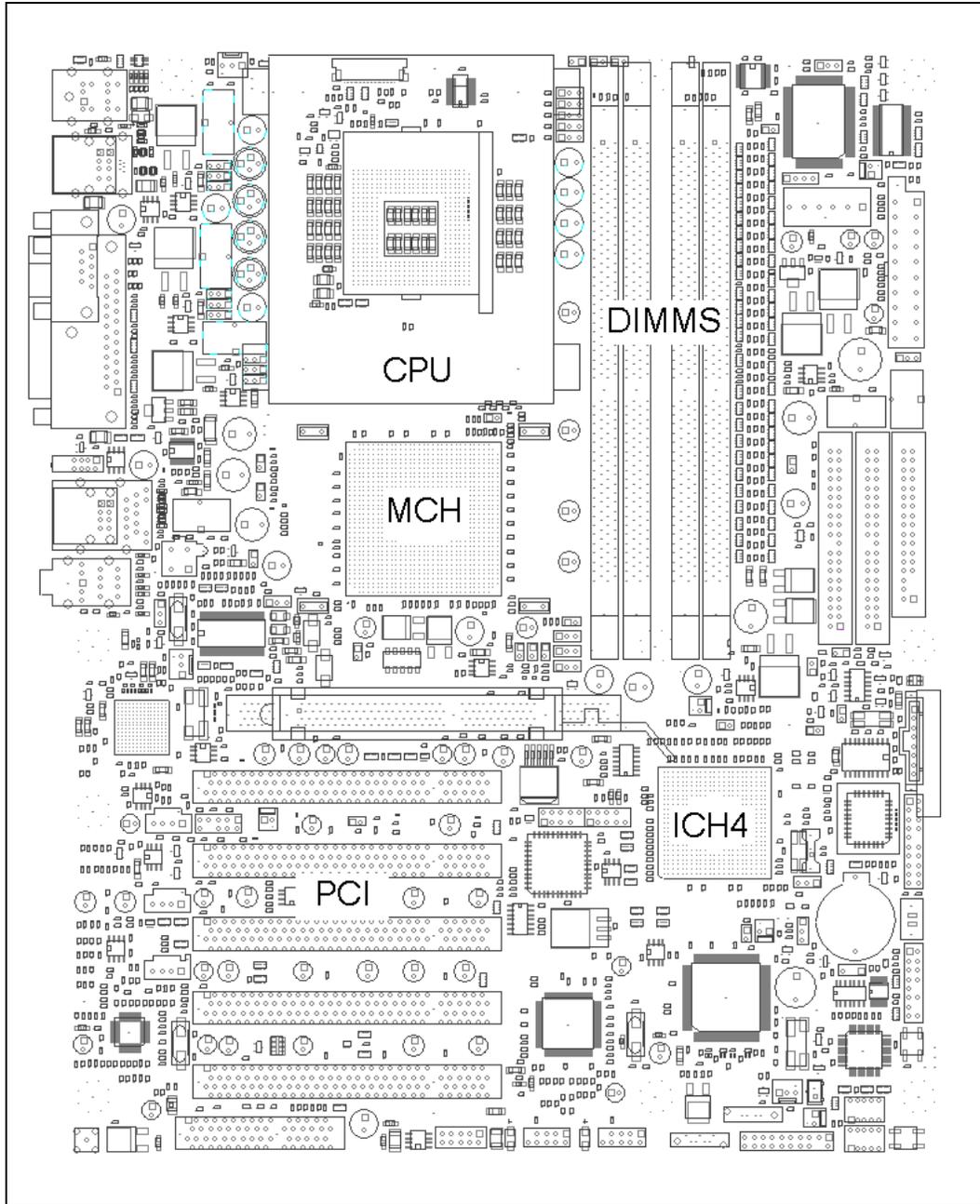
3.2 Platform Stack-Up

Figure 3-2 shows the recommended platform stack-up. All internal layers are 1 oz. copper. Top and bottom layers are 0.5 oz. not including the plating. Because of the stackup, some signals will be routed stripline and/or microstrip. Layer 1, layer 4, and the bottom layer are used for signal routing with all three layers providing ground referencing.

Intel strongly recommends that system designers use the stack-up shown in Figure 3-2. Intel encourages platform designers to perform comprehensive simulation analysis to ensure all timing specifications will be met. This is particularly important if a design deviates from the design guidelines provided.

Figure 3-2. Board Stack-Up

		Layer Thickness	Copper Weight
Top	SIGNAL	2.1	0.5 oz plus plating
	PREPREG	4.0	
Layer 2	GND	1.2	1 oz.
	CORE	4.3	
Layer 3	POWER	1.2	1 oz.
	PREPREG	6.5	
	CORE	23.0	
	PREPREG	6.5	
Layer 4	SIGNAL	1.2	1 oz.
	CORE	4.3	
Layer 5	GND	1.2	1 oz.
	PREPREG	4.0	
Bottom	SIGNAL	2.1	0.5 oz plus plating
Panel Thickness (mils) =		61.6	Assumes finished thickness on µStrip Layers

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Platform Clock Routing Guidelines   **4**

To minimize jitter, improve routing, and reduce cost, E7205 chipset-based systems will use a single-chip clock solution, the CK408. The CK408 provides three 133/100 MHz differential output pairs for all of the bus agents, and six 66 MHz speed clocks that drive all I/O buses. Figure 4-1 shows the implementation of the bus clocks for this configuration. For more information on CK408, refer to the *CK408 Clock Synthesizer/Driver Specification*.

Table 4-1. Intel® E7205 Chipset Clock Group

Clock Name	Frequency (MHz)	Receiver
Host_CLK	133/100	Processor, MCH, Debug Port
CLK66	66	MCH, Intel® ICH4, AGP
CLK33	33	PCI Connector, ICH4, SIO, FWH
CLK14	14.318	ICH4, SIO
USBCLK	48	ICH4

Table 4-2. Platform System Clock Cross-Reference

Clock Group	CK-408	Component	Component Pin Name
HOST_CLK	CPU#	Debug Port	BCLK0
	CPU	Debug Port	BCLK1
	CPU#	Processor	BCLK0
	CPU	Processor	BCLK1
	CPU#	MCH	HCLKINN
	CPU	MCH	HCLKINP
CLK66	3V66_4	AGP	AGPCLK
	3V66_3	Port 80	N/A
	3V66_2	Intel® ICH4	CLK66
	3V66_1	MCH	GCLKIN
	3V66_0	Test Point	N/A
CLK33	PCI_33MHz	Slot 4	CLK
		Slot 5	CLK
		FWH. LPC	CLK, CLK
		SIO, Glue Chip	CLOCKI, CLK_IN
		SATA, 1394	PCI_CLK, PCI_PCLK
		LAN	P_CLK
		ICH4	PCICLK
	PCIclkF	Slot 3	CLK
		Slot 2	CLK
		Slot 1	CLK
CLK14	REF0	Audio	BIT_CLK
		ICH4	CLK14
		SIO	CLOCKI
USBCLK	USB48MHz	ICH4	CLK48

Figure 4-1. Intel® E7205 Chipset-Based System Clocking Diagram
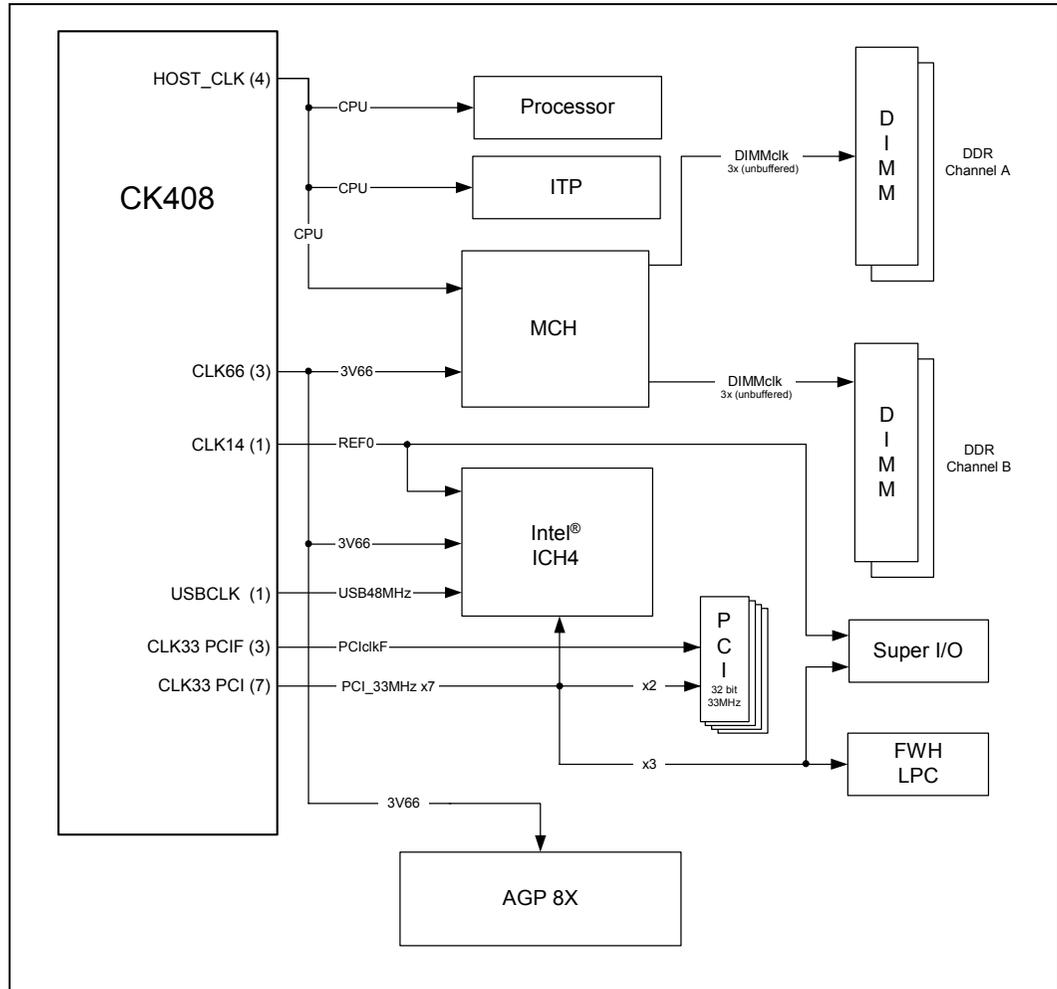
4.1 Clock Groups

4.1.1 HOST_CLK Clock Group

4.1.1.1 HOST_CLK Clock Topology

The CK408 clock synthesizer provides three sets of 133/100 MHz differential clock outputs. The differential clocks are driven to the processors, the chipset, and the debug port as shown in Figure 4-1.

The clock driver differential bus output structure is a "Current Mode Current Steering" output, which develops a clock signal by alternately steering a programmable constant current to the external termination resistors, R_T. The resulting amplitude is determined by multiplying I_{OUT} by the value of R_T. The current I_{OUT} is programmable by a resistor and an internal multiplication factor so that the amplitude of the clock signal can be adjusted for different values of R_T to match impedances and to accommodate future load requirements.

The recommended termination for the differential bus clock is a "Shunt Source Termination." Refer to Figure 4-2 for an illustration of this termination method. Parallel R_T resistors perform a dual function—they convert the current output of the clock driver into a voltage, and they match the driver output impedance to the transmission line. The series resistors, R_S, provide isolation from the clock driver's output parasitics, which would otherwise appear in parallel with the termination resistor, R_T.

The value of R_T should be selected to match the characteristic impedance of the motherboard, and R_S should be between 20 Ω and 33 Ω. Simulations have shown that R_S values above 33 Ω provide no benefit to signal integrity and only degrade the edge rate.

Figure 4-2. Source Shunt Termination
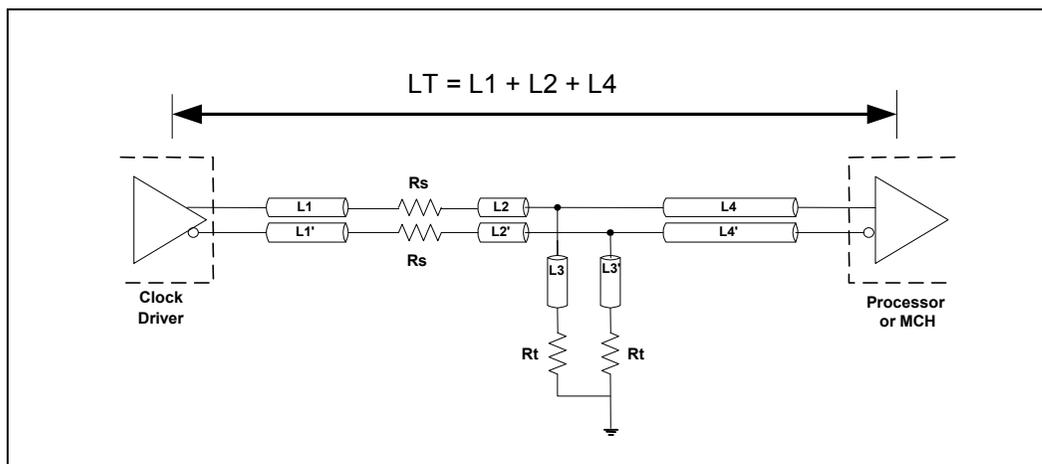
Table 4-3. HOST_CLK Routing Guidelines

Layout Guideline	Value	Illustration	Notes
HCLKIN skew between agents	300 ps total Budget: 150 ps for clock driver 150 ps for interconnect	Figure 4-2 and Figure 4-4	1,2,3,4
Differential pair spacing	20 – 25 mils	Figure 4-5	5,6
Spacing to other traces	25 mils	Figure 4-5	
Serpentine spacing	Maintain a minimum S/h ratio of > 5/26 Keep parallel serpentine sections as short as possible. Minimize 90 degree bends. Make 45 degree bends, if possible.	Figure 4-5	
Motherboard impedance – differential	100 Ω typical		8
Motherboard impedance – single ended	50 Ω ± 10%		9
Processor routing length – L1, L1': Clock driver to R_S	0.5 inch max	Figure 4-2	13
Processor routing length – L2, L2': R_S to R_S-R_T node	0 – 0.2 inch"	Figure 4-2	13
Processor routing length – L3, L3': R_S-R_T node to R_T	0 – 0.2 inch	Figure 4-2	13
Processor routing length – L4, L4': R_S-R_T Node to Load	0 – 10 inches	Figure 4-2	
MCH routing length – L1, L1': Clock Driver to R_S	0.5 inch max	Figure 4-2	13
MCH routing length – L2, L2': R_S to R_S-R_T node	0 – 0.2 inch	Figure 4-2	13
MCH routing length – L3, L3': R_S-R_T node to R_T	0 – 0.2 inch	Figure 4-2	13
MCH routing length – L4, L4': R_S-R_T Node to Load	0 – 10 inches	Figure 4-2	
Processor to CS length matching (LT)	0.282 inch ± 0.010 inch Chipset LT must be 0.282 inch longer than Processor LT	Figure 4-2	10
Processor to processor length matching (LT)	± 10 mils	Figure 4-2	15
HCLKINP – HCLKINN length matching	± 10 mils		
R_S series termination value	33 $\Omega \pm 5\%$	Figure 4-2	11
R_T shunt termination value	49.9 Ω± 1% (for 50 Ω MB impedance)	Figure 4-2	12

NOTES:
1. The skew budget includes clock driver output pair to output pair jitter (differential jitter), clock skew due to interconnect process variation, and static skew due to layout differences between clocks to all bus agents.
2. This number does not include clock driver common mode (cycle to cycle) jitter or spread spectrum clocking.
3. The interconnect portion of the total budget for this specification assumes that clock pairs are routed on multiple routing layers and are routed no longer than the maximum recommended lengths.
4. Skew measured at the load between any two-bus agents. Measured at the crossing point.

5. Edge to edge spacing between the two traces of any differential pair. Uniform spacing should be maintained along the entire length of the trace.
6. Clock traces are routed in a differential configuration. Maintain the minimum recommended spacing between the two traces of the pair. Do not exceed the maximum trace spacing because this will degrade the noise rejection of the network.
7. Set line width to meet correct motherboard impedance. The line width value provided here is a recommendation to meet the proper trace impedance based on the recommended stack up.
8. The differential impedance of each clock pair is approximately 2*Zsingle-ended*(1-2*Kb) where Kb is the backwards crosstalk coefficient. For the recommended trace spacing, Kb is very small and the effective differential impedance is approximately equal to 2 times the single-ended impedance of each half of the pair.
9. The single ended impedance of both halves of a differential pair should be targeted to be of equal value. They should have the same physical construction. If the HCLKIN traces vary within the tolerances specified, both traces of a differential pair must vary equally.
10. Length compensation for the processor socket and package delay is added to chipset routing to match electrical lengths between the chipset and the processor from the die pad of each. Therefore, the motherboard trace length for the chipset will be longer than the trace length for the processor.
11. Rs values between 20 Ω – 33 Ω have been shown to be effective.
12. R_T shunt termination value should match the motherboard impedance.
13. Minimize L1, L2 and L3 lengths. Long lengths on L2 and L3 degrade effectiveness of source termination, and contribute to ring back.
14. The goal of constraining all bus clocks to one physical routing layer is to minimize the impact on skew due to variations in Er, and the impedance variations due to physical tolerances of circuit board material.
15. Length of LT for one processor must match the LT of all other HCLKIN traces to other processor with specific tolerance.

Figure 4-3. Length Matching of Host Clocks (with Package Compensation)
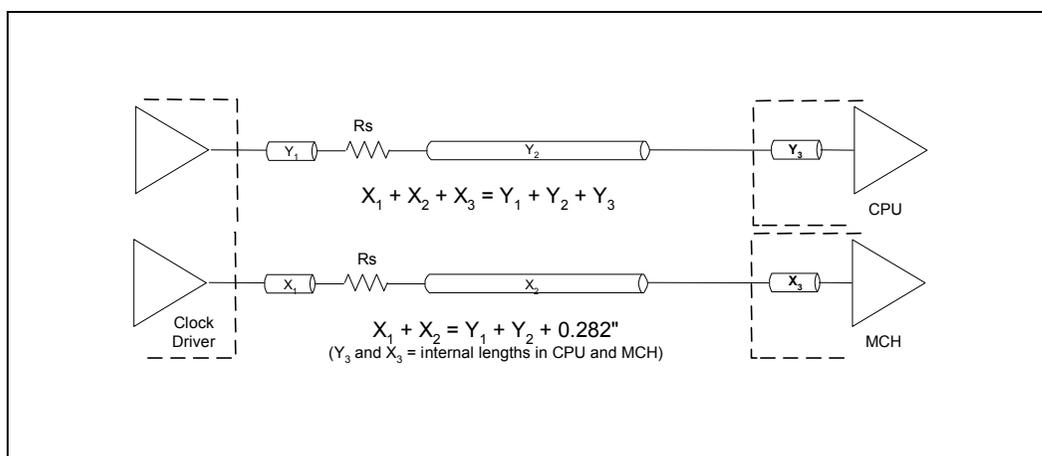
It's important that the host clocks from the clock pin to the processor silicon match the length from the clock pin to the MCH silicon. Package compensation is optional, but can be accommodated very easily.

The In-Target Probe clock lengths require a defined relationship to the processor and MCH host clock lengths. For more information on this relationship, refer to *ITP700 Debug Port Design Guide* (available at http://www.intel.com/design/Xeon/guides/249679.htm) for the design of your platform.

Figure 4-4. Clock Skew As Measured from Agent to Agent
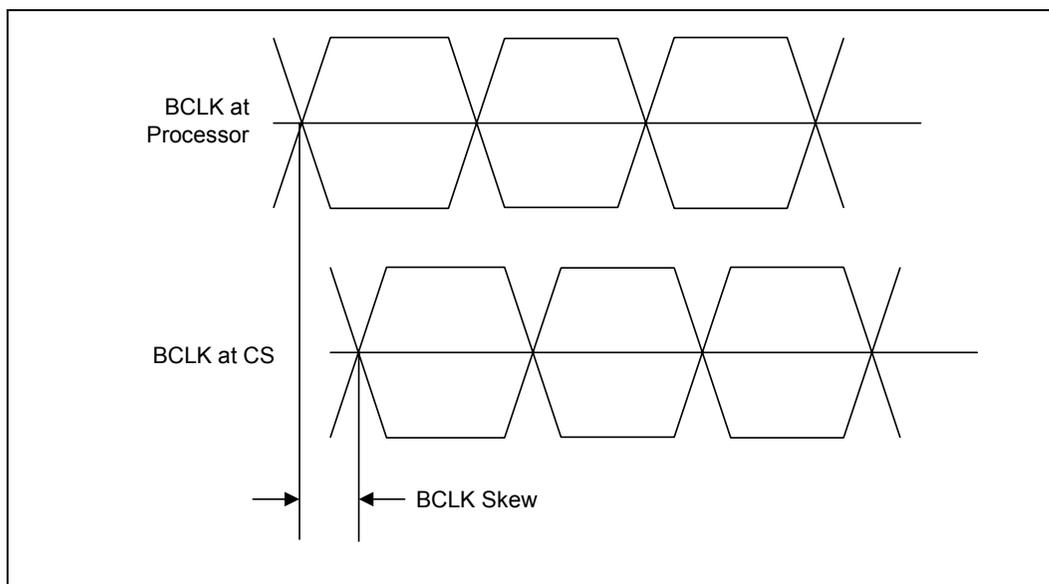
Figure 4-5. Trace Spacing
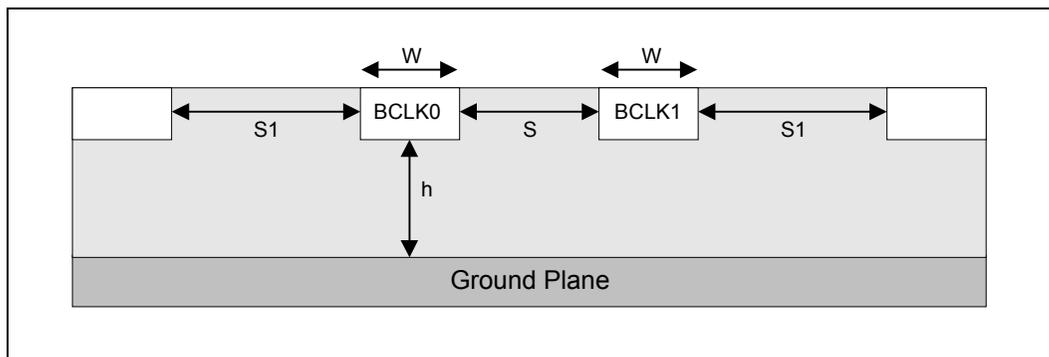
4.1.1.2   HOST_CLK General Routing Guidelines

- When routing the differential clocks, do not split up the two halves of a differential clock pair between layers, and route to all agents on the same physical routing layer referenced to ground.

- If a layer transition is required, make sure that the skew induced by the vias used to transition between routing layers is compensated in the traces to other agents.

- Do not place vias between adjacent complementary clock traces, and avoid differential vias. Vias placed in one half of a differential pair must be matched by a via in the other half. Differential vias can be placed within length L1, between clock driver and R_S, if needed to shorten length L1.

4.1.2   CLK66 Group

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the MCH, ICH4, and AGP.

Figure 4-6. Topology for CLK66
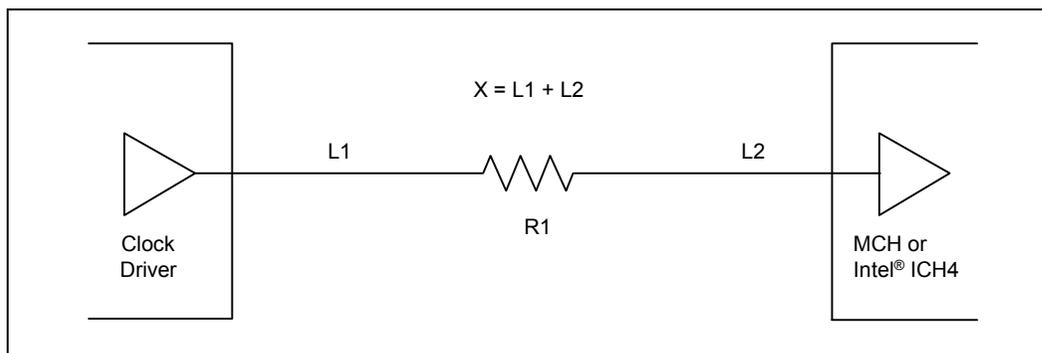
Table 4-4. CLK66 Routing Guidelines

Parameters	Routing Guidelines
Clock Group	CLK66
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, and 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 9.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The CLK66 group should minimize skew (~0) between each other.
Clock Driver to MCH	X (X can be between 3 inches– 9.5 inches)
Clock Driver to Intel® ICH4	X
Clock Driver to AGP connector	X – 4.6 inches (4 inches add-in card clock length plus 0.6 inch approximation for connector delay)

4.1.2.1   CLK66 Group to AGP Connector

The driver is the clock synthesizer's 66 MHz clock output buffer, and the receiver is the 66 MHz clock input buffer at the AGP device. Use these guidelines when routing to an AGP connector.

Figure 4-7. Topology for CLK66 to AGP Connector
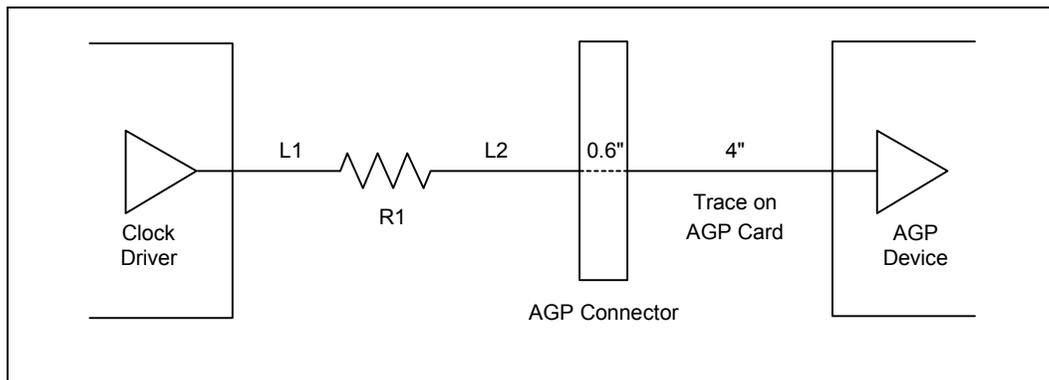
Table 4-5. CLK66 Routing Guidelines (for AGP Connector)

Parameters	Routing Guidelines
Topology	Point-to-point
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Spacing to Other Traces	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	MCH 66 MHz Clock – L1 – 4.6 inches
AGPCLK Total Length (L1+L2)	MCH 66 MHz Clock – 4.6 inches (Must be matched to ± 100 mils of the CLK66 total length)
Resistor	R1 = 33 Ω ± 5%

4.1.2.2   CLK66 Skew Requirements

All 66 MHz clock lengths require length matching. All devices down on the motherboard must have matching clock lengths. The AGP connector is equivalent approximately to 0.6 inch of trace, and 4 inches of clock trace exists on the add-in card. Therefore, the AGP clock is routed 4.6 inches shorter than the clocks to down devices (See Figure 4-8).

The skew between clocks can be further reduced by including the package lengths internal to the MCH and ICH4 in the length matching equations. This is not a requirement, but improves timing margins. Figure 4-9 shows the relationship between the 66 MHz clocks when accounting for internal package lengths.

Figure 4-8. Clock Skew and Tracing Requirements (Without Package Compensation)
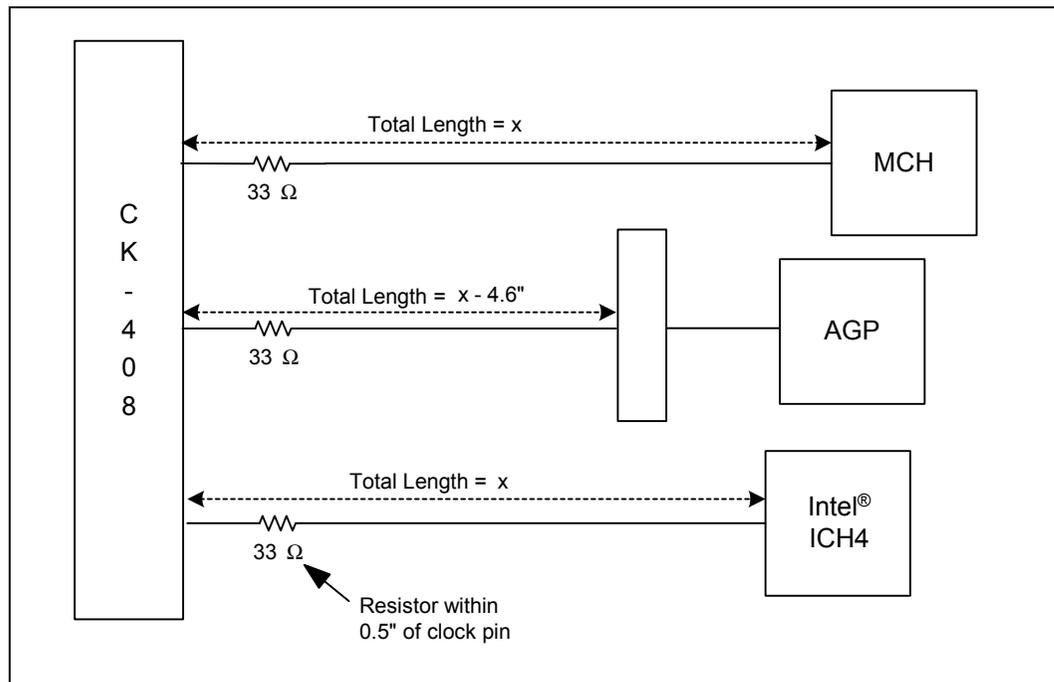
Figure 4-9. Clock Skew and Trace Requirements (With Package Compensation)
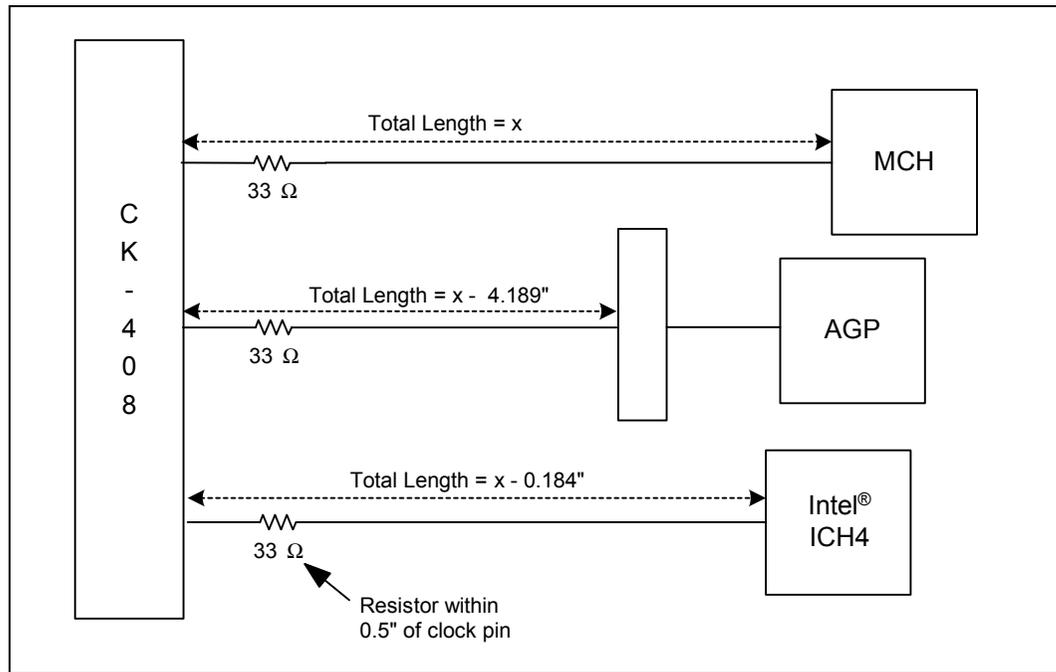
4.1.3 CLK33 Clock Group

The driver is the clock synthesizer's 33 MHz clock output buffer, and the receiver is the 33 MHz clock input buffer at the PCI devices on the PCI cards.

Figure 4-10. Topology for CLK33 to PCI Device Down
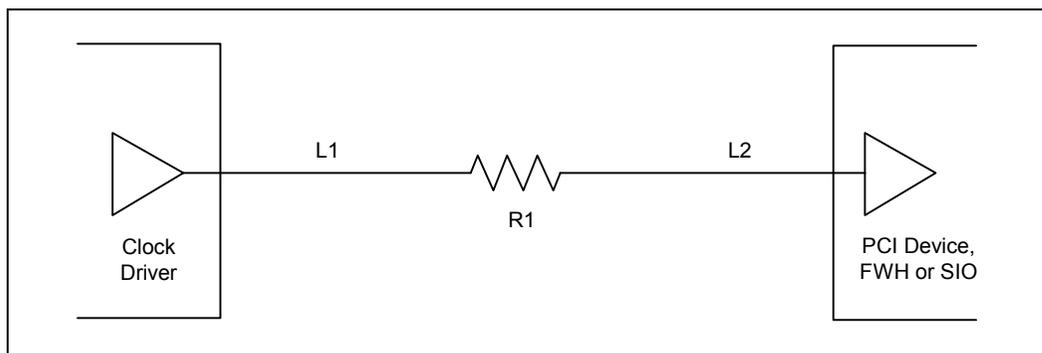
Table 4-6. CLK33 Routing Guidelines (PCI Device Down)

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point-to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1[1]
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Spec is 2 ns. All PCI devices must be within 2 ns of Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore, up to ± 1 ns may be used to ease routing.

NOTES:
1. The 66 MHz total clock length must equal the 33 MHz total clock length, which is a requirement of the ICH4.
2. The designer must ensure that the total device to device skew on PCI bus does not exceed 2 ns including clock generator skew.

Figure 4-11. Topology for CLK33 to PCI Connector
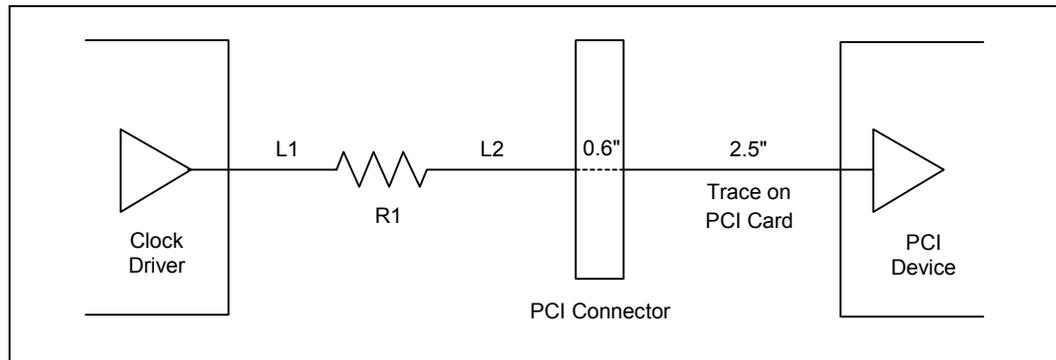
Table 4-7. CLK33 Routing Guidelines (for PCI Connector)

Parameter	Routing Guidelines
Clock Group	CLK33
Topology	Point- to-Point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50 inch
Trace Length – L2	ICH 66 MHz Clock – L1 – 3.1"
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	The maximum PCI device to PCI device skew allowed by the PCI Spec is 2 ns. All PCI devices must be within 2 ns of the Intel® ICH4 clock. The clock generator spec allows for 500 ps skew; therefore, up to ± 1 ns may be used to ease routing.

4.1.3.1 CLK33 Skew Requirements

All 33 MHz clocks to PCI devices must match in length. In addition, the 33 MHz clock to the ICH4 must match the length of the 66 MHz clock to the ICH4. The PCI connector is equivalent to approximately 0.6 inch of trace, and 2.5 inches of clock trace exists on the add-in card. Therefore, the clock to PCI slots is required to be 3.1 inches shorter than the clocks to down devices to ensure that the length from the clock chip to all PCI devices is equal.

The skew between clocks can be further improved by including the package lengths internal to the MCH and ICH4. This is not a requirement, but improves timing margins. Figure 4-13 shows the relationship between the 33 MHz clocks when accounting for internal package lengths.

Figure 4-12. Clock Skew and Tracing Requirements (Without Package Compensation)
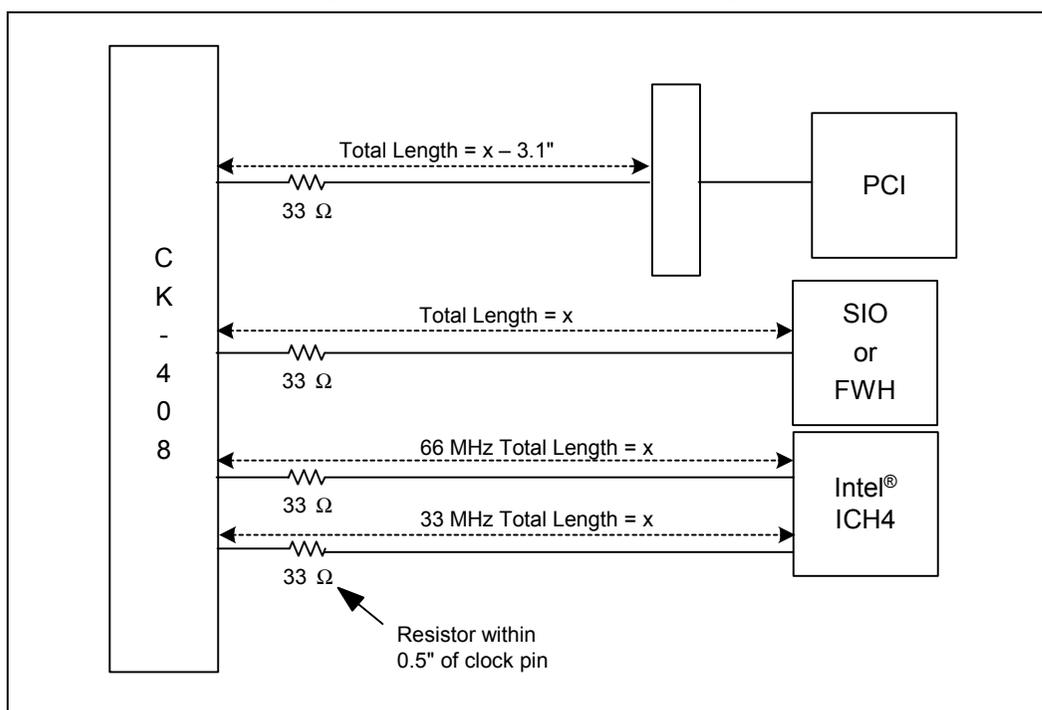
Figure 4-13. Clock Skew and Trace Requirements (With Package Compensation)
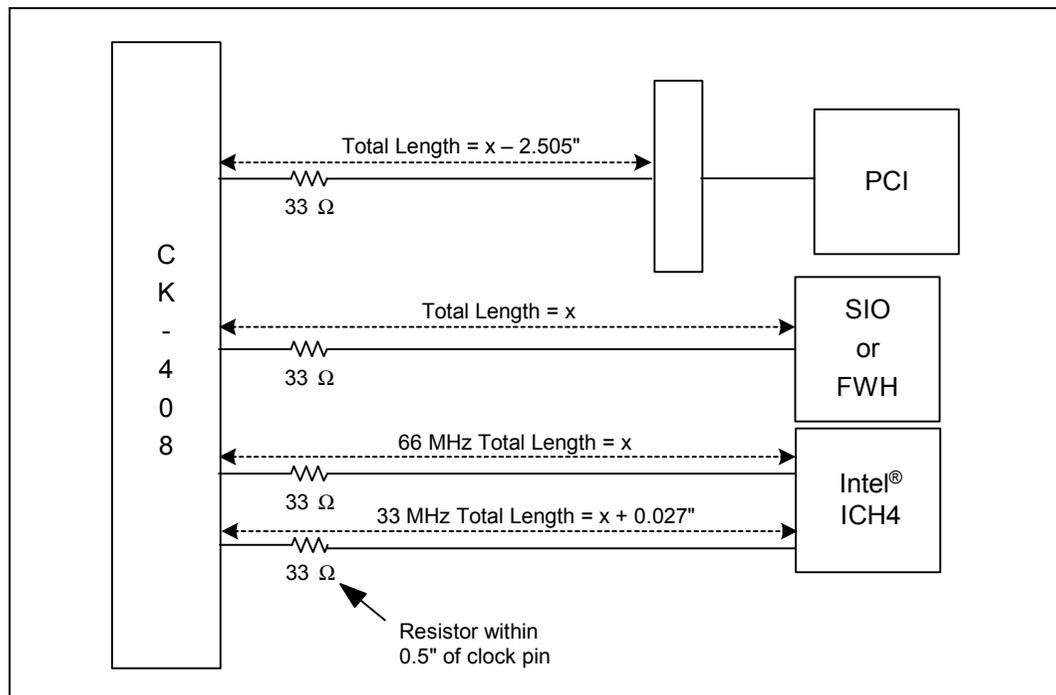
4.1.4   CLK14 Clock Group

The driver is the clock synthesizer's 14.318 MHz clock output buffer, and the receiver is the 14.318 MHz clock input buffer at the ICH4 and SIO.

Figure 4-14. Topology for CLK14
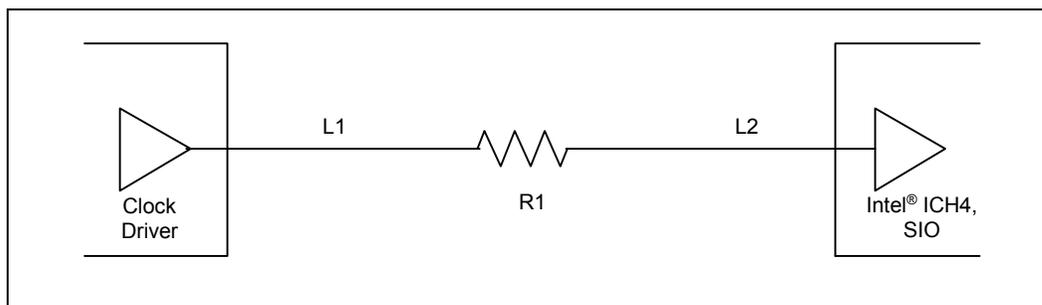
Table 4-8. CLK14 Routing Guidelines

Parameter	Routing Guidelines
Clock Group	CLK14
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 – 0.50"
Trace Length – L2	3.00 – 9.00"
Resistor	R1 = 33Ω ± 5%
Skew Requirements	Should have minimal skew (~ 0) between each other. However, each of the clocks in this group is asynchronous to clocks of any other group.

4.1.5 USBCLK Clock Group

The driver is the clock synthesizer's USB clock output buffer, and the receiver is the USB clock input buffer at the ICH4.

Figure 4-15. Topology for USB_CLK
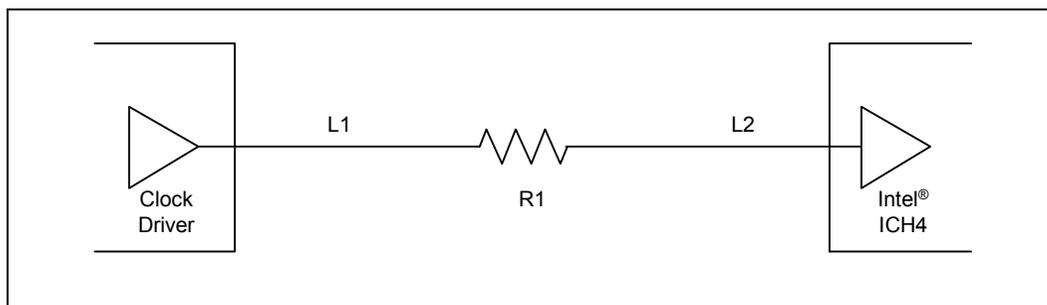
Table 4-9. USBCLK Routing Guidelines

Parameter	Routing Guidelines
Clock Group	USBCLK
Topology	Point-to-point
Reference Plane	Ground Referenced (contiguous over entire length)
Characteristic Trace Impedance (Z_0)	50 Ω ± 10%
Trace Width	6 mils on external layers, 5 mils on internal layers
Trace Spacing	25 mils
Trace Length – L1	0.00 inch – 0.50 inch
Trace Length – L2	3.00 inches – 12.00 inches
Resistor	R1 = 33 Ω ± 5%
Skew Requirements	None – USBCLK is asynchronous to any other clock on the board.
Maximum Via Count per Signal	2

4.2 Clock Driver Decoupling

The decoupling requirements for a CK408 compliant clock synthesizer are as follows:

- One 22 µF polarized (decoupling) cap placed close to the V_{DD} generation circuitry.

- Eleven 0.1 µF high-frequency decoupling caps placed close to the V_{DD} pins on the Clock driver.

- Three 0.1 µF high-frequency decoupling caps placed close to the V_{DDA} pins on the Clock driver.

- One 10 µF polarized (decoupling) cap placed close to the V_{DDA} pins on the Clock driver.

- One 0.1 µF high-frequency decoupling cap placed close to the V_{DDA} generation circuitry.

- All decoupling caps should be placed close to the Clock driver pins. Refer to Figure 4-16.

Figure 4-16. Decoupling Capacitors Placement and Connectivity
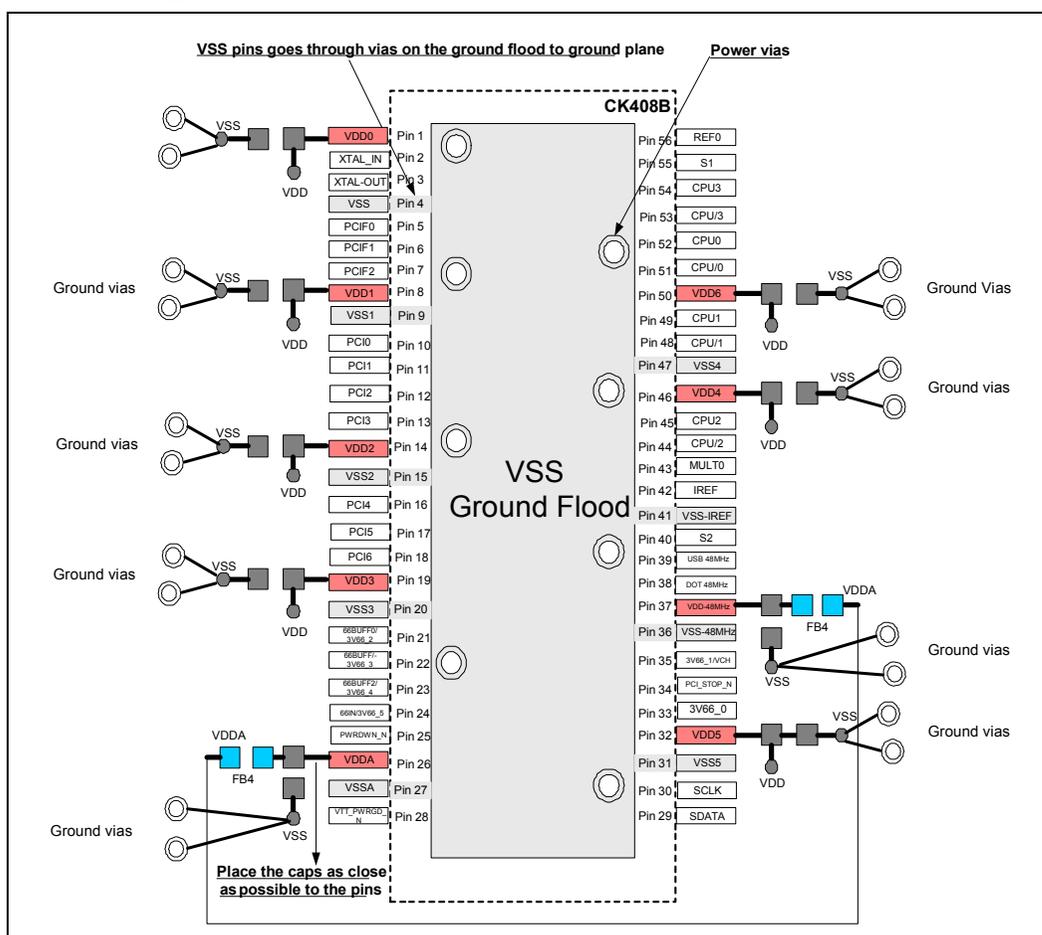
4.3 Clock Driver Power Delivery

Special care must be taken to provide a quiet V_{DDA} supply to the Ref V_{DD}, V_{DDA} and the 48 MHz V_{DD}. These V_{DDA} signals are especially sensitive to switching noise induced by the other V_{DD}s on the clock chip. They are also sensitive to switching noise generated elsewhere in the system, such as CPU VRM. It is recommended that a ground flood be placed directly under the clock chip to provide a low impedance connection for the VSS pins. In addition, power vias should be distributed evenly throughout the ground flood.

Note: For all power connections to planes, decoupling caps, and vias, the maximum trace width allowable and shortest possible lengths should be used to ensure lowest possible inductance.

4.4 EMI Constraints

Clocks are a significant contributor to EMI. The following recommendations can aid in EMI reduction:

- Maintain uniform spacing between the two halves of differential clocks.
- Route clocks on physical layer adjacent to a VSS reference plane only.

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System Bus Routing Guidelines 5

5.1 Processor System Bus Guidelines

This section covers the system bus source synchronous (data, address, and associated strobes) and common clock signal routing for systems. Table 5-1 summarizes the layout recommendations for Pentium 4 processors with 512-KB L2 cache on 0.13 micron process configurations, and expands on specific design issues and their recommendations.

Table 5-1. System Bus Routing Summary for the Processor[1]

Parameter	Type
Line-to-Line Spacing[2]	Data and common clock system bus must be routed at 7-mil wide traces and with 13-mil spacing
Breakout Guidelines (Processor and MCH)	7-mil wide with 5-mil spacing for a maximum of 250 mils from the component ball
Data Line Lengths (agent to agent spacing)	2"– 10" from pin to pin Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. Signals should be referenced to VSS.
DSTBn/p[3:0]#	A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip). A data strobe and its complement should be routed within ± 25 mils of the same pad-to-pad length. If one strobe switches layers, its complement must switch layers in the same manner. DSTBn/p# should be referenced to VSS
Address Line Lengths (agent to agent spacing) ADSTB[1:0]#	2" – 10" from pin to pin Address signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. The pad is defined as the attach point of the silicon die to the package substrate. Length must be added to the system board to compensate for package length differences. A layer transition may occur if the reference plane remains the same (VSS) and the layers are all of the same configuration (all stripline or all microstrip).
Common Clock Line Lengths	2.5" – 10" pin to pin. No length compensation is necessary.
Topology	Point-to-point (chipset to processor).
Routing Priorities	All signals should be referenced to VSS. Ideally, layer changes should not occur for any signals. If a layer change must occur, reference plane must be VSS and the layers must all be of the same configuration (all stripline or all microstrip for example). The Data Bus must be routed first, then the address bus and then common clock.
Clock keep-Out Zones	Refer to Table 4-3.
Trace Impedance	50 $\Omega \pm 15\%$

NOTES:

1. Refer to the *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet* for MCH package dimensions, and refer to the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Signal Integrity and Usage Guidelines* for processor package dimensions.
2. Data and common clock system bus may be routed at 7 mil wide traces and with 10 mil spacing if line length is kept under 6 inches.
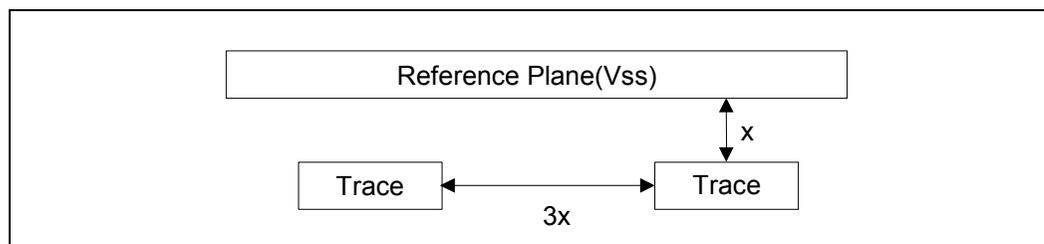
The return path is the route current takes to return to its source. It may take a path through ground planes, power planes, other signals, integrated circuits, and vias, VRMs etc. It is useful to think of the return path as following a path of least resistance back to the original source. Discontinuities in the return path often have signal integrity and timing effects that are similar to the discontinuities in the signal conductor. Therefore, the return paths must be given similar considerations. A simple way to evaluate return path parasitic inductance is to draw a loop that traces the current from the driver through the signal conductor to the receiver, and then back through the ground/power plane to the driver again. The smaller the area of the loop, the lower the parasitic inductance will be.

The following sets of return path rules apply:

- Always trace out the return current path and provide as much care to the return path as the path of the signal conductor.
- Decoupling capacitors do not adequately compensate for a plane split.
- Do not allow splits in the reference planes in the path of the return current.
- Do not allow routing of signals on the reference planes near system bus signals.
- Maintain VSS as a reference plane for all system bus signals.
- Do not route over via anti-pads or socket anti-pads.

5.2 GTLREF Layout and Routing Recommendations

There are four AGTL+ GTLREF pins on the processor that are used to set the reference voltage level for the AGTL+ signals (GTLREF).   Because all of these pins are connected inside the processor package, the GTLREF voltage may be supplied to only one of the four pins.

Figure 5-2. GTLREF Routing
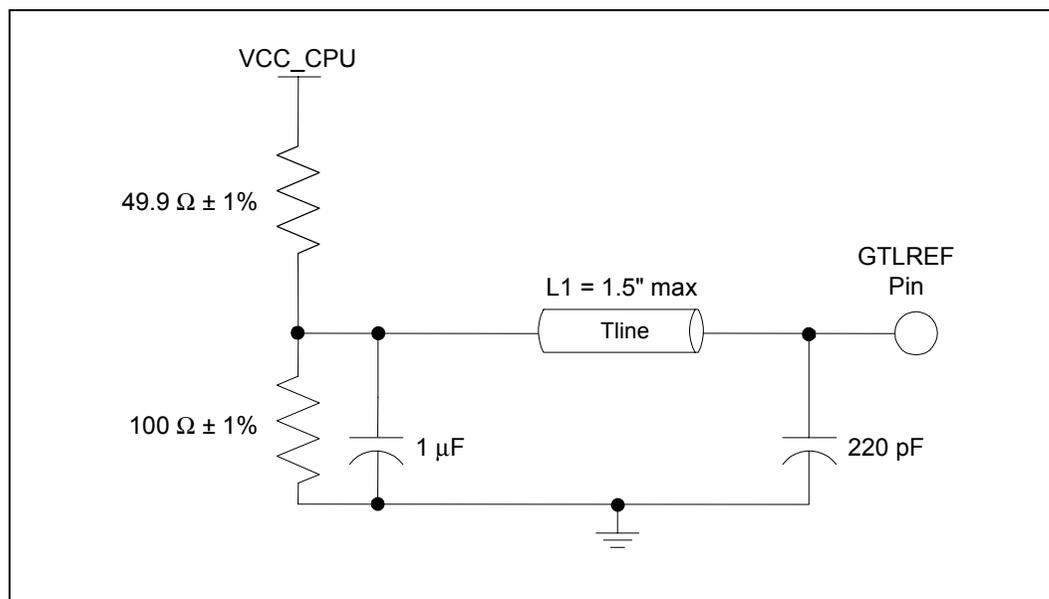
- The processor must have one dedicated voltage divider.

- Decouple the voltage divider with a 1 μF capacitor.

- Keep the voltage divider within 1.5 inches of the GTLREF pin

- Decouple the pin with a high-frequency capacitor (such as a 220 pF 603) as close to the pin as possible

- Keep signal routing at least 10 mils separated from the GTLREF routes. Use a minimum of a 7-mil trace for routing.

- Do not allow signal lines to use the GTLREF routing as part of their return path (i.e., do not allow the GTLREF routing to create splits or discontinuities in the reference planes of the System Bus signals.)

5.2.1 HVREF, HSWNG, HRCOMP Layout and Routing Recommendations at the MCH

The HVREF signals must be tied to a resistor divider network that supplies 2/3*VCC_CPU. Use one 49.9 Ω ± 1% resistor to the VCC_CPU plane, and one 100 Ω ± 1% resistor to ground for the divider. Decouple with one 0.1 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at a minimum of 10 mils away from other signals.

The HSWNG signals must be tied to a resistor divider network that supplies 1/3*VCC_CPU. Use one 300 Ω ± 1% resistor to the VCC_CPU plane, and one 150 Ω ± 1% resistor to ground for the divider. Decouple with one 0.01 µF capacitor at the MCH. The trace to the voltage divider should be routed at a maximum of 3 inches at 12 mils wide. Keep this trace at least 10 mils away from other signals.

Each HRCOMP signal must be tied to ground through a 32.4 Ω ± 1% resistor. The trace to each resistor should be routed a maximum of 0.5 inches at 10 mils wide. Keep each trace at least 7 mils away from other signals.

5.3 Processor Configuration

5.3.1 Intel® Pentium® 4 Processor with 512-KB L2 Cache on 0.13 Micron Process Configuration

This section provides more details for routing Pentium 4 processors with 512-KB L2 cache on 0.13 micron process-based systems. Both recommendations and considerations are presented.

For proper operation of the processor and chipset, it is necessary that the system designer meet the timing and voltage specifications of each component. The following recommendations are Intel's best guidelines based on extensive simulation and experimentation that make assumptions that may not apply to specific OEM system designs. The most accurate way to understand the signal integrity and timing of the system bus in a platform is by performing a comprehensive simulation analysis. It is conceivable that adjustments to trace impedance, line length, termination impedance, board stack-up, and other parameters can be made that improve system performance.

Refer to the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet* for a system bus signal list, a description of signal types, and signal definitions.

intel®

5.3.2 Topology and Routing

Table 5-2. Source Synchronous Signal Groups and the Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, A[16:3]#	ADSTB0#
A[31:17]#	ADSTB1#
D[15:0]#, DBI0#	DSTBP0#, DSTBN0#
D[31:16]#, DBI1#	DSTBP1#, DSTBN1#
D[47:32]#, DBI2#	DSTBP2#, DSTBN2#
D[63:48]#, DBI3#	DSTBP3#, DSTBN3#

5.3.2.1 Design Recommendations

The following are the design recommendations for the data, address, data strobes, and common clock signals. Based on the example shown in Figure 5-3, the data, address, strobe and common clock should be routed 7 mils with 13 mil spacing. For the following discussion, the pad is defined as the attach point of the silicon die to the package substrate.

Data

The pin-to-pin distance for the data signals from the processor to the chipset should be between 2.0 inches and 10 inches (i.e., 2.0" < L1 < 10"). Data signals of the same source synchronous group should be routed to the same pad-to-pad length within ± 100 mils of the associated strobes. As a result, additional trace will be added to some data nets on the system board so that all trace lengths within the same data group are the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe will be different, which results in an inequity between the setup and hold times. Data signals may change layers if the reference plane remains VSS.

$$\text{delta}_{\text{net,strobe}} = (\text{cpu\_pkglen}_{\text{net}} - \text{cpu\_pkglen}_{\text{strobe*}}) + (\text{cs\_pkglen}_{\text{net}} - \text{cs\_pkglen}_{\text{strobe}})$$

Equation 5-1. Calculation to Determine Package Delta Addition to Motherboard Length for UP Systems

Note: Refer to *Intel*® *E7205 Chipset Memory Controller Hub (MCH) Datasheet* for package lengths.

Note: Strobe package length is the average of the strobe pair.

Address

Address signals follow the same rules as data signals with the exception that they should be routed to the same pad-to-pad length within ± 200 mils of the associated strobes. Address signals may change layers if the reference plane remains VSS.

Data Strobes

A strobe and its complement should be routed to a length equal to their corresponding data group's mean pad-to-pad length ± 25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ± 25 mils of the same length. It is recommended that skew be simulated to determine the length that best centers the strobe for a given system.

Common Clock

Common clock signals should be routed to a minimum pin-to-pin motherboard length of 2.5 inches, and a maximum motherboard length of 10 inches.

Figure 5-3. Processor Topology
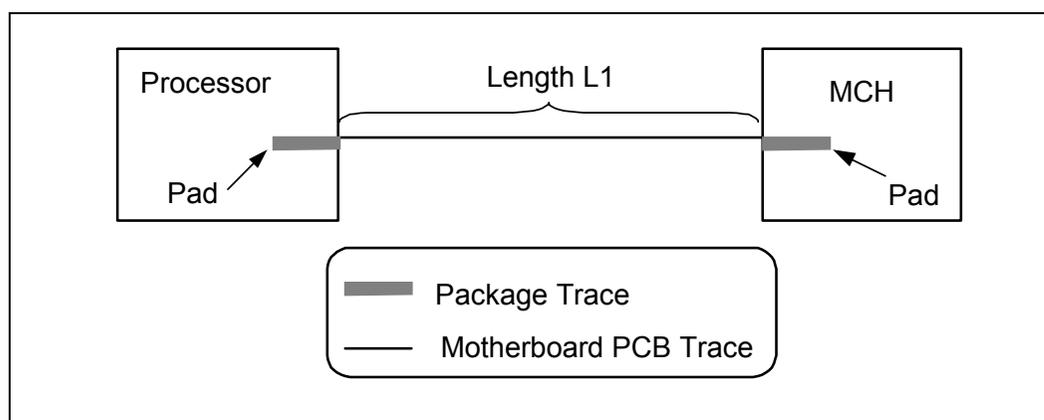
5.4 Routing Guidelines for Asynchronous GTL+ and Other Signals

This section describes layout recommendations for signals other than data, strobes and address. Table 5-3 lists the signals that are described in this section.

Table 5-3. Miscellaneous Signals (Signals That Are Not Data, Address, or Strobe)

Signal Name	Type	Direction	Topology	Driven by
A20M#	Asynchronous GTL+	I	2	Intel® ICH4
BR0#	AGTL+	I/O	4	Processor
XCOMP/YCOMP	Analog	I	5	
FERR#	Asynchronous GTL+ Open Drain	O	1	Processor
IGNNE#	Asynchronous GTL+	I	2	ICH4
INIT#	Asynchronous GTL+	I	2-A	ICH4
LINT0/INTR LINT1/NMI	Asynchronous GTL+	I	2	ICH4
PROCHOT#	Asynchronous GTL+ Open Drain	O	1	Processor
PWRGOOD	Other	I	2-B	ICH4
RESET#	AGTL+ Open Drain	I	4	MCH
SLP#	Asynchronous GTL+	I	2	ICH4
SMI#	Asynchronous GTL+	I	2	ICH4
STPCLK#	Asynchronous GTL+	I	2	ICH4
THERMTRIP#	AGTL+ Open Drain	O	1	Processor
VCCA	Power	I	3	External logic
VCCIOPLL	Power	I	3	External logic
VCC_SENSE	Other	O		Processor
VCCVID[4:0]	Open Drain 3.3 V Tolerant	O	8, 9	Processor
VSSA	Power	I	3	Ground
THERMDA/ THERMDC	Other	I/O	6	External logic
TESTHI	Other	I/O	7	External logic

All signals must meet the AC and DC specifications described in the *Intel® Pentium® 4 Processor with 512KB L2 Cache on .13 Micron Process Datasheet*.

5.4.1 Topologies

The following sections describe the topologies and layout recommendations for the miscellaneous signals.

5.4.1.1 Topology 1: Asynchronous GTL+ Signals Driven by the Processor—FERR#, PROCHOT# and THERMTRIP#

These signals should adhere to the following routing and layout recommendations. Figure 5-4 illustrates the recommended topology. If PROCHOT# is routed to external logic, voltage translation may be required to avoid excessive voltage levels at the processor and to meet input thresholds for the external logic.

Table 5-4. Layout Recommendations for FERR# and THERMTRIP# Signals—Topology 1

Trace Z_O	Trace Spacing	L1	L3	R_{PU}
50 Ω	7 mil	1" – 12"	3" max	62 ± 5% Ω

Figure 5-4. Routing Illustration for FERR# and THERMTRIP#
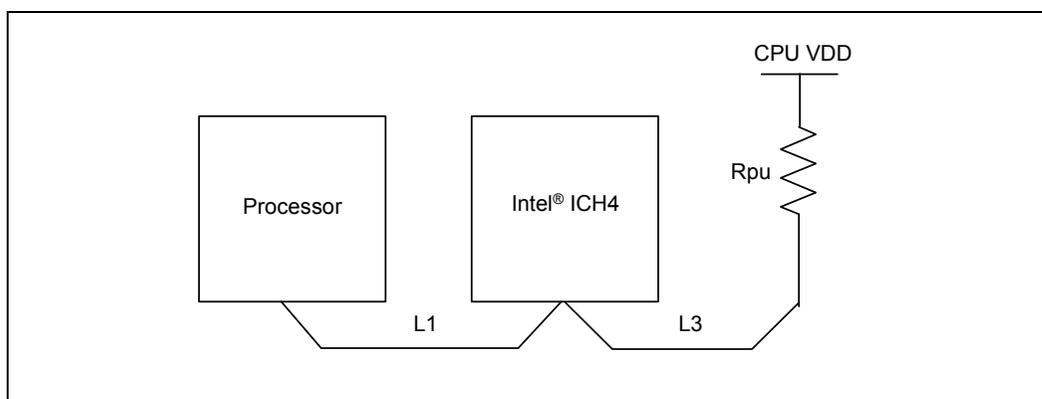
Table 5-5. Layout Recommendations for PROCHOT# Signal—Topology 1

Trace Z_O	Trace Spacing	L1	L2	L3	R_{PU}
50 Ω	7 mil	1" – 17"	10" max	3" max	62 ± 5% Ω

Figure 5-5. Routing Illustration for PROCHOT#
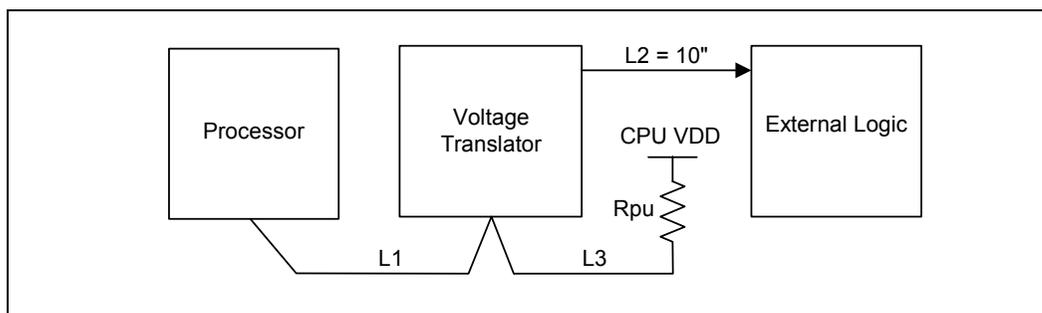
5.4.1.2 Topology 2: Asynchronous GTL+ Signals Driven by the Intel® ICH4— A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#

The V_CPU_IO signals are documented to support only 0.8 V to 1.75 V. The ICH4 output signals voltage swing depend on the voltage passed into these signals (V_CPU_IO[2:0]), and voltages below 0.8 V are not supported by the ICH4's buffers. These signals should adhere to the following routing and layout recommendations. Figure 5-6 illustrates the recommended topology.

Table 5-6. Layout Recommendations for Miscellaneous Signals—Topology 2

Processor CMOS Routing Requirements	Maximum Trace Length	Signal Referencing	Processor CMOS Signals Length Matching
5 on 5	L1 = 19 inches	N/A	None

Figure 5-6. Routing Illustration for A20M#, IGNNE#, LINT[1:0], SLP#, SMI#, and STPCLK#
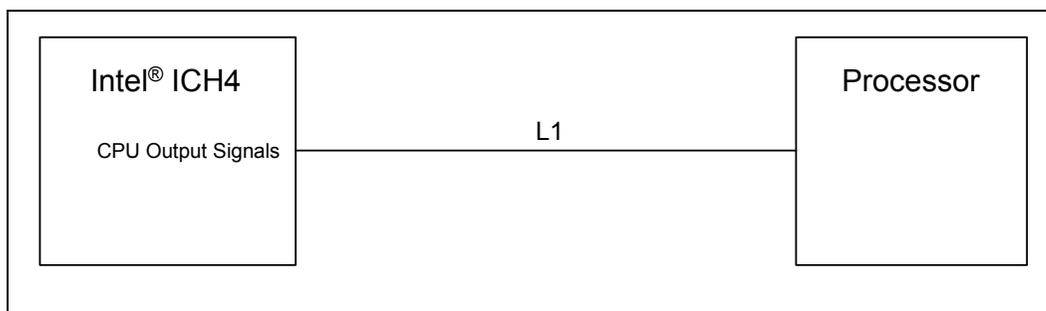
5.4.1.3 Topology 2-A: INIT#

Level shifting is required for the INIT# signal to the FWH to meet the input logic levels of the FWH. See Section 10.4.4 for voltage level translation circuitry.

Table 5-7. Layout Recommendations for INIT#—Topology 2A

Trace Z_O	Trace Spacing	L1	L2	L3	L4	R_{PU}
50 Ω	7 mil	2" max	10" max	17" max	3" max	300 Ω ± 5%

Figure 5-7. Routing Illustration for INIT#
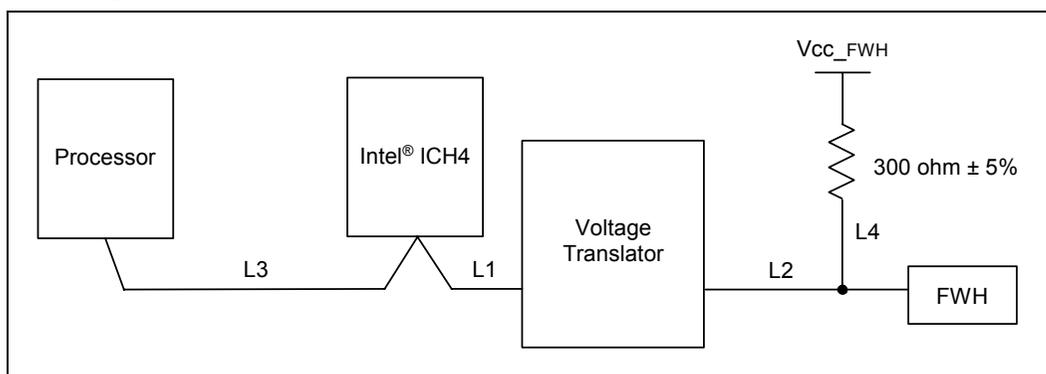
5.4.1.4 Topology 2-B: Miscellaneous Signals Driven by the Intel® ICH4 Open Drain; PWRGOOD

This signal should adhere to the following routing and layout recommendations. Figure 5-8 illustrates the recommended topology.

Table 5-8. Layout Recommendations for Miscellaneous Signals—Topology 2B

Trace Z_O	Trace Spacing	L1	L3	R_{PU}
50 Ω	7 mil	1" – 12"	3" max	300 Ω ± 5%

Figure 5-8. Routing Illustration for PWRGOOD
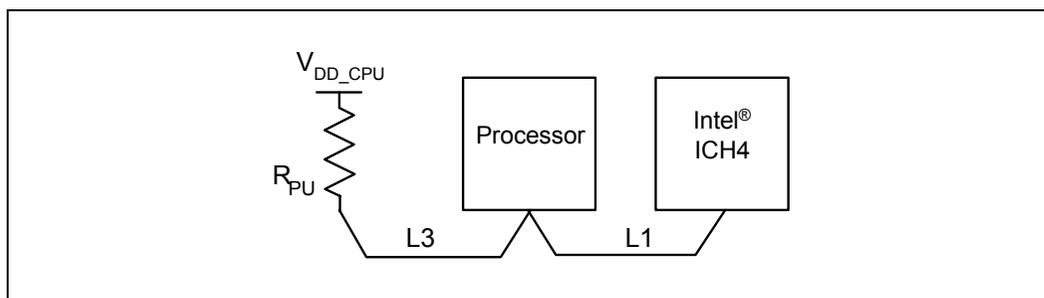
5.4.1.5 Topology 3: VCCIOPLL, VCCA and VSSA

VCCIOPLL and VCCA are isolated power for internal PLLs. It is critical that they have clean, noiseless power on their input pins. Keep these signals away from noisy or high-frequency signals. Keep their traces as short as possible. Follow the recommendations in Figure 5-9 for layout guidelines. VSSA should not be connected directly to ground on the system board. Further details can be found in Section 12.6

Figure 5-9. Routing Illustration for VCCIOPLL, VCCA and VSSA
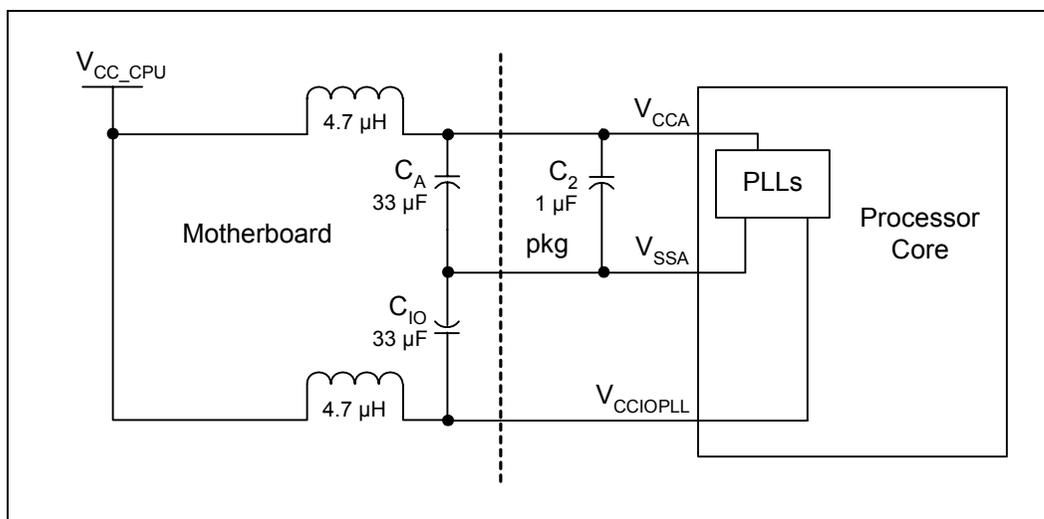
5.4.1.6 Topology 4: BR0# and RESET#

Since the processor does not have on-die termination on the BR0# and RESET# signals, it is necessary to terminate using discrete components on the system board. Connect the signals between the components as shown in Figure 5-10. The E7205 chipset has on-die termination and thus it is necessary to terminate only at the processor end. The value of R_T should be $51\Omega \pm 5\%$ for RESET#. The value of R_T should be $150\,\Omega - 220\,\Omega \pm 5\%$ for BR0#.

Figure 5-10. Routing Illustration for BR0# and RESET#
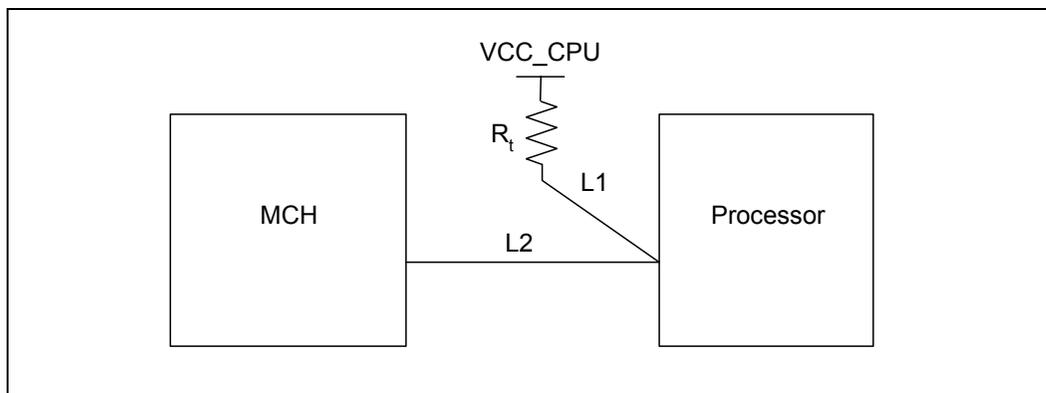
Table 5-9. BR0# and RESET# Lengths

Signal	R_T	L1	L2
RESET#	51 Ω	≤ 1" – 2"	2.5" – 10"
BR0#	150 – 220 Ω	≤ 1" – 2"	2.5" – 10"

5.4.1.7 Topology 5: XCOMP/YCOMP Signals

Terminate the XCOMP/YCOMP pins to ground through two resistors. Refer to the latest schematics for the resistor values. Do not wire the COMP pins together; connect each pin to its own termination resistor.

5.4.1.8 Topology 6: THERMDA/THERMDC Routing Guidelines

The processor incorporates an on-die thermal diode. THERMDA (diode anode) and THERMDC (diode cathode) pins on the processor can be connected to a thermal sensor located on the system board to monitor the die temperature of the Processor for thermal management/long term die temperature change monitoring purpose. This thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Because the thermal diode is used to measure a very small voltage from the remote sensor, care must be taken to minimize noise induced at the sensor inputs. Below are some guidelines:

- Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4 to 8 inches away as long as the worst noise sources such as clock generators, data buses and address buses etc. are avoided.

- Route the THERMDA and THERMDC lines in parallel and close together with ground guards enclosed.

- Use wide tracks to reduce inductance and noise pickup that may be introduced by narrow ones. A width of 10 mils and spacing of 10 mils is recommended.

5.4.1.9 Topology 7: TESTHI and RESERVED Pins

TESTHI[11:8] and TESTHI1 must be connected to VCC_CPU via a pull-up resistor. TESTHI[5:2], TESTHI0, and TESTHI12 must be connected to VCC_CPU via a pull-up resistor or be tied directly to VCC_CPU. Ideally, each TESTHI pin should be pulled up with a resistor value that matches the impedance of the system bus interface. If a value matching the system bus interface is not possible, each signal must use a pull-up resistor with a value between 40 Ω and 60 Ω.

Additionally, if the ITPCLKOUT[1:0] pins are not used then they may be tied directly to VCC_CPU, or connected individually to VCC_CPU using pull-up resistors with values between 1 kΩ and 10 kΩ. Tying ITPCLKOUT[1:0] directly to VCC_CPU or sharing a pull-up resistor to VCC_CPU, will prevent use of debug interposers. This implementation is strongly discouraged for system boards that do not implement an onboard debug port.

5.4.1.10 Topology 8: VCCVID Regulator Recommendations

- The output of the voltage regulator used to generate VCCVID should be no more than 1.5 inches away from pin AF4 of the processor.

- The trace connecting the voltage regulator output to pin AF4 should be as wide as practical, but not less than 0.025 inches.

- The trace connecting the voltage regulator output to pin AF4 should have both a 0.1 µF and 1.0 µF capacitor for decoupling. The 1.0 µF capacitor should be located as close as possible to the output of the voltage regulator. The 0.1 µF capacitor should be located as close as possible to pin AF4 on the processor.

If an integrated voltage regulator such as the MIC5248 is used, the voltage input (pin 1) should be connected to the system boards VCC or 3.3 V rails through a zero ohm resistor. The input of the voltage regulator should also be decoupled with a 0.1 µF capacitor at the pin. The trace connecting the voltage regular input to the zero resistor should be equal to or greater than the voltage regulator output trace connected to the processor (i.e. if the connection to the processor is 0.025 inches than the trace width to the input of the voltage regulator should be 0.025 inches or greater). The voltage regulator power good signal (pin 4) should be connected to the voltage regulator output (pin 5) through a 10 kΩ resistor.

5.4.1.11   Topology 9: Processor Voltage Regulator Sequencing Requirements

The Pentium 4 processor with 512-KB L2 cache on 0.13 micron process requires a 1.3 V supply to the VCCVID pins to support the on-die VID generation circuitry. A linear regulator is recommended to generate this voltage. The on-die VID generation circuitry has some power sequencing requirements. Figure 5-11 shows a block diagram of a power sequencing implementation. Figure 5-12 and Figure 5-13 illustrate timing diagrams of the power sequencing requirements.

Figure 5-11. Power Sequencing Block Diagram
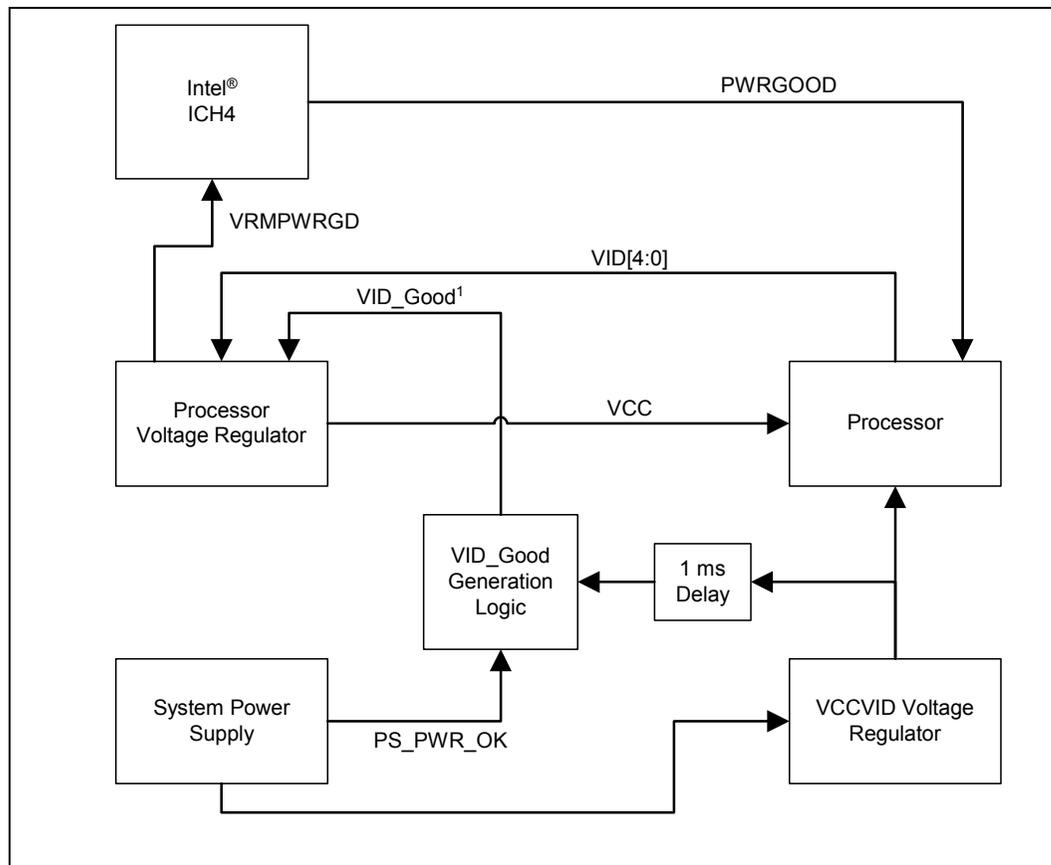
NOTES:
  1. VID_Good connected to voltage regulator controller output enable.

Figure 5-12. Power-on Sequence Timing Diagram
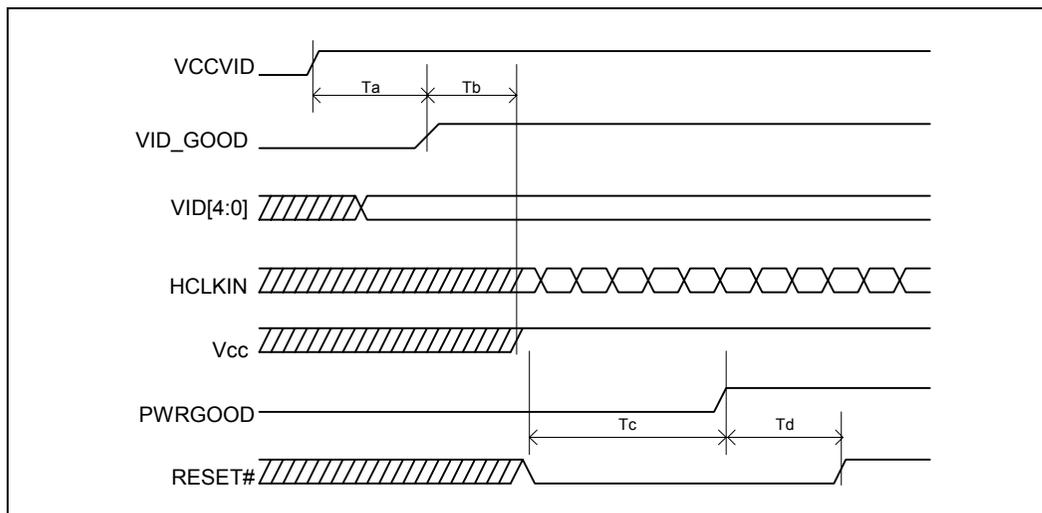
NOTES:
1. Ta = 1 ms minimum (VCCVID > 1V to VID_GOOD high)
2. Tb = 50 ms maximum (VID_GOOD to VCC valid maximum time)
3. Tc = T37 (PWRGOOD inactive pulse width) = 10 BCLKs min
4. Td = T36 (PWRGOOD to RESET# de-assertion time) = 1 ms (min), 10 ms (max)
5. VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regulator control silicon.

Figure 5-13. Power-off Sequence Timing Diagram
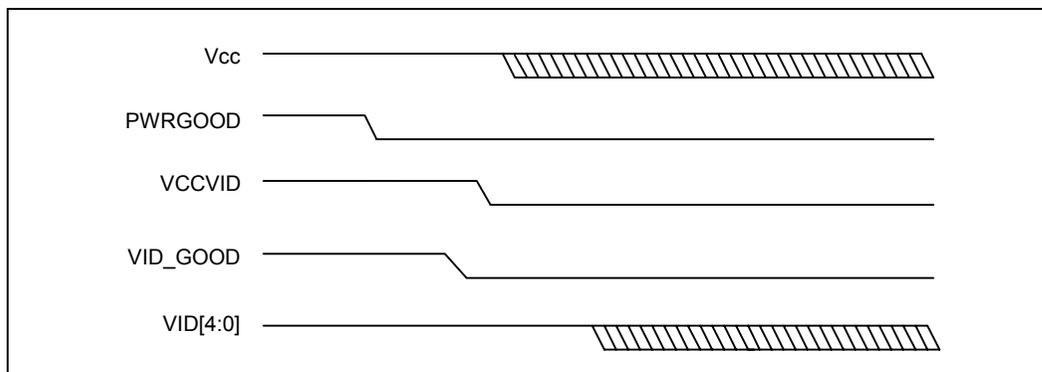
NOTES:
1. This timing diagram is not intended to show specific times. Instead a general ordering of events with respect to time should be observed.
2. When VCCVID is less than 1 V, VID_GOOD must be low.
3. VCC must be disabled before VID[4:0] becomes invalid.
4. VID_GOOD is not a processor signal. This signal is routed to the output enable pin of the voltage regulator control silicon.

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DDR System Memory Design Guidelines 6

This chapter contains information and details for designing an E7205 chipset-based platform with DDR PC2100. The chapter provides information on the DDR reference stack-up, topologies, and DDR layout, and routing guidelines for each system memory interface signal group that is described. This chapter also provides system memory bypass capacitor guidelines and DDR power deliver requirements. Together, these guidelines provide for a robust DDR solution for an E7205 chipset-based design.

As system memory transfer rates increase, careful attention must given to all of the E7205 chipset guidelines to provide system robustness for DDR PC2100.

As stated earlier, the MCH is a dual channel memory interface. The pinout for the two channels has been optimized for a motherboard design with interleaved DIMMs. The DIMM closest to the MCH is DIMM0 on channel A, the next DIMM is DIMM0 on Channel B. The DIMMs continue to alternate between Channel A and B to the termination resistors.

The Double Data Rate (DDR) SDRAM system memory interface supports unbuffered memory only. The system memory interface can be divided into six signal groups: Data, Address/Command, Control, Feedback, Clocks and DC bias signals. Table 6-1 summarizes the signal groupings. Refer to the *Intel*® *E7205 Chipset Memory Controller Hub (MCH) Datasheet* for more information about these signals.

The E7205 chipset supports Error Checking and Correction (ECC).

Table 6-1. Intel® E7205 Chipset DDR Signal Groups

Group	Signal Name
Control	CKE_x[3:0]
	CS_x[3:0]#
Clocks	CMDCLK_x[7:0]
	CMDCLK_x[7:0]#
Data	DQ_x[63:0]
	DQS[_x17:0]
	CB_x[7:0]
Address / Command	MA_x[12:0]
	BA_x[1:0]
	RAS_x#
	CAS_x#
	WE_x#
DC Biasing	RCVENOUT_x#
DC Bias	DRCOMP_H
	DRCOMP_V
	ODTCOMP
	DRCOMPVREF_H
	DRCOMPVREF_V
	DDR_STRAP
	DVREF_A / DVREF_B

6.1 DDR-SDRAM Stack-Up and Referencing Guidelines

The E7205 chipset platform designs using the DDR-SDRAM memory sub-system require continuous ground referencing for all DDR signals. Based on the six-layer stack-up shown below, the DDR channel is completely ground referenced. Although the DDR bus is technically referencing both power and ground on layer 4, it is much more tightly coupled to the ground plane because it is closer to the ground plane. Attention still must be paid to ensure that DDR signals do not cross power plane splits because a small percentage of the return current travels through the power planes.

All DDR signals must be ground referenced to provide an optimal current return path. To do this, the ground plane must be solid and continuous from the MCH DDR signal pins to beyond the VTT termination capacitors at the end of the channel.

Figure 6-1. Board Stack-Up

		Layer Thickness	Copper Weight
Top	SIGNAL	2.1	0.5 oz plus plating
	PREPREG	4.0	
Layer 2	GND	1.2	1 oz.
	CORE	4.3	
Layer 3	POWER	1.2	1 oz.
	PREPREG	6.5	
	CORE	23.0	
	PREPREG	6.5	
Layer 4	SIGNAL	1.2	1 oz.
	CORE	4.3	
Layer 5	GND	1.2	1 oz.
	PREPREG	4.0	
Bottom	SIGNAL	2.1	0.5 oz plus plating

Panel Thickness (mils) = 61.6   Assumes finished thickness on uStrip Layers

6.2 Unbuffered DDR System Memory Topology and Layout Design Guidelines

This section contains information and details on the DDR topologies, layout and routing guidelines. The guidelines are provided for each corresponding signal group: Data, Address/ Command, Control, Feedback, Clock and DC biasing.

The MCH has two channels of DDR memory. All signals can break out of the MCH and route entirely referenced to ground. The general routing strategy in a 6-layer board is to route all the data and strobes for Channel B (closest to edge of MCH package) on the top layer. The Channel A data and strobes can be routed entirely on the layer 4. The address, control and clock signals for both channels can be routed entirely on the bottom layer. With this strategy, the whole interface will be ground referenced. The specific details of those individual topologies will be shown in the following sections.

Figure 6-2. DDR Routing Strategy

SIGNAL	<---- Ch B DQ/DQS
PREPREG	
GND	
CORE	
POWER	
PREPREG	
CORE	
PREPREG	
SIGNAL	<---- Ch A DQ/DQS
CORE	
GND	
PREPREG	
SIGNAL	<---- Ch A & B Add/Ctrl/Clocks
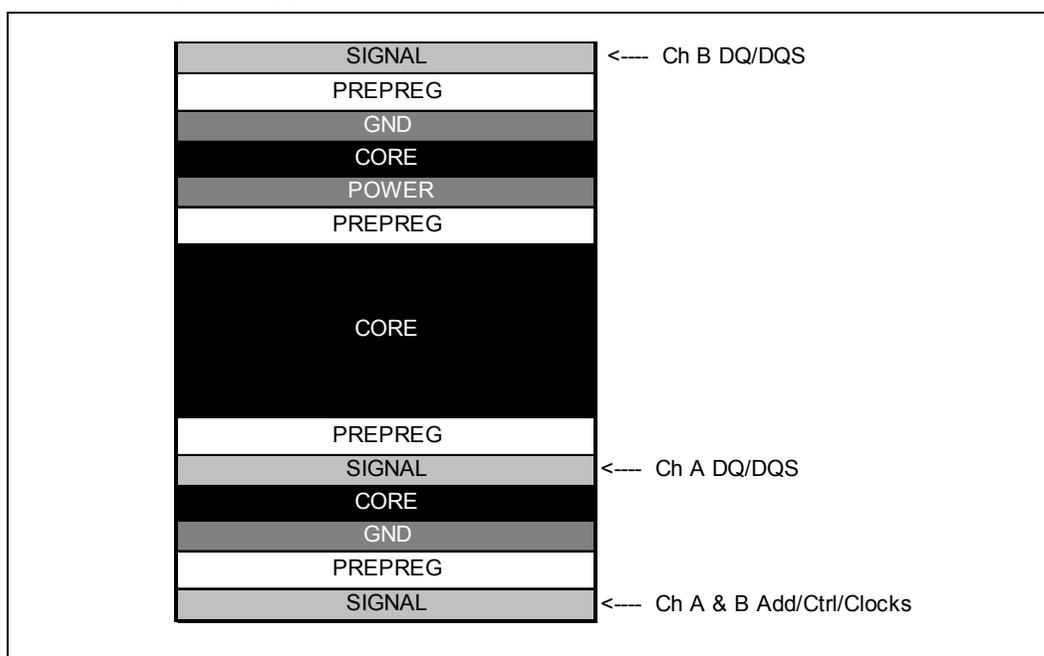
Because of the height-restricted areas of the ATX chassis, it is best to place the DIMMs as close to the back of the chassis as possible. With the E7205 chipset platform having interleaved DIMMs, placing the termination resistors immediately after the last DIMM in Channel A, physically the third DIMM from the MCH was not ideal. Instead, the termination resistors for both channels were placed beyond the last DIMM. The result of this is that lengths to termination resistors on Channel A grow larger than previous DDR designs, especially for chip selects and clock enable signals. The additional advantage of this is that Channel B data and strobes can be routed on the top layer with no layer transitioning. The Channel A data and strobes transition to layer 4 at the MCH and can route to the DIMMs and return to the top layer to terminate at the resistor pads. The same is true for the clocks, control and address signals which are routed on the bottom layer.

Figure 6-3. DDR DIMM and Termination Strategy
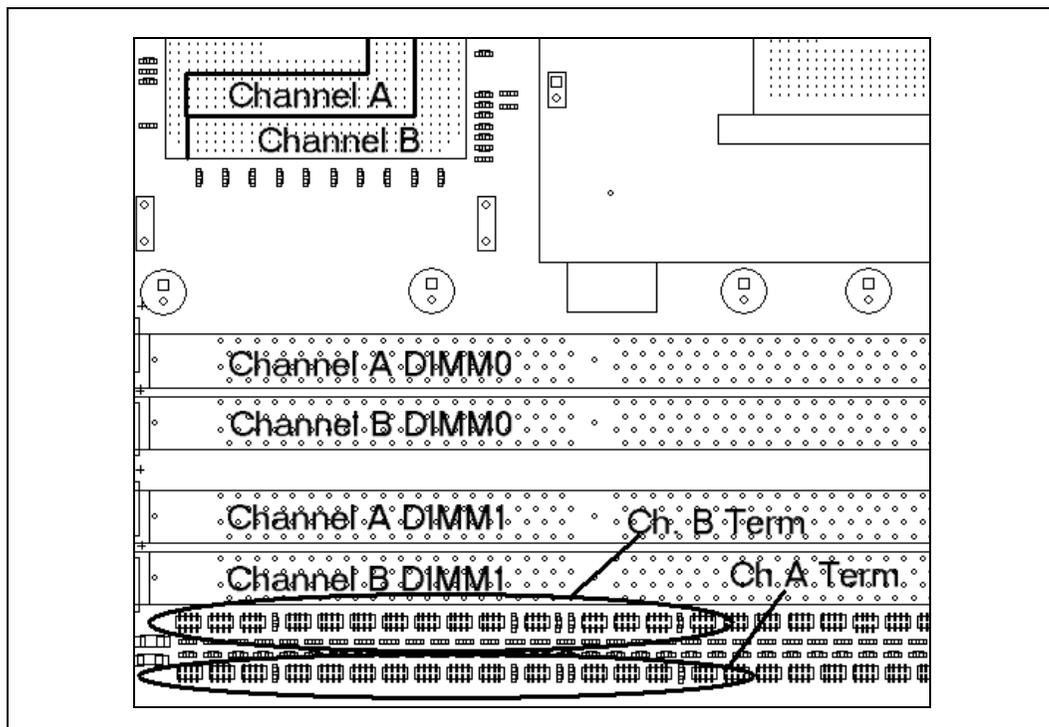
The following signaling group sections are intentionally ordered in the same fashion that Intel recommends approaching the length matching criteria. The CKE and CS# signals should be routed first and made as short as possible. From those lengths, the required command clock group lengths are determined which will drive the required lengths for the data/strobe groups and address/control groups, respectively.

6.2.1   Control Signals — CKE_x[3:0], CS_x[3:0]#

The MCH control signals are source-clocked signals that include 4 clock enable (CKE) and 4 chip selects (CS#) signals. These control signals are clocked into the DIMMs using the positive edge of the differential clock signals. The Intel MCH drives the control signals and clocks signals together, with the clocks centered in the valid control window. Only one chip select (CS#) and one clock enable (CKE) signal is needed for each DDR-SDRAM physical DIMM device row.

Two chip selects and two clock enables are routed to each DIMM (one for each side) to support double-sided DDR DIMMs. Table 6-2 below summarizes the CKE/CS# to DIMM pin mapping.

Table 6-2. Control Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CS_x0#	DIMM0	157
CS_x1#	DIMM0	158
CS_x2#	DIMM1	157
CS_x3#	DIMM1	158
CKE_x0	DIMM0	21
CKE_x1	DIMM0	111
CKE_x2	DIMM1	21
CKE_x3	DIMM1	111

Resistor packs are acceptable for the parallel control termination resistors (R_{TT}), but the control signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, address/ command signals.

Table 6-3 and Figure 6-4 through Figure 6-6 depict the recommended topology and layout routing guidelines for the DDR-SDRAM control signals for the first and second DIMM.

Figure 6-4. DIMM-0 Control Signal Routing Topology (CS_x[1:0]#, CKE_x[1:0])
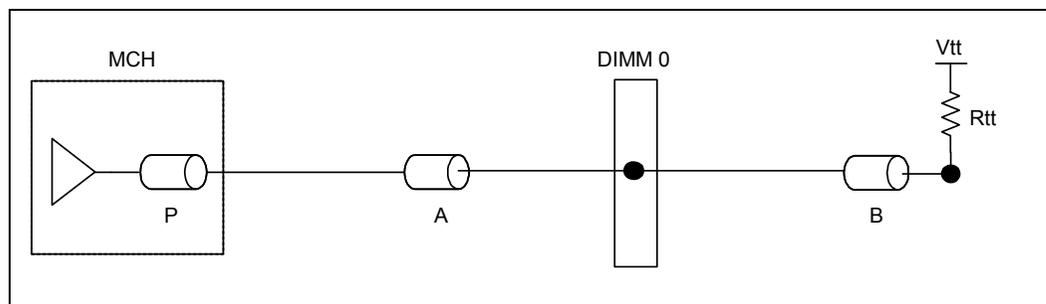
Figure 6-5. DIMM-1 Control Signal Routing Topology (CS_x[3:2]#, CKE_x[3:2])
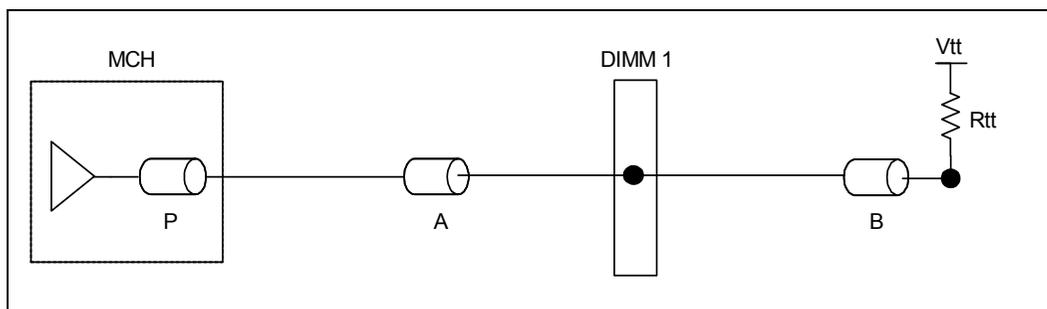
Table 6-3. Control Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CS_x[3:0]#, CKE_x[3:0]
Topology	Point-to-point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_O)	A, B = 60 Ω ± 10%
Nominal Trace Width	A, B = 5 mils
Nominal Trace Spacing	MCH to first DIMM = 15 mils
Group Spacing	20 mils minimum spacing from non-DDR related signals.
Trace Length A (CS_x[1:0]#/CKE_x[1:0]) – MCH Signal Ball to DIMM Pins on First DIMM	CS#: 1.5" – 5.5" CKE: 1.5" – 5.5"
Trace Length A (CS_x[3:2]#/CKE_x[3:2]) – MCH Signal Ball to DIMM Pins on Second DIMM	CS#: 1.5" – 5.5" CKE: 1.5" – 5.5"
Trace Length B (CS_x[1:0]#/CKE_x[1:0]) – DIMM pins on first DIMM to R_{TT} Pad	CS#: 0.1" – 2.5" CKE: 0.1" – 2.5"
Trace Length B (CS_x[3:2]#/CKE_x[3:2]) –- DIMM pins on Second DIMM to R_{TT} Pad	CS#: 0.1" – 2.5" CKE: 0.1" – 2.5"
Termination Resistor (R_{TT})	56 Ω ± 5%
MCH Breakout Guidelines	5 mil width using maximum spacing until broken out beyond the MCH package.
Length Tuning Method	CS_x[3:0]#/CKE_x[3:0] do not have length matching requirements. Keep as short as possible because the longest CS# or CKE length drives the minimum CMDCLK length. See the following section for details.

Figure 6-6. Control Signal Trace Width/Spacing Routing on Lead-in Length
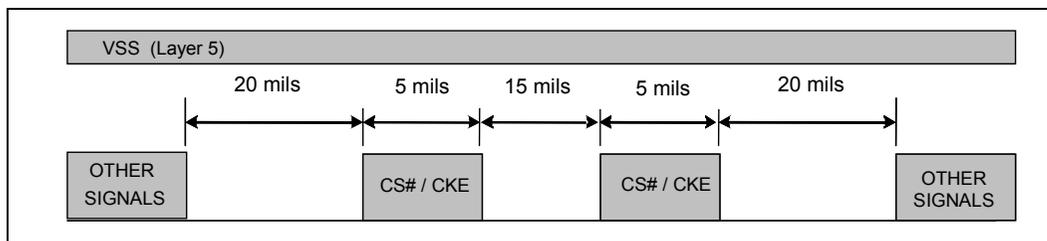
6.2.1.1 Control Group Signal Length Matching Requirements

The CS# and CKE signals do not require length matching but must be routed as short as possible. As an example, CS_x[1:0]# and CKE_x[1:0] will be routed to the first DIMM in either Channel A or Channel B. After routing those four signals, the longest net, which includes the MCH internal package length, will drive the minimum length for the clocks to the first DIMM in the channel, CMDCLK_x[0,4,6] and CMDCLK_x[0,4,6]#. It's important to include the internal lengths in calculating the longest net because the longest net on the board may not be the longest net from MCH die pad to DIMM pin.

6.2.2 Clock Signals — CMDCLK_x[7:0], CMDCLK_x[7:0]#

The MCH clock signals include 8 differential clock pairs CMDCLK_x[7:0] and CMDCLK_x[7:0]#. In an unbuffered configuration, CMDCLK_x[3:2] and CMDCLK_x[3:2]# are left floating because only six pairs are needed for a 2-DIMM per channel configuration. The MCH generates and drives these differential clock signals required by the DDR interface; therefore no external clock driver is required for the DDR interface. Three differential clock pairs are routed to each DIMM connector. Table 6-4 summarizes the clock signal mapping.

Table 6-4. Clock Signal Mapping

Signal	Routed to
CMDCLK_x[0,4,6], CMDCLK_x[0,4,6]#	DIMM0
CMDCLK_x[1,5,7], CMDCLK_x[1,5,7]#	DIMM1
CMDCLK_x[2,3],CMDCLK_x[2,3]#	No Connect

The differential clock pairs must be routed differentially from the MCH to their associated DIMM pins, and must maintain the correct isolation spacing from other signals. When the signals serpentine, maintain a minimum of 20-mil spacing. The differential clock pair must maintain correct spacing to remain differential.

Table 6-5 is provided to help the routing of the clock signals. The table summarizes a typical clock signal to DIMM pin mapping.

Table 6-5. Clock Signal DIMM Pin Mapping

Signal	Relative to	DIMM pin
CMDCLK_x0	DIMM0	137
CMDCLK_x0#	DIMM0	138
CMDCLK_x4	DIMM0	16
CMDCLK_x4#	DIMM0	17
CMDCLK_x6	DIMM0	76
CMDCLK_x6#	DIMM0	75
CMDCLK_x1	DIMM1	137
CMDCLK_x1#	DIMM1	138
CMDCLK_x5	DIMM1	16
CMDCLK_x5#	DIMM1	17
CMDCLK_x7	DIMM1	76
CMDCLK_x7#	DIMM1	75

The CS# and CKE lengths drive the minimum length requirements for the command clocks. The rest of the DDR system memory signals are tuned to CMDCLK/CMDCLK#. The individual group signal length matching requirements are detailed in their corresponding section for each system memory group. CMDCLK/CMDCLK# must be length-matched to each other.

No external termination resistors are needed for the clock signals. Table 6-6 and Figure 6-7 through Figure 6-9 show the recommended topology and layout routing guidelines for the DDR-SDRAM differential clocks.

Figure 6-7. DDR Clock Routing Topology (CMDCLK_x[0,4,6]/CMDCLK_x[0,4,6]#)
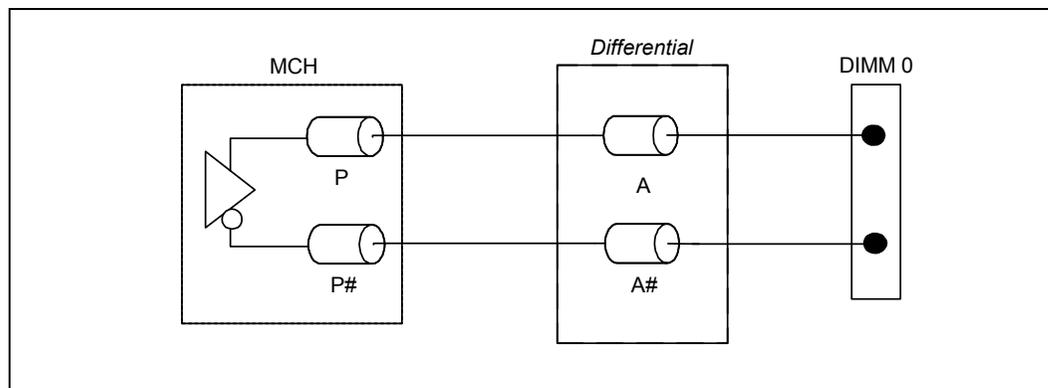
Figure 6-8. DDR Clock Routing Topology (CMDCLK_x[1,5,7]/CMDCLK_x[1,5,7]#)
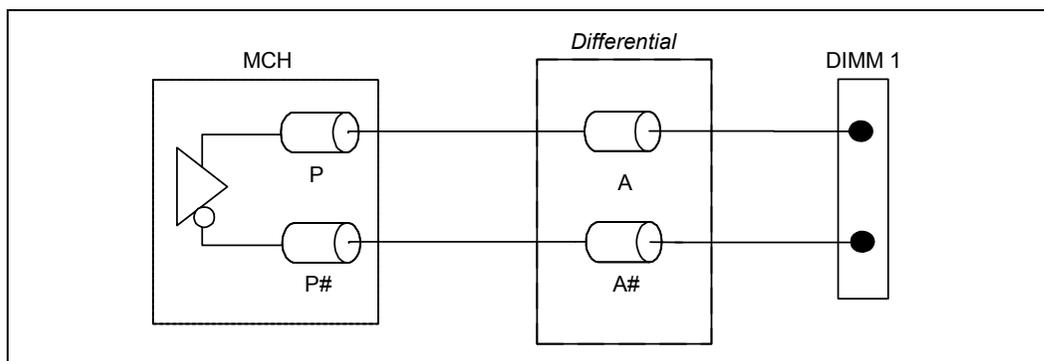
Table 6-6. Clock Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	CMDCLK_x[7:4,1:0]/CMDCLK_x[7:4,1:0]#
Topology	Point-to-point
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_O)	Differential = 84 Ω ± 10%
Nominal Trace Width	6 mils
Nominal Differential Trace Spacing	7 mils
Group Spacing	20 mils minimum spacing from another DDR signal group. 20 mils minimum spacing from non-DDR related signals.
Serpentine Spacing	20 mils minimum
Trace Length A (CMDCLK_x[0,4,6]) – MCH Signal Ball to pin of first DIMM	Min = 3.5" Max = 9.0"
Trace Length A (CMDCLK_x[1,5,7]) – MCH Signal Ball to pin of Second DIMM	Min = 3.5" Max = 9.0"
MCH Breakout Guidelines	5-mil width with 5-mil differential spacing until broken out of package.
Length Matching	Exact length matching from MCH internal die pad to DIMM connector pin is required for CMDCLKs and their complements. In addition, CMDCLKs must length match the other command clocks connecting to the same DIMM, i.e., CMDCLK_x0 must match CMDCLK_x4 and CMDCLK_x6 which all route to the first DIMM.

Figure 6-9. Clock Signal Trace Width/Spacing Routing Cross Section
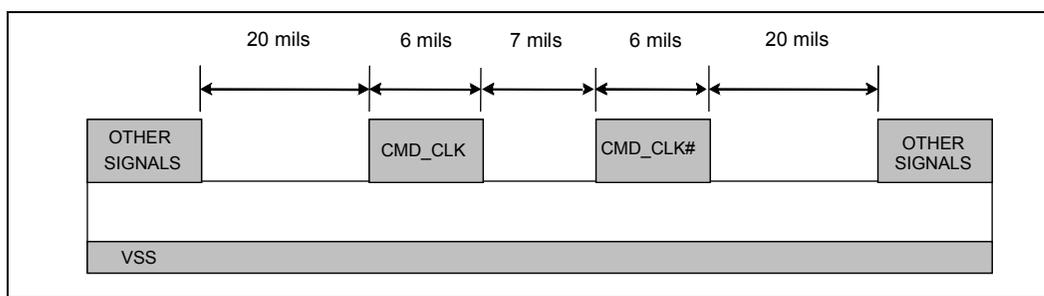
6.2.2.1   Clock Group Signal Length Matching Requirements

The MCH provides three differential clock pair signals for each DIMM. A differential clock pair consists of a CMDCLK signal and its complement signal CMDCLK#. In the previous section, it was advised that the CS# and CKE signals be routed as short as possible. Including the MCH internal package lengths in the comparison, the longest CS# or CKE is determined. From this net, the minimum length of the command clocks is determined. The longest net within CS_x[1:0]# and CKE_x[1:0] will determine the minimum length of CMDCLK_x[0,4,6]. The longest net within CS_x[3:2]# and CKE_x[3:2] will determine the minimum length of CMDCLK_x[1,5,7].

If the longest CKE has a lead-in length between:

	1.5 - 2.5"	then the minimum CMDCLK length $\geq$ CKE + 2.0"
or	2.5 - 3.5"	then the minimum CMDCLK length $\geq$ CKE + 2.5"
or	3.5 - 4.0"	then the minimum CMDCLK length $\geq$ CKE + 3.0"
or	4.0 - 5.5"	then the minimum CMDCLK length $\geq$ CKE + 3.5"

If the longest CS# has a lead-in length between:

	1.5 - 2.5"	then the minimum CMDCLK length $\geq$ CS# + 1.0"
or	2.5 - 3.0"	then the minimum CMDCLK length $\geq$ CS# + 1.5"
or	3.0 - 3.5"	then the minimum CMDCLK length $\geq$ CS# + 2.0"
or	3.5 - 4.5"	then the minimum CMDCLK length $\geq$ CS# + 2.5"
or	4.5 - 5.5"	then the minimum CMDCLK length $\geq$ CS# + 3.0"

It is important to compare the CS# and CKE lengths after the previous equations have been applied to determine the minimum command clock length. For instance, a CS# length of 2 inches and a CKE length of 1.9 inches would suggest the CS# signal would create the longest minimum command clock length requirement. After applying the equations, the CS# length is adjusted to 3 inches (2" + 1") and the CKE length is adjusted to 3.9 inches (1.9" + 2.0"). Therefore, the longest adjusted net is actually the CKE signal and it will determine the minimum command clock length.

From the above equations, it is clear why the CS# and CKE signals must be as short as possible. The maximum control signal length drives the command clocks to be longer. This requires the data and strobe signals to increase in length as well.

Figure 6-10 shows the length matching requirements between the control and the clock signals.

Figure 6-10. Control Signal to CMDCLK Trace Length Matching Requirements
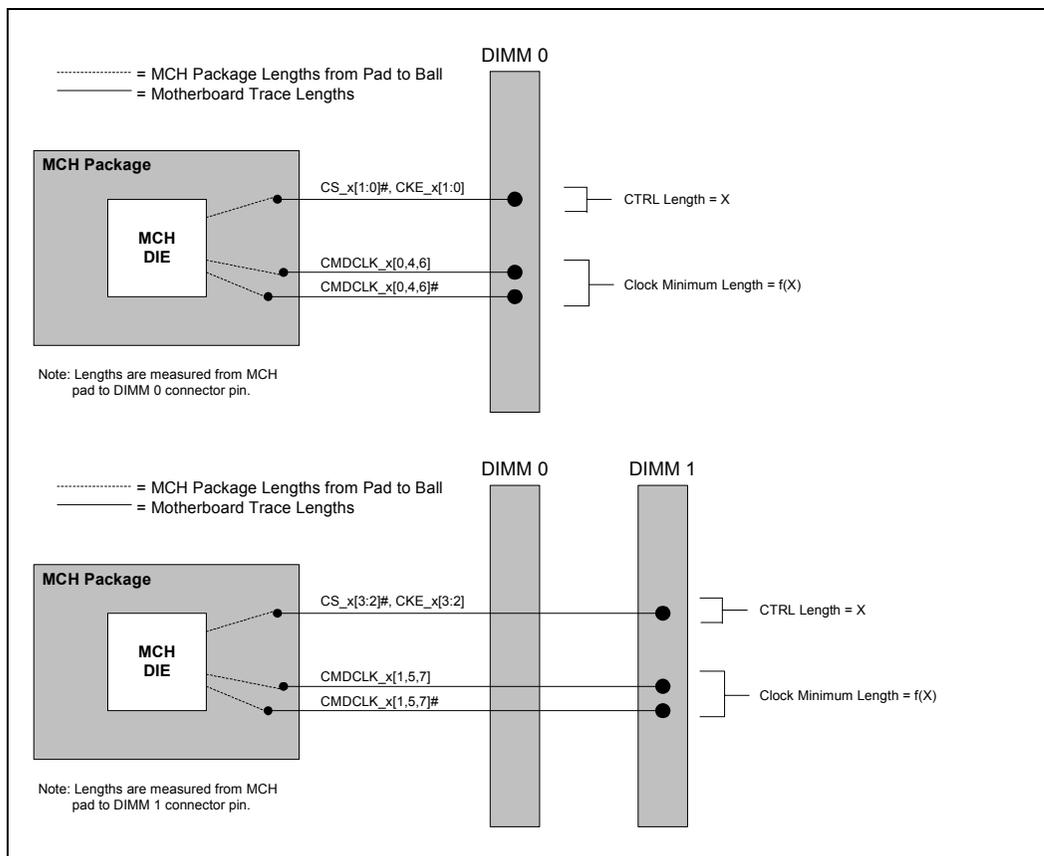
CMDCLK and its complement CMDCLK# within each differential clock pair requires exact length matching from MCH pad to the pins of the DIMM connector.

The length of the CMDCLK and its complement to first and second DIMM include the MCH package length + the motherboard trace length. The internal package trace lengths is provided in the *Intel® E7205 Chipset Memory Controller Hub (MCH) Datasheet.*

In addition, clock length matching is required between clock pairs associated to the same DIMM. The differential clock pairs for the first DIMM connector, CMDCLK_x[0,4,6]/ CMDCLK_x[0,4,6]#, require exact matching of the trace lengths from MCH internal pad to the pins of the first DIMM connector. The differential clock pairs for the second DIMM connector, CMDCLK_x[1,5,7]/CMDCLK_x[1,5,7]#, require exact matching of the trace lengths from MCH internal pad to the pins of the second DIMM connector.

> CMDCLK_x0 = CMDCLK_x0# = CMDCLK_x4 = CMDCLK_x4# = CMDCLK_x6 = CMDCLK_x6#

and

> CMDCLK_x1 = CMDCLK_x1# = CMDCLK_x5 = CMDCLK_x5# = CMDCLK_x7 = CMDCLK_x7#

Note that the differential clocks must also be tuned with the data strobes, address/command, and control signals. Figure 6-11 shows the length matching requirements for the differential clock signals.

Figure 6-11. CMDCLK to CMDCLK# Trace Length Matching Requirements
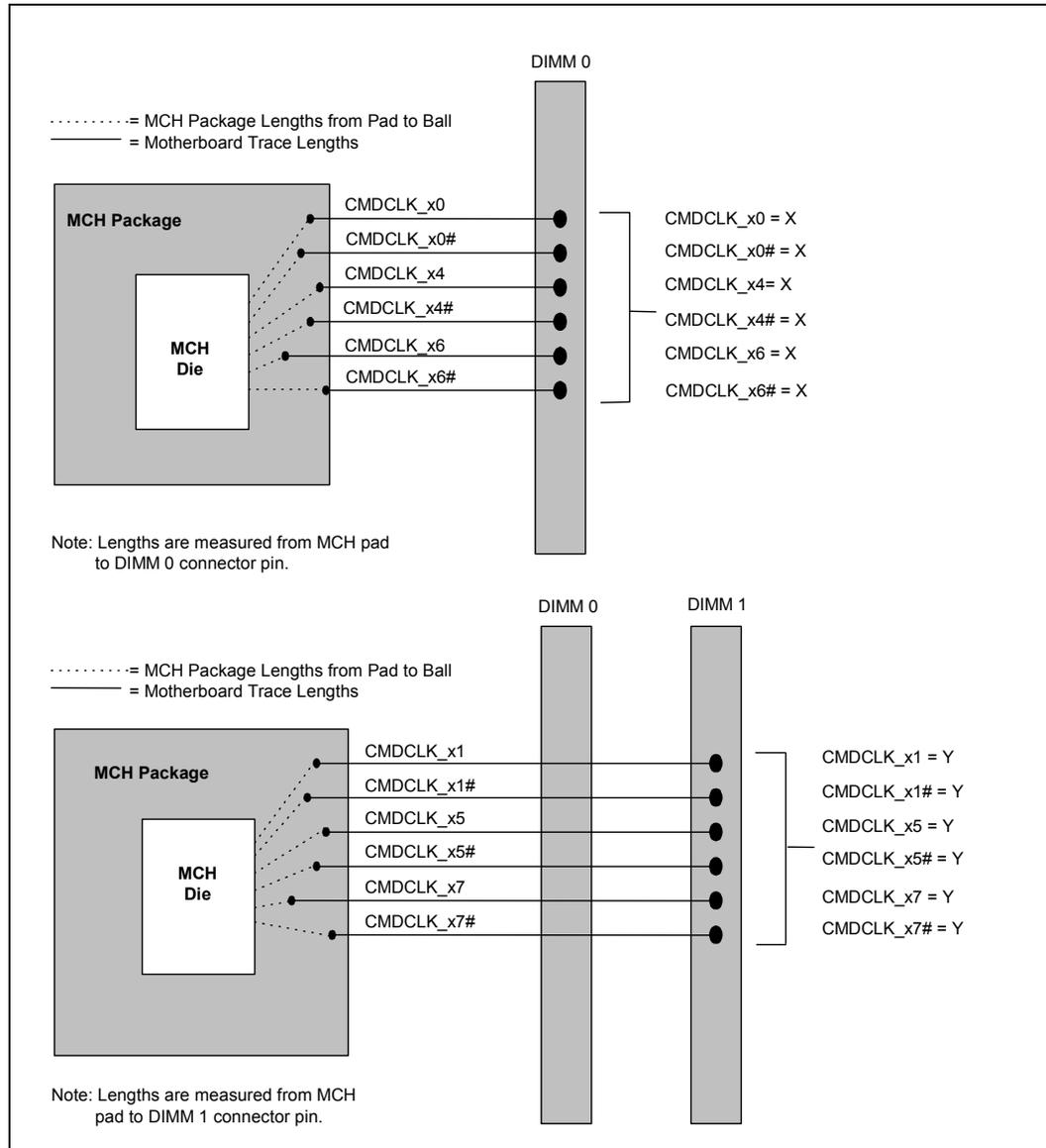
6.2.3 Data Signals — DQ_x[63:0], DQS_x[17:0], CB_x[7:0]

The MCH data signals are source synchronous signals that include the 64-bit wide data bus, 8 check bits, and 9 data strobe signals. DQS_x[17:9] are needed only for x4 devices that are unique to registered memory. The signals DQS_x[17:9] can be tied directly to ground at the DIMMs. Table 6-7 summarizes the DQ/CB to DQS mapping.

Table 6-7. Signals and Associated Strobe

Signal	Associated Strobe
DQ_x[7:0]	DQS_x0
DQ_x[15:8]	DQS_x1
DQ_x[23:16]	DQS_x2
DQ_x[31:24]	DQS_x3
DQ_x[39:32]	DQS_x4
DQ_x[47:40]	DQS_x5
DQ_x[55:48]	DQS_x6
DQ_x[63:56]	DQS_x7
CB_x[7:0]	DQS_x8

It is important to note that the DQ and CB signals must be length matched only to their associated DQS in board etch length—the lengths do not have to account for package compensation. The DQSs and DQ/CBs must match in length only from the MCH ball to DIMM pin. However, the strobe signals (DQS) do have to package compensate when determining their minimum length relative to the command clocks. The following sections provide more information on the length tuning method.

Resistor packs are acceptable for the parallel data and data strobe termination resistors (R_{TT}), but data and strobe signals should not be routed to the same resistor pack (RPACK) used by address/command, or control signals.

Figure 6-12 and Table 6-8 describe the recommended topology and layout routing guidelines for the DDR-SDRAM data signals.

Note: It is important to note that the data/strobe groups require a "mixed impedance" topology. The lead-in length from the MCH to the first DIMM is a lower impedance than the segment connecting the first DIMM to the second DIMM and continuing to the termination resistor.

The variables in the figure are:

> P = MCH package trace from silicon to the package ball
> A = Board trace from the ball of the MCH to the first DIMM pin
> B = Board trace from the first DIMM to the second DIMM pin
> C = Board trace from the second DIMM pin to the termination resistor pin

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Figure 6-12. Data Signal Routing Topology
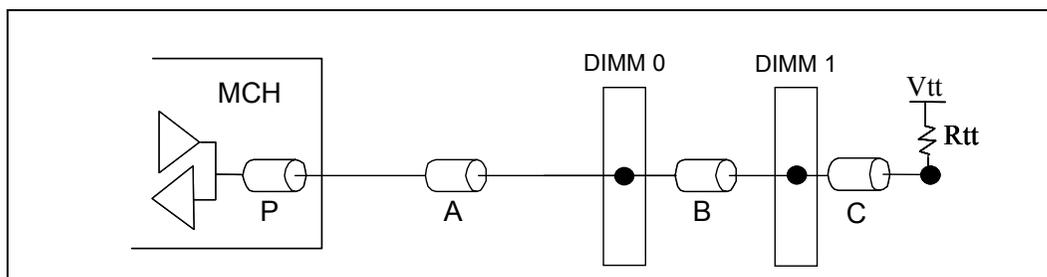
Table 6-8. Data Signal Group Routing Guidelines (Channel A and B)

Parameter	Routing Guidelines
Signal Group	DQ_x[63:0], CB_x[7:0], DQS_x[8:0]
Topology	Daisy Chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_O)	A = 50 Ω, B, C = 60 Ω ± 10%
Nominal Trace Width	A = 7 mils B, C = 5 mils
Nominal Trace Spacing	MCH to first DIMM = 10 mils data, 12 mils strobe Within DIMM Pin Field = 7 mils From DIMM to DIMM = 15 mils Second DIMM to Rtt = 15 mils
Group Spacing	20 mils minimum from non-DDR related signals.
Trace Length A – MCH Ball to First DIMM Pin	Min = 1.5" Max = 5.5"
Trace Length B – First DIMM Pin to Second DIMM Pin	Min = 1.1" Max = 1.2"
Trace Length C – DIMM Pin to termination resistor pad	Min = 0.1" Max = 1.5"
Termination Resistor (R_{TT})	39 Ω ± 5%
MCH Breakout Guidelines	5 mil width with 5 mil spacing until beyond the package edge
Length Tuning Method	Length matching from the MCH internal die pad to the DIMM connector pin is required for DQ_x[63:0], CB_x[7:0] to DQS_x[8:0]. DQS_x[8:0] requires tuning to the DDR clock signals. See following sections for details.

6.2.3.1 Data Group Signal Length Matching Requirements

6.2.3.1.1 Strobe to Command Clock Length Matching Requirements

The tuning of strobes and differential clock signals must take into account the package lengths internal to the MCH package. Matching requires tuning from the MCH internal pad ball to the pins of the DIMM connector.

To Channel A first DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 3.0$ inches

To Channel B first DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 2.5$ inches

To Channel A second DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 3.3"$

To Channel B second DIMM:

CMDCLK Length = X,
DQS Length = Y,
where $Y \geq X - 2.8"$

Length X and Y to first and second DIMM include the MCH package length + the motherboard trace length from the ball of the MCH to the DIMM. No length matching is required from the second DIMM to the parallel termination resistors. Figure 6-13 shows the length matching requirements between the DQS and clock signals for Channel B only.

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Figure 6-13. Channel B DQS to CMDCLK Trace Length Matching Requirements
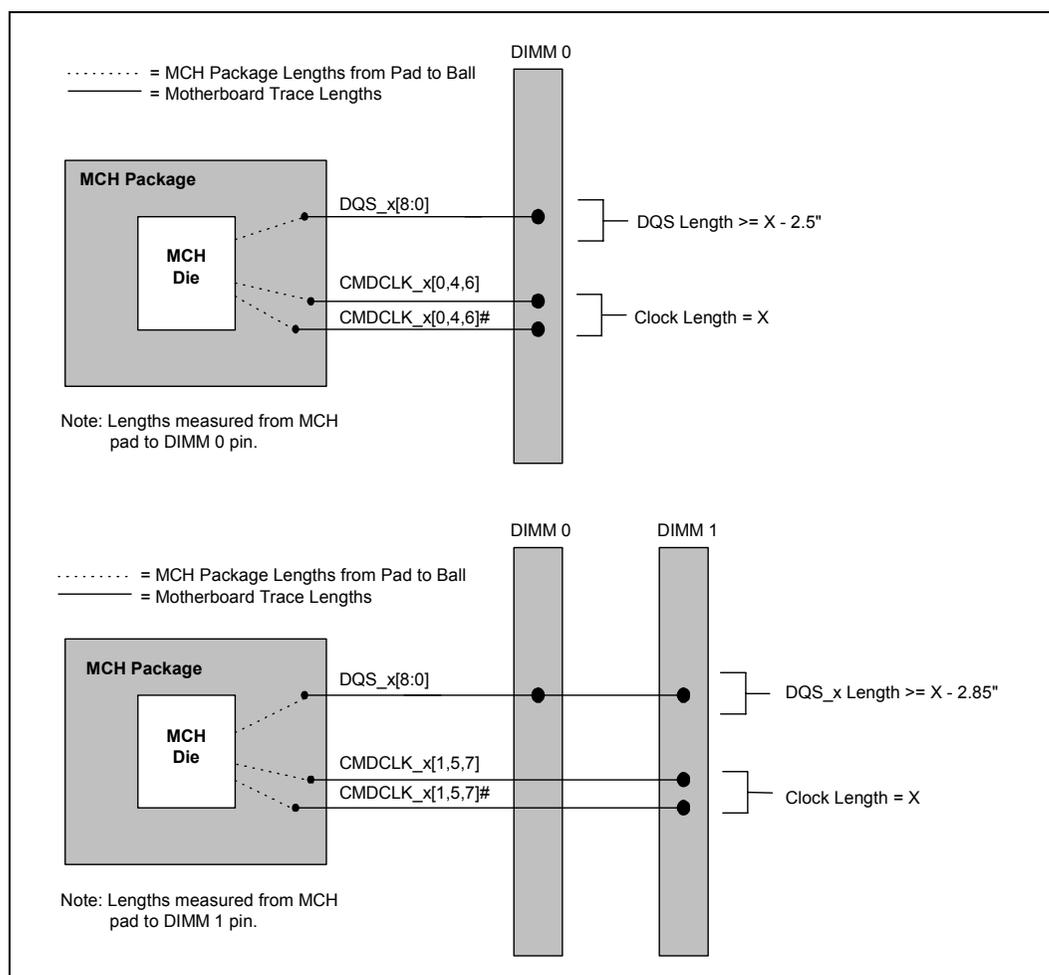
6.2.3.1.2   Data to Strobe Length Matching Requirements

The tuning of the data strobes to the associated data and check bit signals does not require taking package length compensation into account. It is required that the strobes use package compensation when determining the required lengths relative to the command clocks as described in the previous section. However, length matching of the strobe to its associated data and check bits requires accounting only for the board etch. For instance, a command clock length to the first DIMM in Channel A equal to 8 inches requires that the strobe length to the first DIMM have a minimum length of 5 inches (8 inches –3 inches) from die pad to DIMM. If the DQS_x0 happens to have 500 mils of internal package length, the board etch must be 4.5 inches. The eight signals, DQ_x[7:0], would then have to be routed to 4.5 inches, and do not require package compensation.

DQS Length = X,
Associated DQ/CB Byte Group Length = Y,
$(X - 25 \text{ mils}) \leq Y \leq (X + 25 \text{ mils})$

Length X and Y to first and second DIMM do not include the MCH package length—only the motherboard trace length. No length matching is required from the second DIMM to the parallel termination resistors.

Table 6-9 and Figure 6-14 show the length matching requirements between the DQ, CB, and DQS signals.

Table 6-9. DQ/CB to DQS Length Matching Mapping

Signals	Length Mismatch	Relative to
DQ_x[7:0]	± 25 mils	DQS_x0
DQ_x[15:8]	± 25 mils	DQS_x1
DQ_x[23:16]	± 25 mils	DQS_x2
DQ_x[31:24]	± 25 mils	DQS_x3
DQ_x[39:32]	± 25 mils	DQS_x4
DQ_x[47:40]	± 25 mils	DQS_x5
DQ_x[55:48]	± 25 mils	DQS_x6
DQ_x[63:56]	± 25 mils	DQS_x7
CB_x[7:0]	± 25 mils	DQS_x8

It is important to note that the ± 25 mils tolerance must be divided between the segment from the MCH to the first DIMM, and the first DIMM to the second DIMM. For instance, a designer may use ± 15 mils of tolerance on the lead-in length to the first DIMM, and use ± 10 mils on the DIMM to DIMM segment. This ensures that the overall ± 25 mils requirement is met. If the ± 25 mils tolerance were used on each segment individually, a data signal's length could theoretically be out of specification by 25 mils at the second DIMM. The division of the tolerance is arbitrary, but allowing more lenience on the lead-in length is typically the easiest from a routing standpoint.

Figure 6-14. DQ/CB to DQS Length Matching
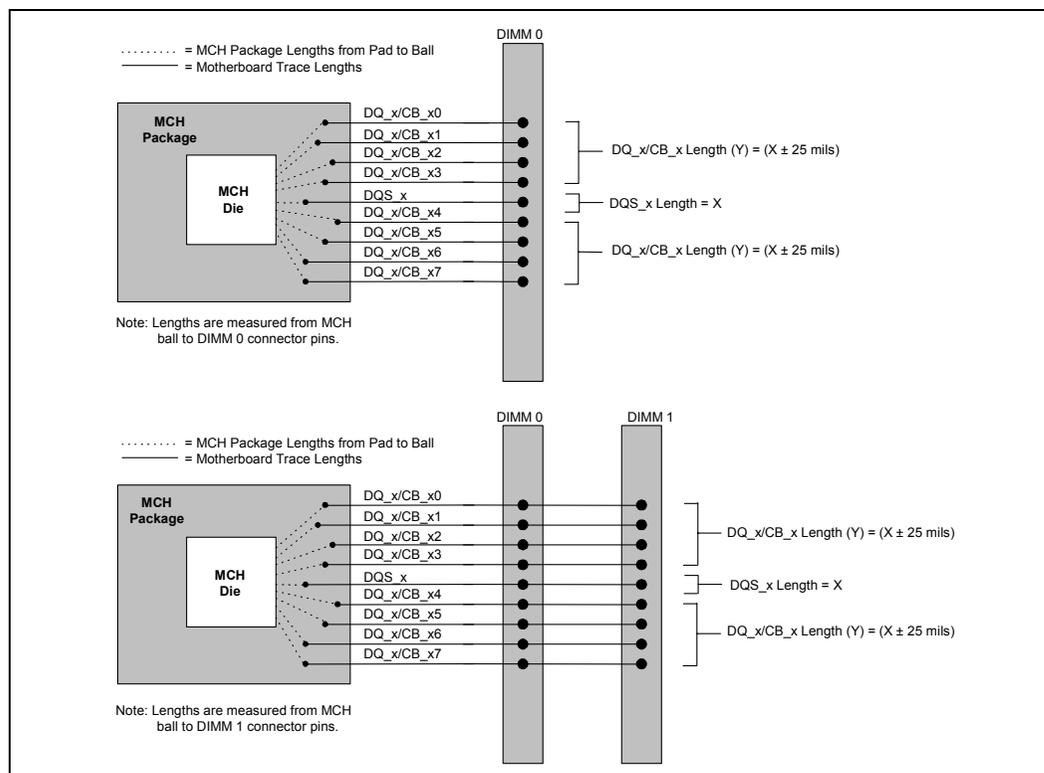
6.2.4 Address/Command Signals — MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#

The MCH address/command signals are source-clocked signals that include 13 system memory address (MA_x[12:0]), 2 bank address (BA), row address select (RAS_x#), column address select (CAS_x#), and write enable (WE_x#) signals. The address/command signals are clocked into the DIMMs using the positive edge of the differential clock signals. The MCH drives the address/command and clock signals together.

Resistor packs are acceptable for the series (Rs) and parallel (R_{TT}) address/command termination resistors, but address/command signals cannot be routed to the same resistor pack (RPACK) used by data, data strobe, or control signals.

There is a required length relationship between the command clocks and the address/command signals, but it usually comes out naturally through normal routing without extra consideration. Details are explained in the following section.

Table 6-10 and Figure 6-15 and Figure 6-16 show the recommended topology and layout routing guidelines for the DDR-SDRAM address/command signals.

Figure 6-15. Address/Command Signal Routing Topology
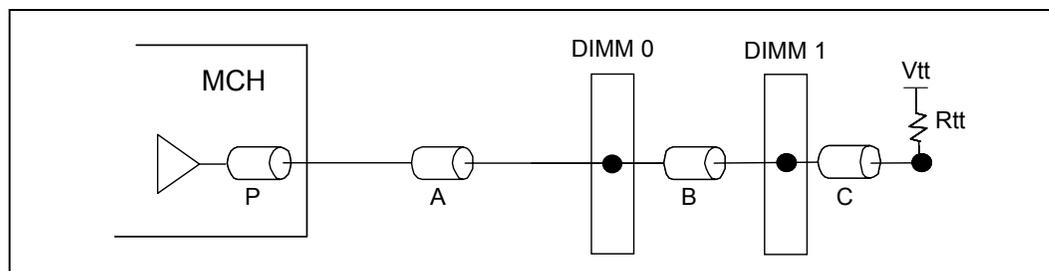
Table 6-10. Address/Command Signal Group Routing Guidelines

Parameter	Routing Guidelines
Signal Group	MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#
Topology	Daisy chain
Reference Plane	Ground Referenced
Characteristic Trace Impedance (Z_O)	A, B, C = 60 Ω ± 15%
Nominal Trace Width	A, B, C = 5 mils
Nominal Trace Spacing from MCH	MCH to first DIMM = 12 mils Within DIMM Pin Field = 7 mils From DIMM to DIMM = 12 mils Second DIMM to Rtt = 12 mils
Group Trace Spacing	20 mils spacing from non-DDR related signals.
Trace Length A – MCH Signal Ball to DIMM 1 pin	Min = 1.5" Max = 6.5"
Trace Length B – DIMM pin to DIMM pin	Min = 1.1" Max = 1.2"
Trace Length C – Last DIMM pin to parallel termination resistor pad	Min = 0.1" Max = 1.5"
Termination Resistor (R_{TT})	56 Ω ± 5%
MCH Breakout Guidelines	5 mil trace width with maximum spacing allowable until beyond the MCH package edge. This breakout length should be as short as possible
Length Tuning Method	MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x# do not require tuning to each other. The lengths are related to the DIMM's associated command clocks. See following section on length requirements.

Figure 6-16. Address/Command Signal Width/Spacing Routing on Lead-in Length
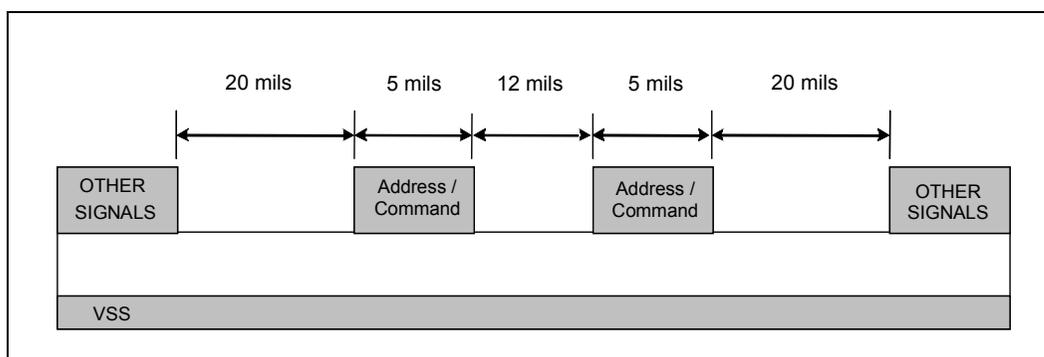
6.2.4.1   Address/Command Group Signal Length Matching Requirements

The tuning of the address/command signals (MA_x[12:0], BA_x[1:0], RAS_x#, CAS_x#, WE_x#) and differential clock signals must take into account the internal package lengths of the MCH package. Matching will require tuning of the address/command signals to the differential clock signals from the MCH ball pad to the pins of the DIMM connector. The address/command signals must be routed 1.5 inches or less than the command clock length to the associated DIMM. The address/command signals route to both DIMMs, while the command clocks route only to one respective DIMM. Therefore, the address/command signal length from the MCH die pad to the first DIMM must be 1.5 inches or less than CMDCLK_x[0,4,6] from the die pad to the first DIMM. The address/command signals lengths from the MCH die pad to the second DIMM must be 1.5 inches or less than the CMDCLK_x[1,5,7] lengths. The following equation reiterate the previous text:

Command Clock Length = X,
Address/Command Length $\leq$ (X – 1.5 inches),

No length matching is required from the last DIMM to the parallel termination resistors. Figure 6-17 shows the length matching requirements between the address/command signals and the clock signals.

Figure 6-17. Address/Command Signal to Command Clock Length Matching Requirements

Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide
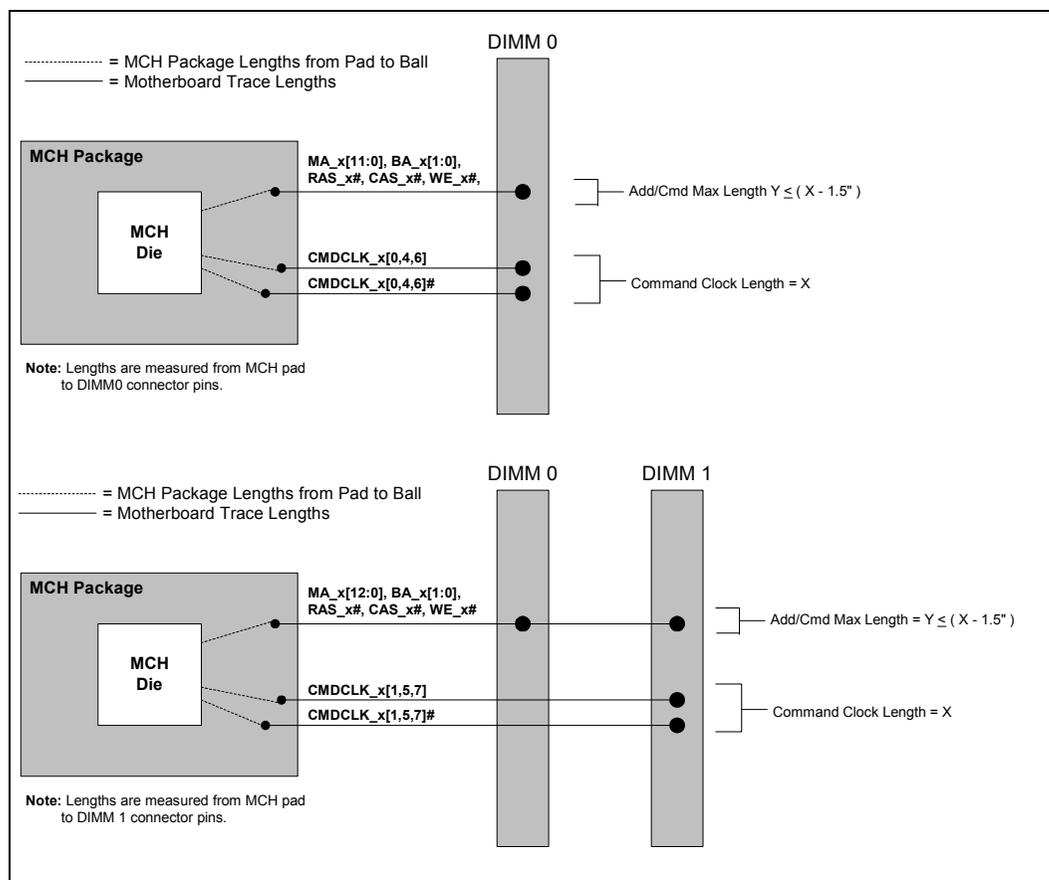
6.2.5   DC Biasing

6.2.5.1   RCVENOUT_A#, RCVENOUT_B#

The MCH provides two pins, RCVENOUT_A# and RCVENOUT_B#, for Channel A and B, respectively. There is an internal delay loop inside the E7205 chipset package that requires an external termination for the driver. The signal must be tied to a resistor divider between the 2.5 V rail and ground. The high and low side resistor values are shown in Figure 6-18. It is important that the two signal pins do not share a single resistor divider even though the recommended circuit is identical for both. The following figures and table show the recommended topology and layout routing guidelines for the RCVENOUT# signal.

Figure 6-18. DDR Feedback RCVENOUT_A#, RCVENOUT_B# Routing Topology
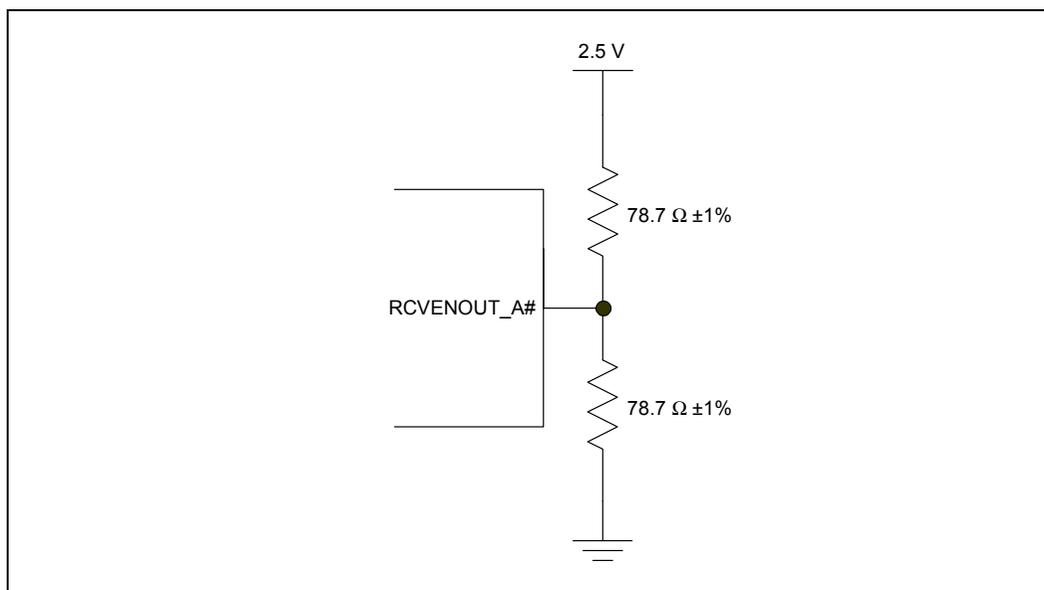
Table 6-11. RCVEN_OUT_A#, RCVENOUT_B# Routing Requirements

Parameter	Routing Guidelines
Signal Group	RCVENOUT_x#
Topology	Point-to-point with resistor divider
Characteristic Trace Impedance	50 Ω
Nominal Trace Width	7 mils
Max Trace Length to Resistor Divider	< 750 mils

6.2.5.2 DRCOMPVREF_H, DRCOMPVREF_V

The MCH provides signals DRCOMPVREF_H and DRCOMPVREF_V for voltage referencing. DRCOMPVREF_H and DRCOMPVREF_V are used for both channel A and B as voltage referencing for the horizontal and vertical buffer resistive compensation circuitry. The DRCOMPVREF_H and DRCOMPVREF_V signals can be shorted together and tied to a single resistor divider network. The values for the biasing circuitry and routing topology are shown in Figure 6-19.

Figure 6-19. DRCOMPVREF_H and DRCOMPVREF_V Routing Topology
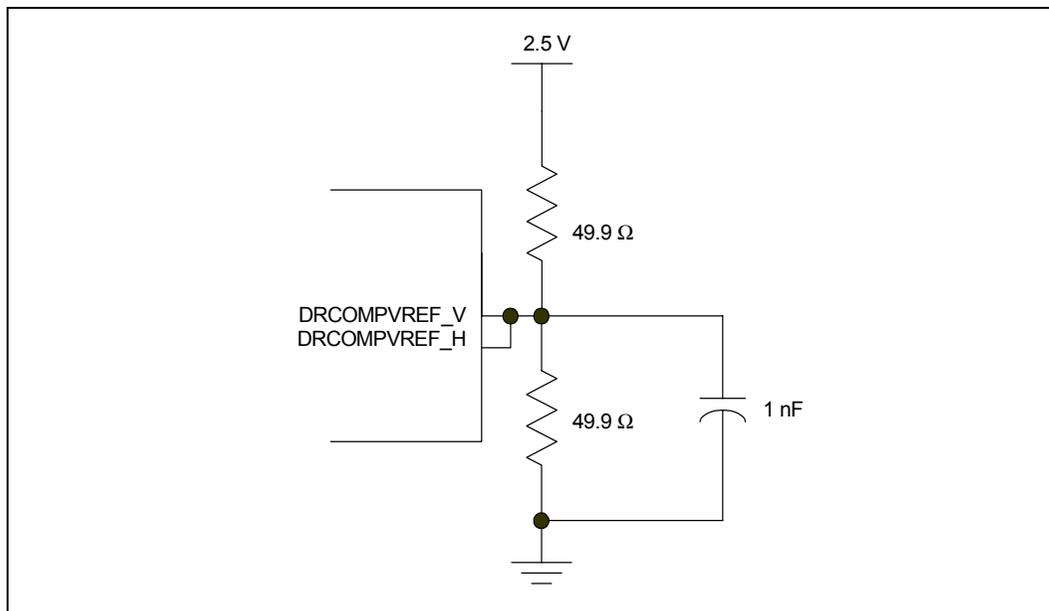
NOTE: The capacitor in the figure is 1 nanoFarad.

Table 6-12. DRCOMPVREF_H and DRCOMPVREF_V Routing Requirements

Parameter	Routing Guidelines
Signal Group	DRCOMPVREF_H, DRCOMPVREF_V
Topology	Point-to-point with resistor divider
Nominal Trace Width	20 mils
Resistor Value (Pull-up and Pull-down)	49.9 Ω ± 1%

6.2.5.3   VREF_A and VREF_B

VREF_A and VREF_B are describe in Section 6.4.4.

6.2.5.4   DRCOMP_H and DRCOMP_V

The MCH provides two signals for resistive compensation. The DRCOMP_H and DRCOMP_V signals are used to calibrate the horizontal and vertical DDR buffers, respectively. It is important that these signals do not share biasing circuitry. The individual signal must tie to its own individual resistor which ties to ground. The values for the biasing circuitry and routing topology are provided in Figure 6-20 and Table 6-13.

Figure 6-20. DRCOMP_H and DRCOMP_V Routing Topology
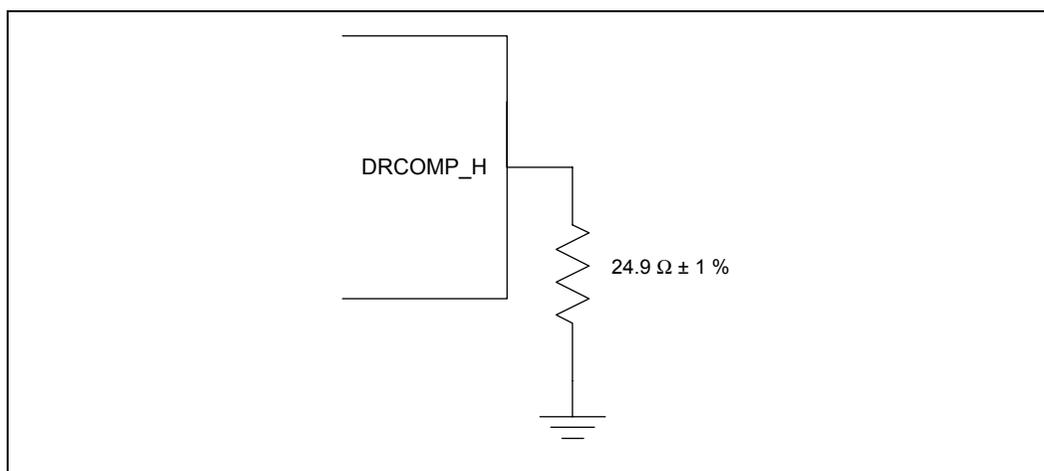
Table 6-13. DRCOMP_H and DRCOMP_V Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DRCOMP_H, DRCOMP_V
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Characteristic Trace Impedance (Z_O)	50 Ω
Nominal Trace Width	7 mils
Resistor Value	24.9 Ω ± 1%
Max Trace Length to Resistor Divider	< 750 mils

6.2.5.5 DDR_STRAP

The MCH provides a signal that is used to indicate to the BIOS the type of memory that is implemented in a motherboard design. This signal should be pulled to 2.5 V. The topology is shown below.

Figure 6-21. DDR_STRAP Routing Topology
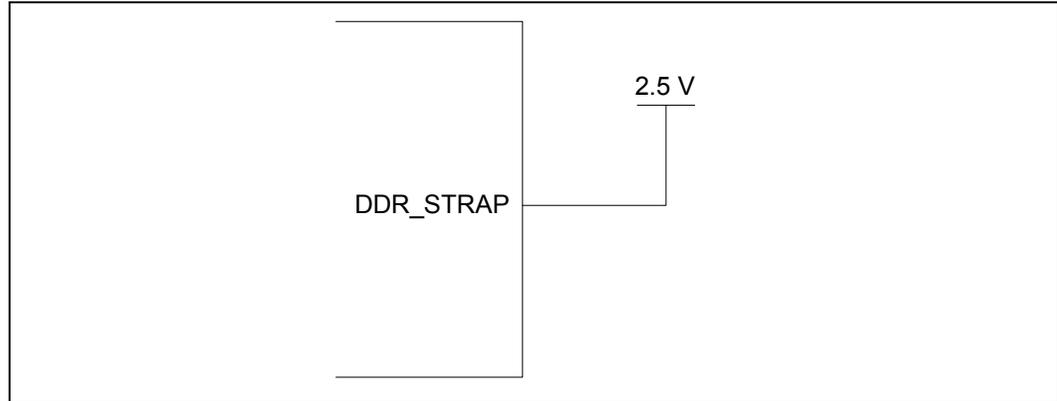
Table 6-14. DDR_STRAP Routing Guidelines

Parameter	Routing Guidelines
Signal Group	DDR_STRAP
Topology	Float or point-to-point with pull-down resistor
Nominal Trace Width	7 mils

6.2.5.6 ODTCOMP

The MCH provides a signal that is used to tune the on-die termination resistors on the DDR interface. This signal should be tied ground through a resistor. The topology and resistor value is shown in Figure 6-22.

Figure 6-22. ODTCOMP Routing Topology
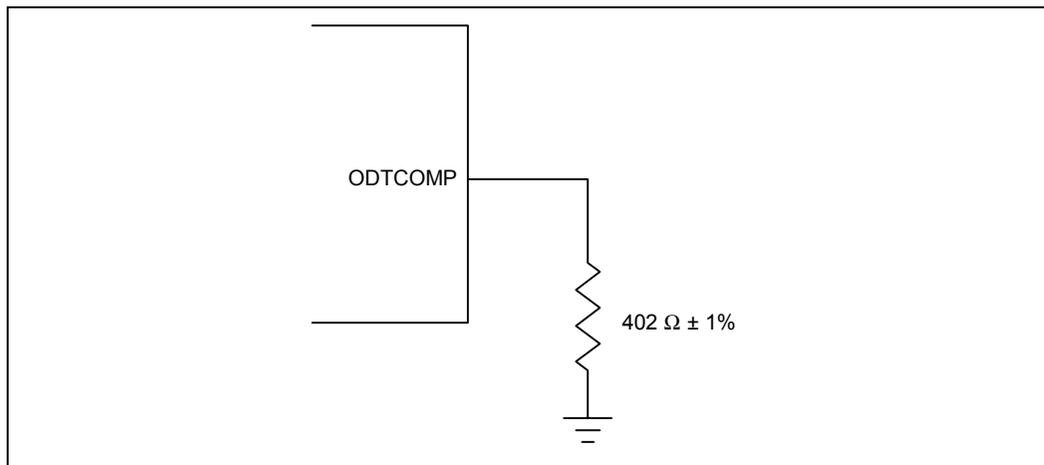
Table 6-15. ODTCOMP Routing Requirements

Parameter	Routing Guidelines
Signal Group	ODTCOMP
Topology	Point-to-point with pull-down resistor
Reference Plane	Ground referenced
Resistor Value	402 Ω ± 1%
Characteristic Trace Impedance (Z_O)	50 Ω
Nominal Trace Width	7 mils
Max Trace Length Limit to Resistor	< 750 mils

6.3 System Memory Bypass Capacitor Guidelines

6.3.1 MCH System Memory Interface Decoupling Requirements

6.3.1.1 MCH System Memory High-Frequency Decoupling

Every MCH ground and power ball in the system memory interface should have its own via. For 2.5 V high-frequency decoupling, a minimum of ten 0603 0.1 µF high-frequency capacitors are required and must be within 100 mils of the MCH package. The vias should be placed within 25 mils of the capacitor pads. The traces from the ground and power vias to the capacitor pad must be as wide as possible. Figure 6-23 shows the MCH DDR 2.5 V high-frequency decoupling capacitors.

Figure 6-23. MCH DDR 2.5 V Decoupling
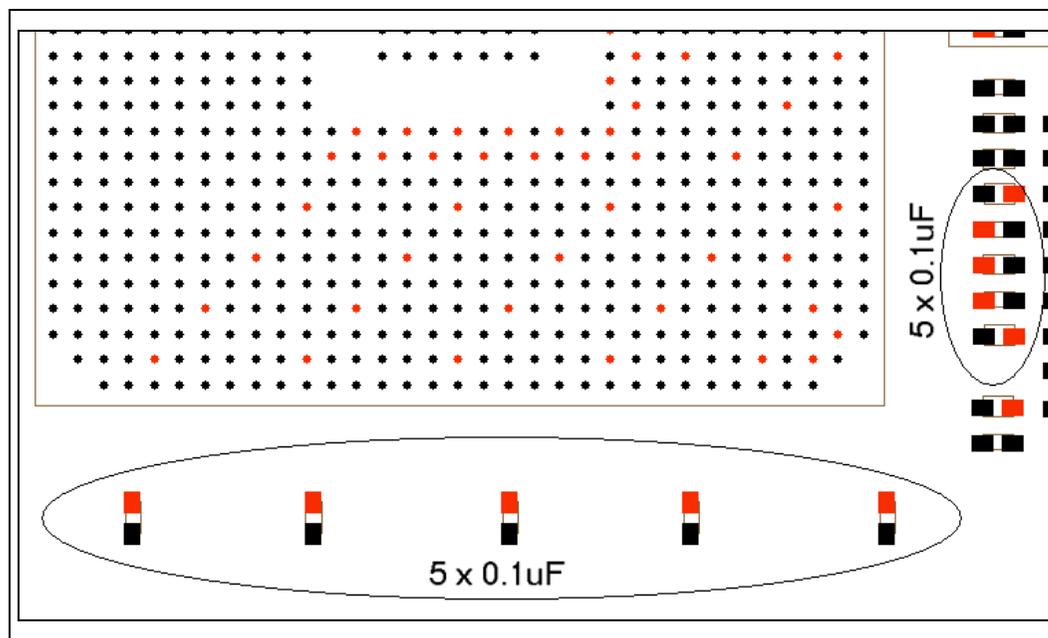
Table 6-16. MCH System Memory Decoupling Capacitor Requirements

Parameter	Guideline
Capacitor Number	Ten 0603 0.1 µF MLC capacitors placed near MCH
Capacitor Placement	Within 100 mils of the MCH
Capacitor Pad to Ground via Trace Width	Route as wide as possible with a minimum width of 18 mils
Vias (Power and Ground)	Placed within 25 mils of the capacitor pad

6.3.1.2 MCH System Memory Low-Frequency Bulk Decoupling

The MCH system memory interface requires low-frequency bulk decoupling. Place four 100 µF electrolytic capacitors between the MCH and the first DIMM connector. These capacitors are in addition to the bulk decoupling required by the 2.5 V regulator (regulator bulk decoupling is design specific).

Figure 6-24. Shared MCH/DIMM 2.5 V Bulk Decoupling Example
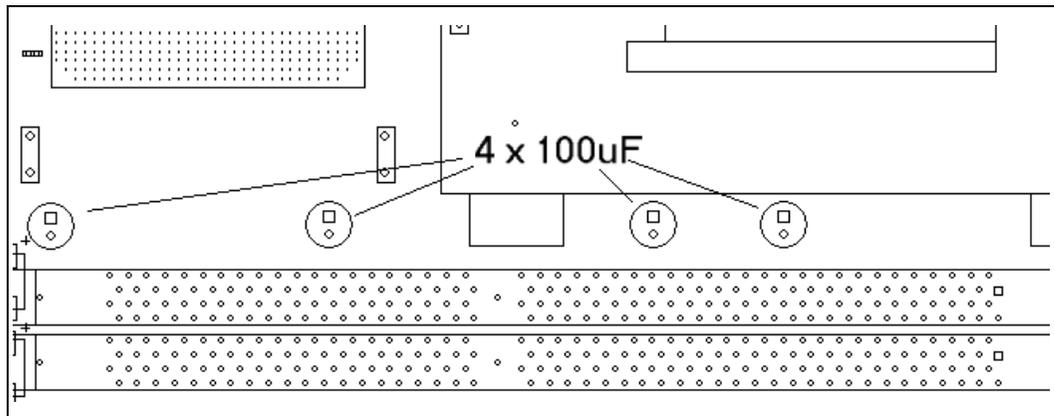
Table 6-17. MCH System Memory Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Four 100 µF capacitors
Capacitor placement	Evenly placed between the MCH and first DIMM pin

6.3.2 DDR-DIMM Decoupling Requirements

The DDR DIMMs require bulk decoupling in addition to the decoupling that is required by the MCH. Place two 100 µF capacitors per DIMM at each end. A 4-DIMM design would use eight total 100 µF caps. Using a 7343-sized capacitor will allow placement under the lever actuated arms of the DIMMs.

Figure 6-25. DIMM Bulk Capacitor Requirements
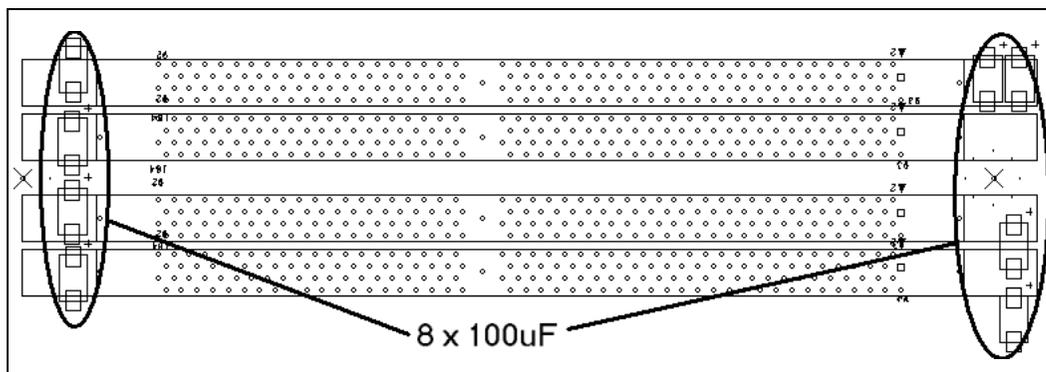
Table 6-18. DIMM Bulk Capacitor Requirements

Parameter	Guideline
Capacitor number	Two 100 µF capacitors per DIMM
Capacitor placement	One placed at both the left side and the right side of the DIMM sockets

6.4 Power Delivery

The following guidelines are recommended for an E7205 chipset DDR system memory design. The main focus of these MCH guidelines is to minimize signal integrity problems and improve the power delivery of the MCH system memory interface and the DDR-DIMMs.

6.4.1 DDR Voltage Regulator Guidelines

E7205 chipset designs using the DDR-SDRAM memory sub-system require several different voltages: 2.5 V, 1.25 V, and VREF. To generate these voltages, a 2.5 V and a 1.25 V regulator are required and must be designed to supply the required voltage and current levels to meet both the MCH and the DDR-SDRAM device requirements. DDR voltage regulation will be governed by either an on-motherboard regulator circuitry or a module with the necessary complement of external capacitance, and will vary according to the needs of different OEM design targets.

6.4.2   Power Delivery Guidelines for 2.5 V

Attention must be paid to the 2.5 V power plane to ensure proper MCH and DIMM power delivery. This 2.5 V plane must extend from the MCH 2.5 V power vias all the way to the 2.5 V DDR voltage regulator and its bulk capacitors. The 2.5 V power plane under the DIMM connectors must encompass all of the DIMM 2.5 V pins.

The 2.5 V power plane, which is generated by the 2.5 V regulator, is used to supply power to the MCH 2.5 V I/O Ring, the DDR-SDRAM 2.5 V Core, and the DDR-SDRAM 2.5 V I/O Ring. The 2.5 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

6.4.3   Power Delivery Guidelines for 1.25 V

The 1.25 V power plane, which is generated by the 1.25 V regulator, is used to supply the DDR termination voltage (VTT). Special considerations must be taken for the 1.25 V regulator design because it must be able to source and sink a significant amount of current. The 1.25 V regulator should be placed at the end of the DDR channel near the VTT Termination Island.

6.4.4   DDR Reference Voltage

The DDR system memory reference voltage (VREF) is used by the DDR-SDRAM devices to compare the input signal levels of the data, command, and control signals, and is also used by the MCH to compare the input data signal levels. VREF must be generated as shown in the Figure 6-26. It should be generated from a typical resistor divider using 1%-tolerance resistors. The VREF resistor divider should be placed no further than 1.0 inch from the DIMMs. Additionally, VREF must be decoupled locally at each DIMM connector and at the MCH. Finally, the VREF signal should be routed with as wide a trace as possible (12 mils minimum width), and isolated from other signals with a minimum of 12 mils spacing. During breakout from the MCH, a minimum of 7 mil spacing can be maintained for a maximum length of 350 mils.

Figure 6-26. DDR VREF Generation Example Circuit
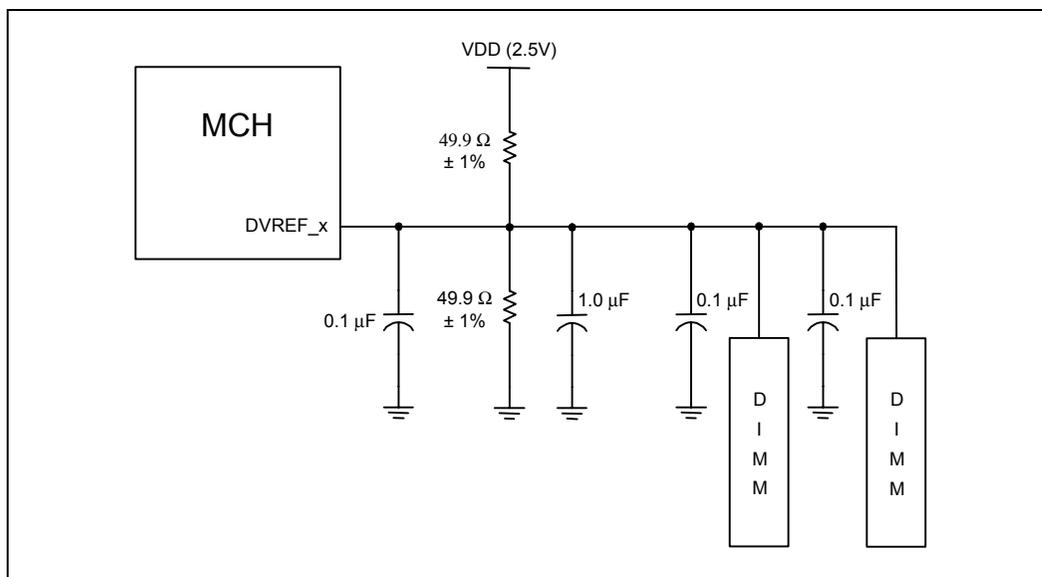
Table 6-19. DDR VREF Generation Requirements

Parameter	Guideline
VREF Routing	Minimum 12 mils wide and separated from other traces with a minimum 12 mils spacing, except during breakout, which is allowed 7 mil spacing to other signals for no more than 350 mils.
Voltage Divider	Place resistor divider consisting of two 49.9 Ω ± 1% resistors. Minimize distance from MCH to resistor divider.
Decoupling Requirements	Three 0603 0.1 µF capacitors One 0603 1.0 µF capacitor
Decoupling Placement	Place one 0.1 µF decoupling cap at each of the DIMM sockets, and one 0.1 µF decoupling cap at the MCH. Place the 1.0 µF decoupling cap near the voltage divider.

6.4.5   DDR VTT Termination

All DDR signals, except the command clocks, must be terminated to 1.25 V (VTT) using 5% resistors at the end of the channel opposite the MCH. Place a solid 1.25 V (VTT) termination island on the top signal layer, just beyond the last DIMM connector. The VTT termination island must be at least 50 mils wide. Use this termination island to terminate all DDR signals using one resistor per signal. Resistor packs are acceptable, with the understanding that the signals within an RPACK are from the same DDR signal group. No mixing of signals from different DDR signal groups is allowed within an RPACK. The parallel termination resistors connect directly to the VTT island on the top signal layer.

Figure 6-27. DDR VTT Termination Island Example
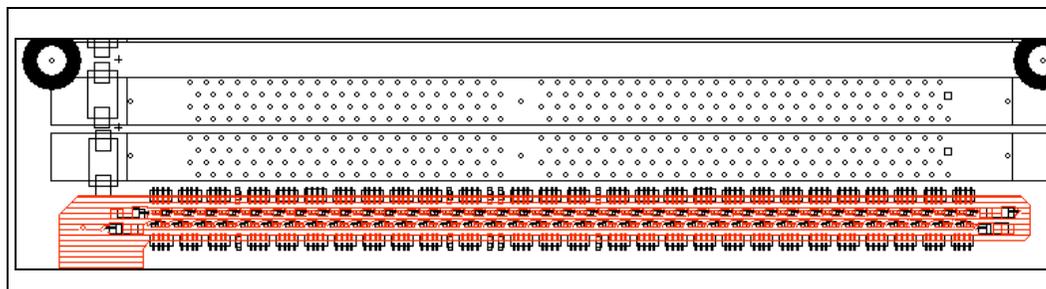
Table 6-20. DDR VTT Termination Island Requirements

Parameter	Guideline
Island Width	50 mils minimum
Resistor and capacitor connectivity	Connect termination resistors and decoupling capacitors directly to the termination island

6.4.5.1   VTT Termination Island High-Frequency Decoupling Requirements

The VTT Island must be decoupled using high-speed bypass capacitors—one 0603 0.1 µF capacitor per two DDR signals, or two capacitors per RPACK. These decoupling capacitors connect directly to the VTT island and to ground, and must be spread-out across the termination island so that all the parallel termination resistors are near high-frequency capacitors. The capacitor ground via should be within 25 mils of the capacitor pad and the via, and the pad should be connected with as wide a trace as possible. The distance from any DDR termination resistor pin to a 0.1 µF VTT capacitor pin must not exceed more than 100 mils.

Finally, place two 4.7 µF ceramic capacitors on each end of the termination island (see Figure 6-30).

Figure 6-28. DDR VTT Termination 0.1 µF High-Frequency Capacitor Example 1
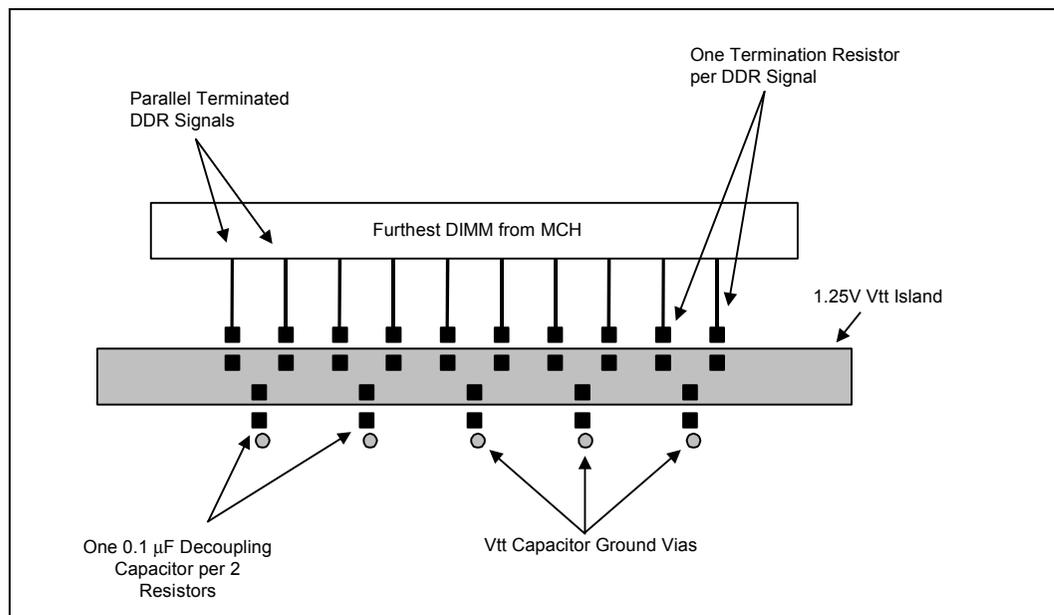
Figure 6-29. DDR VTT Termination and High-Frequency Capacitor Example 2
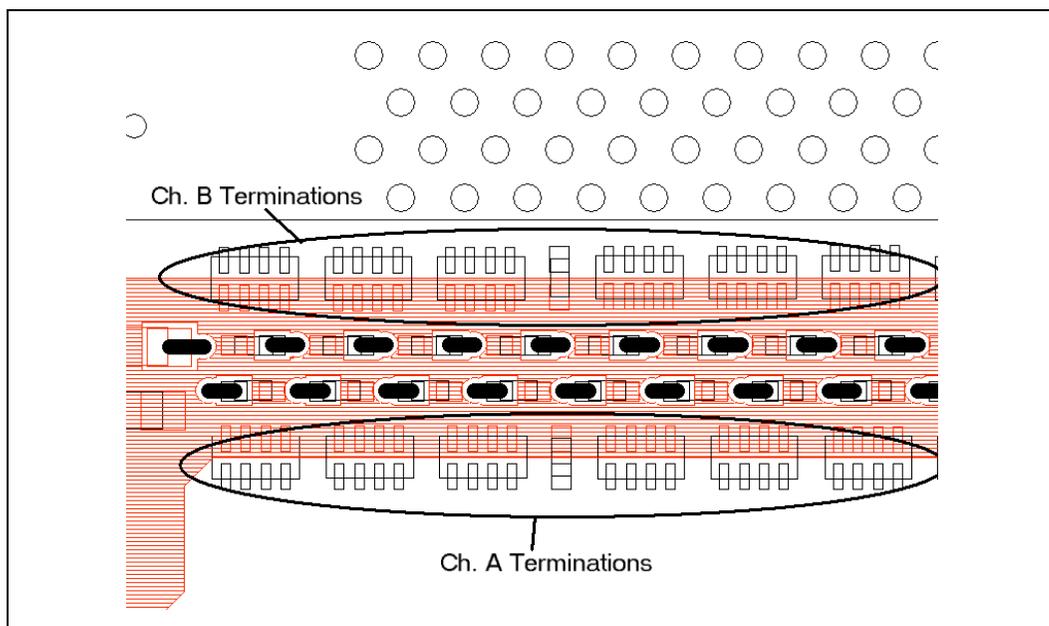
Figure 6-30. DDR VTT Termination 4.7 µF High-Frequency Capacitor Example
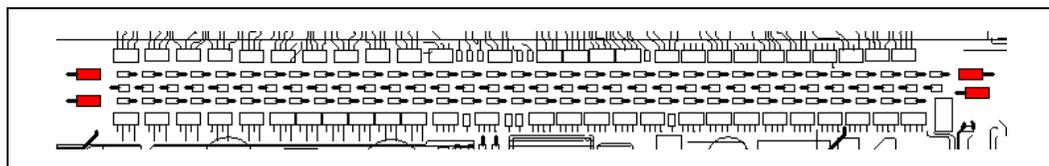
Table 6-21. DDR VTT Termination Island High-Frequency Decoupling Requirements

Parameter	Guideline
0.1 µF capacitors	Place one decoupling cap for every two DDR signals/ termination resistors (or two caps for every RPACK). The distance from any termination resistor to decoupling capacitor should not exceed 100 mils.
4.7 µF capacitors	Four capacitors required. Place two capacitors at each end of the termination island.

6.4.5.2 VTT Termination Island Low-Frequency Bulk Decoupling Requirements

The VTT termination island requires low-frequency bulk decoupling. The output of the 1.25 V regulator must have enough bulk decoupling to ensure the stability of the regulator. The amount of bulk decoupling required at the output of the 1.25 V regulator will vary according to the needs of specific OEM design targets.

6.4.6 Power Sequencing Requirements

6.4.6.1 MCH Power Sequencing Requirements

There are no MCH power sequencing requirements. All MCH power rails should be stable before deasserting reset. Common design practice is to have all MCH power rails come up as close in time as possible.

6.4.6.2 DDR-SDRAM Power Sequencing Requirements

There are no DDR-SDRAM power sequencing requirements except that 1.25 V must come up after the 2.5 V rail. Because of this requirement, designs should have the 1.25 V rail derived from a regulator with 2.5 V as its input.

Hub Interface 1.5 7

This chapter describes the routing guidelines for the 8-bit hub interface 1.5. This hub interface connects the MCH to the ICH4 (see Figure 7-1). This interface supports only the parallel termination mode. Therefore, the DPRSLPVR pin on the ICH4 must be tied to ground to ensure that it will run in parallel mode.

The MCH and ICH4 ball assignments are optimized to simplify the hub interface routing between these devices. The hub interface signals must be routed directly from the MCH to the ICH4 with all signals referenced to VSS. Layer transitions should be keep to a minimum. If a layer change is required, use only two vias per net and keep all data signals and associated strobe signals on the same layer.

The 8-bit hub interface signals are all in the same data group (i.e., all signals are associated with HI_STBS/HI_STBF).

Figure 7-1. 8-Bit Hub Interface1.5 Routing
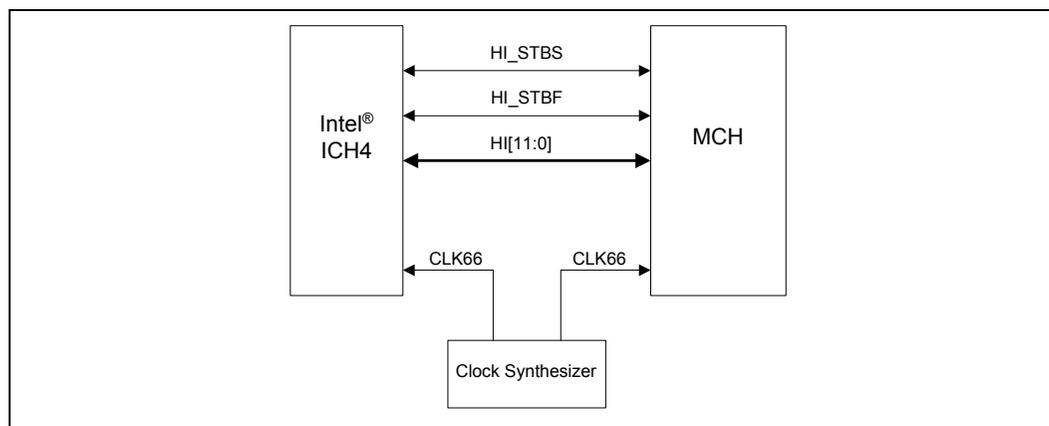
7.1   Hub Interface 1.5 High-Speed Routing Guidelines

The Hub Interface 1.5 signal groups are listed in Table 7-1. The general routing parameters for the HI 1.5 signals are listed in Table 7-2.

Table 7-1. HI 1.5 Signal Groups

Group	Signals
Common Clock Signal	HI_x[11:8]
Source Synchronous Signal	HI_x[7:0], HI_STBF, HI_STBS
Miscellaneous Signal	HIRCOMP, HISWNG, HIVREF

Table 7-2. HI 1.5 Routing Parameters

System Type	Trace Length Min-Max	Trace Z_O	Trace Width/Spacing	Breakout Width/ Spacing
266 MT/s	3"–20"	50 Ω ± 10%	Data to Data: 7/13 mils Strobe to Strobe: 7/13 mils Strobe to Data: 7/18 mils Other signals to Data: 7/13 mils	7/5 mils at MCH (max dist = 750 mils) 7/5 mils at Intel® ICH4 (max dist = 500 mils)

Each strobe signal trace must be the same length for HI 1.5 devices on the motherboard, and each data signal trace must be matched within ± 100 mils.

7.2 Hub Interface 1.5 Generation/Distribution of Reference Voltages

The nominal Hub Interface 1.5 reference voltage is 0.35 V ± 5%. The 8-bit hub interface on the MCH has a dedicated HIVREF pin to sample this reference voltage. In addition to the reference voltage, a reference swing voltage must be supplied to control buffer voltage swing characteristics. The nominal hub interface 1.5 reference voltage swing must be 0.8 V for the MCH and ICH4. Each hub interface on the MCH has a dedicated HISWNG pin to sample this reference swing voltage. The ICH4 also has a dedicated reference swing voltage pin (HITERM). Refer to the Table 7-3. Both of these reference voltages can be generated locally with a single voltage divider circuit. Figure 7-2 shows an example voltage divider circuit.

Table 7-3. HI 1.5 Reference Circuit Specifications

Reference Voltage Specification (V) (HIREF)	Reference Swing Voltage Specification (V) (HITERM)	1.3 V Voltage DIvider Circuit Recommended Values	1.5 V Voltage DIvider Circuit Recommended Values	
			Group 1[1]	Group 2[1]
0.350 ± 5%	For Intel® ICH4 = 0.8 For MCH = 0.8	R1 = 402 Ω ± 1% R2 = 511 Ω ± 1% R3 = 549 Ω ± 1% C1 = 0.1 µF C2 = 0.01 µF	R6 = 80.6 Ω ± 1% R5 = 51.1 Ω ± 1% R4 = 40.2 Ω ± 1% C1 = 0.1 µF C2 = 0.01 µF	R6 = 226 Ω ± 1% R5 = 147 Ω ± 1% R4 = 113 Ω ± 1% C1 = 0.1 µF C2 = 0.01 µF

NOTE:
1. Use only resistors from group 1 or 2—do not mix values from these groups.

Figure 7-2. HI 1.5 Locally Generated Reference Divider Circuits
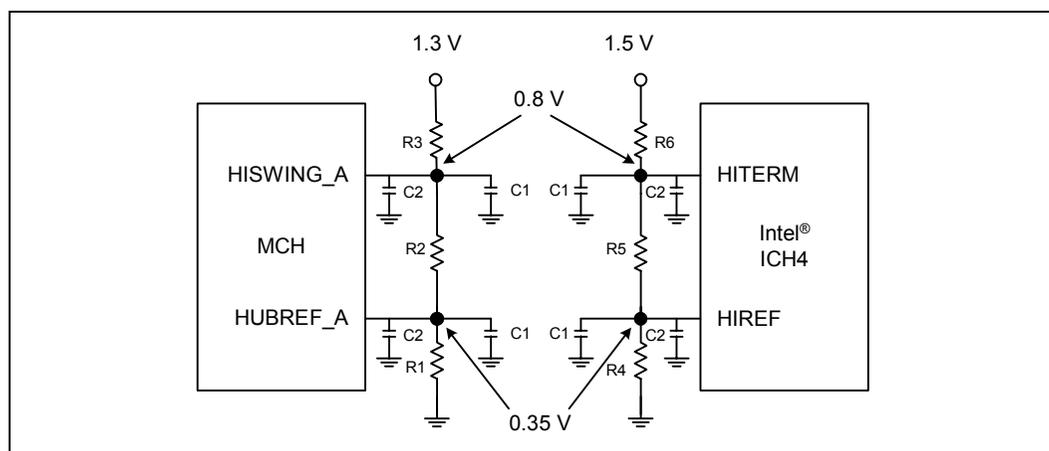
All resistor values must be rated at ± 1% tolerance. The selected resistor values must also ensure that the reference voltage and reference swing voltage tolerance are maintained over the input leakage specification. A 0.1 µF capacitor (C1 in Figure 7-2) should be placed close to each resistor divider, and a 0.01 µF bypass capacitor (C2 in Figure 7-2) should be placed within 0.25 inches of reference voltage pins. The trace length from the voltage divider circuit to the HIREF and HUBREF pins must be no longer than 3.5 inches.

Both the voltage reference and voltage swing reference signals should be routed at least 20 mils to 25 mils from all other signals.

7.3 Hub Interface 1.5 Resistive Compensation

The hub interface uses a resistive compensation signal (RCOMP) to compensate buffer characteristics for temperature, voltage, and process.

Table 7-4. Hub Interface 1.5 RCOMP Resistor Values

Component	Trace Impedance	RCOMP Resistor Value	RCOMP Resistor Tied To
MCH	50 Ω ± 10%	R1 = 32.4 Ω ± 1%	VCC1_3
Intel® ICH4	50 Ω ± 10%	R2 = 43.3 Ω ± 2%	VCC1_5

Figure 7-3. Hub Interface 1.5 RCOMP Circuits
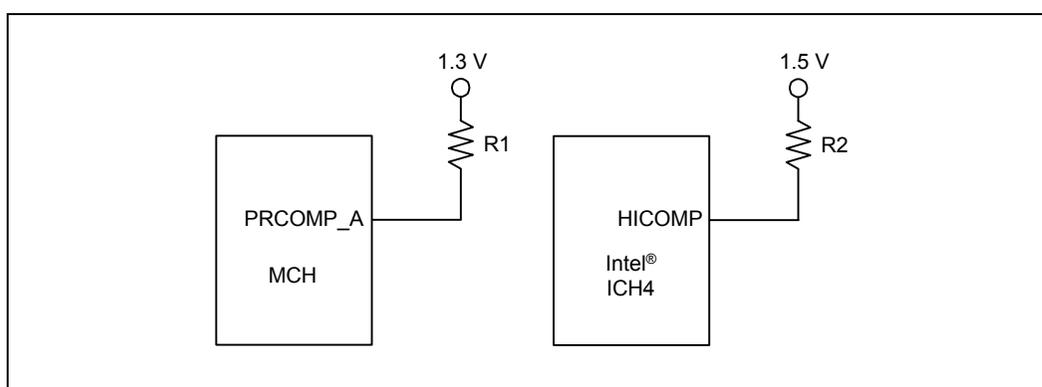
7.4 8-Bit Hub Interface Decoupling Guidelines

To improve I/O power delivery, use two 0.1 µF capacitors per each component (i.e., the ICH4 and MCH). These capacitors should be placed within 150 mils of each package, adjacent to the rows that contain the hub interface. If the layout allows, wide metal fingers running on the VSS side of the board should connect the VCC1_5/VCC1_3 side of the capacitors to the VCC1_5/VCC1_3 power pins. Similarly, if layout allows, metal fingers running on the VCC1_5/VCC1_3 side of the board should connect the ground side of the capacitors to the VSS power pins.

Serial ATA 8

This chapter provides guidelines for integrating discrete high-speed Serial ATA onto systems based on the E7205 chipset using ICH4. The topics discussed include layout and routing guidelines, and platform integration.

Note: The guidelines recommended in this chapter are based on experience and simulation work performed at Intel while developing Serial ATA. This work is ongoing, and the recommendations and considerations are subject to change. Table 8-1 shows a comparison of the Serial ATA (Gen I) and Parallel ATA technologies.

Table 8-1. Serial ATA vs. Parallel ATA

Parameter	Serial ATA	Parallel ATA
Performance	150 MB/s	100 MB/s
Max Cable Length	39.37 inches	18 inches
Signaling Tolerance	250 mV	5 V
Signal pins on cable	4	26

Figure 8-1 shows the Serial ATA solution using a discrete host controller.

Figure 8-1. Uni-Processor System Block Diagram (Intel® ICH4) with Serial ATA
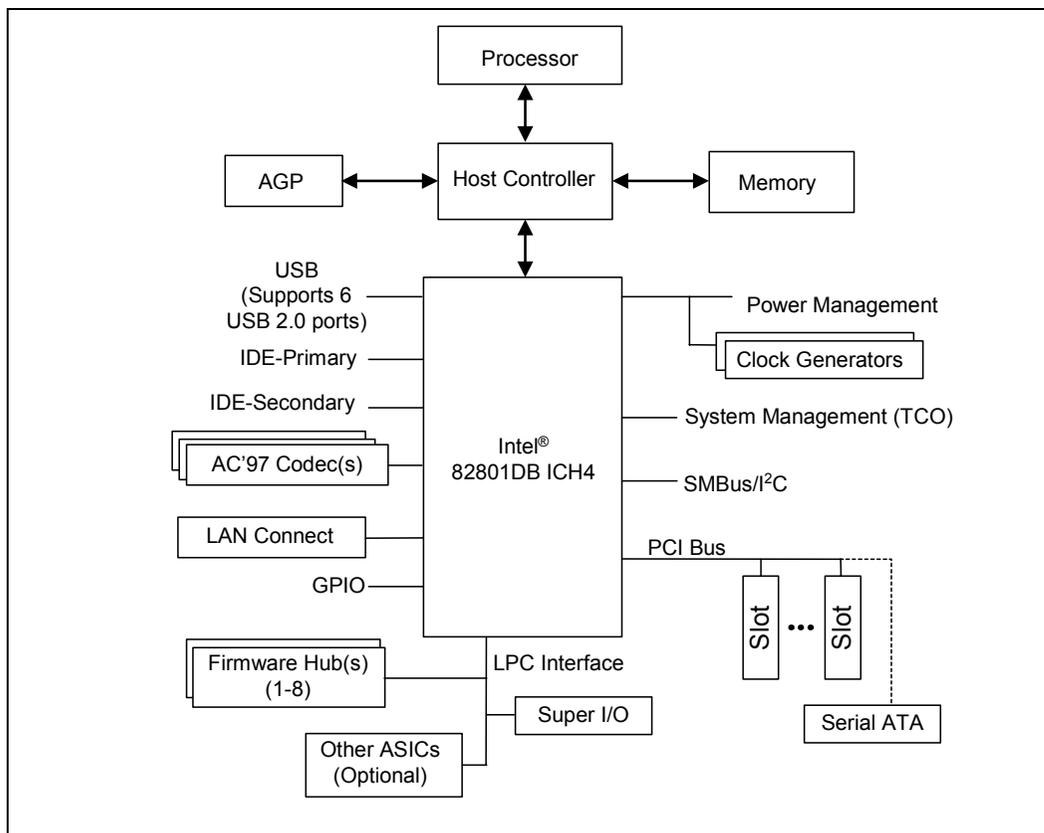
8.1 Host Controller Details

The E7205 chipset platform will use the Sil3112* device from Silicon Image. This section gives details on package type, mechanical specifications, function, and general layout of the part.

8.1.1 Functional Description

The Sil3112 is a PCI-to-Serial ATA controller chip that transfers data between the PCI bus and storage media. The Sil3112 communicates with the ICH4 over the PCI bus, and communicates with storage media over the Serial ATA bus.

Note: The Sil3112 PCI interface is compliant with *PCI Local Bus Specification (Revision 2.2)*.

8.1.2 Mechanical Specifications

Figure 8-2. Host Controller Mechanical Specifications (144-pin TQFP Package Type)
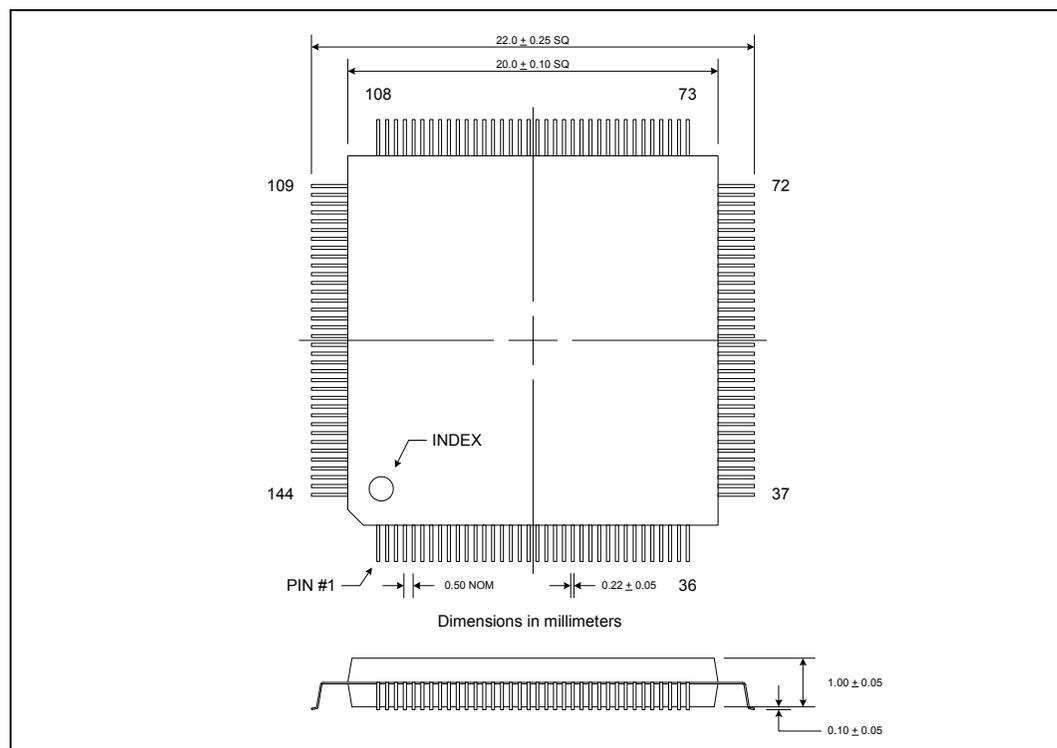
8.1.3   Quadrant Layout

Figure 8-3. Quadrant Layout of the Host Controller
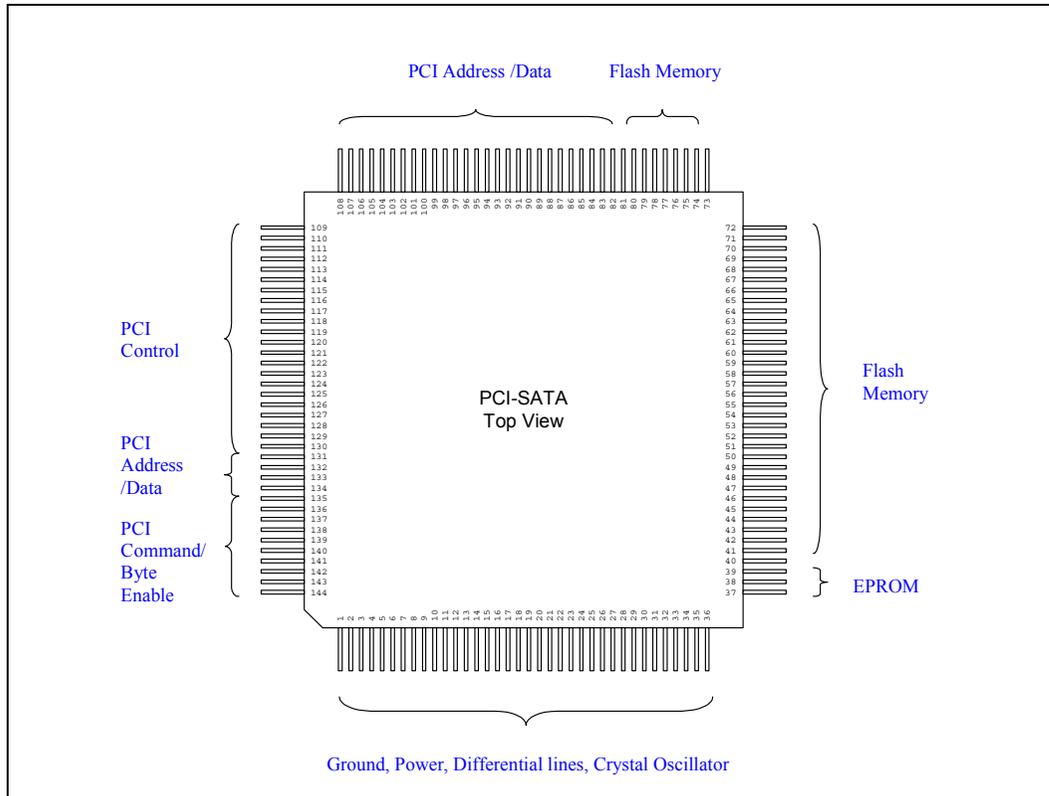
8.2 Layout/Routing Guidelines

8.2.1 General Recommendations

8.2.1.1 Ground Planes

Considerations for designing the ground planes around differential lines:

- The ground plane over/under the differential traces should be a continuous plane from chip ground to connector ground.

- Any discontinuity or a split of the ground plane should be avoided.

- The ground plane should have ground contact to both the chip analog ground (pin numbers 8, 11, 14,17, 21, 24, 27, 30, 34), and at connector ground.

- The ground plane should extend more than twice the width of the signal trace beyond the differential pair.

8.2.1.2 Clock Topology

The Serial ATA device requires a 25 MHz crystal in combination with it own PLLs. A 22 pF capacitor to each of the clock pins (XTAL0, XTAL1) is recommended.

Figure 8-4. Example of Clock Implementation
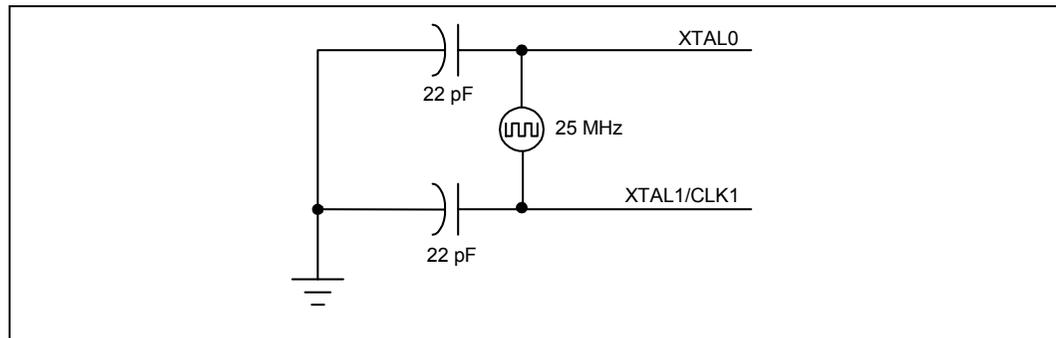
8.2.2 Routing Constraints

This section describes critical considerations for routing signals and power to the chip and connector. Three of the topics discussed are stack-up, trace length, and connector placement.

8.2.2.1 6-Layer Stack-Up PCB

Figure 8-5. Microstrip PCB Stack-Up
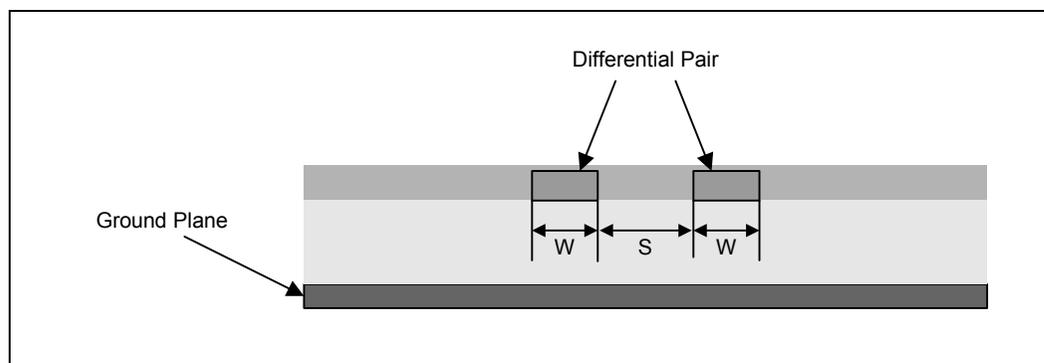
Table 8-2. Microstrip PCB Stack-Up

Parameter	Value
S (Separation between differential pair)	7 mils
W (width of transmission line)	5 mils
Z_o = Z11	58 Ω
Z_{diff} (Differential Line Impedance)	100 Ω ± 5 Ω

8.2.2.2 Differential Lines Discussion

8.2.2.2.1 Length

The length of the differential pairs (Tx pair and Rx pair) should be as short as possible. The recommended maximum length constraint is 3.9 inches. If the maximum length is exceeded, the high-frequency differential signal will suffer signal attenuation and increased rise time/fall time.

8.2.2.2.2 Length Matching

The two traces in a differential pair should be matched in length. The lines should have same line length, number of vias, transmission line structure, and pad sizes. The traces in a differential pair should match in length within 17.72 mils. The 17.72 mils difference of the signal propagation produces about 3 ps skew.

8.2.2.2.3   Pads and Stubs

The size of the soldering pads on the differential pair should be small to reduce the parasitics of the pads. It is recommended to keep the pad size 60 mils x 30 mils or smaller. This will enable the parasitic capacitance of a bonding pad to be kept below 50 pF. The capacitance loading effect of the conventional pad (with ground plane under the pad) is not acceptable. Hence, the ground plane under the bonding pad must be removed. The effect of other metals on the opposite side of the PCB core can be ignored because the thickness of the core is 40 mils, which is relatively thick. Stubs should be avoided on the differential lines.

8.2.2.2.4   Crosstalk

To reduce the crosstalk noise between the nearby differential pairs or to other adjacent signal lines, grounded shield guard can be inserted between the pairs or before the adjacent lines to the differential pairs. To improve the effect of the shields, the shield guard should be grounded at the chip and at the Serial ATA connector. Figure 8-6 shows the grounded shield guard for the microstrip line structure. It is recommended that $Sg \geq 2W$, where W is width of the differential signal trace.

Figure 8-6. Grounded Shield Guard
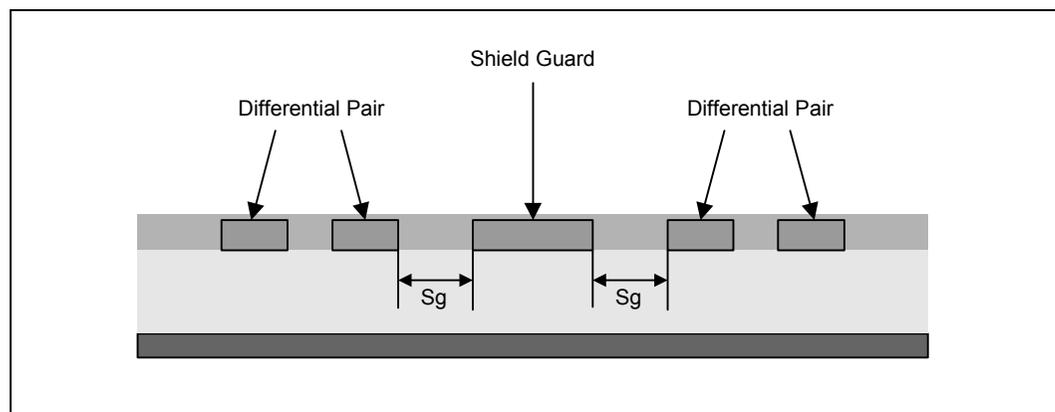
8.2.3   Layout Routing Strategy

8.2.3.1   Routing of Differential Lines

The two routing examples for Sil3112 and the Serial ATA connector are shown in Figure 8-7, Figure 8-8, Figure 8-9 and Figure 8-10. Figure 8-7 and Figure 8-8 are examples of vertical orientation of the Serial ATA connectors, while Figure 8-9 and Figure 8-10 are examples of horizontal orientation of the Serial ATA connectors. In the figures, differential pairs (Tx, Rx) are connected between the Sil3112 chip and the Serial ATA connectors.

Figure 8-7. Serial ATA Connectors (Vertical Orientation Example 1)
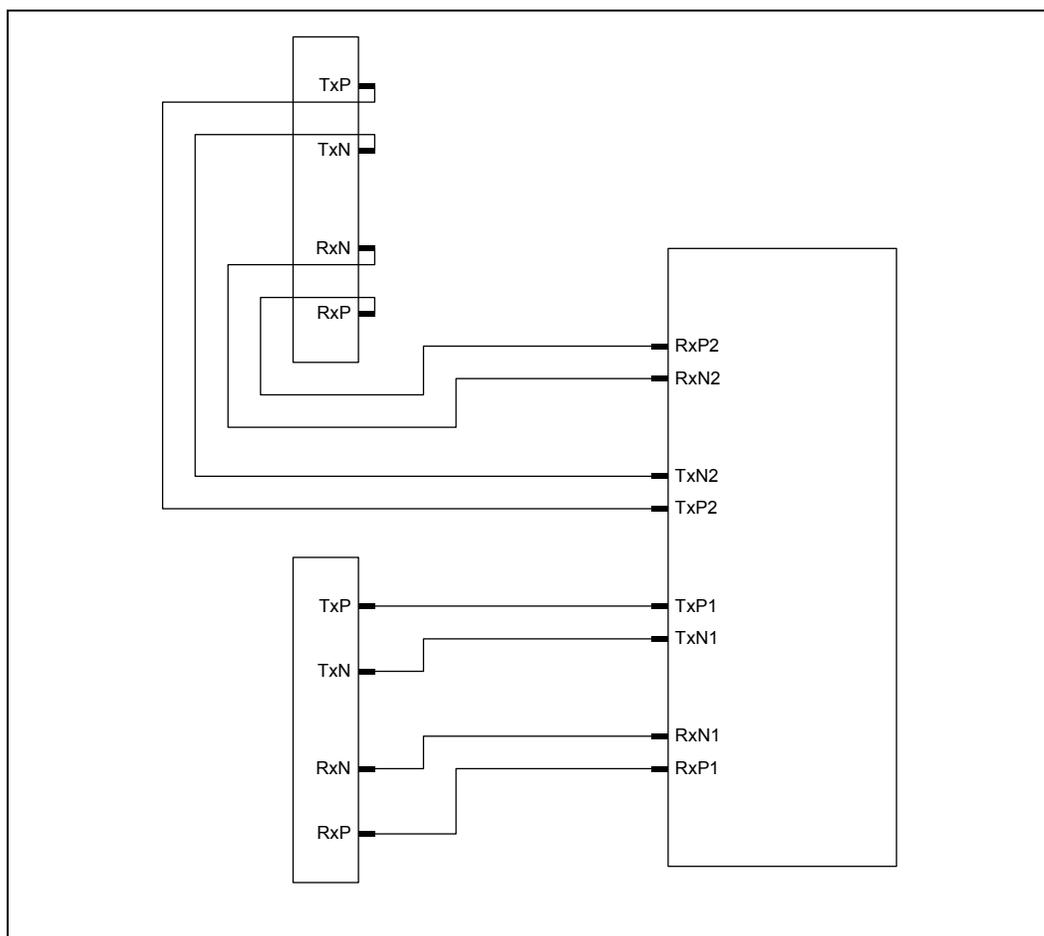
Figure 8-8. Serial ATA Connectors (Vertical Orientation Example 2)
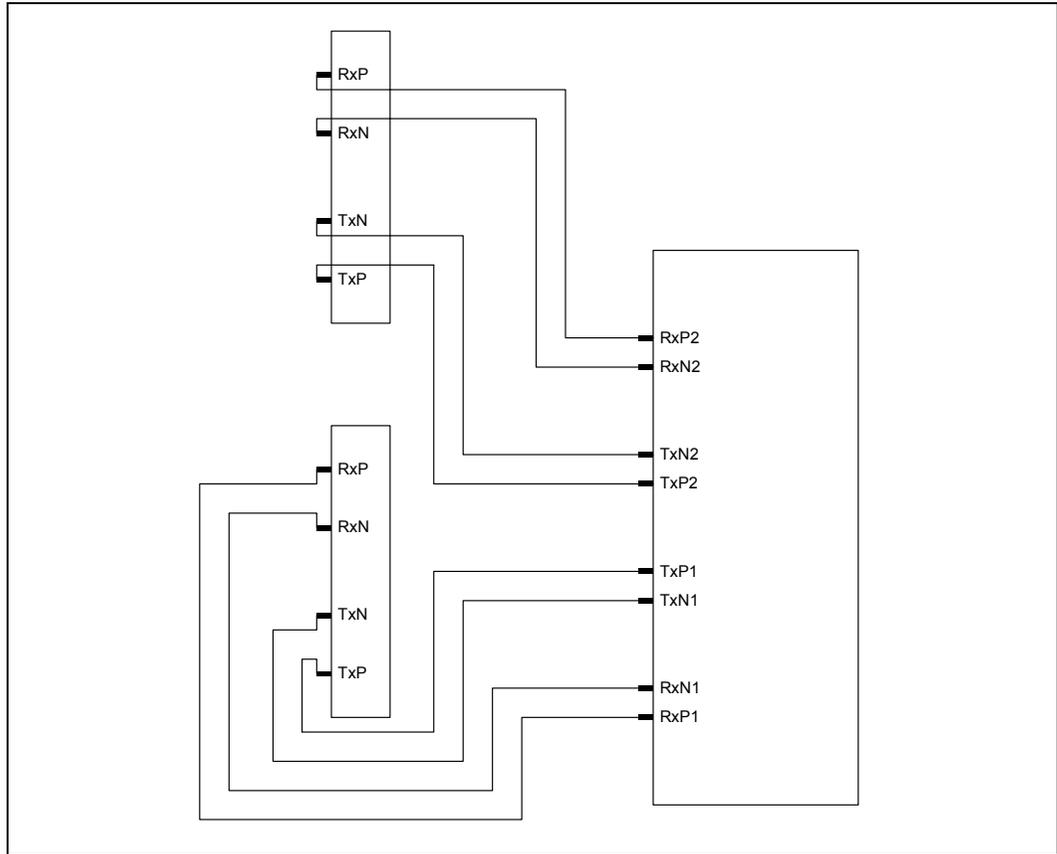
Figure 8-9. Serial ATA Connectors (Horizontal Orientation Example 1)
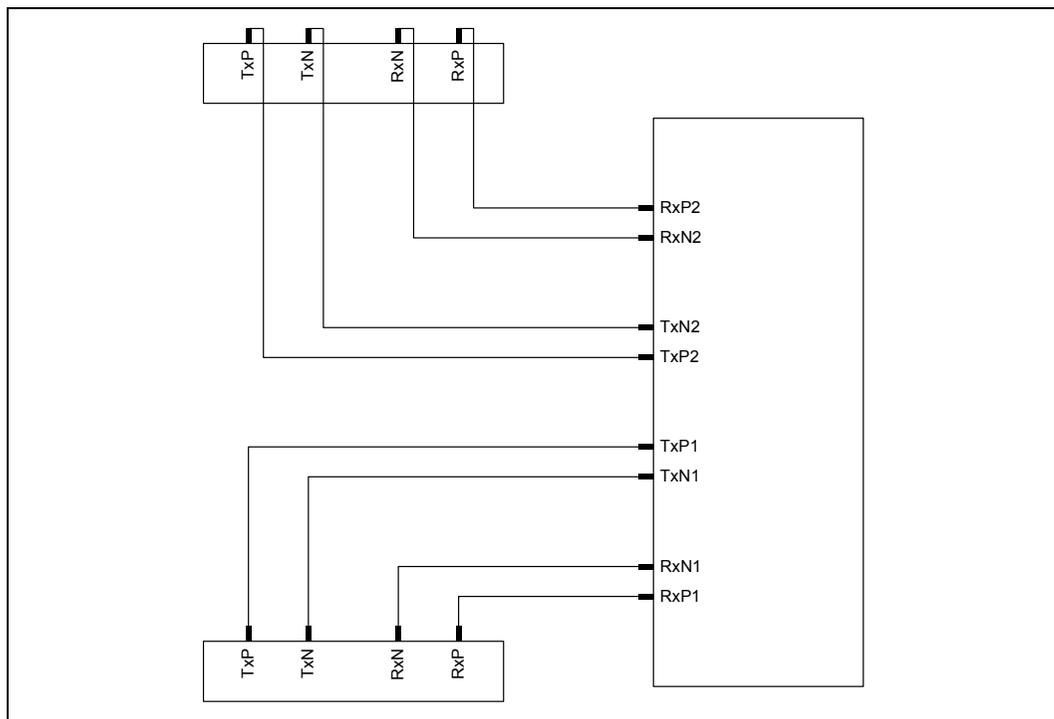
Figure 8-10. Serial ATA Connectors (Horizontal Orientation Example 2)
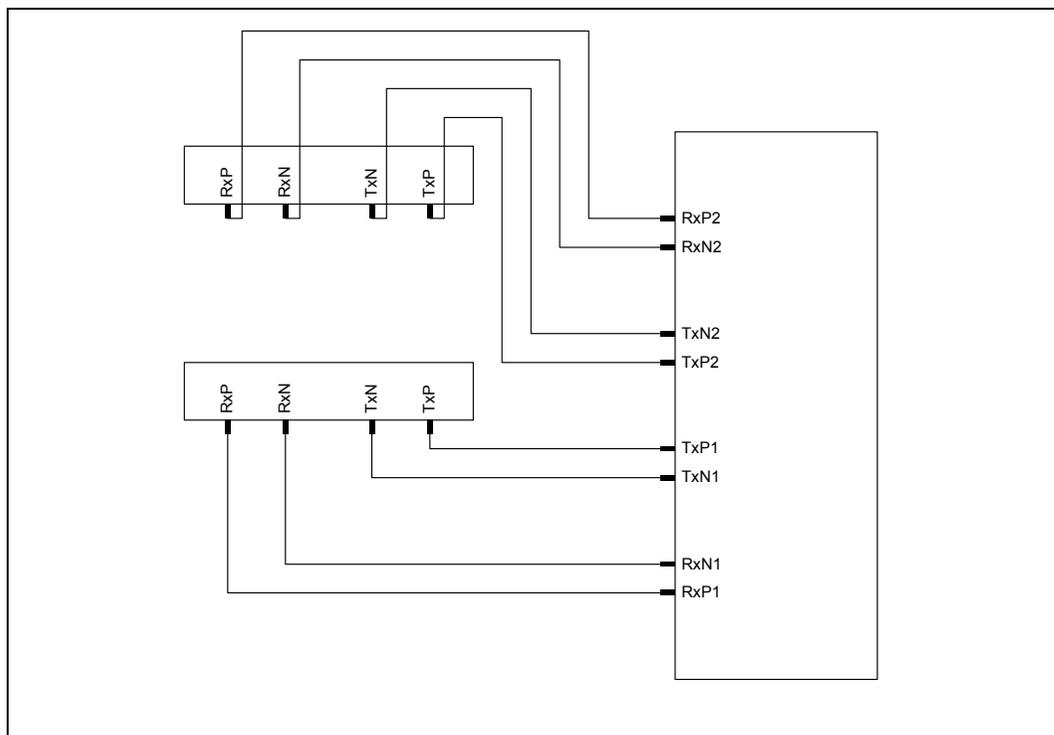
8.3 Platform Integration Considerations

8.3.1 Power Supply Considerations

8.3.1.1 Voltages

The voltages that are supplied to the controller are 1.8 V and 3.3 V. The 3.3 V pins are used to supply power to I/O, which have a tolerance of ± 0.3 V. The 1.8 V pins supply power to the internal core and SerDes power.

8.3.1.2 Power Consumption

The estimated typical power consumption for the Sil3112 is shown in Table 8-3.

Table 8-3. Typical Power Consumption

Voltage	Current
1.8 V Supply current for PHY blocks	190 mA
1.8 V Supply current for core logic	140 mA
3.3 V Supply current (for I/Os)	55 mA

8.3.1.3 Decoupling

The recommended number of decoupling capacitors for the 3.3 V signal rail is eleven. Each of these capacitors should have a value of 0.1 µF. For the 1.8 V signal rail it is recommended to use ten 0.1 µF capacitors and one 10 µF capacitor. In all these cases the capacitor should be placed as close as possible to the package. When choosing these components, the smallest components should be chosen since they have the least parasitic inductance.

Optional solder pads for coupling capacitors are recommended both for Tx and Rx serial lines. For DC coupling case, a 0 Ω resistor can be placed between these pads. For AC coupling, 0.01 µF ceramic capacitors can be used. When placing solder pads for coupling capacitors, minimum solder pad size should be used. No stubs from the Tx/Rx lines are allowed.

To improve the decoupling capability of the small decoupling capacitors (0.1 µF or 0.01 µF), LIC (Low Inductance Capacitor) can be used with BGA type bonding. These decoupling capacitors can be placed between GND and VDD, and the soldering pads should be small.

8.3.1.4   Power Supply Isolation for Analog Blocks

Table 8-4. Differential Pin Description

Pin #	Pin Name	Function
6	VDDD	Rx power
12	VDDD	Tx power
19	VDDD	PLL power
25	VDDD	Tx power
32	VDDD	Rx power
37	VDDD	Xtal power

These power pins supply internal analog and clock generation blocks. They are sensitive to power supply noise. Attention should be paid to proper isolation and bypassing of these pins. Figure 8-11 shows the recommended circuitry.

Figure 8-11. Example Circuitry for Analog Blocks
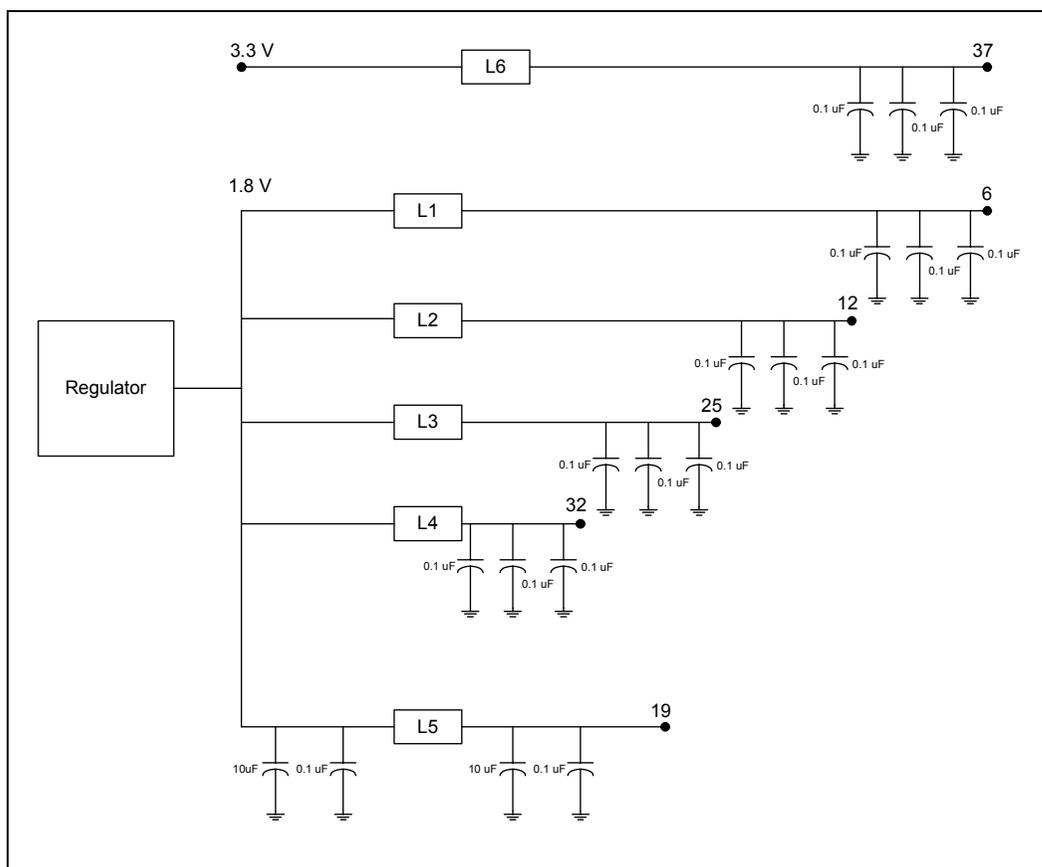
Table 8-5. Ferrite Bead Specifications (L1, L2, L3, L4, L5, L6)

Requirement	Specification
Impedance	>50 Ω at 100 MHz
Series Resistance	< 0.5 Ω
I_{max}	> 100 mA

8.3.1.5   VREG Implementation

To provide 1.8 V signals to the necessary pins, you must have a well-designed voltage regulator circuit. The recommended circuit contains one 10 Ω resistor, one 100 Ω resistor, and one 45.3 Ω resistor. The circuit should contain a 1 µF capacitor, a 0.1 µF capacitor, and one 22 pF capacitor.

Figure 8-12. VREG Implementation
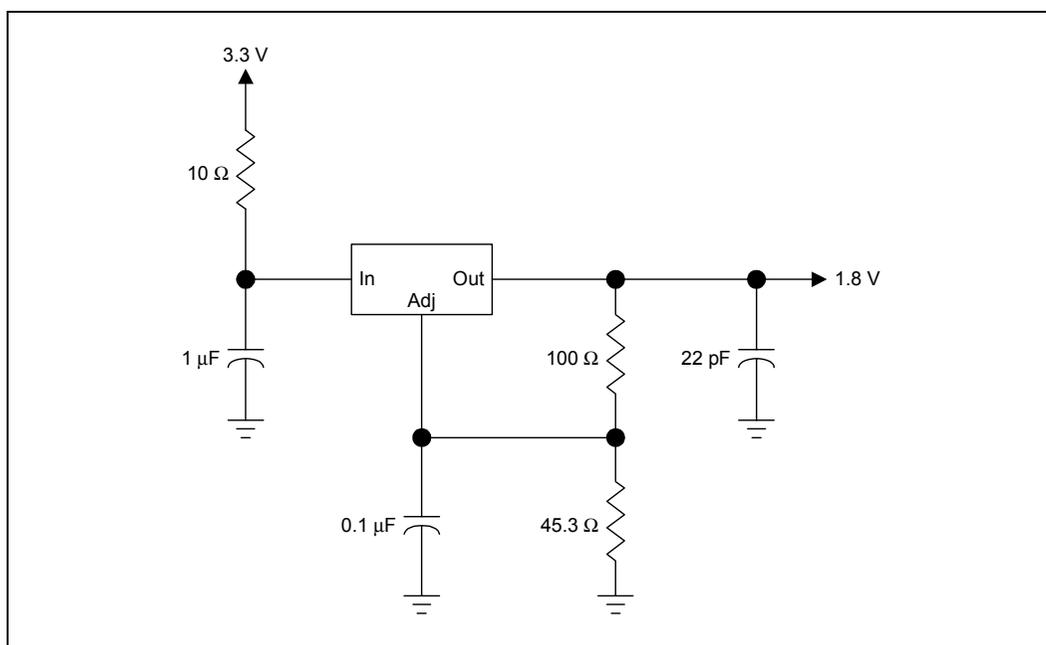
NOTE: The 22 pF capacitor should be placed near the output of the regulator circuit.

8.3.2   SMBus Considerations

The SMBus controller in the Sil3112* part is a master device that will contend with the ICH4. To eliminate the contention, it is recommended to disconnect the SMBus signals to the Serial ATA controller. The SMBus signals on the Serial ATA controller are master device/output signals, and therefore the pins can be left floating.

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AGP 8X 9

This chapter contains information for one possible AGP routing and layout solution that is based on the reference platform. Other implementations of AGP routing may be used with proper simulation based on parameters specified in the design guide available at www.agpforum.org.

Refer to Section 14.6 and Section 15.5 for AGP 8X schematic and layout checklists.

Table 9-1 and Table 9-2 show the AGP signal groups and associated strobes.

Note: The AGP supports both 4X and 8X operation.

Table 9-1. Signal Groups

Group	Signals
1	AD[15:0], C#/BE[1:0], ADSTBF0, ADSTBS0
2	AD[31:16], C#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0), ADSTBF1, ADSTBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0), SBSTBF, SBSTBS
4	IRDY, TRDY, FRAME, SERR# (AGP 2.0), SERR (AGP 3.0), STOP, DEVSEL, PAR
5	RBF# (AGP 2.0), RBF (AGP 3.0), WBF# (AGP 2.0), WBF (AGP 3.0), REQ, GNT

Table 9-2. Associated First and Second Strobes

Group	Signals	First Strobe	Second Strobe
1	AD[15:0], C#/BE[1:0]	ADSTBF0	ADSTBS0
2	AD[31:16], C#/BE[3:2], DBI_HI, DBI_LO (AGP 3.0)	ADSTBF1	ADSTBS1
3	SBA[7:0] (AGP 2.0), SBA[7:0]# (AGP 3.0)	SBSTBF	SBSTBS

9.1 Recommended AGP 8X Routing Parameters

The AGP 8X signals must be routed directly from the MCH to the AGP connector with all signals referenced to VSS. A consistent VSS reference plane must be maintained at all times. In addition, all signals within an address/data group must be routed on the same layer (see Table 9-1 for address/data groups). Table 9-3 summarizes the routing parameters for the AGP interface.

Table 9-3. AGP 8X Routing Parameters

Signal Group	Trace Impedance (Z_0)[1]	Layer	Spacing	Min Length	Max Length
Strobe to Strobe	60 Ω[1]	Stripline	20 mils	2.5"	7.0"
		Microstrip	25 mils	2.5"	6.0"
Strobe to Data		Stripline	20 mils	2.5"	7.0"
		Microstrip	25 mils	2.5"	6.0"
Data to Data		Stripline	20 mils	2.5"	7.0"
		Microstrip	20 mils	2.5"	6.0"
Common Clock		Stripline	15 mils	2.5"	7.5"
		Microstrip	15 mils	2.5"	7.5"

NOTE:
1. To meet the 60 Ω trace impedance requirement, a trace width of 5 mils was used based on the board stack-up described in Section 3.2. The trace width needed to meet the 60 Ω requirement will vary according to platform stack-up.

9.2 Length Matching

The data groups shown in Table 9-2 must match the strobes within 25 mils. First and second strobes must match to within 5 mils. There are no requirements for length matching between groups, and there are no length matching requirements for signals in groups 4 and 5.

Note: MCH package lengths must be considered when tuning the AGP bus.

9.3 Miscellaneous Signal Requirements

9.3.1 SERR/PERR

The PERR signal is not supported by the MCH and must be supplied to the card based on the GC_8XDET signal. SERR# (AGP2.0) or SERR (AGP 3.0) routes between the connector and the MCH with no special termination. See Figure 9-1 for a PERR reference circuit. The circuit supplies pull-down to ground during 8X operation, and a pull-up to 1.5 V during 4X operation.

Figure 9-1. PERR Reference Circuit
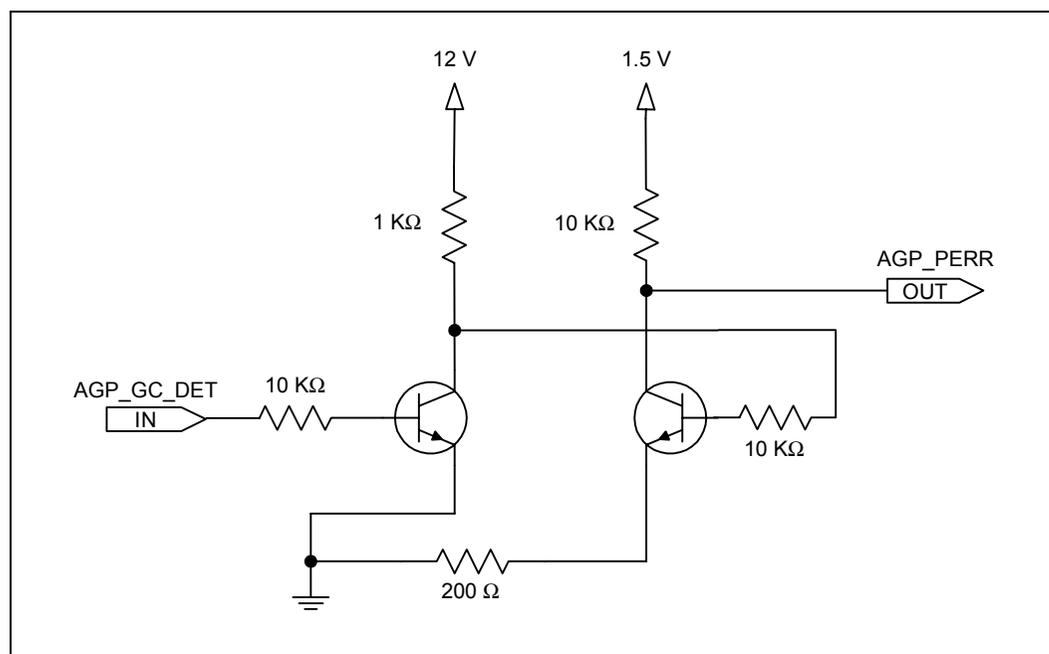
9.3.2 TYPEDET

The TYPEDET signal is not required due to the use of a 1.5 V connector.

9.3.3 PRCOMP_AGP[1:0]

These signals are used to calibrate the AGP buffers. The PRCOMP signals each require a 43 Ω resistor to VCC_AGP.

9.3.4   PREF_AGP[1:0]

A complex VREF circuit is required to meet the reference voltage requirements for AGP 4X and 8X. One possible implementation of this circuit can be found in the AGP Design Guide available at www.agpforum.org.

While the VREF voltage for AGP 8X mode is 0.35 V, the circuit implemented in the CRB schematics seems to show a voltage of only 0.3 V. If the resistance across the transistor is taken into account, it can be shown that the circuit generates the required 0.35 V.

9.3.5   PSWNG_AGP[1:0]

Provide the reference voltages used by the AGP RCOMP circuits. PSWNG_AGP is based on a resistor divider circuit and comes off of 1.5 V. The voltage level is 0.8 V for 8X mode and is the maximum voltage for the AGP signal bus. For AGP 4X mode, the PSWNG_AGP level is a "don't care."

Intel® I/O Controller Hub 4 (ICH4)　　10

10.1　System Overview

The ICH4 is designed for a variety of processors/memory controller hubs and has improved enhancements over the Intel® ICH2 and Intel® ICH3.

The ACPI compliant ICH4 platform can support the Full-on, Stop Grant, Suspend to RAM, Suspend to Disk, and Soft-Off power management states. Through the use of the integrated LAN functions, the ICH4 also supports Wake-on-LAN for remote administration and troubleshooting.

The ICH4 integrates an UltraATA/100 controller, one EHCI host controller, and three UHCI host controllers supporting six external ports, LPC interface controller, FWH interface controller, PCI interface controller, AC '97 digital controller, integrated LAN controller, and a hub interface for communication with the MCH. The ICH4 component will provide the data buffering and interface arbitration required to ensure that system interfaces operate efficiently and provide the bandwidth necessary to enable the system to obtain peak performance.

10.1.1　System Features

The I/O Controller Hub provides the I/O subsystem with access to the rest of the system. Additionally, it integrates the following functions:

- Upstream hub interface for access to the MCH
- 2 channel Ultra ATA/100 Bus Master IDE controller
- 1 EHCI USB 2.0 Host Controller and 3 UHCI USB 1.1 Host Controllers (Expanded capabilities for six ports)
- SMBus 2.0 controller
- FWH interface
- LPC interface
- AC '97 2.3 interface
- PCI 2.2 interface
- Integrated System Management Controller
- Integrated LAN Controller

The ICH4 also contains the arbitration and buffering necessary to ensure efficient utilization of these interfaces.

10.1.2 Bandwidth Summary

Table 10-1 provides a summary of the ICH4 system bandwidth.

Table 10-1. Intel® ICH4 System Bandwidth Summary

Interface	Clock Speed (MHz)	Samples Per Clock	Data Rate (Mega-samples/s)	Data Width (bits)	Bandwidth (MB/s)
Hub Interface	66	4	266	8	266
PCI 2.2	33	1	33	32	133
IDE	Up to 44.444 Write Up to 50 Read	1	44.444 (Write 50 (Read)	16	88.9 (Write) 100 (Read)
LCI	5 – 50	1	5 – 50	3	1.875 – 18.75
AC '97	12.288	1	12.288	1	1.536
LPC	33	1	33	4	16.5
USB 2.0 High Speed	Up to 240 (embedded in data)	Up to 2	480	1	60
SMBus	10	1	10	1	1.25

10.1.3 System Configurations

Table 10-1 shows a typical platform configuration using the ICH4 component.

Figure 10-1. Intel® ICH4 System Block Diagram
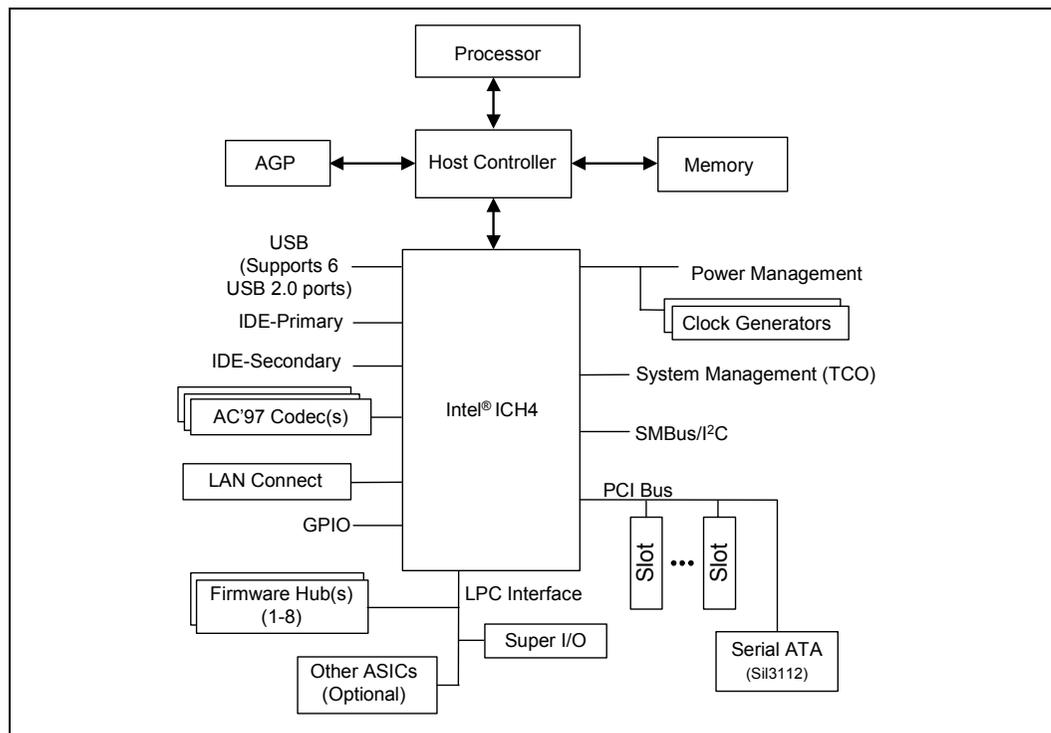
10.1.4 Intel® ICH4 Conventions and Terminology

Table 10-2 defines the conventions and terminology that are used in the following ICH4 descriptions.

Table 10-2. Intel® ICH4 Conventions and Terminology

Term	Definition
AC	Audio Codec
AMC	Audio/Modem Codec
Anti-Etch	Any plane-split, void or cutout in a VCC or GND plane is referred to as an anti-etch
BER	Bit Error Rate.
CMC	Common Mode Choke.
CNR	Communications and Networking Riser.
EMI	Electro Magnetic Interference.
ESD	Electro Static Discharge.
FS	Full Speed; Refers to USB 1.1 Full Speed.
FWH	Firmware Hub. A nonvolatile memory device used to store the system BOIS.
HS	High Speed. Refers to USB 1.1 High Speed.
Intel® ICH4	I/O Controller Hub Fourth Generation.
LOM	LAN on Motherboard.
LPC	Low Pin Count.
LS	Low Speed. Refers to USB 1.1 Low Speed.
MC	Modem Codec.
PCM	Pulse Code Modulation.
PLC	Platform LAN Connect.
RTC	Real Time Clock.
SMBus	System Management Bus. A two-wire interface through which various system components can communicate.
SPD	Serial Presence Detect.
S/PDIF	Sony/Phillips Digital Interface.
STD	Suspend to Disk.
STR	Suspend to RAM.
TCO	Total Cost of Ownership.
TDM	Time Division Multiplexed.
TDR	Time Domain Reflectometry.
µBGA* CSP	Micro Ball Grid Array.
USB	Universal Serial Bus.

10.2 Platform Initiatives

10.2.1 Integrated LAN Controller

The ICH4 incorporates an integrated LAN Controller. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers CPU utilization by off-loading communication tasks from the CPU.

The ICH4 supports several components, depending upon the target market. Available LAN components include the Intel® 82562ET/82562EZ for basic Ethernet 10/100 connection, the Intel® 82562EM/82562EX component which provides an Ethernet 10/100 connection with the added manageability capabilities, the Intel® 82540EM Gigabit Ethernet Controller, and the Intel® 82551QM Fast Ethernet Controller.

Table 10-3. LAN Component Overview

LAN Component	Interface To Intel® ICH4	Connection	Features
Intel® 82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 Pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

10.2.2 Ultra ATA/100 Support

The ICH4 supports the IDE controller with two sets of interface signals (Primary and Secondary) that can be independently enabled, tri-stated or driven low. The component supports Ultra ATA/100, Ultra ATA/66, Ultra ATA/33, and multiword PIO modes for transfers up to 100 MB/sec.

10.2.3 Expanded USB Support

The ICH4 contains three UHCI Host Controllers and one EHCI Host Controller. Each UHCI Host Controller includes a root hub with two separate USB ports each, for a total of six legacy USB ports. The EHCI Host Controller includes a root hub that supports up to six USB 2.0 ports. The ICH4 supports a maximum of six USB ports at any given time. The connection to either a UCHI or the EHCI is dynamic and dependent on the USB device capability, meaning that all ports support HS/FS/LS.

10.2.4 Manageability and Other Enhancements

The ICH4 platform integrates several functions designed to manage the system and lower the total cost of ownership (TCO) of the system. These system management functions are designed to report errors, diagnose the system, and recover from system lockups without the aid of an external microcontroller.

10.2.4.1 SMBus 2.0

The ICH4 integrates an SMBus 2.0 controller. The SMBus provides an interface to manage peripherals such as serial presence detection (SPD) on RAM, thermal sensors, PCI cards, etc. The slave interface allows an external microcontroller to access system resources.

The ICH4 platform integrates several functions designed to expand the capability of interfacing several components to the system.

10.2.4.2 Interrupt Controller

The interrupt capabilities of the ICH4 platform maintain the support for up to eight PCI interrupt pins and PCI 2.2 Message-Based Interrupts. In addition, the ICH4 supports system bus interrupt delivery.

10.2.4.3 Intel® Compatible Firmware Hub (FWH)

The ICH4 platform supports the Intel Compatible Firmware Hub BIOS Memory size up to 8 MB for increased system flexibility.

10.2.5 AC '97 6-Channel Support

The *Audio Codec '97 (AC'97) Specification, Version 2.3* defines a digital interface that can be used to attach an audio codec (AC), a modem codec (MC), and/or an audio/modem codec (AMC) in various configurations. The AC '97 specification defines the interface between the system logic and the audio or modem codec known as the "AC-link."

The ICH4 platform's AC '97 (with the appropriate codecs) improves overall platform integration by incorporating the AC-link. By using an audio codec, the AC-link allows for cost-effective, high-quality, integrated audio on the ICH4 platform. In addition, an AC '97 soft modem can be implemented with the use of a modem codec. Several system options exist when implementing AC '97. The ICH4 integrated digital link allows several external codecs to be connected to the ICH4. The system designer can provide audio with an audio codec, a modem with a modem codec, or an integrated audio/modem codec (Figure 10-2). The digital link is expanded to support three audio codecs or a combination two audio codecs and a modem codec (Figure 10-3 and Figure 10-4).

The digital link in the ICH4 is AC '97 compliant, supporting up to three codecs with independent PCI functions for audio and modem. Microphone input and left and right audio channels are supported for a high quality two-speaker audio solution. Wake on ring from suspend is also supported with an appropriate modem codec.

The ICH4 expands audio capability with support for up to six channels of PCM audio output (full AC3 decode). Six-channel audio consists of Front Left, Front Right, Back Left, Back Right, Center, and SubWoofer for a complete surround sound effect. ICH4 has expanded support for three audio codecs on the AC-link.

Figure 10-2. AC '97 with Audio/Modem Codec
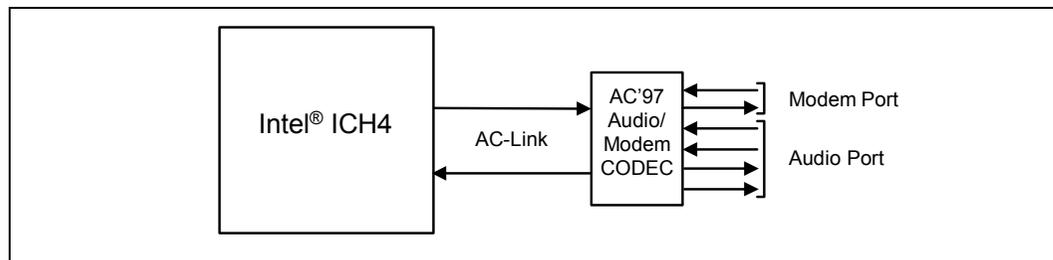
Figure 10-3. AC '97 with Audio Codecs (4 Channel Secondary)
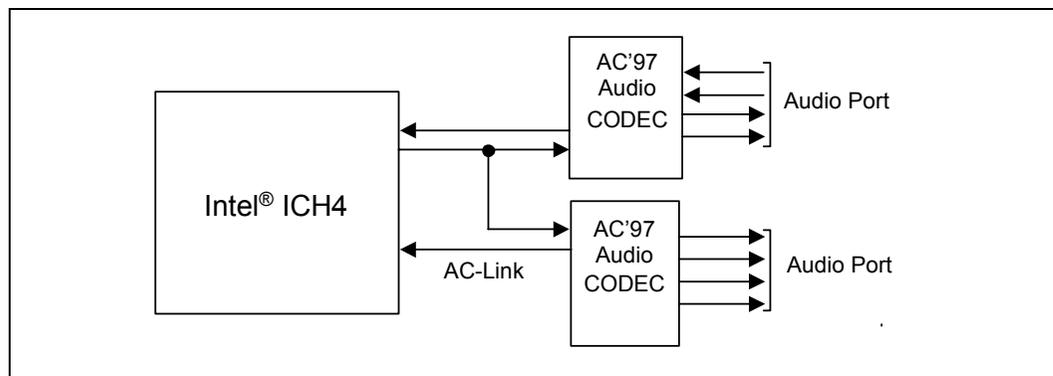
Figure 10-4. AC '97 with Audio and Modem Codec
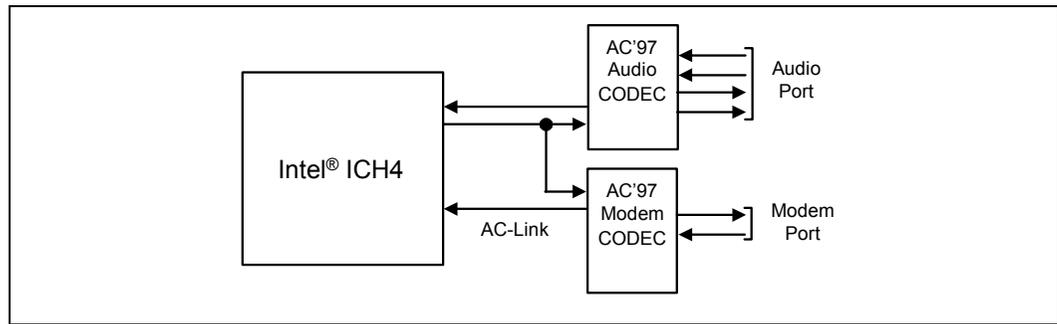
Figure 10-5. AC '97 with 2 Audio and a Modem Codec (4 Channel Secondary)
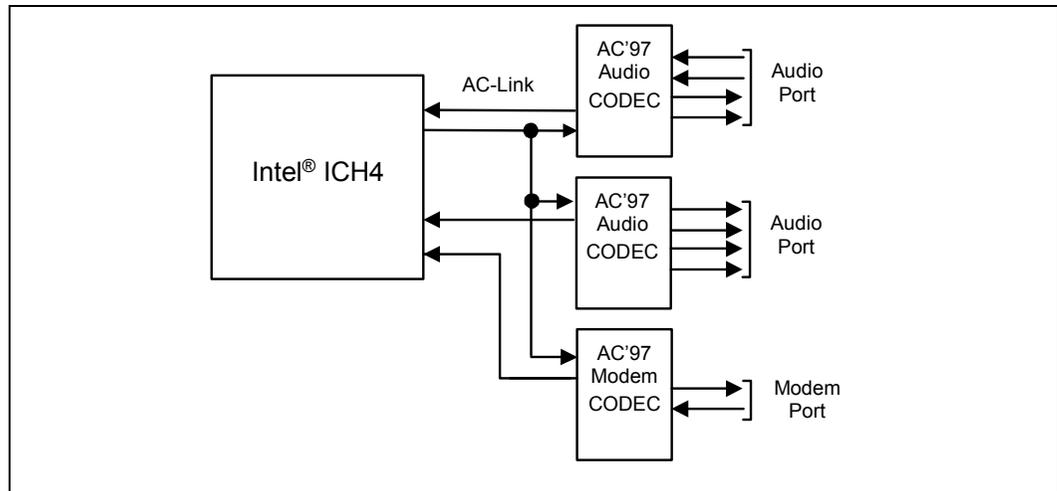
10.3 Layout/Routing Guidelines

This section describes motherboard layout and routing guidelines for ICH4 based systems. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

Warning: If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design.

Even when the guidelines are followed, critical signals should still be simulated to ensure proper signal integrity and flight time. As bus speeds increase, it is imperative that the guidelines documented are followed precisely.

Warning: Any deviation from these guidelines must be simulated!

10.3.1 General Recommendations

The trace impedance typically noted (i.e., 60 Ω ± 15%) is the "nominal" trace impedance. That is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce crosstalk and settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, the routing guidelines documented in this section should be followed.

All recommendations in this section (except where noted) assume 5-mil wide traces. If trace width is greater than 5 mils, the trace spacing requirements must be adjusted accordingly (linearly).

If the six layer stack-up is not used, extremely thorough simulations of all interfaces must be completed. Using a thicker dielectric (prepreg) will make routing very difficult or impossible.

10.3.2   Component Quadrant Layout

The quadrant layouts shown are approximate, and the exact ball assignments should be used to conduct routing analysis. These quadrant layouts are designed for use during component placement.

Figure 10-6. Intel® ICH4 Component Quadrant Layout (Top View)
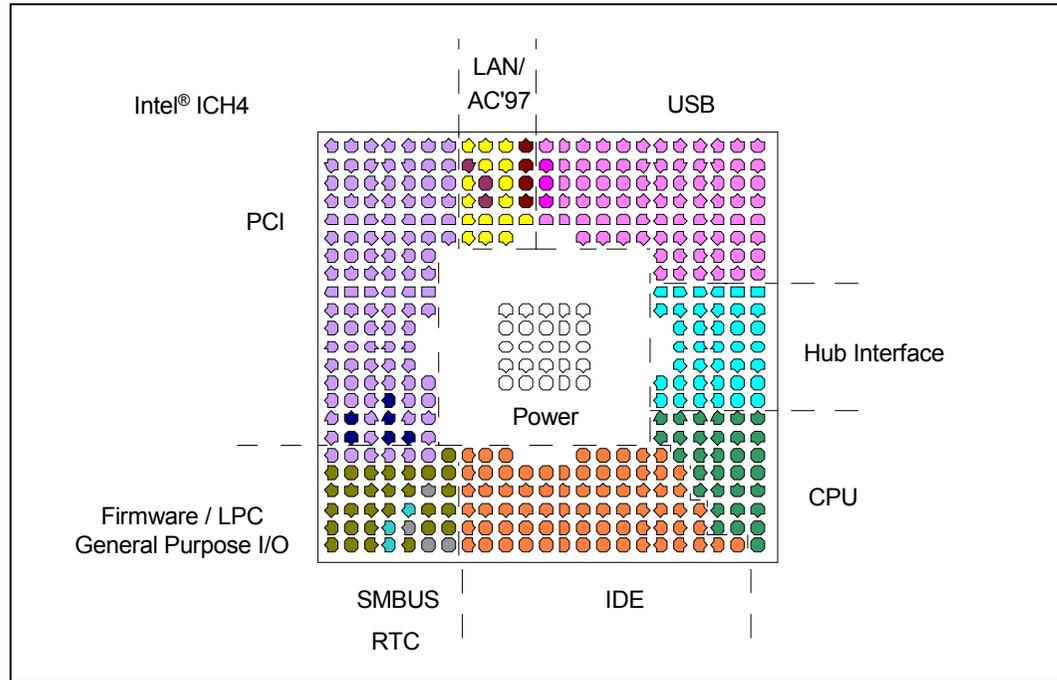
10.3.3   IDE Interface

This section contains guidelines for connecting and routing the ICH4 IDE interface. The ICH4 has two independent IDE channels. This section provides guidelines for IDE connector cabling and motherboard design, including component and resistor placement, and signal termination for both IDE channels. The ICH4 has integrated the series resistors that have been typically required on the IDE data signals (PDD[15:0] and SDD[15:0]) running to the two ATA connectors. While it is not anticipated that additional series termination resistors will be required, OEMs should verify motherboard signal integrity through simulation. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the motherboard. The additional resistor layout increases flexibility by offering stuffing options for later use.

The IDE interface can be routed with 5-mil traces on 7-mil spaces and must be less than 8 inches long (from ICH4 to IDE connector). Additionally, the maximum length difference between the shortest data signal and the longest strobe signal of a channel is 0.5 inches.

Table 10-4. IDE Routing Summary

Trace Impedance	Maximum Trace Lengths	IDE Signal Length Matchin
51 Ω – 69 Ω, 60 Ω target	8 inches	No more than 0.5 inches (500 mils) between the shortest data signal and the longest strobe signal

10.3.3.1   Cabling

Length of cable: Each IDE cable must be equal to or less than 18 inches.

Capacitance: Less than 35 pF.

Placement: A maximum of 6 inches between drive connectors on the cable. If a single drive is placed on the cable, it should be placed at the end of the cable. If a second drive is placed on the same cable, it should be placed on the next closest connector to the end of the cable (6 inches away from the end of the cable).

Grounding: Provide a direct, low impedance chassis path between the motherboard ground and hard disk drives.

10.3.4   Cable Detection for Ultra ATA/66 and Ultra ATA/100

The ICH4 IDE Controller supports PIO, Multi-word (8237 style) DMA, Ultra DMA modes 0 through 5, and Native Mode IDE. Note that there are no motherboard hardware requirements for supporting Native Mode IDE. Native Mode IDE is supported through the operating system and system drivers. The ICH4 must determine the type of cable that is present to configure itself for the fastest possible transfer mode that the hardware can support.

An 80-conductor IDE cable is required for Ultra DMA modes greater than 2 (Ultra ATA/33). This cable uses the same 40-pin connector as the old 40-pin IDE cable. The wires in the cable alternate: ground, signal, ground, signal, ground, signal, ground, etc. All the ground wires are tied together on the cable (and they are tied to the ground on the motherboard through the ground pins in the 40-pin connector). This cable conforms to the *Small Form Factor Specification SFF-8049*. This specification can be obtained from the Small Form Factor Committee.

To determine if Ultra DMA modes greater than 2 (Ultra ATA/33) can be enabled, the ICH4 requires the system software to attempt to determine the cable type used in the system. If the system software detects an 80-conductor cable, it may use any Ultra DMA mode up to the highest transfer mode supported by both the chipset and the IDE device. If a 40-conductor cable is detected, the system software must not enable modes faster than Ultra DMA Mode 2 (Ultra ATA/33).

Intel recommends that cable detection be performed using a combination Host-Side/Device-Side detection mechanism. Note that Host-Side detection cannot be implemented on an NLX form factor system because this configuration does not define interconnect pins for the PDIAG#/CBLID# from the riser (containing the ATA connectors) to the motherboard. These systems must rely on the Device-Side Detection mechanism only.

10.3.4.1 Combination Host-Side/Device-Side Cable Detection

Host side detection (described in the ATA/ATAPI-6 Standard) requires the use of two GPI pins (one for each IDE channel). The proper way to connect the PDIAG#/CBLID# signal of the IDE connector to the host is shown in Figure 10-7. All IDE devices have a 10 kΩ pull-up resistor to 5 V on this signal. A 10 kΩ pull-down resistor on PDIAG#/CBLID# is required to prevent the GPIO from floating if a device is not present, and allows for use of a non-5 V tolerant GPIO.

Figure 10-7. Combination Host-Side/Device-Side IDE Cable Detection
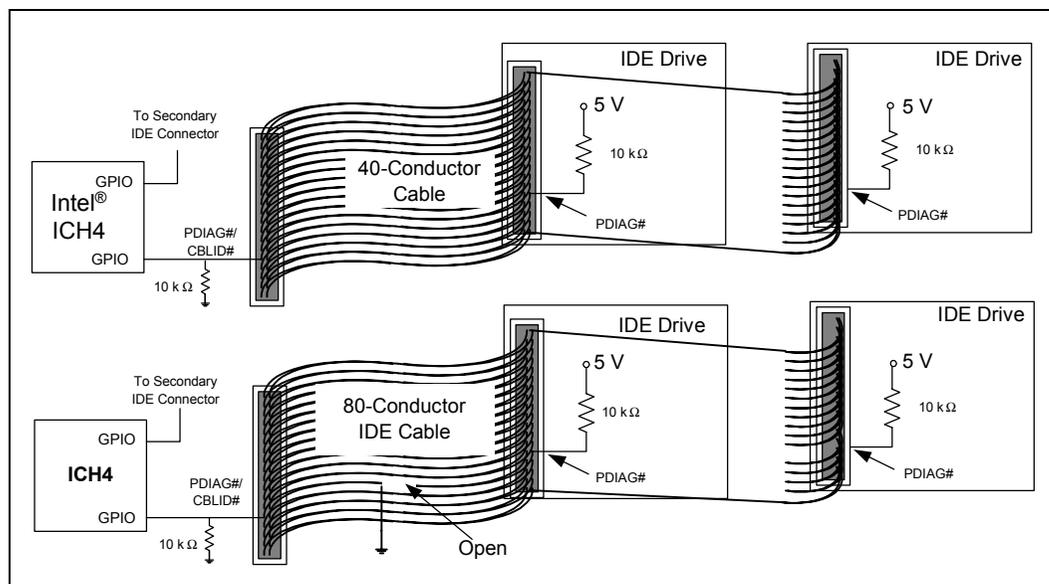
This mechanism allows the BIOS, after diagnostics, to sample PDIAG#/CBLID#. If the signal is high there is 40-conductor cable in the system and Ultra DMA modes greater than 2 (Ultra ATA/33) must not be enabled.

If PDIAG#/CBLID# is detected low, there may be an 80-conductor cable in the system, or there may be a 40-conductor cable and a legacy slave device (Device 1) that does not release the PDIAG#/CBLID# signal as required by the ATA/ATAPI-6 standard. In this case, BIOS should check the IDENTIFY DEVICE information in a connected device that supports Ultra DMA modes higher than 2. If ID Word 93 bit 13 is 1, an 80-conductor cable is present. If this bit is 0, a legacy slave (Device 1) is preventing proper cable detection, and BIOS should configure the system as though a 40-conductor cable is present and should notify the user of the problem.

10.3.4.2   Device-Side Cable Detection

For platforms that must implement Device-Side detection only (e.g., NLX platforms), a 0.047 µF capacitor is required on the motherboard as shown in Figure 10-8. This capacitor should not be populated when implementing the recommended combination Host-Side/Device-Side cable detection mechanism described previously. Note that some drives may not support device-side cable detection.

Figure 10-8. Device Side IDE Cable Detection
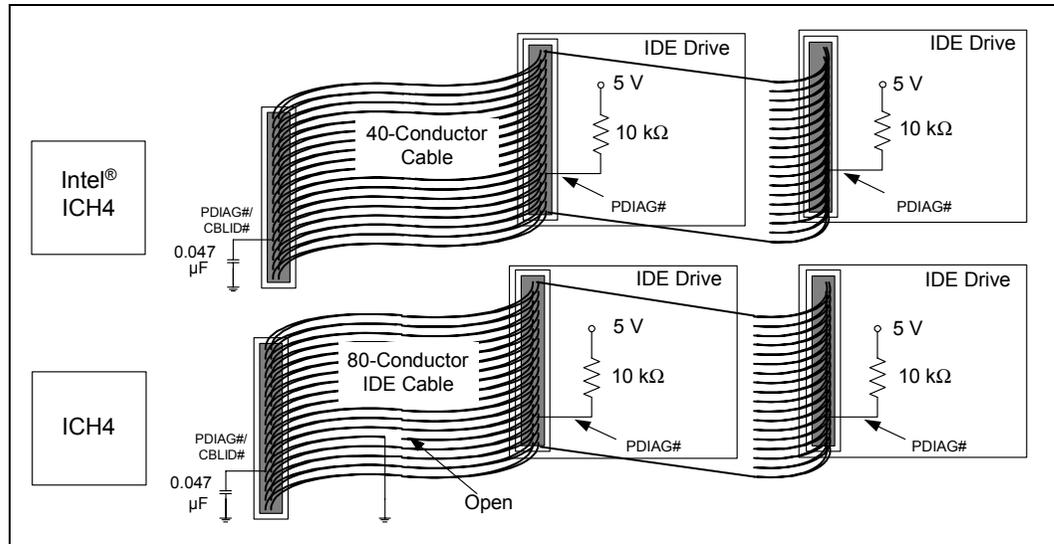
This mechanism creates a resistor-capacitor (RC) time constant. Drives supporting Ultra DMA modes greater than 2 (Ultra DMA/33) will drive PDIAG#/CBLID# low and then release it (pulled up through a 10 kΩ resistor). The drive will sample the signal after releasing it. In an 80-conductor cable, PDIAG#/CBLID# is not connected through to the host; therefore, the capacitor has no effect. In a 40-conductor cable the signal is connected to the host; therefore, the signal rises more slowly as the capacitor charges. The drive can detect the difference in rise times and reports the cable type to the BIOS when it sends the IDENTIFY_DEVICE packet during system boot as described in the ATA/ATAPI-4 Standard.

10.3.4.3   Primary IDE Connector Requirements

The requirements for the primary IDE connector are shown in Figure 10-9.

- A 22 Ω – 47 Ω series resistor is required on RESET#. The correct value should be determined for each unique motherboard design based on signal quality.

- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and to VCC3_3.

- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY.

- Series resistors can be placed on the control and data lines to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the primary connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Figure 10-9. Connection Requirements for Primary IDE Connector
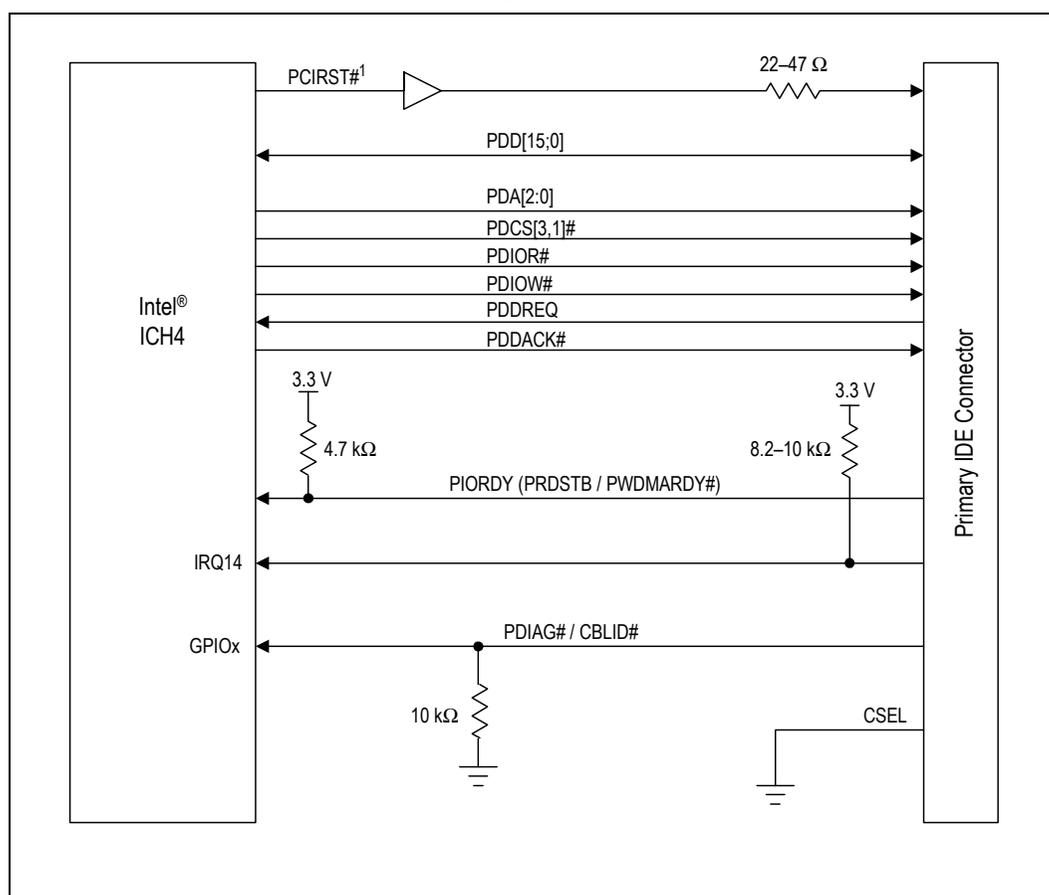
NOTES:
1. Because of ringing, PCIRST# must be buffered.

10.3.4.4 Secondary IDE Connector Requirements

The requirements for the secondary IDE connector are shown in Figure 10-10,

- 22 Ω –47 Ω series resistors are required on RESET#. The correct value should be determined for each unique motherboard design based on signal quality.

- An 8.2 kΩ to 10 kΩ pull-up resistor is required on IRQ14 and to VCC3_3.

- A 4.7 kΩ pull-up resistor to VCC3_3 is required on PIORDY and SIORDY

- Series resistors can be placed on the control and data line to improve signal quality. The resistors are placed as close to the connector as possible. Values are determined for each unique motherboard design.

- The 10 kΩ resistor to ground on the PDIAG#/CBLID# signal is now required on the Secondary Connector. This change is to prevent the GPI pin from floating if a device is not present on the IDE interface.

Figure 10-10. Connection Requirements for Secondary IDE Connector
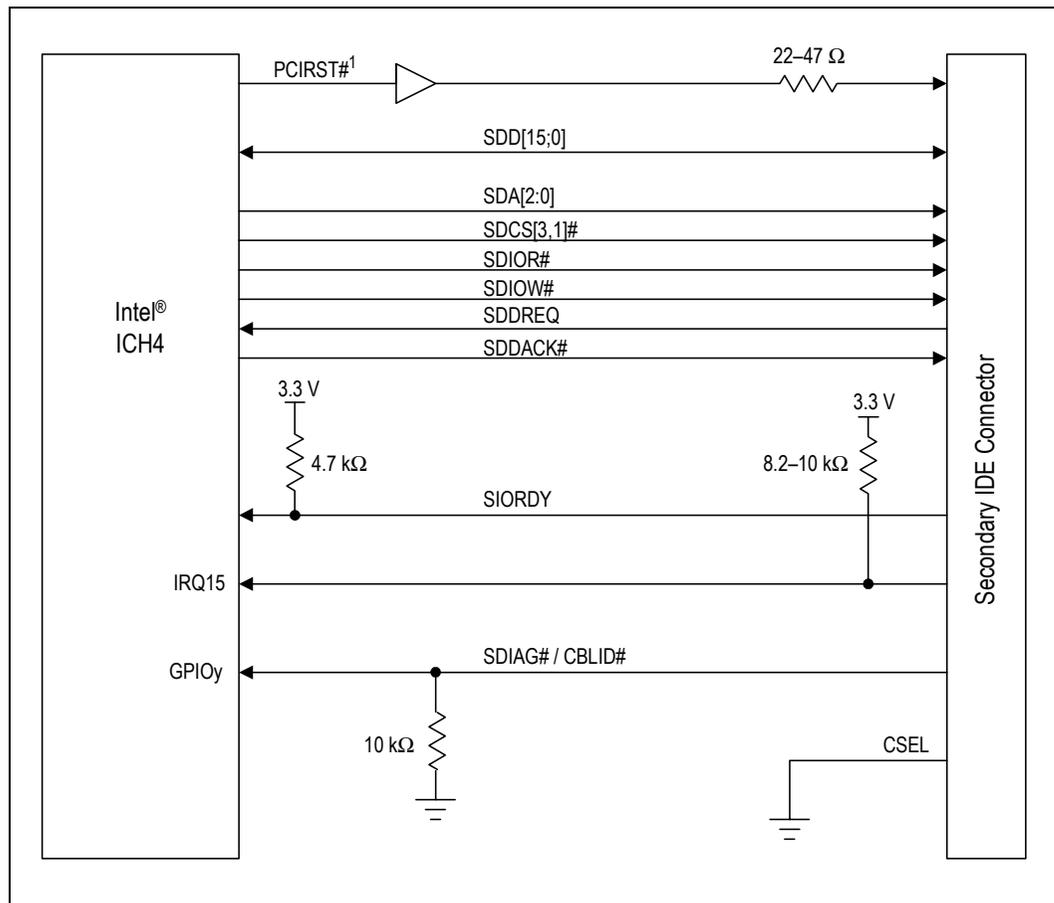
NOTES:
 1. Because of ringing, PCIRST# must be buffered.

10.3.5   AC '97

The ICH4 implements an AC '97 compliant digital controller. Any codec attached to the ICH4 AC-link must be AC '97 compliant as well. Contact your codec IHV for information on AC '97 compliant products. The *Audio Codec '97 (AC'97) Specification, Version 2.3* is on the Intel website:

http://developer.intel.com/ial/scalableplatforms/audio/index.htm#97spec/

The AC-link is a bi-directional, serial PCM digital stream. It handles multiple input and output data streams as well as control register accesses, employing a time division multiplexed (TDM) scheme. The AC-link architecture provides for data transfer through individual frames transmitted in a serial fashion. Each frame is divided into 12 outgoing and 12 incoming data streams, or slots. The architecture of the ICH4 AC-link allows a maximum of three codecs to be connected. Figure 10-11 shows a three codec ICH4 AC-link topology.

Figure 10-11. Intel® ICH4 AC '97 – Codec Connection
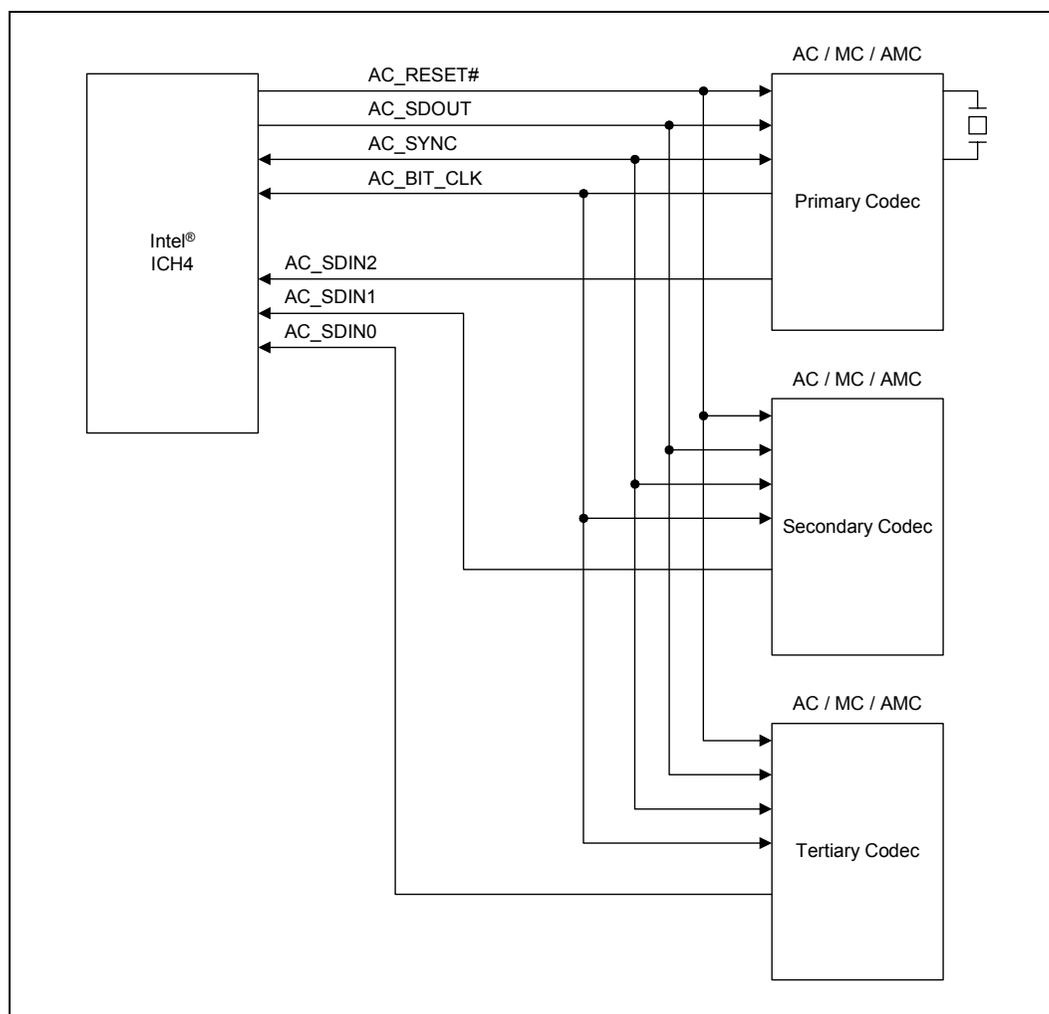
NOTE: If a modem codec is configured as the primary AC-link codec, there should not be any Audio Codecs residing on the AC-link. The primary codec must be connected to AC_SDIN2 if also routing to CNR. If no CNR exists on the platform, the primary codec may be connected to AC_SDIN0 as described in the ICH4 datasheet.

Using the assumed 6-layer stack-up, the AC '97 interface can be routed using 4-mil traces with 6-mil spacing between the traces. Maximum length between ICH4 to CODEC/CNR is 14 inches. This assumes that a CNR riser card implements its audio solution with a maximum trace length of 6 inches for the AC-link. Trace impedance should be $Z_0 = 60 \Omega \pm 15\%$.

Clocking is provided from the primary codec on the link via AC_BIT_CLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirements. AC_BIT_CLK is a 12.288 MHz clock driven by the primary codec to the digital controller (ICH4) and to any other codec that is present. That clock is used as the time base for latching and driving data. **Clocking AC_BIT_CLK off the CK408 14.31818 MHz clock is not supported.**

The ICH4 supports wake on ring from S1-S5 via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec.

The ICH4 has weak pull-downs/pull-ups that are always enabled. This will keep the link from floating when the AC-link is off or there are no codecs present.

The Shut-off bit not set indicates that there is a codec on the link. Therefore, AC_BIT_CLK and AC_SDOUT will be driven by the codec and ICH4 respectively. However, AC_SDIN0, AC_SDIN1, and AC_SDIN2 may not be driven. If the link is enabled, the assumption can be made that there is at least one codec.

Figure 10-12. Intel® ICH4 AC '97 – AC_BIT_CLK Topology
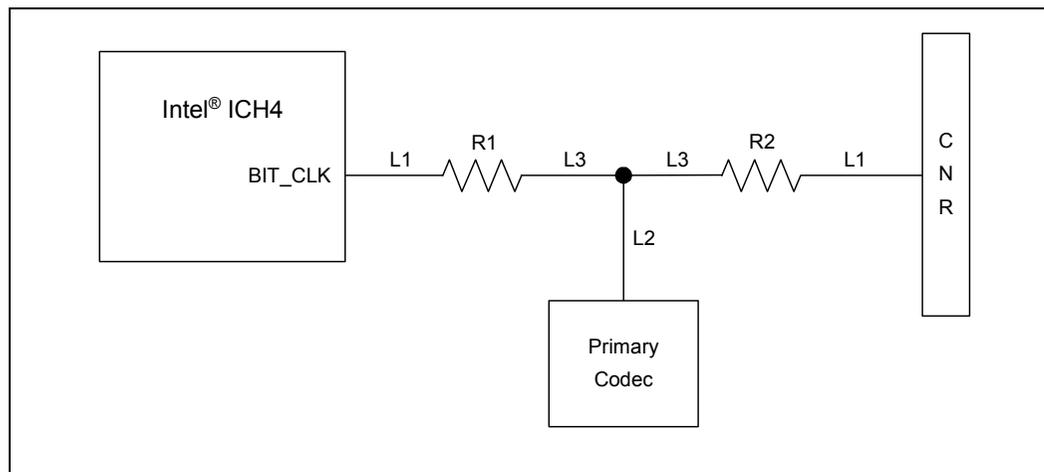
Table 10-5. AC '97 AC_BIT_CLK Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_BIT_CLK Signal Length Matching
51 Ω – 69 Ω, 60 Ω target	L1 = (1 to 8) – L3 inches L2 = (0.1 to 6) inches L3 = (0.1 to 0.4) inches L4 = (1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = Optional 0 Ohm resistor for debug purposes	N/A

NOTE: Simulations were performed using Analog Device's codec (AD1885) and the Cirrus Logic's codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1is best.

Figure 10-13. Intel® ICH4 AC '97 – AC_SDOUT/AC_SYNC Topology
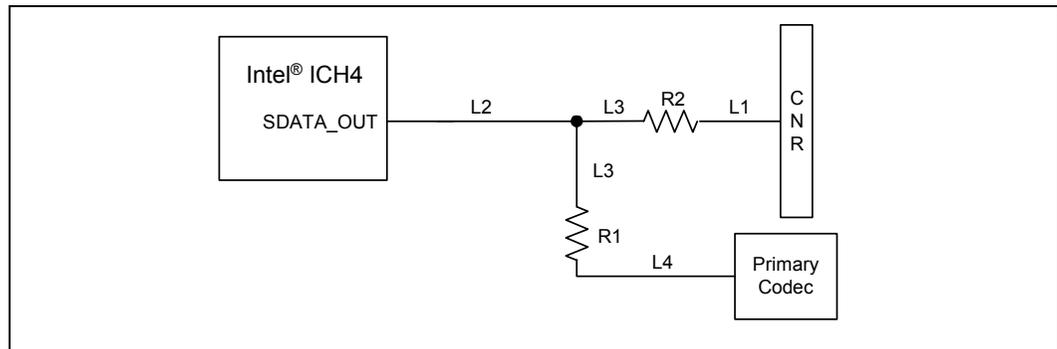
Table 10-6. AC '97 AC_SDOUT/AC_SYNC Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_SDOUT/ AC_SYNC Signal Length Matching
51 Ω – 69 Ω, 60 Ω target	L1 = (1 to 6) – L3 inches L2 = (1 to 8) inches L3 = (0.1 to 0.4) inches L4 = (0.1 to 6) – L3 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise, R2 = 0 Ohm.	N/A

NOTES:
1. Simulations were performed using Analog Device's* codec (AD1885) and the Cirrus Logic's* codec (CS4205b). Results showed that if the AD1885 codec is used, a 33 Ω resistor is best for R1; and if the CS4205b codec is used, a 47 Ω resistor for R1 is best.
2. Bench data shows that a 47 Ω resistor for R1is best for the Sigmatel* 9750 codec.

Figure 10-14. Intel® ICH4 AC '97 – AC_SDIN Topology
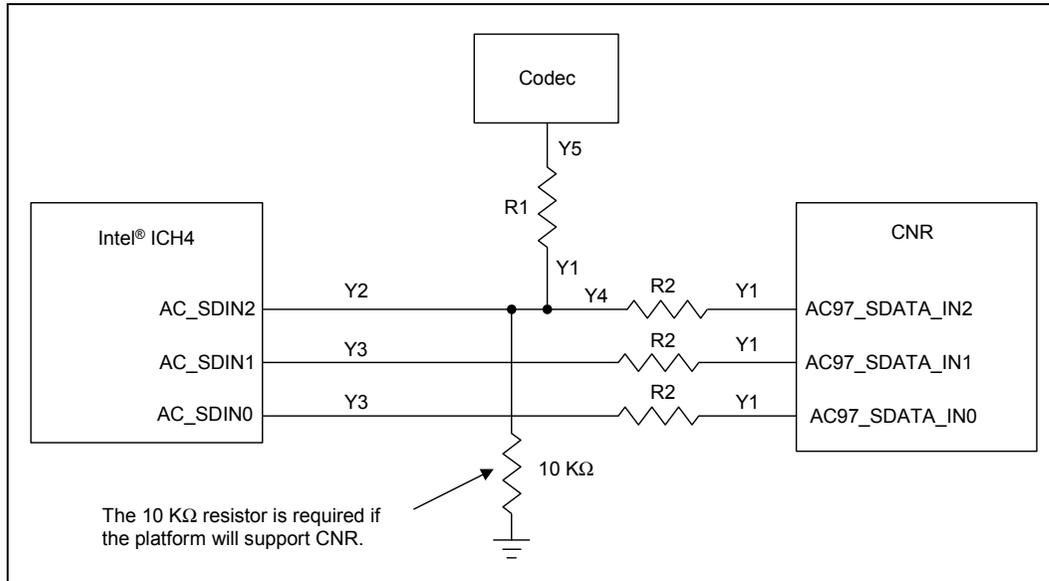
Table 10-7. AC '97 AC_SDIN Routing Summary

Trace Impedance	Maximum Trace Length	Series Termination Resistance	AC_SDIN Signal Length Matching
51 Ω – 69 Ω, 60 Ω target	Y1 = (0.1 to 0.4) inches Y2 = (1 to 8) – Y1 inches Y3 = (1 to 14) – Y1 inches Y4 = (1 to 6) – Y1 inches Y5 = (0.1 to 6) – Y1 inches	R1 = 33 to 47 Ω R2 = R1 if the CNR card that will be used with the platform does not have a series termination on the card. Otherwise, R2 = 0 Ohm.	N/A

NOTES:
1. Simulations were performed using Analog Device's* codec (AD1885) and the Cirrus Logic's* codec (CS4205b). Results showed that if the AD1885 codec was used a 33 Ω resistor was best for R1 and if the CS4205b codec was used a 47 Ω resistor for R1 was best.
2. Bench data shows that a 47 Ω resistor for R1is best for the Sigmatel* 9750 codec.

10.3.5.1 AC '97 Routing

To ensure the maximum performance of the codec, proper component placement and routing techniques are required. These techniques include properly isolating the codec, associated audio circuitry, analog power supplies, and analog ground planes from the rest of the motherboard. This includes plane splits and proper routing of signals not associated with the audio section. Contact your vendor for device-specific recommendations.

The basic recommendations are as follows:

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split lines. Analog and digital signals should be located as far as possible from each other.
- Partition the board with all analog components grouped together in one area, and all digital components in another.
- Separate analog and digital ground planes should be provided with the digital components over the digital ground plane, and the analog components, including the analog power regulators, over the analog ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Keep digital signal traces, especially the clock, as far as possible from the analog input and voltage reference pins.
- Do not completely isolate the analog/audio ground plane from the rest of the board ground plane. There should be a single point (0.25 inches to 0.5 inches wide) where the analog/ isolated ground plane connects to the main ground plane. The split between planes must be a minimum of 0.05 inches wide.
- Any signals entering or leaving the analog area must cross the ground split in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.
- Analog power and signal traces should be routed over the analog ground plane.
- Digital power and signal traces should be routed over the digital ground plane.
- Bypassing and decoupling capacitors should be close to the IC pins or positioned for the shortest connections to pins, with wide traces to reduce impedance.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Regions between analog signal traces should be filled with copper, which should be electrically attached to the analog ground plane. Regions between digital signal traces should be filled with copper, which should be electrically attached to the digital ground plane.
- Locate the crystal or oscillator close to the codec.

10.3.5.2   Motherboard Implementation

The following design considerations are provided for the implementation of an ICH4 platform using AC '97. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board-related issues. These recommendations are not the only implementation or a complete checklist, but they are based on the ICH4 platform.

- Active components such as FET switches, buffers, and logic states should not be implemented on the AC-link signals, except for AC_RST#. Doing so would potentially interfere with timing margins and signal integrity.

- The ICH4 supports wake-on-ring from S1–S5 states via the AC-link. The codec asserts AC_SDIN to wake the system. To provide wake capability and/or caller ID, standby power must be provided to the modem codec. Internal pull-downs will prevent the inputs from floating if no codec is attached to the link, so external resistors are not required.

- PC_BEEP should be routed through the audio codec. Care should be taken to avoid the introduction of a pop when powering the mixer up or down.

10.3.5.2.1   Valid Codec Configurations

Table 10-8. Valid Codec Configurations

Option	Primary Codec	Secondary Codec	Tertiary Codec
1	Audio	Audio	Audio
2	Audio	Audio	Modem
3	Audio	Audio	Audio/Modem
4	Audio	Modem	Audio
5	Audio	Audio/Modem	Audio
6	Audio/Modem	Audio	Audio

NOTES:
1. For power management reasons, codec power management registers are in audio space. Therefore, if there is an audio codec in the system it must be Primary. In addition, there cannot be two modems in a system because there is only one set of modem DMA channels.
2. The ICH4 supports a modem codec on any of the AC_SDIN lines. However, the Modem Codec ID must be either 00 or 01.

10.3.5.3   SPKR Pin Consideration

SPKR is used as both the output signal to the system speaker, and as a functional strap. The strap function enables or disables the "TCO Timer Reboot function" based on the state of the SPKR pin on the rising edge of PWROK. When enabled, the ICH4 sends an SMI# to the processor upon a TCO timer timeout. The status of this strap is readable via the NO_REBOOT bit (bit 1, D31: F0, Offset D4h). The SPKR signal has a weak integrated pull-down resistor (the resistor is only enabled during boot/reset). Therefore, its default state is a logical zero or set to reboot. To disable the feature, a jumper can be populated to pull the signal line high (see Figure 10-15). The value of the pull-up must be such that the voltage divider output caused by the pull-up, the effective pull-down (R_{EFF}), and the ICH4's integrated pull-down resistor will be read as logic high (0.5 VCC3_3 to VCC3_3 + 0.5 V).

Figure 10-15. Example Speaker Circuit
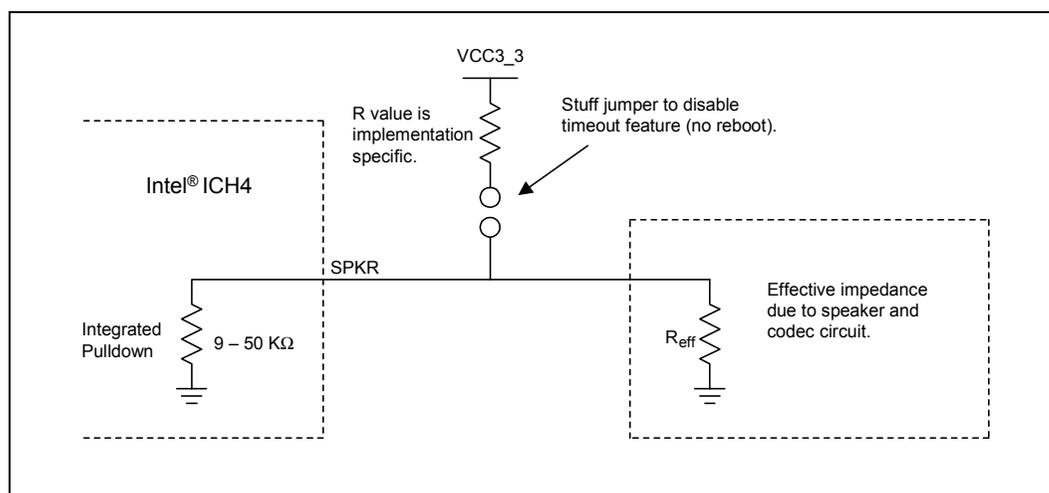
10.3.6   CNR

The Communication and Networking Riser (CNR) Specification defines a hardware scalable Original Equipment Manufacturer (OEM) motherboard riser and interface. This interface supports multi-channel audio, V.90 analog modem, phone-line based networking, 10/100 Ethernet based networking, SMBus Interface Power Management Revision 1.1, and USB 2.0. The CNR specification defines the interface, which should be configured before shipment of the system. Standard I/O expansion slots, such as those supported by the PCI bus architecture, are intended to continue serving as the upgrade medium. The CNR mechanically shares a PCI slot. Therefore, the system designer will not sacrifice a PCI slot if he decides not to include a CNR in a particular build.

Figure 10-16 shows the interface for the CNR connector. Refer to the appropriate section of this document for the corresponding design and layout guidelines. The Platform LAN Connection (PLC) can be either an 82562ET/EZ or an 82562EM/EX component. Refer to the CNR specification for additional information.

For more information, refer to the *Communication Network Riser Specification, Revision 1.2* available at:

http://developer.intel.com/technology/cnr/download.htm

Figure 10-16. CNR Interface
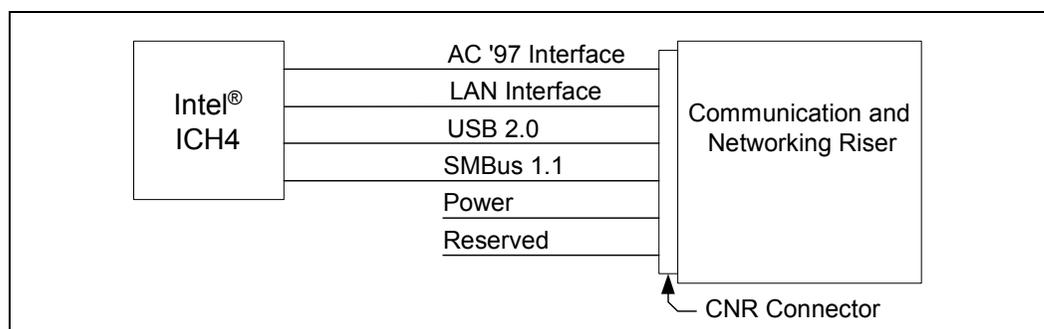
10.3.6.1   AC '97 Audio Codec Detect Circuit and Configuration Options

The following are general circuits and guidelines to implement a number of codec configurations. Refer to the *Communication Network Riser Specification, Revision 1.2* for Intel's recommended codec configurations.

Table 10-9. Signal Descriptions

Signal	Description
CDC_DN_ENAB#	When low, indicates that the codec on the motherboard is enabled and primary on the AC '97 Interface. When high, indicates that the motherboard codec(s) must be removed from the AC '97 Interface (held in reset) because the CNR codec(s) will be the primary device(s) on the AC '97 Interface
AC97_RESET#	Reset signal from the AC '97 Digital Controller (Intel® ICH4)
SDATA_IN*n*	AC '97 serial data from an AC '97-compliant codec to an AC '97-compliant controller (i.e., the ICH4)

10.3.6.1.1 CNR 1.2 AC '97 Disable and Demotion Rules for the Motherboard

The following are the CNR1.2 AC '97 Disable and Demotion Rules for the motherboard:

1. All AC '97 "non-chaining" codecs on the motherboard **must** always disable themselves when the CDC_DN_ENAB# signal is in a high state.

2. A motherboard AC '97 codec **must** never change its address or SDATA_IN line used, regardless of the state of the CDC_DN_ENAB# signal.

3. On a motherboard containing an AC '97 Controller supporting three AC '97 codecs, the AC '97 v2.2 or AC '97 Revision 2.3 codec on the motherboard **must** be connected to the SDATA_IN2 signal of the CNR connector.

4. A motherboard should not contain any more than a single AC '97 codec.

The above rules allow for forward and backward compatibility between CNR Version 1.1/ 1.2 cards. For more information on chaining, consult the *Communication Network Riser Specification, Revision 1.2*.

Figure 10-17. Motherboard AC '97 CNR Implementation with a Single Codec Down on Board
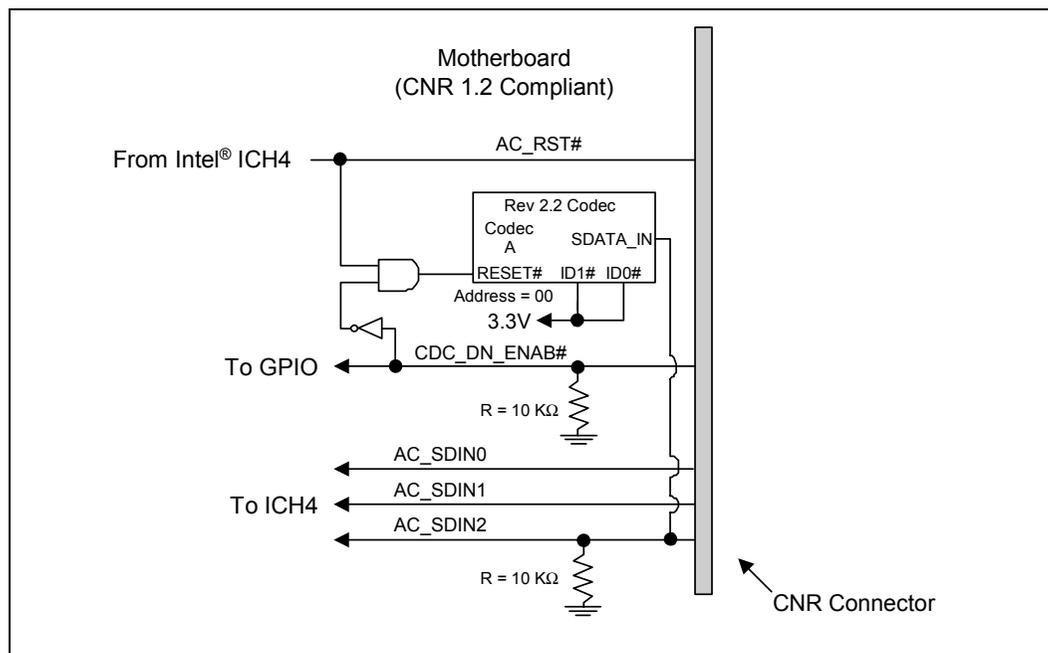
Figure 10-18. Motherboard AC '97 CNR Implementation with no Codec Down on Board
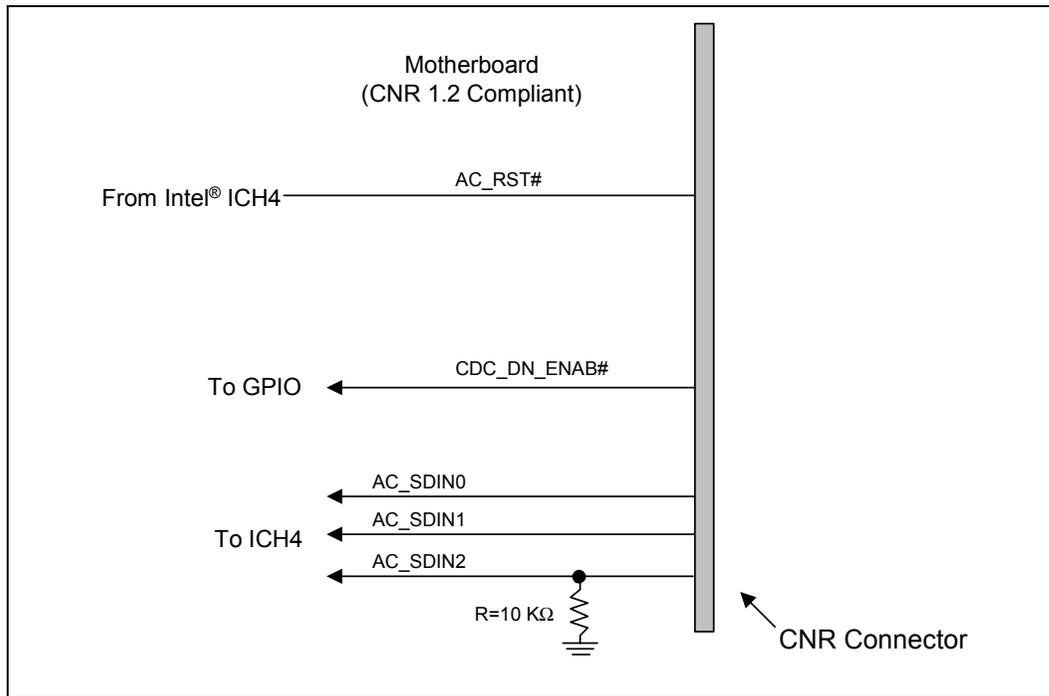
10.3.6.2   CNR Routing Summary

Table 10-10 is a summary of the CNR Riser routing requirements.

Table 10-10. CNR Routing Summary

Trace Impedance	Maximum Trace Length	Signal Length Matching	Signal Referencing
77 Ω – 103 Ω differential, 90 Ω differential target	10"	No more then 150 mils trace mismatch	Ground
51 Ω – 69 Ω, 60 Ω target	AC_BIT_CLK (See Figure 10-12) AC_SDOUT (See Figure 10-13) AC_SDIN (See Figure 10-14)	N/A	Ground
51 Ω – 69 Ω, 60 Ω target	9.5" (See Table 10-21)	Equal to or up to 500 mils shorter than the LAN_CLK trace	Ground

10.3.7 USB 2.0

10.3.7.1 Layout Guidelines

10.3.7.1.1 General Routing and Placement

Use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems

- Place the ICH4 and major components on the un-routed board first. With minimum trace lengths, route high-speed clock, periodic signals, and USB 2.0 differential pairs first. Maintain maximum possible distance between high-speed clocks/periodic signals to USB 2.0 differential pairs and any connector leaving the PCB (i.e., I/O connectors, control and signal headers, and power connectors).

- USB 2.0 signals should be **ground referenced**.

- Route USB 2.0 signals using a minimum of vias and corners. This reduces reflections and impedance changes.

- When it becomes necessary to turn 90 degrees, use two 45 degree turns or an arc instead of making a single 90 degree turn. This reduces reflections on the signal by minimizing impedance discontinuities (see Figure 10-43).

- Do not route USB 2.0 traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.

- Stubs on high-speed USB signals should be avoided because stubs cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the total of all the stubs on a particular line should not be greater than 200 mils.

- Route all traces over continuous planes (VCC or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Similarly, avoid changing layers with USB 2.0 traces as much as practical. It is preferable to change layers to avoid crossing a plane split. Refer to Section 10.3.7.2.

- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).

- Keep USB 2.0 USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.

- Follow the 20*h rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (VCC or GND, depending on the plane the trace is over). For the suggested stack-up the height above the plane is 4.5 mils. This calculates to a 90-mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

10.3.7.1.2 USB 2.0 Trace Separation

Use the following separation guidelines. Figure 10-19 provides an illustration of the recommended trace spacing.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations will normally occur because of package breakout and routing to connector pins. Just ensure the amount and length of the deviations are kept to the minimum possible.

- Use an impedance calculator to determine the trace width and spacing required for the specific board stackup being used.

- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.

- Based on simulation data, use 20-mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

Figure 10-19. Recommended USB Trace Spacing
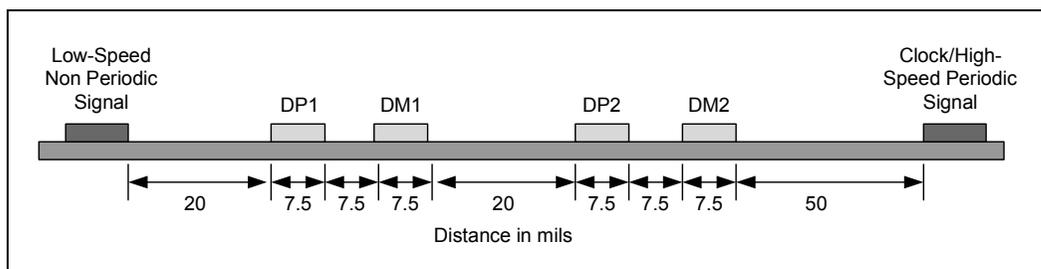
10.3.7.1.3 USBRBIAS/USBRBIAS# Connection

The USBRBIAS pin and the USBRBIAS# pin can be shorted and routed 5 on 5 to one end of a 22.6 Ω ± 1% resistor to ground. Place the resistor within 500 mils of the ICH4 and avoid routing next to clock pins.

Figure 10-20. USBRBIAS/USBRBIAS# Connection
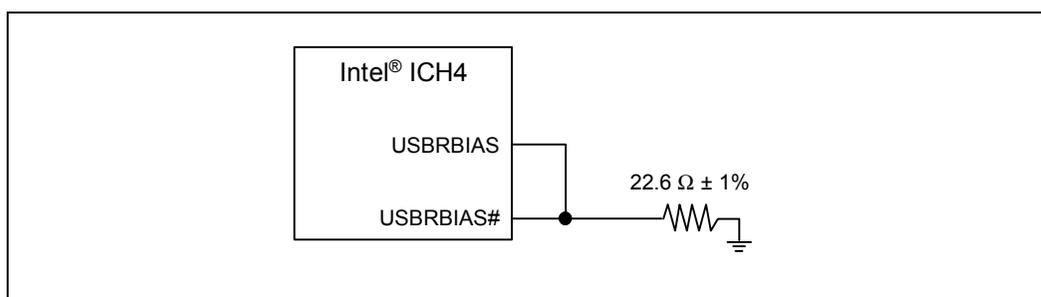
Table 10-11. USBRBIAS/USBRBIAS# Routing Summary

Trace Impedance	Maximum Trace Length	Signal Length Matching	Signal Referencing
51 Ω – 69 Ω, 60 Ω target	500 mils	N/A	N/A

10.3.7.1.4   USB 2.0 Termination

A common-mode choke should be used to terminate the USB 2.0 bus. Place the common-mode choke as close as possible to the connector pins. See Section 10.3.7.5 for details.

10.3.7.1.5   USB 2.0 Trace Length Pair Matching

USB 2.0 signal pair traces should be trace length matched. Max trace length mismatch between USB 2.0 signal pair should be no greater that 150 mils.

10.3.7.1.6   USB 2.0 Trace Length Guidelines

Use the following trace length guidelines.

Table 10-12. USB 2.0 Trace Length Guidelines

USB 2.0 Trace Impedance	Config	Signal Ref	Signal Matching	Motherboard Trace Length	Card Trace Length	Maximum Total Length
77 Ω – 103 Ω differential, 90 Ω differential target	Back Panel	Ground	The max mismatch between data pairs should not be greater than 150 mils	17 inches	N/A	17 inches
77 Ω – 103 Ω differential, 90 Ω differential target	CNR			8 inches	6 inches	14 inches
77 Ω – 103 Ω differential, 90 Ω differential target	Front Panel			**Cable Lengths**	**Motherboard Trace Length**	**Daughter Card Trace Length** / **Maximum Total Length**
				9	6	2 / 17
				10.5	5	2 / 17.5
				12	4	2 / 18
				13.5	3	2 / 18.5
				15	2	2 / 19

NOTES:
1. These lengths are based on simulation results and may be updated in the future.
2. All lengths are based upon using a common-mode choke (see Section 10.3.7.5.1 for details on common-mode choke).
3. The numbers in Table 10-12 are based on the following simulation assumptions:
   a. CNR configuration: max 6 inches trace on add-on card.
   b. An approximate 1:1 trade-off can be assumed for Motherboard Trace Length vs. Daughter card Trace Length (e.g., trade 1 inch of Daughter card for 1 inch of Motherboard Trace Lengths).
4. Routing guidelines are based on the stack-up assumptions in Chapter 3.
5. Numbers in Table 10-12 are based on the following simulation assumptions:
   a. Trace length on front panel connector card assumed a max of 2 inches.
   b. USB twisted-pair shielded cable as specified in USB 2.0 specification was used.
6. For front panel solutions, signal matching is considered from the ICH4 to the front panel header.

10.3.7.2   Plane Splits, Voids and Cut-Outs (Anti-Etch)

The following guidelines apply to the use of plane splits voids and cut-outs.

10.3.7.2.1   VCC Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Use the following guidelines for the VCC plane.

1. Traces should not cross anti-etch because it greatly increases the return path for those signal traces. This applies to USB 2.0 signals, high-speed clocks, and signal traces as well as slower signal traces that might be coupling to them. USB signaling is not purely differential in all speeds (i.e., the Full-speed Single Ended Zero is common mode).

2. Avoid routing of USB 2.0 signals within 25-mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.

When breaking signals out from packages it is sometimes very difficult to avoid crossing plane splits or changing signal layers, particularly in today's motherboard environment that uses several different voltage planes. Changing signal layers is preferable to crossing plane splits if a choice has to be made between one or the other.

If crossing a plane split is completely unavoidable, proper placement of stitching capacitors can minimize the adverse effects on EMI and signal quality performance caused by crossing the split. Stitching capacitors are small-valued capacitors (1 μF or lower in value) that bridge voltage plane splits close to where high speed signals or clocks cross the plane split. The capacitor ends should tie to each plane separated by the split. They are also used to bridge, or bypass, power and ground planes close to where a high-speed signal changes layers. As an example of bridging plane splits, a plane split that separates VCC5 and VCC3_3 planes should have a stitching capacitor placed near any high-speed signal crossing. One side of the capacitor should tie to VCC5, and the other side should tie to VCC3_3. Stitching caps provide a high-frequency current return path across plane splits. They minimize the impedance discontinuity and current loop area that crossing a plane split creates.

10.3.7.3   GND Plane Splits, Voids, and Cut-Outs (Anti-Etch)

Avoid anti-etch on the GND plane.

10.3.7.4 USB Power Line Layout Topology

The following is a suggested topology for power distribution of Vbus to USB ports. Circuits of this type provide two types of protection during dynamic attach and detach situations on the bus: inrush current limiting (droop), and dynamic detach flyback protection. These two situations require both bulk capacitance (droop), and filtering capacitance (for dynamic detach flyback voltage filtering). It is important to minimize the inductance and resistance between the coupling capacitors and the USB ports. That is, capacitors should be placed as close as possible to the port, and the power-carrying traces should be as wide as possible, preferably a plane.

Figure 10-21. Good Downstream Power Connection
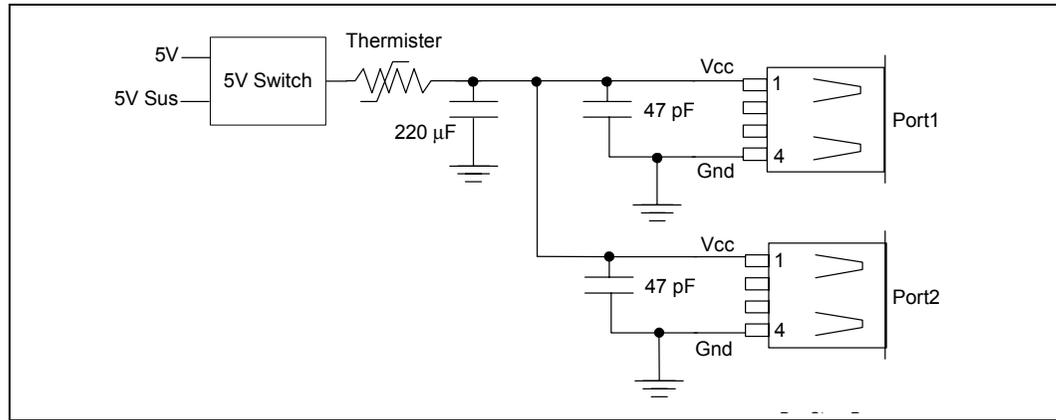
10.3.7.5   EMI Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

10.3.7.5.1   Common Mode Chokes

Testing has shown that common-mode chokes can provide required noise attenuation. A design should include a common-mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. The choke should be placed as close as possible to the USB connector signal pins. In systems that route USB to a front panel header, the choke should be placed on the front panel card. See

Figure 10-22. A Common-Mode Choke
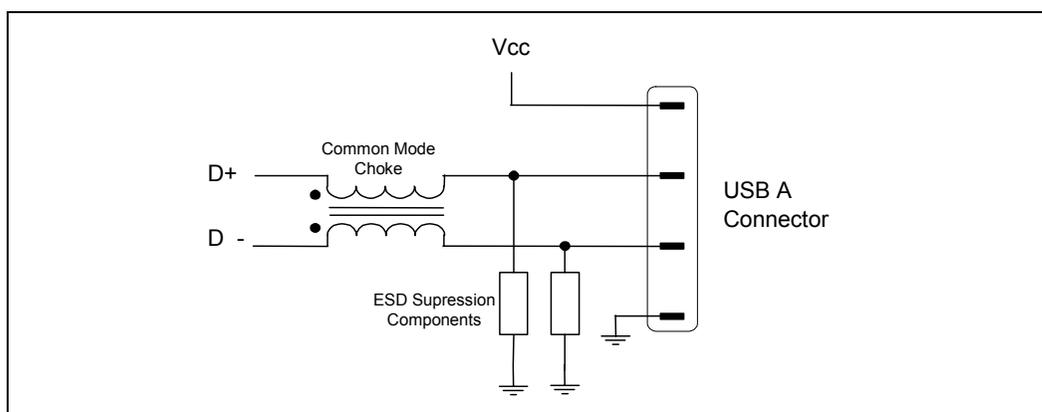
Common mode chokes distort full-speed and high-speed signal quality. As the common mode impedance increases the distortion increases, so you should test the effects of the common mode choke on full speed and high-speed signal quality. Common Mode Chokes with a target impedance of 80 Ω to 90 Ω at 100 MHz generally provide adequate noise attenuation.

Finding a common mode choke that meets the designer's needs is a two-step process.

1. A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that you are trying to suppress.

2. Once you have a part that gives passing EMI results, test the effect this part has on signal quality. Higher impedance common-mode chokes generally have a greater damaging effect on signal quality, so care must be used when increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for low-speed, full-speed, and high-speed USB operation.

10.3.7.6   ESD

Classic USB (1.0/1.1) provided ESD suppression using in line ferrites and capacitors that formed a low pass filter. This technique doesn't work for USB 2.0 because of the much higher signal rate of high-speed data. A device that has been tested successfully is based on spark gap technology. Proper placement of any ESD protection device is on the data lines between the common mode choke and the USB connector data pins as shown in Figure 10-22. Other types of low-capacitance ESD protection devices may work as well but were not investigated. As with the common mode choke solution, it is recommended to include footprints for some type of ESD protection device as a stuffing option in case it is needed to pass ESD testing.

10.3.7.7   Front Panel Solutions

10.3.7.7.1   Cables

The front panel internal cable solution must meet all the requirements of Chapter 6 of the *USB 2.0 Specification* for High/Full-speed cabling for each port with the exceptions described in Cable Option 2. For more information refer to the FPIO design guideline available at:

> http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Internal Cable Option 1

Use standard High-speed/Full-speed compatible USB cables. These must meet all cabling requirements called out in Chapter 6 of the *USB 2.0 Specification*. Recommended motherboard mating connector pin-out is covered in detail later in this document.

Internal Cable Option 2

Use custom cables that meet all of the requirements of Chapter 6 of the *USB 2.0 Specification* with the following additions/exceptions.

- They can share a common jacket, shield, and drain wire.
- Two ports with signal pairs that share a common jacket may combine Vbus and ground wires into a single wire provided the following conditions are met:
  — The bypass capacitance required by Section 7.2.4.1 of the *USB 2.0 Specification* is physically located near the power and ground pins of the USB connectors. This is easiest to achieve by mounting the front panel USB connectors and the bypass capacitance on a small PCB (daughter card). Refer to the front panel daughter card referenced later for details.
  — Selecting proper wire size: A general rule for replacing two power or ground wires with a single wire is to choose a wire size from Table 6-6 in Section 6.6.3 of the *USB 2.0 Specification* that has less than or equal to ½ the resistance of either of the two wires being combined. The data is provided for reference in the following table.

Table 10-13. Conductor Resistance (Table 6-6 from USB 2.0 Specification)

American Wire Gauge (AWG)	Ohm / 100 Meters Maximum
28	23.20
26	14.60
24	9.09
22	5.74
20	3.58

Example: 2–24 gauge (AWG) power or ground wires can be replaced with one 20-gauge wire.

Proper wire gauge selection is important to meet the voltage drop and droop requirements called out in the *USB 2.0 Specification* at the USB connectors as well as at the stake pins on the PCB.

Placing the capacitance near the USB connectors for cables that share power and ground conductors is required to ensure the system passes droop requirements. Cables that provide individual power and ground conductors for each port can usually meet droop requirements by providing adequate capacitance near the motherboard mating connector because droop is actually an effect felt by adjacent ports due to switching transients on the aggressor port. In the separate conductor case, all transients will be seen/dampened by the capacitance at the motherboard mating connector before they can cause problems with the adjacent port sharing the same cable. See section 7.2.2 and 7.2.4.1 of the *USB 2.0 Specification* for more details.

Cables that contain more than two signal pairs are not recommended because of unpredictable impedance characteristics.

10.3.7.7.2 Motherboard/PCB Mating Connector

Proper selection of a motherboard mating connector for front panel USB support is important to ensure that signal quality is not adversely affected because of a poor connector interface. The cable and PCB mating connector must also pass the TDR requirements listed in the USB 2.0 Specification.

Pinout

A ten pin, 0.1-inch pitch stake pin assembly is recommended with the pinout listed in Table 10-14 and the schematic shown in Figure 10-23.

Table 10-14. Front Panel Header Pinout

Pin	Description
1	VCC
2	VCC
3	dm1
4	dm2
5	dp1
6	dp2
7	Gnd
8	Gnd
9	key
10	No connect or over-current sense

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Figure 10-23. Front Panel Header Schematic
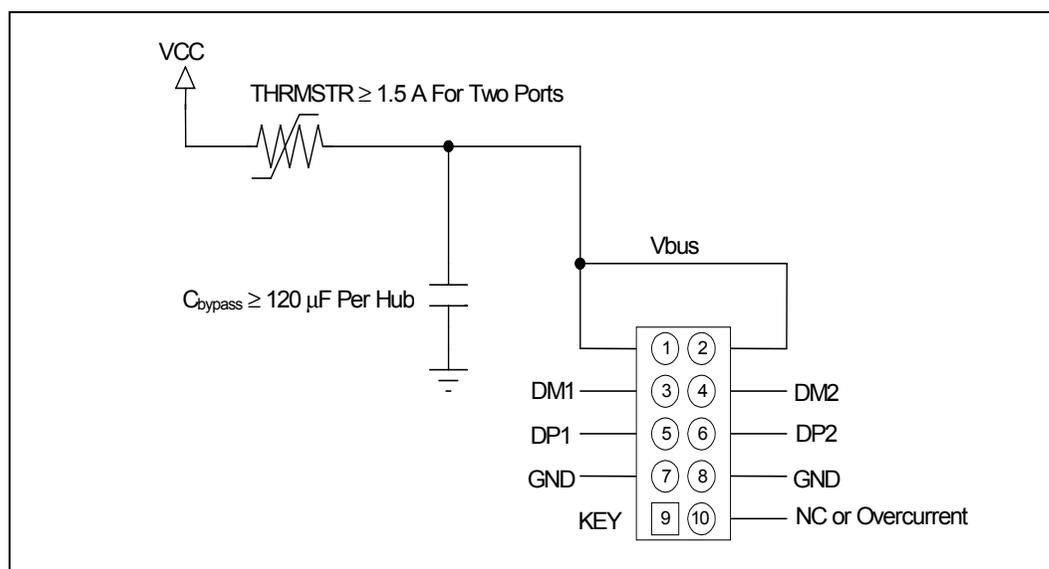
It is **highly** recommended that the fuse element (thermistor) for the front panel header be included on the motherboard to protect the motherboard from damage.

- This protects the motherboard from damage in the case where an un-fused front panel cable solution is used.

- It also provides protection from damage if an un-keyed cable is inadvertently plugged onto the front panel USB connector.

- It provides protection to the motherboard in the case where the front panel cable is cut or damaged during assembly or manufacturing resulting in a short between Vbus and ground.

Routing Considerations

- Traces or surface shapes from VCC to the thermistor, to Cbypass and to the connector power and ground pins should be at least 50 mils wide to ensure adequate current carrying capability.

- There should be double vias on power and ground nets, and the trace lengths should be kept as short as possible.

10.3.7.7.3   Front Panel Connector Card

The best way to provide front or side panel support for USB is to use a daughter card and cable assembly. This allows the placement of the EMI/ESD suppression components right at the USB connector where they will be the most effective. Figure 10-24 shows the major components associated with a typical front/side panel USB solution that uses a front panel connector card. For more information, refer to the FPIO design guideline available at:

> http://www.formfactors.org/developer/fpio_design_guideline.pdf.

Figure 10-24. Motherboard Front Panel USB Support
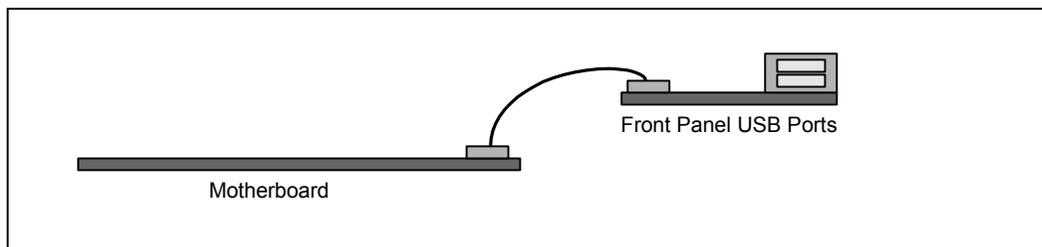
When designing the motherboard with front/side panel support, the system integrator should know which type of cable assembly will be used. If the system integrator plans to use a connector card, ensure that there aren't duplicate EMI/ESD/thermistor components placed on the motherboard because this will usually cause drop/droop and signal quality degradation or failure.

Front Panel Daughter Card Design Guidelines

- Place the Vbus bypass capacitance, Common Mode Choke, and ESD suppression components on the daughter card as close as possible to the connector pins.
- Follow the same layout, routing and impedance control guidelines as specified for motherboards.
- Minimize the trace length on the front panel connector card. Less than 2-inch trace length is recommended.
- Use the same mating connector pin-out as previously outlined for the motherboard.
- Trace length guidelines are given in Table 10-12.

10.3.8   I/O APIC Design Recommendation

The processor does not support I/O APIC. Follow these recommendations.

- **On the ICH4**
  - Tie APICCLK directly to ground
  - Tie APICD0, APICD1 to ground through a 10 kΩ resistor (Separate pull-downs are required if using XOR chain testing.)
- **On the Processor**
  - Consult processor documentation

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10.3.9   SMBus 2.0/SMLink Interface

The SMBus interface on the ICH4 uses two signals, SMBCLK and SMBDATA, to send and receive data from components residing on the bus. These signals are used exclusively by the SMBus Host Controller. The SMBus Host Controller resides inside the ICH4.

The ICH4 incorporates a SMLink interface supporting Alert on LAN*, Alert on LAN2* and a slave functionality. It uses two signals: SMLINK[1:0]. SMLINK0 corresponds to an SMBus clock signal, and SMLINK1 corresponds to an SMBus data signal. These signals are part of the SMB Slave Interface.

For Alert on LAN* functionality, the ICH4 transmits heartbeat and event messages over the interface. When using the 82562EM/82562EX Platform LAN Connect Component, the ICH4's integrated LAN Controller will claim the SMLink heartbeat and event messages and send them out over the network. An external, Alert on LAN2*-enabled LAN Controller (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) will connect to the SMLink signals to receive heartbeat and event messages, as well as access the ICH4 SMBus Slave Interface. The slave interface function allows an external microcontroller to perform various functions. For example, the slave write interface can reset or wake a system, generate SMI# or interrupts, and send a message. The slave read interface can read the system power state, read the watchdog timer status, and read system status bits.

Both the SMBus Host Controller and the SMBus Slave Interface obey the SMBus 1.0 protocol, so the two interfaces can be externally wire-OR'd together to allow an external management ASIC (e.g., 82562EM/82562EX 10/100 Mbps Platform LAN Connect) to access targets on the SMBus as well as the ICH4 Slave interface. Additionally, the ICH4 supports slave functionality, including the Host Notify protocol, on the SMLink pins. Therefore, to be fully compliant with the SMBus 2.0 specification (which requires the Host Notify cycle), the SMLink and SMBus signals must be tied together externally. This is done by connecting SMLink0 to SMBCLK, and SMLink1 to SMBDATA.

Figure 10-25. SMBUS 2.0/SMLink Interface
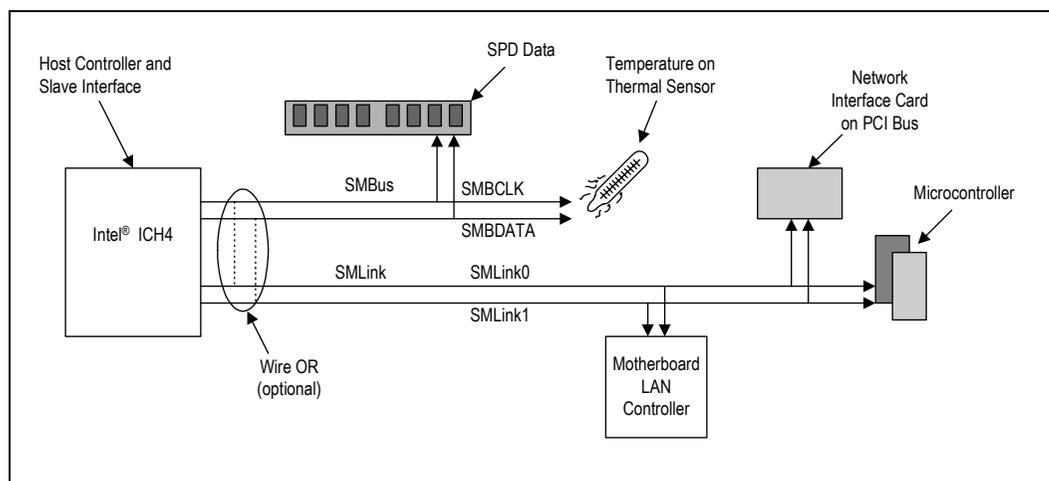
NOTE: Intel does not support external access of the ICH4's Integrated LAN Controller via the SMLink interface. Also, Intel does not support access of the ICH4's SMBus Slave Interface by the ICH4's SMBus Host Controller. Refer to the ICH4 datasheet for full functionality descriptions of the SMLink and SMBus interface.

10.3.9.1   SMBus Architecture and Design Considerations

10.3.9.1.1   SMBus Design Considerations

There is not a single SMBus design solution that will work for all platforms. One must consider the total bus capacitance and device capabilities when designing SMBus segments. Routing SMBus to the PCI slots makes the design process even more challenging since they add so much capacitance to the bus. This extra capacitance has a large affect on the bus time constant which in turn affects the bus rise and fall times.

Primary considerations in the design process are:

- Device class (High/Low power). Most designs use primarily High Power Devices.

- Are there devices that must run in S3?

- Amount of VCC_suspend current available (i.e., minimizing the load of VCC_suspend).

10.3.9.1.2   General Design Issues / Notes

Regardless of the architecture used, there are some general considerations.

- The pull-up resistor size for the SMBus data and clock signals is dependent on the bus load (this includes all device leakage currents). Generally, the SMBus device that can sink the least amount of current is the limiting agent on how small the resistor can be. The pull-up resistor cannot be made so large that the bus time constant (Resistance X Capacitance) does not meet the SMBus rise and time specification.

- The maximum bus capacitance that a physical segment can reach is 400 pF.

- The ICH4 does not run SMBus cycles while in S3.

- SMBus devices that can operate in STR must be powered by the VCC_suspend supply.

- If SMBus is connected to PCI, it must be connected to all PCI slots.

10.3.9.1.3   High Power/Low Power Mixed Architecture

This design allows for current isolation of high and low current devices and also allows SMBus devices to communicate while in S3. VCC_suspend leakage is minimized by keeping non-essential devices on the core supply. This is accomplished by the use of an "FET" to isolate the devices powered by the core and suspend supplies (See Figure 10-26).

Figure 10-26. High Power/Low Power Mixed VCC_suspend/VCC Architecture
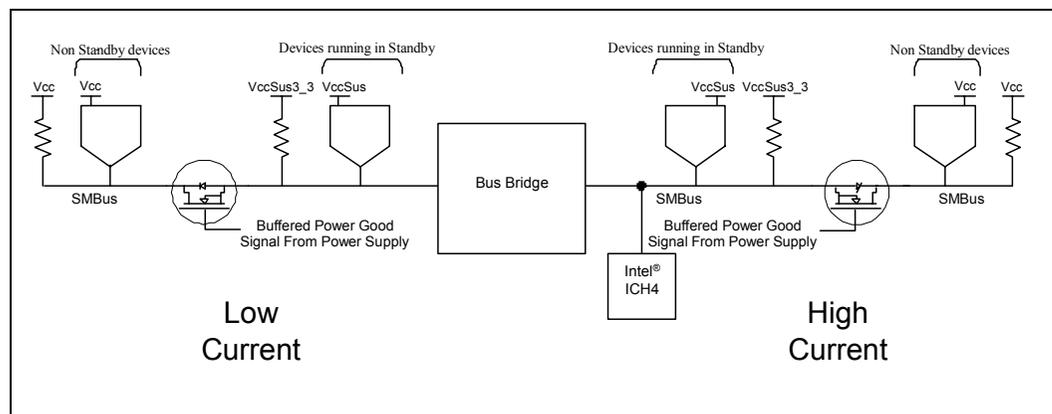
Added Considerations for Mixed Architecture

- The bus switch must be powered by VCC_suspend.

- Devices that are powered by the VCC_suspend well must not drive into other devices that are powered off. This is accomplished with the "bus switch".

- The bus bridge can be a device like the Phillips* PCA9515

10.3.9.2   Calculating The Physical Segment Pull-Up Resistor

The following tables are provided as a reference for calculating the value of the pull-up resistor that may be used for a physical bus segment. If any physical bus segment exceeds 400 pF, a bus bridge device such as the Phillips PCA9515 must be used to separate the physical segment into two segments that individually have a bus capacitance less than 400 pF.

Table 10-15. Bus Capacitance Reference Chart

Device	No. of Devices/ Trace Length	Capacitance Includes	Cap (pF)
Intel® ICH4	1	Pin Capacitance	12
CK408	1	Pin Capacitance	10
DIMMS	2	Pin Capacitance (10 pF) + 1 inch worth of trace capacitance (2 pF/inch) per DIMM and 2 pF connector capacitance per DIMM	28
PCI Slots	2	Each PCI add-in card is allowed up to 40 pF + 3 pF per each connector	86
	3		129
	4		172
	5		215
	6		258
SMBus Trace Length in inches	≥24	2 pF per inch of trace length	48
	≥36		72
	≥48		96
CNR	1	Pin Capacitance (10 pF) + 6 inch worth of trace capacitance (2 pF/inch) and 2 pF connector capacitance	24

Table 10-16. Bus Capacitance/Pull-Up Resistor Relationship

Physical Bus Segment Capacitance	Pull-Up Range (For VCC = 3.3 V
0 to 100 pF	8.2 kΩ to 1.2 kΩ
100 to 200 pF	4.7 kΩ to 1.2 kΩ
200 to 300 pF	3.3 kΩ to 1.2 kΩ
300 to 400 pF	2.2 kΩ to 1.2 kΩ

10.3.10   PCI

The ICH4 provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification, Revision 2.2*. The implementation is optimized for high-performance data streaming when the ICH4 is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, refer to the *PCI Local Bus Specification Revision 2.2*.

The ICH4 supports six PCI Bus masters (excluding the ICH4) by providing six REQ#/GNT# pairs. In addition, the ICH4 supports two PC/PCI REQ#/GNT# pairs, one of which is multiplexed with a PCI REQ#/GNT# pair.

10.3.10.1   PCI Routing Summary

The following represents a summary of the routing guidelines for the PCI Slots. Simulations assume that PCI cards follow the PCI Specification, Revision 2.2 trace length guidelines.

Figure 10-27. PCI Bus Layout Example
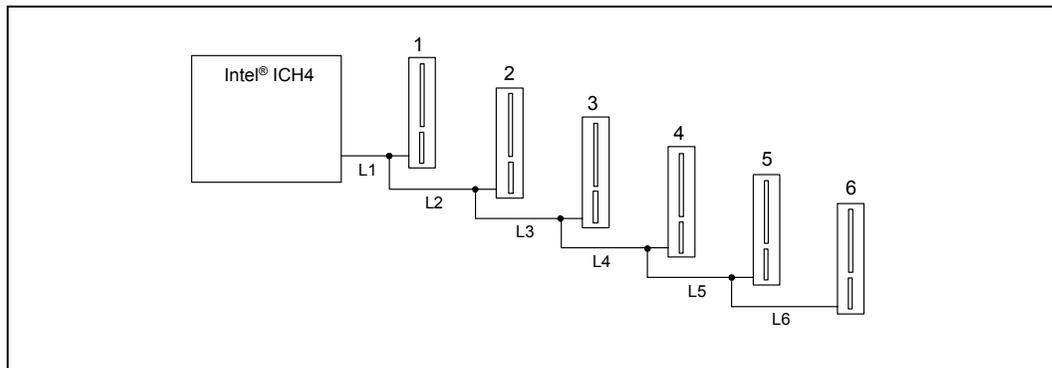
NOTE: If a CNR connector is placed on the platform, it will share a slot space with one of the PCI slots. However, it will not take away from the slot functionality.

Figure 10-28. PCI Bus Layout Example with IDSEL
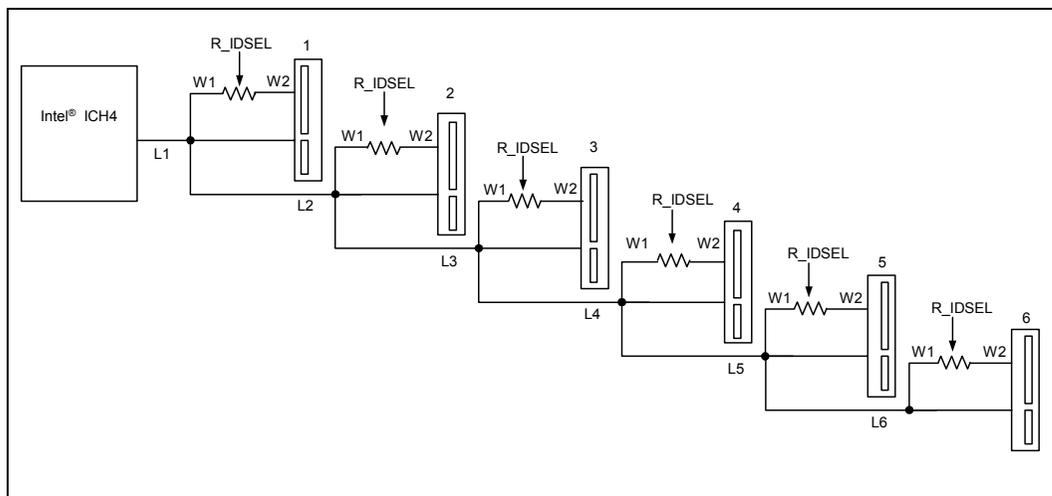
Table 10-17. PCI Data Signals Routing Summary

Trace Impedance	Topology	Maximum Trace Length					
		L1	L2	L3	L4	L5	L6
47 Ω – 69 Ω, 60 Ω target	2 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	N/A	N/A	N/A	N/A
	3 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.5 inches	1.5 inches	N/A	N/A	N/A
	4 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	4 to 10 inches	1.0 inches	1.0 inches	1.0 inches	N/A	N/A
51 Ω – 69 Ω, 60 Ω target	5 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 8 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	N/A
	6 Slots W1=W2= 0.5 inches, R_IDSEL = 300 to 900 Ω	5 to 7 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches	1.0 inches

Figure 10-29. PCI Clock Layout Example
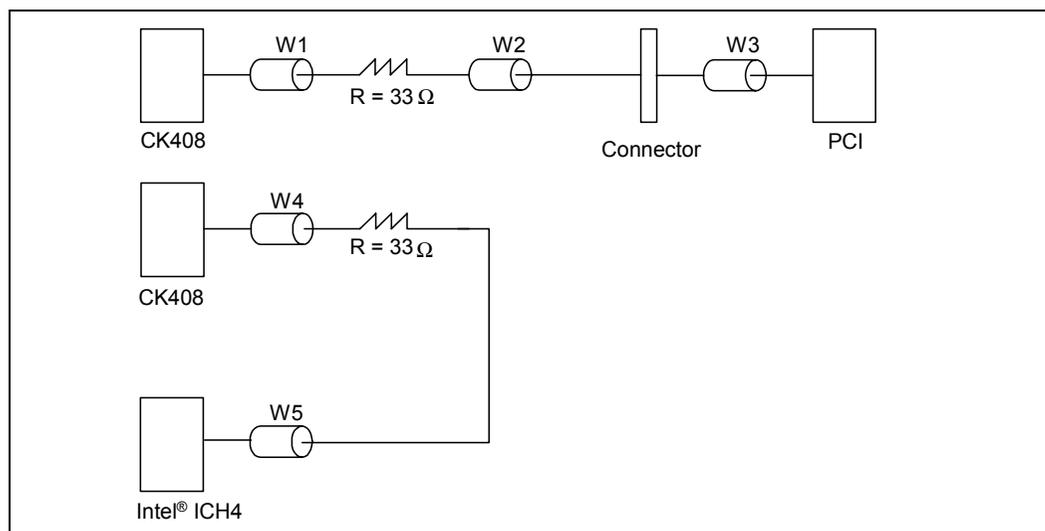
Table 10-18. PCI Clock Signals Routing Summary

Trace Impedance	Topology	Maximum Trace Length				
		W1	W2	W3	W4	W5
51 Ω – 69 Ω, 60 Ω target	2–6 slots	0.5 inches	(W5 – 4.5) inches	2.5 inches (shown as reference only)	0.5 inches	Can be as long as needed as long as W2 is scaled accordingly

10.3.11 RTC

The ICH4 contains a real time clock (RTC) with 256 bytes of battery-backed SRAM. The internal RTC module provides two key functions: keeping date and time and storing system data in its RAM when the system is powered down.

The ICH4 uses a crystal circuit to generate a low-swing 32 kHz input sine wave. This input is amplified and driven back to the crystal circuit via the RTCX2 signal. Internal to the ICH4, the RTCX1 signal is amplified to drive internal logic as well as to generate a free running full swing clock output for system use. This output ball of the ICH4 is called SUSCLK (see Figure 10-30).

Figure 10-30. RTCX1 and SUSCLK Relationship in Intel® ICH4
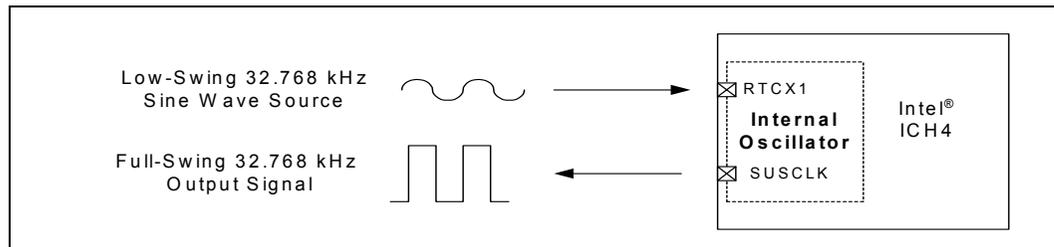
For further information on the RTC, refer to Application Note AP-728 *ICH/ICH4/ICH4-M/ICH3-S/ICH3-M Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions*. This application note is valid for ICH4.

Even if the ICH4 internal RTC is not used, it's still necessary to supply a clock input to RTCX1 of the ICH4 because other signals are gated from that clock in suspend modes. However, in this case, the frequency accuracy (32.768 kHz) of the clock inputs is not critical, a cheap crystal can be used, or a single clock input can be driven into RTCX1 with RTCX2 left as no connect (see Figure 10-31). This is not a validated feature on ICH4.

Note: The peak to peak swing on RTCX1 cannot exceed 1.0 V.

Figure 10-31. External Circuitry for the Intel® ICH4 (Internal RTC Is Not Used)
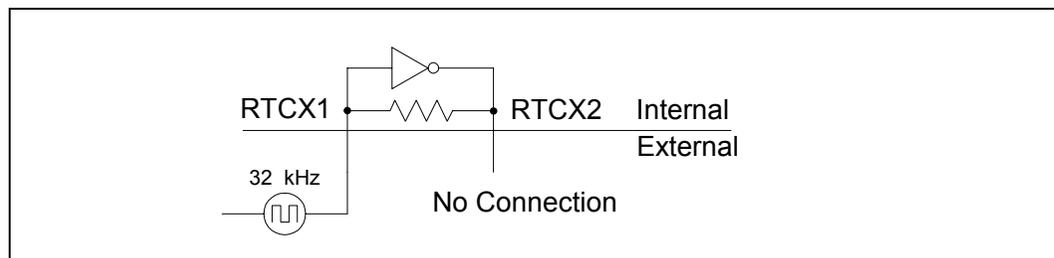
10.3.11.1 RTC Crystal

The ICH4 RTC module requires an external oscillating source of 32.768 kHz connected on the RTCX1 and RTCX2 balls. Figure 10-32 shows the external circuitry that comprises the ICH4 RTC oscillator.

Figure 10-32. External Circuitry for the Intel® ICH4 RTC
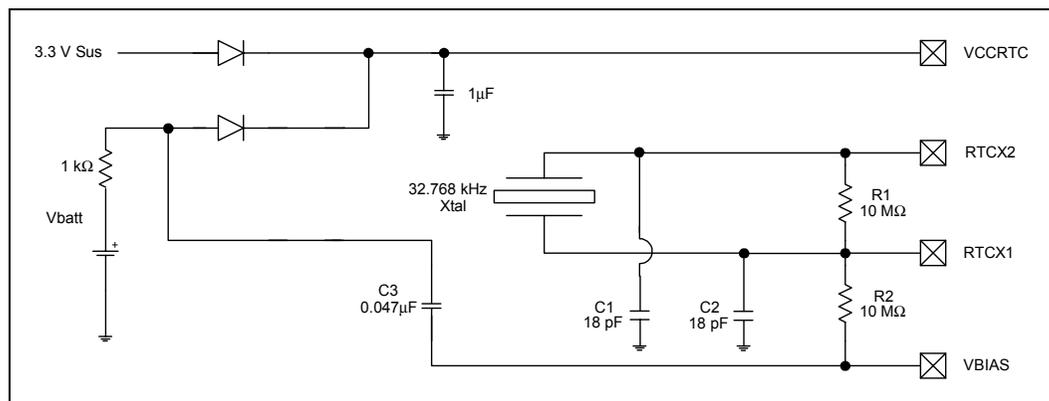
NOTES:
1. The exact capacitor value must be based on the crystal maker's recommendation. (Typical values for C1 and C2 are 18 pF, based on crystal load of 12.5 pF).
2. VccRTC: Power for RTC Well
3. RTCX2: Crystal Input 2 – Connected to the 32.768 kHz crystal.
4. RTCX1: Crystal Input 1 – Connected to the 32.768 kHz crystal.
5. VBIAS: RTC BIAS Voltage – This ball is used to provide a reference voltage. This DC voltage sets a current that is mirrored throughout the oscillator and buffer circuitry.
6. VSS: Ground

Table 10-19. RTC Routing Summary

Trace Impedance	Max Trace Length to Crystal	Signal Length Matching	R1, R1, C1, and C2 Tolerances	Signal Referencing
51 Ω – 69 Ω, 60 Ω target	1 inch	N/A	R1 = R2 = 10 MΩ ± 5% C1 = C2 = (NPO class) See Section 10.3.11.2 for calculating a specific capacitance value for C1 and C2	Ground

10.3.11.2   External Capacitors

To maintain the RTC accuracy, the external capacitor C3 must be 0.047 µF, and capacitor values C_1 and C_2 should be chosen to provide the manufacturer's specified load capacitance (C_{LOAD}) for the crystal when combined with the parasitic capacitance of the trace, socket (if used), and package. The following equation can be used to choose the external capacitance values:

$$C_{LOAD} = [(C_1 + C_{IN1} + C_{TRACE1})*(C_2 + C_{IN2} + C_{TRACE2})]/[(C_1 + C_{IN1} + C_{TRACE1} + C_2 + C_{IN2} + C_{TRACE2})] + C_{PARASITIC}$$

Where:

- C_{LOAD} = crystal's load capacitance. This value can be obtained from Crystal's specification.

- C_{IN1}, C_{IN2} = input capacitances at the RTCX1, RTCX2 balls of the ICH4. These values can be obtained in the ICH4 datasheet.

- C_{TRACE1}, C_{TRACE2} = trace length capacitances measured from Crystal terminals to the RTCX1, RTCX2 pins. These values depend on the characteristics of board material, the width of signal traces, and the length of the traces. Typical value, based on a 5 mil wide trace and a ½ ounce copper pour, is approximately equal to:

  C_{TRACE} = trace length * 2 pF/inch (assuming a 5 mil trace ½ oz. copper)

- $C_{PARASITIC}$ = crystal's parasitic capacitance. This capacitance is created by the exist of 2 electrode plates and the dielectric constant of the crystal blank inside the crystal part. Refer to the crystal's specification to obtain this value.

Ideally, C1, C2 can be chosen such that C1 = C2. Using the C_{LOAD} equation, the value of C1, C2 can be calculated to give the best accuracy (closest to 32.768 kHz) of the RTC circuit at room temperature. However, C2 can be chosen such that C2 > C1. C1 can then be trimmed to obtain the 32.768 kHz.

In certain conditions, both C1, C2 values can be shifted away from the **theoretical values** (calculated values from the above equation) to obtain the closest oscillation frequency to 32.768 kHz. When C1, C2 value are smaller then the theoretical values, the RTC oscillation frequency will be higher.

The following example describes the calculation of practical C1, C2 values if theoretical values cannot guarantee the accuracy of the RTC in low temperature conditions:

Example 1

According to a required 12 pF load capacitance of a typical crystal that is used with the ICH4, the calculated values of C1 = C2 is 10 pF at room temperature (25 °C) to yield a 32.768 kHz oscillation.

At 0 °C the frequency stability of crystal is –23 ppm (assuming that the circuit has 0 ppm at 25 °C). This makes the RTC circuit oscillate at 32.767246 kHz instead of 32.768 kHz.

If the values of C1, C2 are chosen to be 6.8 pF instead of 10 pF, The RTC will oscillate at higher frequency at room temperature (+23 ppm), but this configuration of C1 / C2 makes the circuit oscillate closer to 32.768 kHz at 0 °C. The 6.8 pF value of C1 and 2 is the **practical value**.

Note that the temperature dependency of the crystal frequency is a parabolic relationship (ppm / degree square). The effect of changing crystal's frequency when operating at 0 °C (25 °C below room temperature) is the same when operating at 50 °C (25 °C above room temperature).

10.3.11.3   RTC Layout Considerations

Since the RTC circuit is very sensitive and requires highly accurate oscillation, reasonable care must be taken during RTC circuit layout and routing. Some recommendations are:

- Reduce trace capacitance by minimizing the RTC trace length. ICH4 requires a trace length less than 1 inch on each branch (from crystal's terminal to RTCXn pin). Routing the RTC circuit should be kept simple to simplify the trace length measurement and to increase the accuracy of trace capacitance calculations. Trace capacitance depends on the trace width and dielectric constant of board's material. On FR-4, a 5-mil trace has approximately 2 pF per inch.

- Trace signal coupling must be reduced by avoiding routing of adjacent PCI signals close to RTCX1, RTCX1, and VBIAS.

- Ground guard plane is highly recommended.

- The oscillator VCC should be clean. Use a filter, such as an RC low-pass or a ferrite inductor.

10.3.11.4   RTC External Battery Connection

The RTC requires an external battery connection to maintain its functionality and its RAM while the ICH4 is not powered by the system.

Example batteries are Duracell* 2032, 2025, and 2016 (or equivalent), which can give many years of operation. Batteries are rated by storage capacity. The battery life can be calculated by dividing the capacity by the average current required. For example, if the battery storage capacity is 170 µAh (assumed usable) and the average current required is 3 µA, the battery life will be at least:

$$170,000\ \mu Ah\ /\ 5\mu A = 34,000\ h = 3.9\ years$$

The voltage of the battery can affect the RTC accuracy. In general, when the battery voltage decays, the RTC accuracy also decreases. High accuracy can be obtained when the RTC voltage is in the range of 3.0 V to 3.3 V.

The battery must be connected to the ICH4 via an isolation Schottky diode circuit. The Schottky diode circuit allows the ICH4 RTC well to be powered by the battery when the system power is not available, and by the system power when it is available. To do this, the diodes are set to be reverse biased when the system power is not available. Figure 10-33 is an example of a diode circuit.

Figure 10-33. A Diode Circuit to Connect RTC External Battery
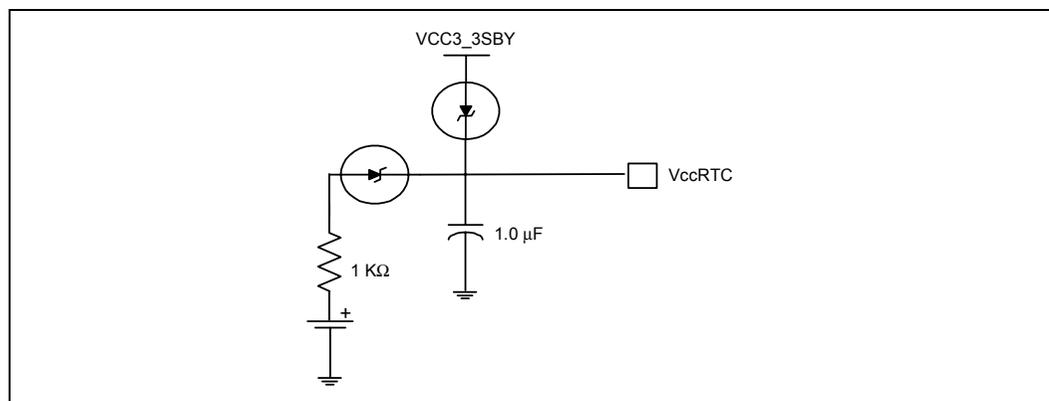
10.3.11.5 RTC External RTCRST# Circuit

Figure 10-34. RTCRST# External Circuit for the Intel® ICH4 RTC
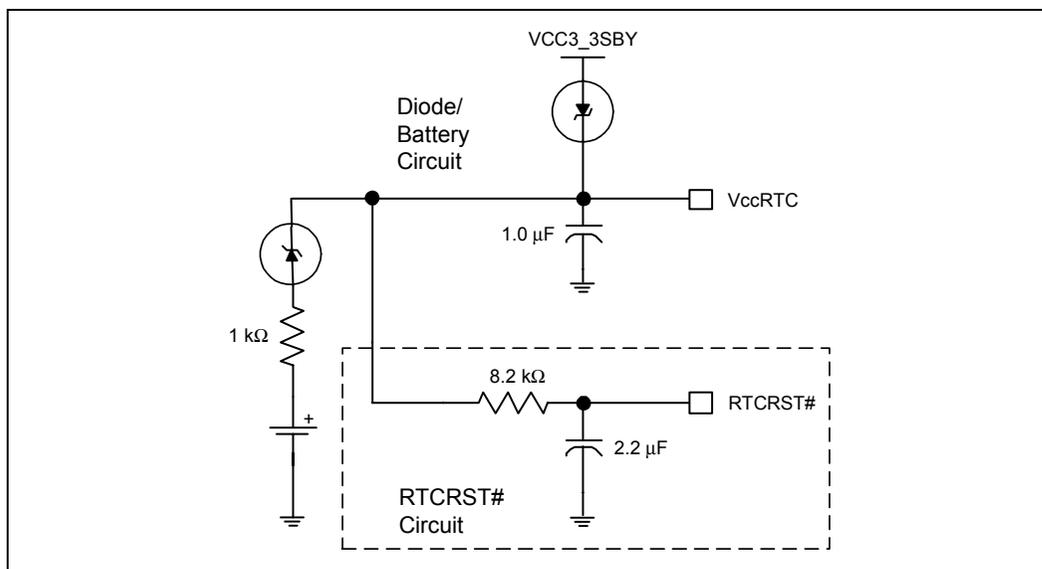
The ICH4 RTC requires some additional external circuitry. The RTCRST# signal is used to reset the RTC well. The external capacitor and the external resistor between RTCRST# and the RTC battery (Vbat) were selected to create an RC time delay such that RTCRST# will go high some time after the battery voltage is valid. The RC time delay should be in the range of 18 ms–25 ms. When RTCRST# is asserted, bit 2 (RTC_PWR_STS) in the GEN_PMCON_3 (General PM Configuration 3) register is set to 1 and remains set until software clears it. Therefore, when the system boots, the BIOS knows that the RTC battery has been removed.

This RTCRST# circuit is combined with the diode circuit (shown in the Figure 10-33) whose purpose is to allow the RTC well to be powered by the battery when the system power is not available. Figure 10-34 is and example of this circuitry that is used in conjunction with the external diode circuit.

10.3.11.6 VBIAS DC Voltage and Noise Measurements

VBIAS is a DC voltage level that is necessary for biasing the RTC oscillator circuit. This DC voltage level is filtered from the RTC oscillation signal by the RC Network of R2 and C3 (see Figure 10-32). Therefore, it is a self-adjusted voltage. Board designers should not manually bias the voltage level on VBIAS. Checking VBIAS level is used for testing purposes only to determine the right bias condition of the RTC circuit.

VBIAS should be at least 200 mV DC. The RC network of R2 and C3 filters out most of the AC signal that exists on this ball. However, the noise on this ball should be kept to a minimum to guarantee the stability of the RTC oscillation.

Probing VBIAS requires the same technique as probing the RTCX and RTCX2 signals (using Op-Amp). See Application Note AP-728 for further details about measuring techniques.

Note: VBIAS is very sensitive to environmental conditions.

10.3.11.7 SUSCLK

SUSCLK is a square waveform signal output from the RTC oscillation circuit. Depending on the quality of the oscillation signal on RTCX1 (largest voltage swing), the SUSCLK duty cycle can be between 30-70%. A SUSCLK duty cycle beyond the 30-70% range indicates a poor oscillation signal on RTCX1 and RTCX2.

SUSCLK can be probed directly using normal probe (50 Ω input impedance probe), and is an appropriated signal that is used to check the RTC frequency to determine the accuracy of the ICH4's RTC Clock (see Application Note AP-728 for further details).

10.3.11.8 RTC-Well Input Strap Requirements

All RTC-well inputs (RSMRST#, RTCRST#, INTRUDER#) must be either pulled up to VccRTC or pulled down to ground while in G3 state. RTCRST#, when configured as shown in Figure 10-34, meets this requirement. RSMRST# should have a weak external pull-down to ground, and INTRUDER# should have a weak external pull-up to VccRTC. This will prevent these nodes from floating in G3, and correspondingly will prevent $I_{CC}RTC$ leakage that can cause excessive coin-cell drain. The PWROK input signal should also be configured with an external weak pull-down.

10.3.12 Internal LAN Layout Guidelines

The ICH4 provides several options for LAN capability. The platform supports several components depending upon the target market. Available LAN components include the 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, 82562EZ/82562ET and 82562EX/82562EM Platform LAN Connect components.

Table 10-20. LAN Component Connections/Features

LAN Component	Interface To Intel® ICH4	Connection	Features
Intel® 82540EM (196 BGA)	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82551QM (196 BGA)	PCI	Performance 10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting, PCI 2.2 compatible
Intel® 82562EM (48 Pin SSOP) Intel® 82562EX (196 BGA)	LCI	10/100 Ethernet with Alert on LAN* (AoL) alerting	Ethernet 10/100 connection, Alert on LAN (AoL)
Intel® 82562ET (48 Pin SSOP) Intel® 82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection

Which LAN component to use on the ICH4 platform depends on the end user's need for connection speed, manageability, and bus connection type. In addition, footprint compatible packages make it possible to design a platform that can use any of the LAN components without the need for a motherboard redesign.

10.3.12.1 Footprint Compatibility

The 82540EM Gigabit Ethernet Controller, 82551QM Fast Ethernet Controller, and the 82562EX/82562EZ Platform LAN Connect devices are all manufactured in a footprint-compatible 15 mm x 15 mm (1 mm pitch), 196-ball grid array package. Many of the critical signal pin locations on the 82540EM, 82551QM, and 82562EX/82562EZ are identical, allowing designers to create a single design that accommodates any one of these parts. Because the use of some pins on the 82540EM differ from the use on the 82551QM or the 82562EX/82562EZ, the parts are not referred to as "pin compatible." The term "footprint compatible" refers to the fact that the parts share the same package size, same number and pattern of pins, and layout of signals that allow for the flexible, cost effective, multipurpose design.

Design guidelines are provided for each required interface and connection. Refer to the following figures and tables for the corresponding section of the design guide. The guidelines use the 82546EZ to refer to both the 82562EZ and the 82562EX. The 82562EX is specified in those cases where there is a difference.

Figure 10-35. Intel® ICH4/Platform LAN Connect Sections
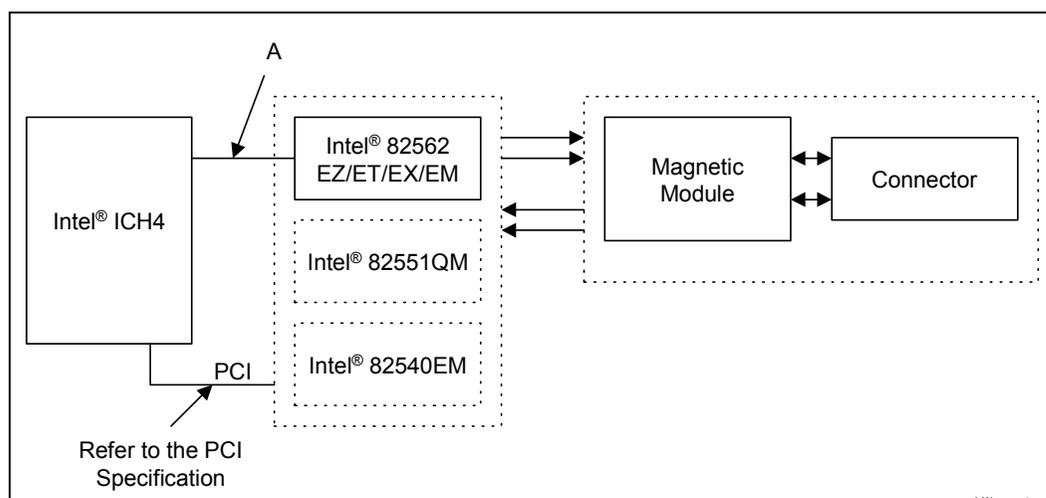
NOTE: 82562EZ/EX, 82551QM, and 82540EM are footprint compatible with each other. 82562ET/EM are footprint compatible with each other.

Table 10-21. LAN Design Guide Section Reference

Layout Section	Figure 10-35 Reference	Design Guide Section
Intel® ICH4 – LAN Connect Interface (LCI)	A	Section 10.3.12.2, "Intel® ICH4 – LAN Connect Interface Guidelines"
Intel® 82562EZ/EX Intel® 82562ET/EM	A	Section 10.3.13, "Design and Layout Considerations for Intel" 82562EZ/ET/EX/EM"

10.3.12.2 Intel® ICH4 – LAN Connect Interface Guidelines

This section contains guidelines on how to implement a Platform LAN Connect device on a system motherboard or on a CNR riser card. It should not be treated as a specification, and the system designer must ensure through simulations or other techniques that the system meets the specified timings. Special care must be given to matching the LAN_CLK traces to those of the other signals, as shown below. The following are guidelines for the ICH4 to LAN Connect Interface. The following signal lines are used on this interface:

- LAN_CLK
- LAN_RSTSYNC
- LAN_RXD[2:0]
- LAN_TXD[2:0]

This interface supports 82562ET and 82562EM components. Signal lines LAN_CLK, LAN_RSTSYNC, LAN_RXD0, and LAN_TXD0 are shared by all components.

10.3.12.2.1 Bus Topologies

The Platform LAN Connect Interface can be configured in several topologies:

- Direct point-to-point connection between the ICH4 and the LAN component
- LOM/CNR Implementation

LOM (LAN On Motherboard) or CNR Point-To-Point Interconnect

The following are guidelines for a single solution motherboard. Either 82562EM, 82562ET, or CNR are uniquely installed.

Figure 10-36. Single Solution Interconnect
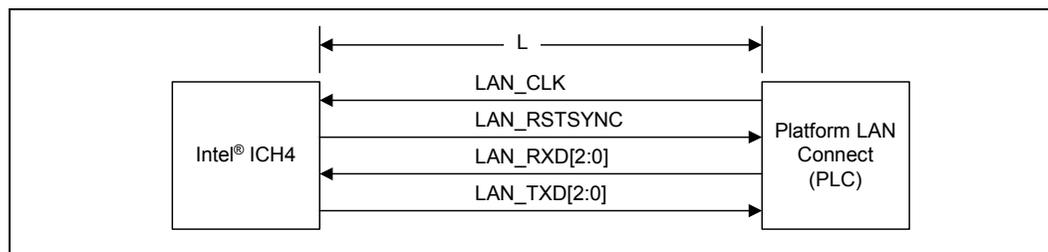
Table 10-22. LAN LOM or CNR Routing Summary

	Maximum Trace Length	Trace Impedance	Signal Referencing	LAN Signal Length Matching
Intel® 82562EZ/ET/ EX/EM	4.5 to 12 inches	51 Ω – 69 Ω, 60 Ω target	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/ET/ EX/EM on CNR	2 to 9.5 inches			

LOM (Lan On Motherboard) and CNR Interconnect

The following guidelines apply to an all-inclusive configuration of PLC design. This layout combines LAN on motherboard and the CNR solutions. The resistor pack ensures that either a CNR option or a LAN on motherboard option can be implemented at one time. (See Figure 10-37 and Table 10-23).

Figure 10-37. LOM/CNR Interconnect
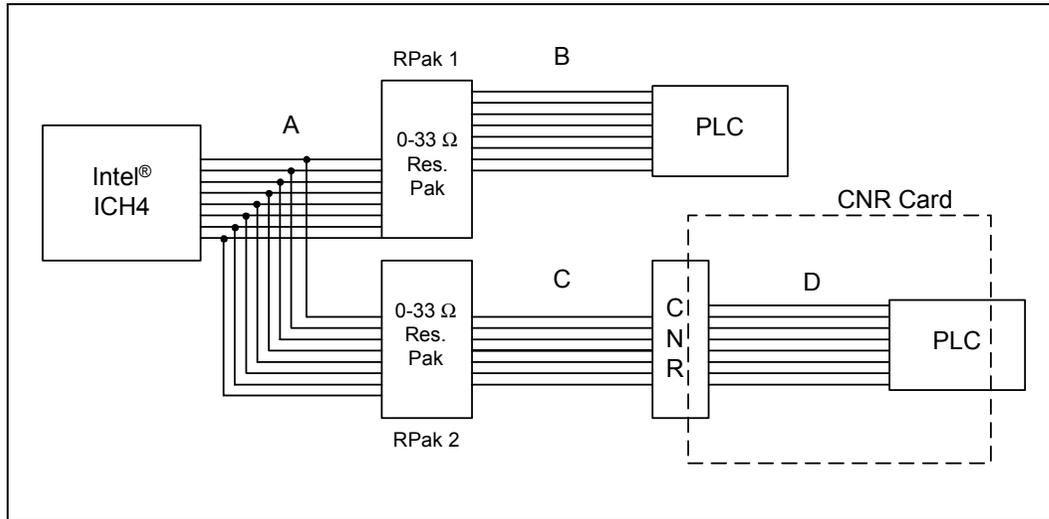
NOTE: Either RPak 1 or RPak 2 can be populated, but not both.

Table 10-23. LAN LOM/CNR 'Dual Routing Summary

	Maximum Trace Length				Trace Impedance	Signal Ref.	LAN Signal Length Matching
	A	B	C	D			
Intel® 82562EZ/ET/EX/EM	0.5 to 7.5 inches	4 to (11.5 –A) inches	NA	NA	51 Ω – 69 Ω, 60 Ω target	Ground	Data signals must be equal to or no more than 0.5 inches (500 mils) shorter than the LAN clock trace.
Intel® 82562EZ/ET/EX/EM on CNR[1]	0.5 to 7.5 inches	NA	1.5 to (9 –A) inches	0.5 to 3 inches			

NOTES:

1. Total motherboard trace length should not exceed 9 inches

Additional guidelines for this configuration are as follows:

- Stubs due to the resistor pack should not be present on the interface.
- The resistor pack value can be 0 to 33 Ω (See Section 10.3.12.2.5).

10.3.12.2.2 Signal Routing and Layout

Platform LAN Connect Interface signals must be carefully routed on the motherboard to meet the timing and signal quality requirements of this interface specification. The following are some general guidelines that should be followed. It is recommended that the board designer simulate the board routing to verify that the specifications are met for flight times and skews due to trace mismatch and crosstalk. On the motherboard the length of each data trace is either equal in length to the LAN_CLK trace, or up to 0.5 inches shorter than the LAN_CLK trace. (LAN_CLK should always be the longest motherboard trace in each group.)

Figure 10-38. LAN_CLK Routing Example
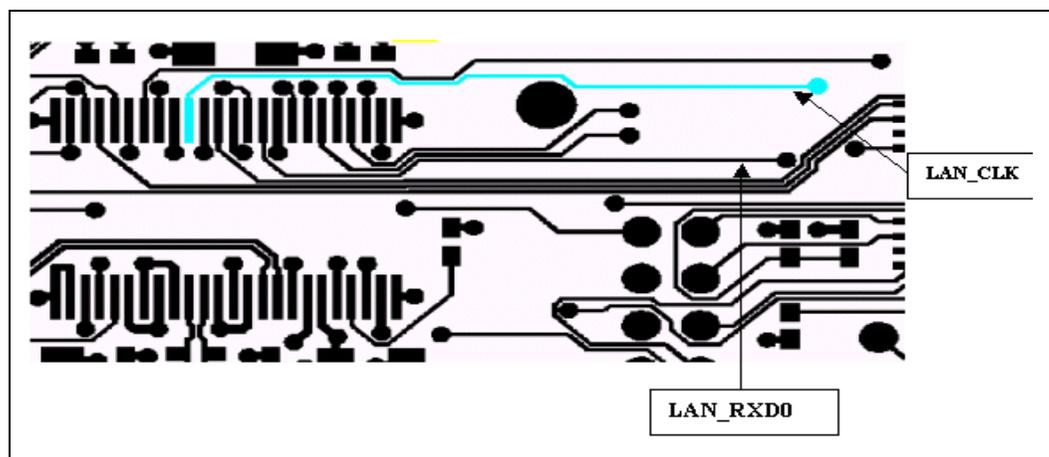
10.3.12.2.3 Crosstalk Consideration

Noise due to crosstalk must be carefully controlled to a minimum. Crosstalk is the key cause of timing skews and is the largest part of the tRMATCH skew parameter. tRMATCH is the sum of the trace length mismatch between LAN_CLK and the LAN data signals. To meet this requirement on the board, the length of each data trace is either equal to or up to 0.5 inches shorter than the LAN_CLK trace. Maintaining at least 100 mils of spacing should minimize noise due to crosstalk from non-PLC signals.

10.3.12.2.4 Impedances

The motherboard impedances should be controlled to minimize the impact of any mismatch between the motherboard and the add-in card. An impedance of 60 Ω ± 15% is strongly recommended; otherwise, signal integrity requirements may be violated.

10.3.12.2.5 Line Termination

Line termination mechanisms are not specified for the LAN Connect Interface. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, over/undershoot, and ringback. A 0 Ω to 33 Ω series resistor can be installed at the driver side of the interface should the developer have concerns about over/undershoot. Note that the receiver must allow for any drive strength and board impedance characteristic within the specified ranges.

10.3.12.2.6 Disabling Intel® ICH4 Integrated LAN

The LAN Connect Interface on the ICH4 can be left as a no-connect if it is not used.

10.3.13 Design and Layout Considerations for Intel® 82562EZ/ET/EX/EM

For correct LAN performance, designers must follow the general guidelines outlined in Section 10.3.12.2. Additional guidelines for implementing an 82562EZ/ET/EX/EM Platform LAN Connect component are provided below.

10.3.13.1 Guidelines for Intel® 82562EZ/ET/EX/EM Component Placement

Component placement can affect signal quality, emissions, and temperature of a board design. This section provides guidelines for component placement.

Careful component placement can:

- Decrease potential problems directly related to electromagnetic interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of space needed for the Ethernet LAN interface is important because all other interfaces will compete for physical space on a motherboard near the connector edge. As with most subsystems, the Ethernet LAN circuits must be as close as possible to the connector. Thus, it is imperative that all designs be optimized to fit in a very small space.

10.3.13.1.1 Crystals and Oscillators

To minimize the effects of EMI, clock sources should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference of communication. The retaining straps of the crystal (if they should exist) should be grounded to prevent possibility radiation from the crystal case, and the crystal should lay flat against the PC board to provide better coupling of the electromagnetic fields to the board.

For a noise-free and stable operation, place the crystal and associated discretes as close as possible to the 82562EZ/ET/EX/EM, keeping the trace length as short as possible, and do not route any noisy signals in this area.

10.3.13.1.2 Intel® 82562EZ/EX / Intel® 82551QM Termination Resistors

The 100 Ω (± 1%) resistor that is used to terminate the differential transmit pairs (TDP/TDN) and the 121 Ω ± 1% receive differential pairs (RDP/RDN) should be placed as close to the Platform LAN connect component 82562EZ/ET/EX/EM) as possible. This is because these resistors are terminating the entire impedance that is seen at the termination source (i.e., 82562ET), including the wire impedance reflected through the transformer.

Figure 10-39. Intel® 82562EZ/ET/EX/EM Termination
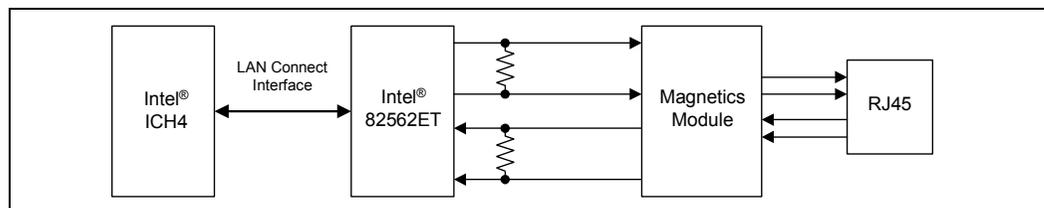
NOTE: Place termination resistors as close to the Intel® 82562ET as possible.

10.3.13.1.3 Critical Dimensions

There are two dimensions to consider during layout. Distance 'A' from the line RJ45 connector to the magnetics module, and distance 'B' from the 82562EZ/ET/EX/EM to the magnetics module. The combined total distances A and B must not exceed 4 inches (preferably, less than 2 inches). See Figure 10-40.

Figure 10-40. Critical Dimensions for Component Placement
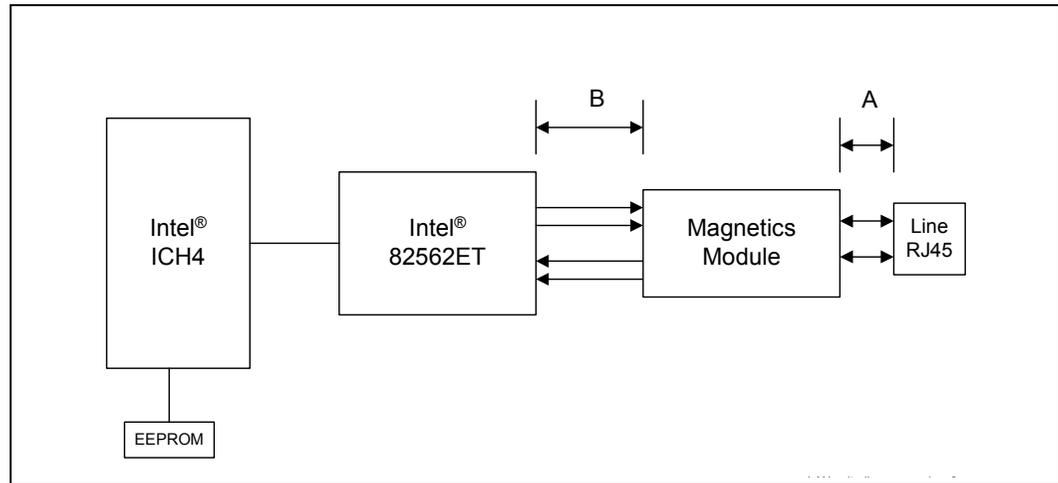
Table 10-24. Dimensions for Figure 10-40

Distance	Priority	Guideline
A	1	< 1 inch
B	2	< 1 inch

Distance from Magnetics Module to RJ45 (Distance A)

The distance A in Figure 10-40 above should be given the highest priority in board layout. The distance between the magnetics module and the RJ45 connector should be kept to less than one inch of separation. The following trace characteristics are important and should be observed:

- Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 60 Ω. However, the differential impedance can also be affected by the spacing between the traces.

- Trace Symmetry: Differential pairs (such as TDP and TDN) should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Caution: Asymmetric and unequal length traces in the differential pairs contribute to common mode noise. This can degrade the receive circuit's performance and contribute to radiated emissions from the transmit circuit. If the 82562EZ/ET/EX/EM must be placed further than a couple of inches from the RJ45 connector, distance B can be sacrificed. Keeping the total distance between the 82562EZ/ET/EX/EM and RJ45 as short as possible should be a priority.

Note: Measured trace impedance for layout designs targeting 100 Ω often result in lower actual impedance. OEMs should verify actual trace impedance and adjust their layout accordingly. If the actual impedance is consistently low, a target of 105 Ω–110 Ω should compensate for second order effects.

Distance from Intel® 82562EZ/ET/EX/EM to Magnetics Module (Distance B)

Distance B should also be designed to be less than one inch between devices. The high-speed nature of the signals propagating through these traces requires that the distance between these components be closely observed. In general, any section of traces that is intended for use with high-speed signals should observe proper termination practices. Proper termination of signals can reduce reflections caused by impedance mismatches between device and traces. The reflections of a signal may have a high-frequency component that may contribute more EMI than the original signal itself. For this reason, these traces should be designed to a 100 Ω differential value. These traces should also be symmetric and of equal length within each differential pair.

10.3.13.1.4 Reducing Circuit Inductance

The following guidelines show how to reduce circuit inductance in both back planes and motherboards. Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane. Similarly, every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible because signals with fast rise and fall times contain many high-frequency harmonics that can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and will reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

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Terminating unused connections

In Ethernet designs it is common practice to terminate unused connections on the RJ45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. The method most often implemented is called the "Bob Smith" Termination. In this method a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

10.3.13.1.5 Termination Plane Capacitance

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs (TDP/TDN and RDP/RDN) from the unused pairs of the RJ45. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termplane capacitance is not large enough to pass EFT (Electrical Fast Transient) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac to meet the EFT requirements.

Figure 10-41. Termination Plane
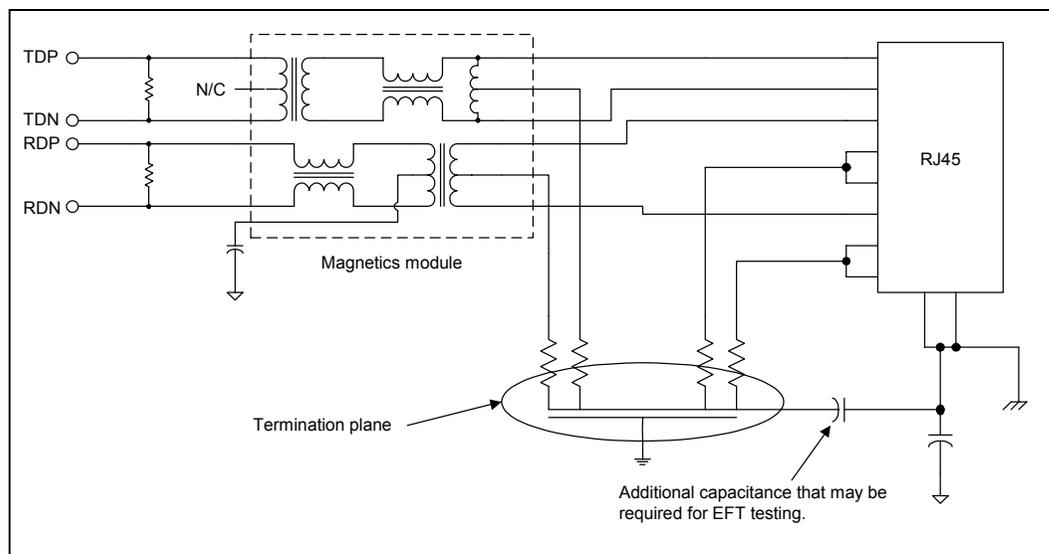
10.3.13.2 Intel® 82562EZ/ET/EX/EM Disable Guidelines

To disable the 82562EZ/ET/EX/EM, the device must be isolated (disabled) before assertion of reset (RSM_PWROK). Using a GPIO such as GPO28 to be LAN_Enable (enabled high), LAN will default to enabled on initial power-up and after an AC power loss. This circuit shown in Figure 10-42 allows this behavior. The BIOS controlling the GPIO can disable the LAN PHY.

Figure 10-42. Intel® 82562EZ/ET/EX/EM Disable Circuitry
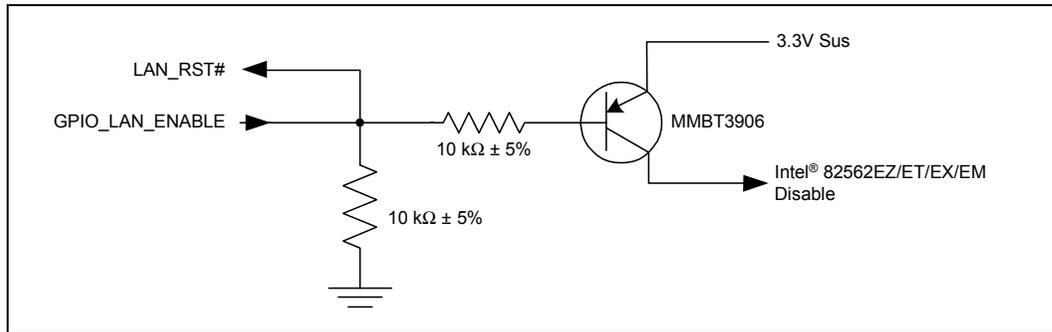
There are 4 pins that are used to put the 82562EZ/ET/EX/EM controller in different operating states: Test_En, Isol_Tck, Isol_Ti, and Isol_Tex. Table 10-25 describes the operational/disable features for this design.

The four control signals shown in Table 10-25 should be configured as follows:

- Test_En should be pulled-down through a 100 Ω resistor.

- The remaining 3 control signals should each be connected through 100 Ω series resistors to the common node *Intel® 82562EZ/ET/EX/EM _Disable* of the disable circuit.

Table 10-25. Intel® 82562EZ/ET/EX/EM Control Signals

Test_En	Isol_Tck	Isol_Ti	Isol_Tex	State
0	0	0	0	Enabled
0	1	1	1	Disabled w/ Clock (low power)
1	1	1	1	Disabled w/out Clock (lowest power)

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10.3.13.3 General LAN Differential Pair Trace Routing Considerations

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance.

Note: Some suggestions are specific to a 4.3 mil stack-up.):

- Maintain constant symmetry and spacing between the traces within a differential pair.

- Keep the signal trace lengths of a differential pair equal to each other.

- Keep the total length of each differential pair under 4 inches. [Many customer designs with differential traces longer than 5 inches have had one or more of the following issues: IEEE phy conformance failures, excessive EMI (Electro Magnetic Interference), and/or degraded receive BER (Bit Error Rate).]

- Do not route the transmit differential traces closer than 100 mils to the receive differential traces.

- Do not route any other signal traces both parallel to the differential traces, and closer than 100 mils to the differential traces (300 mils is recommended).

- Keep maximum separation between differential pairs to 7 mils.

- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90 degree bend is required, it is recommended to use two,45 degree bends. Refer to Figure 10-43.

- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.

- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.

Figure 10-43. Trace Routing
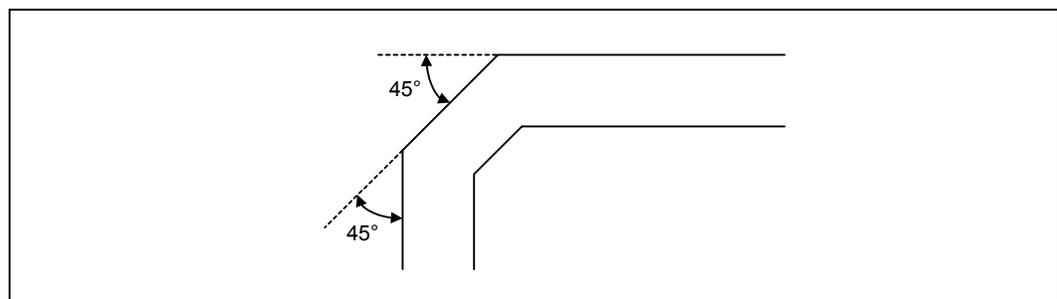
10.3.13.3.1 Trace Geometry and Length

The key factors in controlling trace EMI radiation are the trace length, and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane. Differential trace impedances should be controlled to be ~100 Ω. It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge-to-edge).

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. For similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance. Additionally, the PLC should not be closer than one inch to the connector/magnetics/ edge of the board.

10.3.13.3.2 Signal Isolation

The following are rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Note: Over the length of the trace run, each differential pair should be at least 0.3 inches away from any parallel signal traces.

- Physically group together all components associated with one clock trace to reduce trace length and radiation.

- Isolate I/O signals from High-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.

- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

10.3.13.3.3   Magnetics Module General Power and Ground Plane Considerations

To properly implement the common mode choke functionality of the magnetics module, the chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum.

Figure 10-44. Ground Plane Separation
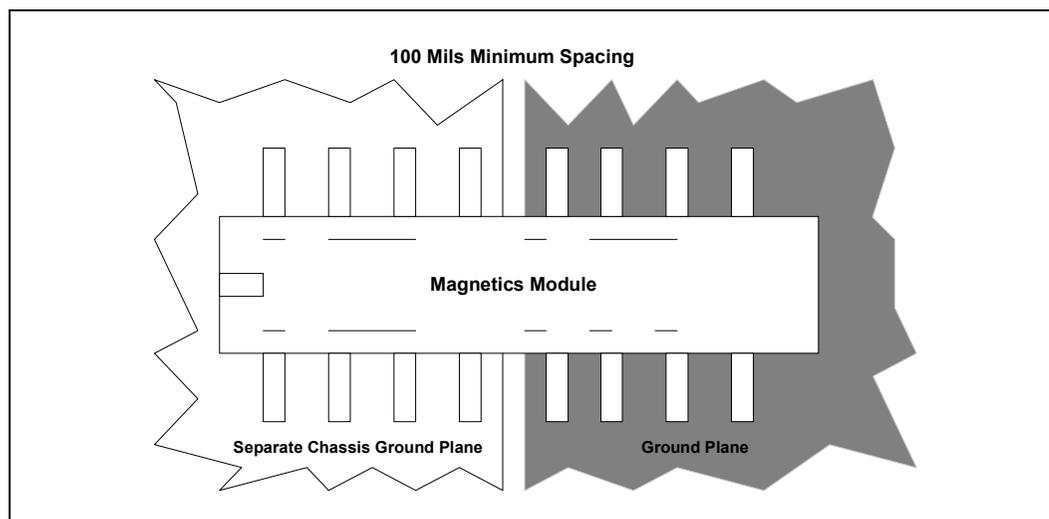
Good grounding requires minimizing inductance levels in the interconnections, and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions (do not route over a split plane). If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.

- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.

- All ground vias should be connected to every ground plane, and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.

- Physically locate grounds between a signal path and its return. This will minimize the loop area.

- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high-frequency harmonics that can radiate EMI.

- The ground plane beneath the filter/transformer module should be split. The RJ45 connector side of the transformer module should have chassis ground beneath it. By splitting ground planes beneath transformer, noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the transformer is minimized. There should not be a power plane under the magnetics module.

10.3.13.3.4   Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN On Motherboard Designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.

2. Lack of symmetry between the two traces within a differential pair. (Each component and/or via that one trace encounters must be encountered by the other trace at the same distance from the PLC.) Asymmetry can create common-mode noise and can distort the waveforms.

3. Excessive distance between the PLC and the magnetics, or between the magnetics and the RJ45 connector. Beyond a total distance of about 4 inches, it can become extremely difficult to design a spec-compliant LAN product. Long traces on FR4 (fiberglass epoxy substrate) will attenuate the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer (see #9 below). The magnetics should be as close to the connector as possible (= one inch).

4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive emissions (failing FCC), and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.3 inches from the differential traces.

5. Routing the transmit differential traces next to the receive differential traces. The transmit trace that is closest to one of the receive traces will put more crosstalk onto the closest receive trace and can greatly degrade the receiver's BER over long cables. After exiting the PLC, the transmit traces should be kept 0.3 inches or more away from the nearest receive trace. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ45, and the PLC.

6. Use of an inferior magnetics module. The magnetics modules that we use have been fully tested for IEEE PLC conformance, long cable BER, and for emissions and immunity. (Inferior magnetics modules often have less common-mode rejection and/or no auto transformer in the transmit channel.)

7. Use of an 82555 or 82558 physical layer schematic in a PLC design. The transmit terminations and decoupling are different. There are also differences in the receive circuit. Follow the appropriate reference schematic or Application Note.

8. Not using (or incorrectly using) the termination circuits for the unused pins at the RJ45 and for the wire-side center-taps of the magnetics modules. These unused RJ pins and wire-side center-taps must be correctly referenced to chassis ground via the proper value resistor and a capacitance or termplane. If these are not terminated properly, there can be emissions (FCC) problems, IEEE conformance issues, and long cable noise (BER) problems. The Application Notes have schematics that illustrate the proper termination for these unused RJ pins and the magnetics center-taps.

9. Incorrect differential trace impedances. It is important to have ~100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. It is very common to see customer designs that have differential trace impedances between 75 Ω and 85 Ω, even when the designers think they've designed for 100 Ω. (To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge-to-edge capacitive coupling between the two traces. When the two traces within a differential pair are kept close[2] to each other, the edge coupling can lower the effective differential impedance by 5 Ω - 20 Ω. A 10 Ω – 15 Ω drop in impedance is common.) Short traces will have fewer problems if the differential impedance is a little off.

10. Use of capacitor that is too large between the transmit traces and/or too much capacitance from the magnetic's transmit center-tap (on the Intel 82562ET side of the magnetics) to ground. Using capacitors more than a few pF in either of these locations can slow the 100 Mbps rise and fall time so much that they fail the IEEE rise time and fall time specs. This will also cause return loss to fail at higher frequencies, and will degrade the transmit BER performance. Caution should be exercised if a cap is put in either of these locations. If a cap is used, it should almost certainly be less than 22 pF. (6 pF to 12 pF values have been used on past designs with reasonably good success.) These caps are not necessary unless there is some overshoot in 100 Mbps mode.

Note:

1. It is important to keep the two traces within a differential pair close[2] to each other. Keeping them close[2] helps to make them more immune to crosstalk and other sources of common-mode noise. This also means lower emissions (i.e., FCC compliance) from the transmit traces, and better receive BER for the receive traces.

2. *Close* should be considered to be less than 0.030 inches between the two traces within a differential pair. 0.007 inch trace-to-trace spacing is recommended.

10.4 FWH Guidelines

The following provides general guidelines for compatibility and design recommendations for supporting the FWH device. The majority of the changes will be incorporated in the BIOS. Refer to the FWH BIOS Specification or equivalent.

10.4.1 FWH Vendors

The following vendors manufacture firmware hubs that conform to the Intel FWH Specification. Contact the vendor directly for information on packaging and density.

- SST   http://www.ssti.com/
- STM   http://us.st.com/stonline/index.shtml
- ATMEL   http://www.atmel.com

10.4.2 FWH Decoupling

A 0.1 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple high-frequency noise, which may affect the programmability of the device. Additionally, a 4.7 µF capacitor should be placed between the VCC supply pins and the VSS ground pins to decouple low frequency noise. The capacitors should be placed no further than 390 mils from the VCC supply pins.

10.4.3   In Circuit FWH Programming

All cycles destined for the FWH will appear on PCI. The ICH4 hub interface to PCI Bridge will put all processor boot cycles out on PCI (before sending them out on the FWH interface). If the ICH4 is set for subtractive decode, these boot cycles can be accepted by a positive decode agent on the PCI bus. This enables the ability to boot from a PCI card that positively decodes these memory cycles. To boot from a PCI card, it is necessary to keep the ICH4 in subtractive decode mode. If a PCI boot card is inserted and the ICH4 is programmed for positive decode, there will be two devices positively decoding the same cycle.

10.4.4   FWH INIT# Voltage Compatibility

The FWH INIT# signal trip points must be considered because they are **not** consistent among different FWH manufacturers. The INIT# signal is active low. Therefore, the inactive state of the ICH4 INIT# signal must be at a value slightly higher than the VIH min FWH INIT# pin specification. The ICH4 inactive state of this signal is typically governed by the formula V_CPU_IOmin - noise margin. Therefore if the V_CPU_IOmin of the processor is 1.6 V, the noise margin is 200 mV, and the VIH min spec of the FWH INIT# input signal is 1.35 V, there would be no compatibility issue because 1.6 V–0.2 V = 1.40 V, which is greater than the 1.35 V minimum of the FWH. If the VIH min of the FWH is 1.45 V there would be an incompatibility, and logic translation would have be used. Note that these examples do not take into account actual noise that may be encountered on INIT#. Care must be taken to ensure that the VIH min specification is met with ample noise margin.

See Section 5.4.1.3 for INIT# topology and guidelines. The voltage translator circuitry is shown in Figure 10-45.

Figure 10-45. FWH Level Translation Circuit
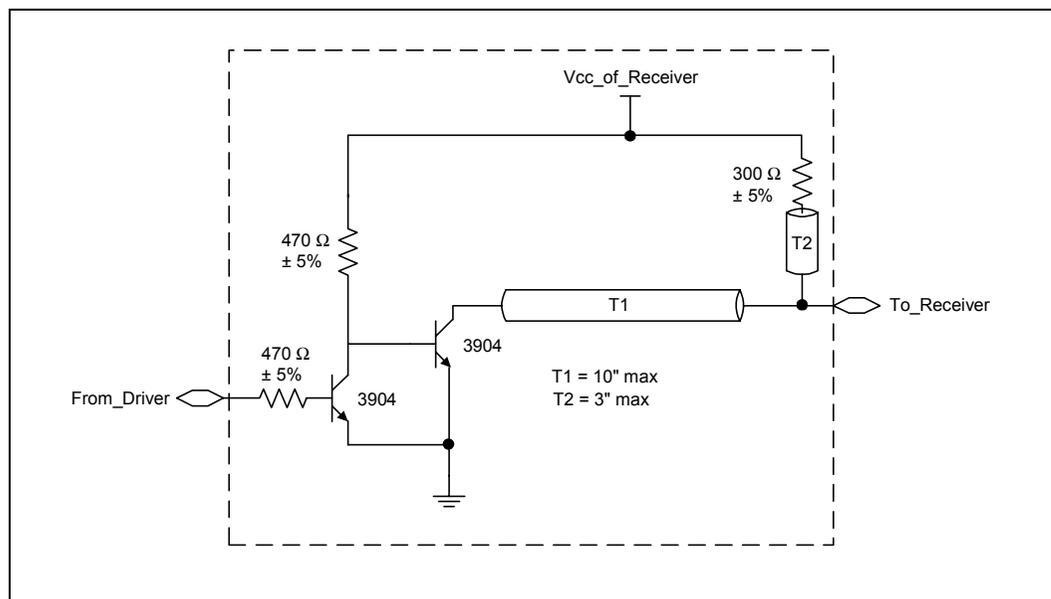
10.4.5   FWH V$_{PP}$ Design Guidelines

The V$_{PP}$ pin on the FWH is used for programming the flash cells. The FWH supports V$_{PP}$ of 3.3 V or 12 V. If V$_{PP}$ is 12 V, the flash cells will program about 50% faster than at 3.3 V. However, the FWH supports 12 V V$_{PP}$ for only 80 hours (3.3 V on V$_{PP}$ does not affect the life of the device). The 12 V V$_{PP}$ would be useful in a programmer environment, which is typically an event that occurs very infrequently (much less than 80 hours). The V$_{PP}$ pin **must** be tied to 3.3 V on the motherboard.

In some instances, it is desirable to program the FWH during assembly with the device soldered down on the board. To decrease programming time it becomes necessary to apply 12 V to the V$_{PP}$ pin. The following circuit allows testers to put 12 V on the V$_{PP}$ pin while keeping this voltage separated from the 3.3 V plane to which the rest of the power pins are connected. This circuit also allows the board to operate with 3.3 V on this pin during normal operation.

Figure 10-46. FWH V$_{PP}$ Isolation Circuitry
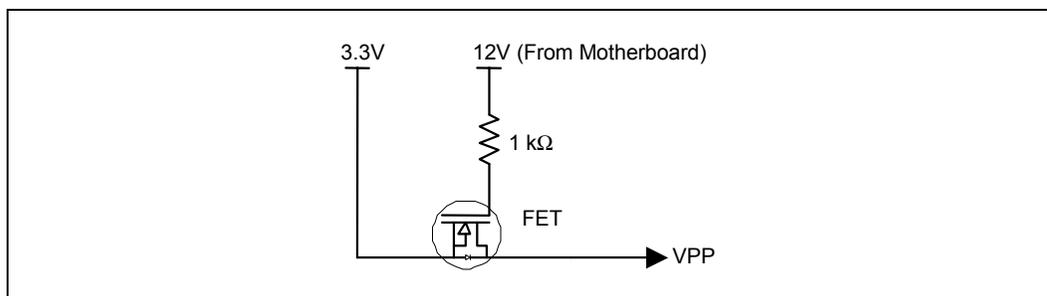
10.5 Power Management Interface

10.5.1 SYS_RESET# Usage Model

The System Reset ball (SYS_RESET#) on the ICH4 can be connected directly to the reset button on the systems front panel provided that the front panel header pulls this signal up to 3.3 V standby through a weak pull-up resistor. The ICH4 will debounce signals on this pin (16 ms) and will allow the SMBus to go idle before resetting the system; thus helping prevent a slave device on the SMBus from "hanging" by resetting in the middle of a cycle.

10.5.2 PWRBTN# Usage Model

The Power Button ball (PWRBTN#) on the ICH4 can be connected directly to the power button on the systems front panel. This signal is internally pulled-up in the ICH4 to 3.3 V standby through a weak pull-up resistor (24 kΩ nominal). The ICH4 has 16 ms of internal debounce logic on this pin.

Figure 10-47. SYS_RESET# and PWRBTN# Connection
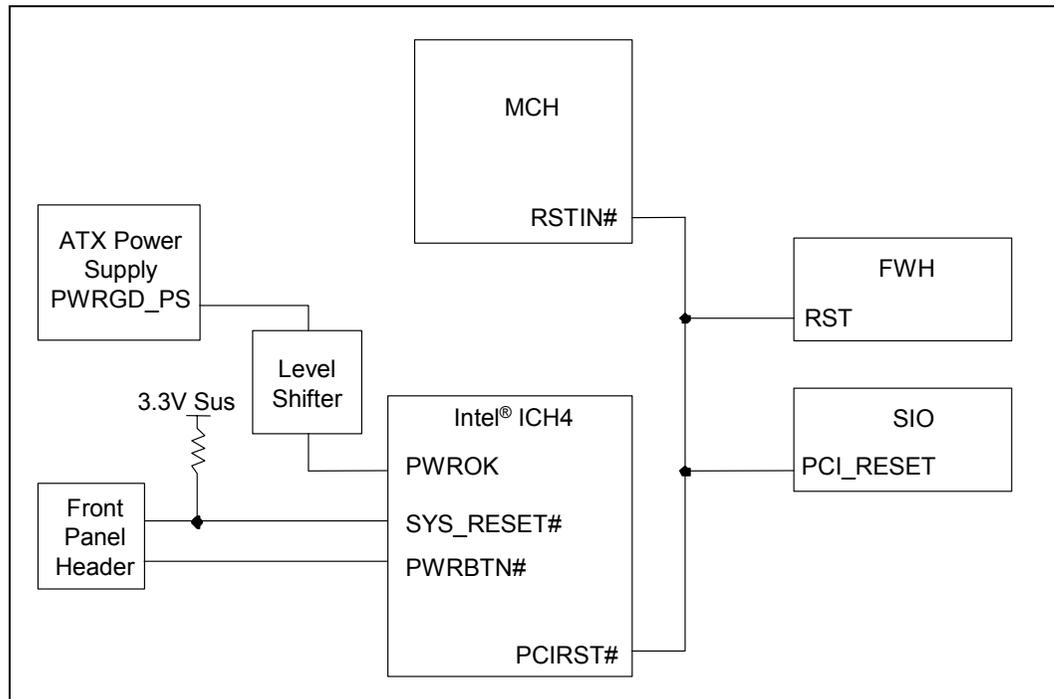
10.6 Power-Well Isolation Control Requirements

The RSMRST# signal of the ICH4 must transition from 20% signal level to 80% signal level and vice-versa in 50 µs. Slower transitions may result in excessive droop on the VccRTC node during Sx-to-G3 power state transitions (removal of AC power). Droop on this node can potentially cause the CMOS to be cleared or corrupted, the RTC to loose time after several AC power cycles, or erroneous intruder bit assertion.

The circuit shown in Figure 10-48 can be implemented to control well isolation between the VccSus3_3 and RTC power-wells in the event that RSMRST# is not being actively asserted during the discharge of the standby rail or does not meet the 50 µs rise/fall time.

Figure 10-48. RTC Power Well Isolation Control
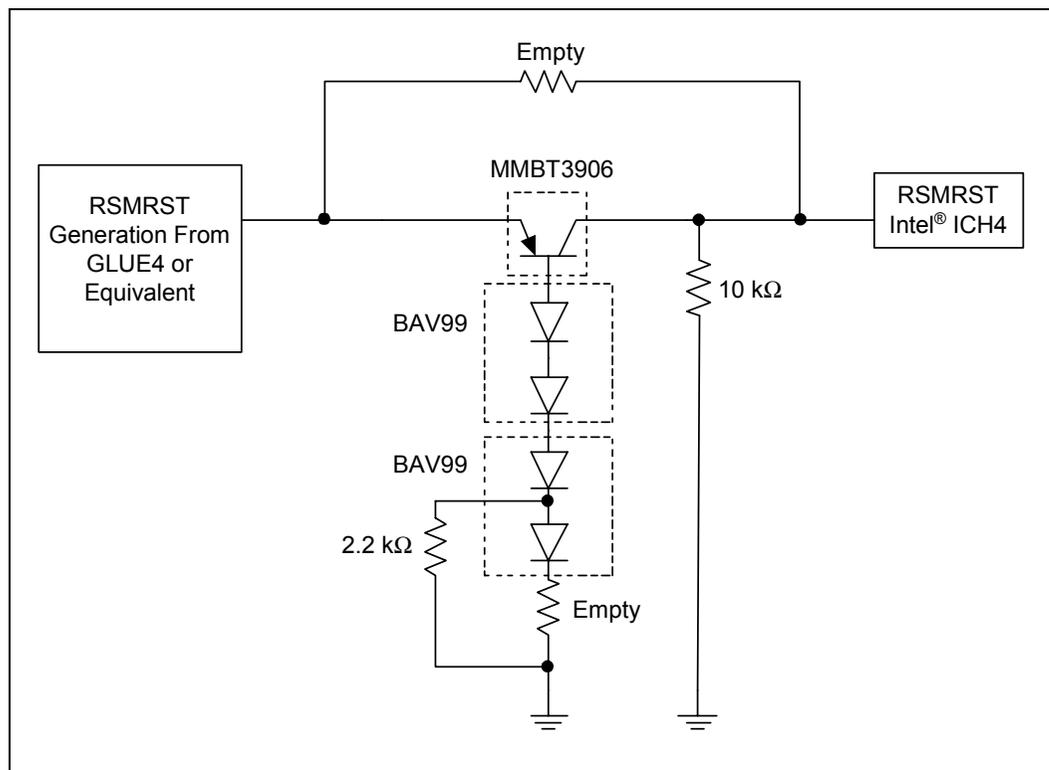
10.7 General Purpose I/O

10.7.1 GPIO Summary

The ICH4 has 12 general purpose inputs, 8 general purpose outputs, and 16 general purpose inputs/outputs. Some of these general purpose inputs and outputs have native functions assigned to them.

Table 10-26. GPIO Summary (Sheet 1 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
0	Yes[2]	Core	Input	5 V
1	Yes[2]	Core	Input	5 V
2	Yes[2]	Core	Input	5 V
3	Yes[2]	Core	Input	5 V
4	Yes[2]	Core	Input	5 V
5	Yes[2]	Core	Input	5 V
6	Yes	Core	Input	5 V
7	Yes	Core	Input	5 V
8	Yes	Resume	Input	3.3 V
9	Yes	Resume	Input	3.3 V
10	Yes	Resume	Input	3.3 V
11	Yes[2]	Resume	Input	3.3 V
12	Yes	Resume	Input	3.3 V
13	Yes	Resume	Input	3.3 V
14	Yes	Resume	Output	3.3 V
15	Yes	Resume	Output	3.3 V
16	Yes[2]	Core	Output	3.3 V
17	Yes[2]	Core	Output	3.3 V
18	Yes	Core	Output	3.3 V
19	Yes	Core	Output	3.3 V
20	Yes	Core	Output	3.3 V
21	Yes	Core	Output	3.3 V
22	Yes	Core	Output open drain	3.3 V
23	Yes	Core	Output	3.3 V
24	Yes	Resume	Input-Output[1]	3.3 V
25	Yes	Resume	Input-Output[1]	3.3 V
26	Yes	Resume	Input-Output[1]	3.3 V
27	Yes	Resume	Input-Output[1]	3.3 V
28	Yes	Resume	Input-Output[1]	3.3 V
29	Yes	Resume	Input-Output[1]	3.3 V
30	Yes	Resume	Input-Output[1]	3.3 V
31	Yes	Resume	Input-Output[1]	3.3 V
32	Yes	Core	Input-Output[1]	3.3 V

Table 10-26. GPIO Summary (Sheet 2 of 2)

GPIO#	Available	Power Well	Input/Output/ Input-Output	Tolerance
33	Yes	Core	Input-Output[1]	3.3 V
34	Yes	Core	Input-Output[1]	3.3 V
35	Yes	Core	Input-Output[1]	3.3 V
36	Yes	Core	Input-Output[1]	3.3 V
37	Yes	Core	Input-Output[1]	3.3 V
38	Yes	Core	Input-Output[1]	3.3 V
39	Yes	Core	Input-Output[1]	3.3 V
40	Yes	Core	Input-Output[1]	3.3 V
41	Yes	Core	Input-Output[1]	3.3 V
42	Yes	Core	Input-Output[1]	3.3 V
43	Yes	Core	Input-Output[1]	3.3 V

NOTES:
1. Defaults as an Output to the ICH4.
2. Can be used as GPIO if the native function is not needed. ICH4 defaults these signals to native functionality.

10.8 System Design Considerations

10.8.1 Power Delivery

Table 10-27. Power Delivery Terminology

Term	Description
Suspend-To-RAM (STR)	In the STR state, the system state is stored in main memory and all unnecessary system logic is turned off. Only main memory and logic required to wake the system remain powered. This state is used in the Customer Reference Board to satisfy the S3 ACPI power management state.
Full-power Operation	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (CPU stop-grant state) state.
Suspend Operation	During suspend operation, power is removed from some components on the motherboard. The customer reference board supports two suspend states: Suspend-to-RAM (S3), and Soft-off (S5).
Power Rails	An ATX power supply has 6 power rails: +5 V, –5 V, +12 V, –12 V, +3.3 V, and 5 VSB. In addition to these power rails, several other power rails are created with voltage regulators on the Intel® ICH4 Chipset Reference Board.
Core power rail	A power rail that is on only during full-power operation. These power rails are on when the PSON signal is asserted to the ATX power supply. The core power rails that are distributed directly from the ATX power supply are: ± 5 V, ± 12 V, and + 3.3 V.
Standby Power Rail	A power rail that is on during suspend operation (these rails are also on during full-power operation). These rails are on at all times (when the power supply is plugged into AC power). The only standby power rail that is distributed directly from the ATX power supply is 5 VSB (5 V Standby). There are other standby rails that are created with voltage regulators on the motherboard.
Derived Power Rail	A derived power rail is a power rail that is generated from another power rail using an on-board voltage regulator. For example, 3.3 VSB is usually derived (on the motherboard) from 5 VSB using a voltage regulator.
Dual Power Rail	A dual power rail is derived from different rails at different times (depending on the power state of the system). Usually, a dual power rail is derived from a standby supply during suspend operation, and from a core supply during full-power operation. Note that the voltage on a dual power rail may be misleading.

10.8.1.1 Intel® ICH4 Reference Board Power Delivery

Figure 10-49. Intel® ICH4 Platform Power Delivery Example
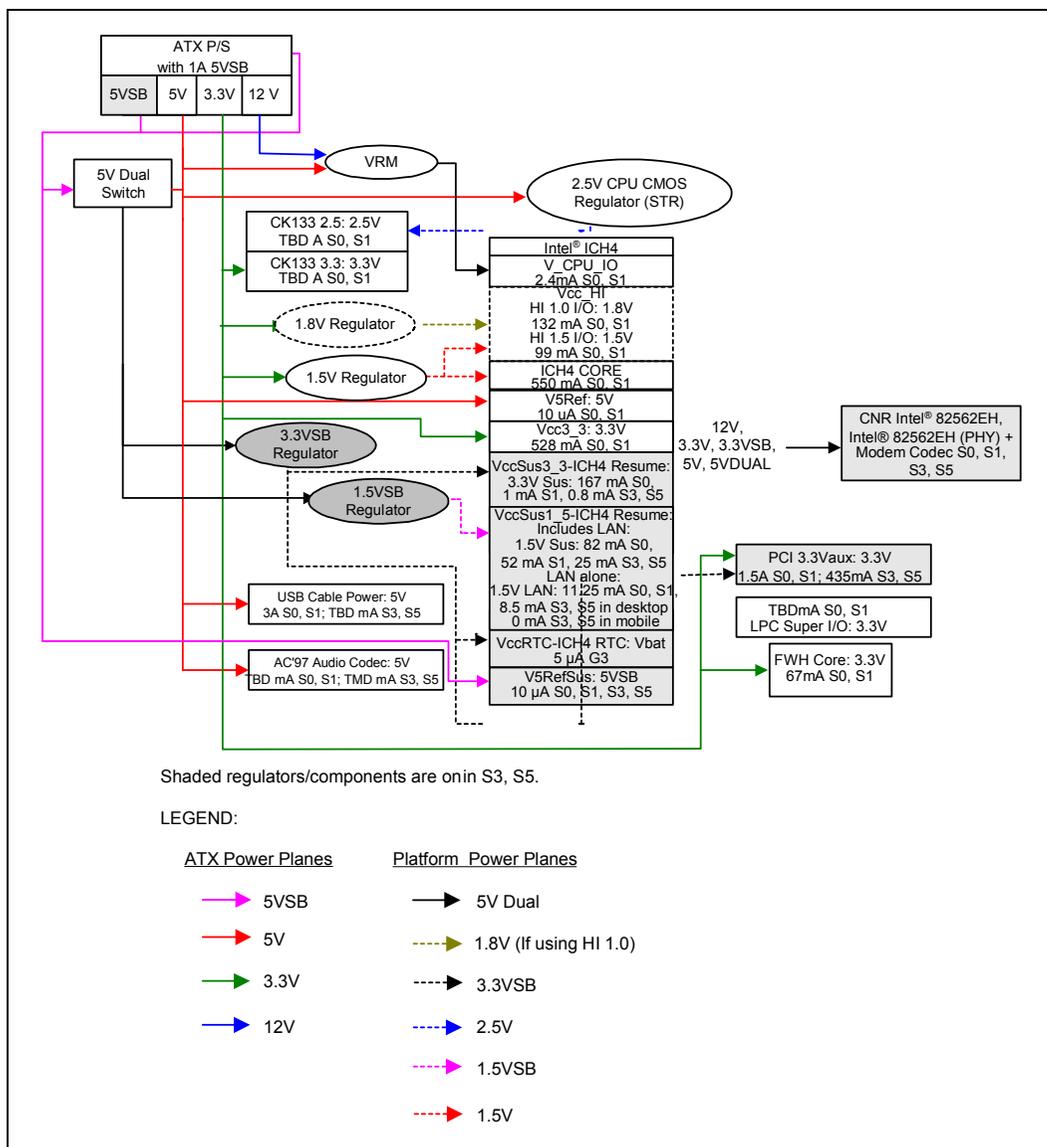
Figure 10-49 shows the suggested power delivery architecture for the ICH4 chipset. This power delivery architecture supports the "Instantly Available PC Design Guidelines" via the suspend-to-RAM (STR) state. During STR, only the necessary devices are powered. These devices include main memory, the ICH4 resume well, PCI wake devices (via 3.3 Vaux), and USB (USB can be powered only if sufficient standby power is available). To ensure that enough power is available during STR, a thorough power budget must be completed. The power requirements must include each device's power requirements, both in suspend and in full-power. The power requirements must be compared against the power budget supplied by the power supply. Because of the requirements of main memory and PCI 3.3 Vaux (and possibly other devices in the system), it is necessary to create a dual power rail.

The models given in this Design Guide are only examples. There are many power distribution methods that achieve similar results. It is critical when deviating from these examples in any way to consider the effect of the change.

In addition to the power planes provided by the ATX power supply, an instantly available ICH4 chipset-based system (using Suspend-to-RAM) requires 7 power planes to be generated on the board. The requirements for each power plane are described in this section. In addition to on-board voltage regulators, the ICH4 Chipset Reference Board has a 5 V Dual Switch.

5 V Dual Switch

This switch powers the 5 V Dual plane from the 5 V core ATX supply during full-power operation. During Suspend-to-RAM the 5 V Dual plane is powered from the 5 V Standby power supply. Note that the voltage on the 5 V Dual plane is not 5 V. There is a resistive drop through the 5 V Dual Switch that must be considered. Therefore, **no components** should be connected directly to the 5 V Dual plane. On the ICH4 Reference Board, the only devices connected to the 5 V Dual plane are voltage regulators (to regulate to lower voltages).

Note: This switch is not required in an ICH4 chipset-based system that does not support Suspend-to-RAM (STR).

1.8 V

The 1.8 V plane powers the ICH4 Hub Interface 1.0 I/O buffers. If using Hub Interface 1.5, the Hub Interface power signals should be connected to 1.5 V.

Note: This regulator is not required in all designs

1. 5 V

The 1.5 V plane powers the ICH4 hub interface 1.5 I/O buffers, as well as other components. For ICH4 power requirements for this rail, see Table 10-28. For decoupling considerations, see Section 10.8.1.5.

Note: This regulator is required in all designs.

3.3 VSB

The 3.3 VSB plane powers the I/O buffers in the resume well of the ICH4 and the PCI 3.3 Vaux suspend power pins. The 3.3 Vaux requirement states that during suspend, the system must deliver 375 mA to each wake-enabled card, and 20 mA to each non wake-enabled card. During full-power operation, the system must be able to supply 375 mA to EACH card. Therefore, the total current requirement is:

Full-power Operation: 375 mA * number of PCI slots
Suspend Operation: 375+20 * (number of PCI slots - 1)

In addition to the PCI 3.3 Vaux, the ICH4 suspend well power requirements must be considered as shown in Figure 10-49.

Note: This regulator is required in all designs.

1.5 VSB

The 1.5 VSB plane powers the logic to the ICH4 resume well.

10.8.1.2   Power Supply PS_ON Consideration

If a pulse on SLP_S3# or SLP_S5# is short (~ 10-100 mS) such that PS_ON is driven active during the exponential decay of the power rails, a few power supply designs may not be designed to handle the short pulse condition. In this case, the power supply will not respond to this event and will never power back up. These power supplies would have to be unplugged and re-plugged to bring the system back up. Power supplies not designed to handle this condition must have their power rails decay to a certain voltage level before they can properly respond to PS_ON. This level varies with affected power supply.

The ATX spec does not specify a minimum pulse width on PS_ON de-assertion, which means power supplies must be able to handle any pulse width. This issue can affect any power supply (beyond ATX) with similar PS_ON circuitry. Because of variance in the decay of the core power rails per platform, a single board or chipset silicon fix would be non-deterministic (may not solve the issue in all cases).

The platform designer must ensure that the power supply used with the platform is not affected by this condition.

10.8.1.3   Intel® ICH4 Analog Power Delivery

There are no analog ICH4 circuits that require filters.

10.8.1.4   Intel® ICH4 Power Delivery

Figure 10-50. Intel® ICH4 Layer 1 Power Delivery
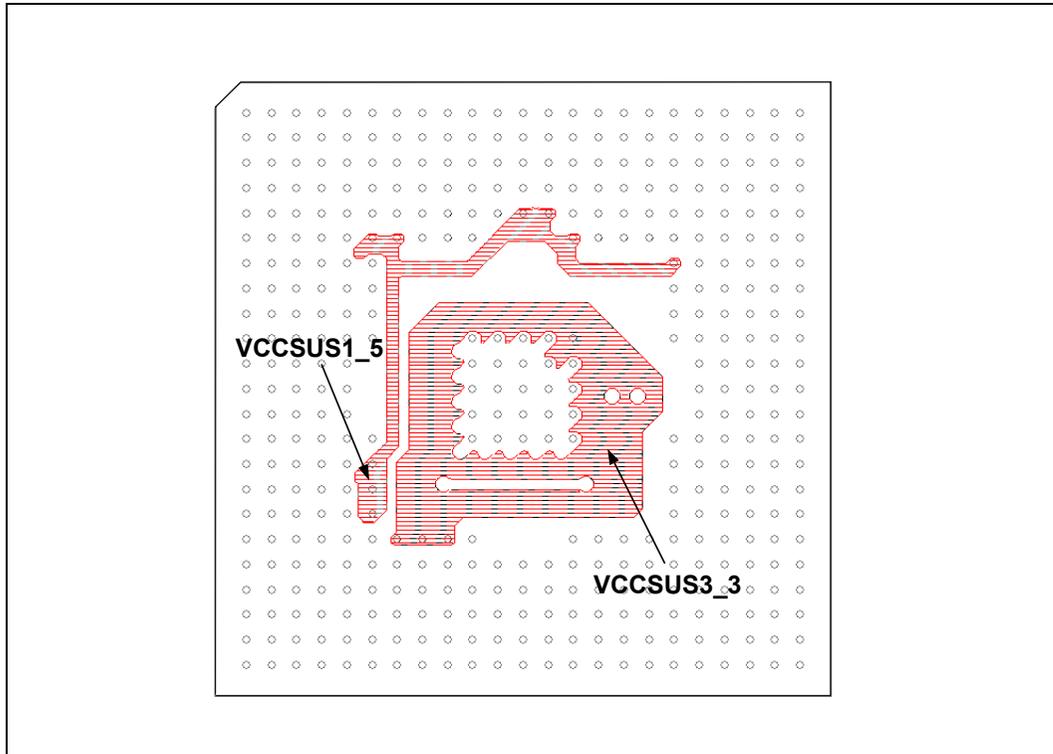
Figure 10-51. Intel® ICH4 Layer 3 Power Delivery
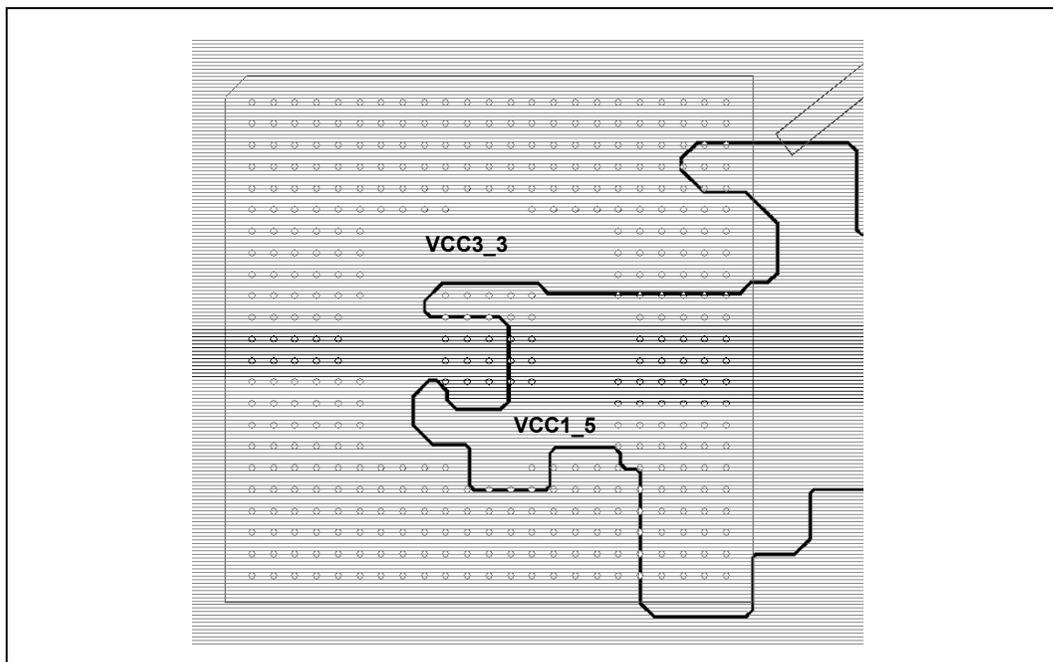
Figure 10-52. Intel® ICH4 Layer 4 Power Delivery
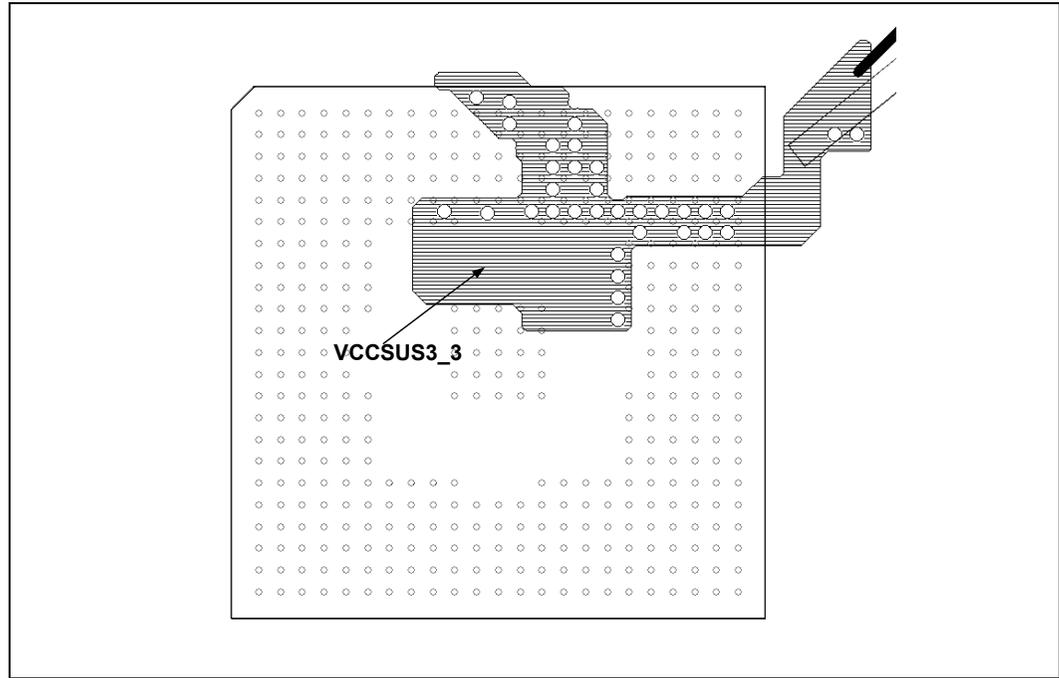
Figure 10-53. Intel® ICH4 Layer 6 Power Delivery
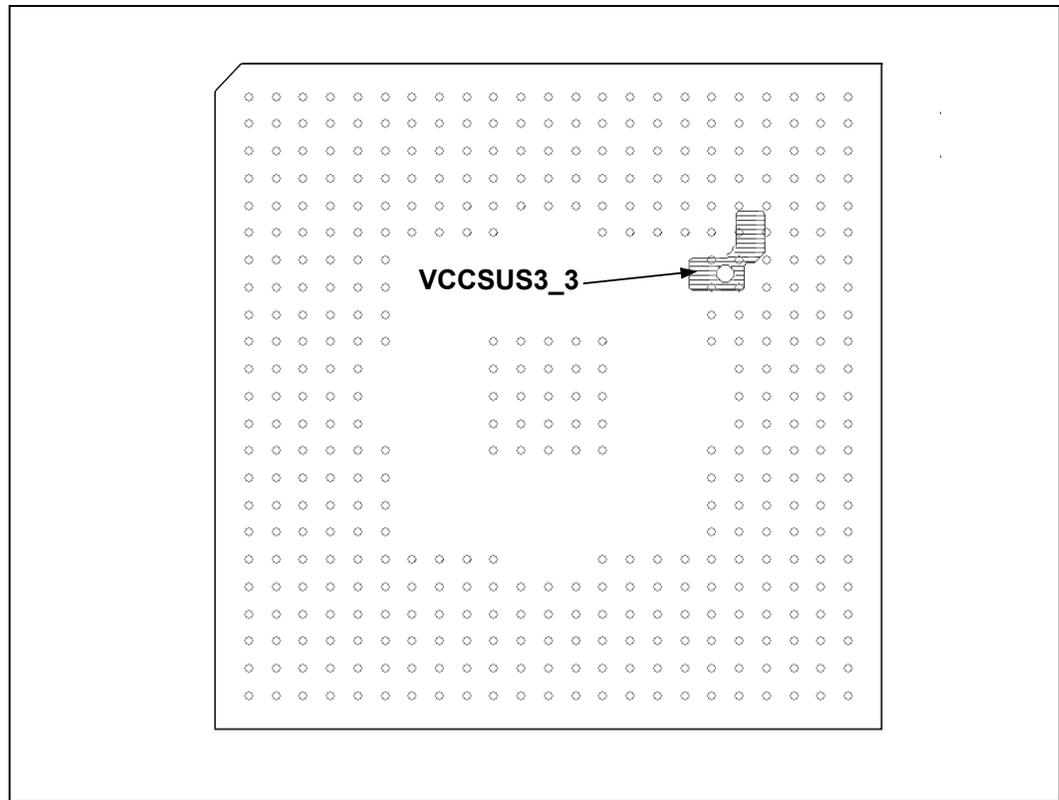
10.8.1.5   Intel® ICH4 Decoupling Recommendations

The ICH4 is capable of generating large current swings when switching between logic high and logic low. This condition can cause the component voltage rails to drop below specified limits. To avoid this, ensure that the appropriate amount of bulk capacitance is added in parallel to the voltage input pins. It is recommended that the developer use the amount of decoupling capacitors specified in Table 10-28 to ensure that the component maintains stable supply voltages. The capacitors should be placed as close to the package as possible (100 mils nominal). Rotate caps that are placed over power planes to minimize loop inductance. The basic theory for minimizing loop inductance is to consider which voltage is on layer two (power or ground), and spin the decoupling cap with the opposite voltage towards the BGA (Ball Grid Array). This greatly minimizes the total loop inductance. It is recommended that for prototype board designs the designer include pads for extra power plane decoupling caps.

Table 10-28. Decoupling Requirements for Intel® ICH4

Pin	Decoupling Requirements	Decoupling Type (Pin type)	Decoupling Placement
VCC3_3	(6) 0.1 μF	Decoupling Cap (VSS)	Place near balls: A4, A1, H1, T1, AC10, and AC18
VccSus3_3	(2) 0.1 μF	Decoupling Cap (VSS)	Place near balls: A22 and AC5
V_CPU_IO	(1) 0.1 μF	Decoupling Cap (VSS)	Place near ball: AA23
VC1_5	(2) 0.1 μF	Decoupling Cap (VSS)	Place near balls: K23 and C23
VccSus1_5	(2) 0.1 μF	Decoupling Cap (VSS)	Place near balls: A16 and AC1
V5REF	(1) 0.1 μF	Decoupling Cap (VSS)	Place near ball: E7
V5REF_Sus	(1) 0.1 μF	Decoupling Cap (VSS)	Place near ball: A16
VccRTC	(1) 0.1 μF	Decoupling Cap (VSS)	Place near ball: AB5
VCCHI	(2) 0.1 μF	Decoupling Cap (VSS)	Place near balls: T23 and N23
VCCPLL	(1) 0.1 μF and (1) 0.01 μF	Decoupling Cap (VSS)	Place near ball: C22

Figure 10-54. Intel® ICH4 Decoupling Capacitor Placement
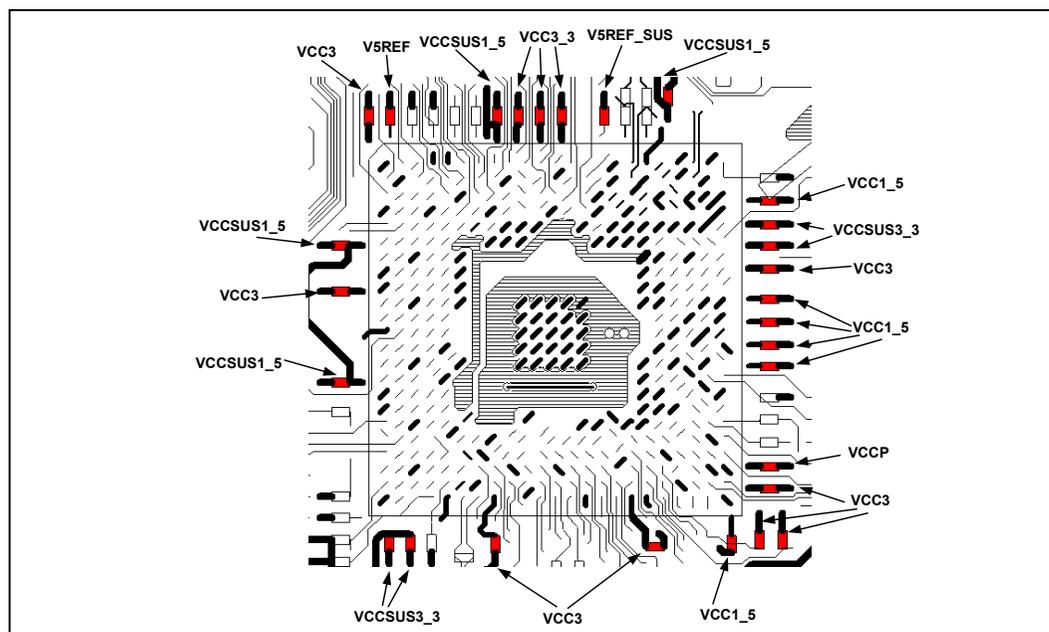
10.8.1.6 3.3 V/1.5 V and 3.3 V/1.8 V Power Sequencing

There are no power sequencing requirements for the associated 3.3 V/1.5 V rails or the 3.3 V/1.8 V rail of the ICH4. It is generally good design practice to core power up before or at the same time as the other rails.

10.8.1.7 V5REF/ 3.3 V Sequencing

V5REF is the reference voltage for 5 V tolerance on inputs to the ICH4. V5REF must be powered up before VCC3_3, or after VCC3_3 within 0.7 V. Also, V5REF must power down after VCC3_3, or before VCC3_3 within 0.7 V. This rule must be followed to ensure the safety of the ICH4. If the rule is violated, internal diodes will attempt to draw power sufficient to damage the diodes from the VCC3_3 rail. Figure 10-55 shows a sample implementation of how to satisfy the V5REF/VCC3_3 sequencing rule.

This rule also applies to the stand-by rails, but in most platforms the VccSus3_3 rail is derived from the VccSus5 rail. Therefore, the VccSus3_3 rail will always come up after the VccSus5 rail. As a result, V5REF_SUS will always be powered up before VccSus3_3. In platforms that do not derive the VccSus3_3 rail from the VccSus5 rail, this rule must be observed in the platform design.

Figure 10-55. Example V5REF / 3.3 V Sequencing Circuitry
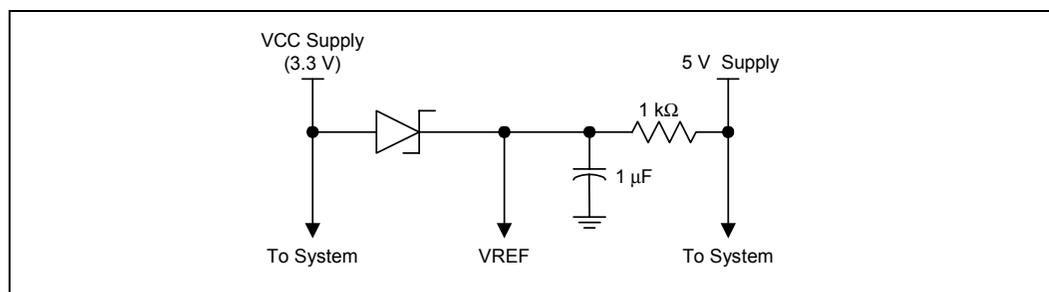
10.8.1.8 Intel® ICH4 Power Consumption Numbers

Table 10-29 describes ICH4 power consumption.

Table 10-29. Intel® ICH4 Power Consumption Measurements

Power Plane	Maximum Power Consumption				
	S0	S1	S3	S4/S5	G3
1.5 V Core	550 mA	266 mA	N/A	N/A	N/A
3.3 V I/O	528 mA	0.76 mA	N/A	N/A	N/A
1.5 V SUS	82 mA	52 mA	25 mA	25 mA	N/A
3.3 V SUS [1]	167 mA	1 mA	0.8 mA		N/A
VccRTC	N/A	N/A	N/A	N/A	5 μA
V_CPU_IO [2]	2.4 mA	2.4 mA	N/A	N/A	N/A
VCCHI [3] HI 1.0 (1.8 V) HI 1.5 (1.5 V)	 132 mA 99 mA	 132 mA 99 mA	 N/A N/A	 N/A N/A	 N/A N/A
V5REF	10 μA	10 μA	N/A	N/A	N/A
V5REF_SUS	10 μA	10 μA	10 μA	10 μA	10 μA

NOTES:
1. 3.3 V SUS S0 assumes maximum USB 2.0 traffic (6 ports populated).
2. V_CPU_IO S1 state primarily due to STPCLK# activity.
3. VCCHI power consumption is dependant on the Hub Interface being used

10.8.2 Thermal Design Power

The thermal design power is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the product. It does not represent the expected power generated by a power virus.

The ICH4 thermal design power consumption dissipation is estimated to be 2.9 Watts.

10.8.3 Glue Chip 4 (Intel® ICH4 Glue Chip)

To reduce the component count and BOM cost of the ICH4 platform, Intel has developed an ASIC component that integrates miscellaneous platform logic into a single chip. The ICH4 Glue Chip is designed to integrate the following functions into a single device. By integrating much of the required glue logic into a single device, overall board cost can be reduced.

Features

- Dual, Strapping, Selectable Feature Sets
- Audio-disable circuit
- Mute Audio Circuit
- 5 V reference generation
- 5 V standby reference generation
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK (PWRGD_3V) signal generation
- Power Sequencing / BACKFEED_CUT
- Power Supply turn on circuitry
- RSMRST# generation
- Voltage translation for DDC to VGA monitor
- HSYNC / VSYNC voltage translation to VGA monitor
- Tri-state buffers for test
- Extra GP Logic Gates
- Power LED Drivers
- Flash FLUSH# / INIT# circuit

More information regarding this component is available from the following vendors:

Vendor	Contact Information
Philips Semiconductors	6028 44th Way NE Olympia, WA 98516-2477 Phone: (360) 413-6900 Fax: (360) 438-3606
Fujitsu Microelectronics	3545 North 1st Street, M/S 104 San Jose, CA 95134-1804 Phone: 1-800-866-8600 Fax: 1-408-922-9179

NOTE: These vendors are listed by Intel as a convenience to Intel's general customer base, but Intel does not make any representations or warranties whatsoever regarding quality, reliability, functionality, or compatibility of these devices. This list and/or these devices may be subject to change without notice.

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Debug Port 11

Refer to *ITP700 Debug Port Design Guide* for all information necessary to develop a Debug Port on this platform including electrical specifications, mechanical requirements, and all In-Target Probe (ITP) signal layout guidelines.

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Power Distribution Guidelines **12**

Table 12-1. Power Delivery Terminology

Term	Definition
Full-Power	During full-power operation, all components on the motherboard remain powered. Note that full-power operation includes both the full-on operating state, and the S1 (processor stop-grant) state.
Power Rails	A power supply has five power rails: +12 V, –12 V, +5 V, +3.3 V, +5VSB. In addition to these power rails coming off the power supply, several other power rails are created by voltage regulators on the E7205 chipset Reference Board.
Core Power	A power rail that is only on during full-power operation. These power rails are on when rail the active-low PSON signal is asserted to the power supply. The core power rails that are distributed directly from the power supply are: +12 V, –12 V, +5 V, and +3.3 V.
Standby Power Rail	Standby power is supplied by the power supply during times when the system is powered down. The purpose is to maintain functions that must always be enabled, such as the date and time-of-day within the BIOS. A 5VSB power rail is provided by the power supply.
Derived Power	A derived power rail is any power rail generated from another power rail using a Rail on-board voltage regulator. For example, +2.5 V is derived from a +5 V power rail using a voltage regulator.

12.1 Customer Reference Board Power Delivery

Figure 12-1 shows the power delivery architecture for the Customer Reference Board.

Figure 12-1. Intel® E7205 Chipset Power Delivery Example
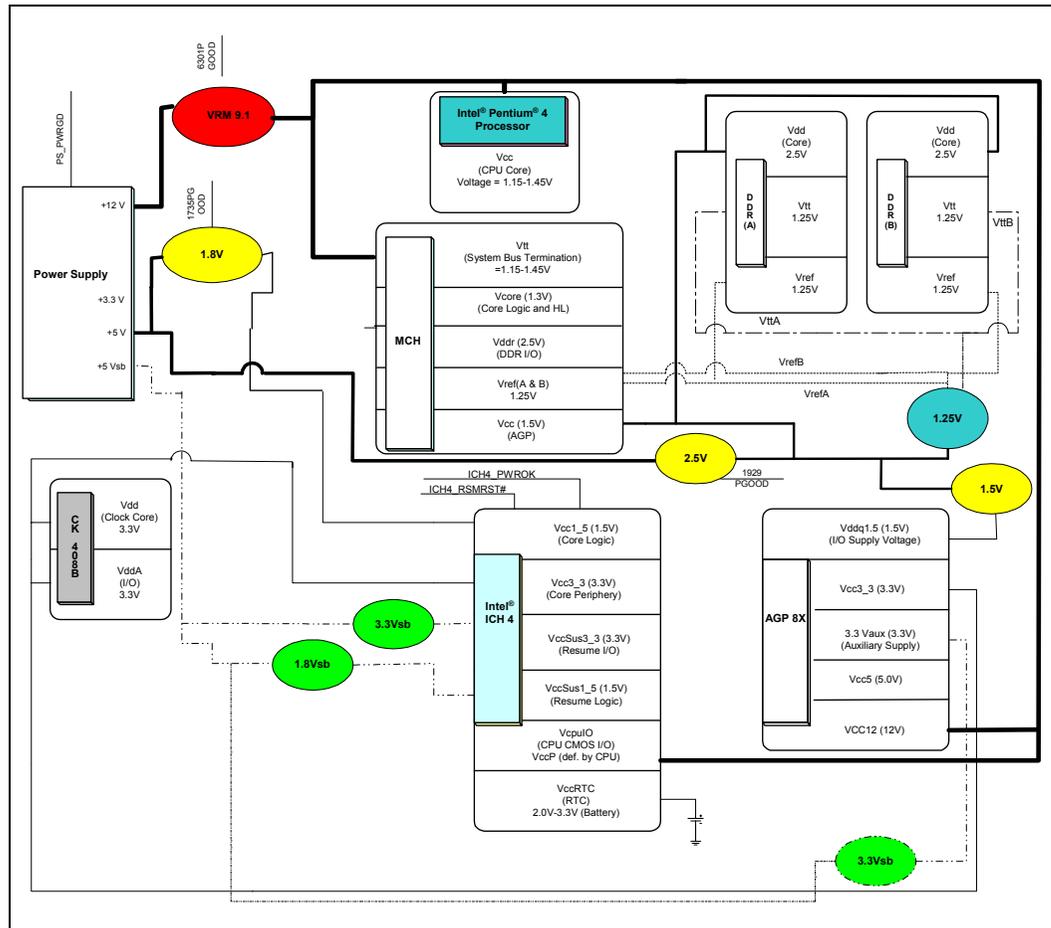
NOTE: The examples given in this Design Guide are only examples. Many power distribution methods achieve similar results. It is critical, when deviating from these examples in any way to consider the effects of the change.

12.1.1 Voltage Rail and Max Current Specifications

12.1.1.1 Processor VID

The processor core voltage power plane is used to power the processors. The core voltage operates between 1.3 V and 1.5 V. The VRM or VRD equivalent will be a VRM 9.1 design. Refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*. A VRM 9.1 compatible design is required for all E7205 chipset platforms.

12.1.1.2 2.5 V

The 2.5 V power plane is used to power the DDR DRAM core, the MCH DDR I/O ring, and the 2.5 V-to-1.25 V switching regulator. The 2.5 V power plane is created using a switching regulator, which should be able to support the specification listed in Table 12-2. This switching regulator receives its input directly from the 5 V power rail of the power supply. Refer to the DRAM specification for vendor specific maximum current.

12.1.1.3 1.5 V

The 1.5 V power plane powers the AGP 8X component and the AGP 8X interface located on the MCH. Refer to Table 12-2 for details.

12.1.1.4 1.25 V

The voltage regulator produces two 1.25 V rails. One is for VREF, and the other is for V_{TERM}. The switching regulator divides the 2.5 V power rail by two to drive 1.25 V reference voltage. This provides some common mode noise rejection between the DDR termination and I/O voltages. Because of power sequencing requirements, the 1.25 V power rail must be derived by the 2.5 V regulator. Refer to Table 12-2 for details.

12.1.1.5 1.8 V

The 1.8 V power plane is created using a switching regulator that sources from the 5 V power rail on the power supply. The 1.8 V plane powers the ICH4 core logic. Refer to Table 12-2 for maximum current specification.

12.1.1.6 1.3 V

The 1.3 V power plane powers the MCH core logic. Refer to Table 12-2 for maximum current specification.

12.1.1.7 5 VSB

The 5 VSB power plane comes directly from the 5 VSB power rail and has two functions: to provide power to resume functions in I/O devices off of the ICH4, and to provide 1.8 VSB power through a linear regulator. Refer to Table 12-2 for maximum current specification.

12.1.1.8   3.3 VSB

The 3.3 VSB power plane is the output of a 5 VSB-to-3.3 VSB voltage regulator. The power plane is used solely for the resume I/O features of the ICH4. Refer to Table 12-2 for maximum current specification.

12.1.1.9   1.8 VSB

As already stated, the 1.8 VSB provides power to the resume logic within the ICH4. Refer to Table 12-2 for maximum current specification.

Table 12-2. Platform Component Max Current Specifications

Platform Component	Voltage Rail (V) / Max Current Specification (A)					
	1.3	1.25	1.4	1.5	2.5	3.3
MCH	3.20		2.10	0.6	6.80	–
Intel® ICH4	–	–	–	0.97	–	0.61
DDR	–	6.20	–	–	21.00	
CK 408	–	–	–	–	–	0.36
Rail Totals (A)	3.20	6.20	2.10	1.03	26.80	0.97

12.2   Power Requirements

Intel recommends using an *Intel® Pentium® 4 Processor VR-Down Design Guidelines*-compliant regulator for the processor system board designs. An *Intel® Pentium® 4 Processor VR-Down Design Guidelines*-compliant regulator may be integrated as part of the system board or on a module. The system board designer should properly place high-frequency and bulk-decoupling capacitors as needed between the voltage regulator and the processor to ensure voltage fluctuations remain within the specifications in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. See Table 12-3 for recommendations on the amount of decoupling needed.

Specifications for the processor voltage are contained in the *Intel® Pentium® 4 Processor in the 478 Pin Package Datasheet*. These specifications are for the processor die. For guidance on correlating the die specifications to socket level measurements, refer to the *Intel® Pentium® 4 Processor VR-Down Design Guidelines*.

The voltage tolerance of the loadlines contained in these documents help the system designer achieve a flexible motherboard design solution for all frequencies of the processor. Failure to meet the load line requirements when modeling the system power delivery may result in a system that is not upgradeable.

The processor requires local regulation because of its higher current requirements, and to maintain power supply tolerance. For example, an on-board DC-to-DC converter converts a higher DC voltage to a lower level using a switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R). More important however, an on-board regulator regulates the voltage locally, which minimizes DC line losses by reducing motherboard resistance on the processor voltage. Figure 12-2 shows an example of the placement of the local voltage regulation circuitry.

In this section, North and South are used to describe a specific side of the socket based on the placement of the customer reference board shown in Figure 3-1. North refers to the side of the processor closest to the back panel, and South refers to the side of the processor closest to the system memory.

Figure 12-2. VR Component Placement
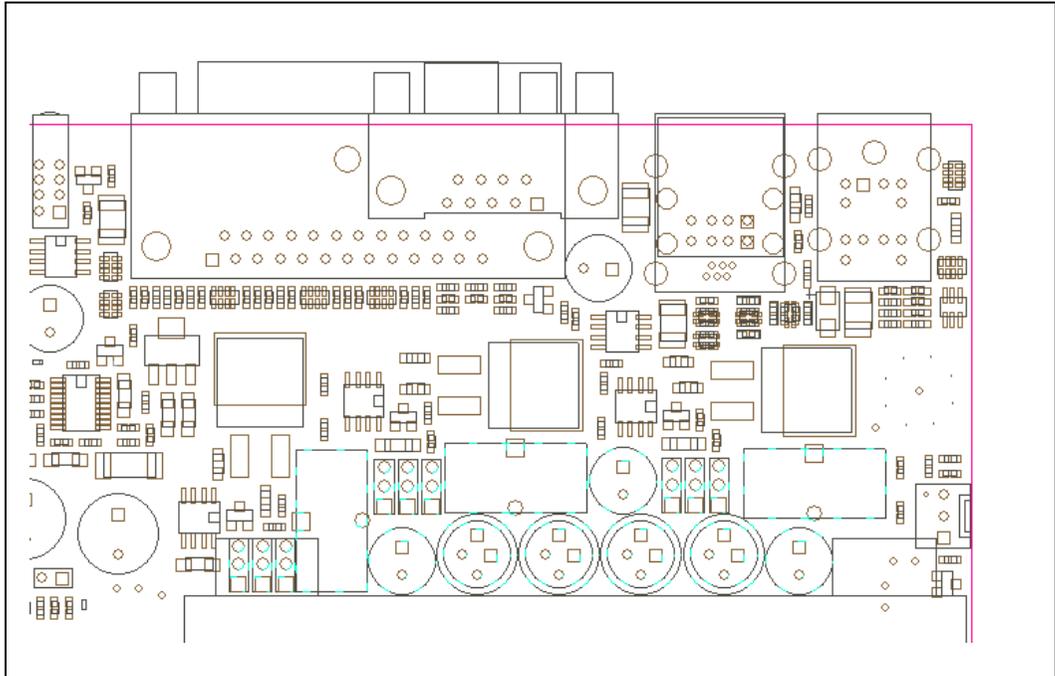
12.3 Decoupling Requirements

For the processor voltage regulator circuitry to meet the transient specifications of the processor, proper bulk and high-frequency decoupling is required. The decoupling requirements for the processor power delivery in this case are shown in Table 12-3.

Table 12-3. Decoupling Requirements

Capacitance	ESR (each)	ESL (each)	Ripple Current Rating (each)	Notes
11 OS-CONs*, 560 µF	9 mΩ, max	4 nH, max	4.080 A$_{rms}$	1
38 1206 package, 10 µF	3.97 mΩ, typ	880 pH, typ		1

NOTE:
 1. The ESR, ESL, and ripple current values in this table are based on the values used in power delivery simulation by Intel, and are not vendor specifications.

The decoupling should be placed as close as possible to the processor power pins. Table 12-4 and Figure 12-3 illustrate the recommended placement.

Table 12-4. Decoupling Locations

Type	Number	Location
560 µF OS-CONs*	6	North side of the processor as close as possible to the keep-out area for the retention mechanism
560 µF OS-CONs*	5	South side of the processor as close as possible to the keep-out area for the retention mechanism
1206 package, 10 µF	14	North side of the processor as close as possible to the processor socket
1206 package, 10 µF	10	Inside the processor socket cavity
1206 package, 10 µF	14	South side of the processor as close as possible to the processor socket

Figure 12-3. Processor Decoupling Placement

intel®
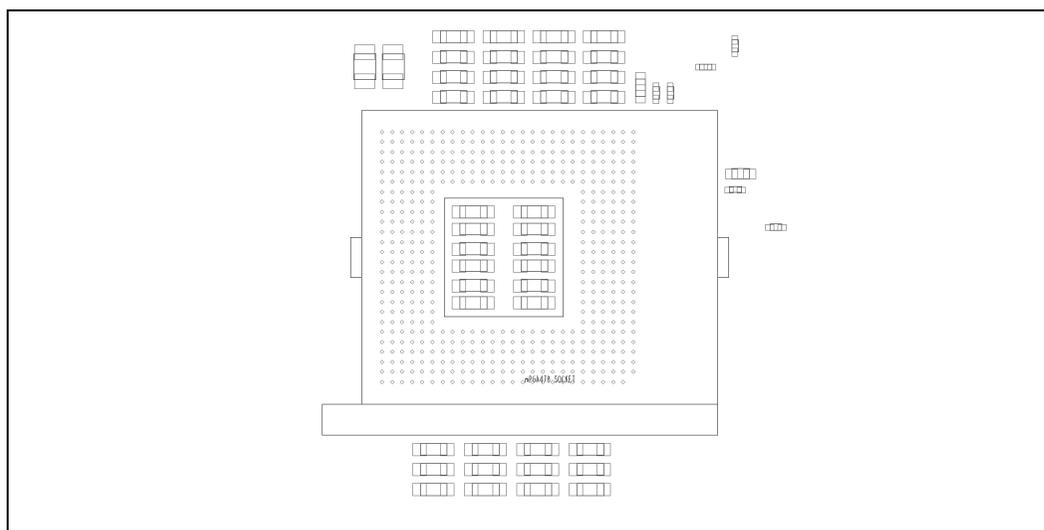
12.4   Layout

All six layers in the processor area should be used for power delivery. Four layers should be used for VCC_CPU, and two layers should be used for ground. Traces are not sufficient for supplying power to the processor because of the high current and low resistance required to meet the processor voltage specifications. To satisfy these requirements, shapes that encompasses the power delivery part of the processor pin field are required. Figure 12-4 through Figure 12-6 show examples of how to use shapes to deliver power to the processor.

Figure 12-4. Top Layer Plane
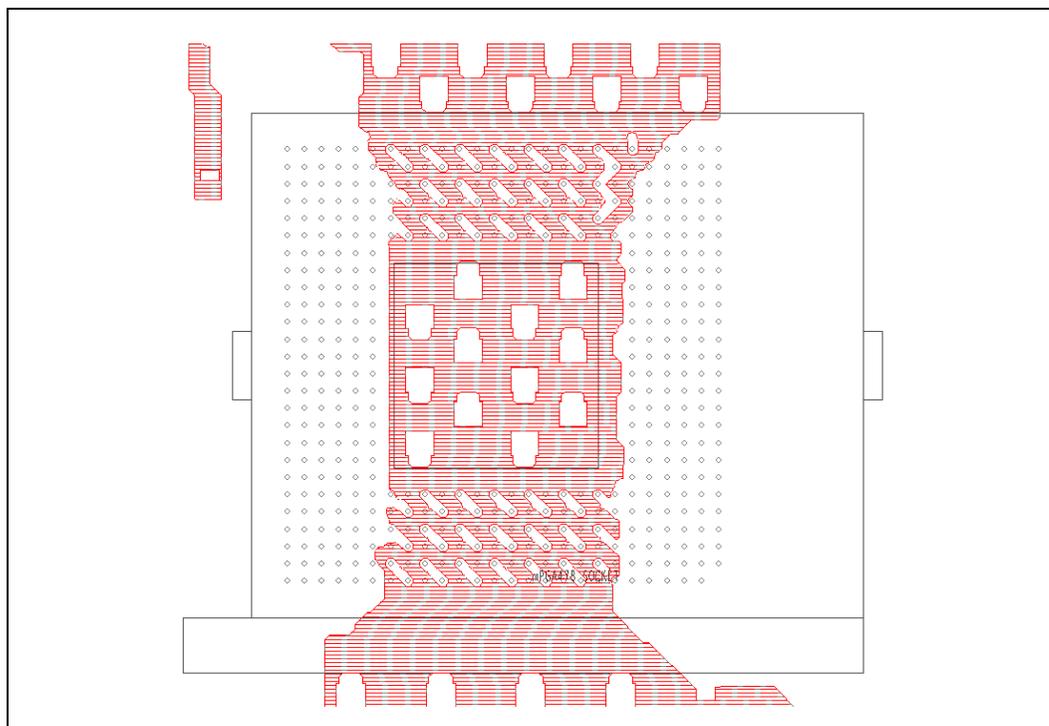
Figure 12-5. Layer 3 Plane
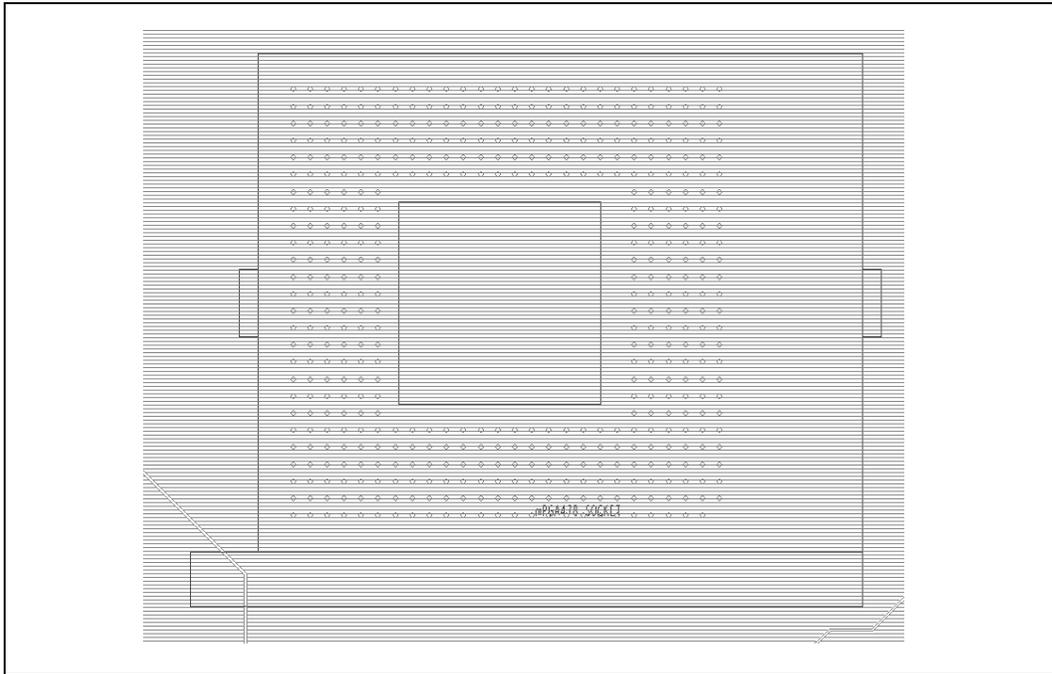
Figure 12-6. Bottom Layer Plane

Intel® Pentium® 4 Processor and Intel® E7205 Chipset Platform Design Guide
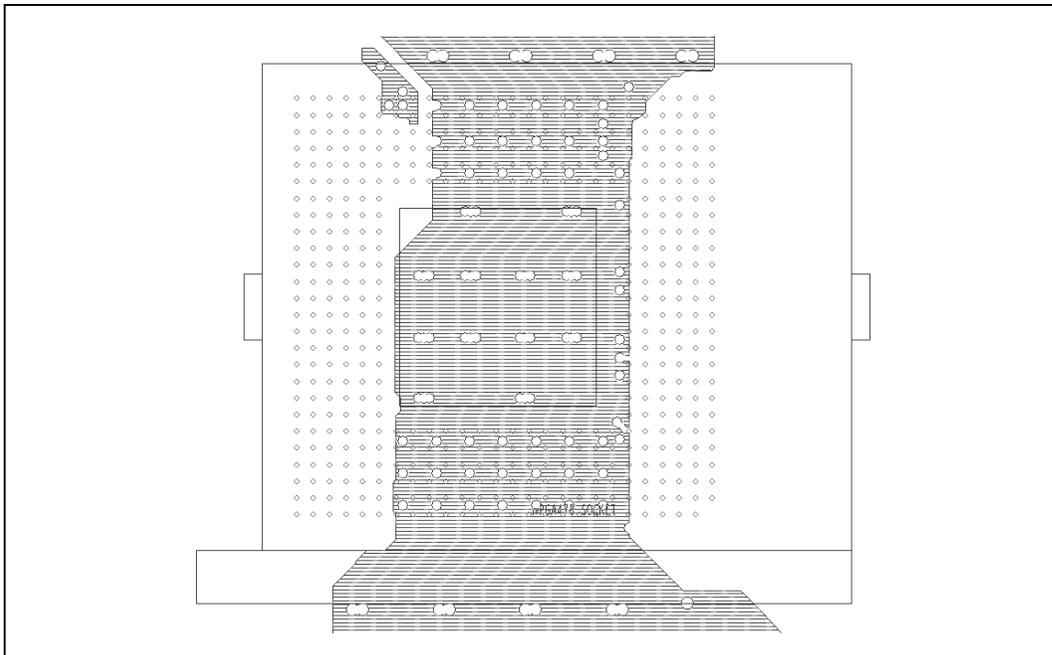
The high-frequency decoupling capacitors should be placed with alternating VCC_CPU and VSS to provide a better path for power delivery through the capacitor field. An example of this placement is shown in Figure 12-7.

Figure 12-7. Alternating VCC_CPU/VSS Capacitor Placement
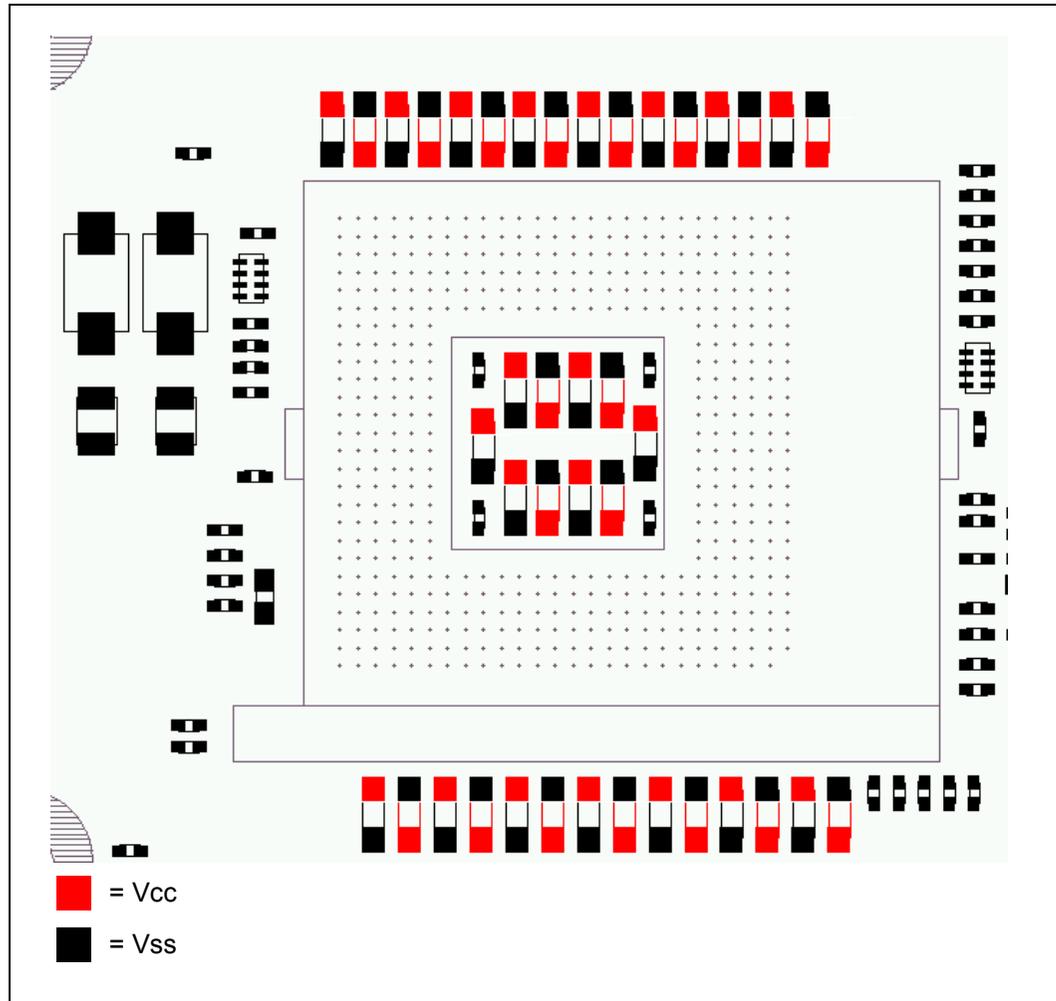
The processor socket has 478 pins with 50-mil pitch. The routing of the signals, power and ground pins will require creation of many vias. These vias cut up the power and ground planes beneath the processor resulting in increased inductance of these planes. To provide the best path through the via field, it is recommended that vias be shared for every two processor ground pins and for every two processor power pins. Figure 12-8 illustrates this via sharing.

Figure 12-8. Shared Power and Ground Vias
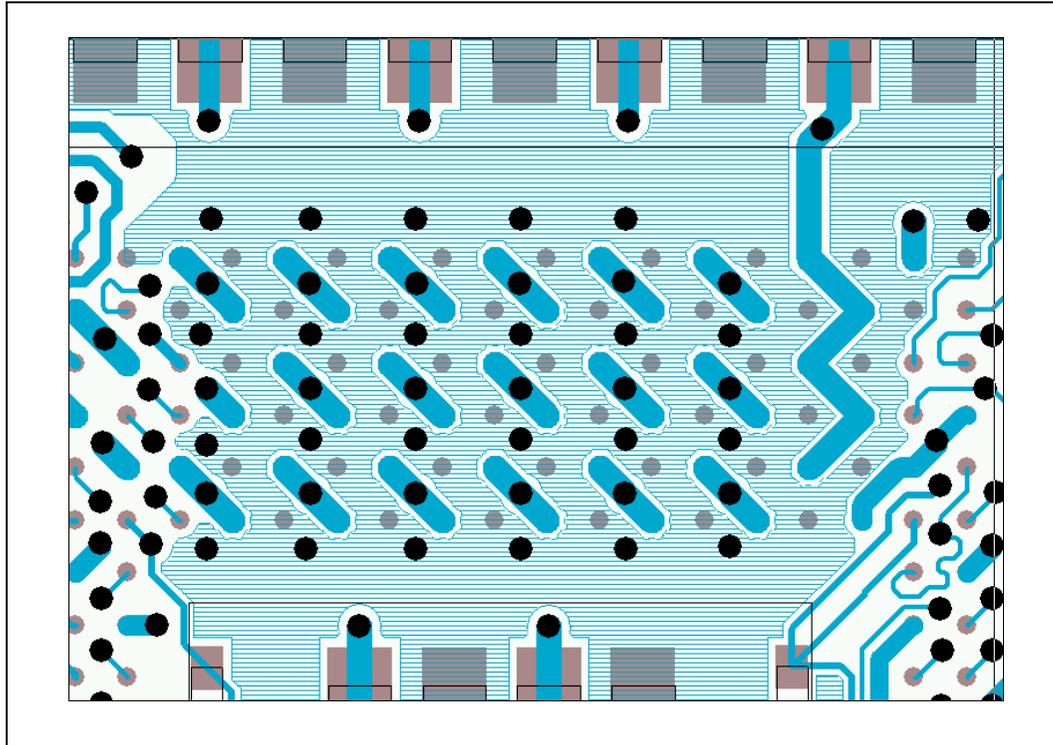
The switching voltage regulators typically used for processor power delivery require the use of a feedback signal for output error correction. The VCC_SENSE and VSS_SENSE pins on the processor should not be used for generating this feedback. These pins should be used as measurement points for lab measurements only. They can be routed to a test point or via on the back of the motherboard with a trace that is a maximum length of 100 mils for this purpose. The socket loadline defined in the *Intel® Pentium® 4 Processor in the 478 Pin Package VR Down Design Guidelines* is defined from pins AC14 (VCC_CPU) and AC15 (VSS), and should be validated from these pins. These pins are located approximately in the center of the pin field on the North side of the processor. Feedback for the voltage regulator controller should therefore be taken close to this area of the power delivery shape. Figure 12-9 shows an example routing of the feedback signal. It is routed as a trace from the 1206 capacitor in the Northwest corner of the processor back to the voltage regulator controller. Because the feedback in this case is not taken from the exact point that defines the socket loadline (pins AC14/AC15), it is important to consider any voltage drop from the feedback point to these pins in the design.

Figure 12-9. Routing of VR Feedback Signal
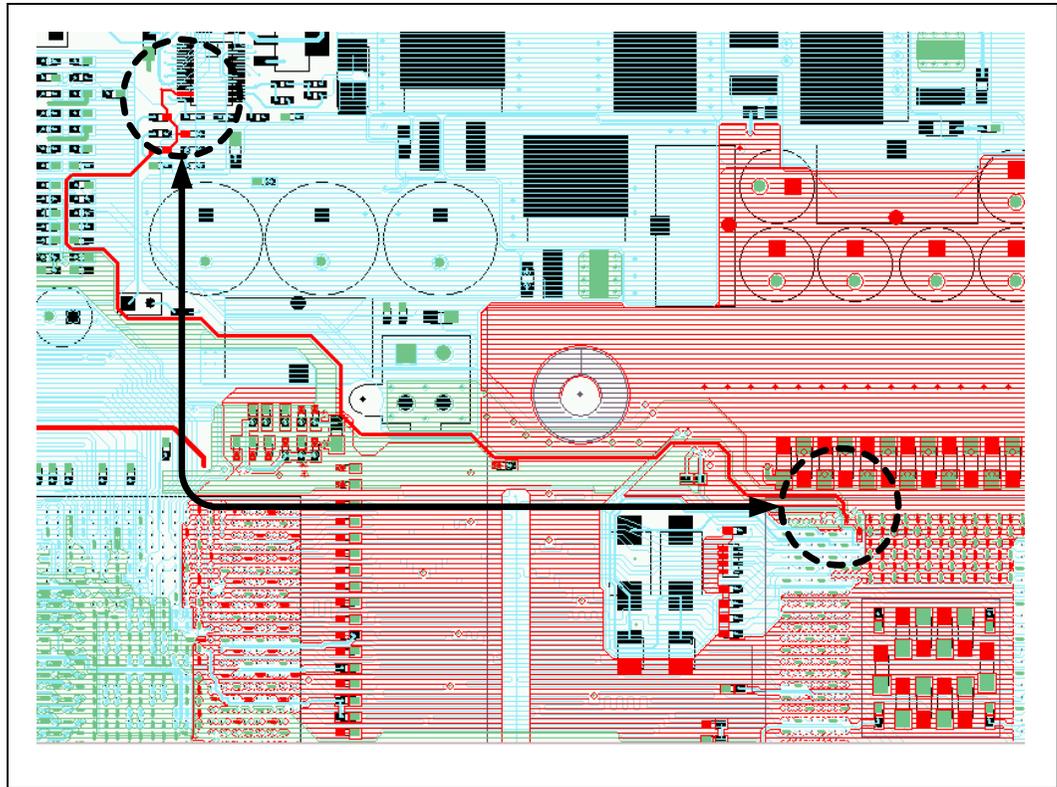
12.5 Thermal Considerations

For a power delivery solution to meet the flexible motherboard (FMB) requirements, it must be able to deliver a fairly high amount of current. This high amount of current also requires that the solution be able to dissipate the associated heat generated by the components and keep all of the components and the PCB within their thermal specifications. OEMs should evaluate their component configurations, system airflow, and layout to ensure adequate thermal performance of the processor power delivery solution.

12.5.1 Simulation

To completely model the system board, one must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins, body of components (such as resistors and capacitors), processor socket, and the voltage regulator module. More detailed models showing these effects are shown in Figure 12-10.

Figure 12-10. Detailed Power Distribution Model for Processor with Voltage Regulator on System Board
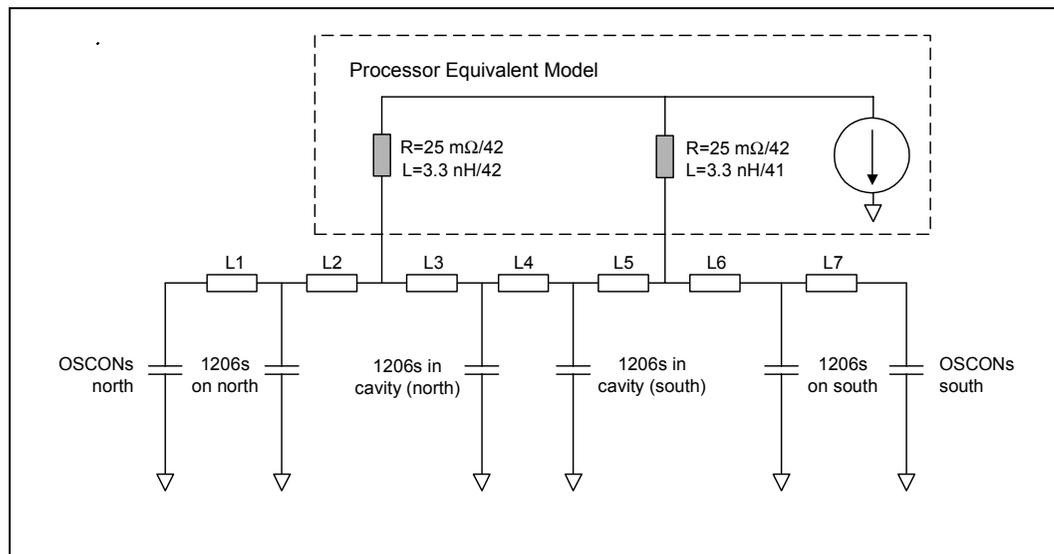
Table 12-5 lists model parameters for the system board shown in Figure 12-10.

Table 12-5. Intel® Pentium® 4 Processor Power Delivery Model Parameters

Segment	Resistance
L1	0.22 mΩ
L2	0.283 mΩ
L3	0.283 mΩ
L4	0.144 mΩ
L5	0.283 mΩ
L6	0.375 mΩ
L7	

12.6 Filter Specifications for VCCA, VCCIOPLL, and VSSA

VCCA and VCCIOPLL are power sources required by the PLL clock generators on the processor silicon. Since these PLLs are analog in nature, they require quiet power supplies for minimum jitter. Jitter is detrimental to the system—it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). To prevent this degradation, these supplies must be low pass filtered from VCC. The general desired filter topology is shown in Figure 12-11. Not shown in the core is parasitic routing. Excluded from the external circuitry are parasitics associated with each component.

Figure 12-11. Typical VCCIOPLL, VCCA, and VSSA Power Distribution
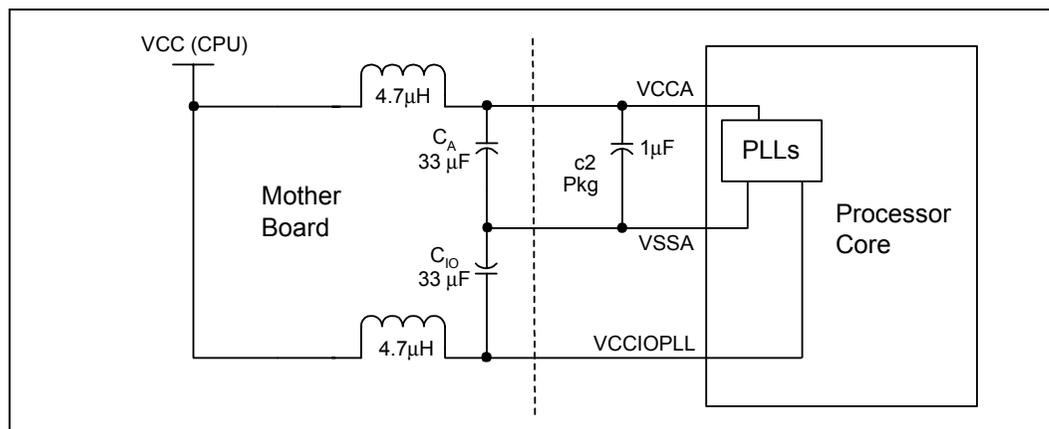
The function of the filter is two-fold. It protects the PLL from external noise through low-pass attenuation. It also protects the PLL from internal noise through high-pass filtering. In general, the low-pass description forms an adequate description for the filter. For simplicity, this document addresses the recommendation for the VCCA filter design. The same characteristics and design approach is applicable for the VCCIOPLL filter design.

Note: The 1 µF package capacitor shown in Figure 12-11 does not exist on the Pentium 4 processors in the 478- pin package. It is present for the Pentium 4 processors with 512-KB L2 cache on 0.13 micron process only.

The AC low-pass recommendation, with input at VCC and output measured across the capacitor (C_A or C_{IO} in Figure 12-11), is as follows:

> < 0.2 dB gain in pass band
>
> < 0.5 dB attenuation in pass band < 1 Hz (see DC drop in next set of requirements)
>
> > 34 dB attenuation from 1 MHz to 66 MHz
>
> > 28 dB attenuation from 66 MHz to core frequency

The filter recommendation (AC) is graphically shown in Figure 12-12.

Figure 12-12. Filter Recommendation
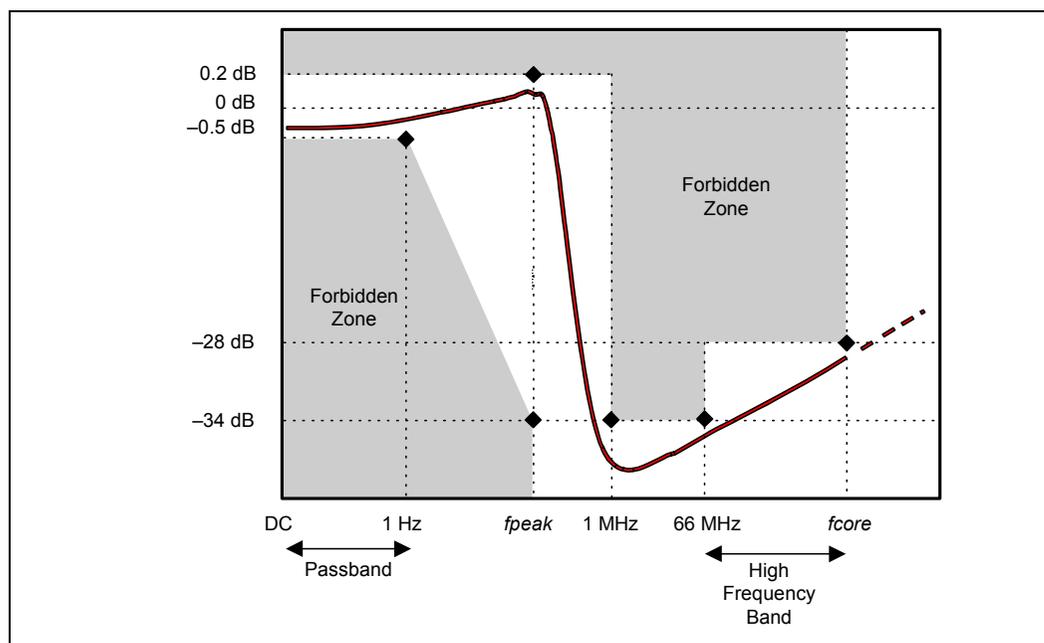
NOTES:
 1. Diagram not to scale.
 2. No specification for frequencies beyond *fcore* (core frequency).
 3. *fpeak*, if existent, should be less than 0.05 MHz.

Other recommendations:

- Use shielded type inductors to minimize crosstalk.

- Capacitors for the filter can be any value between 22 µF and 100 µF as long as components with ESL ≤ 5 nH and ESR < 0.3 Ω are used.

- Values of either 4.7 µH or 10 µH may be used for the inductor.

- Filter should support DC current > 60 mA

- DC voltage drop from VCC to VCCA should be < 60 mV.

- To maintain a DC drop of less than 60 mV, the total DC resistance of the filter from VCC_CPU to the processor socket should be a maximum of 1 Ω

Other routing requirements:

- C should be within 600 mils of the VCCA and VSSA pins. An example of the component placement is shown in Figure 12-13.

- VCCA route should be parallel and next to VSSA route (minimize loop area).

- A minimum of a 12 mil trace should be used to route from the filter to the processor pins.

- L should be close to C.

Figure 12-13. Example Component Placement for PLL Filter
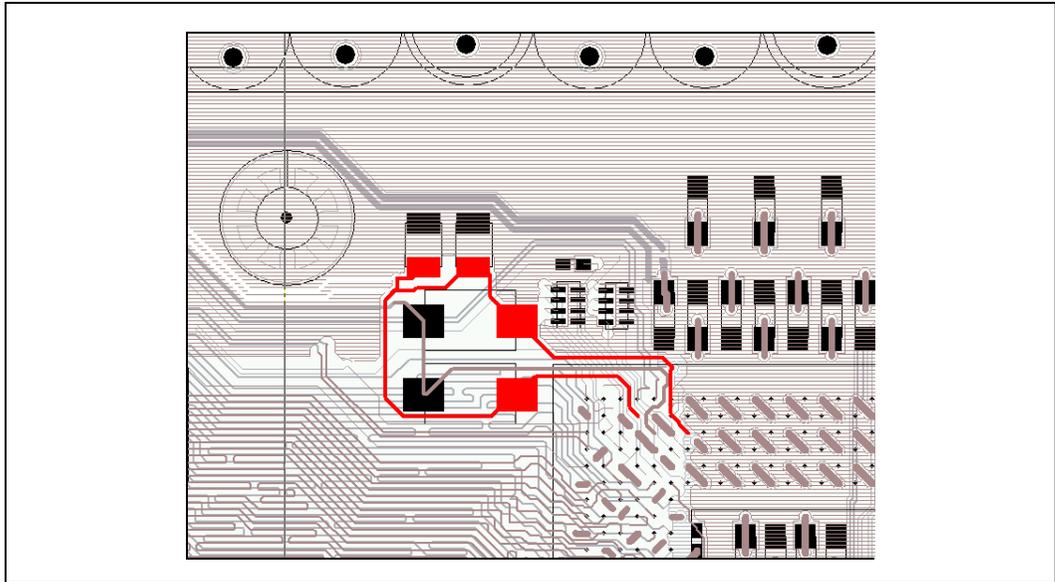
12.7 MCH Power Delivery Requirements

The following guidelines are recommended for optimum MCH power delivery. The main focus of these guidelines is to minimize power noise and signal integrity problems to the E7205 chipset. The following guidelines are not intended to replace thorough system validation on E7205 chipset-based products.

Figure 12-14. MCH Decoupling Placement (Backside View)
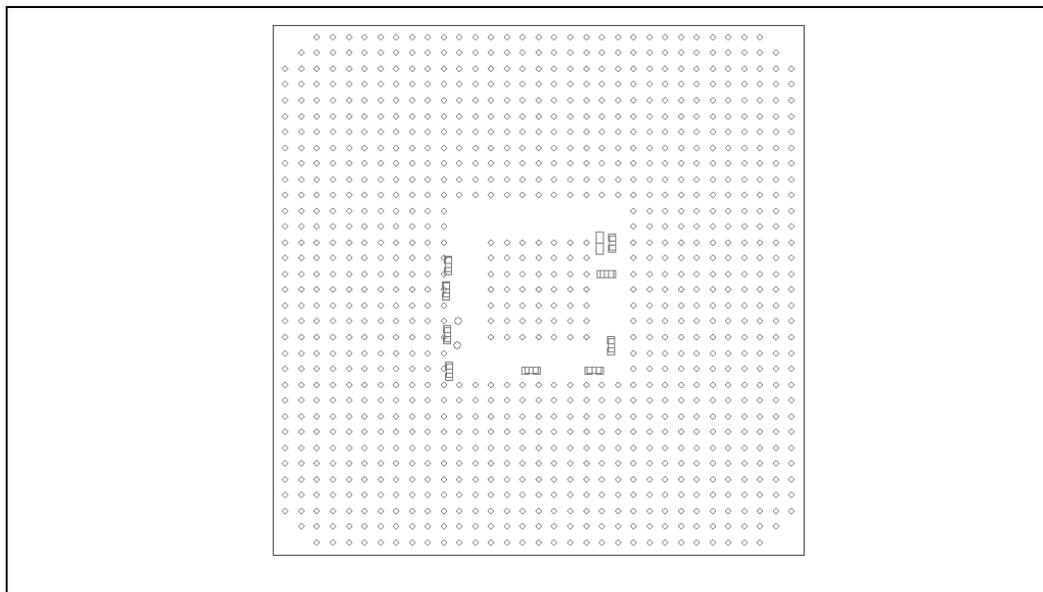
12.7.1 2.5 V Power Plane (DDR)

See Section 6.3.1.1.

12.7.2 1.25 V Power Plane (DDR_VTT)

See Section 6.4.3 and Section 6.4.2.

12.7.3 VCC_CPU

A maximum of five, 0.1 µF capacitors are recommended (at least four (4) with 900 pH to 1.1 nH inductance must be placed under the MCH) for FSB 1.45 V power plane decoupling. The designer should evenly distribute placement of decoupling capacitors among the FSB interface signal field. In addition to the minimum decoupling capacitors under the MCH, the designer should place a maximum of nine evenly-spaced capacitors for FSB (at least seven must be within 0.5 inch of the outer row of balls to the MCH).

12.7.4 1.5 V Power Plane (AGP)

Ten 0.1 µF high-frequency decoupling capacitors (package 0603) should be placed near the MCH to assist in the signal integrity areas of via stitching and return paths for the read condition of the AGP interface.

12.7.5   1.3 V Power Plane (VCC_CORE)

There are no additional decoupling requirements for the 1.3 V power plane.

12.7.6   Filter Specifications

VCCAHI and VCCAFSB are required by the MCH's internal PLLs and DLLs. VCCAHI is created by using a low pass filter on VCC1_3. VCCAFSB is created by using a low pass filter on VCC1_3. The MCH has internal analog PLL clock generators that require quiet power supplies for minimum jitter. Jitter is detrimental to a system—it degrades external I/O timings, as well as internal core timings (i.e., maximum frequency). The filter topologies are shown in Figure 12-15 through Figure 12-16.

When designing the VCCAHI and VCCAFSB filters (Figure 12-15 and Figure 12-16) make sure that the following guidelines are followed:

— One Inductor 100 nH close to the edge of the package (within 1 inch form the die).
— One LF capacitor 100 µF or 150 µF close to the edge of the package.
— At least one Low ESL HF capacitor, 0.1 µF on the backside of the motherboard under the die.

Figure 12-15. MCH Filter Topology for VCCAHI (HUB Interface)
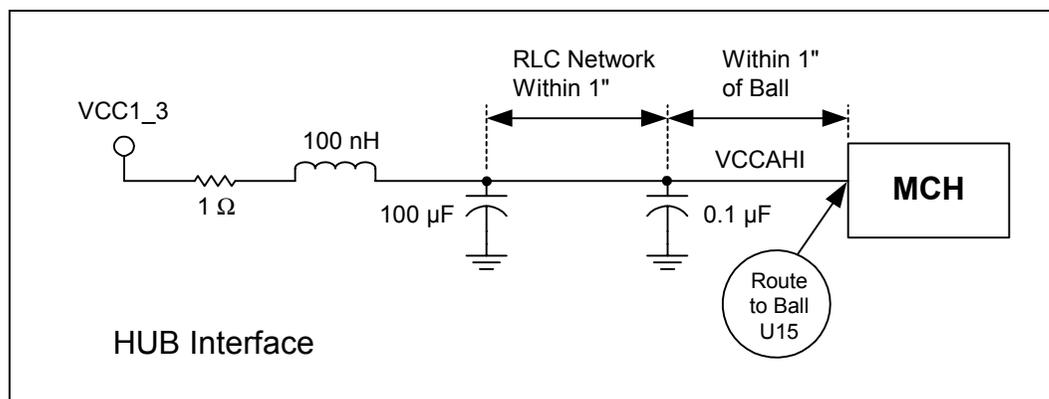
Figure 12-16. MCH Filter Topology for VCCAFSB (System Bus)
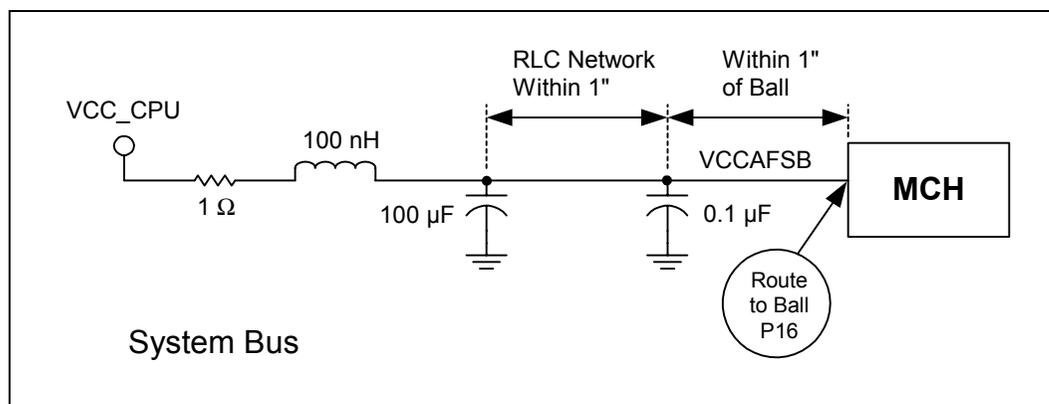
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Mechanical Design Considerations   **13**

13.1   Retention Mechanism Placement and Keep-Outs

The RM requires a keep-out zone for a limited component height area under the RM as shown in Figure 13-1 and Figure 13-2. The figures show the relationship between the RM mounting holes and pin one of the socket, and show the keep-out requirements.

The retention holes should be non-plated holes. The retention holes should have a primary and secondary side route keep-out area of 0.409 inches diameter.

For heatsink volumetric information, refer to the *Intel® Pentium® 4 Processor in the 478-pin Package Thermal Design Guidelines*.

Figure 13-1. Retention Mechanism Keep-Out
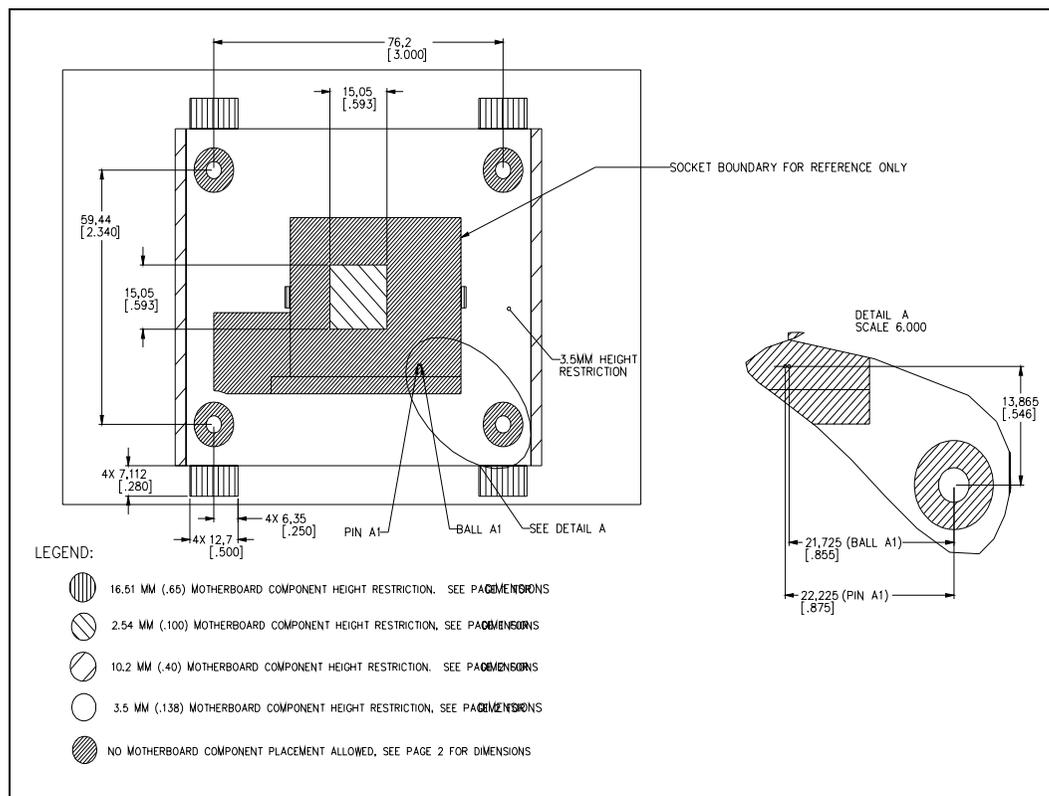
Figure 13-2. Retention Mechanism Keep-Out

![intel® logo]
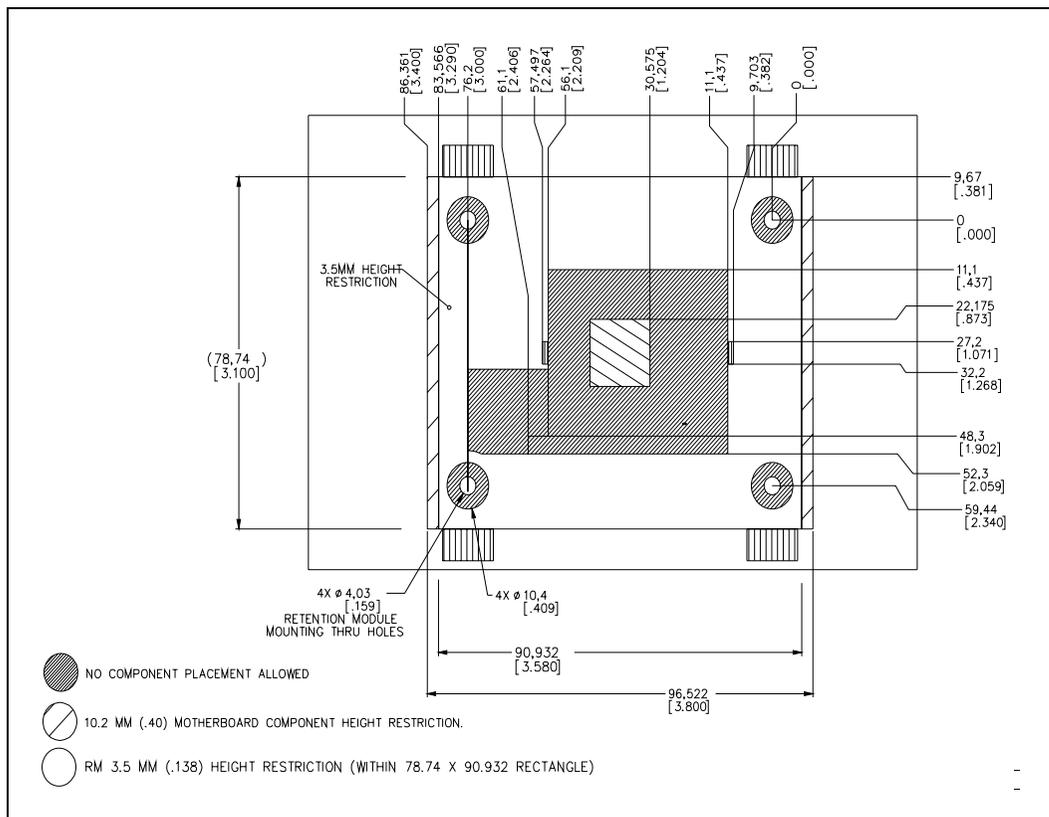
Schematic Checklist   **14**

14.1   Processor Checklist

Table 14-1 is a schematic checklist for the Pentium 4 processor with 512-KB L2 cache on 0.13 micron process.

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 1 of 3)

Checklist Items	Recommendations	Comments	√
Processor / MCH Signals			
A[35:3]	• Connect to HA[35:3] pins on MCH.		
ADS#	• Connect to the associated pin on the MCH.		
ADSTB[1:0]#	• Connect to HADSTB[1:0]# pins on MCH.		
BNR#	• Connect to the associated pin on the MCH.		
BPRI#	• Connect to the associated pin on the MCH.		
BR0#	• Connect to the associated pin on the MCH. • Terminate to VCC_CPU through a 150 Ω resistor near the processor.		
RESET#	• Connect to the associated pin on the MCH. • Terminate to VCC_CPU through a 150–220 Ω ± 5% resistor near the processor.		
D[63:0]#	• Connect to HD[63:0]# pins on MCH.		
DBI[3:0]#	• Connect to the associated pin on the MCH.		
DBSY#	• Connect to the associated pin on the MCH.		
DEFER#	• Connect to the associated pin on the MCH.		
DRDY#	• Connect to the associated pin on the MCH.		
DSTBN[3:0]#	• Connect to HDSTBN[3:0]# pins on MCH.		
DSTBP[3:0]#	• Connect to HDSTBP[3:0]# pins on MCH.		
HIT#	• Connect to the associated pin on the MCH.		
HITM#	• Connect to the associated pin on the MCH.		
LOCK#	• Connect to HLOCK# pin on MCH.		
REQ[4:0]#	• Connect to HREQ[4:0]# pins on MCH.		
RS[2:0]#	• Connect to the associated pin on the MCH.		
TRDY#	• Connect to HTRDY# pin on MCH.		

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 2 of 3)

Checklist Items	Recommendations	Comments	√
Processor / Intel® ICH4 Signals			
A20M#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required).		
CPUSLP#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required).		
FERR#	• Connect to the associated pin on the ICH4. • Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the ICH4.		
IGNNE#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required).		
INIT#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required). • A voltage translator is required for FWH. • Connect to Firmware Hub.		
LINT[1:0]	• LINT1 connects to ICH4 NMI (No extra pull-up resistors required). • LINT0 connects to ICH4 INTR (No extra pull-up resistors required).		
PWRGOOD	• Connects to ICH4 CPUPWRGD pin (Weak external pull-up resistor required). • Terminate to VCC_CPU through a 300 Ω ± 5% resistor.		
SMI#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required).		
STPCLK#	• Connect to the associated pin on the ICH4 (No extra pull-up resistors required).		
Processor Only Signals			
AP[1:0]#	• No Connect.		
BCLK[1:0]	• Connect to CK-408. • Connect 20 Ω – 33 Ω series resistors to each clock signal. • Connect a 49.9 Ω ± 1% shunt source termination (R_T) resistor to GND for each signal on the processor side of the series resistor (50 MB impedance).		
BPM[5:0]#	• These signals should be terminated with a 51 Ω ± 5% resistor to VCC_CPU near the processor. If a debug port is implemented termination is required near the debug port as well. Refer to the *ITP700 Debug Port Design Guide* for further information.		
BINIT#	• No Connect.		

BSEL[1:0]	• BSEL0:
	   Connect to CK-408.
	   Terminate to CK-408 3.3 V supply through a 1 kΩ resistor.
	• BSEL1:
	   No connect.		

COMP[1:0]	• Terminate to GND through a 49.9 Ω ± 1% resistor. • Minimize the distance from termination resistor and processor pin.		

Table 14-1. Intel® Pentium® 4 Processor Schematic Checklist (Sheet 3 of 3)

Checklist Items	Recommendations	Comments	√
DBR#	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
DP[3:0]#	• No Connect.		
IERR#	• No Connect.		
GTLREF3	• Terminate to VCC_CPU through a 49.9 Ω ± 1% resistor. • Terminate to GND through a 100 Ω ±1 % resistor. • Should be 2/3 VCC_CPU.		
GTLREF[2:0]	• No connect.		
ITP_CLK0	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
ITP_CLK1	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
MCERR#	• No Connect.		
PROCHOT#	• No Connect.		
RSP#	• No Connect.		
SKTOCC#	• Connect to Glue Chip / Discrete Logic (If pin is used).		
TCK	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
TDI	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
TDO	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
TESTHI	• See Section 5.4.1.9.		
THERMTRIP#	• Terminate to VCC_CPU through a 62 Ω ± 5% resistor near the processor.		
THERMDA	• Connect to thermal monitor circuitry if used.		
THERMDC	• Connect to thermal monitor circuitry if used.		
TMS	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
TRST#	• Refer to the *ITP700 Debug Port Design Guide* for further information.		
VCCA	• Connect with isolated power circuitry to VCC_CPU.		
VCCIOPLL	• Connect with isolated power circuitry to VCC_CPU.		
VCC_SENSE	• Used as feedback to VR controller or leave as no connect.		
VCCVID	• Connect to 1.2 V linear regulator. • The voltage specification for VCCVID is 1.2 V +10% / -5%. The voltage specification applies to both static and AC components for this voltage. In addition, the rising edge of the voltage must be monotonic.		
VID[4:0]	• Connect to VR or VRM. These signals must be pulled up to 3.3 V through 1 kΩ pull-ups.		
VSSA	• Connect with isolated power circuitry to VCC_CPU.		
VSS_SENSE	• No Connect		

14.2 Intel® E7205 Chipset MCH Checklist

For specific layout recommendations, refer to the appropriate section of this document.

Table 14-2. MCH Schematic Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
Host Interface			
ADS# AP[1:0]# BINIT# BNR# BPRI# BREQ0# DBSY# DEFER# HA[35:3]# HD[63:0]# HADSTB[1:0]# HDSTBP[3:0]# HDSTBN[3:0]# HIT# HITM# HLOCK# HREQ[4:0]# HTRDY# DEP[3:0]# DRDY# RS[2:0]# RSP# CPURST# XERR#	• See Processor section of this checklist.		
DINV[3:0]#	• Connect to Processor DBI[3:0]#.		
Hub Interface A			
HI_A[11:0]	• Maximum length of 20" (stripline routing).		
PSTRBF_0 PSTRBS_0	• Connect to Intel® ICH4. • Must **not** have pull-up, pull-down, or series resistors.	• The length of each data signal must be matched within ± 0.1 of the associated HI_STRB differential pair.	
Clocks, Reset, Miscellaneous Signals			
HCLKINP HCLKINN	• Route to CK408 with a 49.9 Ω pull-down resistor to ground.		
RSTIN#	• Connect to PCIRST# output of the Intel® ICH4.		
PRCOMP_A	• Tie the COMP pin to a 32.4 Ω ± 1% Pull up to VCC.	• Used to calibrate the I/O Buffers. • Resistive compensation is used by the ICH4 and MCH to adjust the buffer characteristics to specific board characteristic. Same compensation must be used on both ICH4 and MCH side.	
HYRCOMP HXRCOMP	• Tie the COMP pin to a 24.9 Ω ± 1% pull down resistor to ground.	• This signal is used to calibrate the Host AGTL+ I/O buffers characteristics to specific board characteristic.	

Table 14-2. MCH Schematic Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
PRCOMP_AGP0 PRCOMP_AGP1	• Tie the COMP pin to a 43.2 Ω ± 1% pull down resistor to ground.	• Resistive compensation is used by the AGP to adjust the buffer characteristics to specific board characteristics.	
TESTSIG1 TESTSIG2	• Can be left as No Connect.		
TESTSIG3	• Tie to a resistor divider with 100 Ω to VSS and 49.9 Ω to 1.3 V.		
TESTSIG4	• 24.9 Ω pull-up to 1.3 V.		
Voltage References - Power Planes			
HDVREF[3:0] HAVREF[1:0] CCVREF	• Use one dedicated voltage divider for all these signals. Decouple the voltage divider with 1 µF capacitor.	• To provide constant and clean power delivery to the data, address and common clock signals of the host AGTL+ interface.	
VREF_DDR	• Route from VR to DIMMs and MCH.		
PREF_A	• Hub reference voltage = 0.350 V ± 1%. • R1 = 392 ± 1% Ω R2 = 499 ± 1% Ω R3 = 453 ± 1% Ω C1 = 0.1 µF C2 = 0.01 µF	• HIVREF should be generated locally with a voltage divider circuit. The value of these resistors must be chosen to ensure that the reference voltage tolerance is maintained over the entire input leakage specification. • Resistances shown are only suggested values to achieve proper reference voltage of 0.35 V. See latest board schematics for actual CRB implementation.	
HXSWNG HYSWNG	• The host compensation reference voltage can be implemented using a simple voltage divider circuit. • R1 =150 ± 1% and R2 =301± 1% C1 = C2 = 0.01 µF	• The HSWNG inputs of MCH are used provide reference voltage for the compensation logic.	
HISWNG[B:A]	• Hub reference swing voltage = 0.800 V ±1%. • $R6^1$ = 80.6 ± 1% Ω or $R6^2$ = 226 ± 1% $R5^1$ = 51.1 ± 1% Ω or $R5^2$ = 147 ± 1% $R4^1$ = 40.2 ± 1% Ω or $R4^2$ = 113 ± 1% C1 = 0.1 µF C2 = 0.01 µF	• The MCH hub interfaces use a compensation voltage to control the buffer voltage characteristics. • Resistances shown are only suggested values to achieve proper swing voltage of 0.8 V. See latest board schematics for actual CRB implementation. **NOTE:** Use only resistors from group 1 or 2; do not mix values from these groups.	

14.3   Intel® ICH4 Checklist

For specific layout recommendations, refer to the appropriate section of this document.

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 1 of 8)

Checklist Items	Recommendations	Comments	√
PCI Interface			
PERR#, SERR#, PLOCK#, STOP#, DEVSEL#, TRDY#, IRDY#, FRAME#, REQ[4:0]#, GPIO0/REQA#, GPIO1/REQB# / REQ5#	• These signals require a pull-up resistor. Recommend an 8.2 kΩ pull-up resistor to VCC3_3 or a 2.7 kΩ pull-up resistor to VCC5.	• See PCI 2.2 Component Specification for pull-up recommendations for VCC3_3 and VCC5.	
PCIRST#	• The PCIRST# signal should be buffered to form the IDERST# signal 33 Ω series resistor to IDE connectors.	• Improves Signal Integrity.	
PCIGNT[4:0]#	• No external pull-up resistors are required on PCI GNT signals. However, if external pull-up resistors are implemented, they must be pulled up to VCC3_3.	• These signals are actively driven by the Intel® ICH4.	
PME#	• No extra pull-up resistor.	• This signal has integrated pull-up of 18 kΩ to 42 kΩ.	
GNTA# /GPIO16, GNTB/ GNT5#/ GPIO17	• No extra pull-up needed.	• These signals have integrated pull-ups of 24 kΩ. • GNTA has an added strap function of "top block swap". The signal is sampled on the rising edge of PWROK. Default value is high or disabled due to pull-up. A Jumper to a pull-down resistor can be added to manually enable the function.	
IDSEL	• The series resistor on IDSEL should be 300 Ω to 900 Ω.	• See Table 10-17.	
Hub Interface			
HICOMP	• Tie the HICOMP pin to a 43.3 Ω ± 1% pull-up resistor to VCC1_5.	• ZCOMP No longer supported.	
HI_VSWING	• 800 mV.	• See Section 7.2.	
LAN Interface			
LAN_CLK	• Connect to LAN_CLK on Platform LAN Connect Device.	• ICH4 contains integrated 100 kΩ nominal pull-down resistor on signal.	
LAN_RXD[2:0]	• Connect to LAN_RXD on Platform LAN Connect Device.	• ICH4 contains integrated 10 kΩ pull-up resistors on interface.	
LAN_TXD[2:0], LAN_RSTSYNC	• Connect to LAN_TXD on Platform LAN Connect Device.		
If the LAN connect interface is not used.	• Platform LAN connect interface can be left NC if not used.	• Input buffers internally terminated.	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 2 of 8)

Checklist Items	Recommendations	Comments	√
EEPROM Interface			
EE_DOUT	• Prototype Boards should include a placeholder for a pull-down resistor on this signal line, but do not populate the resistor. Connect to EE_DIN of EEPROM or CNR Connector.	• ICH4 contains integrated pull-up resistor for this signal. • Connected to EEPROM data input signal (Input from EEPROM perspective and output from ICH4 perspective).	
EE_DIN	• No extra circuitry required. Connect to EE_DOUT of EEPROM or CNR Connector.	• ICH4 contains integrated pull-up resistor for this signal. • Connected to EEPROM data output signal (Output from EEPROM perspective and input from ICH4 perspective).	
FWH/LPC Interface			
FWH[3:0] / LAD[3:0], LDRQ[1:0]	• No extra pull-ups required. Connect straight to FWH/LPC.	• ICH4 Integrates 24 kΩ pull-up resistors on these signal lines.	
FWH Decoupling	• Follow vendor recommendation.		
Interrupt Interface			
PIRQ[D:A]#	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15.	
PIRQ[H:E]#/ GPIO[5:2]	• These signals require a pull-up resistor. Recommend a 2.7 kΩ pull-up resistor to VCC5 or 8.2 kΩ to VCC3_3.	• The PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14 or 15.	
APIC	• The APICCLK should be tied directly to GND. Pull APICD[1:0] to GND through a 10 kΩ pull-down resistor. If using XOR chain testing, a pull-down for each APIC signal is required (i.e., two 10 kΩ pull-down resistors).		
SERIRQ	• External weak (8.2 kΩ) pull-up resistor to VCC3_3 is recommended.	• Open drain signal.	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 3 of 8)

Checklist Items	Recommendations	Comments	√
GPIO			
GPIO Pins	GPIO[7:0]: • These pins are in the main power well. Pull-ups must use the VCC3_3 plane. • Unused core well inputs must be pulled up to VCC3_3. • GPIO[1:0] can be used as REQ[B:A]#. • GPIO1 can be used as PCI REQ5#. • GPIO[5:2] can be used as PIRQ[H:E]#. • GPIO6. • These signals are 5 V tolerant. • These pins are inputs. GPIO8 and [13:11]: • These pins are in the resume power well. Pull-ups must use the VccSus3_3 plane. • Unused resume well inputs must be pulled up to VccSus3_3. • These signals **are not** 5 V tolerant. • GPIO11 can be used as SMBALERT#. • These pins are inputs. GPIO[23:16]: • Fixed as output only. Can be left NC. • GPIO22 is open drain. • GPIO[17:16] can be used as GNT[B:A]#. • GPIO17 can be used as PCI GNT5#. • GPIO18. • GPIO19. • GPIO20. • GPIO21. • GPIO22 (open drain). • GPIO23. • These signals **are not** 5 V tolerant. GPIO[28, 27, 25, 24]: • I/O pins. Default as outputs so can be left as NC. • These pins are in the Resume Power Well. • GPIO[28:27, 25] From resume power well. (Note: use pull-up to VccSus3_3 if these signals are pulled-up). • GPIO24. • These signals **are not** 5 V tolerant. GPIO[43:32]: • I/O pins. From main power well. • Default as outputs. • These signals **are not** 5 V tolerant.	• Ensure that ALL unconnected signals are OUTPUTS ONLY!	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 4 of 8)

Checklist Items	Recommendations	Comments	√
USB			
USBRBIAS	• 22.6 Ω ± 1% connected to ground.		
USBRBIAS#	• Connected to the same 22.6 Ω ±1% resistor to ground as USBRBIAS.		
USBP[5:0]P, USBP[5:0]N	• No external resistors required.	• Output driver impedance of 45 Ω provided.	
OC[5:0]	• If not used, use 10 kΩ to VccSus3_3.	• Inputs must not float.	
Unconnected USB data signals	• Unconnected USB data signals can be left as no-connects.		
Power Management			
THRM#	• Connect to temperature Sensor. • pull-up if not used (an 8.2 kΩ pull-up resistor to VCC3_3).	• Input to ICH4 cannot float. THRM# polarity bit defaults THRM# to active low, so pull-up.	
THRMTRIP#	• See Section 5.4.1.1	• Input to Intel ICH4 cannot float.	
SLP_S3#, SLP_S4# SLP_S5#	• No pull-up/down resistors needed. Signals driven by ICH4.	• Signals driven by ICH4.	
PWROK	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VCC3_3 and VCC1_5 have reached their nominal voltages.	• Timing requirement.	
PWRBTN#	• No extra pull-up resistors.	• This signal has an integrated pull-up of 18 kΩ – 42 kΩ.	
SYS_RESET#	• Recommend an 8.2 kΩ pull-up resistor to VccSus3_3. Also a (100 Ω to 8.2 kΩ) pull-down resistor isolated from SYS_RESET# by means of a normally open switch.	• Input to Intel ICH4 cannot float. This pin forces an internal reset to the ICH4 after the signal is internally debounced.	
RI#	• RI# does not have an internal pull-up. Recommend an 8.2 kΩ pull-up resistor to resume well.	• If this signal is enabled as a wake event, it is important to keep this signal powered during the power loss event. If this signal goes low (active), when power returns the RI_STS bit will be set and the system will interpret that as a wake event.	
RSMRST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to LAN_RST#.	• Timing requirement.	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 5 of 8)

Checklist Items	Recommendations	Comments	√
LAN_RST#	• Recommend a 10 kΩ pull-down to ground. • This signal should be connected to power monitoring logic, and should go high no sooner than 10 ms after both VccSus3_3 and VccSus1_5 have reached their nominal voltages. Can be tied to RSMRST#.	• Timing requirement.	
Processor Signals			
A20M#, CPU_SLP#, IGNNE#, INTR, NMI, SMI#, STPCLK#	• Point-to-point connection. No external termination required at the ICH4. See Section 5.4.1.2 for processor guidelines.		
INIT#	• See Section 5.4.1.3 and Section 10.4.4.		
FERR#	• Requires external pull-up resistor to CPUVDD. See Section 5.4.1.1 for processor guidelines.		
RCIN#, A20GATE	• Pull-up signals to VCC3_3 through a 10 kΩ resistor.	• Typically driven by open drain external micro-controller.	
CPUPWRGD	• Connect to the processor's CPUPWRGD input. Requires external pull-up resistor. See Section 14.1 for processor guidelines.	• Refer to documentation of the processor that platform utilizes for specific values. This signal represents a logical AND of the Intel ICH4's PWROK and VRMPWRGD signals.	
System Management			
SMBDATA, SMBCLK	• Require external pull-up resistors. See Section 10.3.9 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination. • Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. • Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1.	• Value of pull-ups resistors determined by line load.	
SMBALERT# / GPIO11	• See GPIO section if SMBALERT# not implemented.		

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 6 of 8)

Checklist Items	Recommendations	Comments	√
SMLINK[1:0]	• Requires external pull-up resistors. See Section 10.3.9 to determine the appropriate power well to use to tie the pull-up resistors. (Core well, suspend well, or a combination). • Pull-up value also determined by bus section characteristics. Additional circuitry may be required to connect high and low powered sections. • Required to be tied to SMLink signals for SMBus 2.0 compliance. SMBCLK should be tied to SMLINK0 and SMBDATA should be tied to SMLINK1.	• Value of pull-ups resistors determined by line load. Typical value used is 8.2 kΩ.	
INTRUDER#	• Pull signal to VccRTC (VBAT) through ~10 kΩ.	• Signal in VccRTC (VBAT) well.	
RTC			
VBIAS	• The VBIAS pin of the ICH4 is connected to a 0.047 µF capacitor. See Figure 10-32.	• For noise immunity on VBIAS signal.	
RTCX1,RTCX2	• Connect a 32.768 kHz crystal oscillator across these pins with a 10 MΩ resistor. See Section 10.3.11.3 for capacitor guidelines.	• The external circuitry shown in Figure 10-32 will be required to maintain the accuracy of the RTC. • The circuitry is required since the new RTC oscillator is sensitive to step voltage changes in VccRTC and VBIAS. A negative step on power supply of more than 100 mV will temporarily shut off the oscillator for hundreds of milliseconds.	
RTCRST#	• Time constant due to RC filter on this line should be 18-25 ms. Recommended value for Resistor = 180 kΩ and Capacitor is 0.1 µF.	• Timing Requirement.	
AC'97			
AC_SDOUT	• Requires a jumper to 8.2 kΩ pull-up resistor. Should not be stuffed for default operation. • Series termination resistor 0 Ω to 47 Ω on board codec.	• This pin has a weak internal 20 kΩ nominal pull-down. To properly detect a safe_mode condition a strong pull-up will be required to over-ride this internal pull-down.	
AC_SDIN1, AC_SDIN0	• Internal pull-downs in Intel ICH4; no external pull-downs required. • Series termination resistor 0 Ω to 47 Ω from the AC_SDIN lines to the ICH4.	• These pins have a weak internal 20 kΩ nominal pull-down.	
AC_SDIN2	• Series termination resistor 33 Ω to 47 Ω from the AC_SDIN lines to the ICH4.	• This pin has a weak internal 20 kΩ nominal pull-down.	
AC_BITCLK	• No extra pull-down resistors required. • Series termination resistor 33 Ω to 47 Ω from the motherboard codec to the ICH4.	• This pin has a weak internal 20 kΩ nominal pull-down.	

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 7 of 8)

Checklist Items	Recommendations	Comments	√
AC_SYNC	• No extra pull-down resistors required.	• Some implementations add termination for signal integrity. Platform specific.	
Miscellaneous Signals			
SPKR	• See Section 10.3.5.3.	• Has integrated pull-down. The integrated pull-down is only enabled at boot/reset for strapping functions; at all other times, the pull-down is disabled.	
TP0	• TP0 requires external pull-up resistor to VccSus3_3.		
Power			
V_CPU_IO[2:0]	• The power pins should be connected to the proper power plane for the processor's CMOS compatibility signals. Use one 0.1 µF decoupling capacitor.	• Used to pull-up all processor interface signals.	
VccRTC	• Use one 0.1 µF decoupling capacitor. • No clear CMOS jumper on VccRTC. Use a jumper on RTCRST# or a GPI, or use a safe mode strapping for clear CMOS.		
VCC3_3	• Use six 0.1 µF decoupling capacitors.		
VccSus3_3	• Use two 0.1 µF decoupling capacitors.		
VCC1_5	• Use two 0.1 µF decoupling capacitors.		
VccSus1_5	• Use two 0.1 µF decoupling capacitor.		
V5REF_Sus	• Use one 0.1µF decoupling capacitor. • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3. For most platforms this is not an issue because VccSus3_3 is usually derived from V5REF_Sus.		
V5REF	• Use one 0.1 µF decoupling capacitor. • V5REF is the reference voltage for 5 V tolerant inputs in the ICH4. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.		
VCCPLL	• Use one 0.1 µF decoupling capacitor and one 0.01 µF decoupling capacitor.		
VCCHI	• Use two 0.1 µF capacitors.		
HIREF	• 350 mV.		

Table 14-3. Intel® ICH4 Schematic Checklist (Sheet 8 of 8)

Checklist Items	Recommendations	Comments	√
IDE Checklist			
PDD[15:0], SDD[15:0]	• No extra series termination resistors or other pull-ups/pull-downs are required. PDD7/SDD7 does not require a 10 kΩ pull-down resistor. • Refer to ATA ATPI-6 Specification.	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.	
PDIOW#, PDIOR#, PDDACK#, PDA[2:0], PDCS1#, PDCS3#, SDIOW#, SDIOR#, SDDACK#, SDA[2:0], SDCS1#, SDCS3#	• No extra series termination resistors. Pads for series resistors can be implemented should the system designer have signal integrity concerns.	• These signals have integrated series resistors. **NOTE:** Simulation data indicates that the integrated series termination resistors are a nominal 33 Ω but can range from 31 Ω to 43 Ω.	
PDREQ, SDREQ	• No extra series termination resistors. • No pull-down resistors needed.	• These signals have integrated series resistors in the ICH4.	
PIORDY, SIORDY	• No extra series termination resistors. • Pull-up to VCC3_3 via a 4.7 kΩ resistor.	• These signals have integrated series resistors in the ICH4.	
IRQ14, IRQ15	• Recommend 8.2 kΩ –10 kΩ pull-up resistors to VCC3_3. • No extra series termination resistors.	• Open drain outputs from drive.	
IDERST#	• The PCIRST# signal should be buffered to form the IDERST# signal. A 33 Ω series termination resistor is recommended on this signal.		
Cable Detect	Host Side/Device Side Detection (*recommended method*): • Connect IDE pin PDIAG#/CBLID to an ICH4 GPIO pin. Connect a 10 kΩ resistor to GND on the signal line. Device side detection: • Connect a 0.047 µF capacitor from IDE pin PDIAG#/CBLID to GND. No ICH4 connection.	• The 10 kΩ resistor to GND prevents GPI from floating if no devices are present on either IDE interface. Allows use of 3.3 V and 5 V tolerant GPIOs. **NOTE:** All Ultra DMA drives supporting modes greater than Mode 2 will have the capability to detect cables.	

14.4 Hub Interface Checklist

Table 14-4. Hub Interface Checklist

Checklist Items	Recommendations	Comments	√
MCH / Intel® ICH4 Signals			
HI_x[11:0]	• Connect together.		
HI_STB	• Connect together.		
HI_STB#	• Connect together.		
HI_REF	• Connect voltage divider circuit with R1=R2=150 Ω ± 1%. • Use two 0.1 µF capacitors within 150 mils of the ICH4. The MCH should be decoupled with one 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby. • Bypass to GND through a 0.1 µF capacitor located near each component's (MCH and ICH4) HIREF pin. • Decouple with a 0.1 µF capacitor placed near the divider circuit.		
VCC1_8	• Connect to 1.8 V power supply.		
MCH Signals Only			
PRCOMP_A	• Pull-up to VCC1_3 through a 32.4 Ω ± 1% resistor.		
ICH4 Signals Only			
HICOMP	• Tie the HICOMP pin to a 43.3 Ω ± 1% pull-up resistor to VCC1_5. ZCOMP is no longer supported.		

14.5 DDR SDRAM Checklist

Table 14-5. DDR SDRAM Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	• Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 39 Ω resistor. Resistor packs can be used, but do not use address/command or control signals on the same RPACK as these signals.		
DQS[17:9]	• These signals are left floating at the MCH. Ground them at the DIMM.		
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	• Connect from MCH to first and second DIMM in channel, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Resistor packs can be used, but do not use data/strobe or control signals on the same RPACK as these signals.		
CS_x[3:0]# CKE_x[3:0]	• Connect to a single DIMM, then terminate to DDR_VTERM (1.25 V) through a 56 Ω resistor. Refer to Table 6-2 for correct DIMM pin mapping. Resistor packs can be used, but don't use data/strobe or address/command signals on the same RPACK as these signals.		
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	• Route each signal and its complement differentially to the DIMM. Signal does not route to termination. Refer to Table 6-5 for correct DIMM pin mapping.		
VREF	• Connect to a resistor divider, 49.9 Ω to both 2.5 V and GND near the MCH, and add a 1 µF decoupling capacitor from VREF to ground near the divider. Connect to the VREF pin on each DIMM in the channel. Decouple each DIMM with a 0.1 µF capacitor. Decouple with a 0.1 µF capacitor near the MCH. See Section 6.4.4 for details.		
MCH Signals Only			
CMDCLK_x[3:2] CMDCLK_x[3:2]#	• These signals are left floating at the MCH.		
RCVENOUT_x#	• Connect to a resistor divider, 78.7 Ω to both 2.5 V and ground.		
DRCOMPVREF_H DRCOMPVREF_V	• Connect these signals together and to a resistor divider, 49.9 Ω to both 2.5 V and ground, decoupled with a 100 pF capacitor from DRCOMPVREF to ground.		
DRCOMP_H DRCOMP_V	• Connect to ground through a 24.9 Ω resistor.		
DDR_STRAP	• Connect directly to 2.5 V.		
ODTCOMP	• Connect to ground through a 402 Ω resistor.		
VCCDDR	• Connect to 2.5 V.		

Table 14-5. DDR SDRAM Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
DIMM Signals Only			
A13 FETEN VDDID	• No Connect.		
SDA	• Connect to SMBus Data.		
SCL	• Connect to SMBus Clock.		
VDD VDDQ	• Connect to 2.5 V.		
VSS	• Connect to ground.		
VDDSPD	• Connect to power (from a minimum of 2.3 V to a maximum of 3.6 V Strongly recommended connecting to 3.3 V.		
Decoupling Capacitors			
MCH High-Frequency Decoupling	• Place ten 0603 0.1 µF MLC capacitors near the MCH. Connect from 2.5 V to ground.		
MCH Bulk Decoupling	• Place four 100 µF capacitors between the MCH and the first DIMM. Connect from 2.5 V to ground.		
DIMM Decoupling	• Place two 100 µF capacitors per DIMM, one each on either side of the DIMM socket. Connect from 2.5 V to ground.		
VTT Decoupling	• Place one 0.1 µF capacitor for every two termination resistors (or 2 caps/RPACK). Place four 4.7 µF capacitors around the termination island, two on either side (See Figure 6-30). Connect from 1.25 V to ground.		

14.6 AGP Interface Checklist

Table 14-6. AGP Interface Checklist (Sheet 1 of 2)

Checklist Items[1]	Recommendations	Comments	√
MCH / Connector Signals			
AD_STB[1:0] (AGP 2.0) AD_STBF[1:0] (AGP 3.0)	• Connect to AGP connector.		
AD_STB[1:0]# (AGP 2.0)/ AD_STBS[1:0] (AGP 3.0)			
DBI_LO (AGP 3.0)			
GAD[31:0]			
GC/BE[3:0]# (AGP 2.0)/ GC#/BE[3:0] (AGP 3.0)			
GC_DET#	• See Figure 9-1		
GDEVSEL# (AGP 2.0)/ GDEVSEL (AGP 3.0)	• Connect to AGP connector.		
GFRAME# (AGP 2.0)/ GFRAME (AGP 3.0)			
GGNT# (AGP 2.0)/ GGNT (AGP 3.0)			
GIRDY# (AGP 2.0)/ GIRDY (AGP 3.0)			
GPAR			
GREQ# (AGP 2.0) GREQ (AGP 3.0)			
GSTOP# (AGP 2.0)/ GSTOP (AGP 3.0)			
GTRDY# (AGP 2.0/ GTRDY (AGP 3.0)			
MB_DET#	• Terminate to GND.		
PIPE# (AGP 2.0)/ DBI_HI (AGP 3.0)	• Connect to AGP connector.		
RBF (AGP 2.0)/ RBF# (AGP 3.0)			
SBA[7:0] (AGP 2.0)/ SBA[7:0]# (AGP 3.0)			
SB_STB (AGP 2.0)/ SB_STBF (AGP 3.0)			
SB_STB# (AGP 2.0)/ SB_STBS (AGP 3.0)			
ST0			
ST1			
ST2			
WBF# (AGP 2.0)/ WBF (AGP 3.0)			
VCC1_5	• Connect to 1.5 V power supply.		

Table 14-6. AGP Interface Checklist (Sheet 2 of 2)

Checklist Items[1]	Recommendations	Comments	√
Connector Signals Only			
3.3Vaux	• Connect to PCI 3.3VAUX.		
12V	• Connect to 12 V.		
AGPCLK	• Connect to CK408.		
INTA#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document.		
INTB#	• See recommendations for PIRQ[D:A]# signals in the ICH4 Section of this document.		
PERR	• Refer to Section 9.3.1.		
SERR# (AGP 2.0)/ SERR (AGP 3.0)	• Connect to AGP connector.		
OVRCNT	• No connect.		
PCIRST	• Connect to PCI slot PCIRST.		
PME#	• Connect to PCI PME#.		
TYPEDET#	• Refer to Section 9.3.2.		
USB+	• No connect.		
USB–	• No connect.		
VCC	• Connect to VCC3_3.		
VCC5	• Connect to VCC.		
VDDQ	• Connect to V1.5CORE.		
PREF_AGP[1:0]	• Connect to VREF divider network at the AGP connector.		
MCH Signals Only			
PREF_AGP[1:0]	• Connect to VREFCG pin on connector. • Terminate to ground through a 0.1 µF capacitor at the MCH.		
PRCOMP_AGP[1:0]	• Pull each signal to VCC_AGP through a 43.2 Ω ± 1% resistor.		

NOTE:
1. Checklist items may have differing names depending on the AGP signaling mode being used. In these cases, the differing names are separated by a slash with AGP2.0 signal names listed first, followed by AGP3.0 signal names.

14.7   CK 408 Clock Interface Checklist

Table 14-7. CK 408 Clock Interface Checklist (Sheet 1 of 2)

Checklist Items	Recommendations	Comments	√
66BUFF0	• Connect to MCH. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66BUFF1	• Connect to ICH4. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66BUFF2	• Connect to AGP. • Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
66IN	• No Connect.		
CPU[1:0]	• Connect to processor. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU[1:0]#	• Connect to processor. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU2 CPU2#	• Connect to MCH. • Connect to a series 27 Ω ± 5% resistor and terminate to GND through a 49.9 Ω ± 1% resistor.		
CPU_STOP#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
DOT48MHz	• No Connect.		
IREF	• Terminate to GND through a 475 Ω ± 1% resistor.		
MULT0	• Connected from the VCC3_3 through a series 10 kΩ ± 5% resistor and terminate to GND through a parallel 1 kΩ ± 1% resistor.		
PCI[6:0]	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
PCIF[2:0]	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
PCI_STOP#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
PWRDWN#	• Terminate to VCC3_3 through a 1 kΩ ± 1% resistor.		
REF0	• Connect to a series 33 Ω ± 5% resistor and terminate to GND through a 10 pF ± 5% capacitor.		
S[1:0]	• Terminate to VCC_CLK through a 1 kΩ ± 5% resistor.		
S2	• Terminate to GND through a 1 kΩ ± 5% resistor.		
SCLK	• Connect to DIMMs.		
SDATA	• Connect to DIMMs.		
USB48MHz	• Connect to ICH4. • Terminate to GND through a 33 Ω ± 5% resistor and a 10 pF ± 5% capacitor.		
VDD	• Terminate to VCC_CLK.		

Table 14-7. CK 408 Clock Interface Checklist (Sheet 2 of 2)

Checklist Items	Recommendations	Comments	√
VDD48MHz	• Terminate to VCC_CLK.		
VDDA	• Terminate to GND through a 0.1 µF ± 5% capacitor.		
VSS	• Terminate to GND.		
VSSA	• Terminate to GND.		
VSS48MHz	• Terminate to GND.		
VSSIREF	• Terminate to GND.		
VTT_PWRGD#	• Connect to an inverted copy of VCC_CPU. Refer to the respective section of the design guide for more details.		
XTAL_IN	• Terminate to GND through a 10 pF ± 5% capacitor.		
XTAL_OUT	• Terminate to GND through a 10 pF ± 5% capacitor.		

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Layout Checklist 15

15.1 System Bus Layout Checklist

Table 15-1. System Bus Layout Checklist (Sheet 1 of 2)

No.	Recommendations	Comments	√
Data Signals: D[63:0]#, DBI[3:0]#			
1	• Point-to-point Topology.		
2	• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.		
3	• 2.0 inches to 10.0 inches pin-to-pin data signal lengths.		
4	• Traces should be 7 mils wide with 13 mil spacing.		
5	• Data signals of the same source synchronous group should be routed to the same pad-to-pad length within +100 mils of the associated strobes.		
Data Strobes: DSTBN/P[3:0]			
1	• Traces should be 7 mils wide with 13 mil spacing.		
2	• Data strobes and their compliments should be routed within +25 mils of the same pad to pad length.		
Address Strobes: ADSTB[1:0]			
1	• Point-to-point Topology.		
2	• Edge to edge spacing versus trace to reference plane height ratio should be 3:1.		
3	• 2.0 inches to 10.0 inches pin-to-pin address signal lengths.		
4	• Traces should be 7 mils wide with 13 mil spacing.		
Address Signals: A[3:31]#, REQ[4:0]			
1	• Traces should be 7 mils wide with 13 mil spacing.		
2	• 2.0 inches to 10.0 inches pin-to-pin address signal lengths.		
3	• Address signals of the same source synchronous group should be routed to the same pad-to-pad length within +200 mils of the associated strobes.		
Clocks: HCLKINP/HCLKINN			
1	• These should be routed as a differential pair with 7 mil traces and 7 mil spacing between them.		
2	• 2.5 inches to 10.0 inches pin-to-pin common clock lengths.		
3	• 25 mil spacing should be maintained around all clocks.		

Table 15-1. System Bus Layout Checklist (Sheet 2 of 2)

No.	Recommendations	Comments	√
	Processor AGTL+: FERR#, PROCHOT#, THERMTRIP#		
1	• Traces should be 5 mils wide with 7 mil spacing.		
2	• 1.0 inches to 12.0 inches max from Processor to Intel® ICH4.		
3	• 3.0 inches max from ICH4 to VDD.		
	ICH4 AGTL+: A20M#, IGNNE#, INIT#, LINT[1:0], SLP#, SMI#, STPCLK		
1	• Traces should be 5 mils wide with 7 mil spacing.		
2	• 12.0 inches max from ICH4 to Processor.		
3	• Level shifting is required from the INIT# pin to FWH.		
	ICH4 Open Drain AGTL+: PWRGOOD		
1	• 7 mil spacing.		
2	• 1.0 inch to 12.0 inches max from ICH4 to Processor.		
3	• 1.1 inches max breakout length.		
4	• 3.0 inches max from Processor to VDD.		
	Miscellaneous AGTL+: BR0#, RESET#		
1	• Terminate using discrete components on the system board.		
2	• Minimize the distance between the terminating resistors and processor.		
3	• Connect the signals between these components.		
	Miscellaneous AGTL+: COMP[1:0]		
1	• Minimize the distance from terminating resistor.		
	Miscellaneous AGTL+: THERMDA, THERMDC		
1	• 10 mils wide by 10 mil spacing.		
2	• Remote sensor should be placed as close as possible to THERMDA/THERMDC pins. It can be approximately 4.0 inches to 8.0 inches away as long as the worst noise sources such as clock generators, data, buses and address buses, etc. are avoided.		
3	• Route in parallel and close together with ground guards enclosed.		

15.2 Intel® ICH4 Layout Checklist

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 1 of 5)

No.	Recommendations	Comments	√
1	• Board impedance must be 50 Ω ± 10% if using Hub Interface 1.5.		
2	• Traces must be routed 5 mils wide with 15 mils spacing.		
3	• To breakout of the MCH and Intel® ICH4 package, the Hub Interface signals can be routed 5 on 5. Signals must be separated to 5 on 15 within 300 mils of the package.		
4	• Max trace length 20" is dependant on MCH/ICH4 simulations.		
5	• Data signals must be matched within ± 0.1 inches of the HI_STB differential pair.		
6	• HI_STB/HI_STBS and HI_STB#/HI_STBF lengths must be matched.		
7	• (Local Reference Divider Circuit only) HIREF dividers should be placed no more than 4 inches of away from MCH or ICH4.		
8	• HI signals must be referenced to ground.		
IDE Interface			
1	• 5 mil wide and 7 mil spaces.		
2	• Max trace length is 8 inches long.		
3	• The maximum length difference between the data and strobe lengths is 0.5 inches.		
USB 2.0			
1	• With minimum trace lengths, route high-speed clock and USB differential pairs first.		
2	• Route USB signals ground referenced.		
3	• Route USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes.		
4	• When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal by minimizing impedance discontinuities.		
5	• Do not route USB traces under crystals, oscillators, clock synthesizers, magnetic devices or IC's that use and/or duplicate clocks.		
6	• Stubs on USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, the sum of all stubs on a given data line should not be greater than 200 mils.		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 2 of 5)

No.	Recommendations	Comments	√
7	• Route all traces over continuous planes (GND) with no interruptions. Avoid crossing over anti-etch if possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces. (Applies to USB signals, high-speed clocks, as well as slower signals that might be coupling to them.)		
8	• Keep USB signals clear of the core logic set. High current transients are produced during internal state transitions, which can be very difficult to filter out.		
9	• Keep traces at least 90 mils away from the edge of the plane (VCC or GND depending on which plane to which the trace is routed). This helps prevent the coupling of the signal onto adjacent wires and helps prevent free radiation of the signal from the edge of the PCB.		
10	• Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. (Recommended: 7.5 on 7.5 spacing with 4-layer, 4.3 mil prepreg stackup).		
11	• Minimize the length of high-speed clock and periodic signal traces that run parallel to USB signal lines to minimize crosstalk. The minimum recommended spacing to clock signals is 50 mils.		
12	• Use 20 mil minimum spacing between USB signal pairs and other signal traces. This helps to prevent crosstalk.		
13	• USB signal pair traces should be trace length matched. Max trace length mismatch between USB signal pair (such as DM1 and DP1) should be no greater than 150 mils.		
14	• No termination resistors needed for USB.		
15	• USBRBIAS (ball A23) and USBRBIAS# (ball B23) should be routed 5 on 5 with a single trace 500 mils or less to the 22.6 Ω 1% resistor to ground.		
16	• Maximum length from the ICH4 to the back panel should not be greater than 17 inches. Maximum length from the ICH4 to the CNR should not be greater than 8 inches.		
Platform LAN Connect Interface			
1	• Trace spacing: 5 mils wide, 10 mil.		
2	• Stubs due to R-pak CNR/LOM stuffing option should not be present.	• To minimize inductance.	
3	• Max mismatch between the length of a clock trace and the length of any data trace is 0.5 inches (clock must be longest trace).	• To meet timing and signal quality requirements.	
4	• Maintain constant symmetry and spacing between the traces within a differential pair out of the LAN PHY.	• To meet timing and signal quality requirements.	
5	• Keep the total length of each differential pair (from PHY to connector) under 4 inches (preferably less than 2 inches).	• Issues found with traces longer than 4 inches: IEEE phy conformance failures, excessive EMI and or degraded receive BER.	

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 3 of 5)

No.	Recommendations	Comments	√
6	• Do not route the transmit differential traces closer than 100 mils to the receive differential traces.	• To minimize crosstalk.	
7	• Distance between differential traces and any other signal line is 100 mils. (300 mils recommended).	• To minimize crosstalk.	
8	• Route 5 mils on 10 mils for differential pairs (out of LAN phy).	• To meet timing and signal quality requirements.	
9	• Differential trace impedance should be controlled to be ~100 Ω.	• To meet timing and signal quality requirements.	
10	• For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90-degree bend is required, it is recommended to use two 45-degree bends.	• To meet timing and signal quality requirements.	
11	• Traces should be routed away from board edges by a distance greater than the trace height above the ground plane.	• This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.	
12	• Do not route traces and vias under crystals or oscillators.	• This will prevent coupling to or from the clock.	
13	• Trace width to height ratio above the ground plane should be between 1:1 and 3:1.	• To control trace EMI radiation.	
14	• Traces between decoupling and I/O filter capacitors should be as short and wide as practical.	• Long and thin lines are more inductive and would reduce the intended effect of decoupling capacitors.	
15	• Vias to decoupling capacitors should be sufficiently large in diameter.	• To decrease series inductance.	
16	• Avoid routing high-speed LAN near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.	• To minimize crosstalk.	
17	• Isolate I/O signals from high-speed signals.	• To minimize crosstalk.	
18	• Place the Intel® 82562ET/EM part more than 1.5 inches away from any board edge.	• This minimizes the potential for EMI radiation problems.	
19	• Place at least one bulk capacitor (4.7 µF or greater OK) on each side of the Intel® 82562ET/EM.	• Research and development has shown that this is a robust design recommendation.	
20	• Place decoupling capacitors (0.1 µF) as close to the Intel® 82562ET/EM as possible.		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 4 of 5)

No.	Recommendations	Comments	√
AC'97			
1	Z_O AC97 = 60 Ω ± 15%.		
2	4 mil trace width, 6 mil spacing between traces.		

3	AC_SDIN Max Trace Lengths
	• ICH4 to primary codec:
	  L = 14 inches.
	• From Primary Codec T junction to CNR:
	  L = 6 inches.
	• CNR:
	  L = 14 inches.
	   (Using given example 4-layer 4.3 mil prepreg stackup.)		

4	AC_SDOUT Max Trace Lengths
	• ICH4 to primary codec:
	  L = 14 inches.
	• CNR:
	  L = 14 inches.
	  (Using given example 4-layer 4.3 mil prepreg stackup.)		

5	AC_BIT_CLK Max Trace Lengths
	• ICH4 to primary codec:
	  L = 13.6 inches.
	• CNR:
	  L = 13.6 inches.
	  (Using given example 4-layer 4.3 mil prepreg stackup.)		

6	• Series termination resistor on AC_BIT_CLK line should be no more than 0.9 to 7.6 inches from the ICH4.		
7	• Series termination resistors on AC_SDIN lines if needed should be no more than 100 to 400 mils from the CNR card or the on board codec.		
Clocking			
1	• CLK_33 goes to ICH4, FWH, and SIO. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 15 inches max. Routed on one Layer.		
2	• PCI_33 goes to PCI Device or PCI Slot, there are 5 clocks. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 13 inches max. Routed on one Layer.		
3	• CLK_66 goes to ICH4 and MCH. • Clock chip to series resistor 0.5 inches and from series resistor to receiver 14 inches max. Routed on one Layer.		

Table 15-2. Intel® ICH4 Layout Checklist (Sheet 5 of 5)

No.	Recommendations	Comments	√
RTC			
1	• RTC LEAD length = 1.0 inches Max.		
2	• Minimize capacitance between RTCX1 and RTCX2.		
3	• Put GND plane underneath Crystal components.		
4	• Do not route switching signals under the external components (unless on other side of board).		
5	• If SUSCLK is not used in the platform it should be routed to a testpoint.	• The ability to probe this signal can decrease the resolution time for RTC related issues.	
PCI Guidelines			
1	• Data Lines - See specific topology guidelines in Table 10-17).		
2	• Clock Lines (See Figure 10-29 and Table 10-18).		
3	• IDSEL (See Figure 10-28).		
Processor CMOS Guidelines			
1	• Series termination should be less than 2000 mils from the ICH4. Total length from the ICH4 to the processor should be no more than 19 inches.		
FWH Decoupling Guidelines			
1	• 0.1 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		
2	• 4.7 µF capacitors should be placed between the VCC supply pins and the VSS ground pins and no less than 390 mils from the VCC supply pins.		

15.2.1 Intel® ICH4 Decoupling

Table 15-3. Intel® Decoupling Checklist

No.	Recommendations	Comments	√
1	• VCC3_3: Six 0.1 µF capacitors. Less than 100 mils from package Place near balls: A4, A1, H1, T1, AC10, and AC18.		
2	• VccSus3_3: Two 0.1 µF capacitors. Less than 100 mils from package Place near balls: A22 and AC5.		
3	• V_{CPU_IO}: One 0.1 µF capacitor. Less than 100 mils from package Place capacitor near ball AA23.		
4	• VCC1_5: Two 0.1 µF capacitors. Less than 100 mils from package Place near balls: K23 and C23.		
5	• VccSus1_5: Two 0.1 µF capacitors. Less than 100 mils from package Place near balls: A16 and AC1.		
6	• V5REF: One 0.1 µF capacitor. Less than 100 mils from package Place capacitor near balls: E7. • V5REF is the reference voltage for 5 V tolerant inputs in the Intel® ICH4. Tie to pins V5REF[2:1]. V5REF must power up before or simultaneous to VCC3_3. It must power down after or simultaneous to VCC3_3.		
7	• V5REF_Sus: One 0.1 µF capacitor. Less than 100 mils from package Place capacitor near ball: A16. • V5REF_Sus only affects 5 V-tolerance for USB OC[5:0]# pins and can be connected to VccSus3_3 if 5 V tolerance on these signal is not required.		
8	• VccRTC: One 0.1 µF capacitor. Place near ball: AB5.		
9	• VCCHI: Two 0.1 µF capacitor. Less than 100 mils from package Place near balls: T23 and N23.		
10	• VCCPLL: One 0.1 µF and one 0.01 µF capacitor. Within 100 mils of package Place near ball: C22.		

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15.3　Hub Interface Layout Checklist

Table 15-4. Hub Interface Layout Checklist

No.	Recommendations	Comments	√
General Recommendations			
1	• It is recommended that all signals be referenced to VSS.		
2	• Board impedance must be 60 Ω ± 10%.		
3	Traces must be routed as follows (see below for breakout routing requirements): • Data to Data: 7/13 mils. • Strobe to Strobe: 7/13 mils. • Strobe to Data: 7/18 mils. • Other signals to Data: 7/13 mils.		
4	• Max trace length is 8 inches.		
Data Signals			
1	• Can be routed to 7 on 5 for breakout, but must be separated to 5 on 15 within 300 mils of the package.		
2	• No explicit matching requirements between individual data signals.		
Strobe Signals			
1	• Strobe pair should have a minimum of 15 mils spacing from any adjacent signals.		
2	• Each strobe signal must be the same length.		
3	• Strobe trace lengths should be 0 – 400 mils shorter than the longest data trace length.		

15.3.1 Hub Interface Decoupling, Compensation, and VREF

Table 15-5. Hub Interface Decoupling, Compensation, and VREF Checklist

No.	Recommendations	Comments	√
VCC1_8 Decoupling			
1	• Decouple the Intel® ICH4 with two 0.1 µF capacitors within 150 mils from the package.		
2	• Decouple the MCH with one 0.1 µF capacitor within 150 mils of the package and one 10 µF capacitor nearby.		
3	• Capacitors should be adjacent to hub interface rows.		
HLRCOMP			
1	• Place resistor using a 10 mils wide and 0.5 inch max trace length.		
2	• 7 mil group spacing.		
3	• Minimize the distance between HLRCOMP resistor and MCH.		
HI_REF			
1	• Should be placed no more than 4 inches of away from MCH or ICH4.		
2	• Bypass to ground with a 0.1 µF capacitor located within 0.25 inches of each component's HIREF pin.		
3	• Place one 0.1 µF capacitor at the divider.		

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15.4 System Memory Layout Checklist

15.4.1 Unbuffered DDR (2 DIMM) Checklist

Table 15-6. Unbuffered DDR (2 DIMM) Checklist

Checklist Items	Recommendations	Comments	√
MCH / DIMM Signals			
DQ_x[63:0] CB_x[7:0] DQS_x[8:0]	• Route on a ground-referenced layer (stripline for Channel A, microstrip for Channel B). MCH to first DIMM should be 1.5"–5.0", Z_O = 50 Ω, 7/15. First DIMM to second DIMM should be 1.1"–1.2", 60 Ω, 5/15. Second DIMM to termination should be 0.1"–1.5", 60 Ω, 5/15. DQ/CB lengths should be within 25 mils of associated DQS. Make sure to match the strobe lengths to the clocks as described in Section 6.2.3.	ChA	
		ChB	
MA_x[12:0] BA_x[1:0] RAS_x# CAS_x# WE_x#	• Route on a ground-referenced microstrip layer, Z_O = 60 Ω, 5/12. MCH to first DIMM should be 1.5"–6.5". First DIMM to second DIMM should be 1.1"–1.2". Second DIMM to termination should be 0.1"–1.5". Make sure to match the signal lengths to the clocks as described in Section 6.2.4.1.	ChA	
		ChB	
CS_x[3:0]# CKE_x[3:0]	• Route on a ground-referenced microstrip layer, Z_O = 60 Ω, 5/15. MCH to DIMM should be 1.5"–5.5", DIMM to termination should be 1.0"–2.5". Make sure to match the signal lengths to the clocks as described in Section 6.2.2.1.	ChA	
		ChB	
CMDCLK_x[7:4,1:0] CMDCLK_x[7:4,1:0]#	• Route differentially on a ground-referenced microstrip layer. MCH to DIMM should be 3.5"–9.0", diff. Z_O = 84 Ω, 6/7. Keep clock pairs 20 mils from any other signals. Make sure to adhere to length matching rules for above signals.	ChA	
		ChB	
VREF	• Route a 12 mil wide trace to the resistor divider and to each DIMM in the channel. Keep all other signals at least 20 mils away.	ChA	
		ChB	
MCH Signals Only			
RCVENOUT_x#	• Connect to resistor divider with a 7 mil wide trace. Keep the trace length to a minimum.	ChA	
		ChB	
DRCOMPVREF_H DRCOMPVREF_V	• Connect to resistor divider with a 20 mil wide trace. Keep the trace length to a minimum.		
DRCOMP_H DRCOMP_V	• Connect to pull-down resistor with a 7 mil wide trace. Keep the trace length to a minimum.		
DDR_STRAP	• Connect to 2.5 V with a 7 mil wide trace. Keep the trace length to a minimum.		
ODTCOMP	• Connect to pull-down resistor with a 7 mil wide trace. Keep the trace length to a minimum.		

15.5 AGP 8X Layout Checklist

Table 15-7. AGP 8X Layout Checklist (Sheet 1 of 3)

No.	Recommendations	Comments	√
Power Plane Decoupling			
1	• Use high-frequency decoupling capacitors in the range of (0.001 µF – 1 µF).		
2	• Use bulk decoupling capacitors in the range of (0.001 µF – 1 µF).		
3	• Capacitors should be as close to the power pins as possible. If possible, capacitors should be mounted on the backside of the graphics card under the controller package. Bulk decoupling can be mounted near the chipset interface and near the connector for power delivery and signaling reasons.		
AC Signal Decoupling Requirements			
1	• Place 3 0.01 µF or larger, low ESL capacitors as close as possible to a VCC3_3 pair of pins on the connector.		
2	• Place 6 0.01 µF or larger, low ESL capacitors as close as possible to a VDDQ pair of pins on the connector.		
3	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the +5 V connector pin.		
4	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the +12 V connector pin.		
5	• Place 1 0.01 µF or larger, low ESL capacitor as close as possible to the 3.3 Vaux connector pin.		
6	• All power and ground pins must be connected to the motherboard to guarantee power delivery and proper AC signal return paths.		
7	• All ground pins on the add-in cards must be connected for proper grounding and AC return paths. All VDDQ pins must be connected on the add-in card to the local VDDQ power plane. All used power pins must be bypassed to ground close to the connector with a 0.01 µF or larger, low ESL/ESR capacitor to provide good AC coupling to the adjacent signaling pins.		

Table 15-7. AGP 8X Layout Checklist (Sheet 2 of 3)

No.	Recommendations	Comments	√
Motherboard Layout Requirements			
1	• AGP strobe signals must be grouped with associated data signals. It is also recommended that the strobe be centered within its associated group to minimize the signal to strobe skew.		
2	• AD_STB0 (AGP 2.0) / AD_STBFO (AGP 3.0) and AD_STB0# (AGP 2.0) / AD_STBS0 (AGP 3.0) should be grouped with AD[15:0] and C/BE[1:0]#.		
3	• AD_STB1 (AGP 2.0) / AD_STBF1 (AGP 3.0) and AD_STB1# (AGP 2.0) / AD_STBS1 (AGP 3.0) should be grouped with AD[31:16], C/BE[3:2]#, DBI_HI, DBI_LO (AGP 3.0).		
4	• SB_STB and SB_STB# should be grouped with SBA[7:0] (AGP 2.0). or • SB_STBF and SB_STBS should be grouped with SBA[7:0]#.		
5	• Traces should as short and direct as possible. Avoid changing the power plane reference during routing.		
6	• PCB should be fabricated using FR-4 with an overall board thickness of 62 miles ± 10%. The outer layers should use ½ copper and the inner layers should use 1 oz. copper.		
7	• AGP signals must be carefully routed on the motherboard and graphics card to meet the timing and signal quality requirements of the specification.		
Trace Length Mismatch Requirements			
1	• Avoid signal mismatch by routing all lines within a group using the same type (either stripline or microstrip).		
2	• For add-in cards, the data lines should be kept within ± 0.025 inches from their respective strobe.		
3	• For motherboards, the data lines should be kept within ± 0.025 inches from their respective strobe.		
Strobe Trace Routing Considerations			
1	• The strobe signals should be routed together, but separated by at least five times the maximum dielectric thickness to each other and to any other signal routed adjacent to the strobe.		
Board Constraints			
1	• Impedance of required microstrip traces is specified at 60 Ω ± 10% and the impedance for stripline traces is specified at 56 Ω ± 10% for add-in cards and motherboards.		
2	• Reduce crosstalk by decreasing the distance of a trace to the nearest reference plane (dielectric thickness/height). Or increase the distance to adjacent traces.		
3	• The 8X mode source synchronous signals and the 66 MHz clock signal should not cross any split planes. Ensure signal quality is not compromised.		
4	• All 8X mode source synchronous signals should be routed on a layer reference to a ground plane.		
5	• Dummy vias should be used to match the total via count for each group.		

Table 15-7. AGP 8X Layout Checklist (Sheet 3 of 3)

No.	Recommendations	Comments	√
	Control Signal and Clock Recommendations		
1	• There are no external pull-up or pull-down resistors for control signals on the AGP 8X mode board design since resistors are integrated inside the device buffers.		
	Ground Plane References		
1	• Each source synchronous signal group must be routed on the same layer referenced to ground with the same layer transitions.		
	VDDQ Plane		
1	• The plane from the voltage regulator source to the AGP connector VDDQ pins should be wide enough to minimize the inductance path.		
2	• Buffer I/O rail on the add-in card should connect to the VDDQ plane directly.		
	Connector Impedance Matching		
1	• The motherboard designer can put short trace stubs near each connector pin to increase the equivalent capacitance which can help reduce the AGP connector impedance.		
	Trace Bends and Serpentines		
1	• Void 90 degrees bends, instead use two 45 degree bends. Trace bends and serpentines generate coupling causing the line to be shorter electrically.		

15.6 CK 408 Layout Checklist

Table 15-8. CK 408 Layout Checklist (Sheet 1 of 3)

No.	Recommendations	Comments	√
Host Clock: CPU#/CPU			
1	• 7 mils wide.		
2	• Differential pair spacing should be based on a distance from HCLKINN to HCLKINP.		
3	• Spacing to other traces should 4 times to 5 times greater than distance from HCLKINN to HCLKINP.		
4	• Processor routing length- Clock driver to R_S should be 0.5 inch max.		
5	• Processor routing length- R_S to R_S-R_T should be 0 inch to 0.2 inch.		
6	• Processor routing length- R_S-R_T node to R_T should be 0 inch to 0.2 inch.		
7	• Processor routing length- R_S-R_T node to load should be 2 inches to 9 inches.		
8	• MCH routing length- Clock driver to R_S should be 0.5 inch max.		
9	• MCH routing length- R_S to R_S-R_T should be 0.5 inch max.		
10	• MCH routing length- R_S-R_T node to R_T should be 0.0 inch to 0.2 inch max.		
11	• MCH routing length- R_S-R_T node to load should be 2.0 inches to 9.0 inches max.		
12	• Clock driver to processor and clock driver to chipset length matching should be 600 mils.		
13	• 10 mil length matching between HCLKINN to HCLKINP.		
14	• Do not split up the two halves of a differential clock pair between layers.		
15	• Route all agents on the same physical routing layer referenced to ground of the differential clock.		
16	• Make sure that the skew induced by the vias is compensated in the traces to other agents.		
17	• Do not place vias between adjacent complementary clock traces.		
18	• Maintain uniform spacing between the two halves of differential clocks.		
19	• Route clocks on physical layers adjacent to the VSS reference plane only.		

Table 15-8. CK 408 Layout Checklist (Sheet 2 of 3)

No.	Recommendations	Comments	√
	66 MHz Clock Group		
1	• Point-to-point Topology.		
2	• 5 mils wide and 20 mil spacing.		
3	• 20 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 4.0 inches and 8.5 inches.		
6	• The total trace lengths must be matched to ± 100 mils of each other.		
7	• Follow these guidelines when routing to an AGP device down on the motherboard.		
	AGP Clock (when routing to an AGP connector)		
1	• Point-to-point Topology.		
2	• 5 mils wide and 20 mil spacing.		
3	• 20 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length must be 4.0 inches less than the CLK66 total trace lengths ± 100 mils.		
	33 MHz Clock Group		
1	• Point-to-point Topology.		
2	• 5 mils wide and 15 mil spacing.		
3	• 15 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total mismatch between any two 33 MHz clocks must be less than 7.5 inches. If routing to a PCI connector, 2.6 inches of routing on the PCI card must be included in the 7.5 inches total mismatch.		
6	• The 33 MHz clock to the Intel® ICH4 must be matched to ± 100 mils of the 66 MHz clock to the ICH4.		
	14 MHz Clock Group		
1	• Balanced T Topology.		
2	• 5 mils wide and 10 mil spacing.		
3	• 10 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• The total trace length from the Clock driver to SIO and Clock driver must be matched to 0.5 inch.		
6	• Signal must T within 12 inches of the series termination. • Max trace length of stubs is 6 inches.		
7	• Total trace length matched to ± 0.5 inch of each other.		

Table 15-8. CK 408 Layout Checklist (Sheet 3 of 3)

No.	Recommendations	Comments	√
USB Clock			
1	• Point-to-point Topology.		
2	• 5 mils wide.		
3	• 15 mil group spacing.		
4	• Series termination within 0.5 inch of the driver.		
5	• Trace length from series termination to receiver on the motherboard between 3.0 inches and 12 inches.		

15.6.1   CK 408 Decoupling Checklist

Table 15-9. CK 408 Decoupling Checklist

No.	Layout Recommendations	Comments	√
VDDA/VDD Decoupling			
1	• Place one 10 µF capacitor close to the VDD generation circuitry.		
2	• Place six 0.1 µF capacitors close to the VDD pins on the clock driver.		
3	• Place three 0.01 µF capacitors close to the VDDA pins on the clock driver.		
4	• Place one 10 µF bulk decoupling capacitor close to the VDDA generation circuitry.		
5	• Host clock pairs must be differentially routed on the same physical routing layer.		
6	• Differential clocks must not have more than two via transitions.		
7	• Ground referencing is strongly recommended for all platform clocks.		
8	• Motherboard layer transitions and power plane splits must be kept to a minimum.		

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Schematics   *A*

This appendix contains a set of schematics for the Intel® Pentium® 4 processor / Intel® E7205 chipset platform Customer Board (CRB).

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INTEL(R) PENTIUM(R) 4 PROCESSOR- INTEL(R) E7205 CHIPSET CUSTOMER REFERENCE SCHEMATICS

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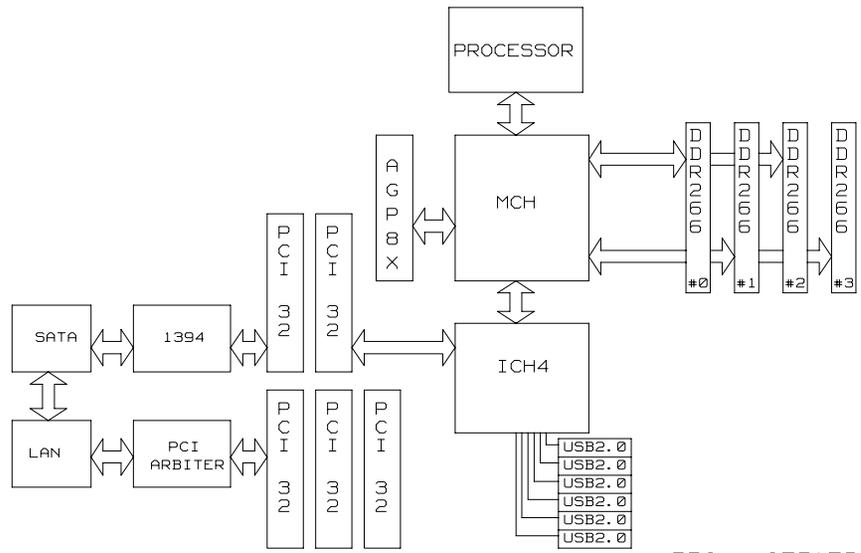
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PROCESSOR

AGP8X

MCH

DDR266 #0 DDR266 #1 DDR266 #2 DDR266 #3

SATA   1394

LAN   PCI ARBITER

PCI 32   PCI 32

ICH4

PCI 32   PCI 32   PCI 32

USB2.0
USB2.0
USB2.0
USB2.0
USB2.0
USB2.0

CR-1

300 WATT POWER SUPPLY CONN	— VREG —

uPGA478
PROCESSOR SOCKET

CK_408 CLOCK

SM BUS

ICH4: I/O

E7205 CHIPSET

PSB

AGP8X PRO50
AGP CONN
SLOT 6

AGP BUS
32-BIT

MCH: MEMORY
CONTROLLER HUB

CHANNEL A

144-BIT
UNBUFFERED DUAL DATA RATE SDRAM
(2-DDR SDRAM DIMMS)

DIMM 0:1

CHANNEL B

144-BIT
UNBUFFERED DUAL DATA RATE SDRAM
(2-DDR SDRAM DIMMS)

DIMM 0:1

VREG
MCH/AGP

ICH4: I/O

SM BUS

ATX FORM FACTOR
SLOT 5 SHARED W/CNR

HUB INTERFACE
HI 1.5, 8-BIT

PCI SLOT 1
PCI SLOT 2
PCI SLOT 3
PCI SLOT 4
PCI SLOT 5

HECETA
HARDWARE
MONITOR

SM BUS

PCI REQ/GNT
ARBITER

ICH4: I/O
CONTROLLER HUB

SM BUS

PRI IDE CONN
SEC IDE CONN

DD BUS

PCI BUS

LAN
CONTROLLER

1394
CONTROLLER

SATA
CONTROLLER

USB

LCI OPTION

RJ45
PORT

1394 PORT
BACK PANEL

SATA PORT
SATA PORT

BACK PANEL
USB PORT 1
USB PORT 2

LPC BUS

1394 SMBUS
EEPROM

1394-SM BUS

1394 PORT
FRONT PANEL

FRONT PANEL

BACK PANEL
USB PORT 3
USB PORT 4

FRONT PANEL
USB PORT 5
USB PORT 6

LCI

ICH4: I/O

SM BUS

CNR RISER
PCI SLOT 5 NEAR BOARD
EDGE SHARED W/CNR

USB PORT 6: CNR OPTION

PORT ANGELES
I/O

FWH
FIRMWARE HUB

TPM
SAFEKEEPER

SM BUS
AC '97 LINK

SM BUS

PORT-80
LEDS

AC '97 AUDIO
CODEC

AMP

MIC IN (3-STACK)

PS2 MOUSE &
KEYBOARD

PARALLEL (1)
SERIAL (1)

FLOPPY DISK
DRIVE CONN

AUX IN (ATAPI)
CD IN (ATAPI)
TELEPHONY (ATAPI)
STEREO LINE OUT (3-STACK)
STEREO LINE IN (3-STACK)

DEBUG PORTS
1X3 & 2X10

ICH4: I/O   SM BUS

BLOCK DIAGRAM

DRAWING
NGRVP.SCH_1.2
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MCH: MEMORY
CONTROLLER HUB
P_PCIRST*   H_CPURST*
PWRGD_3V

H_TRST*   uPGA478 SOCKET
H_CPURST*
H_PWRGD

DBR: FP_RST*

P_PCIRST*
FWH: FIRMWARE HUB
PWRGD_3V

CDC_DOWN_RST*
P_RST_SLOTS*

SIO/GLUE CHIP

P_PCIRST*
AUD_LINK_RST*

FP_RST*
SLP_S5*   PWRGD_3V
SLP_S3*   RSMRST*
PWRGD_PS   IDE_RST*
               KBRST*
               PS_ON*

P_RST_SLOTS*
AGP CONN
1394
P_RST_SLOTS*
SATA
P_RST_SLOTS*
PCI ARB
P_RST_SLOTS*

P_RST_SLOTS*
PCI SLOT 1
PCI SLOT 2
PCI SLOT 3
PCI SLOT 4
PCI SLOT 5

PORT B0
POC HDR
LPC LAI HDR
KBRST*

P_PCIRST*_DEBUG*

P_PCIRST*
BUFFER

P_PCIRST*
BUFFER

P_PCIRST*_LED*
DEBUG LED (YELLOW)

LAN (GBIT)
P_PCIRST*
LAN (10/100)

TPM SAFEKEEPER
P_PCIRST*

EVAL SLOT OPTION
FP_RST*

PUSHBUTTON DBG
FP_RST*

HECETA4 OPTION
FP_RST*

RES (SERIES)

ITP   FP_RST*
H_CPURST*
H_TRST*

PS_ON*
POWER CONNECTOR
PWRGD_PS

PS_ON*
VIDGD OPTION

IDE_RST*
IDE CONN1
IDE CONN2

DIAG-LED
FWH
USB OC FP CNTL
USB OC BPL CNTL
USB OC BPR CNTL

P_PCIRST*
RES (SERIES)
P_PCIRST_ICH*

RES (OPTION)

AC97 AUDIO CODEC
CDC_DOWN_RST*
AUD_LINK_RST*

FRONT PANEL CONN
FP_RST*
SW_ON*

PUSHBUTTON DBG
SW_ON*

CUSTOM FP CONN 1
SW_ON*

CUSTOM FP CONN 2
SW_ON*

H_PWRGD
P_PCIRST*
PWRGD_3V   AUD_LINK_RST*
RSMRST*

ICH: I/O
CONTROLLER HUB
ICH_LAN_RST

SW_ON*   SLP_S4*
KBRST*   SLP_S3*

CNR(SHARED SLOT)
AUD_LINK_RST*
ICH_LAN_RST

RESET MAP

DIMM 1,3

DIMM 0,2

ITP

PROCESSOR

PCI SLOT 1-5

CK_P_33M_SX

CK_M_133_CH_B

CK_M_133_CH_A

CK_H_133M_ITP

CK_H_133M_CPU

CK_P_33M_LAN

LAN
PCI INTERFACE

CK_P_33M_1394

1394

CK_P_33M_SATA

SATA 25 MHZ

CK_H_133M_MCH

CK_P_33M_TPM

TPM SECURITY

MCH

CK_66M_MCH

CK_P_33M_FWH

RESISTOR

LPC HDR

FWH

CK408

CK_G_66M_AGP

AGP CONNECTOR

CK_P_33M_SIO

SIO/GLUE CHIP

14.318 MHZ

CK_48M_ICH_USB

CK_14M_SIO

CK_14M_AUDIO (OPTION)

CK_14M_ICH

AUDIO 24.576MHZ
XTAL 24M (OPTION)

CK_P_33M_ARB

PCI ARBITER

CK_P_33M_ICH

ICH4

32KHZ SUSCLK

PORT 80

1/2

CK_P_66M_PORT80_R

12.288MHZ_BIT CLK

32.768KHZ

5-50 MHZ

CNR

LAN (82562EX/EZ)
(LAN CONNECT INTERFACE)

25 MHZ

CLOCK DISTRIBUTION

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ICH

PIN NAME	POWER WELL	USAGE	AFTER RSMRST	DURING S3/S5	NOTES
GPI[0]	MAIN	P_REQA*	---	---	P/U ON PG 41, 2.7K TO VCC5
GPI[1]	MAIN	P_REQ5*	---	---	P/U ON PG 41, 2.7K TO VCC5, USED ON LAN
GPI[2]	MAIN	P_INTE*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS
GPI[3]	MAIN	P_INTF*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS, SATA
GPI[4]	MAIN	P_INTG*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS
GPI[5]	MAIN	P_INTH*	---	---	P/U ON PG 41, 8.2K TO VCC3, USED ON PCI SLOTS
GPI[6]	MAIN	AGPBUSY-NOT USED	---	---	P/U ON PG 30, 10K TO VCC3 [STRAPPED TOGETHER WITH GP7]
GPI[7]	MAIN	AVAILABLE-NOT USED	---	---	P/U ON PG 30, 10K TO VCC3 [STRAPPED TOGETHER WITH GP6]
GPI[8]	RESUME	CDC_DWN_ENAB*	---	---	P/D ON PG 30, 10K TO GROUND (EMPTY 100K P/U TO 3.3V STBY)
GPI[11]	RESUME	SMB_ALERT-NOT USED	---	---	P/U ON PG 30, 10K TO 3.3VSB
GPI[12]	RESUME	LPC_SIO_SMI*	---	---	P/U ON PG 61, 10K TO 3.3V STBY, USED ON PORT ANGELES IO_SMI/GPIO4
GPI[13]	RESUME	LPC_SIO_PME*	---	---	P/U ON PG 61, 10K TO 3.3V STBY, USED ON PORT ANGELES IO_PME
GPO[16]	MAIN	P_GNTA*	HIGH	OFF	EMPTY P/D ON PG 41, 10K TO GROUND
GPO[17]	MAIN	P_GNT5*	HIGH	OFF	USED ON LAN
GPO[18]	MAIN	STPPCI-NOT USED	HIGH	OFF	
GPO[19]	MAIN	SLP_S1-NOT USED	HIGH	OFF	
GPO[20]	MAIN	STPCPU-NOT USED	HIGH	OFF	
GPO[21]	MAIN	C3_STAT-NOT USED	HIGH	OFF	
GPO[22]	MAIN	CPU_PERF-NOT USED	HI-Z	OFF	P/U ON PG 30, 10K TO VCC3 (O/D OUTPUT)
GPO[23]	MAIN	GMUXSEL-NOT USED	LOW	OFF	
GPIO[24]	RESUME	CLK_RUN-NOT USED	LOW	DEFINED	
GPIO[25]	RESUME	GPIO_GRN_BLNK- NOT USED	HIGH	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE
GPIO[27]	RESUME	GPIO_YLW_BLNK- NOT USED	HIGH	DEFINED	GPIO 25, 27, 28 ARE BLINK CAPABLE
GPIO[28]	RESUME	GPIO_LAN_DISABLE/EMAIL_LED	HIGH	DEFINED	P/D ON PAGE 27, 10K TO GROUND, GPIO 25, 27, 28 ARE BLINK CAPABLE
GPIO[32]	MAIN	GPIO_MUTE_AUDIO-NOT USED	---	---	
GPIO[33]	MAIN	GPIO_AUD_EN- NOT USED	---	---	
GPIO[36]	MAIN	AVAILABLE-NOT USED	---	---	
GPIO[37]	MAIN	BOARD_SKU0	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)
GPIO[38]	MAIN	BOARD_SKU1	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)
GPIO[39]	MAIN	BOARD_SKU2	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)
GPIO[40]	MAIN	BOARD_SKU3	---	---	P/D ON PAGE 30, 10K TO GROUND (EMPTY 10K P/U TO VCC3)
GPIO[41]	MAIN	AGPPRO_PRESENT1	---	---	CONNECTED TO AGPPRO CONNECTOR
GPIO[42]	MAIN	AGPPRO_PRESENT2	---	---	CONNECTED TO AGPPRO CONNECTOR
GPIO[43]	MAIN	RSVD-BOARD_SKU4	---	---	P/D ON PAGE 30, 10K P/U TO VCC3 (EMPTY 10K TO GND)

FMH

PIN NAME	POWER WELL	USAGE	AFTER RSMRST	DURING S3/S5	NOTES
GPI0		GPIO_DMA66_DETECT_PRI	INPUT	DEFINED	P/D ON PAGE 32, 15K TO GROUND
GPI1		GPIO_DMA66_DETECT_SEC	INPUT	DEFINED	P/D ON PAGE 32, 15K TO GROUND
GPI2		AVAILABLE-NOT USED	INPUT	DEFINED	P/D ON PAGE 66, 10K TO GROUND (EMPTY 10K P/U TO VCC3): COM2 DETECT IF P-UP
GPI3		MANUFACTURING MODE	INPUT	DEFINED	P/U ON PAGE 66, 4.7K TO VCC3 (EMPTY PAD-SITE TO ALLOW ICT PROBE)
GPI4		NORMAL/CONFIG/RECOVERY BIOS	INPUT	DEFINED	P/D ON PAGE 66, 4.7K TO GROUND (HEADER TO ALLOW 1K P/U TO VCC3)

SIO/GLUE

PIN NAME	POWER WELL	USAGE	AFTER RSMRST	DURING S3/S5	NOTES
GPIO0		FAN1_CTRL (TRISTATE @PWRGD)	---	OUTPUT	PAGE 68-72; DESIGN FEATURE WITH EMPTY P/U, EMPTY FET FOR FAN EXP.
GPIO1		FAN2_CTRL (TRISTATE @PWRGD)	---	OUTPUT	P/U ON PG 72, 1K TO VCC3
GPIO2		DIAGLED-DATA- RESISTOR CFG OPTION	---	OUTPUT	PAGE 96-92; DESIGN FEATURE WITH P/U, P/D RESISTOR STRAPPING
GPIO3		DIAGLED-STB- RESISTOR CFG OPTION	---	OUTPUT	PAGE 96-92; DESIGN FEATURE WITH P/U, P/D RESISTOR STRAPPING
GPIO4		IO_SMI* (TRISTATE @PWRGD)	---	OUTPUT	P/U ON PG 61, 10K TO 3.3V STBY, USED ON ICH IO_SMI/GPI12
GPIO5		AVAILABLE-NOT USED (TRISTATE@PWR)	---	OUTPUT	EMPTY P/U, P/D PAGE 61; OPTION FOR FORCING SIO ADDRESS SELECT
IO/PME*		IO_PME* (INACTIVE @ PWRGD)	---	OUTPUT	P/U ON PG 61, 10K TO 3.3V STBY, USED ON ICH IO_PME/GPI13
GPIO6, 7		FAN_TACH1 & 2, (TRISTATE @PWRGD)	---	INPUT	PAGE 72; 10K PULL-UP TO 12V (THROUGH A VOLTAGE DIVIDER)

IRQ ROUTING TABLE

ICH SIGNALS	AGP	SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	ICH4 AC97,SMBUS	ICH4 LAN	ICH4 USB #1	ICH4 USB #2	ICH4 USB #3	ICH4 USB 2.0	KENAI LAVON LAN	SATA	1394
P_INTA*	IRQA			IRQD		IRQC				X						
P_INTB*	IRQB			IRQC		IRQA	N/A	X								IRQA
P_INTC*				IRQA	IRQB							X		IRQA		
P_INTD*				IRQB	IRQA						X					
P_INTE*		IRQD	IRQC			IRQD			X							
P_INTF*		IRQA	IRQB		IRQC										IRQA	
P_INTG*		IRQB	IRQA		IRQD											
P_INTH*		IRQC	IRQD			IRQB							X			
REQ/GNT	0	1		ARB-2	ARB-3	ARB-4	N/A		5					5	4	3
IDSEL		16	17	18	19	20	N/A		24					21	22	23

GPIO / IRQ / IDSEL

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J1E1 A16104-006
478 PIN SOCKET

J1E1 A16104-006
478 PIN SOCKET

J1E1 A16104-006
478 PIN SOCKET
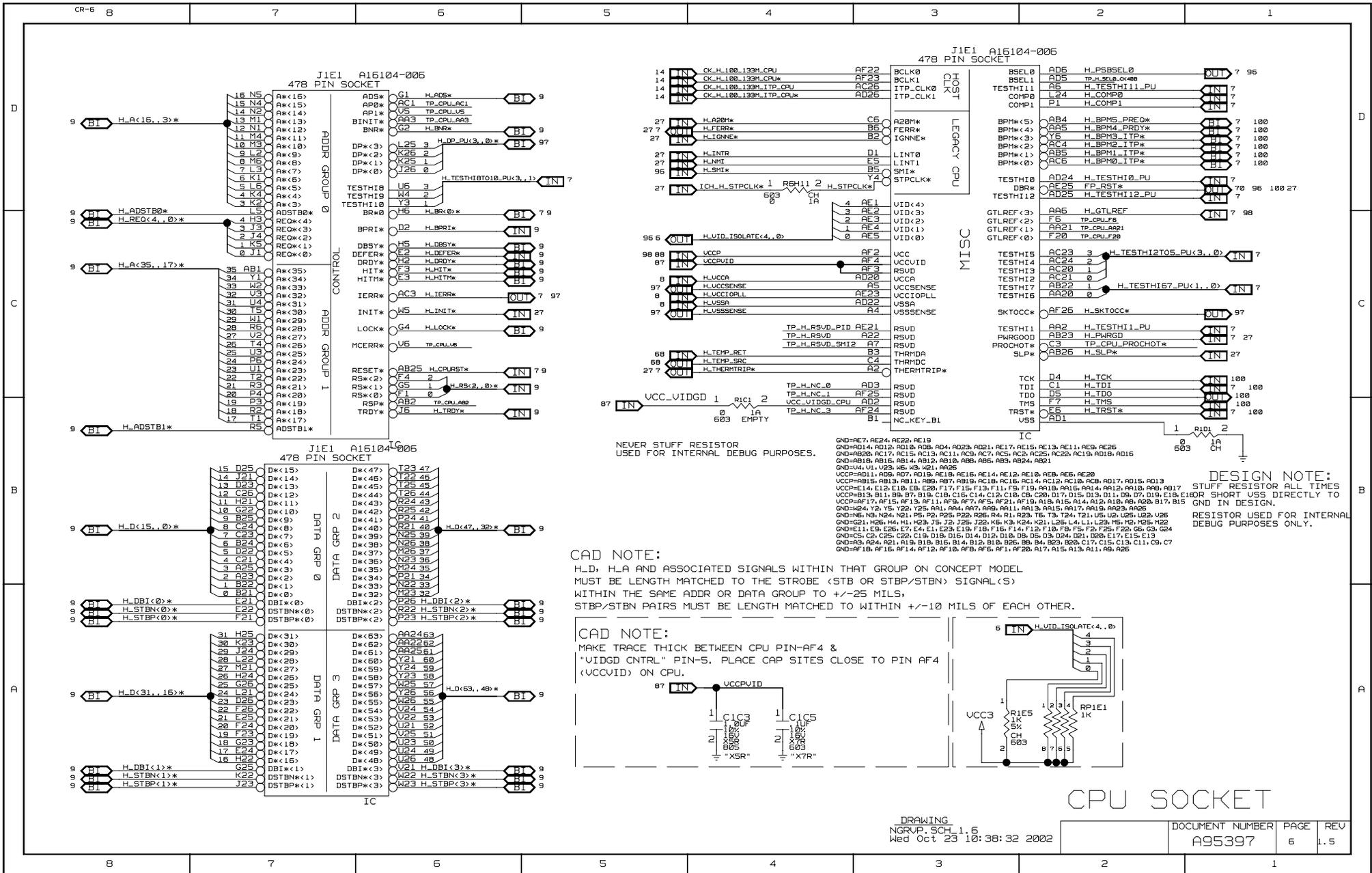
NEVER STUFF RESISTOR
USED FOR INTERNAL DEBUG PURPOSES.

VCC_VIDGD

DESIGN NOTE:
STUFF RESISTOR ALL TIMES
SHORT VSS DIRECTLY TO
GND IN DESIGN.

RESISTOR USED FOR INTERNAL
DEBUG PURPOSES ONLY.

CAD NOTE:
H_D, H_A AND ASSOCIATED SIGNALS WITHIN THAT GROUP ON CONCEPT MODEL
MUST BE LENGTH MATCHED TO THE STROBE (STB OR STBP/STBN) SIGNAL(S)
WITHIN THE SAME ADDR OR DATA GROUP TO +/-25 MILS,
STBP/STBN PAIRS MUST BE LENGTH MATCHED TO WITHIN +/-10 MILS OF EACH OTHER.

CAD NOTE:
MAKE TRACE THICK BETWEEN CPU PIN-AF4 &
"VIDGD CNTRL" PIN-5. PLACE CAP SITES CLOSE TO PIN AF4
(VCCVID) ON CPU.

CPU SOCKET

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CPU SIGNAL TERMINATION

98 88 IN VCCP

ITP/TAP TERMINATION

98 88 IN VCCP

CAD NOTE:
PLACE @ CPU END OF ROUTE

CAD NOTE:
PLACE @ ICH END OF ROUTE

CAD NOTE:
PLACE @ CPU END OF ROUTE

R1C10
49.9
1%
CH
603

R1E4
150
5%
CH
603

R3C1
301
1%
CH
603

R5G1
62
5%
CH
603

R5G2
62
5%
CH
603

R1D12
62
5%
CH
603

RP1C1 S1 5% .063W IC SM
RP1C1 S1 5% .063W IC SM
RP1D1 S1 5% .063W IC SM
RP1D1 S1 5% .063W IC SM
RP1D1 S1 5% .063W IC SM
RP1D1 S1 5% .063W IC SM

R1D10
5%
CH
603

R1D9
680
5%
CH
603

H_IERR* OUT 6 97
H_THERMTRIP* OUT 6 27
H_FERR* OUT 6 27
H_PWRGD OUT 27 6
H_BR<0>* OUT 6 9
H_CPURST* OUT 9 6 97 100

H_BPM5_PREQ* OUT 6 100
H_BPM4_PRDY* OUT 6 100
H_BPM3_ITP* OUT 6 100
H_BPM2_ITP* OUT 6 100
H_BPM1_ITP* OUT 6 100
H_BPM0_ITP* OUT 6 100
H_TDI OUT 100 6
H_TRST* OUT 100 6

CAD NOTE:
PLACE THESE RESISTORS CLOSE TO THE CPU SOCKET

TESTHI PULLUPS

98 88 IN VCCP

RP1D2 RP1D2 RP1D2 RP3D1 RP3D1 RP3C1 RP3C1 RP3C1 RP3C1 RP3D1
S1 S1 S1 S1 S1 S1 S1 S1 S1 S1
5% 5% 5% 5% 5% 5% 5% 5% 5% 5%
.063W .063W .063W .063W .063W .063W .063W .063W .063W .063W
IC IC IC IC IC IC IC IC IC IC
SM SM SM SM SM SM SM SM SM SM

R3C2
49.9
1%
CH
603

R1E2
49.9
1%
CH
603

H_TESTHI0_PU OUT 6
H_TESTHI2_PU OUT 6
H_TESTHI67_PU<1,.0> OUT 6
H_TESTHI2TO5_PU<3,.0> OUT 6
H_TESTHI8TO10_PU<3,.1> OUT 6
H_TESTHI1_PU OUT 6
H_TESTHI11_PU OUT 6

THESE MAY BE COST-REDUCED FOR PRODUCTION BY GROUPING [10:8], [7:2], AND [1:0] TO ONE PULLUP PER GROUP

14 IN VCC3_CLK

R5B2
1k
5%
CH
603

DESIGN NOTE:
ALWAYS STUFF

H_PSBSEL0 OUT 6 96

PRECISION FSB COMPENSATION RESISTORS
202286-068

R1D13
49.9 1%
603 CH

H_COMP1 OUT 6

R3D2
49.9 1%
603 CH

H_COMP0 OUT 6

CAD NOTE:
PLACE THESE OUTSIDE SOCKET CAVITY

SPARE

RP3D1 S1 5% .063W IC SM TP_SPARE_CPU_51_3
RP1C1 S1 5% .063W IC SM TP_SPARE_CPU_51_4
RP1C1 S1 5% .063W IC SM TP_SPARE_CPU_51_6 TP_SPARE_CPU_51_5

GTLREF GENERATION CIRCUIT

98 88 IN VCCP

202286-068
R1D3
49.9 1%
603 CH

H_GTLREF OUT 98 6

R1D5
100
1%
CH
603
202286-097

C1D1
1UF
10V
X5R
805

C1D2
.01UF
50V
X7R
603

CAD NOTE:
PLACE CAPS CLOSE TO GTL REF PIN OF MCH

CPU TERMINATION

PLL SUPPLY FILTER

98 88 IN VCCP

721891-009
L2C1
10UH   "60 MA"
IND   "0805"

644056-008
C2C14
22.0U 20%
6.3V
X5R
1210   H_VSSA   OUT 8 6

H_VCCA   OUT 6

1   R2C1   2
Ø   1A
603   CH

DESIGN NOTE:
EXPERIMENT TO REDUCE DESIGN BY
BY (1) CAP.

98 88 IN VCCP

721891-009
L3C1
10UH   "60 MA"
IND   "0805"

644056-008
C2C13
22.0U 20%
6.3V
EMPTY
1210   H_VSSA   OUT 8 6

H_VCCIOPLL   OUT 6

CAD NOTE:
PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET

TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MIL

CPU PLL FILTERS

MCH

DRAWING
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M_DATA_A<63..0> BI 17 18

M_DATA_B<63..0> BI 22 23

U5C1
E7205 MCH
CHANNEL A

U5C1
E7205 MCH
CHANNEL B

CHANNEL A:

63	AE12	DQ_A63	
62	AG11	DQ_A62	
61	AJ10	DQ_A61	
60	AH11	DQ_A60	
59	AE11	DQ_A59	
58	AF12	DQ_A58	
57	AH10	DQ_A57	
56	AG12	DQ_A56	
55	AG14	DQ_A55	
54	AJ13	DQ_A54	
53	AK14	DQ_A53	
52	AK15	DQ_A52	
51	AE14	DQ_A51	
50	AG15	DQ_A50	
49	AF15	DQ_A49	
48	AE15	DQ_A48	
47	AE17	DQ_A47	
46	AG17	DQ_A46	
45	AK20	DQ_A45	
44	AF18	DQ_A44	
43	AH17	DQ_A43	
42	AJ18	DQ_A42	
41	AJ19	DQ_A41	
40	AE18	DQ_A40	
39	AJ22	DQ_A39	
38	AH22	DQ_A38	
37	AJ24	DQ_A37	
36	AJ25	DQ_A36	
35	AG21	DQ_A35	
34	AH23	DQ_A34	
33	AE20	DQ_A33	
32	AE21	DQ_A32	
31	AE29	DQ_A31	
30	AC27	DQ_A30	
29	AB26	DQ_A29	
28	AA26	DQ_A28	
27	AD29	DQ_A27	
26	AC28	DQ_A26	
25	AB25	DQ_A25	
24	AA25	DQ_A24	
23	W28	DQ_A23	
22	W26	DQ_A22	
21	U28	DQ_A21	
20	V25	DQ_A20	
19	W29	DQ_A19	
18	W25	DQ_A18	
17	U27	DQ_A17	
16	V26	DQ_A16	
15	P28	DQ_A15	
14	P27	DQ_A14	
13	M29	DQ_A13	
12	T25	DQ_A12	
11	R27	DQ_A11	
10	R26	DQ_A10	
9	R25	DQ_A9	
8	P25	DQ_A8	
7	M26	DQ_A7	
6	K28	DQ_A6	
5	G29	DQ_A5	
4	M25	DQ_A4	
3	L27	DQ_A3	
2	J29	DQ_A2	
1	J27	DQ_A1	
0	L25	DQ_A0	

RSVD — AH29 TP_MCH_AH29
RSVD — AJ9 TP_MCH_AJ9
RSVD — AH14 TP_MCH_AH14
RSVD — AH19 TP_MCH_AH19
RSVD — AG23 TP_MCH_AG23
RSVD — AB28 TP_MCH_AB28
RSVD — V27 TP_MCH_V27
RSVD — N28 TP_MCH_N28
RSVD — H28 TP_MCH_H28

DQS_A8 — AH28 8
DQS_A7 — AK8 7
DQS_A6 — AJ15 6
DQS_A5 — AG18 5
DQS_A4 — AF21 4
DQS_A3 — AB29 3
DQS_A2 — V29 2
DQS_A1 — N29 1
DQS_A0 — K26 0   M_DQS_A<8..0> BI 17 19

CMDCLK_A7 — AJ6 CK_M_133M_P_DDR7_A OUT 17
CMDCLK_A7 — AJ7 CK_M_133M_N_DDR7_A 17
CMDCLK_A6 — AG8 CK_M_133M_P_DDR6_A 17
CMDCLK_A6 — AG9 CK_M_133M_N_DDR6_A 17
CMDCLK_A5 — D31 CK_M_133M_P_DDR5_A 17
CMDCLK_A5 — D32 CK_M_133M_N_DDR5_A 17
CMDCLK_A4 — K25 CK_M_133M_P_DDR4_A 17
CMDCLK_A4 — J26 CK_M_133M_N_DDR4_A 17
RSVD — AF19 TP_MCH_AF19
RSVD — AE19 TP_MCH_AE19
RSVD — AK21 TP_MCH_AK21
RSVD — AJ21 TP_MCH_AJ21
CMDCLK_A1 — AE22 CK_M_133M_P_DDR1_A OUT 17
CMDCLK_A1 — AF22 CK_M_133M_N_DDR1_A 17
CMDCLK_A0 — AF24 CK_M_133M_P_DDR0_A 17
CMDCLK_A0 — AG24 CK_M_133M_N_DDR0_A 17

CKE_A3 — K31 3
CKE_A2 — N26 2
CKE_A1 — J33 1
CKE_A0 — K29 0   M_SCKE_A<3..0> OUT 17 19

RSVD — AM9 TP_MCH_AM9
MA_A12 — P33 12
MA_A11 — R32 11
MA_A10 — AM22 10
MA_A9 — R30 9
MA_A8 — W27 8
MA_A7 — T29 7
MA_A6 — AA32 6
MA_A5 — Y30 5
MA_A4 — AA30 4
MA_A3 — AC24 3
MA_A2 — AD26 2
MA_A1 — AG30 1
MA_A0 — AH25 0   M_MAA_A<12..0> OUT 17 18

BA_A1 — AH20 1
BA_A0 — AE16 0   M_BS_A<1..0> OUT 17 19

CAS_A — AN14 M_CAS_A* OUT 17 19
RAS_A — AL16 M_RAS_A* OUT 17 19
WE_A — AM15   M_WE_A*   OUT 17 19

CS_A3 — AF9 3
CS_A2 — AF10 2
CS_A1 — AJ12 1
CS_A0 — AF13 0   M_SCS_A<3..0>* OUT 17 19

RCVENOUT_A — AH31 RCVENOUT_A* IN 13

DRCOMPVREF_H — AK32 DRCOMPVREF_H_V IN 13
DRCOMPVREF_V — AJ31

ODTCOMP — AG33 ODTCOMP IN 13

DRCOMP_H — AK33 DRCOMP_H IN 13
DRCOMP_V — AJ33 DRCOMP_V IN 13

18 17 BI M_DATA_CB_A<7..0>

CB_A7 — AF25
CB_A6 — AG26
CB_A5 — AE24
CB_A4 — AE26
CB_A3 — AE23
CB_A2 — AG27
CB_A1 — AE27
CB_A0 — AF27

98 13 IN V1P25_MCH_VREF_A AG32 VREF_A

98 78 IN V_2P5_SM L24 DDR_STRAP

IC

CHANNEL B:

63	AM3	DQ_B63	
62	AL4	DQ_B62	
61	AM6	DQ_B61	
60	AL8	DQ_B60	
59	AN3	DQ_B59	
58	AM4	DQ_B58	
57	AL7	DQ_B57	
56	AM7	DQ_B56	
55	AN9	DQ_B55	
54	AN11	DQ_B54	
53	AN12	DQ_B53	
52	AL14	DQ_B52	
51	AM10	DQ_B51	
50	AL11	DQ_B50	
49	AM13	DQ_B49	
48	AL13	DQ_B48	
47	AM17	DQ_B47	
46	AM18	DQ_B46	
45	AL18	DQ_B45	
44	AN20	DQ_B44	
43	AM18	DQ_B43	
42	AN18	DQ_B42	
41	AM19	DQ_B41	
40	AN21	DQ_B40	
39	AK23	DQ_B39	
38	AK26	DQ_B38	
37	AK26	DQ_B37	
36	AL23	DQ_B36	
35	AL23	DQ_B35	
34	AN24	DQ_B34	
33	AM25	DQ_B33	
32	AL26	DQ_B32	
31	AE31	DQ_B31	
30	AD32	DQ_B30	
29	AB32	DQ_B29	
28	AB31	DQ_B28	
27	AF32	DQ_B27	
26	AD30	DQ_B26	
25	AC31	DQ_B25	
24	AC33	DQ_B24	
23	W31	DQ_B23	
22	V30	DQ_B22	
21	U31	DQ_B21	
20	T32	DQ_B20	
19	Y33	DQ_B19	
18	W32	DQ_B18	
17	U30	DQ_B17	
16	U33	DQ_B16	
15	N31	DQ_B15	
14	N32	DQ_B14	
13	M33	DQ_B13	
12	K32	DQ_B12	
11	P30	DQ_B11	
10	P31	DQ_B10	
9	L31	DQ_B9	
8	L33	DQ_B8	
7	H31	DQ_B7	
6	H30	DQ_B6	
5	F30	DQ_B5	
4	G33	DQ_B4	
3	H33	DQ_B3	
2	G32	DQ_B2	
1	F32	DQ_B1	
0	E31	DQ_B0	

RSVD — AN29 TP_MCH_AN29
RSVD — AN5 TP_MCH_AN5
RSVD — AK12 TP_MCH_AK12
RSVD — AL19 TP_MCH_AL19
RSVD — AL25 TP_MCH_AL25
RSVD — AD33 TP_MCH_AD33
RSVD — V33 TP_MCH_V33
RSVD — M32 TP_MCH_M32
RSVD — F33 TP_MCH_F33

DQS_B8 — AK29 8
DQS_B7 — AL5 7
DQS_B6 — AM12 6
DQS_B5 — AK16 5
DQS_B4 — AM24 4
DQS_B3 — AC30 3
DQS_B2 — V32 2
DQS_B1 — M30 1
DQS_B0 — G31 0   M_DQS_B<8..0> BI 22 24

CMDCLK_B7 — AK5 CK_M_133M_P_DDR7_B OUT 22
CMDCLK_B7 — AH7 CK_M_133M_N_DDR7_B 22
CMDCLK_B6 — AH8 CK_M_133M_P_DDR6_B 22
CMDCLK_B6 — C32 CK_M_133M_N_DDR6_B 22
CMDCLK_B5 — C33 CK_M_133M_P_DDR5_B 22
CMDCLK_B5 — H27 CK_M_133M_N_DDR5_B 22
CMDCLK_B4 — G28 CK_M_133M_P_DDR4_B 22
CMDCLK_B4 — ... CK_M_133M_N_DDR4_B 22
RSVD — AC25 TP_MCH_AC25
RSVD — AD25 TP_MCH_AD25
RSVD — AF31 TP_MCH_AF31
RSVD — AF30 TP_MCH_AF30
CMDCLK_B1 — AJ27 CK_M_133M_P_DDR1_B OUT 22
CMDCLK_B1 — AJ28 CK_M_133M_N_DDR1_B 22
CMDCLK_B0 — AN27 CK_M_133M_P_DDR0_B 22
CMDCLK_B0 — AM27 CK_M_133M_N_DDR0_B 22

CKE_B3 — J30 3
CKE_B2 — N25 2
CKE_B1 — J32 1
CKE_B0 — L28 0   M_SCKE_B<3..0> OUT 22 24

RSVD — AN8 TP_MCH_AN8
MA_B12 — R29 12
MA_B11 — R33 11
MA_B10 — AL22 10
MA_B9 — T31 9
MA_B8 — Y28 8
MA_B7 — T28 7
MA_B6 — AA33 6
MA_B5 — Y31 5
MA_B4 — AA29 4
MA_B3 — AD27 3
MA_B2 — AE28 2
MA_B1 — AG29 1
MA_B0 — AN23 0   M_MAA_B<12..0> OUT 22 23

BA_B1 — AG20 1
BA_B0 — AF16 0   M_BS_B<1..0> OUT 22 24

CAS_B — AE13 M_CAS_B* OUT 22 24
RAS_B — AM16 M_RAS_B* OUT 22 24
WE_B — AN15   M_WE_B*   OUT 22 24

CS_B3 — AK9 3
CS_B2 — AE10 2
CS_B1 — AK11 1
CS_B0 — AH13 0   M_SCS_B<3..0>* OUT 22 24

RCVENOUT_B — AH32 RCVENOUT_B* IN 13

23 22 BI M_DATA_CB_B<7..0>

CB_B7 — AK27
CB_B6 — AL28
CB_B5 — AK30
CB_B4 — AJ30
CB_B3 — AM28
CB_B2 — AL29
CB_B1 — AM30
CB_B0 — ...

13 IN V1P25_MCH_VREF_B AF33 VREF_B

IC

MCH

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L5C1
.1UH
98 86 [IN] V_1P3_CORE 1 ~~~ 2   VCCAFSB [OUT] 11
"250 MA"   IND
"0805"   721891-004
C5C8   202341-002
100UF   1   C5C15
20%   .1UF
6.0V   20%
TANT   25V
7343 "644502-001"   Y5V
603

L5C2
.1UH
98 86 [IN] V_1P3_CORE 1 ~~~ 2   VCCAHI [OUT] 11
"250 MA"   IND
"0805"   721891-004
C5C10   202341-002
100UF   1   C5C14
20%   .1UF
6.0V   20%
TANT   25V
7343 "644502-001"   Y5V
603

98 78 [IN] V_2P5_SM

U5C1
E7205 MCH
POWER

98 86 [IN] V_1P3_CORE

Pin	Signal		Signal	Pin
P14	VCC		VCCDDR	B32
P18	VCC		VCCDDR	D30
R15	VCC		VCCDDR	F28
R17	VCC		VCCDDR	H26
R19	VCC		VCCDDR	H32
T14	VCC		VCCDDR	K24
T16	VCC		VCCDDR	K30
T18	VCC		VCCDDR	L23
U17	VCC		VCCDDR	M24
U19	VCC		VCCDDR	M28
V14	VCC		VCCDDR	N23
V16	VCC		VCCDDR	P24
V18	VCC		VCCDDR	P26
W15	VCC		VCCDDR	P32
W17	VCC		VCCDDR	R23
W19	VCC		VCCDDR	T24
P20	VCC		VCCDDR	T30
T20	VCC		VCCDDR	U23
V20	VCC		VCCDDR	V24
Y14	VCC		VCCDDR	V28
Y16	VCC		VCCDDR	Y24
Y18	VCC		VCCDDR	Y26
Y20	VCC		VCCDDR	Y32

U5C1
E7205 MCH
HUB INTERFACE

13 [IN] HI_AVSWING   AD2   PSWNG_A   RSVD   J21   MCH_J21_PU [IN] 13
98 13 [IN] HI_AVREF   AE1   PREF_A   RSVD   J20   MCH_J20_PU [IN] 13
13 [IN] HI_ARCOMP   AC1   PRCOMP_A
PWRGD   J23   PWRGD_3V [IN] 67
11   AA6   HI_A11
10   AC6   HI_A10
9   AE2   HI_A9   RSVD   Y11   TP_MCH_Y11
29 [B1] HI<11..0>   8   AB7   HI_A8   RSVD   W11   TP_MCH_W11
7   AA9   HI_A7
6   AB8   HI_A6   XORMODE ◯ G1   XORMODE* [IN] 13
5   AA8   HI_A5
4   AC7   HI_A4   VSS   G2
3   AC4   HI_A3   TESTSIG2   R6   TP_TESTSIG2
2   AD3   HI_A2   TESTSIG1   R5   TP_TESTSIG1
1   AC3   HI_A1
0   AB4   HI_A0

29 [B1] HI_STBF   AD5   PSTRBF_0
29 [B1] HI_STBS   AB5   PSTRBS_0

13 [IN] TESTSIG4   AJ4   TESTSIG4
13 [IN] TESTSIG3   AG6   TESTSIG3
TP_MCH_AF7   AF7   RSVD
TP_MCH_AL2   AL2   RSVD
TP_MCH_AF6   AF6   RSVD
TP_MCH_AG3   AG3   RSVD
TP_MCH_AG5   AG5   RSVD
TP_MCH_AF4   AF4   RSVD
TP_MCH_AK3   AK3   RSVD
TP_MCH_AL1   AL1   RSVD
TP_MCH_AJ3   AJ3   RSVD
TP_MCH_AK2   AK2   RSVD
TP_MCH_AJ1   AJ1   RSVD
TP_MCH_AH1   AH1   RSVD
TP_MCH_AH2   AH2   RSVD
TP_MCH_AD9   AD9   RSVD
TP_MCH_AF1   AF1   RSVD
TP_MCH_AF3   AF3   RSVD
TP_MCH_AE5   AE5   RSVD
TP_MCH_AE7   AE7   RSVD
TP_MCH_AD6   AD6   RSVD
TP_MCH_AC9   AC9   RSVD
TP_MCH_AG2   AG2   RSVD
TP_MCH_AD8   AD8   RSVD

TP_MCH_AE4   AE4   RSVD
TP_MCH_AE8   AE8   RSVD
TP_MCH_AH4   AH4   RSVD
TP_MCH_AH5   AH5   RSVD

IC

11 [IN] VCCAFSB   P16   VCCAFSB
11 [IN] VCCAHI   U15   VCCAHI

98 87 [IN] V_1P5_CORE

Pin	Signal		Signal	Pin
L2	VCCAGP		VCCDDR	AA23
L8	VCCAGP		VCCDDR	AB24
M4	VCCAGP		VCCDDR	AB30
M10	VCCAGP		VCCDDR	AC13
N6	VCCAGP		VCCDDR	AC15
N11	VCCAGP		VCCDDR	AC17
P10	VCCAGP		VCCDDR	AC19
R11	VCCAGP		VCCDDR	AC21
T10	VCCAGP		VCCDDR	AC23
U2	VCCAGP		VCCDDR	AD12
U8	VCCAGP		VCCDDR	AD14
U11	VCCAGP		VCCDDR	AD16
V4	VCCAGP		VCCDDR	AD18
V10	VCCAGP		VCCDDR	AD20
W6	VCCAGP		VCCDDR	AD22
			VCCDDR	AD24
			VCCDDR	AD28

98 86 [IN] V_1P3_CORE

Pin	Signal		Signal	Pin
Y10	VCC		VCCDDR	AF11
AA11	VCC		VCCDDR	AF17
AB6	VCC		VCCDDR	AF23
AB10	VCC		VCCDDR	AF32
AC2	VCC		VCCDDR	AH9
AC11	VCC		VCCDDR	AH15
AD4	VCC		VCCDDR	AH21
AD10	VCC		VCCDDR	AH27
AE6	VCC		VCCDDR	AH30
AG4	VCC		VCCDDR	AK7
AJ2	VCC		VCCDDR	AK13
			VCCDDR	AK19
			VCCDDR	AK25
			VCCDDR	AK31
			VCCDDR	AL32
			VCCDDR	AM5
			VCCDDR	AM11
			VCCDDR	AM17
			VCCDDR	AM23
			VCCDDR	AM29
			VCCDDR	AM31

IC

MCH

CORE_MCH_POWER_GROUND

MCH

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NGRVP.SCH_1.12
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MCH HEATSINK RETENTION
ANCHOR CLIPS: QTY(4)
J5C3 J5E3 J4C3 J4E1

HDR HDR HDR HDR
A13494-005

VCCP
98 88 IN

CAD NOTE:
HYSWING VOLTAGE "10MIL TRACE, 7MIL SPACE"
DESIGN NOTE: HYSWING S/B 1/3*VCCP +/- 2%

HYSWING OUT 98 9

VCCP
98 88 IN

CAD NOTE:
HXSWING VOLTAGE "10MIL TRACE, 7MIL SPACE"
DESIGN NOTE: HXSWING S/B 1/3*VCCP +/- 2%

HXSWING OUT 98 9

V_1P3_CORE
98 86 IN

HI_AVSWING OUT 11

HI_AVREF OUT 98 11

CAD NOTES:
PLACE 0.01UF CAP WITHIN 0.25" OF
DEVICE PIN (MCH, ICH, AGP)
PLACE 0.1UF CAP CLOSE TO RESISTOR CIRCUIT

V_2P5_SM
98 78 IN

V1P25_MCH_VREF_A OUT 98 10

CAD NOTES:
PLACE 0.01UF CAP WITHIN 0.25" OF
DEVICE PIN (MCH, ICH, AGP)

V_2P5_SM
98 78 IN

V1P25_MCH_VREF_B OUT 10

CAD NOTES:
PLACE 0.1UF CAP CLOSE TO MCH

CAD NOTES:
PLACE 0.1UF CAP CLOSE TO MCH

V_2P5_SM
98 78 IN

SYSTEM MEMORY DECOUPLING

V_1P5_CORE
98 87 IN

AGP_PSWING OUT 9

AGPREF OUT 98 9 15

GC_DET_REF 15 IN

CAD NOTES:
PLACE 0.01UF CAP WITHIN 0.25" OF
DEVICE PIN (MCH, ICH, AGP)
PLACE 0.1UF CAP CLOSE TO RESISTOR CIRCUIT

V_1P3_CORE
98 86 IN
TESTSIG4 OUT 11

V_1P3_CORE
98 86 IN
TESTSIG3 OUT 11

VOLTAGE DIVIDER: 2/3 OUTPUT

V_2P5_SM
98 78 IN
DRCOMPUREF_H_V OUT 10

V_2P5_SM
98 78 IN
RCVENOUT_A* OUT 10

V_2P5_SM
98 78 IN
RCVENOUT_B* OUT 10

V_2P5_SM
98 78 IN
V_2P5_SM
"XSR" "XSR"

V_1P5_CORE
98 87 IN

V_1P3_CORE
98 86 IN

VCCP
98 88 IN

V_2P5_SM
98 78 IN

CAD NOTES:
PLACE NEAR DIMMS

VCCP
98 88 IN

MCH_GTLREF OUT 98 9 94

CAD NOTES:
CAP FOR GTLREF INPUTS @MCH
USE 10MIL TRACE, ISOLATE W/ 7MIL SPACE
CAP SHOULD BE PLACED NEAR MCH PIN

VCC3 MCH_J21_PU OUT 11
VCC3 MCH_J20_PU OUT 11
VCC3 MCH_TEST* OUT 9
VCC3 XORMODE* OUT 11

V_1P3_CORE
98 86 IN
HI_ARCOMP OUT 11

V_1P5_CORE
98 87 IN
MCH_AGP_RCOMP1 OUT 9

MCH_AGP_RCOMP0 OUT 9

HYRCOMP OUT 9
HXRCOMP OUT 9
DRCOMP_H OUT 10
DRCOMP_V OUT 10
ODTCOMP OUT 10

MCH TERMINATION

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CLOCK

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AGP PRO CONNECTOR

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NGRVP.SCH_1.16
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DDR CHANNEL A — DIMM 2

SMB ADDRESS
10100100
SPD=A4

A74893-001

DDR CHANNEL A — DIMM 0

SMB ADDRESS
10100000
SPD=A0

CAD NOTE:
PLACE NEAR DIMM, PIN-1

CAD NOTE:
PLACE RES
DIVIDER
NEAR DIMMS

CAD NOTE:
PLACE NEAR DIMM, PIN-1

CH A DDR DIMMS

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DDR RESISTOR TERMINATION

CH A DDR DATA TERMINATION

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V_1P25_MEMVTT

RP3H3
RP5H2
RP4H2
RP4H4
RP3H1
RP2H1
RP2H4
RP2H7
RP1H1

M_DQS_A<8..0>

M_RAS_A*

M_CAS_A*

M_WE_A*

M_BS_A<1..0>

R3H1
RP3G2

M_SCS_A<3..0>*

RP4G8
RP4G8
RP4H6
RP4H6

M_SCKE_A<3..0>

RP2G8
RP2G7
RP2G8
RP2H6

CH A DDR CONTROL TERMINATION

8   7   6   5   4   3   2   1

98 79 IN V_1P25_MEMVTT

+ 1 C1H5
470UF
20%
10V
ALUM
2 RDL
"202008-016"

CAD NOTE:
PLACE AT RIGHT
END OF VTT ISLAND
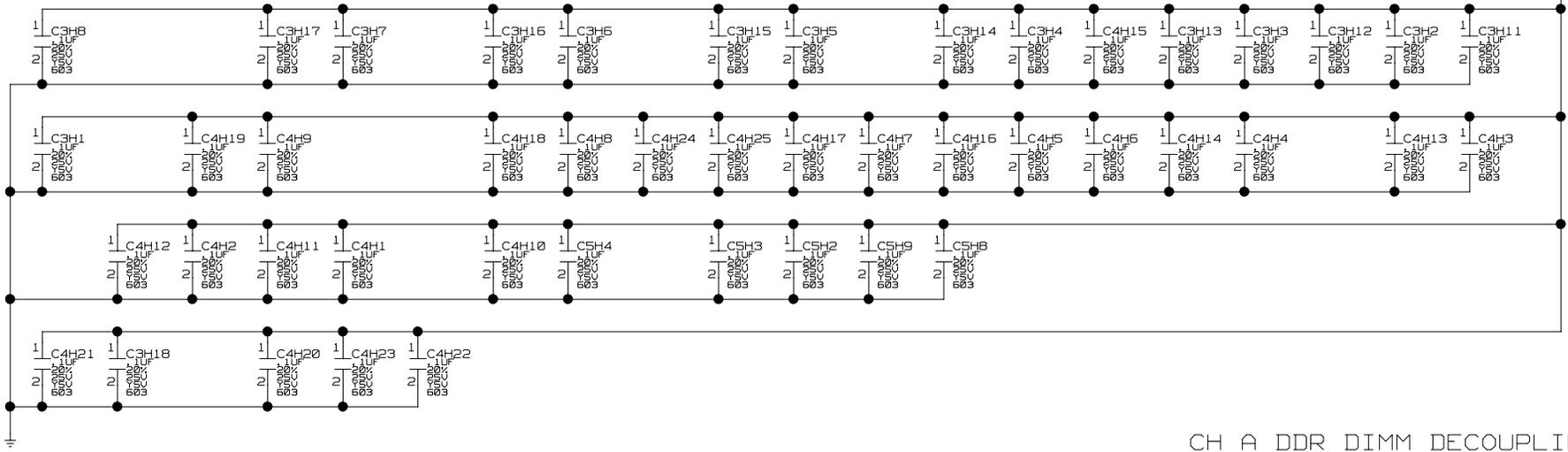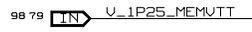
DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

98 79 IN V_1P25_MEMVTT

C3H8 .1UF / C3H17 .1UF / C3H7 .1UF / C3H16 .1UF / C3H6 .1UF / C3H15 .1UF / C3H5 .1UF / C3H14 .1UF / C3H4 .1UF / C4H15 .1UF / C3H13 .1UF / C3H3 .1UF / C3H12 .1UF / C3H2 .1UF / C3H11 .1UF
20% Y5V 603

C3H1 / C4H19 / C4H9 / C4H18 / C4H8 / C4H24 / C4H25 / C4H17 / C4H7 / C4H16 / C4H5 / C4H6 / C4H14 / C4H4 / C4H13 / C4H3
.1UF 20% Y5V 603

C4H12 / C4H2 / C4H11 / C4H1 / C4H10 / C5H4 / C5H3 / C5H2 / C5H9 / C5H8
.1UF 20% Y5V 603

C4H21 / C3H18 / C4H20 / C4H23 / C4H22
.1UF 20% Y5V 603

CH A DDR DIMM DECOUPLING

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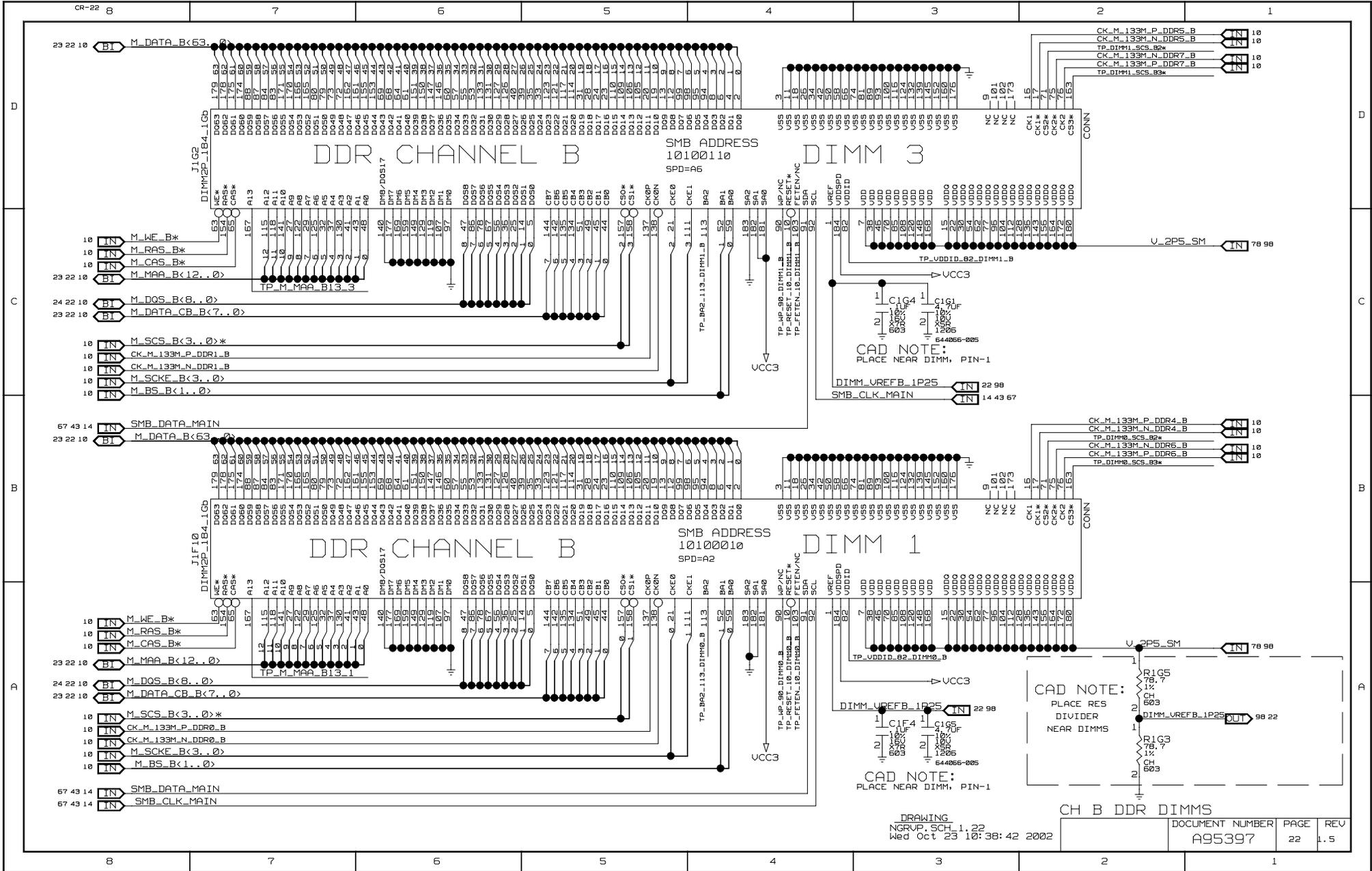
CH B DDR DIMMS

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DDR CHANNEL B

DDR RESISTOR TERMINATION

CH B DDR DATA TERMINATION
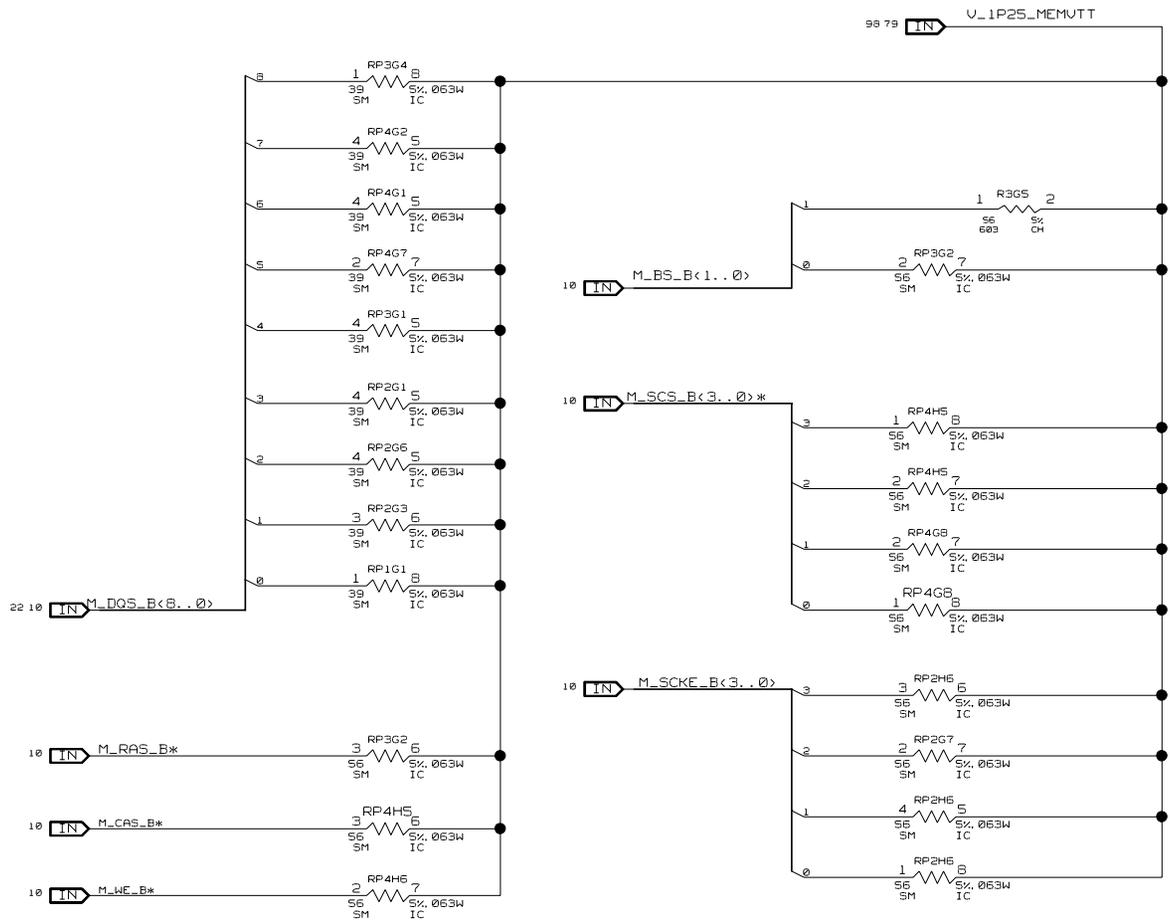
DDR CHANNEL B

CH B DDR CONTROL TERMINATION

DDR CHANNEL B

V_1P25_MEMVTT

98 79 IN

C5H1
4.7UF
10V
EMPTY
1206

C5H7
4.7UF
10V
EMPTY
1206
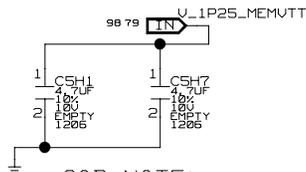
CAD NOTE:
PLACED AT LEFT
END OF VTT ISLAND

DECOUPLING CAPACITORS FOR DDR TERMINATION RESISTORS

98 79 IN V_1P25_MEMVTT

CH B DDR DIMM DECOUPLING

ICH4

U7G1
ICH4

Signal	Pin	Name
P_INTA*	D5	PIRQA*
P_INTB*	C2	PIRQB*
P_INTC*	B4	PIRQC*
P_INTD*	A3	PIRQD*
P_INTE*	C6	PIRQE*/GPIO2
P_INTF*	D7	PIRQF*/GPIO3 INPUT
P_INTG*	C3	PIRQG*/GPIO4 ONLY
P_INTH*	C4	PIRQH*/GPIO5

P_REQ<4..0>*
B6	REQ*<4>
C7	REQ*<3>
B3	REQ*<2>
A2	REQ*<1>
B1	REQ*<0>

P_REQ5* — A6 — REQB*/REQ5*/GPIO1 INPUT
P_REQA* — B5 — REQA*/GPIO0 ONLY

P_GNT<4..0>*
D6	GNT*<4>
B7	GNT*<3>
A7	GNT*<2>
E6	GNT*<1>
C1	GNT*<0>

P_GNT5* — C5 — GNT5*/GNTB*/GPIO17 OUTPUT
P_GNTA* — E8 — GNTA*/GPIO16 ONLY

Signal	Pin	Name
P_FRAME*	F1	FRAME*
P_IRDY*	L5	IRDY*
P_TRDY*	F2	TRDY*
P_DEVSEL*	M3	DEVSEL*
P_STOP*	F3	STOP*
P_PAR	G1	PAR
P_PERR*	L4	PERR*
P_PLOCK*	M2	PLOCK*
P_SERR*	K5	SERR*
P_PME*	W2	PME*
P_PCIRST_ICH*	U5	PCIRST*
CK_P_33M_ICH	P5	PCICLK

AD<31..0> → P_AD<31..0>

C/BE*<3..0> → P_C/BE<3..0>*

IC

U7G1
ICH4

ICH4_IDE_PDD<15..0>

PDD<15..0> / SDD<15..0> → ICH4_IDE_SDD<15..0>

ICH4_IDE_PDIOW* — W12 — PDIOW* — SDIOW* — AA18 — ICH4_IDE_SDIOW*
ICH4_IDE_PDDACK* — Y12 — PDDACK* — SDDACK* — AB19 — ICH4_IDE_SDDACK*
ICH4_IDE_PDDREQ — AA11 — PDDREQ — SDDREQ — AB18 — ICH4_IDE_SDDREQ
ICH4_IDE_PDIOR* — AC12 — PDIOR* — SDIOR* — Y18 — ICH4_IDE_SDIOR*
ICH4_IDE_PIORDY — AB12 — PIORDY — SIORDY — AC19 — ICH4_IDE_SIORDY

ICH4_IDE_PDA<2..0> — PDA0/PDA1/PDA2 — SDA0/SDA1/SDA2 → ICH4_IDE_SDA<2..0>

ICH4_IDE_PDCS1* — Y13 — PDCS1* — SDCS1* — AB21 — ICH4_IDE_SDCS1*
ICH4_IDE_PDCS3* — AB14 — PDCS3* — SDCS3* — AC22 — ICH4_IDE_SDCS3*

IRQ14 — AC13 — ICH4_IDE_IRQ14
IRQ15 — AA19 — ICH4_IDE_IRQ15

IC

ICH

ICH4

ICH

84 IN V_3P3_STBY   1 R7H3 2
                        10K 0%
                        603 CH

U7G1
ICH4

Pin	Signal		Signal	Pin	Net	Dir	

30 IN APICD0_1

J19 APICCLK   INPUT ONLY   GPIO6 R2 ICH_GPI6_GPIO7_PU IN 30
H19 APICD_0   GPIO7 R3
K20 APICD_1   GPIO8 U4 CDC_DWN_ENAB*   IN 30 43 57

6 OUT ICH_H_STPCLK*   V23 STPCLK*   GPIO12 V5 IO_SMI* IN 61
                      AB23 A20M*   GPIO13 W3 IO_PME* IN 61
                      U21 CPUSLP*
                      Y23 CPUPWRGD   OUTPUT ONLY   GPIO18 Y21 TP_GPO18
6 OUT H_A20M*   AB22 INTR   GPIO19 W18 TP_GPO19
                      V21 NMI*   GPIO20 W19 TP_GPO20
                      W23 SMI*   GPIO21 T3 TP_GPO21
6 OUT H_SLP*   W21 IGNNE*   GPIO22 Y2 ICH_GPO22_PU OUT 30
                                      I/O   GPIO23 J21 TP_GPO23
98 61 OUT A20GATE   U22 A20GATE   GPIO24 AC2 TP_GPIO24
98 61 OUT KBRST*   U21 RCIN*   GPIO25 V2 TP_GPIO25
7 6 IN H_FERR*   AA21 FERR*   GPIO27 W1 TP_GPIO27
                      V22 INIT*   GPIO28 W4 GPIO_LAN_DISABLE* OUT 27 44 74
6 7 OUT H_PWRGD   SLP_S3* Y4   SLP_S3*   OUT 67
98 61 56 OUT SER_IRQ J22 SERIRQ   SLP_S4* Y2   SLP_S4*   OUT 67
99 98 66 61 56 L_FRAME* T5 LFRAME*/FWH4 SLP_S5* AA2 TP_SLP_S5*
          BI L_DRQ*   U3   LDRQ0*   RI*   Y1   ICH_RI_PU   BI 30
                      U4   LDRQ1*   SW_ON*   AA1 SW_ON*   IN 70 74 75 96
          TP_ICH_LDRQ1_GPI8*   PWRBTN*
6 OUT H_INTR   SYS_RST* Y3   FP_RST*
                      0 T2 LAD0/FWH0 LANRST* Y5   GPIO_LAN_DISABLE* IN 27
                      1 R4 LAD1/FWH1 TP0   AB2 ICH_BATLOW_PU   IN 30
6 OUT H_NMI   2 T4 LAD2/FWH2 SUS_STAT*/LPCPD AB3 ICH_SUS_STAT IN 61 98
                      3 U2 LAD3/FWH3 VRMPWRGD V19 ICH_VRMPWRGD
99 98 66 61 56 BI L_AD<3..0>   THERMTRIP* W20 H_THERMTRIP*   IN 6 7
96 OUT ICH_H_SMI*   AA4 SUSCLK   THRM*   V1   ICH_THRM_PU*   IN
          61 OUT SUSCLK
                     W6   INTRUDER*   SMILINK0 AC3 SMB_CLK_RESUME   OUT 36 37 38 39 40 44 67 98 68
6 OUT H_IGNNE* 30 IN ICH_INTRUDER_HDR W7 RTCRST* SMILINK1 AB1 SMB_DATA_RESUME OUT 36 37 38 39 40 44 67 68 98
                30 IN ICH_RTCRST_PULLUP AB6 PWROK SMBDATA AB4
                67 IN PWRGD_3V   AA6 RSMRST* SMBCLK AC4
                67 IN RSMRST*   AB5 VCCRTC   SMBALERT*/GPIO11 AA5 SMB_ALERT_PU IN
66 6 OUT H_INIT* 81 IN V_3P0_BAT_VREG Y6 VBIAS
                30 IN VBIAS   SPKR H23 SPKR   BI 30 48 69
                30 IN ICH_RTCX1   AC7 RTCX1
                30 IN ICH_RTCX2   AC6 RTCX2   CLK14 J23 CK_14M_ICH IN 14
                     V20 NC
                     U23 NC   IC

1
R7H5
10K
5%
CH
603
2

1
R7H7
10K
5%
EMPTY
603
2

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CR-27

ICH4

8 7 6 5 4 3 2 1

VCC3

U7G1
ICH4

Pin	Signal
A5	VCC3_3
B2	VCC3_3
H6	VCC3_3
J1	VCC3_3
K6	VCC3_3
M10	VCC3_3
P6	VCC3_3
U1	VCC3_3
P12	VCC3_3
V10	VCC3_3
V16	VCC3_3
V18	VCC3_3
AC6	VCC3_3
AC17	VCC3_3
H18	VCC3_3
J18	VCC3_3

VSS pins (right side):
D22, AC23, AC18, AC14, AC10, AC5, AC1, AB20, AB7, AA22, AA16, AA12, AA9, AA3, Y19, Y7, W22, W8, W5, M20, V17, V15, V3, T23, P20, T19, T1, R21, R18, R5, P22, P13, P11, P3, N23, N21, N19, N14, N13, N12, N11, N10, N5, M13, M12, M11, M1, M22, L21, L13, L12, L11, L10, K23, U20, K19, K13, K11, K3, J6, H1, G21, G19, G5, G3, F8, E22, E21, E19, E18, E17, E16, E14, E10, D23, D21, D19, D17, D15, D12, D8, D4

84 IN V_3P3_STBY
E9, F9, E11, F10, V9, V8, V7, F15, F16, F17, F18, K14 — VCCSUS3_3

98 87 IN V_1P5_CORE
K10, K12, K18, K22, P10, T18, V14, U19 — VCC1_5
L23 VCCHI0
M14 VCCHI1
P18 VCCHI2
T22 VCCHI3

+ 1 C6G5
220UF
20%
25V
ELEC
2 RDL
"201307-001"

84 IN V_1P5_STBY
F6, F7, E12, R6, T6, U6, G18, E13, F14, E20 — VCCSUS1_5

67 IN V_REF5V
E7 V5REF1
V6 V5REF2

67 IN V_REF5V_SUS
E15 V5REF_SUS

98 88 IN VCCP
P14 V_CPU_IO
U18 V_CPU_IO
AA23 V_CPU_IO

98 87 IN V_1P5_CORE
C22 VCCPLL

1 C6G8
.01UF
20%
50V
EMPTY
2 603
"X7R"

1 C6G10
.1UF
10%
16V
EMPTY
2 603
"X7R"

602431-025

VSS pins (left side):
D1, C23, C21, C19, C17, C15, C6, B22, B20, B18, B16, B12, B9, A22, A20, A18, A16, A4, A1

IC

C11335-001

ICH POWER/GND

ICH4

CNR	FP	BPL/LAN	BPR/1394	SIGNAL NAME FROM ICH
		X		USB_BACK1: USBP0
		X		USB_BACK2: USBP1
			X	USB_BACK3: USBP2
			X	USB_BACK4: USBP3
	X			USB_FRONT1: USBP4
X <OPT>	X			USB_FRONT2: _CNR USBP5

U7G1
ICH4

USB_BACK1   C20 USBP_0
USB_BACK1*   D20 USBP_0*
USB_BACK2   A21 USBP_1
USB_BACK2*   B21 USBP_1*
USB_BACK3   C18 USBP_2
USB_BACK3*   D18 USBP_2*
USB_BACK4   A19 USBP_3
USB_BACK4*   B19 USBP_3*
USB_FRONT1   C16 USBP_4
USB_FRONT1*   D16 USBP_4*
USB_FRONT2_CNR   A17 USBP_5
USB_FRONT2_CNR* B17 USBP_5*

USB_OC_BACK_LEFT*   B15 OC*<0>
                     C14 OC*<1>
USB_OC_BACK_RIGHT*   A15 OC*<2>
                     B14 OC*<3>
USB_OC_FRONT*   A14 OC*<4>
                     D14 OC*<5>

TP_ICH_GPIO32   J20 GPIO32
TP_ICH_GPIO33   G22 GPIO33
TP_ICH_GPIO34   F20 GPIO34
TP_ICH_GPIO35   G20 GPIO35
TP_ICH_GPIO36   F21 GPIO36
                H20 GPIO37
                F23 GPIO38
                H22 GPIO39
                G23 GPIO40
                H21 GPIO41
                F22 GPIO42
                E23 GPIO43

BOARDID<4..0>

AGP_PRO_PRSNT1
AGP_PRO_PRSNT2
BOARDID<4>

CK_48M_ICH_USB   F19 CLK48

ICH_USB_RBIAS   B23 USBRBIAS*
                 A23 USBRBIAS

HI<0>   L19 0   HI<11..0>
HI<1>   L20 1
HI<2>   M19 2
HI<3>   M21 3
HI<4>   P19 4
HI<5>   R19 5
HI<6>   T20 6
HI<7>   R20 7
HI<8>   P23 8
HI<9>   L22 9
HI<10>   N22 10
HI<11>   K21   HI<11>

HI_STBS P21 HI_STBS
HI_STBF N20 HI_STBF

HICOMP   R23 HI_RCOMP_ICH
HISWING R22 HI_SWING_ICH
HIREF   M23 HI_VREF_ICH
CLK66   T21 CK_HBL_66M_ICH

LANRXD0   A10 ICH_LAN_RXD0_R
LANRXD1   A9   ICH_LAN_RXD1_R
LANRXD2   A11 ICH_LAN_RXD2_R
LANTXD0   B10 ICH_LAN_TXD0_R
LANTXD1   C10 ICH_LAN_TXD1_R
LANTXD2   A12 ICH_LAN_TXD2_R
LANRSTSYNC B11 ICH_LAN_RST_R
LANCLK   C11 ICH_LAN_CLK_R

EE_DIN   D11 ICH_EE_DIN_R
EE_CS   D10 ICH_EE_CS_R
EE_SHCLK   C12 ICH_EE_CLK_R
EE_DOUT   A8   ICH_EE_DOUT_R

ACSYNC   C9   AUD_LINK-SYNC_R
ACSDOUT   D9   AUD_LINK-SDO_R
ACBITCLK   B8   AUD_LINK-BCLK
ACRST*   C13 AUD_LINK-RST*
ACSDIN0   D13 AUD_LINK-SDI0
ACSDIN1   A13 AUD_LINK-SDI1
ACSDIN2   B13 AUD_LINK-SDI2

IC

CAD NOTE:
CAN BE SHORTED TOGETHER CLOSE TO
ICH WHILE KEEPING TOTAL LENGTH
TO RESISTOR LESS THAN 500 MIL

R6G6
22.6
1%
CH
603

ICH

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SPARE

TP_RPAK_10K_PU_2
2 RP7H1 10K 5% .063W IC SM
7 TP_RPAK_10K_PU_7

TP_ICH_10K_1
1 RP7H1 10K 5% .063W IC SM
8 TP_ICH_10K_8

98 87 IN V_1P5_CORE
VCC3
3 RP7H1 10K 5% .063W IC 6 SM
1 R6G19 43.2 1% CH 603
HI_RCOMP_ICH OUT 29
ICH_GPI6_GPIO7_PU OUT 27

VCC3
4 RP7H1 10K 5% .063W IC 5 SM
APICD0_1 OUT 27
1 R6G9 10K 5% CH 603 2
27 IN ICH_GPO22_PU
OPEN-DRAIN

VCC3
1 R6H2 10K 5% CH 603 2
1 R7H1 4.7K 5% CH 603 2
ICH_THRM_PU* OUT 27
ICH_VRMPWRGD OUT 27

VCC3
1 R6G13 10K 5% CH 603 2
1 R6G4 10K 5% EMPTY 603 2
1 R6G12 10K 5% EMPTY 603 2
1 R6G8 10K 5% EMPTY 603 2
1 R6G2 10K 5% EMPTY 603 2
1 R6G11 10K 5% EMPTY 603 2
1 R6G7 10K 5% CH 603 2
1 R6G14 10K 5% CH 603 2
1 R6G10 10K 5% CH 603 2
1 R6G5 10K 5% CH 603 2
BOARDID<4..0> OUT 29
0 1 2 3 4

84 IN V_3P3_STBY
1 R7H4 10K 5% CH 603 2
1 R7H2 8.2K 5% CH 603 2
1 R7H6 10K 5% CH 603 2
SMB_ALERT_PU OUT 27
ICH_RI_PU OUT 27
ICH_BATLOW_PU OUT 27

DESIGN NOTE:
ATTACH SUITCASE JUMPER TO
ENABLE NO_REBOOT MODE
DEFAULT JUMPER EMPTY
DEBUG ONLY

VCC3
1 R8H1 1K 5% CH 603 2
SPKR_HDR_STRAP
J8H1 1X2HDR HDR
27 IN SPKR

98 87 IN V_1P5_CORE
HI_SWING_ICH OUT 29
1 R6G222 80.6 1% 603
1 C6G13 .01UF 10% 16V X7R 603
1 C6G12 1UF 10% 16V X7R 603
R6G17 51.1 1% CH 603
1 R6G152 40.2 1% 603
1 C6G6 .01UF 10% 50V X7R "X7R"
1 C6G9 1UF 10% 16V X7R 603
HI_VREF_ICH OUT 98 29

CAD NOTES:
PLACE 0.01UF CAP WITHIN 0.25" OF
DEVICE PIN (MCH, ICH, AGP)
PLACE 0.1UF CAP CLOSE TO RESISTOR CIRCUIT

VV & CRB ONLY EVALUATION
R7G9
26 IN P_PCIRST_ICH*
1 0 603 1A CH 2
P_PCIRST* OUT 9 44 56 61 66 95
C7G13 47PF 50V "NPO" EMPTY 603

DESIGN NOTE:
STUFF CAP FOR EMI IF NECESSARY

27 67 43 BI CDC_DWN_ENAB*
1 R6F3 100K 5% 603 2
1 R6F4 4.7K 5% CH 603 2
84 IN V_3P3_STBY

DESIGN NOTE:
STUFF FOR CNR ONLY
(NO AUDIO DOWN)

DESIGN NOTE:
STUFF FOR AUD/CNR
AUD/NO-CNR, NO-AUD/NO-CNR

29 IN ICH_EE_DOUT_R 1 R7G5 2
10K 5% 603 EMPTY

CAD NOTE:
BACKSIDE COMPONENT

CLEAR CMOS
J8H3 1X3HDR
1 TP_CLRCMOS
2 ICH_RTCRST_PULLUP
3 NET_CLR_CMOS_JUMPER
HDR
OUT 30 27
1 R8H6 4.7K 5% CH 603 2

| 1-2 | NORMAL * |
| 2-3 | CLR CMOS |

DEFAULT: *

SERIES TERMINATION FOR SOFT AUDIO
29 IN AUD_LINK_SDO_R 1 R7G8 2 AUD_LINK_SDO OUT 43 48
33 5% 603 CH
29 IN AUD_LINK_SYNC_R 1 R7G7 2 AUD_LINK_SYNC OUT 43 48
33 5% 603 CH

CAD NOTE:
PLACE CLOSE TO ICH

84 IN V_3P3_STBY
98 87 IN V_1P5_STBY
98 87 IN V_1P5_CORE
98 87 IN V_1P5_CORE
81 IN V_3P0_BAT_VREG
67 IN V_REF5V
98 88 IN VCCP
67 IN V_REF5V_SUS

VCC3

C7H3 .1UF 20% 603 Y5V
C7G2 .1UF 20% Y5V 603
C6H1 .1UF 20% Y5V 603
C7G7 .1UF 20% Y5V 603
C6G1 .1UF 20% Y5V 603
C6G11 .1UF 20% Y5V 603

C6H5 .1UF 25V Y5V 603
C6G7 .1UF 25V Y5V 603
C7G8 .1UF 25V Y5V 603
C7F6 .1UF 25V Y5V 603
C7G10 20UF 4.7UF 16V Y5V 1206
C7G11 20UF 4.7UF 16V 60V EMPTY 1206 "Y5V"

C7G6 .1UF 25V Y5V 603
C7H2 .1UF 20V Y5V 603
C7G12 .1UF 20V Y5V 603
C7G3 .1UF 20V Y5V 603

C6G3 .1UF 25V Y5V 603
C7G4 .1UF 20V Y5V 603

VCC3
C6G4 .1UF 25V Y5V 603
C6H3 .1UF 20V Y5V 603
C7H5 .1UF 20% Y5V 603
C7G9 .1UF 20% Y5V 603
C7G1 .1UF 20% Y5V 603
C7H4 .1UF 20% 603 Y5V

CAD NOTE:
PLACE ALL WITHIN 40 MILS OF ICH4.

VBIAS OUT 27
81 IN V_BAT_VREG_R_CR
1 C7H7 2 .047UF 20% 50V X7R 603
C7H6 1UF 20% 50V X7R 603
1 R7H122 10M 5% CH
XY7H1 SOCKET AS2705-003
TH CONN
32.768KHZ SOCKET
Y7H2 32.768KHZ 519601-001
4 1 SM 3 2 EMPTY
1 R7H8 2 10M 5% 603 CH
ICH_RTCX1 OUT 27
ICH_RTCX2 OUT 27
C7H8 6.8PF 50V NPO 603
C7H9 6.8PF 50V NPO 603

CAD NOTE:
PLACE AT SOUTH END OF THE BOARD
DUAL FOOT PRINTED WITH THE CUSTOM INTRUDER HEADER
J9H2 1X2HDR 107555-102
1 2 HDR

CAD NOTE:
PLACE AT NORTH END OF THE BOARD
J8H2 1X2HDR 107555-102
1 2 HDR

81 IN V_3P0_BAT_VREG
1 R8H2 2 330K 5% 603
ICH_INTRUDER_HDR OUT 27 75
1 R8H3 2 22K 5% 603
ICH_RTCRST_PULLUP OUT 30 27
1 C8H7 10UF 10% Y5V 603 2

DRAWING
NGRVP.SCH_1.30
Wed Oct 23 10:38:45 2002

ICH TERMINATION

| DOCUMENT NUMBER | PAGE | REV |
| A95397 | 30 | 1.5 |

LAN CONNECT INTERFACE (LCI) TO CNR
CNR STUFFING OPTION FOR LAN-UP SOLUTION

46 29 IN ICH_LAN_TXD0_R — RP8F2 1 — 8 33 5% 063W SM IC — ICH_LAN_TXD0_CNR OUT 43

46 29 IN ICH_LAN_TXD1_R — RP8F2 2 — 7 33 5% 063W SM IC — ICH_LAN_TXD1_CNR OUT 43

46 29 IN ICH_LAN_TXD2_R — RP8F2 4 — 5 33 5% 063W SM IC — ICH_LAN_TXD2_CNR OUT 43

46 29 OUT ICH_LAN_RXD0_R — RP7F1 1 — 8 33 5% 063W SM IC — ICH_LAN_RXD0_CNR IN 43

46 29 OUT ICH_LAN_RXD1_R — RP7F1 2 — 7 33 5% 063W SM IC — ICH_LAN_RXD1_CNR IN 43

46 29 OUT ICH_LAN_RXD2_R — RP7F1 3 — 6 33 5% 063W SM IC — ICH_LAN_RXD2_CNR IN 43

46 29 IN ICH_LAN_RST_R — RP8F2 3 — 6 33 5% 063W SM IC — ICH_LAN_RST_CNR OUT 43

46 29 OUT ICH_LAN_CLK_R — RP7F1 4 — 5 33 5% 063W SM IC — ICH_LAN_CLK_CNR IN 43

DESIGN NOTE:
LAN CONNECT INTERFACE TO 82562EX/EZ CAN NOT BE STUFFED CONCURRENTLY
82562EX/EZ IS A DESIGN ENGINEERING EVALUATION FEATURE

29 46 OUT ICH_EE_DIN_R — RP7F2 1 — 8 0 5% 063W SM IC — ICH_EE_DIN_CNR IN 43

29 IN ICH_EE_DOUT_R — RP7F2 2 — 7 0 5% 063W SM IC — ICH_EE_DOUT_CNR OUT 43

29 IN ICH_EE_CS_R — RP7F2 4 — 5 0 5% 063W SM IC — ICH_EE_CS_CNR OUT 43

29 IN ICH_EE_CLK_R — RP7F2 3 — 6 0 5% 063W SM IC — ICH_EE_CLK_CNR OUT 43
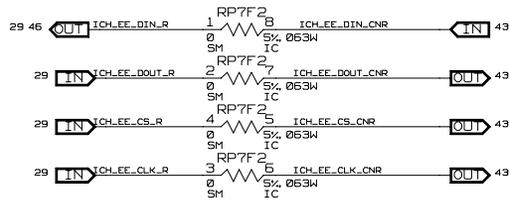
DESIGN NOTE:
0 OHM SERIES "RPACK"
TO CNR EEPROM IS IN PLACE
OPTION OF STUFFING CNR W/LAN,
BYPASSING 82562EX/EZ LAN DOWN
LAN CONNECT INTERFACE STUB REDUCTION.

ICH LAN LINK

IDE CONNECTORS

USB BACK PANEL HEADER (LEFT)

DESIGN NOTE:
STUFF INDUCTOR OPTION
FOR EMI ISSUES

1 R4B4 2
0   1A
603   EMPTY

L4B2
90OHM
IND 4PIN

752402-009
IND

1 R4B5 2
0   1A
603   EMPTY

DESIGN NOTE:
STUFF INDUCTOR OPTION
FOR EMI ISSUES

1 R4B2 2
0   1A
603   EMPTY

L4B1
90OHM
IND 4PIN

752402-009
IND

1 R4B3 2
0   1A
603   EMPTY

29 [BI] USB_BACK1*
29 [BI] USB_BACK1
29 [BI] USB_BACK2*
29 [BI] USB_BACK2

USB_BACK1_R*
USB_BACK1_R
USB_BACK2_R*
USB_BACK2_R

CR4B3   CR4B4
2   1   2   1
EMPTY   EMPTY
A53075-001   A53075-001

CR4B1   CR4B2
2   1   2   1
EMPTY   EMPTY
A53075-001   A53075-001

[BI] 33 47
[BI] 33 47

[BI] 33 47
[BI] 33 47

CAD NOTE:
PLACE DUAL-DIODE COMPONENTS
NEAR USB CONN

DESIGN NOTE:
CONNECTOR STUFFING OPTIONS:
DEFAULT: USE A74307-001 WITH GIGABIT LAN (82540EP) DESIGNS & (2) USB
OPTION: USE A74314-001 WITH 10/100 LAN (82562EX/EZ) DESIGNS & (2) USB
OPTION: USE 749193-001 DOUBLE STACK USB

749193-001
J4A1
2 X USB

83 [IN] VREG_USB_BP_LEFT

47 33 [BI] USB_BACK2_R*
47 33 [BI] USB_BACK2_R

47 33 [BI] USB_BACK1_R*
47 33 [BI] USB_BACK1_R

1
2
3
4

5
6
7
8

9

10

11

12

EMPTY
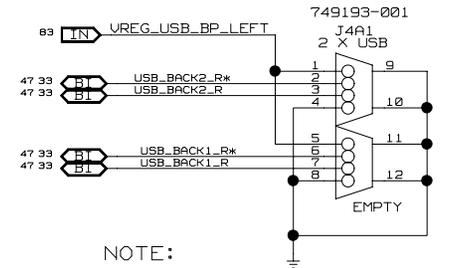
NOTE:
SIGNAL PINS SWAPPED TO ALLOW
OVERLAP WITH COMBO-CONNECTOR

USB BACK PANEL

8   7   6   5   4   3   2   1

CAD NOTE:
TRACE ROUTING IS 7.5 MIL, 7 MIL SPACING

CAD NOTE:
PLACE MIDWAY BETWEEN THE FRONT PANEL HEADER (2X5) & CNR,
RUN MUST HAVE 50 MIL TRACE (FOR POWER) TO BOTH LOCATIONS.

VCC

USB_CNR_PWR   OUT 43

Q9D1
SI4501DY

DESIGN NOTE:
STUFF FOR
"MB WITH FUSE"
FRONT PANEL
SUPPORT

657448-004

	S1	DRN	8
81	IN	VREG_USB_NCH 2	G1	DRN	7
80	IN	V_5P0_STBY 3		G2	DRN	6
81	IN	VREG_USB_PCH 4			DRN	5

IC
A03106-001

2 RT9D1 1
THRMSTR
1.50

USB_FNT_PWR   OUT 35 74
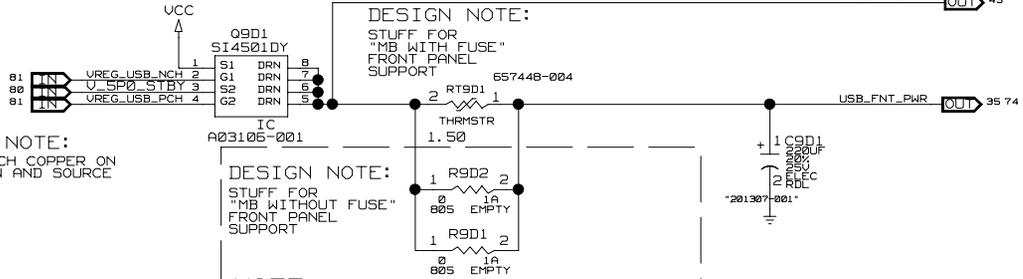
CAD NOTE:
.1 INCH COPPER ON
DRAIN AND SOURCE

DESIGN NOTE:
STUFF FOR
"MB WITHOUT FUSE"
FRONT PANEL
SUPPORT

1 R9D2 2
0   1A
805 EMPTY

1 R9D1 2
0   1A
805 EMPTY

+ 1 C9D1
220UF
25V
ELEC
2 RDL
"201307-001"

NOTE:
IMPLEMENTING THE 0 OHM FEATURE ASSUMES FP CARD HAS A FUSE
IN LINE WITH THE VOLTAGE SUPPLY

DEFAULT: FUSE IN CIRCUIT FOR USB FRONT-PANEL POWER
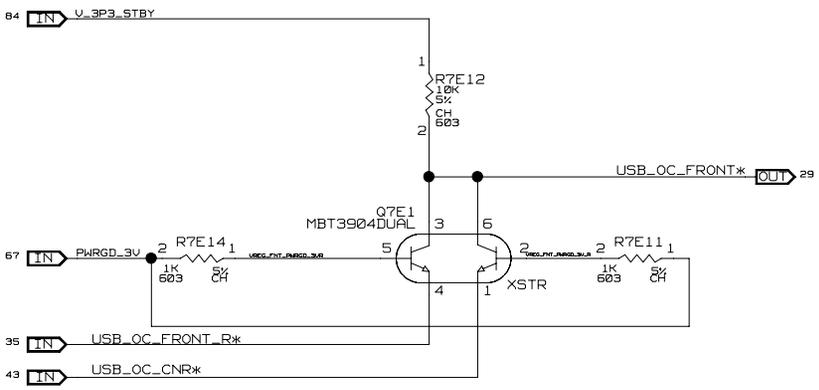
84 IN   V_3P3_STBY

1
R7E12
10K
5%
CH
603
2

USB_OC_FRONT*   OUT 29

Q7E1
MBT3904DUAL   3   6

67 IN   PWRGD_3V   2 R7E14 1   VREG_FNT_PWRGD_3V#   5
1K 603   5% CH

2 VREG_FNT_PWRGD_3V#   2 R7E11 1
1K 603   5% CH

4   1   XSTR

35 IN   USB_OC_FRONT_R*

43 IN   USB_OC_CNR*

USB FP HDR / POWER

USB BACK PANEL HEADER (RIGHT)
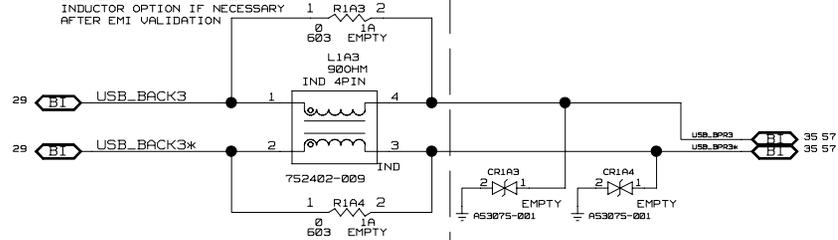
DESIGN NOTE:
INDUCTOR OPTION IF NECESSARY
AFTER EMI VALIDATION

DESIGN NOTE:
CONNECTOR STUFFING OPTIONS:
DEFAULT: USE A74325-001 WITH 1394 & (2) USB
OPTION: USE 749193-001 DOUBLE STACK USB

29 BI USB_BACK3
29 BI USB_BACK3*

L1A3
90OHM
IND 4PIN

USB_BPR3   35 57
USB_BPR3*   35 57

752402-009
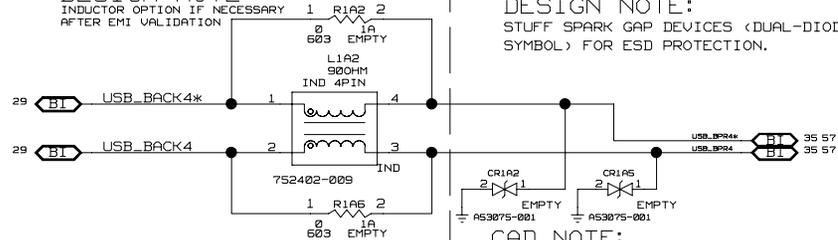
DESIGN NOTE:
STUFF SPARK GAP DEVICES (DUAL-DIODE
SYMBOL) FOR ESD PROTECTION.

DESIGN NOTE:
INDUCTOR OPTION IF NECESSARY
AFTER EMI VALIDATION

L1A2
90OHM
IND 4PIN

29 BI USB_BACK4*
29 BI USB_BACK4

752402-009

CAD NOTE:
PLACE DUAL-DIODE COMPONENTS
NEAR USB CONN

82 IN VREG_USB_BP_RIGHT J1A3
2 X USB
749193-001

57 35 BI USB_BPR4*
57 35 BI USB_BPR4

57 35 BI USB_BPR3*
57 35 BI USB_BPR3

EMPTY

NOTE:
SIGNAL PINS SWAPPED TO ALLOW
OVERLAP WITH COMBO-CONNECTOR

USB FNT PANEL HEADER

J7E1
2X5HDR_9

74 29 BI USB_FRONT1*
74 29 BI USB_FRONT1

USB_FRONT2_R* BI 35 74
USB_FRONT2_R   BI 35 74

HDR

USB SWITCH
USB OPTION FOR CNR OR FRONT PANEL
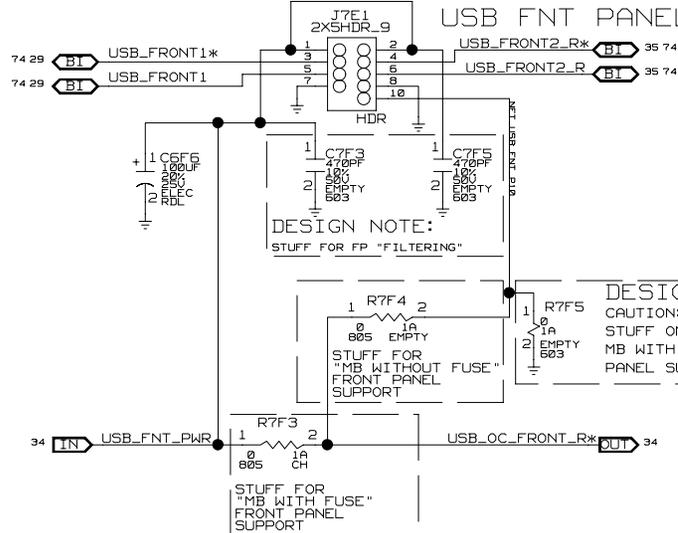
DESIGN NOTE:
STUFF FOR FP "FILTERING"

29 BI USB_FRONT2_CNR
29 BI USB_FRONT2_CNR*

USB_CNR   BI 43
USB_CNR* BI 43

DESIGN NOTE:
CAUTION: 0 OHM TO GND.
STUFF ONLY FOR "CUSTOM
MB WITH FUSE" FRONT
PANEL SUPPORT

STUFF FOR
"MB WITHOUT FUSE"
FRONT PANEL
SUPPORT
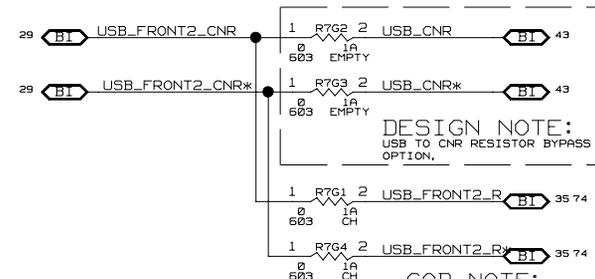
DESIGN NOTE:
USB TO CNR RESISTOR BYPASS
OPTION.

USB_FRONT2_R   BI 35 74

USB_FRONT2_R* BI 35 74

34 IN USB_FNT_PWR

USB_OC_FRONT_R* OUT 34

STUFF FOR
"MB WITH FUSE"
FRONT PANEL
SUPPORT

CAD NOTE:
MINIMIZE STUBS TO 0.100 FOR
CNR AND FRONT PANEL HEADER

DEFAULT: FUSE IN CIRCUIT FOR USB FRONT-PANEL POWER

USB BPR / FP HDR

PCI SLOT 5 SHARED WITH CNR HEADER

PCI SLOT 5
FURTHEST FROM CPU

CR-36

8   7   6   5   4   3   2   1

J9B2
PCI CONN2_2   CONN

VCC3   VCC   +12V   -12V   VCC   VCC3

81 IN   V_3P3_PCIVAUX

26 58 41 38 15 OUT   P_INTB*
26 41 38 15   OUT   P_INTA*

67 15 IN   P_RST_SLOTS*

42 IN   P_GNT_ARB<4..2>*   4

58 44 40 39 38 37 26 15 OUT   P_PME*

58 44 41 40 39 38 37 26   BI   P_FRAME*
         42 60
58 44 41 40 39 38 37 26   BI   P_TRDY*
                       60
58 44 41 40 39 38 37 26   BI   P_STOP*
                       60
98 67 44 40 39 38 37 27   BI   SMB_CLK_RESUME
68 67 44 40 39 38 37 27 68   BI   SMB_DATA_RESUME
                       98
60 58 44 40 39 38 37 26   BI   P_PAR

VCC
RP8E1
1   8   P_REQ64E*
2.7K   5% .063W
SM   IC

60 58 44 40 39 38 37 26   BI   P_AD<31..0>
60 58 44 40 39 38 37 26   BI   P_C/BE<3..0>*

A1 TRST*   M12V_1 B1
A2 P12V_1   TCK   B2
A3 TMS   GND1   B3
A4 TDI   TDO   B4
A5 P5V_2   P5V_0   B5
A6 INTA*   P5V_1   B6
A7 INTC*   INTB*   B7
A8 P5V_3   INTD*   B8
A9 RSVD1   PRST1* B9
A10 P5V_4   RSVD2   B10
A11 RSVD3   PRST2* B11
A12 GND10   GND2   B12
A13 GND16   GND3   B13
A14 3.3VAUX   RSVD5   B14
A15 RST*   GND4   B15
A16 P5V_6   CLK   B16
A17 GNT*   GND7   B17
A18 GND5   REQ*   B18
A19 PME   P5V_11 B19
A20 AD30   AD31   B20
A21 P3.3V   AD29   B21
A22 AD28   GND8   B22
A23 AD26   AD27   B23
A24 GND6   AD25   B24
A25 AD24   P3.3V   B25
A26 IDSEL   C_BE3* B26
A27 P3.3V   AD23   B27
A28 AD22   GND12   B28
A29 AD20   AD21   B29
A30 GND9   AD19   B30
A31 AD18   P3.3V   B31
A32 AD16   AD17   B32
A33 P3.3V   C_BE2* B33
A34 FRAME*   GND14   B34
A35 GND13   IRDY*   B35
A36 TRDY*   P3.3V   B36
A37 GND22   DEVSL* B37
A38 STOP*   GND15   B38
A39 P3.3V   LOCK*   B39
A40 SMB_CLK   PERR*   B40
A41 SMB_DAT   P3.3V   B41
A42 GND25   SERR*   B42
A43 PAR   P3.3V   B43
A44 AD15   C_BE1* B44
A45 P3.3V   AD14   B45
A46 AD13   GND23   B46
A47 AD11   AD12   B47
A48 GND17   AD10   B48
A49 AD09   GND24   B49
    KEY   KEY
A50 B50   A51 B51
    KEY   KEY
A52 C_BE0*   AD08   B52
A53 P3.3V   AD07   B53
A54 AD06   P3.3V   B54
A55 AD04   AD05   B55
A56 GND21   AD03   B56
A57 AD02   GND19   B57
A58 AD00   AD01   B58
A59 P5V_8   P5V_9   B59
A60 REQ64*   ACK64* B60
A61 P5V_12   P5V_5   B61
A62 P5V_10   P5V_7   B62

NC=1,2   732431-002

TP_PCI5_A9
TP_PCI5_A11

TP_PCI5_B4
TP_PCI5_B9
TP_PCI5_B10
TP_PCI5_B11
TP_PCI5_B14

P_INTH*   OUT 39 40 41 26
P_INTE*   OUT 39 40 41 26

CK_P_33M_S5   IN 14

P_REQ_ARB<4..0>*   OUT 37 38 42

P_IRDY*   BI   26 37 38 39 40 41 44 58 60
P_DEVSEL* BI   26 37 38 39 40 41 44 58 60
P_PLOCK*   BI   26 37 38 39 40 41
P_PERR*   OUT 26 37 38 39 40 41 44 58 60
P_SERR*   OUT 26 37 38 39 40 41 44 58 60

P_ACK64*   OUT 37 38 39 40

31
29
27
25
3
23
21
19
17
2
14
12
10
1
8
7
5
3
1

SPARES
RP8E1
TP_2700_RP3   3   6   TP_2700_RP6
2.7K   5% .063W
SM   IC

RP8E1
TP_2700_RP4   4   5   TP_2700_RP5
2.7K   5% .063W
SM   IC

DESIGN NOTE:
PCI SLOT5 = PCI DEVICE #20
REQ/GNT PAIR = #4
IRQ MAP   A : B : C : D
          B : H : A : E

DRAWING
NGRVP.SCH_1.36
Wed Oct 23 10:38:48 2002

PCI SLOT5

DOCUMENT NUMBER   PAGE   REV
A95397   36   1.5

PCI SLOT 4

J8B2
PCI CONN2_2   CONN

DESIGN NOTE:
PCI SLOT4 = PCI DEVICE #19
REQ/GNT PAIR = #3
IRQ MAP   A : B : C : D
          D : C : F : G

DRAWING
NGRVP.SCH_1.37
Wed Oct 23 10:38:49 2002

PCI SLOT4

DOCUMENT NUMBER	PAGE	REV
A95397	37	1.5

PCI SLOT 3

J8B3
PCI CONN2_2   CONN

VCC3   VCC   +12V   -12V   VCC   VCC3

B1 IN V_3P3_PCIVAUX

26 44 41 37 OUT P_INTC*
26 58 41 36 15 OUT P_INTB*

A1	TRST*	M12V_1	TCK	B1
A2	P12V_1		TCK	B2
A3	TMS	GND1	TDO	B3
A4	TDI		TDO	B4
A5	P5V_2	P5V_0		B5
A6	INTA*	P5V_1		B6
A7	INTC*	INTB*		B7
A8	P5V_3	INTD*		B8
A9	RSVD1	PRST1*		B9
A10	P5V_4	RSVD2		B10
A11	RSVD3	PRST2*		B11
A12	GND10	GND2		B12
A13	GND16	GND3		B13
A14	3.3VAUX	RSVD5		B14
A15	RST*	GND4		B15
A16	P5V_6	CLK		B16
A17	GNT*	GND7		B17
A18	GND5	REQ*		B18
A19	PME	P5V_11		B19

TP_PCI3.B4

P_INTD* OUT 37 41 26
P_INTA* OUT 15 36 41 26

TP_PCI3.A9   TP_PCI3.B9
TP_PCI3.A11   TP_PCI3.B10
                TP_PCI3.B11
                TP_PCI3.B14

67 15 IN P_RST_SLOTS*
42 IN P_GNT_ARB<4..2>*

CK_P_33M_S3 IN 14
P_REQ_ARB<4..2>* OUT 36 37 42

58 44 40 39 37 36 26 15 OUT P_PME*

A20	AD30	AD31		B20
A21	P3_3V	AD29		B21
A22	AD28	GND8		B22
A23	AD26	AD27		B23
A24	GND6	AD25		B24
A25	AD24	P3_3V		B25
A26	IDSEL	C_BE3*		B26
A27	P3_3V	AD23		B27
A28	AD22	GND12		B28
A29	AD20	AD21		B29
A30	GND9	AD19		B30
A31	AD18	P3_3V		B31
A32	AD16	AD17		B32
A33	P3_3V	C_BE2*		B33
A34	FRAME*	GND14		B34
A35	GND13	IRDY*		B35
A36	TRDY*	P3_3V		B36
A37	GND22	DEVSL*		B37
A38	STOP*	GND15		B38
A39	P3_3V	LOCK*		B39
A40	SMB_CLK	PERR*		B40
A41	SMB_DAT	P3_3V		B41
A42	GND25	SERR*		B42
A43	PAR	P3_3V		B43
A44	AD15	C_BE1*		B44
A45	P3_3V	AD14		B45
A46	AD13	GND23		B46
A47	AD11	AD12		B47
A48	GND17	AD10		B48
A49	AD09	GND24		B49

58 44 41 40 39 37 36 26 BI P_FRAME*
42 60
58 44 41 40 39 37 36 26 BI P_TRDY*
60
58 44 41 40 39 37 36 26 BI P_STOP*
60
98 67 44 40 39 37 36 27 BI SMB_CLK_RESUME
68
68 67 44 40 39 37 36 27 BI SMB_DATA_RESUME
98
60 58 44 40 39 37 36 26 BI P_PAR

P_IRDY* BI 26 36 37 39 40 41 44 58 60
P_DEVSEL* BI 26 36 37 39 40 41 44 58 60
P_PLOCK* BI 26 36 37 39 40 41
P_PERR* OUT 26 36 37 39 40 41 44 58 60
P_SERR* OUT 26 36 37 39 40 41 44 58 60

	KEY	KEY		
	KEY	KEY		

VCC

RP7E1
3   1   6   REQ64C*
2.7K   5% .063W
SM   IC

A50 B50				
A51 B51				
A52	C_BE0*	AD08		B52
A53	P3_3V	AD07		B53
A54	AD06	P3_3V		B54
A55	AD04	AD05		B55
A56	GND21	AD03		B56
A57	AD02	GND19		B57
A58	AD00	AD01		B58
A59	P5V_8	P5V_9		B59
A60	REQ64*	ACK64*		B60
A61	P5V_12	P5V_5		B61
A62	P5V_10	P5V_7		B62

P_ACK64* OUT 36 37 39 40

NC=1,2   732431-002

60 58 44 40 39 37 36 26 BI P_AD<31..0>
60 58 44 40 39 37 36 26 BI P_C/BE<3..0>*

DESIGN NOTE:

PCI SLOT3 = PCI DEVICE #18
REQ/GNT PAIR = #2
IRQ MAP   A : B : C : D
          C : D : B : A

PCI SLOT3

DOCUMENT NUMBER	PAGE	REV
A95397	38	1.5

CR-38

PCI SLOT 2

VCC3   VCC   +12V   -12V   VCC   VCC3

J7B3
PCI CONN2_2   CONN

B1 [IN] V_3P3_PCIVAUX

A1	TRST*	M12V_1	B1	
A2	P12V_1	TCK	B2	
A3	TMS	GND1	B3	
A4	TDI	TDO	B4	TP_PCI2_B4
A5	P5V_2	P5V_0	B5	

26 41 40 37 [OUT] P_INTG*
26 41 40 36 [OUT] P_INTE*

A6	INTA*	P5V_1	B6	
A7	INTB*	INTB*	B7	P_INTF* [OUT] 37 40 41 60 26
A8	INTC*	INTD*	B8	P_INTH* [OUT] 36 40 41 26
A9	RSVD1	PRST1*	B9	TP_PCI2_B9

TP_PCI2_A9
TP_PCI2_A11

A10	P5V_3	RSVD2	B10	TP_PCI2_B10
A11	RSVD3	PRST2*	B11	TP_PCI2_B11
A12	GND10	GND2	B12	
A13	GND16	GND3	B13	

67 15 [IN] P_RST_SLOTS*
26 [IN] P_GNT<4..0>*

A14	3_3VAUX	RSVD5	B14	TP_PCI2_B14
A15	RST*	GND4	B15	
A16	P5V_6	CLK	B16	CK_P_33M_S2 [IN] 14
A17	GNT*	GND7	B17	P_REQ<4..0>* [OUT] 26 40 41 42 58 60

58 44 40 38 37 36 26 15 [OUT] P_PME*

A18	GND5	REQ*	B18	
A19	PME	P5V_11	B19	
A20	AD30	AD31	B20	
A21	P3_3V	AD29	B21	
A22	AD28	GND8	B22	
A23	AD26	AD27	B23	
A24	GND6	AD25	B24	
A25	AD24	P3_3V	B25	
A26	IDSEL	C_BE3*	B26	
A27	P3_3V	AD23	B27	
A28	AD22	GND12	B28	
A29	AD20	AD21	B29	
A30	GND9	AD19	B30	
A31	AD18	P3_3V	B31	
A32	AD16	AD17	B32	
A33	P3_3V	C_BE2*	B33	

58 44 41 40 38 37 36 26 42 60 [BI] P_FRAME*
58 44 41 40 38 37 36 26 60 [BI] P_TRDY*
58 44 41 40 38 37 36 26 60 [BI] P_STOP*
98 67 44 40 38 37 36 27 68 [BI] SMB_CLK_RESUME
68 67 44 40 38 37 36 27 98 [BI] SMB_DATA_RESUME
60 58 44 40 38 37 36 26 [BI] P_PAR

A34	FRAME*	GND14	B34	
A35	GND13	IRDY*	B35	P_IRDY* [BI] 26 36 37 38 40 41 44 58 60
A36	TRDY*	P3_3V	B36	
A37	GND22	DEVSL*	B37	P_DEVSEL* [BI] 26 36 37 38 40 41 44 58 60
A38	STOP*	GND15	B38	
A39	P3_3V	LOCK*	B39	P_PLOCK* [BI] 26 36 37 38 40 41
A40	SMB_CLK	PERR*	B40	P_PERR* [OUT] 26 36 37 38 40 41 44 58 60
A41	SMB_DAT	P3_3V	B41	
A42	GND25	SERR*	B42	P_SERR* [OUT] 26 36 37 38 40 41 44 58 60
A43	PAR	P3_3V	B43	
A44	AD15	C_BE1*	B44	
A45	P3_3V	AD14	B45	
A46	AD13	GND23	B46	
A47	AD11	AD12	B47	
A48	GND17	AD10	B48	
A49	AD09	GND24	B49	
KEY		KEY		
KEY	A50 B50	KEY		
	A51 B51			
A52	C_BE0*	AD08	B52	
A53	P3_3V	AD07	B53	
A54	AD06	P3_3V	B54	
A55	AD04	AD05	B55	
A56	GND21	AD03	B56	
A57	AD02	GND19	B57	
A58	AD00	AD01	B58	
A59	P5V_8	P5V_9	B59	
A60	REQ64*	ACK64*	B60	P_ACK64* [OUT] 36 37 38 40
A61	P5V_12	P5V_5	B61	
A62	P5V_10	P5V_7	B62	

VCC

RP7E1
2   7
2.7K   5% .063W
SM   IC
REQ64B*

NC=1,2   732431-002

60 58 44 40 38 37 36 26 [BI] P_AD<31..0>
60 58 44 40 38 37 36 26 [BI] P_C/BE<3..0>*

DESIGN NOTE:
PCI SLOT2 = PCI DEVICE #17
REQ/GNT PAIR = #1
IRQ MAP   A : B : C : D
       G : F : E : H

PCI SLOT2

PCI SLOT 1
CLOSEST TO CPU

J6B2
PCI CONN2_2   CONN

DESIGN NOTE:
PCI SLOT1 = PCI DEVICE #16
REQ/GNT PAIR = #0
IRQ MAP   A : B : C : D
          F : G : H : E

PCI SLOT1

DRAWING
NGRVP.SCH_1.40
Wed Oct 23 10:38:50 2002

DOCUMENT NUMBER	PAGE	REV
A95397	40	1.5

CR-41

8   7   6   5   4   3   2   1

PCI SLOT DECOUPLING

PCI PULL-UPS   VCC

VCC3   VCC3   VCC   VCC3   VCC3   VCC

C9D3 100UF
+ 20% 25V ELEC RDL

C8D2 100UF
+ 20% 25V EMPTY RDL

C7E2 22UF
20% 25V EMPTY RDL

C7C8 .1UF 20% Y5V 603

C9D2 .1UF 20% EMPTY 603

C8B12 .1UF 20% EMPTY 603

C9C2 22UF
20% 25V ELEC RDL

C7D4 100UF
20% 25V ELEC RDL

C9B10 22UF
20% 25V ELEC RDL

C7D2 .1UF 20% Y5V 603

C7D1 .1UF 20% EMPTY 603

C9B11 .1UF 20% Y5V 603

C7C9 22UF
20% 25V ELEC RDL

C8D1 100UF
20% 25V EMPTY RDL

C9E1 22UF
20% 25V ELEC RDL

C7D3 .1UF 20% Y5V 603

C9C3 .1UF 20% Y5V 603

C8B10 .1UF 20% Y5V 603

C7C7 22UF
20% 25V EMPTY RDL

C7E1 100UF
20% 25V EMPTY RDL

C8E1 100UF
20% 25V EMPTY RDL

C8C2 .1UF 20% Y5V 603

C8B8 .1UF 20% Y5V 603

C8C1 22UF
+ 20% 25V EMPTY RDL

C6E2 100UF
+ 20% 25V EMPTY RDL

C8B11 100UF
20% 25V EMPTY RDL

+12V

C7B10 22UF
20% 25V ELEC RDL

C6C13 22UF
+ 20% 25V ELEC RDL

GENERAL BULK DCPL

60 58 44 40 39 38 37 36 26 OUT P_SERR*   RP8C2 4 / 5 2.7K SM 5% 063W IC
60 58 44 40 39 38 37 36 26 OUT P_DEVSEL* 1 R6D1 2 2.7K 5% 603 CH
60 58 44 40 39 38 37 36 26 OUT P_IRDY*   RP6D2 2 / 7 2.7K SM 5% 063W IC
40 39 38 37 36 26 OUT P_PLOCK* RP6D2 2 / 7 2.7K SM 5% 063W IC
60 58 44 40 39 38 37 36 26 OUT P_PERR* RP6D1 4 / 5 2.7K SM 5% 063W IC

60 58 44 40 39 38 37 36 26 42 OUT P_FRAME* RP6D1 1 / 8 2.7K SM 5% 063W IC
60 58 44 40 39 38 37 36 26 OUT P_TRDY* RP6D1 3 / 6 2.7K SM 5% 063W IC
60 58 44 40 39 38 37 36 26 OUT P_STOP* RP6D2 1 / 8 2.7K SM 5% 063W IC

RP8C1 4 / 5 2.7K SM 5% 063W IC
RP8C1 2 / 7 2.7K SM 5% 063W IC
RP8C1 4 / 5 2.7K SM 5% 063W IC
RP8C2 2 / 7 2.7K SM 5% 063W IC
60 58 42 40 39 26 OUT P_REQ<4..0>* RP8C1 2 / 7 2.7K SM 5% 063W IC
26 OUT P_REQA* RP8C2 2 / 7 2.7K SM 5% 063W IC
26 44 OUT P_REQ5* RP8C2 3 / 6 2.7K SM 5% 063W IC

VCC3

26 38 36 15 OUT P_INTA* RPBG1 3 / 6 8.2K SM 5% 063W IC
26 58 38 36 15 OUT P_INTB* RP8G2 5 / 4 8.2K SM 5% 063W IC
26 44 38 37 OUT P_INTC* RPBG2 7 / 2 8.2K SM 5% 063W IC
26 38 37 OUT P_INTD* RP8G2 8 / 1 8.2K SM 5% 063W IC
26 40 39 36 OUT P_INTE* RP8G1 2 / 7 8.2K SM 5% 063W IC
26 60 40 39 37 OUT P_INTF* RPBG1 4 / 5 8.2K SM 5% 063W IC
26 40 39 37 OUT P_INTG* RP8G1 1 / 8 8.2K SM 5% 063W IC
26 40 39 36 OUT P_INTH* RPBG2 6 / 3 8.2K SM 5% 063W IC

26 IN P_GNTA*

DESIGN NOTE:
OPTION FOR BIOS
TOP SWAP OVERRIDE

R7G5 10K 5% EMPTY 603

SPARE SECTIONS

TP_SDONE_RP_3   RP6D2 2 / 7 2.7K SM 5% 063W IC   TP_SDONE_RP_6

TP_SBO_RP_4   RP6D2 4 / 5 2.7K SM 5% 063W IC   TP_SBO_RP_5

PCI TERMINATION

8 7 6 5 4 3 2 1

D

"10NS PART"
743390-001
U7F1
EPM7032

14 [IN] CK_P_33M_ARB 43 GCLK
67 15 [IN] P_RST_SLOTS* 1 GCLR
58 44 41 40 39 38 37 36 26 [IN] P_FRAME* 44 OE1
60 26 [IN] P_GNT<2>* 2 OE2

IO32 41 P_REQ<2>* [OUT] 26 39 40 41 42
IO31 40 "NC"
IO30 39 P_GNT_ARB<4>* [OUT] 42 36 37 38
IO29 38 "NC"
IO28 37 "NC"
IO27 36 P_GNT_ARB<3>* [OUT] 42 36 37 38
IO26 34 "NC"
IO25 33 P_GNT_ARB<2>* [OUT] 42 36 37 38
IO24 32 "NC"
IO23 31 "NC"
IO22 29 "NC"
IO21 28 "NC"
IO20 27 "NC"
IO19 26 "NC"
IO18 25 "NC"
IO17 24 "NC"
IO16 21 "NC"
IO15 20 "NC"
IO14 19 "NC"
IO13 18 "NC"
IO12 17 "NC"
IO11 16 "NC"
IO10 14 "NC"
IO9 13 "NC"
IO8 12 "NC"
IO7 11 "NC"
IO6 9 "NC"
IO5 8 "NC"
IO4 7 "NC"
IO3 6 P_REQ_ARB<2>* [IN] 36 37 38
IO2 5 P_REQ_ARB<3>* [IN] 36 37 38
IO1 4 P_REQ_ARB<4>* [IN] 36 37 38

IC
VCC3(PQFP)=9,17,29,41
GND(PQFP)=4,16,24,36
NC(PQFP)=45

VCC3(PLCC)=3,15,23,35
GND(PLCC)=10,22,30,42

VCC3 VCC3
1 C7F1 1 C7F4
.1UF .1UF
20% 20%
25V 25V
603 603
2 2

VCC3 VCC3
1 C7E3 1 C7F2
.1UF .1UF
20% 20%
25V 25V
EMPTY EMPTY
603 603
2 2

VCC
1 RBC1 2
2.7K 5%
603 CH
1 RBC2 2
2.7K 5%
603 CH
1 R9C2 2
2.7K 5%
603 CH

DESIGN NOTE:
STUFF 0 OHM BYPASS RESISTORS IF ARBITER SITE IS EMPTY.
ARBITER CAN BE EMPTY ONLY IF BOTH SATA & 1394 ARE EMPTY.

DESIGN NOTE:
STUFF IF ARBITER IS STUFFED

60 58 42 41 40 39 26 [OUT] P_REQ<4..0>* 2 1 R7E7 2 P_REQ_ARB<4..2>* [IN] 36 37 38
0 1A
603 EMPTY
3 1 R7E8 3
0 1A
603 EMPTY
4 1 R7E9 4
0 1A
603 EMPTY

26 [IN] P_GNT<4..0>* 2 1 R7E13 2 P_GNT_ARB<4..2>* [OUT] 42 36 37 38
0 1A
603 EMPTY
3 1 R7F1 3
0 1A
603 EMPTY
4 1 R7E10 4
0 1A
603 EMPTY

PCI ARBITER

DRAWING
NGRUP.SCH_1.42
Wed Oct 23 10:38:51 2002

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PCI SLOT 5 (NEAR BOARD EDGE) SHARED WITH CNR HEADER

J9B1
CNR60

CNR SLOT DECOUPLING

VCC
"X5R" C9E2 1 2
10.0UF 20%
6.3V
EMPTY
1206

VCC3
"X7R" C9D4 1 2
.1UF 20%
25V
Y5V
603

+12V
"X7R" C9B9 1 2
.1UF 20%
25V
Y5V
603

Pin	Signal		Pin	Signal
B1	RESERVED	A1	RESERVED	
B2	RESERVED	A2	RESERVED	
B3	RESERVED	A3	GND	
B4	GND	A4	RESERVED	
B5	RESERVED	A5	RESERVED	
B6	RESERVED	A6	GND	
B7	GND	A7	LAN_TXD2	
B8	LAN_TXD1	A8	LAN_TXD0	
B9	LAN_RSTSYNC	A9	GND	
B10	GND	A10	LAN_CLK	
B11	LAN_RXD2	A11	LAN_RXD1	
B12	LAN_RXD0	A12	RESERVED	
B13	GND	A13	USB+	
B14	RESERVED	A14	GND	
B15	+5VDUAL	A15	USB-	
B16	USB_OC	A16	+12V	
B17	GND	A17	GND	
B18	-12V	A18	+3.3VDUAL	
B19	+3.3VD	A19	+5VD	
B20	GND	A20	GND	
B21	EEDO	A21	EEDI	
B22	EECK	A22	EECS	
B23	GND	A23	SMB_A1	
B24	SMB_A0	A24	SMB_A2	
B25	SMB_SCL	A25	SMB_SDA	
B26	CDC_DWN_ENAB	A26	AC97_RESET	
B27	GND	A27	AC97_SDATA_IN2	
B28	AC97_SYNC	A28	AC97_SDATA_IN1	
B29	AC97_SDATA_OUT	A29	AC97_SDATA_IN0	
B30	AC97_BITCLK	A30		

CONN
750073-002

31 IN ICH_LAN_TXD1_CNR
31 IN ICH_LAN_RST_CNR
31 OUT ICH_LAN_RXD2_CNR
31 OUT ICH_LAN_RXD0_CNR
34 IN USB_CNR_PWR
34 OUT USB_OC_CNR*
-12V
VCC3 +3.3VD

31 OUT ICH_EE_DIN_CNR
31 IN ICH_EE_CLK_CNR

98 22 17 67 14 B1 SMB_CLK_MAIN
27 67 30 OUT CDC_DWN_ENAB*

ICH_LAN_TXD2_CNR IN 31
ICH_LAN_TXD0_CNR IN 31
ICH_LAN_CLK_CNR OUT 31
ICH_LAN_RXD1_CNR OUT 31
USB_CNR B1 35
USB_CNR* B1 35
+12V
V_3P3_PCIVAUX IN 81
VCC
ICH_EE_DOUT_CNR IN 31
ICH_EE_CS_CNR IN 31
SMB_DATA_MAIN B1 14 67 17 22 98
AUD_LINK_RST* IN 29
AUD_LINK_SDI2 OUT 29 48
AUD_LINK_SDI1 OUT 29
AUD_LINK_SDI0_CNR

30 IN AUD_LINK_SYNC   R9C11 1 2 AUD_LINK_SYNC_CNR
0 603   1A CH

30 IN AUD_LINK_SDO   R9C10 1 2 AUD_LINK_SDO_CNR
0 603   1A CH

29 48 B1 AUD_LINK_BCLK   R9C12 1 2 AUD_LINK_BCLK_CNR
0 603   1A CH

29 OUT AUD_LINK_SDI0   R9C9 1 2
0 603   1A CH

SMB ADDRESS
10101100

VCC

R9C7 10K 5% EMPTY 603	R9C4 10K 5% CH 603	R9C5 10K 5% CH 603

CNR_SMB_A0
CNR_SMB_A1
CNR_SMB_A2

R9C8 10K 5% CH 603	R9C3 10K 5% EMPTY 603	R9C6 10K 5% EMPTY 603

CNR

A76663-003

U5A1
196-PIN PBGA

P_AD<31..0>

Pin	Signal		Signal	Pin	Net	Port
31	B8	AD<31>	MDI+0	C13	LAN_MDI_0	47
30	A8	AD<30>	MDI-0	C14	LAN_MDI_0*	47
29	C7	AD<29>	MDI+1	E13	LAN_MDI_1	47
28	C6	AD<28>	MDI-1	E14	LAN_MDI_1*	47
27	B6	AD<27>	MDI+2	F13	LAN_MDI_2	47
26	B5	AD<26>	MDI-2	F14	LAN_MDI_2*	47
25	A5	AD<25>	MDI+3	H13	LAN_MDI_3	47
24	B4	AD<24>	MDI-3	H14	LAN_MDI_3*	47
23	B3	AD<23>				
22	B1	AD<22>	CTRL_15	P11	LAN_LX2_1P5	46
21	C1	AD<21>	CTRL_25	B13		
20	D3	AD<20>	PHY_REF	B14	LAN_K_PHY_REF	
19	D2	AD<19>	K_XTAL1	K14	LAN_KX1	46
18	D1	AD<18>	K_XTAL2	J14	LAN_KX2	46
17	E3	AD<17>	NC	N11	LAN_LX1	46
16	K1	AD<16>				
15	L2	AD<15>	LINK_UP*	A12	LAN_LINK_UP*	47
14	L1	AD<14>	LINK_100*	B11	LAN_LINK100*	47
13	M3	AD<13>	LINK_1000*	B12	LAN_LINK1000*	47
12	M2	AD<12>	ACTLED*	C11	LAN_ACTLED*	47
11	M1	AD<11>				
10	N2	AD<10>	EESK	M10	LAN_KE_EESK	46
9	N3	AD<9>	EECS	P7	LAN_KE_EECS	46
8	P3	AD<8>	EEDI	P10	LAN_KE_EEDI	46
7	N4	AD<7>	EEDO	N10	LAN_KE_EEDO	46
6	P4	AD<6>				
5	M5	AD<5>	TEST_EN	A13	LAN_KER_TEST_EN	
4	N5	AD<4>	JTCK	L14	LAN_JTCK_JTXD2	46
3	P5	AD<3>	JTRST*	L13	LAN_JRST_JTXD1*	46
2	P6	AD<2>	JTMS	L12	TP_JTMS_FLA5_NC	
1	M7	AD<1>	JTDI	M13	LAN_JTDI_JTRST/SYNC	46
0	N7	AD<0>	JTDO	M14	LAN_JTDO_JTXD0	46

P_C/BE<3..0>*

3	C4	CBE*<3>	PHY_TEST	F12	TP_PHYTST_FLD2_NC
2	F3	CBE*<2>	MSDACN	H12	TP_PHYTST_FLD6_NC
1	L3	CBE*<1>	MSDACP	J13	TP_PHYTST_FLA0_NC
0	M4	CBE*<0>	AUXPWR	J12	LAN_AUXPWR_FLA1_NC

P_REQ5* C3 P_REQ*
P_GNT5* J3 P_GNT*
CK_P_33M_LAN G1 P_CLK CLK_BYP* L7 TP_CLKBYP_MDMCS_ADV10
P_DEVSEL* A4 P_IDSEL CLK_VIEW M8 TP_CLKVIEW_FLSH0E_NC
  H3 P_DEVSEL*
P_PERR* J2 P_PERR* FLSH_SCK N9 TP_FLSHSCK_FLSHCS_NC
P_SERR* F2 P_SERR* FLSH_CE* M9 TP_FLSHCE_FLSHWE_NC
P_FRAME* A2 P_FRAME* FLSH_SI M11 TP_FLSHSI_FLA12_NC
P_IRDY* G3 P_IRDY* FLSH_SO P9 TP_FLSHSO_FLA16_NC
P_TRDY* F1 P_TRDY*
P_PCIRST* B9 P_RST* SDP0 N14 LAN_SDP0_FLA8_JCLK 46
  H1 P_STOP* SDP1 P13 LAN_SDP1_FLA9_JRXD0 46
P_STOP* H2 P_INT* SDP6 N13 LAN_SDP6_FLA10_JRXD1 46
P_INTC* J1 P_PAR SDP7 M12 LAN_SDP7_FLA11_JRXD2 46
P_PAR A6 P_PME*
P_PME* C2 P_M66EN NC C8 LAN_NC_CLKRUN_NC
  NC D12 TP_NC_TI
LAN_M66EN_PRST_NC NC D14 TP_NC_TCK
  NC D10 TP_NC_NC_ISOLEXEC

LAN_PCIZP G4 PCIZP
LAN_PCIZN H4 PCIZN
  A9 LAN_PWRGD
TP_WOL C5 APM_WKUP
  A10 SMB_CLK
LAN_PWRGD/ALTRST* C9 SMB_DATA
  B10 SMB_ALRT*

NC=A1,A14,J4,P1,P14 IC

DESIGN NOTE:
UN-STUFF FOR 82540EM A2
STUFF W/10K 82540EM A1
STUFF W/100K 82551QM

1 R6A12 2 100K 5% 603 EMPTY

1 R6A23 1 33.2 1% 603 CH

V_3P3_PCIVAUX
GPIO_LAN_DISABLE*

1 R6A7 2 0 1A 603 CH

SMB_CLK_RESUME
SMB_DATA_RESUME

VCC3

1 R6A4 2 3.3K 5% 603 CH LAN_SMB_ALRT*

R6A14 0 1A CH 603
R6A18 54.9 1% CH 603

DESIGN NOTE:
UN-STUFF ONLY FOR
82562EX/EZ LAN

DESIGN NOTE:
UN-STUFF FOR 82551QM,
82562EX/EZ LAN

DESIGN NOTE:
UN-STUFF 82551QM,
82562EX/EZ LAN, 82540EM A1

LAN_RBIAS100_2P5 46

1 R6A11 619 1% 2 EMPTY 603

DESIGN NOTE:
STUFF WITH 619 OHM 202286-173
FOR 82551QM, 82562EX/EZ LAN.

DESIGN NOTE:
STUFF WITH 2.49K OHM
1% 202286-231 FOR 82540EM

R6A2 3.3K CH 603
R6A8 2.49K 1% CH 603

REPLACE WITH 549 OHM
1% 202286-168 FOR 82551QM,
82562EX/EZ LAN

1 R6A9 2 3.3K 5% CH 603 V_3P3_PCIVAUX

1 R6B6 2 3.3K 5% 603 CH

DESIGN NOTE:
UN-STUFF FOR 82551QM
82562EX/EZ LAN

R6A6 3.3K EMPTY 603

DESIGN NOTE:
STUFF FOR 82551QM

LAN CONTROLLER

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8 7 6 5 4 3 2 1

D

C

B

A

U6A1
196-PIN PGBA

81 [IN] V_3P3_PCIVAUX

A3 3P3V<10>   VSS<39> B3
A7 3P3V<9>   VSS<38> B7
A11 3P3V<8>   VSS<37> C10
E1 3P3V<7>   VSS<36> C12
K3 3P3V<6>   VSS<35> D5
K4 3P3V<5>   VSS<34> D6
K13 3P3V<4>   VSS<33> D7
N6 3P3V<3>   VSS<32> D8
N8 3P3V<2>   VSS<31> E2
P2 3P3V<1>   VSS<30> E4
P12 3P3V<0>   VSS<29> E5
                         E6
46 [IN] LAN_V_2P5
D9 2P5V<3>   VSS<28> E7
D11 2P5V<2>   VSS<27> E8
G12 2P5V<1>   VSS<26> E9
L8 2P5V<0>   VSS<25> E10
               VSS<24> F4
46 [IN] LAN_V_1P5   VSS<23> F5
E12 1P5V<27>   VSS<22> F6
G5 1P5V<26>   VSS<21> F7
G6 1P5V<25>   VSS<20> F8
G13 1P5V<24>   VSS<19> F9
H5 1P5V<23>   VSS<18> F10
H6 1P5V<22>   VSS<17> F11
H7 1P5V<21>   VSS<16> G7
H8 1P5V<20>   VSS<15> G8
J5 1P5V<19>   VSS<14> G9
J6 1P5V<18>   VSS<13> G10
J7 1P5V<17>   VSS<12> G11
J8 1P5V<16>   VSS<11> G14
J9 1P5V<15>   VSS<10> H9
J10 1P5V<14>   VSS<9>   H10
J11 1P5V<13>   VSS<8>   K2
K5 1P5V<12>   VSS<7>   K12
K6 1P5V<11>   VSS<6>   L6
K7 1P5V<10>   VSS<5>   L11
K8 1P5V<9>   VSS<4>   M6
K9 1P5V<8>   VSS<3>   N1
K10 1P5V<7>   VSS<2>   N12
K11 1P5V<6>   VSS<1>   P8
L4 1P5V<5>   VSS<0>
L5 1P5V<4>
L9 1P5V<3>   ALTCLK125 D4
L10 1P5V<2>   VSS   D13
E11 1P5V<1>   VIO   G2
H11 1P5V<0>   NC

NC=A1,A14,J4,P1,P14   IC

CAD NOTE:
PLACE CLOSE TO VIO BALL (G2)

81 [IN] V_3P3_PCIVAUX 1 R6A212
100K 5%
603   CH

LAN_VIO

1 C6A10
.1UF
20%
35V
603
2

DESIGN NOTE:
STUFF FOR 82540EM & 82551QM

LAN POWER / GND

CR-46

8　7　6　5　4　3　2　1

DESIGN NOTE:
LAN CONNECT INTERFACE TO THE 82562EX/EZ CAN NOT BE STUFFED CONCURRENTLY
82562EX/EZ IS A DESIGN ENGINEERING EVALUATION FEATURE

82562EX/EZ LAN CONNECT INTERFACE STUFFING RESISTORS

| | RP8F1 | |
31 29 OUT　ICH_LAN_TXD0_R　4　5　LAN_JTDO_JTXD0　OUT 44
33　5% 063W
SM　EMPTY

RP7F3
31 IN　ICH_LAN_RXD0_R　4　5　LAN_SDP1_FLA9_JRXD0　IN 44
33　5% 063W
SM　EMPTY

RP8F1
31 29 OUT　ICH_LAN_TXD1_R　3　6　LAN_JRST_JTXD1　OUT 44
33　5% 063W
SM　EMPTY

RP7F3
31 IN　ICH_LAN_RXD1_R　3　6　LAN_SDP6_FLA10_JRXD1　IN 44
33　5% 063W
SM　EMPTY

RP8F1
31 29 OUT　ICH_LAN_TXD2_R　1　8　LAN_JTCK_JTXD2　OUT 44
33　5% 063W
SM　EMPTY

RP7F3
31 IN　ICH_LAN_RXD2_R　2　7　LAN_SDP7_FLA11_JRXD2　IN 44
33　5% 063W
SM　EMPTY

RP8F1
31 29 OUT　ICH_LAN_RST_R　2　7　LAN_JTDI_JTRST/SYNC　OUT 44
33　5% 063W
SM　EMPTY

RP7F3
31 IN　ICH_LAN_CLK_R　2　7　LAN_SDP0_FLA8_JCLK　IN 44
33　5% 063W
SM　EMPTY

CAD NOTE:
R-PAKS SHOULD BE PLACED CLOSE TO THE ICH

DESIGN NOTE:
0 OHM SERIES "R" ON
82562EX/EZ EEPROM
ORG (PIN 6) IS IN
PLACE FOR EVAL; MAY
BE REMOVED ON PRODUCT.

DESIGN NOTE:
0 OHM SERIES "RPACK"
TO 82562EZ/EZ EEPROM
IS IN PLACE FOR
OPTION OF STUFFING
CNR W/OUT LAN DOWN
(STUB REDUCTION).

VOLTAGE REGULATION –
FOR 82540EM 1.5V RAIL ONLY

81 IN　V_3P3_PCIVAUX

DESIGN NOTE:
DO NOT STUFF UNLESS
KENAI STEPPING IS
REVISIONED

R5A3
5100
5%
EMPTY
603

C5A3
10.0UF
20%
X5R
1206

C5A4
1UF
20%
Y5V
603

44 IN　LAN_LX2_1P5　R5A2　AN_CTRL_1P5
0　1A
603　CH

Q6A2
BCP69T1
XSTR
A70751-001

R5A4
30K
603　CH

DESIGN NOTE:
STUFF FOR KENAI

LAN_V_1P5　OUT 46 45

VOLTAGE REGULATION –
FOR 82540EM 2.5V RAIL ONLY

81 IN　V_3P3_PCIVAUX

R6A3
5100
5%
CH 603

C6A2
10.0UF
20%
6.3V
1206

C6A6
1UF
20%
25V
603

44 IN　LAN_RBIAS100_2P5　R6A10　AN_CTRL_2P5
0　1A
603　CH

Q6A1
BCP69T1
XSTR
A70751-001

R6A5
100K 5%
603 EMPTY
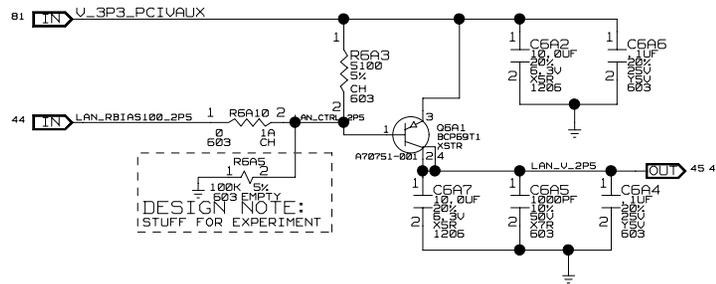
DESIGN NOTE:
STUFF FOR EXPERIMENT

C6A7
10.0UF
20%
6.3V
1206

C6A5
1000PF
10%
X7R
603

C6A4
1UF
20%
Y5V
603

LAN_V_2P5　OUT 45 47

82540EM/82551QM EEPROM
DESIGN NOTE:
STUFF THIS EEPROM ONLY WITH 82540EM AND 82551QM.
SKUS. PLACE NEAR LAN CONTROLLER.

81 IN　V_3P3_PCIVAUX　R6BB　EEPROM_ORG_LAN
1　2
0　1A
603　CH

44 OUT　LAN_KE_EEDO

44 IN　LAN_KE_EEDI

44 IN　LAN_KE_EECS

U6B1
AT93C66
4 DO ORG 6
3 DI
2 SK VCC 8
1 CS GND
NC=7
IC 5
729345-001

44 IN　LAN_KE_EESK

81 IN　V_3P3_PCIVAUX
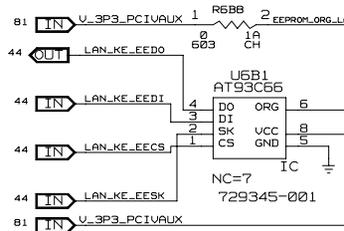
82562EX/EZ EEPROM
DESIGN NOTE:
STUFF THIS EEPROM ONLY WITH 82562EX/EZ
SKUS. PLACE NEAR ICH.

84 IN　V_3P3_STBY　R7F2　EEPROM_ORG_ICH
1　2
0　1A
603　EMPTY

RP7F4
29 31 OUT　ICH_EE_DIN_R　4　5　LAN_EE4
5% 063W
SM　EMPTY

RP7F4
29 IN　ICH_EE_DOUT_R　3　6　LAN_EE3
5% 063W
SM　EMPTY

U7F2
AT93C46A_66
3 DI
2 CS DO 6
1 SK ORG 5

RP7F4
29 IN　ICH_EE_CS_R　1　8　LAN_EE1
5% 063W
SM　EMPTY

VCC=8
GND=5
NC=7　109868-001
VCC=V_3P3_STBY
EMPTY

RP7F4
29 IN　ICH_EE_CLK_R　2　7　LAN_EE2
5% 063W
SM　EMPTY

LAN DECOUPLING
DECOUPLING CAPS SHARE BETWEEN
82540EM, 82551QM, 82562EX/EZ

81 IN　V_3P3_PCIVAUX　R6A13
1　2
0　1A
603　EMPTY

DESIGN NOTE:
STUFF FOR 82551QM,
82562EX/EZ LAN

LAN_V_1P5　OUT 46 45

C6A13
10.0UF
20%
6.3V
X5R
1206

C6A15
1UF
20%
Y5V
603

C6B5
1UF
20%
Y5V
603

C6B5
1UF
20%
Y5V
603

C6B4
1UF
20%
Y5V
603

C6B6
1UF
20%
Y5V
603

C6B7
1UF
20%
Y5V
603

81 IN　V_3P3_PCIVAUX

81 IN　V_3P3_PCIVAUX

C6A1
10.0UF
20%
6.3V
X5R
1206

C6B1
4.7UF
20%
EMPTY
1206

C6A8
1UF
20%
Y5V
603

C6B9
1UF
20%
Y5V
603

C6B8
1UF
20%
Y5V
603

LAN CRYSTAL
DESIGN NOTE:
STUFF FOR 82551QM

44 OUT　LAN_LX1　R6B3
1　2
0　5%
402 EMPTY

44 IN　LAN_LX2_1P5　R6B5
1　2
0　5%
402 EMPTY

R6B2
10M　5%
603 EMPTY

44 OUT　LAN_KX1　R6B4
1　2
0　5%
402 CH

LAN_XTAL1

25.000MHZ Y6B1
630770-011
XTAL SM
LAN_XTAL2

C6B14
33PF 5%
50V
NP0
603

44 IN　LAN_KX2　R6B7
1　2
0　5%
402 CH
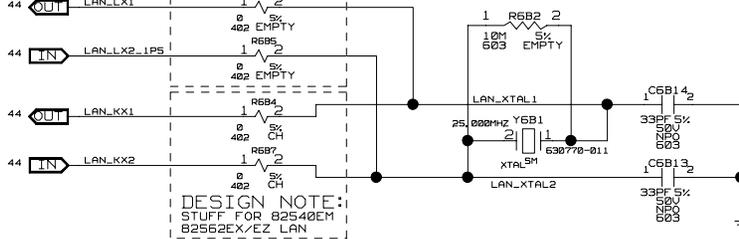
DESIGN NOTE:
STUFF FOR 82540EM
82562EX/EZ LAN

C6B13
33PF 5%
50V
NP0
603

LAN CONTROL / EEPROM

DESIGN NOTE:
CONNECTOR STUFFING OPTIONS:
DEFAULT: USE A74307-001 WITH GIGABIT (82540EM) DESIGNS & (2) USB
OPTION: USE A74314-001 WITH 10/100 (82551QM) DESIGNS & (2) USB
OPTION: USE 749193-001 DOUBLE STACK USB

LED DECOUPLING
CAD NOTE:
LED CAPS SHOULD BE PLACED
NEXT TO CONNECTOR

LAN CONNECTOR
DESIGN NOTE:
USE A74307-001 WITH GIGABIT (82545EM) DESIGNS
USE A74314-001 WITH 10/100 (82551QM) DESIGNS

LAN BI-COLOR SPEED LED

10 MBPS	OFF
100 MBPS	GREEN
1000 MBPS	YELLOW

CAD NOTE:
MAKE TRACE THICK

46 IN   LAN_V_2P5

1000
JA4A1
GBE_MAGJACK3_10

47 44 BI	LAN_MDI_0 10	TD0+
47 44 BI	LAN_MDI_0* 11	TD0-
		VCT 9 VCT_CONN
47 44 BI	LAN_MDI_1 12	TD1+
47 44 BI	LAN_MDI_1* 13	TD1-
	SGND 18	
47 44 BI	LAN_MDI_2 14	TD2+
47 44 BI	LAN_MDI_2* 15	TD2-
47 44 BI	LAN_MDI_3 16	TD3+
47 44 BI	LAN_MDI_3* 17	TD3-

A74307-001   IO
GND=23..30

R5B1
0   1A
603   CH

C4B21
1UF
50V
Y5V
603

DESIGN NOTE:
STUFF FOR 82540EM;
UNSTUFF FOR 82551QM
& 82562EX/EZ

44 IN   LAN_ACTLED*
C4B2
470PF
10%
50V
X7R
603

47 44 OUT   LAN_LINK_UP*
C4B3
470PF
10%
50V
X7R
603

47 44 BI   LAN_LINK100*
C4B1
470PF
10%
50V
X7R
603
"X7R"

47 BI   LAN_LINK
C5A10
470PF
10%
50V
X7R
603

USB STACK

B3 IN   VREG_USB_BP_LEFT
DUAL LAYOUT

USB STACK
JA4A1
2 X USB

33 BI	USB_BACK1_R*	1 1000
33 BI	USB_BACK1_R	2
		3
		4
33 BI	USB_BACK2_R*	5 1000
33 BI	USB_BACK2_R	6
		7
		8
		IO

1000
JA4A1
GRN_LED
44 IN   LAN_ACTLED* 20   19   LAN_LINK_UP*   OUT 44 47
IO

1000
JA4A1
GRN_LED
47 BI   LAN_LINK 22   21 LAN_LINK100*   BI 44 47
IO
YLW_LED

STUFFING OPTIONS FOR LED ENABLING
DESIGN NOTE:
STUFF FOR 10/100 (82551QM, 82562EX/EZ

R5A5
1   0   5%   2   V_3P3_PCIVAUX   IN B1
402 EMPTY

47 BI   LAN_LINK
DESIGN NOTE:
STUFF FOR GIGABIT (82540EM)

R5A6
1   0   2   LAN_LINK1000*   BI 44
402 5%
CH

DIFFERENTIAL PAIR TERMINATIONS

47 44 BI   LAN_MDI_0
MDI_DIV_0_0*
DESIGN NOTE:
STUFF FOR 82540EM ONLY
R5A15
49.9
1%
1
C5A9
0.01UF
10%
16V
X7R
402
2
R5A17
49.9
1%
CH
402
47 44 BI   LAN_MDI_0*

47 44 BI   LAN_MDI_1
MDI_DIV_1_1*
DESIGN NOTE:
STUFF FOR 82540EM ONLY
R5A19
49.9
1%
1
C5A11
0.01UF
10%
16V
X7R
402
2
R5A20
49.9
1%
CH
402
47 44 BI   LAN_MDI_1*
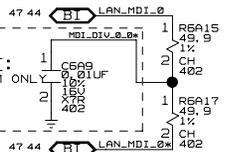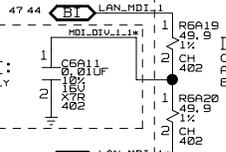
DESIGN NOTE:
CHANGE TO 62 OHM
A36093-077 FOR 82551QM
82562EX/EZ LAN

47 44 BI   LAN_MDI_2
MDI_DIV_2_2*
R5A22
49.9
1%
1
C5A12
0.01UF
10%
16V
X7R
402
2
R5A24
49.9
1%
CH
402
47 44 BI   LAN_MDI_2*
DESIGN NOTE:
STUFF FOR 82540EM ONLY

47 44 BI   LAN_MDI_3
MDI_DIV_3_3*
R5A25
49.9
1%
1
C5A14
0.01UF
10%
16V
X7R
402
2
R5A26
49.9
1%
CH
402
47 44 BI   LAN_MDI_3*

LAN / USB CONNECTOR

AUD_LINK_SDO   30 IN
AUD_LINK_SYNC   30 IN

CK_14M_AUD IN 14

R9B2
0   1A
603 CH

CAD NOTE:
PLACE CAREFULLY: NO STUBS
DESIGN NOTE:
STUFF FOR ALL CODECS WITH 14 MHZ CLK

DESIGN NOTE:
STUFF ONLY IF AUDIO IS PRESENT AND NO CNR

AUD_LINK_RST*   29 IN
R8B13
0 603 1A EMPTY

DESIGN NOTE:
STUFF IF AUDIO AND CNR ARE PRESENT

CDC_DWN_RST*   67 IN
R8B12
1K 603 5% CH

AUD_CK_24M_XTL_I

Y9B1
24.576MHZ
630770-010
SM EMPTY

C9B6
52PF 5% 50V EMPTY 603 603275-112 "NPO"

R8B10
0 1A
603 CH

AUD_CK_24M_XTL_O

DESIGN NOTE:
STUFF FOR 9766 SUPPORT WITH 14MHZ CLK

AUD_LINK_BCLK BI 43 29
R8B2
33 603 5% CH
C8B2
10PF 50V EMPTY 603

AUD_LINK_SDI2 OUT 29 43
R8B3
33 603 5% CH

SPKR 27 IN
R8B9 PC_BEEP_AMP
10K 603 5%

PC_BEEP_AMP OUT 55

R8B4
100 603 CH
C8B3
1UF 20% 25V Y5V 603

U8A2
STAC9766
A62521-002
NC=49 IC

2 XTL_IN
5 SDATA_OUT
10 SYNC
11 RESET

3 XTL_OUT
6 BIT_CLK
8 SDATA_IN

CDC_RESET*

AUD_STRAP_45 45 ID0
AUD_STRAP_46 46 ID1
SPDIF_SENSE   47 EAPD

55 BI

48 SPDIF AUD_SPDIF OUT 52

R7A6   R7A13
330K   330K
5%   5%
EMPTY 603   EMPTY 603

DESIGN NOTE:
ENGINEER DEBUG SITES FOR 9766

AUD_MONO_IN 50 IN
R8B1 AUD_MONO_IN.PN1
0 603 1A CH
C8B1
1.0UF 10% 10V Y5V 603

R8B8
5.6K EMPTY 603

DESIGN NOTE:
STUFF ONLY IF ANALOG MODEM INPUT REQUIRES ADDITIONAL ATTENUATION

39 HP_OUT_L
41 HP_OUT_R

AUD_CDC_LOUT OUT 52
AUD_CDC_ROUT OUT 52

AUD_PCBEEP_IN_CODEC 12 PC_BEEP
AUD_MONO_IN_R   13 PHONE
AUD_LAUXIN   14 AUX_L
AUD_RAUXIN   15 AUX_R
TP_VID_L   16 VIDEO_L
TP_VID_R   17 VIDEO_R
AUD_LCD   18 CD_L
AUD_CDGND   19 CD_GND
AUD_RCD   20 CD_R
AUD_MIC_IN   21 MIC1
TP_AUD_MIC2_IN   22 MIC2
AUD_LLINEIN   23 LINE_IN_L
AUD_RLINEIN   24 LINE_IN_R
AUD_3D_C   34 NC_34

35 LINE_OUT_L TP_AUD_LINE_LOUT_R
36 LINE_OUT_R TP_AUD_LINE_ROUT_R
37 MONO_OUT   AUD_MONO_OUT_C OUT 50

50 IN
50 IN
50 IN
50 IN
50 IN
51 IN
50 IN
50 IN

VCC3

1 DVDD1
9 DVDD2
4 DVSS1
7 DVSS2
25 AVDD1
38 AVDD2
26 AVSS1
42 AVSS2

27 REFFLT
28 VREFOUT
29 AFLT1
30 AFLT2
31 NC_31
32 CAP2
33 NC_33   AUD_3D_R
43 GPIO0   AVDD3_ANALOG_R
44 GPIO1   AVSS3_GNDSTRAP
40 HP_COMM

AUD_A_REFFLT OUT 49
AUD_A_VREF   OUT 55
AUD_AFLT1   OUT 49
AUD_AFLT2   OUT 49
AUD_AFLT3   OUT 49
AUD_AFLT4   OUT 49

C9B3   C9B8   C8B4
1UF   10UF   1UF
20%   20%   20%
25V   35V   25V
Y5V   ELEC   Y5V
603   RDL   603
            "201307-102"

V_5P0_AUD_ANALOG 54 IN

CBA9   CBA10
1.0UF   1.0UF
10%   20%
10V   35V
Y5V   Y5V
603   603

V_5P0_AUD_ANALOG 54 IN

AVSS2_DCPL

R9A4
0 1A
603 CH

C9A11   C9A7
1.0UF   1.0UF
10%   20%
10V   35V
Y5V   Y5V
603   603

AUDIO CODEC

CR-49

CAD NOTE:
KEEP CAPS AS CLOSE
AS POSSIBLE TO AC97
CODEC.

48 IN AUD_A_REFFLT

48 IN AUD_AFLT1
48 IN AUD_AFLT2
48 IN AUD_AFLT4

644066-001
1 C8A2
1UF
10%
10V
X7R
2 605

602433-016
1 C9A3
1UF
20%
6.3V
X5R
2 603

1 C8A1
390PF
5%
50V
COG
2 603

1 C8A3
390PF
5%
50V
COG
2 603

1 C8A9
1UF
10%
10V
X7R
2 603

1 C9A5
1UF
10%
10V
X7R
2 603

"X7R"

"COG"   "COG"

AUDIO

8 7 6 5 4 3 2 1

D

663573-011
J7B2
1X4HDR
TELEPHONY
GREEN
ATAPI HEADER

AUD_MONO_IN — OUT 48
C7A6
AUD_MONO_OUT_C_HDR 1 2 AUD_MONO_OUT_C — IN 48
1.0UF 10%
10V
Y5V
603

CAD NOTE:
PLACE CAP CLOSE TO CODEC

C

663573-010
J7B1
1X4HDR
AUX IN
WHITE
ATAPI HEADER

AUD_LAUXIN_R
RP8B1
1 8
6.8K 5% .25W
SM IC
AUD_LAUXIN_C
CBA23
1 2
X5R 603
1UF 20%
6.3V
AUD_LAUXIN — OUT 48

AUD_RAUXIN_R
RP8B1
4 5
6.8K 5% .25W
SM IC
AUD_RAUXIN_C
CBA22
1 2
X5R 603
1UF 20%
6.3V
AUD_RAUXIN — OUT 48

RP8B1 6
6.8K
5%
.25W
IC
SM
3

RP8B1 7
6.8K
5%
.25W
IC
SM
2

B

663573-001
J8B1
1X4HDR
CD IN
BLACK
ATAPI HEADER

AUD_LCD_R
RP8B2
1 8
6.8K 5% .25W
SM IC
AUD_LCD_C
CBA21
1 2
X5R 603
1UF 20%
6.3V
AUD_LCD — OUT 48

AUD_CDGND_R
RP8B2
3 6
6.8K 5% .25W
SM IC
AUD_CDGND_C
CBA20
1 2
X5R 603
1UF 20%
6.3V
AUD_CDGND — OUT 48

RP8B2
2 7
6.8K 5% .25W
SM IC

AUD_RCD_R
RP8B2
4 5
6.8K 5% .25W
SM IC
AUD_RCD_C
CBA17
1 2
X5R 603
1UF 20%
6.3V
AUD_RCD — OUT 48

RP8B3 1
6.8K
5%
.25W
IC
SM
8

RP8B3 2
6.8K
5%
.25W
IC
SM
7

RP8B3 3
6.8K
5%
.25W
IC
SM
6

RP8B3 4
6.8K
5%
.25W
IC
SM
5

A

J5A1
3 STACK AUDIOJACK
35
34
33
32
JACK

AUD_RLINEIN_R 1
FB5A3
0.2A
FB
2
AUD_RLINEIN_R_FB
RBA7
1 2
6.8K 5%
603 CH
AUD_RLINEIN_C
CBA14
1 2
X5R 603
1UF 20%
6.3V
AUD_RLINEIN — OUT 48

AUD_LLINEIN_R 1
FB5A2
0.2A
FB
2
AUD_LLINEIN_R_FB
RBA8
1 2
6.8K 5%
603 CH
AUD_LLINEIN_C
CBA15
1 2
X5R 603
1UF 20%
6.3V
AUD_LLINEIN — OUT 48

C5A7
220PF
10%
50V
X7R
603
1
2

C5A5
220PF
10%
50V
X7R
603
1
2

OUT 51

RBA13
1
6.8K
5%
CH
603
2

RBA12
1
6.8K
5%
CH
603
2

AUD_JACK_GND — OUT 51 52 54

AUDIO CONNECTORS

8 7 6 5 4 3 2 1

AUDIO MIC IN

DESIGN NOTE:
USE 75 OHM VALUE
FOR THESE SITES WHEN
SPDIF IS USED
PART# 202285-022

DESIGN NOTE:
STUFF ONLY WHEN
FRONT PANEL HEADER
IS NOT STUFFED

DESIGN NOTE:
WHEN FRONT PANEL DONGLE IS PLUGGED INTO HEADER AND HEAD-
PHONE IS INSERTED, BACK PANEL AUDIO OUTPUT IS DISABLED.

AUD_R_FNTOUT [OUT] 53
AUD_L_FNTOUT [OUT] 53

STEREO
LINE OUT

UNKN
600
0.2A
BROAD

AUD_R_PCSPKR [OUT] 55

J5A1
3 STACK AUDIOJACK

25
24
23
22

JACK

48 [IN] AUD_CDC_ROUT

C7A7
100UF
PART# 201307-004
+
20% 25V
ELEC
RDL

AUD_R_LINEOUT_PL_PH1

1 RBA2B 2
10   5%
603   CH

1 R7A1 2 AUD_R_RETIN
0   1A
603   EMPTY

[OUT] 52 53 55

55 53 52 [BI] AUD_R_RETIN   1   2 AUD_R_LINEOUT
                            FB5A6
                            FB

48 [IN] AUD_CDC_LOUT

C7A1
100UF
PART# 201307-004
+
20% 25V
ELEC
RDL

AUD_L_LINEOUT_PL_PH1

1 RBA6 2
10   5%
603   CH

1 R7A2 2 AUD_L_RETIN
0   1A
603   EMPTY

[OUT] 52 53 55

55 53 52 [BI] AUD_L_RETIN   1   2 AUD_L_LINEOUT
                            FB5A1
                            FB

UNKN
600
0.2A
BROAD

AUD_L_PCSPKR [OUT] 55

2 RBA21   2 RBA25
  470   470
  5%   5%
  CH   CH
  603   603
1   1

C5A6   C5A2
1 220PF   1 220PF
  10%   10%
  50V   50V
  X7R   X7R
2 603   2 603

AUD_JACK_GND [OUT] 50 51 54

AUDIOJACK SUPPORTS SPDIF FEATURE WHEN
SPDIF CIRCUITRY IS STUFFED

48 [IN] AUD_SPDIF

1 C9A1 2
4700PF 20%
50V
EMPTY
603

AUD_SPDIF_LEFT

1 R9A1 2
330   5%
603   EMPTY

1 R9A9
  10K
  5%
2 EMPTY 603

1 C9A12
  470PF
  10%
  50V
2 EMPTY 603

DESIGN NOTE:
STUFF SITES FOR SPDIF FEATURE
EMPTY 10K SITE FOR DYNAMIC SPDIF SENSE

AUDIO

DESIGN EVALUATION USES SUITCASE JUMPERS

DESIGN NOTE:
FRONT PANEL DONGLE W/OUTPUT PLUG MUST HAVE SPRING CLIPS ROUTED BACK TO PINS 6 & 10
TO ALLOW BACK PANEL AUDIO AS ALTERNATIVE WHEN HP-JACK ISN'T PLUGGED INTO FRONT PANEL

DESIGN NOTE:
WHEN NO FRONT PANEL DONGLE IS PLUGGED INTO HEADER, SUITCASE JUMPERS
CAN BE PLACED ON PIN 5-6, 9-10 TO ALLOW BACK PANEL AUDIO OUTPUT

DEFAULT CONFIGURATION IS FOR FP DONGLE

J7B4
2X5HDR_8

51 OUT	AUD_MIC_IN_FP	1
51 IN	AUD_MIC_BIAS	3
52 IN	AUD_R_FNTOUT	5
	TP_HP_ON 7	
52 IN	AUD_L_FNTOUT	9

2	V_5P0_AUD_ANALOG	IN 54
4		
6	AUD_R_RETIN	OUT 52 55
10	AUD_L_RETIN	OUT 52 55

HDR
109717-205

1 C7B14	1 C7B12	1 C7B9	1 C7B5	1 C7B3	1 C7B8	1 C7B13
47PF	47PF	47PF	47PF	47PF	47PF	47PF
5%	5%	5%	5%	5%	5%	5%
50V	50V	50V	50V	50V	50V	50V
2 EMPTY	2 EMPTY	2 EMPTY	2 EMPTY	2 EMPTY	2 EMPTY	2 EMPTY
503	503	503	503	503	503	503

CAD NOTE:
PLACE NEAR AUDIO CIRCUIT

AUDIO FRONT PANEL

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VREG AUDIO OPTION

SPECIAL OPTION
SIGNAL QUALITY SOLUTION
UNSTUFF 0 OHM RESISTOR

80 IN> V_5P0_STBY

108506-004

201005-018

C9B5
.1UF
20%
25V
Y5V
603

C9B4
10UF
10%
10V
Y5V
603

R9B4
603 1A
0
CH

L9B1
.27UH
EMPTY

JEDEC TYPE
SML1210

V_5P0_AUD_ANALOG OUT> 54 48 51 53 55
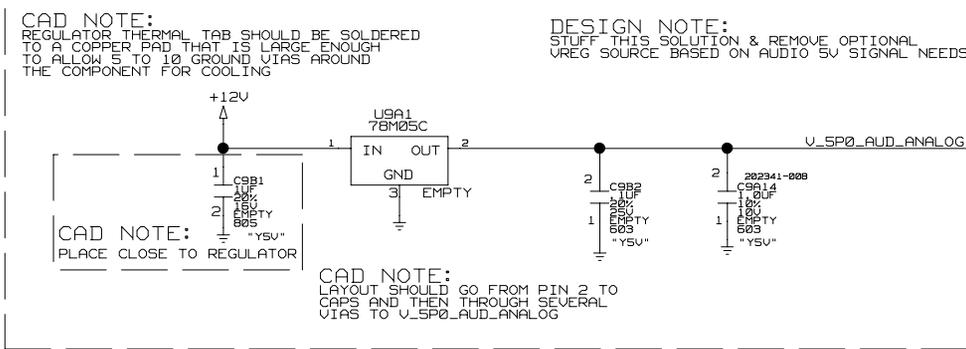
CAD NOTE:
REGULATOR THERMAL TAB SHOULD BE SOLDERED
TO A COPPER PAD THAT IS LARGE ENOUGH
TO ALLOW 5 TO 10 GROUND VIAS AROUND
THE COMPONENT FOR COOLING

DESIGN NOTE:
STUFF THIS SOLUTION & REMOVE OPTIONAL
VREG SOURCE BASED ON AUDIO 5V SIGNAL NEEDS

+12V

U9A1
78M05C

1 IN OUT 2

GND

3 EMPTY

C9B1
.1UF
20%
16V
EMPTY
805

"Y5V"

CAD NOTE:
PLACE CLOSE TO REGULATOR

V_5P0_AUD_ANALOG

C9B2
.1UF
20%
EMPTY
603

"Y5V"

C9A14
10UF
10%
10V
EMPTY
603

"Y5V"

202341-008

C9A13
10UF
20%
35V
ELEC
RDL

"201307-102"

OUT> 54 48 51 53 55

CAD NOTE:
LAYOUT SHOULD GO FROM PIN 2 TO
CAPS AND THEN THROUGH SEVERAL
VIAS TO V_5P0_AUD_ANALOG

DESIGN NOTE:
ALWAYS STUFF THIS CAP

52 51 50 IN> AUD_JACK_GND

108506-004

108506-004

C5A1
.1UF
20%
25V
EMPTY
603

"Y5V"

R5A1
603 1A
0
EMPTY

R8A1
603 1A
0
CH
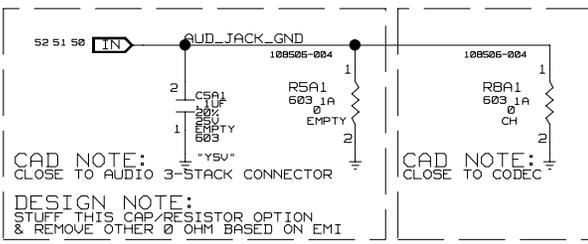
CAD NOTE:
CLOSE TO AUDIO 3-STACK CONNECTOR

CAD NOTE:
CLOSE TO CODEC

DESIGN NOTE:
STUFF THIS CAP/RESISTOR OPTION
& REMOVE OTHER 0 OHM BASED ON EMI

AUDIO VREG

FOR AUDIO MODULE EVALUATION ONLY; SPDIF SENSE SUPPORT,

CUSTOM INTERNAL
AUDIO AMPLIFIER
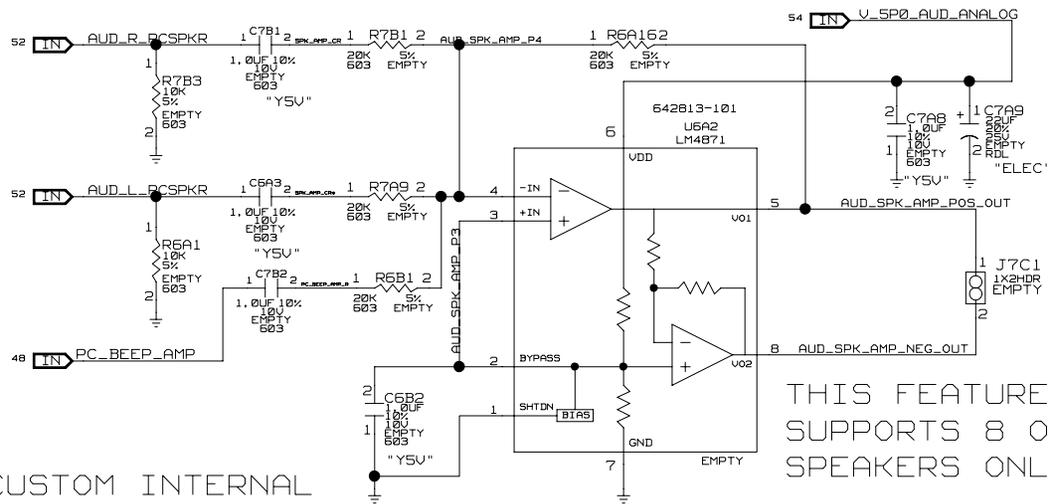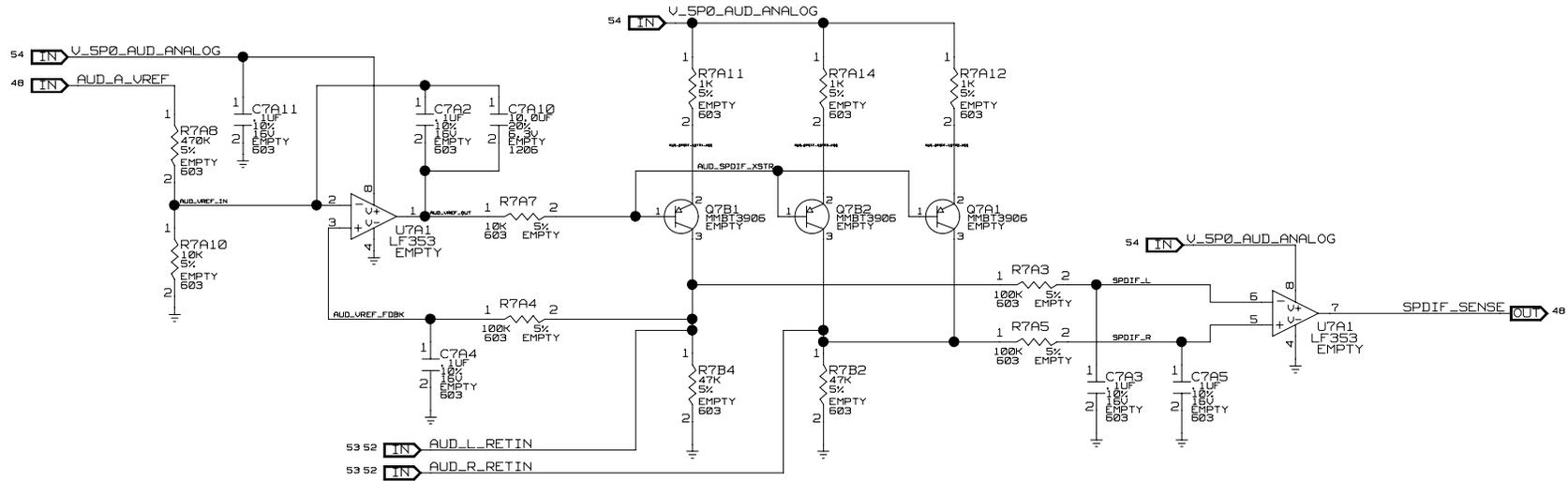
THIS FEATURE
SUPPORTS 8 OHM
SPEAKERS ONLY

SP DIF / CUSTOM FEATURE

BOM=OPT_CUST_I

DRAWING
NGRVP.SCH_1.55
Wed Oct 23 10:38:56 2002

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SECURITY: TPM (TRUSTED PLATFORM MODULE)

ATMEL AT97SC3201

L_AD<3..0>

99 98 66 61 27 [BI]

U6J2
AT97SC3201

3   24 LAD(3)   XTAL1   9
2   23 LAD(2)   XTAL2   8
1   26 LAD(1)
0   25 LAD(0)

IOA   3   TP_IOA
IOB   6   TP_IOB
IOC   22 TP_IOC

CK_P_33M_TPM   14
P_PCIRST*   30
L_FRAME*   27
SER_IRQ   98 61 27

28 LCLK
1   LRESET*
2   LFRAME*
27 SIRQ

XTAMPER   21 TCPA_XTAMPER
CLKRUN*   7   TCPA_JMP

V_3P0_BAT_VREG   81
V_3P3_STBY   84

14 VBB
13 VCC

GND   12

C6H7
4.7UF
20%
16V
EMPTY
1206   "Y5V"

NC=11,12 (SOIC)
NC=4,5,10,11,15,16,17,18,19,20 (SSOP)

EMPTY

Y6J1
32.768KHZ   619601-001
1   4
2   3
SM
EMPTY

TCPA_XTAL1
C6J1
1   2
10PF 5%
50V
EMPTY
603   "NPO"

TCPA_XTAL2
C6J2
1   2
10PF 5%
50V
EMPTY
603   "NPO"

R6H20
3.3K
5%
EMPTY
603
1
2

R6J2
1   2
3.3K   5%
603   EMPTY

V_3P3_STBY   [IN] 84

1394/USB HEADER BACK PANEL

1394 HEADER FRONT PANEL

1394 HEADER FRONT PANEL

1394 USB FRONT PANEL HEADER

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1394 CONTROLLER

DOCUMENT NUMBER	PAGE	REV
A95397	58	1.5

DRAWING
NGRVP.SCH_1.58
Wed Oct 23 10:38:58 2002

"LM1117 ADJ REGULATOR"

VCC3

ADJ
U9G1
MC33269   A57605-002

2 | IN   OUT | 3

ADJ

1   SM

1 | 202341-008
C9G5
1.0UF
10%
Y5V
2 | 10V
603

VREG_SATA_ADJ

V_1P8_SATA   OUT > 60 85

1
R9G2
100
1%
CH
2   603

1 | C9G2
+   100UF
20%
35V
ELEC
2 | "201307-004"

1
R9G1
45.3
1%
CH
2   603

1 | C9G6
1UF
10%
16V
X7R
2 | 603

SATA VREG

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SATA CONTROLLER

CR-61

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

DESIGN NOTE:
EMPTY IF HECETA6 IS STUFFED
EMPTY IF HECETA4 IS STUFFED

CPU_FAN_PWM NEEDS DESIGN MODIFICATION FOR HECETA4 SUPPORT
TO ALLOW PWM CONTROL THROUGH FET ON HEC4 PIN-16 WHILE NOT PULSING
THE FP_RST SIGNAL THROUGH THE 0 OHM RESISTOR (ALSO ON HEC4 PIN-16)

R1J12
CPU_FAN_PWM   OUT 68 72

DESIGN NOTE:
EMPTY IF HECETA6 IS STUFFED
STUFF IF HECETA4 IS STUFFED

R1J11
FNT_REAR_FAN_PWM3   OUT 68 72

DESIGN NOTE:
REMOVE OR EMPTY SITES
FOR PRODUCT;
BIOS AUTO-DETECTS ADDRESS
WITHOUT STUFFING SITES

84 IN V_3P3_STBY
84 IN V_3P3_STBY
84 IN V_3P3_STBY

VCC3
VCC3

U1H1
PORT_ANGELES   A78930-001

RP1J3 10K 5% .063W IC SM
RP1J3 10K 5% .063W IC SM

R1J10 4.7K 5% EMPTY 603
R1J12 4.7K 5% EMPTY 603

27 OUT IO_PME*

FLOPPY
62 OUT SIO_FDD_DRVDEN0 22 DRVDEN0
62 OUT SIO_FDD_DRVDEN1 21 DRVDEN1
62 OUT SIO_FDD_MTR0* 19   MTR0*
62 OUT SIO_FDD_DS0* 18   DS0*
62 OUT SIO_FDD_DIR* 17   DIR*
62 OUT SIO_FDD_STEP* 16   STEP*
62 OUT SIO_FDD_WDATA* 15   WDATA*
62 OUT SIO_FDD_WGATE* 14   WGATE*
62 OUT SIO_FDD_HDSEL* 10   HDSEL*
62 IN SIO_FDD_INDEX* 20   INDEX*
62 IN SIO_FDD_TRK0* 13   TRK0*
62 IN SIO_FDD_WRTPRT* 12 WRTPRT*
62 IN SIO_FDD_RDATA* 11   RDATA*
62 IN SIO_FDD_DSKCHG* 9   DSKCHG*

GPIO
VCC3(4) 60
VCC3(3) 49
VCC3(2) 31
VCC3(1) 6
V_3P3_STBY(3) 107
V_3P3_STBY(2) 93
V_3P3_STBY(1) 76

GPIO0 103 I_PA_FAN1
GPIO1 104 I_PA_FAN2
GPIO2 105 GP21_STRAP
GPIO3 106 GP20_STRAP
GPIO4 108 IO_SMI*   27
GPIO5 109 PA_GPIO5

VCC3

PS/2
KDAT 4 SIO_KBDATA   63
KCLK 3 SIO_KBCLOCK 63
MDAT 2 SIO_MSDATA   63
MCLK 1 SIO_MSCLOCK 63
KBRST* 7 KBRST*
GA20M 5   A20GATE

LPC
99   IO_PME*
062 LAD<0>
161 LAD<1>
259 LAD<2>
357 LAD<3>
99 98 66 56 27 BI L_AD<3..0>

27 IN L_FRAME* 56 LFRAME*
27 OUT L_DRQ* 54   LDRQ*
SIO_PCIRST* 63   PCI_RESET*
30 IN P_PCIRST*   52 LPCPD*
52 IN ICH_SUS_STAT
14 IN CK_P_33M_SIO 55 PCI_CLK
98 56 27 BI SER_IRQ   SER_IRQ

R1H5 603 0 1A

SERIAL
65 IN SIO_COM_RXD1 25 RXD
65 OUT SIO_COM_TXD1 27 TXD/TEST_EN2
65 IN SIO_COM_DSR1* 24 DSR*
65 OUT SIO_COM_RTS1* 26 RTS*
65 IN SIO_COM_CTS1* 28 CTS*
65 OUT SIO_COM_DTR1* 30 DTR*/XOR
65 IN SIO_COM_RI1* 32 RI*
65 IN SIO_COM_DCD1* 23 DCD*

PARALLEL
INITP* 48 SIO_LPT_INIT*   64
SLCTIN* 47 SIO_LPT_SLCTIN* 64
PD<0> 44 0
PD<1> 43 1
PD<2> 42 2
PD<3> 41 3
PD<4> 40 4
PD<5> 39 5
PD<6> 38 6
PD<7> 37 7   SIO_LPT_PD<7..0> 64
SLCT 33 SIO_LPT_SLCT   64
PE 34   SIO_LPT_PE   64
BUSY 35 SIO_LPT_BUSY   64
ACK* 36 SIO_LPT_ACK*   64
ERROR* 45 SIO_LPT_ERR*   64
ALF* 50 SIO_LPT_ALF*   64
STROBE* 51 SIO_LPT_STROBE* 64

CLOCK
14 IN CK_14M_SIO 65 CLOCK14
27 IN SU5CLK 91   CLOCK32

FAN
GPIO6/TACH1 111 FAN1_TACH
GPIO7/TACH2 112 FAN2_TACH

R1J4 FRONT_FAN_TACH IN 72
R1J5 REAR_FAN_TACH   IN 72

VSS<7> 110
VSS<6> 96
VSS<5> 78
VSS<4> 58
VSS<3> 46
VSS<2> 29
VSS<1> 8

1 OF 2
NC=117..129
IC

DESIGN NOTE:
EMPTY IF HECETA6 IS STUFFED
STUFF IF HECETA4 IS STUFFED

VCC3
RP1J3 10K 5% .063W IC SM
RP1J3 10K 5% .063W IC SM

OUT 98 27
OUT 27 98

27 OUT L_DRQ*
30 BI P_PCIRST*
52 IN ICH_SUS_STAT
98 56 27 BI SER_IRQ

R1H2 10K 5% CH 603
R1H1 10K 5% EMPTY 603

DESIGN NOTE:
STUFF FOR SIGNAL QUALITY
"NPO" C1H17 10PF 50V EMPTY 603

BOM=CORE

84 IN V_3P3_STBY
VCC3

C1J6 .1UF 20% 25V 603
C1H22 .1UF 20% 25V 603
C1J1 .1UF 20% 25V 603
C1H16 .1UF 20% 25V 603
C1H18 .1UF 20% 25V 603
C1J2 .1UF 20% 25V 603
C1H21 .1UF 20% 25V 603
C1H14 100UF 20% 25V EMPTY RDL

PLACE NEAR DEVICE PINS 6,31,49,60,76,93,107

PORT ANGELES (PART 1) / SIO

CR-62

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

VCC

CAD NOTE:
PLACE NEAR
FDD CONN

8 RP1J1
1K
5%
.063W
IC
SM

6 RP1J1
1K
5%
.063W
IC
SM

1 R1J1
1K
5%
CH
603

7 RP1J1
1K
5%
.063W
IC
SM

5 RP1J1
1K
5%
.063W
IC
SM

J5J3
2X17HDR_3_5

61 IN	SIO_FDD_DRVDEN0		1	P1
			2	P2
				KEY
	TP_301S	4	P4
61 IN	SIO_FDD_DRVDEN1			KEY
			6	P6
61 OUT	SIO_FDD_INDEX*		7	P7
			8	P8
61 IN	SIO_FDD_MTR0*		9	P9
			10	P10
			11	P11
	TP_302S	12	P12
61 IN	SIO_FDD_DS0*		13	P13
			14	P14
			15	P15
	TP_303S	16	P16
	TP_304S	17	P17
61 IN	SIO_FDD_DIR*		18	P18
			19	P19
61 IN	SIO_FDD_STEP*		20	P20
61 IN	SIO_FDD_WDATA*		21	P21
			22	P22
61 IN	SIO_FDD_WGATE*		23	P23
			24	P24
61 OUT	SIO_FDD_TRK0*		25	P25
			26	P26
	TP_305S	27	P27
61 OUT	SIO_FDD_WRTPRT*		28	P28
			29	P29
61 OUT	SIO_FDD_RDATA*		30	P30
			31	P31
61 IN	SIO_FDD_HDSEL*		32	P32
			33	P33
61 OUT	SIO_FDD_DSKCHG*		34	P34

HDR

FLOPPY CONNECTOR

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

PS2 KEYBOARD

VREG_PS2

SIO_KBDATA
SIO_KBCLOCK
SIO_MSDATA
SIO_MSCLOCK

SIO_KBDATA_FB
SIO_KBCLOCK_FB
SIO_MSDATA_FB
SIO_MSCLOCK_FB

J1A1
PS2 STACK
749231-001

MOUSE

CAD NOTE:
PLACE NEAR
PS/2 CONN

CRP1A1
TVS6_2V
6.2V
EMPTY

DESIGN NOTE:
STUFF FOR EMI ISSUES; NORMALLY EMPTY

CAD NOTE:
PLACE AS CLOSE TO PS/2 CONNECTOR AS POSSIBLE

ATX DOUBLE-STACKED

PS2 KEYBOARD / MOUSE

8 7 6 5 4 3 2 1

SIO_LPT_PD<7,,0>
61 IN

RP3A2
33 5% .063W
SM IC
SIO_LPT_PD6_R

RP3A2
33 5% .063W
SM IC
SIO_LPT_PD7_R

RP3A1
33 5% .063W
SM IC
SIO_LPT_PD0_R

RP3A1
33 5% .063W
SM IC
SIO_LPT_PD1_R

RP3A1
33 5% .063W
SM IC
SIO_LPT_PD2_R

RP3A1
33 5% .063W
SM IC
SIO_LPT_PD3_R

RP3A2
33 5% .063W
SM IC
SIO_LPT_PD4_R

RP3A2
33 5% .063W
SM IC
SIO_LPT_PD5_R

VCC

RP4A1 2,7K 5% .063W IC SM
RP4A1 2,7K 5% .063W IC SM
RP4A1 2,7K 5% .063W IC SM
RP4A1 2,7K 5% .063W IC SM

J3A1
TALL DSUB 25
749179-001

61 IN SIO_LPT_STROBE*
RP4A2
33 5% .063W
SM IC
SIO_LPT_STROBE_R*

61 IN SIO_LPT_ALF*
RP4A2
33 5% .063W
SM IC
SIO_LPT_ALF_R*

61 IN SIO_LPT_INIT*
RP4A2
33 5% .063W
SM IC
SIO_LPT_INIT_R*

61 IN SIO_LPT_SLCTIN*
RP4A2
33 5% .063W
SM IC
SIO_LPT_SLCTIN_R*

VCC

RP3A3 10K 5% .063W IC SM
RP3A3 10K 5% .063W IC SM
RP3A3 10K 5% .063W IC SM
RP3A3 10K 5% .063W IC SM
R3A1 10K 5% CH 603

61 OUT SIO_LPT_ACK*
61 OUT SIO_LPT_BUSY
61 OUT SIO_LPT_PE
61 OUT SIO_LPT_SLCT
61 OUT SIO_LPT_ERR*

1
14
2
15
3
16
4
17
5
18
6
19
7
20
8
21
9
22
10
23
11
24
12
25
13

DSUB
GND=26,27,28

CAD NOTE:
PLACE NEAR
LPT CONN

C3A12 220PF 50V X7R 603
C3A8 220PF 50V X7R 603
C3A2 220PF 50V X7R 603
C4A2 220PF 50V X7R 603

C3A13 220PF 10% 50V X7R 603
C3A9 220PF 10% 50V X7R 603
C3A6 220PF 50V X7R 603
C4A4 220PF 50V X7R 603

C3A14 220PF 10% 50V X7R 603
C3A10 220PF 10% 50V X7R 603
C3A3 220PF 10% 50V X7R 603
C3A1 220PF 10% 50V X7R 603

C2A5 220PF 10% 50V X7R 603
C3A11 220PF 10% 50V X7R 603
C3A7 220PF 10% 50V X7R 603
C3A5 220PF 10% 50V X7R 603
C4A3 220PF 10% 50V X7R 603

PARALLEL PORT

DRAWING
NGRVP.SCH_1.64
Wed Oct 23 10:39:01 2002

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SERIAL PORT A

U1G1
GD75232S   621111-103

61	SIO_COM_DCD1*	19	RY1	RA1	2
61	SIO_COM_DSR1*	18	RY2	RA2	3
61	SIO_COM_RXD1	17	RY3	RA3	4
61	SIO_COM_CTS1*	14	RY4	RA4	7
65	SIO_COM_RI1_ADDIN*	12	RY5	RA5	9
61	SIO_COM_RTS1*	16	DA1	DY1	5
61	SIO_COM_TXD1	15	DA2	DY2	6
61	SIO_COM_DTR1*	13	DA3	DY3	8
		1	VDD+	VDD-	10

NOTE DIRECTION
IC

+12V

VCC=20
GND=11
VCC=V_5P0_STBY

−12V

J2A1   749218-001
2 ROW   10

SIO_COM_DCD1_232	1
SIO_COM_DSR1_232	6
SIO_COM_RXD1_232*	2
SIO_COM_RTS1_232	7
SIO_COM_TXD1_232*	3
SIO_COM_CTS1_232	8
SIO_COM_DTR1_232	4
SIO_COM_RI1_232	9
	5

DSUB

11

C2A8 470PF 10% 50V X7R 603
C2A4 470PF 10% 50V X7R 603
C2A10 470PF 10% 50V X7R 603
C2A9 470PF 10% 50V X7R 603
C2A2 470PF 10% 50V X7R 603
C2A7 470PF 10% 50V X7R 603
C2A3 470PF 10% 50V X7R 603
C2A5 470PF 10% 50V X7R 603

DESIGN NOTE:
SUPPORT FOR RING-IN FROM PCI ADD-IN CARD: WOR OR WOM
J6G1
1X2HDR 107555-102

65 IN SIO_COM_RI1_ADDIN*   1 R6G162
1K 603 5% CH
1 OO 2
HDR

SIO_COM_RI1* OUT 61

80 IN V_5P0_STBY

+12V   −12V

1 202341-002   1 202341-002   1 202341-002
C1G7   C1G5   C1H10
1UF   1UF   1UF
20%   20%   20%
25V   25V   25V
Y5V   Y5V   Y5V
603   603   603
2   2   2

CAD NOTE:
PLACE NEAR 232'S PINS 1, 10, AND 20 RESPECTIVELY
BOM=CORE_COM1

COM1 PORT

RECOVER/CONFIGURE HEADER	MODE
JUMPER ON 1-2 *	NORMAL
JUMPER ON 2-3	CONFIGURE
JUMPER REMOVED	RECOVERY
* DEFAULT JUMPER SETTING	

CONFIGURE= SAFE MODE

J7H1
1X3HDR
RECOVERY_CONFIGURE_PULLUP
29 IN AUD_LINK_SDO_R
HDR

99 98 61 56 27 B1 L_AD<3..0>

U7J1
FWH

67 IN PWRGD_3V
RP7J1
8 1
4.7K 5%
SM .063W IC
7 WP

RP7J1
7 2
4.7K 5% .063W
SM IC
8 TBL

TP_FWH_29 29 IC

30 IN P_PCIRST*
R7J1
1 2 FWHL_RST
47 5%
603 CH
2 RST

14 IN CK_P_33M_FWHCLK 31 CLK

27 IN L_FRAME* 23 FWH4

FWH3 17 3
FWH2 15 2
FWH1 14 1
FWH0 13 0

DQ4/RFU 18 TP_FWH_13
DQ5/RFU 19 TP_FWH_19
DQ6/RFU 20 TP_FWH_20
DQ7/RFU 21 TP_FWH_21
RY/BY/RFU 22 TP_FWH_22

FGPI4 30 PN_FWH_GPI4
FGPI3 3 PN_FWH_GPI3
FGPI2 4 PN_FWH_GPI2
FGPI1 5 GPIO_DMA66_DETECT_SEC
FGPI0 6 GPIO_DMA66_DETECT_PRI

INIT 24

+12V
R7J4
1 1K 5%
CH 603
2

VCC3
Q7J1
FET

1 FWH_VPP VPP

C7J4
1 10PF
5%
50V
NPO
603

VCC3
J8J3
JUMPER
EMPTY
ALWAYS EMPTY
MFG MODE PADS

VCC3
RP7J1
3 4.7K
.063W
IC SM
6

4 RP7J1
4.7K 5%
.063W
IC SM
5

R7H11
1K 5%
CH 603
VCC3

R7H14
1K 5%
CH 603

R7J2
10K 5%
EMPTY
603

VCC3

FWH_H_INIT* IN 66

R7J3
10K 5%
CH 603

32 IN
32 IN

27 VCCA/NC
32 VCC
25 VCC

28 GNDA/NC
16 GND
26 GND

ID3 9 TP_FWH_9
ID2 10 TP_FWH_10
ID1 11 TP_FWH_11
ID0 12 TP_FWH_12

723644-009 IC

C7J2
1 .1UF
20%
25V
Y5V
603
2

VCC3

FIRMWARE HUB DECOUPLING

VCC3
C7H10 C7H11 C7J1
1 .1UF 1 .1UF 1 .1UF
20% 20% 20%
25V 25V 25V
EMPTY Y5V Y5V
603 603 603
2 2 2

VOLTAGE MODIFIER: ICH(VCCP) ISOLATE FROM FWH(VCC3)

DESIGN NOTE:
STUFF FOR PRODUCT
WITH VCCP > 1.5-V

+12V
R6H17
4.7K
5%
CH
603

R7H15
1 2
0 1A
603 EMPTY
Q6H5
MBT3904DUAL

FWH_H_INIT* OUT 66
M_FLUSH_FEEDBACK_Rﬂ

27 IN H_INIT*
R7H16
2 1
4.7K 5% M_INIT_Rﬂ
603 CH
XSTR

FWH

PORT_ANGELES 2 OF 2 INPUTS

PIN	FUNCTION	TYPE
1	TEST_EN	3IPD
2	AUD_LINK_RST*	5I
3	CDC_DWN_ENAB/GPIO12*	5I/O12
70	PRIMARY_HD*	3ISPU_400
71	SECONDARY_HD*	3ISPU_400
72	SCSI*	3ISPU_400
75	FPRST*	3ISPU_400
80	PWRGD_PS	3ISPU_400
81	CPU_PRESENT*	3ISPU_400
83	SLP_S3*	3IS_400
84	SLP_S5*	3IS_400
87	SMB_CLK_M	3IOD6
88	SMB_CLK_R	3IOD6
89	SMB_DAT_M	3IOD6
90	SMB_DAT_R	3IOD6
124	5V_DDCSDA/GPIO8	5IOD6/3IOB
125	5V_DDCSCL/GPIO9	5IOD6/3IOB
126	3V_DDCSDA/GPIO10	3IOD6/3IOB
127	3V_DDCSCL/GPIO11	3IOD6/3IOB
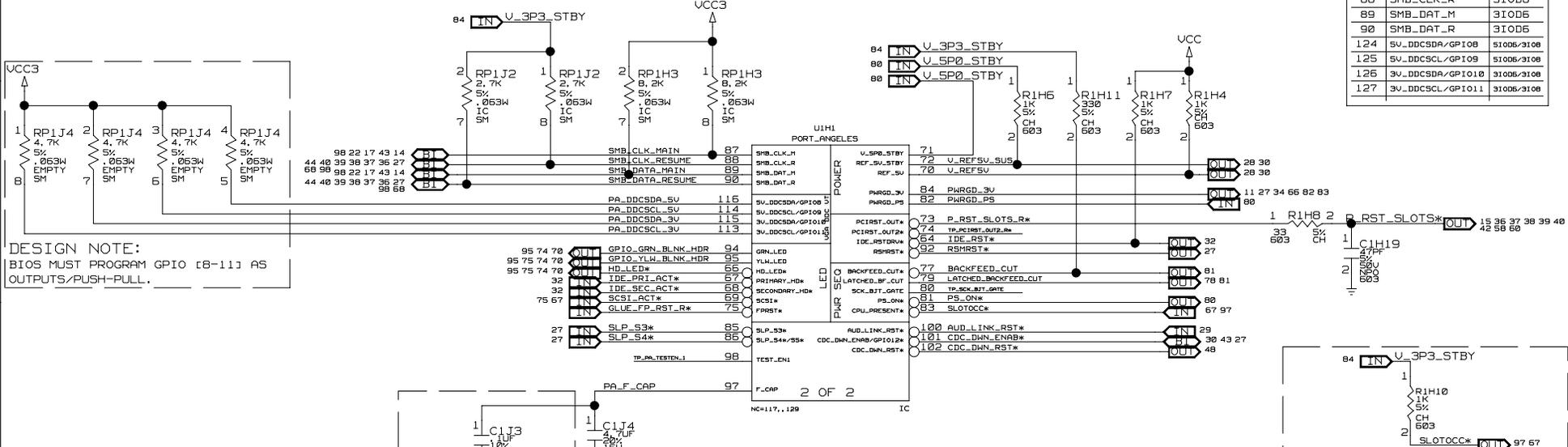
DESIGN NOTE:
BIOS MUST PROGRAM GPIO [8-11] AS OUTPUTS/PUSH-PULL.

CAD NOTE:
PLACE AS CLOSE TO PIN AS POSSIBLE

SPARE

SCSI ACTIVITY LED
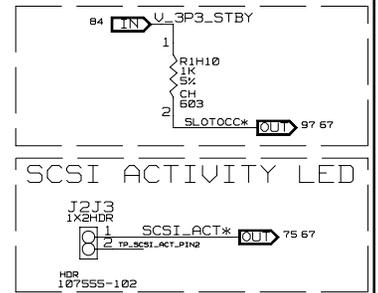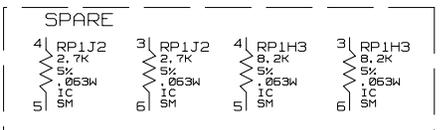
PORT ANGELES (PART 2) / GLUE4

U1H1 PORT_ANGELES

DRAWING
NGRVP.SCH_1.67
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HARDWARE MANAGEMENT: HECETA

HECETA

CAD NOTE:
10MIL TRACE ON SE_ZONE_TDN AND _TDP

CAD NOTE:
DO NOT PLACE HECETA-6 UNDER CPU HEATSINK

CAD NOTE:
SOUTHEAST THERMAL ZONE SENSOR
PLACE BELOW DIMMS
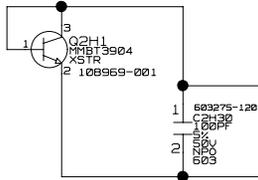
DESIGN NOTE:
ALL STUFFED IF HECETA6
ALL EMPTY IF HECETA4

DESIGN NOTE:
STUFF WITH HECETA6 FOR FAN_CNTL FET (P-UP)
STUFF WITH HECETA4 FOR ADDRESS SELECT

DESIGN NOTE:
ALL STUFFED IF HECETA4
ALL EMPTY IF HECETA6

CPU_FAN_PWM FROM PORT ANGELES PIN-103 THROUGH 0 OHM
NEEDS DESIGN MODIFICATION FOR HECETA4 SUPPORT
TO ALLOW PWM CONTROL THROUGH FET ON HEC4 PIN-16 WHILE NOT PULSING
THE FP_RST SIGNAL THROUGH THE 0 OHM RESISTOR (ALSO ON HEC4 PIN-16)

PRELIMINARY
U1E2
HECETA6
A57150-001

U1E1
HECETA4

CR-68

VCC

27 IN SPKR 1 R8H5 2 CORE_SPKR_R 1 3 Q8H1
1K   MMBT3904
603   5%   XSTR
       CH

1 C8H8   108969-001
   1000PF   2
   10%   SPKR_OUT
2 50V
   EMPTY
   603
   "X7R"

LS8H1
XDCR

1 + AT-08
2   IN

1 R8H7
   47
   5%
   EMPTY
2 603

SPEAKER

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8   7   6   5   4   3   2   1

VCC_HDLED_PWR OUT 75

80 IN V_5P0_STBY   1 R8J7 2
330   5%
603   CH

1 R7J5 2
330   5%
603   CH

R8J8
VCC 1 2
330   5%
603   CH

109717-726
J8J2
2X8HDR_10_14

67 IN HD_LED*
27 100 96 6 OUT FP_RST*

1   2
3   4
5   6
7   8
9   10
11   12
13   14
15   16

GPIO_GRN_BLNK_HDR IN 67
GPIO_YLW_BLNK_HDR IN 67

VCC

TP_SIO_IRRX2
TP_SIO_IRTX2

VCC

HDR

VCC

CP8J2
2 470PF
20%
50V
7 EMPTY
SM

CP8J2
1 470PF
20%
50V
8 EMPTY
SM

CP8J1
1 470PF
20%
50V
8 EMPTY
SM

TP_SIO_IRTX2_CAP2
CP8J1
2 470PF
20%
50V
7 EMPTY
SM
TP_SIO_IRTX2_CAP7

SPARE

CP8J1
4 470PF
20%
50V
5 EMPTY
SM

CP8J1
3 470PF
20%
50V
6 EMPTY
SM

CP8J2
4 470PF
20%
50V
5 EMPTY
SM

CP8J2
3 470PF
20%
50V
6 EMPTY
SM

SW_ON* OUT 74 75 96 27

GPIO_GRN_BLNK_HDR IN 67

J8J1
1X3HDR2
1

102276-304

3

EMPTY

1 C8J3
470PF
10%
2 50V
EMPTY
603

DECOUPLING
VCC3

2 C8J2
.1UF
20%
1 25V
EMPTY
603

GPIO_YLW_BLNK_HDR IN 67

1 C7J3
470PF
10%
2 50V
EMPTY
603

FRONT PANEL HDR

8   7   6   5   4   3   2   1

D

MH9A1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH1J1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH7A1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH5J1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

C

MH5A1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH9J1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH1B1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH9G1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH1G1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

MH5G1
MTG_HOLE
NC9 ⌐9
EMPTY
GND=1, 2, 3, 4, 5, 6, 7, 8

B

A

MOUNTING HOLES

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CR-72

8 7 6 5 4 3 2 1

CPU ALWAYS-ON FAN

CAD NOTE:
(PLACE BELOW/RIGHT CPU SOCKET)

+12V

CPU_DRIVER

J1B1
1X3HDR
1
2
3
HDR
CPU_TACH_OUT

+12V

R1B5
10K
5%
CH
603

R1B7
0
1A
CH
603
200V

Q1C1
EMPTY

68 61 IN CPU_FAN_PWM

A50095-001

DESIGN NOTE:
STUFF PULL-UP (LOCATED ON HECETA PAGE)
WHEN FET IS STUFFED (0 OHM MUST BE UN-STUFFED)

1 R1B6 2 CPU_FAN_TACH OUT 68
15K 5%
603 CH

R1B3
5.6K
5%
CH
603

VCC3

R1G6
1K
5%
CH
603

VCC3

Q1G1
MMBT3904
XSTR

REAR CHASSIS FAN

CAD NOTE:
(PLACE ABOVE/RIGHT CPU SOCKET)

68 61 IN FNT_REAR_FAN_PWM3

R1G2

FNT_REAR_FAN_PWM3_PN1

5% 220
CH 603

108969-001

FNT_REAR_FAN_PWM3_XSTR

R5B4
5% 10
CH 603

REAR_FAN_PWM_R

Q5B1
MMBT2222
XSTR

REAR_DRIVER

+12V

J6B1
1X3HDR
1
2
3
HDR
REAR_TACH_OUT

+12V

R5B3
10K
5%
CH
603

1 R5A7 2 REAR_FAN_TACH OUT 61 68
15K 5%
603 CH

R5A8
5.6K
5%
CH
603

FRONT CHASSIS FAN

CAD NOTE:
(PLACE LOWER LEFT CORNER OF PLATFORM)

2 R9H2 1
10 5% 1/16W
603 CH

FRONT_FAN_PWM_R

Q9H1
MMBT2222
XSTR

101416-501

FRONT_DRIVER

+12V

J9H1
1X3HDR
1
2
3
HDR
FRONT_TACH_OUT

+12V

R9H6
10K
5%
CH
603
1/16W

1 R9H5 2 FRONT_FAN_TACH OUT 61 68
15K 5%
603 CH
1/16W

R9H3
5.6K
5%
CH
603
1/16W

FAN CONTROL

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

D

C

B

CNR
SPD ADDR AC

PCI SLOTS
SPD ADDR N/A

LPC HDR
SPD ADDR A8

SMB_CLK/DATA_RESUME

LAN
SPD ADDR N/A

HECETA
SPD ADDR N/A

ICH

DIMMS

SPD ADDR A0, A2, A4, A6

PORT_ANGELES

A

SMBUS HDR
SPD ADDR N/A

CLOCK
SPD ADDR D2

SMB_CLK/DATA_MAIN

SMBUS ISOLATION MAP

| 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

D   27 [IN] GPIO_LAN_DISABLE* 2 R8J2 1 EMAIL_LED [OUT] 74
0
603
1A
EMPTY

CUSTOM FP HEADER OPTION

753287-001
U8H1   U8H1
74ACT04   74ACT04

J7J1 109717-725
2X10HDR_10

74 [IN] EMAIL_LED 5 >6 EMAIL_BUF2 3 >4 EMAIL_BUF_P4 1 R8J1 2
220
603
5%
EMPTY

PN2_HD_INVERT   2   1
67 [IN] GPIO_YLW_BLNK_HDR   4   3
HD_LED_2BY10   6   5
8   7   TP_PN_2BY10_P8
VCC=14   VCC=14
GND=7   GND=7
67 [IN] GPIO_GRN_BLNK_HDR   12   11   TP_PN_2BY10_P10
14   13   TP_PN_2BY10_P12
80 [IN] V_5P0_STBY   16   15   TP_PN_2BY10_P14
27 96 75 70 [OUT] SW_ON*   18   17
R8H8   TP_PN_2_10_PIN17   20   19
10K   TP_PN_2_10_PIN19
5%
EMPTY
603   U8H1   EMPTY
74ACT04

67 [IN] HD_LED*   1 >2 HD_LED_P2 1 R8H9 2
220
603
5%
EMPTY
VCC=14
GND=7

VCC=V_5P0_STBY(~EMAILINVRT)

B   80 [IN] V_5P0_STBY   CUSTOM USB HEADER OPTION

35 29 [B1] USB_FRONT1*
35 29 [B1] USB_FRONT1

1 C8H9   CAD NOTE: 34 [IN] USB_FNT_PWR   109717-010
.1UF   PLACE NEAR INVERTER
10%
16V   J7F1
2 EMPTY   2X5HDR_10
603
1   2
3   4
5   6
7   8
VCC=V_5P0_STBY(~EMAILINVRT)   9
USB_FRONT2_R* [B1] 35
EMPTY   USB_FRONT2_R [B1] 35

U8H1   U8H1   U8H1
74ACT04   74ACT04   74ACT04   CAD NOTE:
PLACE HEADER AS CLOSE AS POSSIBLE
9 >8 TP_INVC_P8 13 >12 TP_INVC_P12 11 >10 TP_INVC_P10   TO STANDARD USB FP HEADER
EMPTY   EMPTY   EMPTY
VCC=14   VCC=14   VCC=14
GND=7   GND=7   GND=7

SPARES

SPECIAL HEADERS #1

DRAWING
NGRVP.SCH_1.74
Wed Oct 23 10:39:05 2002

DOCUMENT NUMBER	PAGE	REV
A95397	74	1.5
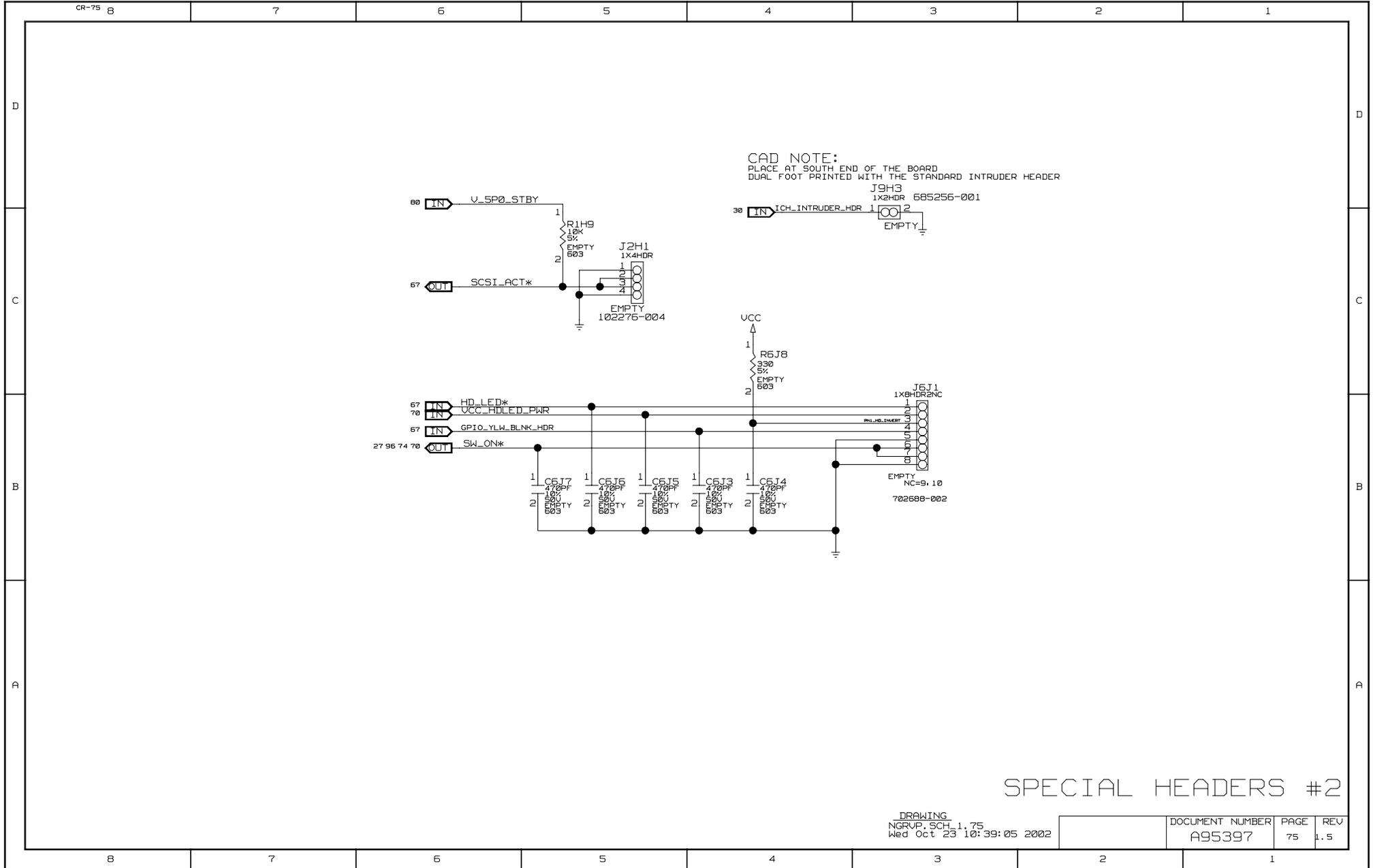
CAD NOTE:
PLACE AT SOUTH END OF THE BOARD
DUAL FOOT PRINTED WITH THE STANDARD INTRUDER HEADER

J9H3
1X2HDR 685256-001

30 IN ICH_INTRUDER_HDR 1 2
EMPTY

80 IN V_5P0_STBY

R1H9
10K
5%
EMPTY
603

J2H1
1X4HDR
1
2
3
4

67 OUT SCSI_ACT*

EMPTY
102276-004

VCC

R6J8
330
5%
EMPTY
603

J6J1
1X8HDR2NC
1
2
3
4
5
6
7
8

67 IN HD_LED*
70 IN VCC_HDLED_PWR
67 IN GPIO_YLW_BLNK_HDR
27 96 74 70 OUT SW_ON*

PNL_HD_INVERT

EMPTY
NC=9,10

702688-002

C6J7   C6J6   C6J5   C6J3   C6J4
1   1   1   1   1
470PF   470PF   470PF   470PF   470PF
10%   10%   10%   10%   10%
50V   50V   50V   50V   50V
2 EMPTY   2 EMPTY   2 EMPTY   2 EMPTY   2 EMPTY
603   603   603   603   603

SPECIAL HEADERS #2

DRAWING
NGRVP.SCH_1.75
Wed Oct 23 10:39:05 2002

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A95397	75	1.5

D

C

B

J2J2
1X6PWR
1
2
3
4
5
6
CONN
NC=7

VCC3 VCC
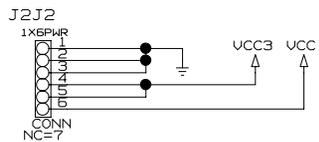
455072-060

CAD NOTE:
KEEP CLOSE TO 2X10 PWR-CONN

DESIGN NOTE:
OPTIONAL FOR EXTRA VOLTAGE LOAD (AGPPRO, ETC.)

A

SPECIAL HEADERS #3

E7205 MCH
X.X (VCCP)
1.3
1.5
2.5

ICH
X.X (VCCP)
1.5
1.5 STBY
3.3 STBY (VCC3 STBY)
3.3 (VCC3)

SIO (PORT ANGELES)
3.3 (VCC3)
3.3 STBY (VCC3 STBY)
5.0 STBY (VCC STBY)

SATA
1.8
3.3 (VCC3)

HSCOM (1394)
3.3 (VCC3)

FWH
3.3 (VCC3)

LAN
3.3 V-AUX (VCC3 OR 3.3 STBY)
3.3 (VCC3)

GLUECHIP
3.3 STBY (VCC3 STBY)
5.0 STBY (VCC STBY)

CK-408
3.3 (VCC3)

CPU
X.X (VCCP)

HEC6
3.3 STBY (VCC3 STBY)
5.0 (VCC)
12
X.X (VCCP)
2.5 (CORE)

HEC4
3.3 STBY (VCC3 STBY)
5.0 (VCC)
3.3 (VCC3)
X.X (VCCP)
2.5 (CORE)

+12V (PLUS 12V FROM POWER-SUPPLY)
-12V (MINUS 12V FROM POWER-SUPPLY)
VCC3 (3.3V FROM POWER-SUPPLY)
VCC (5.0V FROM POWER-SUPPLY)
VCCP (1.10 - 1.85V)
V_1P5_CORE (1.5V DERIVED FROM VCC3)
V_1P3_CORE (1.3V DERIVED FROM VCC3)
V_1P25_MEMVTT (1.25V DERIVED FROM V_2.5)
V_2P5_SM (2.5V DERIVED FROM VCC)
V_3P3_PCI_VAUX (3.3V OR 3.3-STANDBY SOURCE)
V_1P5_STBY (1.5V DERIVED FROM 5.0-STANDBY)
V_3P3_STBY (3.3V DERIVED FROM 5.0-STANDBY)
V_5P0_STBY (5.0V FROM POWER-SUPPLY)
V_3P0_BAT_VREG (~3.0V FROM THE BATTERY OR FROM 3.3STBY THROUGH A DIODE)
V_BAT_VREG_R_CR (3.0V FROM THE BATTERY)
VREG_12V_FILTERED (+12V FILTERED FROM 2X2 12V POWER-SUPPLY)
VREG_USB_BP_LEFT (5.0 FROM VCCC OR 5.0-STANDBY)
VREG_USB_BP_RIGHT (5.0 FROM VCCC OR 5.0-STANDBY)
VREG_PS2 (5.0 FROM VCCC OR 5.0-STANDBY)
USB_FNT_PWR (5.0 FROM VCC OR 5.0-STANDBY)
USB_CNR_PWR (5.0 FROM VCC OR 5.0-STANDBY)

VREG: VOLTAGE DISTRIBUTION

VREG MAP

CR-77

2.5V VREG

1.25V DDR

+12V

81 IN VREG_USB_NCH

R6H9
0
603
1A
CH

Q5H1
MMBT3904
XSTR

C6H5
47UF
20%
X5R
603

98 78 IN V_2P5_SM

R6G20
100
1%
CH
603

IN VMARG_1P25_MEMVTT

R6H1
100
1%
CH
603

DESIGN NOTE:
THIS MAY BE REPLACED WITH
FERRITE BEAD OR INDUCTOR

R6H4
0
1A
CH
805

1P25_MEMVTT_FILTER

C6H2
10UF
10%
10V
X5V
603

U6H1
LM358
IC

DIMM_VREF_1P25_A

12V_SWITCHED_PN1

U6H1
LM358
IC

INV_A_OUT

INV_A_PIN4

C6H4
1UF
20%
25V
Y5V
603

98 78 IN V_2P5_SM

Q5H2
FET
A71095-001

2 R6G231
603
1A
CH

-12V

C6G14
10UF
10%
10V
X5V
603

BAT54C
SOT23C
DIO

CR6H1

1 R6H5 2
1K
603
5%
CH

V_1P25_MEMVTT

C5H10
3300UF
20%
6.3V
RLUM
RDL

C5H5
47UF
10%
10V
X5R
1206

C5H6
1UF
10%
16V
X7R
603

OUT 98 18 19 20 23 24 25

Q5H1
MOSFET
A61801-001

1.25V VREG

DRAWING
NGRVP.SCH_1.79
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POWER SUPPLY CONNECTOR / 12V

BATTERY

VREG GATE CONTROL FOR PS/2, USB
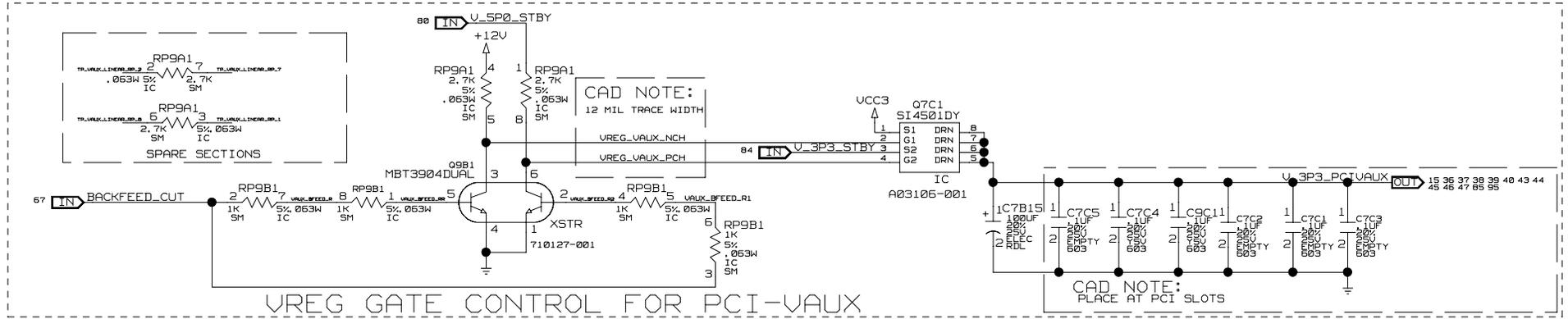
VREG GATE CONTROL FOR PCI-VAUX

BATTERY & PCIVAUX

CAD NOTE:
DO NOT PLACE BATTERY NEAR
MOUNTING HOLES, GROUND OR VIAS

CAD NOTE:
PLACE CAP NEAR ICH

CAD NOTE:
12 MIL TRACE WIDTH

CAD NOTE:
12 MIL TRACE WIDTH

CAD NOTE:
PLACE AT PCI SLOTS

SPARE SECTIONS

SPARE SECTIONS

DRAWING
NGRVP.SCH_1.81
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A95397	81	1.5

D

V_3P3_STBY [IN] 84 — R6G1 — USB_OC_BACK_RIGHT* [OUT] 29
10K 5%
603 CH

CAD NOTE:
VREG_USB MUST BE SPLIT
AMONGST ALL USB CHANNELS.
DO NOT DAISY CHAIN

PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR

PWRGD_3V [IN] 67 — R2A1 — PWRGD_3V_R — Q2A1
10K 5% MMBT3904
603 CH XSTR

VCC
Q2A2
SI4501DY

VREG_USB_NCH [IN] 81 — 2 — S1 DRN 8
V_5P0_STBY [IN] 80 — 3 — G1 DRN 7
VREG_USB_PCH [IN] 81 — 4 — S2 DRN 6
1 — G2 DRN 5

VREG_USB_Q — RT2A1 — VREG_USB_BP_RIGHT [OUT] 35 57
657448-004 C2A1 C1A5
THRMSTR 220UF 470PF
1.50 50V 10%
ELEC 50V
RDL X7R
"201307-001" 603

IC
A03106-001

CAD NOTE:
.1 INCH COPPER ON
DRAIN AND SOURCE

RP1A1
0

C

0805, 30.0HM
(100MHZ), 3A
656554-010
FB1A1
VREG_PS2_FB 1 — 2 — VREG_PS2 [OUT] 63
FB
C1A2
470PF
10%
50V
X7R
603

B

A

VREG BACKPANELRIGHT USB / PS2

DOCUMENT NUMBER | PAGE | REV
A95397 | 82 | 1.5

D

R6G3

84 IN V_3P3_STBY 2 ———1 USB_OC_BACK_LEFT* OUT 29
          10K   5%
          603   CH

CAD NOTE:
VREG_USB MUST BE SPLIT
AMONSGT ALL USB CHANNELS.
DO NOT DAISY CHAIN

PLACE AS CLOSE AS POSSIBLE
TO USB CONNECTOR

VCC   Q4A2
       SI4501DY

67 IN PWRGD_3V 2 ———1 R4A1 PWRGD_3V_R_LEFT 1 3 Q4A1
          10K   5%   MMBT3904
          603   CH   XSTR
                                                 2

81 IN VREG_USB_NCH 1 S1 DRN 8
80 IN V_5P0_STBY   2 G1 DRN 7
81 IN VREG_USB_PCH 3 S2 DRN 6
                     4 G2 DRN 5 VREG_USB_Q_LEFT 1 RT4A1 2

                     IC
                     A03106-001   657448-004 THRMSTR
                                                       1.50

                                                       VREG_USB_BP_LEFT OUT 33 47

                                          + 1 C4A4   1 C4A1
                                               220UF   470PF
                                               20V   10%
                                               25V   50V
                                               ELEC   X7R
                                          2 RDL   2 603
                                          "201307-001"

CAD NOTE:
.1 INCH COPPER ON
DRAIN AND SOURCE

VREG BACKPANEL USB

DOCUMENT NUMBER	PAGE	REV
A95397	83	1.5

8	7	6	5	4	3	2	1

U8F2
EZ1086

80 IN V_5P0_STBY

3 IN OUT 2 V_3P3_STBY OUT 27 28 30 34 46 56 61 67 68 81
                                    82 83 84 85 88 95

OUT 4

ADJ IC

1 C8F12
1.0UF
10%
10V
Y5V
603
2

U8G1
LM317L

84 IN V_3P3_STBY

1 IN OUT 2 V_1P5_STBY OUT 28 30
      OUT 3
      OUT 6
ADJ OUT 7
4   IC NC=5,8

1 C8F15
1.0UF
10%
10V
Y5V
603
2

ADJ_1P5_STBY 1 R8G1 2
              100 1%
              603 CH

1 R8G3
  20
  1%
  CH
  603
2

3.3V STBY / 1.5V STBY

DOCUMENT NUMBER	PAGE	REV
A95397	84	1.5

8	7	6	5	4	3	2	1

VREG DECOUPLING

1.3V CORE

+12V

VCC3

VCC3

1 R6D3
150
1%
CH
603
2

1P3_CORE_358_PLUS_3

1 R6E1
150
1%
CH
603
2

1 C6E1
1.0UF
10%
Y5V
603
2

1P3_CORE_358_MINUS_2

VMARG_1P3_CORE

1 R6E2
196
1%
CH
603
2

1 C6E9
1.0UF
10%
Y5V
603
2

1 C5E7
1.0UF
10%
10V
603
2

3
2
1

8 U5E1
LM358
1 V
G
4 IC
101299-002

1P3_CORE_358_OUT_1

5
6
7

8 U5E1
LM358
1 V
G
4 IC
101299-002

1P3_CORE_358_OUT_7

1 R5D5
1K
5%
CH
603
2

1 R5D6
1K
5%
CH
603
2

3 Q5D1
D FET
G
S
A71095-001

3 Q5D2
D FET
G
S
A71095-001

V_1P3_CORE

1 C5D5
4.7UF
20%
16V
Y5V
1206
2

1 C5E5
4.7UF
20%
16V
Y5V
1206
2

1 C5E3
470UF
20%
16V
ALUM
2 RDL
"202008-026"

1 C5E8
4.7UF
20%
16V
Y5V
1206
2

202170-004

202170-004

202170-004

OUT   98 11 13 94

DESIGN NOTE:
MAY BE MANUALLY MODIFIED
IN BOM TO ADJUST 1.3V
CORE SIGNAL DECOUPLING.

1.3V VREG

1.5V CORE

CAD NOTE:
CONNECT VSENSE (IRU1150, PIN1) TO V_1P5_CORE SIGNAL
CLOSE TO LOAD (ICH OR MCH) FOR REMOTE SENSING.
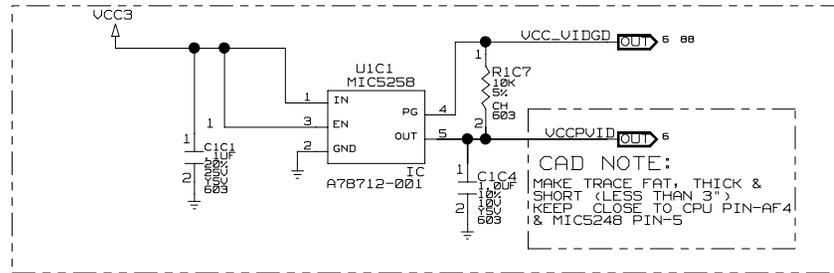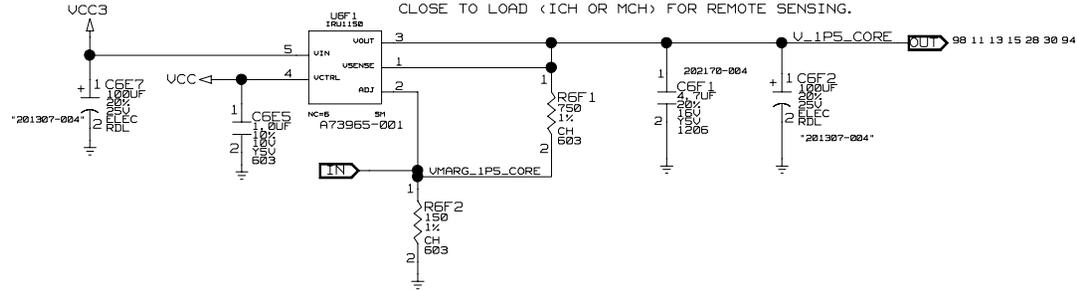
1.5V VREG

CAD NOTE:
MAKE TRACE FAT, THICK &
SHORT (LESS THAN 3")
KEEP CLOSE TO CPU PIN-AF4
& MIC5248 PIN-5

CPU VREG

CAD NOTE:
PHYSICALLY CONNECT THE AGND (TRACE, NOT A PLANE)
TO ONE OF THE OUTPUT CAPS. DISREGARD WARNINGS.

DRAWING
NGRVP.SCH_1.88
Wed Oct 23 10:39:10 2002

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PAGE 88
REV 1.5

CAD NOTE:
PLACE ABOVE (NORTH) OF CPU SOCKET

98 88 IN VCCP

(16 SITES)

CAD NOTE:
PLACE IN CENTER OF CPU SOCKET

98 88 IN VCCP

(12 SITES)

CAD NOTE:
PLACE BELOW (SOUTH) OF CPU SOCKET

98 88 IN VCCP

(12 SITES)

98 88 IN VCCP

(11 SITES)

"628955-020"

DUAL SITE   DUAL SITE   DUAL SITE   DUAL SITE
CAD NOTE: CAD NOTE: CAD NOTE: CAD NOTE:

1
L4B3
1.7UH
80 IN VREG_12V_POWER 1 ⌇⌇ 2   VREG_12V_FILTERED   OUT 88
IND

CAD NOTE:
PLACE NEAR 0.004 OHM,
1% 2512 SENSE RESISTOR

CPU VREG DECOUPLING

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A95397	89	1.5

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DRAWING
NGRVP.SCH_1.90
Wed Oct 23 10:39:11 2002

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A95397	90	1.5

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NGRVP.SCH_1.91
Wed Oct 23 10:39:11 2002

DOCUMENT NUMBER	PAGE	REV
A95397	91	1.5

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DRAWING
NGRVP.SCH_1.92
Wed Oct 23 10:39:11 2002

DOCUMENT NUMBER	PAGE	REV
A95397	92	1.5

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NGRVP.SCH_1.93
Wed Oct 23 10:39:11 2002

DOCUMENT NUMBER	PAGE	REV
A95397	93	1.5

MCH BACK DECOUPLING
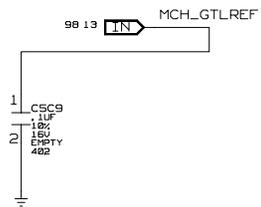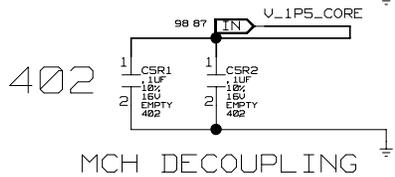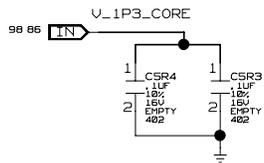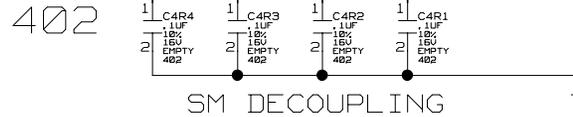
98 13 IN MCH_GTLREF

1 C5C9
.1UF
10%
16V
2 EMPTY
402

V_1P3_CORE
98 86 IN

1 C5R4   1 C5R3
.1UF   .1UF
10%   10%
16V   16V
2 EMPTY   2 EMPTY
402   402

V_1P5_CORE
98 87 IN

402

1 C5R1   1 C5R2
.1UF   .1UF
10%   10%
16V   16V
2 EMPTY   2 EMPTY
402   402

MCH DECOUPLING

98 78 IN V_2P5_SM

402

1 C4R4   1 C4R3   1 C4R2   1 C4R1
.1UF   .1UF   .1UF   .1UF
10%   10%   10%   10%
16V   16V   16V   16V
2 EMPTY   2 EMPTY   2 EMPTY   2 EMPTY
402   402   402   402

SM DECOUPLING

BACKSIDE DECOUPLING

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A95397	94	1.5

DEBUG/EV FEATURE: KEY SIGNAL STATUS LED'S
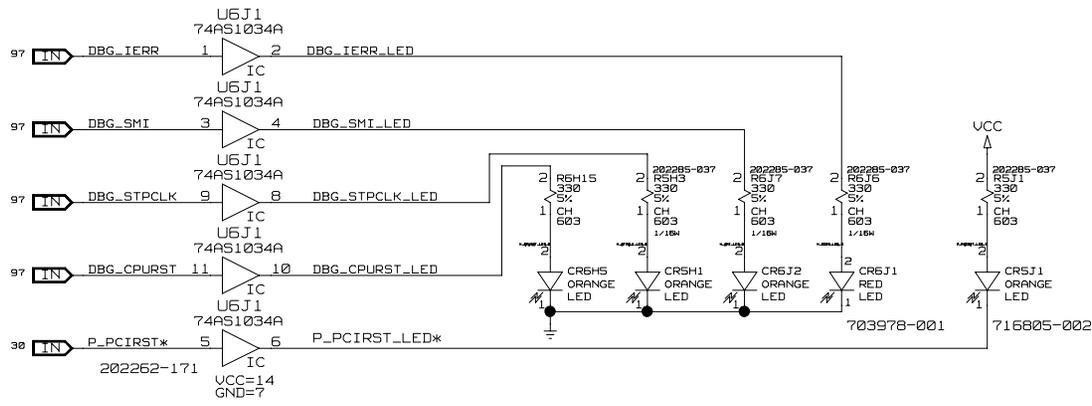
PRODUCT FEATURE: STATUS LED'S

STEADY YELLOW: SLEEPING
BLINK YELLOW: SLEEPING W/MESSAGE

695896-001
CR6J3
DUAL LED

U6J1
74AS1034A
97 IN DBG_IERR 1 > 2 DBG_IERR_LED
IC

67 IN GPIO_YLW_BLNK_HDR 1
67 IN GPIO_GRN_BLNK_HDR 3
GREEN/YELLOW

U6J1
74AS1034A
97 IN DBG_SMI 3 > 4 DBG_SMI_LED
IC

VCC

STEADY GREEN: RUNNING
BLINK GREEN: RUNNING W/MESSAGE

U6J1
74AS1034A
97 IN DBG_STPCLK 9 > 8 DBG_STPCLK_LED
IC

2 R6H15 330 5% 1 CH 603
2 202285-037 R5H3 330 5% 1 CH 603 1/16W
2 202285-037 R6J7 330 5% 1 CH 603 1/16W
2 202285-037 R6J6 330 5% 1 CH 603 1/16W
2 202285-037 R5J1 5% 1 CH 603

VCC
1 R8J9 220 5% 2 CH 603

U6J1
74AS1034A
97 IN DBG_CPURST 11 > 10 DBG_CPURST_LED
IC

CR6H5 ORANGE LED
CR5H1 ORANGE LED
CR6J2 ORANGE LED
CR6J1 RED LED
CR5J1 ORANGE LED

2 CR8J1 GREEN LED 1

U6J1
74AS1034A
30 IN P_PCIRST* 5 > 6 P_PCIRST_LED*
IC
202262-171
VCC=14
GND=7

703978-001
716805-002

67 IN HD_LED*

DEBUG/EV FEATURE: POWER RAIL STATUS LED'S
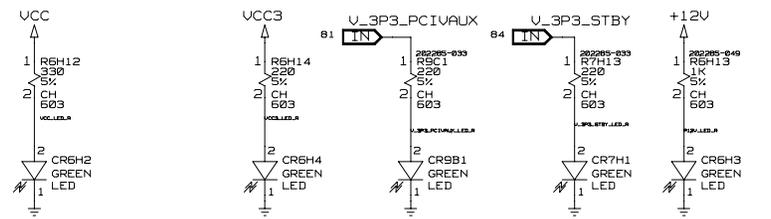
DEBUG/EV FEATURE: RED WARNING LED ON CPU 12V CONNECTOR

VCC
1 R6H12 330 5% 2 CH 603
VCC3
1 R6H14 220 5% 2 CH 603
V_3P3_PCIVAUX
81 IN
1 202285-033 R9C1 220 2 CH 603
V_3P3_STBY
84 IN
1 202285-033 R7H13 220 2 CH 603
+12V
1 202285-049 R6H13 1K 5% 2 CH 603

+12V
R4B13 1K 5% CH 603

CR6H2 GREEN LED
CR6H4 GREEN LED
CR9B1 GREEN LED
CR7H1 GREEN LED
CR6H3 GREEN LED

80 IN VREG_12V_POWER 1 R4B11 2 VREG_12V_POWER_R
2.7K 603 5% CH
Q5B2 MMBT3904 XSTR
108969-001

703978-001
CR5B1 RED LED

CAD NOTE: PLACE @ 2X2 CONNECTOR

U6J1
74AS1034A
30 IN P_PCIRST* 13 > 12 P_PCIRST_DEBUG* OUT 98 99
IC
VCC=14
GND=7
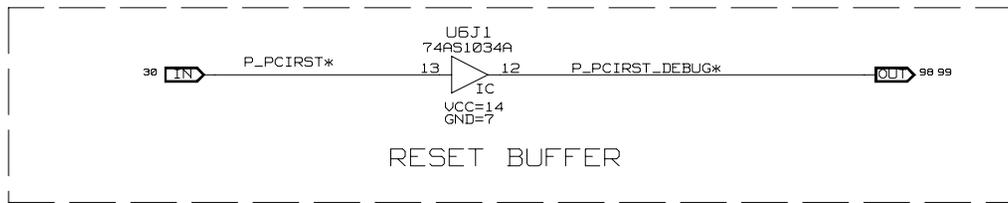
RESET BUFFER

DEBUG POWER LEDS

8   7   6   5   4   3   2   1

DEBUG/EV FEATURE: FRONT PANEL SWITCHES

FP_RST_DEBUG*   1 R9J1 2   FP_RST*   OUT 6   70 100 27
0 1A
603 CH

J9J2
SW
672681-002

SW_ON*   OUT 70 74 75 27

J9J1
SW
672681-002
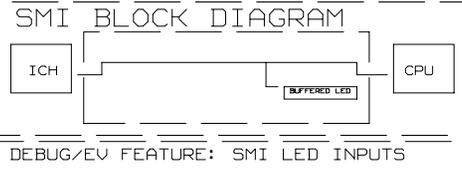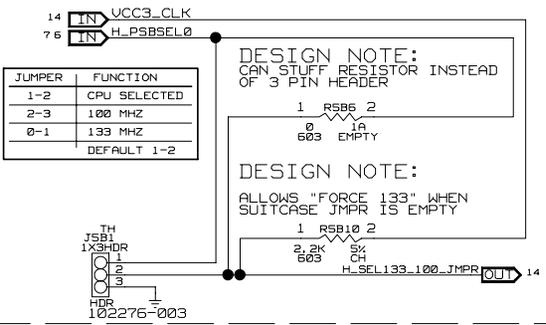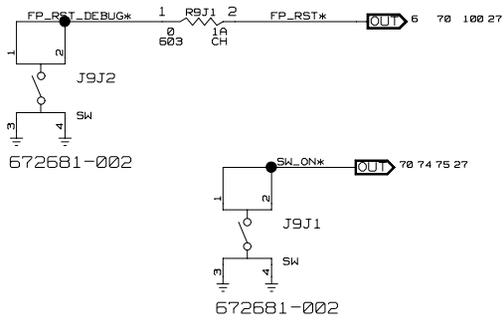
DEBUG/EV FEATURE: VID JUMPERS

DEFAULT
CPU DEFINED

VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	1	1	1	1	OFF
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

* UN-DRIVEN H_VID SIGNALS WILL BE PULLED HIGH BY INTERNAL VREG RESISTOR

H_VID_ISOLATE<0>   IN 6
TH J1F1 1X3HDR
1 R1F1
0
1A
2 EMPTY
603 H_VID<0>   OUT 40 68 88
1-2
HDR
102276-003

H_VID_ISOLATE<1>   IN 6
TH J1F2 1X3HDR
1 R1F2
0
1A
2 EMPTY
603 H_VID<1>   OUT 40 68 88
1-2
HDR
102276-003

H_VID_ISOLATE<2>   IN 6
TH J1F3 1X3HDR
1 R1F3
0
1A
2 EMPTY
603 H_VID<2>   OUT 40 68 88
1-2
HDR
102276-003

H_VID_ISOLATE<3>   IN 6
TH J1F4 1X3HDR
1 R1F4
0
1A
2 EMPTY
603 H_VID<3>   OUT 40 68 88
1-2
HDR
102276-003

H_VID_ISOLATE<4>   IN 6
TH J1F5 1X3HDR
1 R1F5
0
1A
2 EMPTY
603 H_VID<4>   OUT 40 68 88
1-2
HDR
102276-003

14   IN   VCC3_CLK
7 6   IN   H_PSBSEL0

DESIGN NOTE:
CAN STUFF RESISTOR INSTEAD OF 3 PIN HEADER

1 R5B6 2
0 1A
603 EMPTY

JUMPER	FUNCTION
1-2	CPU SELECTED
2-3	100 MHZ
0-1	133 MHZ
	DEFAULT 1-2

DESIGN NOTE:
ALLOWS "FORCE 133" WHEN SUITCASE JMPR IS EMPTY

1 R5B10 2
2.2K 5%
603 CH
H_SEL133_100_JMPR   OUT 14

TH J5B1 1X3HDR
1
2
3
HDR
102276-003

SMI BLOCK DIAGRAM

ICH   BUFFERED LED   CPU

DEBUG/EV FEATURE: SMI LED INPUTS

27   IN   ICH_H_SMI*
603 CH
0 1A
1 R5H1 2
H_SMI*   OUT 6

R6H21
0
1A
CH
603

H_SMI_DEBUG*   OUT 97

DEBUG/EV FEATURE: TDR COUPONS

TDR_TOP_50OHM

TDR PIN
DB1C2

TDR PIN
DB1B2

TDR_TOP_60OHM

TDR PIN
DB9J1

TDR PIN
DBBH1

TDR_INT2_50OHM

TDR PIN
DB4C2

TDR PIN
DB1C1

TDR_INT2_60OHM

TDR PIN
DB9J4

TDR PIN
DB1B1

TDR_BOTTOM_50OHM

TDR PIN
DB9J2

TDR PIN
DB4C1

TDR_BOT_60OHM

TDR PIN
DB8H2

TDR PIN
DB9J3
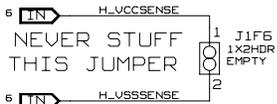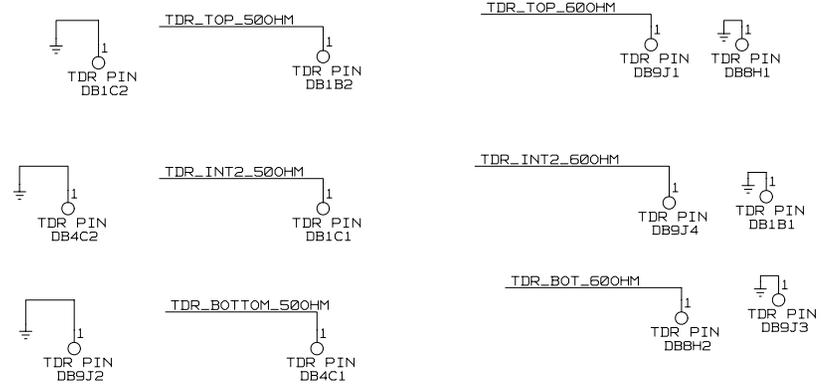
CAD NOTE:
PLACE JUMPER AS CLOSE TO
CPU PINS AS POSSIBLE

6 IN   H_VCCSENSE

NEVER STUFF
THIS JUMPER

1 J1F6
   1X2HDR
   EMPTY
2

6 IN   H_VSSSENSE

DESIGN NOTE:
NO HEADER SHOULD BE STUFFED (ALWAYS EMPTY)
NO SUITCASE JUMPER SHOULD BE ATTACHED
THE STAKE PINS WILL BE USED AS TEST/PROBE POINTS

DEBUG/EV FEATURE: POWER-ON FORCING HEADER

6 IN   H_SKTOCC*

TH
J2J1
1X3HDR
1
2   SLOTOCC*
3
HDR
102276-003

1 R2J1
   0
2 1A
   EMPTY
   603   OUT 67
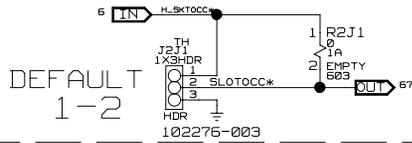
DEFAULT
1-2

DEBUG/EV FEATURE: BACKSIDE RESISTIVE TEST LOAD SITES

98 88 IN   VCCP

1 R3D1   1 R3R2   1 R3R1   1 R3R3
   1K   1K   1K   1K
   5%   5%   5%   5%
   EMPTY   EMPTY   EMPTY   EMPTY
   603   603   603   603
2   2   2   2

H_DP_PU<3..0>*   OUT 6
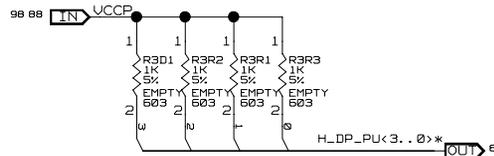
CAD NOTE:
PLACE ON BACKSIDE, KEEP DP TRACE SHORT

DEBUG/EV FEATURE: INVERTING LEVEL SHIFTERS ON PSB SIGNALS FOR DIAG LED'S

VCC3

R6H19
1K
5%
CH
603   DBG_CPURST   OUT 95

97 IN   H_CPURST*   2 R1C11 1   Q6H3
          4.7K   5%   MMBT3904
          603   CH   XSTR
                           108969-001

VCC3

R6J3
1K
5%
CH
603   DBG_SMI   OUT 95

96 IN   H_SMI_DEBUG* 2 R6J4 1   Q6J2
          4.7K   5%   MMBT3904
          603   CH   XSTR
                           108969-001

VCC3

R5H2
1K
5%
CH
603   DBG_STPCLK   OUT 95

IN   H_STPCLK_DEBUG* 2 R6H16 1   Q6H4
      4.7K   5%   MMBT3904
      603   CH   XSTR
                       108969-001

VCC3

R6J5
1K
5%
CH
603   DBG_IERR   OUT 95

76 IN   H_IERR*   2 R6J1 1   Q6J1
          4.7K   5%   MMBT3904
          603   CH   XSTR
                           108969-001

TDR COUPONS

DOCUMENT NUMBER	PAGE	REV
A95397	97	1.5

TEST FEATURE: LPC BUS DEBUG MODULE HEADER
CAD NOTE:
PLACE @ MID-POINT OF TRACE BETWEEN DEVICES

109717-120
J9H4
2X10HDR_4

CAD NOTE:
SIDE KEEP-OUT: 0.080"
END KEEP-OUT: 0.160"

27 IN L_FRAME*
95 IN P_PCIRST_DEBUG*
66 61 56 27 IN L_AD<3>

VCC

6   L_AD<2> IN 27 56 61 66
8   L_AD<1> IN 27 56 61 66

VCC3

L_AD<0> IN
67 44 40 39 38 37 36 27 B1 SMB_CLK_RESUME
68

SMB_DATA_RESUME B1 27 36 37 38 39 40 44 67 68
(SPDA2)
SER_IRQ IN 27 56 61
LPCPD IN 27 56 61

(SPDA1) TP.LPC.MODULE15

27 61 OUT KBRST*

14 IN CK_P_33M_FWHCLK 1 R7J6 2

0   1A
603 EMPTY

SMB ADDRESS
10101000
(SPDA2 PULLED-UP ON MODULE)

HDR

R9H8
1   2 A20GATE IN 27 61
0   1A
603 CH

R9H9
1   2 ICH_SUS_STAT IN 27
0   1A
603 EMPTY

DESIGN NOTE:
STUFF 0 OHM MANUALLY (DEBUG EXPERIMENTS)
CAD NOTE:
PLACE 0 OHM ON CLOCK SIGNAL BETWEEN FWH & LPC HDR &
CLOSE TO FWH FOR STUB REDUCTION

DESIGN NOTE:
STUFF 0 OHM MANUALLY FOR DEBUG
EXPERIMENTS. ONLY ONE SITE SHOULD
BE STUFFED AT A TIME.

DEBUG FEATURE: SMBUS LAI HEADER
J5C2
1X3HDR
1 SMB_CLK_MAIN IN 14 43 67
2
3 SMB_DATA_MAIN IN 14 43 67
HDR

TEST FEATURE: MEASUREMENT/CALIBRATION HEADERS FOR MARGINED VOLTAGES

J1F7
1X2HDR
6 7 OUT H_GTLREF 1
2
EMPTY

J4C2
1X2HDR
9 13 OUT HYSWING 1
2
EMPTY

J4H1
1X2HDR
94 79 68 22 17 13 11 10 78 OUT V_2P5_SM 1
2
EMPTY

J5C1
1X2HDR
94 9 13 OUT MCH_GTLREF 1
2
EMPTY

J4C1
1X2HDR
9 13 OUT HXSWING 1
2
EMPTY

J1H1
1X2HDR
25 24 23 20 19 18 79 OUT V_1P25_MEMVTT 1
2
EMPTY

J5E4
1X2HDR
11 13 OUT HI_AVREF 1
2
EMPTY

J1F9
1X2HDR
17 OUT DIMM_VREFA_1P25 1
2
EMPTY

J5D1
1X2HDR
94 30 28 15 13 11 87 OUT V_1P5_CORE 1
2
EMPTY

J5E2
1X2HDR
15 9 13 OUT AGPREF 1
2
EMPTY

J6G2
1X2HDR
29 30 OUT HI_VREF_ICH 1
2
EMPTY

J5E1
1X2HDR
94 13 11 86 OUT V_1P3_CORE 1
2
EMPTY

J1G3
1X2HDR
22 OUT DIMM_VREFB_1P25 1
2
EMPTY

J3E1
1X2HDR
10 13 OUT V1P25_MCH_VREF_A 1
2
EMPTY

J5F3
1X2HDR
13 12 8 7 5 100 OUT VCCP 1
97 89 68 30 28 86 14
2
EMPTY

CAD NOTE:
ADD NOTE IN SILK:
"NEVER SHORT HDR"
CAD NOTE:
PLACE TOPSIDE SILK LABELS FOR EACH HEADER
DESIGN NOTE:
HEADER SITES ONLY: NEVER STUFF JUMPERS

DESIGN NOTE:
HEADER SITES ONLY: NEVER STUFF SUITCASE JUMPERS
CAD NOTE:
PLACE TOPSIDE SILK LABELS FOR EACH HEADER

DEBUG HEADERS

DOCUMENT NUMBER PAGE REV
A95397   98   1.5

SPARE

TP_RP1_240_1   TP_RP2_240_1

1 RP9H1   2 RP9H1
   240   240
   5%   5%
   .063W   .063W
   IC   IC
8 SM   7 SM
TP_RP1_240_8   TP_RP2_240_8

VCC3

202285-049
FLIPFLOP_PORTB0_PRE
CK_P_33M_PORTB0_FF*

RP8J6
1K
5%
CH
603

U8J1
74LVC74

14 IN   CK_P_66M_PORTB0_R   3   D   Q   5   CK_P_33M_PORTB0   OUT   99

VCC3

PR*

CL*   IC

VCC=14 GND=7
POWER_GROUP=VCC=VCC3

202285-049
RP8J4
1K
5%
CH
603

CLEAR_FLIPFLOP_PORTB0

10 U8J1
74LVC74

12 D   Q   9
11
PR*
CL*   IC
8

VCC=14 GND=7
POWER_GROUP=VCC=VCC3

13 SPARE_PORTB0_FF

SPARE

VCC3
202285-049
RP8J5
1K
5%
CH
603

CAD NOTE: ORIENT TO LEFT

DS9J1
LED_DISPLAY_10P

EPM7032AETC44-10
44 PIN TQFP

U9J1
EPM7032 A38794-001

99 IN   CK_P_33M_PORT80   37 GCLK
95 IN   P_PCIRST_DEBUG*   39 GCLR
                           38 OE1
PORTB0_OE1_OE2_PD   40   OE2

1 202285-025
RP8J3
100
5%
CH
603
2

IO32 44   L_FRAME*   IN 27
IO31 43   TP_PORTB0_UNUSED_43
IO30 42   TP_PORTB0_UNUSED_42
IO29 35   TP_PORTB0_LED_RESET_35
IO28 34   LED_HI_OUT1   OUT 99
IO27 33   LED_HI_OUT2   OUT 99
IO26 32   TP_PORTB0_TDO_32
IO25 31   TP_PORTB0_UNUSED_31
IO24 30   TP_PORTB0_UNUSED_30
IO23 28   TP_PORTB0_UNUSED_28
IO22 27   TP_PORTB0_UNUSED_27
IO21 26   TP_PORTB0_TCK_26
IO20 25   LED_HI_OUT0   OUT 99
IO19 23   LED_LO_OUT0   OUT 99
IO18 22   LED_HI_OUT6   OUT 99
IO17 21   LED_HI_OUT5   OUT 99
IO16 20   LED_HI_OUT4   OUT 99
IO15 19   LED_HI_OUT3   OUT 99
IO14 18   TP_PORTB0_UNUSED_18
IO13 15   LED_LO_OUT5   OUT 99
IO12 14   LED_LO_OUT1   OUT 99
IO11 13   LED_LO_OUT2   OUT 99
IO10 12   LED_LO_OUT3   OUT 99
IO9   11   LED_LO_OUT4   OUT 99
IO8   10   TP_PORTB0_UNUSED_10
IO7   8   TP_PORTB0_UNUSED_8
IO6   7   TP_PORTB0_TMS_7
IO5   6   L_AD<3>   IN 27 56 61 66
IO4   5   L_AD<2>   IN 27 56 61 66
IO3   3   L_AD<1>   IN 27 56 61 66
IO2   2   L_AD<0>   IN 27 56 61 66
IO1   1   TP_PORTB0_TDI_1

IC
VCC(PQFP)=9,17,29,41
GND(PQFP)=4,16,24,36
NC(PQFP)=45
VCC=VCC3(~PORT80DEC)

ALL RPACKS 240 OHMS

CAD NOTE: ORIENT TO RIGHT

DS9J2
LED_DISPLAY_10P

RP9J3   RP9J3   RP9J3
99 IN LED_HI_OUT0   LED_HI_OUT0_R   1 A
99 IN LED_HI_OUT1   LED_HI_OUT1_R 10 B
99 IN LED_HI_OUT2   LED_HI_OUT2_R   8 C
99 IN LED_HI_OUT3   RP9J2   LED_HI_OUT3_R   5 D
99 IN LED_HI_OUT4   RP9J2   LED_HI_OUT4_R   4 E
99 IN LED_HI_OUT5   RP9J2   LED_HI_OUT5_R   2 F
99 IN LED_HI_OUT6   LED_HI_OUT6_R   3 G
                      TP_PORTB0_HI_7 7 DP
                      240 5%.063W
                      SM

6 VCC3
ANODE
9 VCC3

A30432-002 IC

RP9J2   RP9J3
99 IN LED_LO_OUT0   LED_LO_OUT0_R   1 A
99 IN LED_LO_OUT1   RP9J1   LED_LO_OUT1_R 10 B
99 IN LED_LO_OUT2   RP9H1   LED_LO_OUT2_R   8 C
99 IN LED_LO_OUT3   RP9H1   LED_LO_OUT3_R   5 D
99 IN LED_LO_OUT4   RP9J1   LED_LO_OUT4_R   4 E
99 IN LED_LO_OUT5   RP9J1   LED_LO_OUT5_R   2 F
99 IN LED_LO_OUT6   RP9J1   LED_LO_OUT6_R   3 G
                      TP_PORTB0_LO_7 7 DP
                      240 5%.063W
                      SM   IC

6 VCC3
ANODE
9 VCC3

A30432-002 IC

TEST FEATURE: PORT 80 DECODER & DISPLAY

LPC DEBUG / PORT 80

CAD NOTE: PLACE 1 EACH ON PINS 6 & 9 OF EACH DISPLAY

VCC3   VCC3
C9J1   C9H4
.1UF 20%   .1UF 20%
25V   25V
603   603
C9J2   C8J1
.1UF 20%   .1UF 20%
25V   25V
603   603

ITP CONNECTOR

98 88 IN VCCP

C1D3
.1UF
20%
25V
Y5V
603

C1C6
.1UF
20%
25V
Y5V
603

R1D17
39
5%
CH
603

VCC3

R1C8
150
5%
CH
603

R1D11
75
5%
CH
603

R1D8
27
5%
CH
603

J1D1
MINI-ITP-28P

76	H_BPM5_PREQ*	13	BPM5	TDO	7	H_TDO		5
76	H_BPM4_PRDY*	15	BPM4	TCK	5	H_TCK		
76	H_BPM3_ITP*	17	BPM3	TDI	1	H_TDI		76
76	H_BPM2_ITP*	19	BPM2	TMS	2	H_TMS		
76	H_BPM1_ITP*	21	BPM1	TRST	3	H_TRST*		76

IN ... 100

"NC" 4 NC   DBR 25   FP_RST_ITP*
"NC" 6 NC   DBA 24 "NC"

R1C9
1   2   FP_RST*
0   1A
603 CH
OUT 6 70 96 27

68 IN

14 IN CK_H_100_133M_ITP_DWN*
14 IN CK_H_100_133M_ITP_DWN   8 BCLKN
                                  9 BCLKP   VTAP 26
100 IN H_TCK   11 FBO   VTT 27
                                             VTT 28   VCCP
H_CPURST_ITP_HDR* 1 R1D6 2 H_CPURST_ITP_3* 12 RST   IN 88 98
                   150 603 1% CH

A52499-001   CONN
GND=10,14,16,18,20,22

R1D2
97 IN H_CPURST* 1 2
              0   1A
              603 CH

R1D7
49.9
1%
EMPTY
603

98 88 IN VCCP

DESIGN NOTE:
0 OHM SERIES IS STUFFED WHEN ITP HEADER IS INSTALLED

49.9 OHM PULL-UP RESISTOR FOR H_CPURST* IS ALWAYS EMPTY
MANUALLY EMPTY THE 0 OHM RES AND STUFF 49.9 OHM FOR ITP WITHOUT MB RESET

CAD NOTE:
ROUTE H_TCK FROM THE TCK PIN OF THE CONNECTOR TO THE PROCESSOR PIN
FBO TAPS INTO THE H_TCK SIGNAL (CLOSE TO THE TCK PIN OF THE CONNECTOR) WITH LENGTH REQUIREMENTS.
SEE ROUTING GUIDELINES FOR LENGTH MATCHING REQUIREMENTS

ITP

*** Signal Cross-Reference ***
--- for the entire design --

Signal	Pages
1P3_CORE_358_MINUS_2	86
1P3_CORE_358_OUT_1	86
1P3_CORE_358_OUT_7	86
1P3_CORE_358_PLUS_3	86
1P25_MEMVTT_FILTER	79
2P5_DRVH	78
2P5_DRVL	78
2P5_PHASE	78
2P5_PHASE_IND	78
2P5_PHASE_R	78
2P5_PHASE_R_PN1	78
2P5_REF_BYPASS	78
2P5_SM_PHASE_GATE	78
2P5_SM_SENSE	78
12V_SWITCHED_PN1	79
12V_SWITCHED_RES_XSTR_PN1	79
1394HDR3_12V_FUSE	57
1394HDRFP_12V_FUSE	57
1394HDR_12V_FUSE	57 58
1394HDR_12V_FUSE_DIO_HDR2	57
1394HDR_12V_FUSE_DIO_HDR3	57
1394HDR_12V_FUSE_DIO_PWR_9	57
1394HDR_12V_FUSE_PWR_9	57
1394HDR_DIVIDER_STRAP_0	57
1394HDR_DIVIDER_STRAP_1	57
1394HDR_DIVIDER_STRAP_2	57
1394_CLKRUN*	58
1394_CPS_PWR	58
1394_CYCLE_STRAP	58
1394_DVDD_FB	58
1394_FILTER0	58
1394_FILTER1	58
1394_GPIO_STRAP	58
1394_PHY_TEST_MA	58
1394_PLL_VDD_FB	58
1394_R0_STRAP	58
1394_R1_STRAP	58
1394_REG18A	58
1394_REG18B	58
1394_SCL	58
1394_SDA	58
1394_XTAL_XI	58
1394_XTAL_XO	58
A20GATE	27 61 98
ADJ_1P5_STBY	84
AGPREF	13 98 9 15
AGP_PRO_PRSNT1	15 29
AGP_PRO_PRSNT2	15 29
AGP_PSWING	13 9
APICD0_1	30 27
AUD_3D_C	48
AUD_3D_R	48
AUD_AFLT1	48 49
AUD_AFLT2	48 49
AUD_AFLT3	48
AUD_AFLT4	48 49
AUD_A_REFFLT	48 49
AUD_A_VREF	48 55
AUD_CDC_LOUT	48 52
AUD_CDC_ROUT	48 52
AUD_CDGND	50 48
AUD_CDGND_C	50
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*** Unit Cross-Reference ***
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C1F1  CAP-P  89      C2C8  CAPN   89      C2J3  capn   80      C3J2  capn   78
C1F2  CAPN   17      C2C9  CAPN   89      C2J4  capn   80      C3J3  CAP-P  80
C1F3  CAPN   17      C2C10 CAPN   89      C2J5  capn   80      C3J4  capn   80
C1F4  CAPN   22      C2C11 CAPN   89      C2J6  capn   80      C4A1  capn   83
C1G1  CAPN   22      C2C12 CAPN   89      C2J7  CAPN   85      C4A2  capn   64
C1G2  CAPN   17      C2C13 CAPN   8       C2J8  capn   80      C4A3  capn   64
C1G3  CAPN   17      C2C14 CAPN   8       C2J9  capn   80      C4A4  CAP-P  83
C1G4  CAPN   22      C2C15 CAPN   89      C2J10 capn   80      C4B1  CAPN   47
C1G5  CAPN   22      C2C16 CAPN   89      C2J11 capn   80      C4B2  CAPN   47
C1G6  capn   65      C2C17 CAPN   89      C3A1  capn   64      C4B3  CAPN   47
C1G7  capn   65      C2C18 CAPN   89      C3A2  capn   64      C4B4  CAPN   88
C1H1  CAPN   25      C2D1  CAPN   89      C3A3  capn   64      C4B5  CAPN   88
C1H2  CAPN   25      C2D2  CAPN   89      C3A4  capn   64      C4B6  CAPN   80
C1H3  CAPN   25      C2D3  CAPN   89      C3A5  capn   64      C4B7  CAPN   88
C1H4  CAPN   25      C2D4  CAPN   89      C3A6  capn   64      C4B8  CAPN   80
C1H5  CAP-P  20      C2D5  CAPN   89      C3A7  capn   64      C4B9  CAPN   88
C1H6  CAPN   25      C2D6  CAPN   89      C3A8  capn   64      C4B10 CAPN   89
C1H7  CAPN   25      C2D7  CAPN   89      C3A9  capn   64      C4B11 CAPN   89
C1H8  CAPN   25      C2D8  CAPN   89      C3A10 capn   64      C4B12 CAPN   89
C1H9  CAPN   25      C2D9  CAPN   89      C3A11 capn   64      C4B13 CAPN   88
C1H10 capn   65      C2D10 CAPN   89      C3A12 capn   64      C4B14 CAPN   88
C1H11 CAPN   25      C2D11 CAPN   89      C3A13 capn   64      C4B15 CAPN   88
C1H12 CAPN   25      C2D12 CAPN   89      C3A14 capn   64      C4B16 CAPN   89
C1H13 CAPN   25      C2E1  CAPN   89      C3B1  CAPN   88      C4B17 CAPN   89
C1H14 CAP-P  61      C2E2  CAPN   89      C3B2  CAPN   88      C4B18 CAP-P  89
C1H15 CAPN   67      C2E3  CAPN   89      C3B3  CAPN   88      C4B19 CAP-P  89
C1H16 CAPN   61      C2E4  CAPN   89      C3B4  CAPN   88      C4B20 CAP-P  89
C1H17 capn   61      C2E5  CAPN   89      C3B5  CAPN   88      C4B21 CAPN   47
C1H18 CAPN   61      C2E6  CAPN   89      C3B6  CAPN   88      C4C1  CAPN   13
C1H19 CAPN   67      C2E7  CAPN   89      C3B7  CAPN   88      C4C2  CAPN   13
C1H20 CAPN   67      C2E8  CAPN   89      C3B8  CAP-P  89      C4C3  CAPN   13
C1H21 CAPN   61      C2E9  CAPN   89      C3C1  CAPN   88      C4C4  CAPN   13
C1H22 CAPN   61      C2E10 CAPN   89      C3E1  CAPN   13      C4C5  CAPN   13
C1J1  CAPN   61      C2E11 CAPN   89      C3E2  CAPN   13      C4C6  CAPN   13
C1J2  CAPN   61      C2E12 CAPN   89      C3F1  CAP-P  13      C4C7  CAPN   13
C1J3  CAPN   67      C2F1  CAP-P  89      C3H1  CAPN   20      C4C8  CAPN   13
C1J4  CAPN   67      C2F2  CAP-P  89      C3H2  CAPN   20      C4C9  CAPN   13
C1J6  CAPN   61      C2F3  CAP-P  89      C3H3  CAPN   20      C4C10 CAPN   13
C2A1  CAP-P  82      C2H1  CAPN   25      C3H4  CAPN   20      C4C11 CAPN   13
C2A2  capn   65      C2H2  CAPN   25      C3H5  CAPN   20      C4D1  CAPN   13
C2A3  capn   65      C2H3  CAPN   25      C3H6  CAPN   20      C4D2  CAPN   13
C2A4  capn   65      C2H4  CAPN   25      C3H7  CAPN   20      C4D3  CAPN   13
C2A5  capn   64      C2H5  CAPN   25      C3H8  CAPN   20      C4D4  CAPN   13
                     C2H6  CAPN   25      C3H9  CAPN   20      C4D5  CAPN   13
                     C2H7  CAPN   25      C3H10 CAPN   25      C4D6  CAPN   13
                     C2H8  CAPN   25      C3H11 CAPN   20      C4E1  CAPN   13
```

```
C4E2   CAPN   13        C5B11 CAPN   14        C6A14 NCAP   47        C6H3  CAPN   30
C4E3   CAPN   13        C5B12 CAPN   14        C6A15 CAPN   46        C6H4  CAPN   79
C4E4   CAPN   13        C5C1  CAPN   14        C6B1  CAPN   46        C6H5  CAPN   30
C4E7   CAPN   13        C5C2  CAPN   14        C6B2  CAPN   55        C6H6  CAPN   79
C4E8   CAPN   13        C5C3  CAPN   14        C6B3  CAPN   46        C6H7  CAPN   56
C4E9   CAPN   13        C5C4  CAP-P  14        C6B4  CAPN   46        C6J1  CAPN   56
C4E10  CAPN   13        C5C5  CAPN   14        C6B5  CAPN   46        C6J2  CAPN   56
C4E11  CAPN   13        C5C6  CAPN   14        C6B6  CAPN   46        C6J3  CAPN   75
C4E12  CAPN   13        C5C7  CAPN   14        C6B7  CAPN   46        C6J4  CAPN   75
C4E13  CAPN   13        C5C8  CAP-P  11        C6B8  CAPN   46        C6J5  CAPN   75
C4E14  CAPN   13        C5C9  NCAP   94        C6B9  CAPN   46        C6J6  CAPN   75
C4F1   CAP-P  13        C5C10 CAP-P  11        C6B10 CAPN   14        C6J7  CAPN   75
C4F2   CAP-P  13        C5C11 CAPN   13        C6B11 CAPN   14        C7A1  CAP-P  52
C4H1   CAPN   20        C5C12 CAPN   13        C6B12 CAPN   14        C7A2  CAPN   55
C4H2   CAPN   20        C5C13 CAPN   13        C6B13 CAPN   46        C7A3  CAPN   55
C4H3   CAPN   20        C5C14 CAPN   11        C6B14 CAPN   46        C7A4  CAPN   55
C4H4   CAPN   20        C5C15 CAPN   11        C6B15 CAPN   14        C7A5  CAPN   55
C4H5   CAPN   20        C5D1  CAPN   13        C6B16 CAPN   85        C7A6  CAPN   50
C4H6   CAPN   20        C5D2  CAP-P  13        C6B17 CAPN   14        C7A7  CAP-P  52
C4H7   CAPN   20        C5D3  CAPN   13        C6B18 CAPN   14        C7A8  CAPN   55
C4H8   CAPN   20        C5D4  CAPN   13        C6C1  CAPN   14        C7A9  CAP-P  55
C4H9   CAPN   20        C5D5  CAPN   86        C6C2  CAPN   14        C7A10 CAPN   55
C4H10  CAPN   20        C5D6  CAPN   13        C6C3  CAP-P  85        C7A11 CAPN   55
C4H11  CAPN   20        C5D7  CAPN   13        C6C4  CAPN   14        C7B1  CAPN   55
C4H12  CAPN   20        C5D8  CAPN   13        C6C5  CAPN   14        C7B2  CAPN   55
C4H13  CAPN   20        C5D9  CAPN   13        C6C6  CAPN   85        C7B3  capn   53
C4H14  CAPN   20        C5D10 CAPN   13        C6C7  CAPN   14        C7B4  capn   85
C4H15  CAPN   20        C5E1  CAPN   13        C6C8  CAPN   14        C7B5  capn   53
C4H16  CAPN   20        C5E2  CAPN   13        C6C9  CAP-P  85        C7B6  CAPN   85
C4H17  CAPN   20        C5E3  CAP-P  86        C6C10 CAPN   14        C7B7  CAPN   85
C4H18  CAPN   20        C5E4  CAPN   13        C6C12 CAPN   15        C7B8  capn   53
C4H19  CAPN   20        C5E5  CAPN   86        C6C13 CAP-P  41        C7B9  capn   53
C4H20  CAPN   20        C5E6  CAPN   13        C6C14 CAPN   15        C7B10 CAP-P  41
C4H21  CAPN   20        C5E7  CAPN   86        C6C15 CAP-P  15        C7B11 CAPN   15
C4H22  CAPN   20        C5E8  CAPN   86        C6D1  CAP-P  15        C7B12 capn   53
C4H23  CAPN   20        C5E9  CAPN   13        C6D2  CAPN   15        C7B13 capn   53
C4H24  CAPN   20        C5E10 CAPN   13        C6E1  CAPN   86        C7B14 capn   53
C4H25  CAPN   20        C5E11 CAPN   13        C6E2  CAP-P  41        C7B15 CAP-P  81
C4H26  CAPN   25        C5E12 CAPN   13        C6E3  CAPN   15        C7C1  capn   81
C4H27  CAPN   25        C5E13 CAPN   13        C6E4  CAPN   15        C7C2  capn   81
C4H28  CAPN   25        C5E14 CAP-P  13        C6E5  CAPN   87        C7C3  capn   81
C4H29  capn   78        C5E15 CAPN   13        C6E6  CAPN   15        C7C4  capn   81
C4H30  CAP-P  78        C5F1  CAP-P  13        C6E7  CAP-P  87        C7C5  capn   81
C4H31  capn   78        C5H1  CAPN   25        C6E8  CAPN   15        C7C6  CAPN   85
C4H32  CAPN   32        C5H2  CAPN   20        C6E9  CAP-P  86        C7C7  CAP-P  41
C4H33  CAPN   32        C5H3  CAPN   20        C6E10 CAPN   15        C7C8  CAPN   41
C4R1   NCAP   94        C5H4  CAPN   20        C6E11 CAPN   15        C7C9  CAP-P  41
C4R2   NCAP   94        C5H5  CAPN   79        C6E12 CAPN   13        C7D1  CAPN   41
C4R3   NCAP   94        C5H6  CAPN   79        C6F1  CAPN   87        C7D2  CAPN   41
C4R4   NCAP   94        C5H7  CAPN   25        C6F2  CAP-P  87        C7D3  CAPN   41
C5A1   capn   54        C5H8  CAPN   20        C6F3  CAPN   13        C7D4  CAP-P  41
C5A2   capn   52        C5H9  CAPN   20        C6F4  CAPN   13        C7D5  CAPN   85
C5A3   CAPN   46        C5H10 CAP-P  79        C6F5  CAP-P  13        C7E1  CAP-P  41
C5A4   CAPN   46        C5R1  NCAP   94        C6F6  CAP-P  35        C7E2  CAP-P  41
C5A5   CAPN   50        C5R2  NCAP   94        C6G1  CAPN   30        C7E3  CAPN   42
C5A6   capn   52        C5R3  NCAP   94        C6G2  CAPN   85        C7F1  CAPN   42
C5A7   CAPN   50        C5R4  NCAP   94        C6G3  CAPN   30        C7F2  CAPN   42
C5A8   capn   51        C6A1  CAPN   46        C6G4  capn   30        C7F3  capn   35
C5A9   capn   51        C6A2  CAPN   46        C6G5  CAP-P  28        C7F4  capn   42
C5A10  CAPN   47        C6A3  CAPN   55        C6G6  CAPN   30        C7F5  capn   35
C5B1   CAPN   14        C6A4  CAPN   46        C6G7  CAPN   30        C7F6  CAPN   30
C5B2   CAPN   14        C6A5  CAPN   46        C6G8  CAPN   28        C7G1  CAPN   30
C5B3   CAPN   14        C6A6  CAPN   46        C6G9  CAPN   30        C7G2  CAPN   30
C5B4   CAPN   14        C6A7  CAPN   46        C6G10 CAPN   28        C7G3  CAPN   30
C5B5   CAPN   14        C6A8  CAPN   46        C6G11 CAPN   30        C7G4  CAPN   30
C5B6   CAPN   14        C6A9  NCAP   47        C6G12 CAPN   30        C7G5  CAPN   85
C5B7   CAPN   14        C6A10 CAPN   45        C6G13 CAPN   30        C7G6  CAPN   30
C5B8   CAPN   14        C6A11 NCAP   47        C6G14 CAPN   79        C7G7  CAPN   30
C5B9   CAPN   14        C6A12 NCAP   47        C6H1  CAPN   30        C7G8  CAPN   30
C5B10  CAPN   14        C6A13 CAPN   46        C6H2  CAPN   79        C7G9  CAPN   30
```

Ref	Type	Pg
C7G10	capn	30
C7G11	capn	30
C7G12	capn	30
C7G13	capn	30
C7H1	CAPN	85
C7H2	CAPN	30
C7H3	CAPN	30
C7H4	CAPN	30
C7H5	CAPN	30
C7H6	CAPN	30
C7H7	CAPN	30
C7H8	CAPN	30
C7H9	CAPN	30
C7H10	capn	66
C7H11	capn	66
C7J1	capn	66
C7J2	capn	66
C7J3	capn	70
C7J4	capn	66
C8A1	CAPN	49
C8A2	CAPN	49
C8A3	capn	49
C8A5	capn	51
C8A6	CAPN	51
C8A8	CAPN	49
C8A9	CAPN	48
C8A10	capn	48
C8A11	capn	51
C8A12	capn	51
C8A13	capn	51
C8A14	CAPN	50
C8A15	capn	50
C8A16	capn	51
C8A17	capn	50
C8A18	CAPN	51
C8A19	capn	51
C8A20	capn	50
C8A21	capn	50
C8A22	capn	50
C8A23	capn	50
C8B1	CAPN	48
C8B2	capn	48
C8B3	capn	48
C8B4	capn	48
C8B7	CAP-P	85
C8B8	CAPN	41
C8B10	CAPN	41
C8B11	CAP-P	41
C8B12	CAPN	41
C8C1	CAP-P	41
C8C2	CAPN	41
C8D1	CAP-P	41
C8D2	CAP-P	41
C8D3	CAPN	15
C8E1	CAP-P	41
C8E2	CAPN	58
C8E3	CAPN	58
C8E4	CAPN	58
C8E5	CAPN	58
C8F1	CAPN	58
C8F2	CAPN	85
C8F3	CAPN	58
C8F4	CAPN	85
C8F5	CAPN	58
C8F6	CAPN	58
C8F7	CAPN	58
C8F8	CAPN	58
C8F9	CAPN	58
C8F10	CAPN	58
C8F11	CAPN	85

Ref	Type	Pg
C8F12	CAPN	84
C8F13	CAP-P	85
C8F14	CAPN	58
C8F15	capn	84
C8G1	CAPN	60
C8G2	CAPN	60
C8G3	CAPN	60
C8G4	CAPN	60
C8G5	CAPN	60
C8G6	CAPN	60
C8H1	CAPN	60
C8H2	CAPN	60
C8H3	CAPN	60
C8H4	CAPN	60
C8H5	CAPN	60
C8H6	CAPN	81
C8H7	CAPN	30
C8H8	CAPN	69
C8H9	capn	74
C8J1	CAPN	99
C8J2	CAPN	70
C8J3	CAPN	70
C9A1	CAPN	52
C9A3	capn	49
C9A5	CAPN	49
C9A7	capn	48
C9A11	CAPN	48
C9A12	CAPN	52
C9A13	CAP-P	54
C9A14	CAPN	54
C9B1	capn	54
C9B2	CAPN	54
C9B3	CAPN	48
C9B4	CAPN	54
C9B5	CAPN	54
C9B6	capn	48
C9B7	CAPN	85
C9B8	CAP-P	48
C9B9	capn	43
C9B10	CAP-P	41
C9B11	capn	41
C9C1	capn	81
C9C2	CAP-P	54
C9C3	CAPN	41
C9D1	capn	34
C9D2	CAPN	41
C9D3	CAPN	41
C9D4	capn	43
C9E1	CAP-P	41
C9E2	capn	43
C9E3	CAPN	58
C9E4	CAPN	58
C9E5	CAPN	58
C9E6	CAPN	58
C9E7	CAPN	58
C9E8	CAPN	57
C9E9	CAPN	58
C9F1	CAPN	57
C9F2	CAPN	57
C9F3	CAPN	57
C9F4	CAPN	58
C9F5	CAPN	57
C9F6	CAPN	58
C9F7	CAPN	57
C9F8	CAPN	57
C9F9	CAPN	57
C9F10	CAPN	58
C9F11	CAPN	58
C9F12	CAPN	57
C9F13	CAPN	58

Ref	Type	Pg
C9F14	CAP-P	85
C9F15	CAPN	58
C9G1	CAPN	85
C9G2	CAP-P	59
C9G3	CAPN	60
C9G4	CAPN	60
C9G5	CAPN	59
C9G6	CAPN	59
C9G7	CAPN	60
C9G8	CAPN	60
C9G9	CAPN	60
C9G10	CAPN	60
C9G11	CAPN	60
C9H1	CAPN	60
C9H2	CAPN	60
C9H3	CAPN	60
C9H4	CAPN	99
C9H5	CAPN	58
C9J1	CAPN	99
C9J2	CAPN	99
CP8J1	CPAK4C4C	70
CP8J2	CPAK4C4C	70
CR1A1	DIODE	57
CR1A2	DIODE_DUAL	35
CR1A3	DIODE_DUAL	35
CR1A4	DIODE_DUAL	35
CR1A5	DIODE_DUAL	35
CR2B1	DIOSOT23C	88
CR2J1	LED	80
CR3B1	DIOSOT23C	88
CR3B2	DIOSOT23C	88
CR4B1	DIODE_DUAL	33
CR4B2	DIODE_DUAL	33
CR4B3	DIODE_DUAL	33
CR4B4	DIODE_DUAL	33
CR4B5	ZENER	88
CR5B1	LED	85
CR5H1	LED	95
CR5J1	LED	95
CR6H1	DIOSOT23C	79
CR6H2	LED	95
CR6H3	LED	95
CR6H4	LED	95
CR6H5	LED	95
CR6J1	LED	95
CR6J2	LED	95
CR6J3	DUAL_LED	95
CR7H1	LED	95
CR8H1	DIOSOT23C	81
CR8J1	LED	95
CR9B1	LED	95
CR9E1	DIODE	57
CR9F1	DIODE	57
CRP1A1	TVS6_2V	63
DB1B1	TDR_PIN	97
DB1B2	TDR_PIN	97
DB1C1	TDR_PIN	97
DB1C2	TDR_PIN	97
DB4C1	TDR_PIN	97
DB4C2	TDR_PIN	97
DB8H1	TDR_PIN	97
DB8H2	TDR_PIN	97
DB9J1	TDR_PIN	97
DB9J2	TDR_PIN	97
DB9J3	TDR_PIN	97
DB9J4	TDR_PIN	97
DS9J1	LED_DISPLAY_10P	99
DS9J2	LED_DISPLAY_10P	99
FB1A1	FERRITE	82
FB1A2	FERRITE	57

Ref	Type	Pg
FB1A3	FERR_BD	63
FB1A4	FERR_BD	63
FB1A5	FERR_BD	63
FB1A6	FERR_BD	63
FB5A1	FERR_BD	52
FB5A2	FERR_BD	50
FB5A3	FERR_BD	50
FB5A4	FERR_BD	51
FB5A5	FERR_BD	51
FB5A6	FERR_BD	52
FB5C1	FERRITE	14
FB5C2	FERRITE	14
FB9E1	FERR_BD	58
FB9F1	FERR_BD	58
FB9G1	FERR_BD	60
J1A1	PS2STACK	63
J1A2	1394_2USB_STACK	57
J1A3	CON2XUSB	35
J1B1	1X3HDR	72
J1D1	MINI_ITP_20P	100
J1E1	NWD470_GB	6
J1F1	1X3HDR	96
J1F2	1X3HDR	96
J1F3	1X3HDR	96
J1F4	1X3HDR	96
J1F5	1X3HDR	96
J1F6	1X2HDR	97
J1F7	1X2HDR	98
J1F8	DIMM2P_184_1GB	17
J1F9	1X2HDR	98
J1F10	DIMM2P_184_1GB	22
J1G1	DIMM2P_184_1GB	17
J1G2	DIMM2P_184_1GB	22
J1G3	1X2HDR	98
J1H1	1X2HDR	98
J2A1	DSUB9	65
J2H1	1X4HDR	75
J2J1	1X3HDR	97
J2J2	1X6PWR	76
J2J3	1X2HDR	67
J2J4	2X10PWR	80
J3A1	DSUB25TALL	64
J3E1	1X2HDR	98
J4A1	CON2XUSB	33
J4C1	1X2HDR	98
J4C2	1X2HDR	98
J4C3	ANCHOR_CLP_GHST	13
J4E1	ANCHOR_CLP_GHST	13
J4H1	1X2HDR	98
J5A1	AUDIO3STACK	50 51 52
J5B1	1X3HDR	96
J5B2	2X2HDR	80
J5C1	1X2HDR	98
J5C2	1X3HDR	98
J5C3	ANCHOR_CLP_GHST	13
J5D1	1X2HDR	98
J5E1	1X2HDR	98
J5E2	1X2HDR	98
J5E3	ANCHOR_CLP_GHST	13
J5E4	1X2HDR	98
J5F3	1X2HDR	98
J5H1	2X20HDR20	32
J5J2	2X20HDR20	32
J5J3	2X17HDR3_5	52
J6B1	1X3HDR	72
J6B2	CONPCI2_2	40
J6B3	AGPPRO_4X_8X	15
J6G1	1X2HDR	65
J6G2	1X2HDR	98
J6J1	1X8HDR2NC	75

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Ref	Type	Value
J7B1	1X4HDR_COLOR	50
J7B2	1X4HDR_COLOR	50
J7B3	CONPCI2_2	39
J7B4	2X5HDR8	53
J7C1	1X2HDR	55
J7E1	2X5HDR9	35
J7F1	2X5HDR10	74
J7H1	1X3HDR	66
J7J1	2X10HDR10	74
J8B1	1X4HDR	50
J8B2	CONPCI2_2	37
J8B3	CONPCI2_2	38
J8H1	1X2HDR	30
J8H2	1X2HDR	30
J8H3	1X3HDR	30
J8J1	1X3HDR2	70
J8J2	2X8HDR10_14	70
J8J3	MFG_MODE_JMPR	66
J9B1	CNR60_ICH4	43
J9B2	CONPCI2_2	36
J9F1	2X5HDR9	57
J9F2	2X5HDR9	57
J9G1	1X7HDR	60
J9G2	1X7HDR	60
J9H1	1X3HDR	72
J9H2	1X2HDR	30
J9H3	1X2HDR	75
J9H4	2X10HDR4	98
J9J1	SWSPSTPB_SM	96
J9J2	SWSPSTPB_SM	96
JA4A1	GBE_MAGJACK3_10	47
L1A1	IND_4PIN	57
L1A2	IND_4PIN	35
L1A3	IND_4PIN	35
L1A4	IND_4PIN	57
L1B1	INDUCTOR	88
L2B1	INDUCTOR	88
L2C1	INDUCTOR	8
L3B1	INDUCTOR	88
L3C1	INDUCTOR	8
L3J1	INDUCTOR	78
L3J2	INDUCTOR	78
L4B1	IND_4PIN	33
L4B2	IND_4PIN	33
L4B3	INDUCTOR	89
L5C1	INDUCTOR	11
L5C2	INDUCTOR	11
L9B1	INDUCTOR	54
LS8H1	SPKR	69
MH1B1	STD_MTG_HOLE	71
MH1G1	STD_MTG_HOLE	71
MH1J1	STD_MTG_HOLE	71
MH5A1	STD_MTG_HOLE	71
MH5G1	STD_MTG_HOLE	71
MH5J1	STD_MTG_HOLE	71
MH7A1	STD_MTG_HOLE	71
MH9A1	STD_MTG_HOLE	71
MH9G1	STD_MTG_HOLE	71
MH9J1	STD_MTG_HOLE	71
Q1B1	STD40NF3LL	88
Q1B2	SUB70N03_09	88
Q1B3	FET_VREG	88
Q1C1	FET	72
Q1C3	MBT3904DUAL	88
Q1G1	NPN	72
Q2A1	NPN	82
Q2A2	SI4501DY	82
Q2B1	SUB70N03_09	88
Q2B2	STD40NF3LL	88
Q2B3	FET_VREG	88
Q2B4	FET_VREG	88
Q2B5	FET_VREG	88
Q2H1	NPN	68
Q2H2	STD40NF3LL	78
Q3B1	PZT2222A	88
Q3B2	SUB70N03_09	88
Q3B3	STD40NF3LL	88
Q3B4	FET_VREG	88
Q3B5	FET_VREG	88
Q3C1	FET_VREG	88
Q3C2	FET_VREG	88
Q3C3	FET_VREG	88
Q3H1	FET_VREG	78
Q3H2	STD40NF3LL	78
Q4A1	NPN	83
Q4A2	SI4501DY	83
Q5B1	NPN	72
Q5B2	NPN	95
Q5C1	NPN	14
Q5D1	MTD1312	86
Q5D2	MTD1312	86
Q5H1	PMOSFET	79
Q5H2	MTD1312	79
Q6A1	BCP69T1	46
Q6A2	BCP69T1	46
Q6D1	MBT3904DUAL	15
Q6F1	NPN	15
Q6H1	NPN	79
Q6H3	NPN	97
Q6H4	NPN	97
Q6H5	MBT3904DUAL	66
Q6J1	NPN	97
Q6J2	NPN	97
Q7A1	PNP	55
Q7B1	PNP	55
Q7B2	PNP	55
Q7C1	SI4501DY	81
Q7E1	MBT3904DUAL	34
Q7J1	FET	66
Q8H1	NPN	69
Q9B1	MBT3904DUAL	81
Q9C2	MBT3904DUAL	81
Q9D1	SI4501DY	34
Q9H1	NPN	72
R1A1	resn	57
R1A2	RESN	35
R1A3	RESN	35
R1A4	RESN	35
R1A5	RESN	57
R1A6	RESN	35
R1A7	RESN	57
R1B1	RESN	57
R1B2	RESN	88
R1B3	resn	72
R1B4	RESN	88
R1B5	resn	72
R1B6	resn	72
R1B7	resn	72
R1C1	RESN	6
R1C5	RESN	88
R1C7	RESN	87
R1C8	RESN	100
R1C9	RESN	100
R1C10	RESN	7
R1C11	RESN	97
R1D1	RESN	6
R1D2	RESN	100
R1D3	RESN	7
R1D5	RESN	7
R1D6	RESN	100
R1D7	RESN	100
R1D8	RESN	100
R1D9	RESN	7
R1D10	RESN	7
R1D11	RESN	100
R1D12	RESN	7
R1D13	RESN	7
R1D14	resn	68
R1D15	resn	68
R1D16	resn	68
R1D17	RESN	100
R1E1	resn	68
R1E2	RESN	7
R1E3	resn	68
R1E4	RESN	7
R1E5	RESN	6
R1F1	RESN	96
R1F2	RESN	96
R1F3	RESN	96
R1F4	RESN	96
R1F5	RESN	96
R1F7	RESN	17
R1F8	RESN	17
R1G2	resn	72
R1G3	RESN	22
R1G5	RESN	22
R1G6	resn	72
R1H1	RESN	61
R1H2	RESN	61
R1H4	RESN	67
R1H5	RESN	61
R1H6	RESN	67
R1H7	RESN	67
R1H8	RESN	67
R1H9	resn	75
R1H10	RESN	67
R1H11	RESN	67
R1J1	RESN	62
R1J2	RESN	61
R1J4	RESN	61
R1J5	RESN	61
R1J10	RESN	61
R1J11	RESN	61
R1J12	RESN	61
R2A1	resn	82
R2B1	RESN	88
R2B2	RESN	88
R2B3	RESN	88
R2C1	RESN	8
R2G1	RESN	23
R2H1	RESN	18
R2J1	RESN	97
R2J2	resn	80
R2J3	resn	80
R2R1	GND_ISOLATION	88
R2R2	GND_ISOLATION	88
R3A1	resn	64
R3B1	RESN	88
R3B2	RESN	88
R3B3	resn	88
R3B4	RESN	88
R3B5	RESN	88
R3C1	RESN	7
R3C2	RESN	7
R3D1	RESN	97
R3D2	RESN	7
R3E1	RESN	13
R3E2	RESN	13
R3E4	RESN	13
R3E5	RESN	13
R3E6	RESN	13
R3E7	RESN	13
R3G1	RESN	23
R3G2	RESN	23
R3G3	RESN	23
R3G4	RESN	23
R3G5	RESN	24
R3H1	RESN	19
R3H2	RESN	18
R3H3	RESN	18
R3H5	RESN	78
R3H7	RESN	78
R3H8	resn	78
R3H9	resn	78
R3H10	resn	78
R3H11	resn	78
R3R1	RESN	97
R3R2	RESN	97
R3R3	RESN	97
R4A1	resn	83
R4A2	RESN	88
R4B2	RESN	33
R4B3	RESN	33
R4B4	RESN	33
R4B5	RESN	33
R4B6	RESN	88
R4B7	RESN	88
R4B8	RESN	88
R4B9	RESN	88
R4B10	RESN	88
R4B11	RESN	95
R4B12	RESN	88
R4B13	RESN	95
R4C2	RESN	13
R4C4	RESN	13
R4C5	RESN	13
R4C6	RESN	13
R4C7	RESN	13
R4C9	RESN	13
R4C11	RESN	13
R4E2	RESN	13
R4E3	RESN	13
R4E4	RESN	13
R4E5	RESN	13
R4E6	RESN	13
R4E7	RESN	13
R4E8	RESN	13
R4H1	RESN	32
R4H2	RESN	32
R5A1	RESN	54
R5A2	RESN	46
R5A3	RESN	46
R5A4	RESN	46
R5A5	NRES	47
R5A6	NRES	47
R5A7	resn	72
R5A8	resn	72
R5B1	RESN	47
R5B2	RESN	7
R5B3	resn	72
R5B4	resn	72
R5B6	RESN	96
R5B7	RESN	14
R5B8	RESN	14
R5B9	RESN	14
R5B10	RESN	96
R5B11	RESN	14
R5B12	RESN	14
R5B13	RESN	14
R5B15	RESN	14

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```
R5B16 RESN   14      R6B2  RESN   46      R6J7  RESN   95      R8A8  RESN   50
R5B17 RESN   14      R6B3  NRES   46      R6J8  resn   75      R8A9  resn   51
R5B18 RESN   14      R6B4  NRES   46      R7A1  resn   52      R8A10 resn   51
R5B19 RESN   14      R6B5  NRES   46      R7A2  resn   52      R8A11 resn   51
R5B20 RESN   14      R6B6  RESN   44      R7A3  RESN   55      R8A12 RESN   50
R5B21 RESN   14      R6B7  NRES   46      R7A4  RESN   55      R8A13 RESN   50
R5B22 RESN   14      R6B8  RESN   46      R7A5  RESN   55      R8A14 resn   51
R5B23 RESN   14      R6B9  RESN   14      R7A6  resn   48      R8A15 resn   51
R5B24 RESN   14      R6B10 RESN   14      R7A7  RESN   55      R8A16 resn   51
R5B25 RESN   14      R6B12 RESN   14      R7A8  RESN   55      R8A17 RESN   51
R5B26 RESN   14      R6C1  RESN   14      R7A9  RESN   55      R8A18 resn   51
R5B27 RESN   14      R6C2  RESN   14      R7A10 RESN   55      R8A19 resn   51
R5B28 RESN   14      R6C3  RESN   14      R7A11 RESN   55      R8A20 resn   51
R5B29 RESN   14      R6C4  RESN   14      R7A12 RESN   55      R8A21 resn   52
R5B30 RESN   14      R6D1  RESN   41      R7A13 resn   48      R8A22 resn   51
R5C1  RESN   14      R6D2  RESN   15      R7A14 RESN   55      R8A23 resn   51
R5C3  RESN   14      R6D3  RESN   86      R7B1  RESN   55      R8A24 RESN   51
R5C4  RESN   14      R6E1  RESN   86      R7B2  RESN   55      R8A25 resn   52
R5C5  RESN   13      R6E2  RESN   86      R7B3  RESN   55      R8A28 resn   52
R5C6  RESN   13      R6E4  RESN   13      R7B4  RESN   55      R8A29 RESN   51
R5C7  RESN   13      R6E6  RESN   13      R7E7  RESN   42      R8A30 resn   51
R5D1  RESN   13      R6E7  RESN   13      R7E8  RESN   42      R8B1  resn   48
R5D2  RESN   13      R6F1  RESN   87      R7E9  RESN   42      R8B2  resn   48
R5D3  RESN   13      R6F2  RESN   87      R7E10 RESN   42      R8B3  resn   48
R5D4  RESN   13      R6F3  resn   30      R7E11 resn   34      R8B4  resn   48
R5D5  RESN   86      R6F4  resn   30      R7E12 RESN   34      R8B8  resn   48
R5D6  RESN   86      R6G1  resn   82      R7E13 RESN   42      R8B9  resn   48
R5E1  RESN   13      R6G2  RESN   30      R7E14 resn   34      R8B10 resn   48
R5E3  RESN   13      R6G3  resn   83      R7F1  RESN   42      R8B12 resn   48
R5E4  RESN   13      R6G4  RESN   30      R7F2  RESN   46      R8B13 resn   48
R5E5  RESN   13      R6G5  RESN   30      R7F3  resn   35      R8C1  RESN   42
R5E6  RESN   13      R6G6  RESN   29      R7F4  resn   35      R8C2  RESN   42
R5E7  RESN   13      R6G7  RESN   30      R7F5  resn   35      R8F1  RESN   58
R5F1  RESN   13      R6G8  RESN   30      R7G1  RESN   35      R8F2  RESN   58
R5F2  RESN   13      R6G9  RESN   30      R7G2  RESN   35      R8G1  RESN   84
R5G1  RESN   7       R6G10 RESN   30      R7G3  RESN   35      R8G2  RESN   60
R5G2  RESN   7       R6G11 RESN   30      R7G4  RESN   35      R8G3  RESN   84
R5H1  RESN   96      R6G12 RESN   30      R7G5  RESN   41      R8H1  RESN   30
R5H2  RESN   97      R6G13 RESN   30      R7G6  RESN   30      R8H2  RESN   30
R5H3  RESN   95      R6G14 RESN   30      R7G7  RESN   30      R8H3  RESN   30
R5J1  RESN   95      R6G15 RESN   30      R7G8  RESN   30      R8H4  resn   81
R5J2  RESN   32      R6G16 RESN   65      R7G9  resn   30      R8H5  RESN   69
R5J4  RESN   32      R6G17 RESN   30      R7H1  RESN   30      R8H6  RESN   30
R6A1  RESN   55      R6G19 RESN   30      R7H2  RESN   30      R8H7  RESN   69
R6A2  RESN   44      R6G20 RESN   79      R7H3  RESN   27      R8H8  resn   74
R6A3  RESN   46      R6G22 RESN   30      R7H4  RESN   30      R8H9  resn   74
R6A4  RESN   44      R6G23 RESN   79      R7H5  RESN   27      R8H10 RESN   58
R6A5  RESN   46      R6H1  RESN   79      R7H6  RESN   30      R8J1  resn   74
R6A6  RESN   44      R6H2  RESN   30      R7H7  RESN   27      R8J2  resn   74
R6A7  RESN   44      R6H4  RESN   79      R7H8  RESN   30      R8J3  RESN   99
R6A8  RESN   44      R6H5  RESN   79      R7H9  RESN   32      R8J4  RESN   99
R6A9  RESN   44      R6H7  RESN   32      R7H10 RESN   32      R8J5  RESN   99
R6A10 RESN   46      R6H8  RESN   32      R7H11 RESN   66      R8J6  RESN   99
R6A11 RESN   44      R6H9  RESN   79      R7H12 RESN   30      R8J7  RESN   70
R6A12 RESN   44      R6H11 RESN   6       R7H13 RESN   95      R8J8  RESN   70
R6A13 RESN   46      R6H12 RESN   95      R7H14 RESN   66      R8J9  RESN   95
R6A14 RESN   44      R6H13 RESN   95      R7H15 RESN   66      R9A1  resn   52
R6A15 NRES   47      R6H14 RESN   95      R7H16 RESN   66      R9A4  resn   48
R6A16 RESN   55      R6H15 RESN   95      R7J1  RESN   66      R9A9  resn   52
R6A17 NRES   47      R6H16 RESN   97      R7J2  RESN   66      R9B2  RESN   48
R6A18 RESN   44      R6H17 RESN   66      R7J3  RESN   66      R9B4  RESN   54
R6A19 NRES   47      R6H19 RESN   97      R7J4  RESN   66      R9C1  RESN   95
R6A20 NRES   47      R6H20 RESN   56      R7J5  RESN   70      R9C2  RESN   42
R6A21 RESN   45      R6H21 RESN   96      R7J6  RESN   98      R9C3  resn   43
R6A22 NRES   47      R6J1  RESN   97      R8A1  RESN   54      R9C4  resn   43
R6A23 RESN   44      R6J2  RESN   56      R8A3  RESN   51      R9C5  resn   43
R6A24 NRES   47      R6J3  RESN   97      R8A4  resn   51      R9C6  resn   43
R6A25 NRES   47      R6J4  RESN   97      R8A5  resn   51      R9C7  resn   43
R6A26 NRES   47      R6J5  RESN   97      R8A6  resn   52      R9C8  resn   43
R6B1  RESN   55      R6J6  RESN   95      R8A7  RESN   50      R9C9  resn   43
```

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Column 1

```
R9C10 resn      43
R9C11 resn      43
R9C12 resn      43
R9D1  resn      34
R9D2  resn      34
R9E1  RESN      58
R9E2  RESN      58
R9E4  RESN      58
R9E5  RESN      58
R9E6  RESN      57
R9E7  RESN      57
R9E8  RESN      57
R9F1  RESN      57
R9F2  RESN      57
R9F3  RESN      57
R9F4  RESN      57
R9F5  RESN      57
R9F6  RESN      57
R9F7  RESN      57
R9F8  RESN      57
R9F9  RESN      57
R9F10 RESN      57
R9F11 RESN      57
R9F12 RESN      57
R9F13 RESN      58
R9F14 RESN      58
R9F15 RESN      58
R9G1  RESN      59
R9G2  RESN      59
R9H1  RESN      60
R9H2  resn      72
R9H3  resn      72
R9H4  RESN      60
R9H5  resn      72
R9H6  resn      72
R9H7  RESN      60
R9H8  RESN      98
R9H9  RESN      98
R9J1  RESN      96
RM6C1 AGP_RM    15
RP1A1 RPAK4C-4R 82
RP1A2 RPAK4C-4R 63
RP1C1 RPAK4C-4R 7
RP1D1 RPAK4C-4R 7
RP1D2 RPAK4C-4R 7
RP1E1 RPAK4C-4R 6
RP1G1 RPAK4C-4R 23 24
RP1G2 RPAK4C-4R 23
RP1G3 RPAK4C-4R 23
RP1H1 RPAK4C-4R 18 19
RP1H2 RPAK4C-4R 18
RP1H3 RPAK4C-4R 67
RP1J1 RPAK4C-4R 62
RP1J2 RPAK4C-4R 67
RP1J3 RPAK4C-4R 61
RP1J4 RPAK4C-4R 67
RP2G1 RPAK4C-4R 23 24
RP2G2 RPAK4C-4R 23
RP2G3 RPAK4C-4R 23 24
RP2G4 RPAK4C-4R 23
RP2G5 RPAK4C-4R 18 23
RP2G6 RPAK4C-4R 23 24
RP2G7 RPAK4C-4R 18 19 23 24
RP2G8 RPAK4C-4R 18 19
RP2H1 RPAK4C-4R 18 19
RP2H2 RPAK4C-4R 18
RP2H3 RPAK4C-4R 18 23
RP2H4 RPAK4C-4R 18 19
RP2H5 RPAK4C-4R 18
RP2H6 RPAK4C-4R 19 24
```

Column 2

```
RP2H7 RPAK4C-4R 18 19
RP2H8 RPAK4C-4R 18
RP3A1 RPAK4C-4R 64
RP3A2 RPAK4C-4R 64
RP3A3 RPAK4C-4R 64
RP3C1 RPAK4C-4R 7
RP3D1 RPAK4C-4R 7
RP3G1 RPAK4C-4R 23 24
RP3G2 RPAK4C-4R 19 24
RP3G3 RPAK4C-4R 18 23
RP3G4 RPAK4C-4R 23 24
RP3G5 RPAK4C-4R 23
RP3G6 RPAK4C-4R 23
RP3H1 RPAK4C-4R 18 19
RP3H2 RPAK4C-4R 18
RP3H3 RPAK4C-4R 18 19
RP3H4 RPAK4C-4R 18
RP3H5 RPAK4C-4R 18
RP3H6 RPAK4C-4R 18 23
RP3H7 RPAK4C-4R 18 23
RP4A1 RPAK4C-4R 64
RP4A2 RPAK4C-4R 64
RP4G1 RPAK4C-4R 23 24
RP4G2 RPAK4C-4R 23 24
RP4G3 RPAK4C-4R 23
RP4G4 RPAK4C-4R 23
RP4G5 RPAK4C-4R 23
RP4G6 RPAK4C-4R 23
RP4G7 RPAK4C-4R 23 24
RP4G8 RPAK4C-4R 19 24
RP4H1 RPAK4C-4R 18
RP4H2 RPAK4C-4R 18 19
RP4H3 RPAK4C-4R 18
RP4H4 RPAK4C-4R 18 19
RP4H5 RPAK4C-4R 19 24
RP4H6 RPAK4C-4R 19 24
RP4H7 RPAK4C-4R 18
RP4H8 RPAK4C-4R 18
RP5B1 RPAK4C-4R 14
RP5B2 RPAK4C-4R 14
RP5C1 RPAK4C-4R 14
RP5G1 RPAK4C-4R 23
RP5H1 RPAK4C-4R 18
RP5H2 RPAK4C-4R 18 19
RP6B1 RPAK4C-4R 14
RP6C1 RPAK4C-4R 14
RP6D1 RPAK4C-4R 41
RP6D2 RPAK4C-4R 41
RP6D3 RPAK4C-4R 41
RP7E1 RPAK4C-4R 38 39 40
RP7F1 RPAK4C-4R 31
RP7F2 RPAK4C-4R 31
RP7F3 RPAK4C-4R 46
RP7F4 RPAK4C-4R 46
RP7H1 RPAK4C-4R 30
RP7J1 RPAK4C-4R 66
RP8B1 RPAK4C-4R 50
RP8B2 RPAK4C-4R 50
RP8B3 RPAK4C-4R 50
RP8C1 RPAK4C-4R 41
RP8C2 RPAK4C-4R 41
RP8E1 RPAK4C-4R 36 37
RP8F1 RPAK4C-4R 46
RP8F2 RPAK4C-4R 31
RP8G1 RPAK4C-4R 41
RP8G2 RPAK4C-4R 41
RP9A1 RPAK4C-4R 81
RP9B1 RPAK4C-4R 81
RP9D1 RPAK4C-4R 81
RP9D2 RPAK4C-4R 81
```

Column 3

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RP9G1 RPAK4C-4R 58
RP9H1 RPAK4C-4R 99
RP9J1 RPAK4C-4R 99
RP9J2 RPAK4C-4R 99
RP9J3 RPAK4C-4R 99
RT1D1 THERMISTOR 57
RT2A1 THERMISTOR 82
RT4A1 THERMISTOR 83
RT9D1 THERMISTOR 34
RT9E1 THERMISTOR 57
RT9F1 THERMISTOR 57
U1C1  MICS258    87
U1E1  HECETA4    68
U1E2  HECETA6    68
U1G1  GD75232S   65
U1H1  PORT_ANGELES 61 67
U2B1  SC1205     88
U3B1  SC1205     88
U3B2  SC1205     88
U3H1  TPPM0115   78
U4B1  ADP3163    88
U4H1  MICS219BMM 78
U5B1  CK_408     14
U5C1  GRANITEBAY 9 10 11 12
U5E1  LM358      86
U6A1  KENAI32    44 45
U6A2  LM4871     55
U6B1  AT93C66    46
U6F1  IRU1150    87
U6H1  LM358      79
U6J1  74AS1034A  95
U6J2  AT97SC3201 56
U7A1  LF353      55
U7F1  EPM7032_3P3 42
U7F2  AT93C46A_66 46
U7G1  ICH4       26 27 28 29
U7J1  FWH_4M     66
U8A1  LF353      51
U8A2  STAC9766   48
U8F1  TESTTSB43AB23 58
U8F2  VREGEZ1086 84
U8G1  LM317L     84
U8G2  CMD_SATA   60
U8H1  74ACT04    74
U8J1  74LVC74    99
U9A1  78M05C     54
U9G1  MC33269    59
U9H1  AT24C32_64 58
U9J1  EPM7032    99
XBT7J1 BATT_HLDR_2PIN 81
XY7H1 XTAL_HLDR 30
Y5B1  CRYSTAL    14
Y6B1  CRYSTAL    46
Y6J1  XTAL4P     56
Y7H2  XTAL4P     30
Y8H1  CRYSTAL    60
Y9B1  CRYSTAL    48
Y9F1  CRYSTAL    58
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