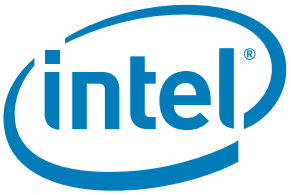
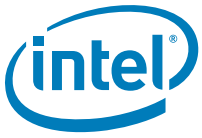


Intel® C102/C104 Scalable Memory Buffer

Thermal/Mechanical Specification and Design Guidelines

February 2014

Reference Number: 329788-001



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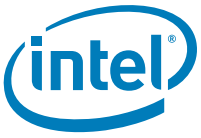
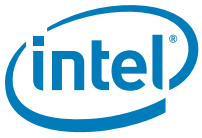


Figures

Tables



Revision History

Document Number	Description	Date
329788-001	• Initial release of the document.	February 2014

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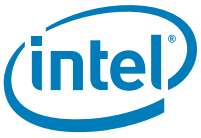


1 Introduction

This document addresses thermal design and specifications of the Intel® C102/C014 Scalable Memory Buffer. Information provided in this document is intended only for use with these products. Unless otherwise specified, specification and guidance provided in this document applies only to these products. In this document the term ‘memory buffer’ refers to Intel C102/C104 Scalable Memory Buffer, unless otherwise identified.

The goals of this document are to:

- Outline the thermal and mechanical operating limits and specifications for the Intel C102/C104 Scalable Memory Buffer.
- Describe reference thermal solutions that meet the specifications of the Intel C102/C104 Scalable Memory Buffer.

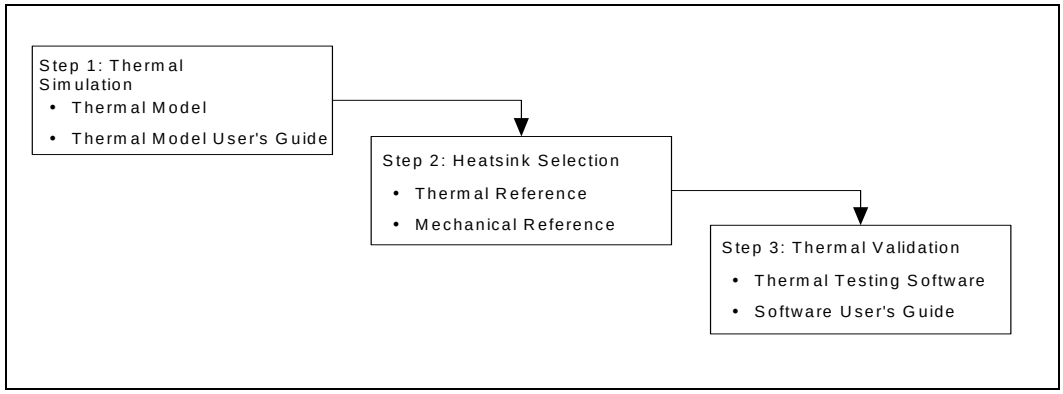
Properly designed thermal solutions provide adequate cooling to maintain the component die temperature within its thermal specifications. This is accomplished by providing a low local-ambient temperature, ensuring adequate local airflow, and minimizing the die to local-ambient thermal resistance. By maintaining the memory buffer component die temperature at or below the specified limits, a system designer can ensure the proper functionality, performance, and reliability of the component. Operation outside the functional limits of the component is not supported and can cause loss of data integrity. Operation outside the damage limit can cause permanent, non-recoverable damage to the component.

The simplest and most cost-effective method to improve the inherent system cooling characteristics is through careful chassis design and placement of fans, vents, and ducts. When additional cooling is required, component thermal solutions may be implemented in conjunction with system thermal solutions. The size of the fan or heatsink can be varied to balance size and space constraints with acoustic noise.

1.1 Design Flow

To develop a reliable, cost-effective thermal solution, several tools have been provided to the system designer. Figure 1-1 illustrates the design process implicit to this document and the tools appropriate for each step.

Figure 1-1. Thermal Design Process



1.2 Definition of Terms

Table 1-1. Definition of Terms

Term	Definition
BLT	Bond Line Thickness. Final settled thickness of the thermal interface material after installation of heatsink.
FC-BGA	Flip Chip Ball Grid Array. A package type defined by a plastic substrate where a die is mounted using an underfill C4 (Controlled Collapse Chip Connection) attach style. The primary electrical interface is an array of solder balls attached to the substrate opposite the die. Note that the device arrives at the customer with solder balls attached.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.
Intel® SMI 2	Intel® Scalable Memory Interconnect 2.
T_{case_max}	Maximum die operating temperature, as measured at the geometric center of the top of the die.
T_{case_min}	Minimum die operating temperature, as measured at the geometric center of the top of the die.
TDP	Thermal Design Power: Thermal solutions should be designed to dissipate this target power level. TDP is not the maximum power that the chipset can dissipate.
T_{SENSOR}	Die temperature as reported by the device digital thermal sensor (DTS).

1.3 Reference Documents

The reader of this specification should also be familiar with material and concepts presented in the following documents:

Title	Document Number
Intel® C102/C104 Scalable Memory Buffer Datasheet	330032-001

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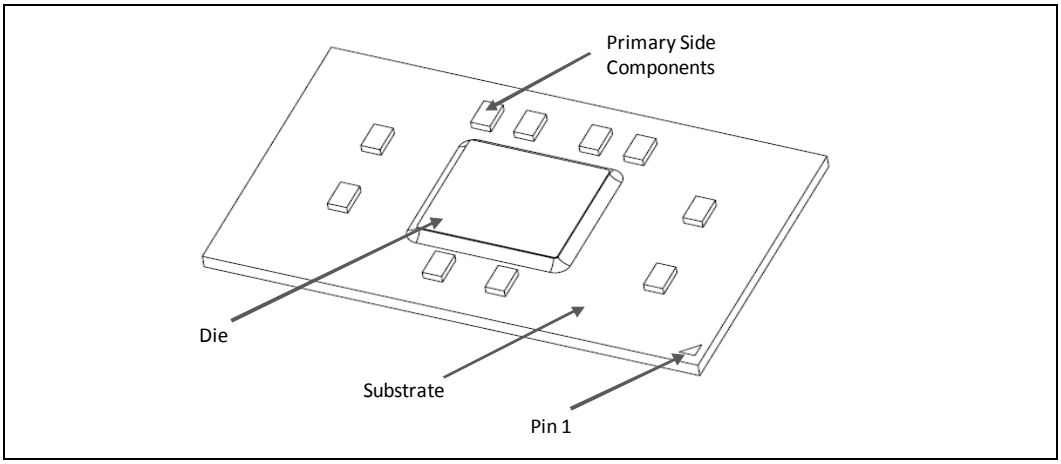
2 Packaging Technology

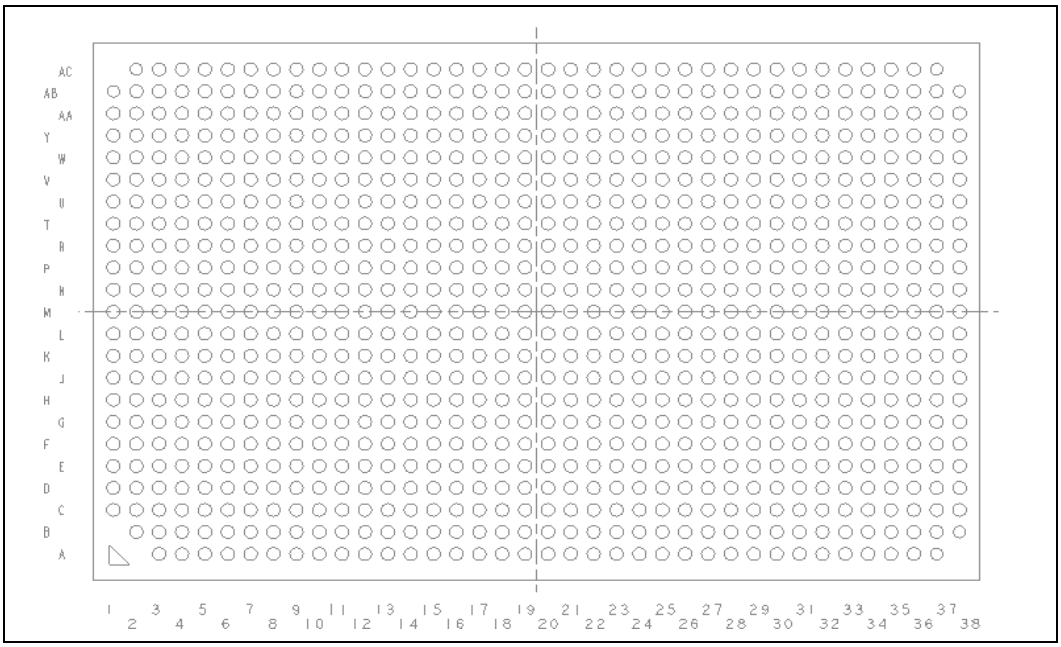
Intel C102/C014 Scalable Memory Buffer is a bare die component, surface mounted on FCBGA package form factor (see Figure 2-1 through Figure 2-2) with a total of 868 lead-free solder balls in a grid array of 0.8 mm pitch on a 31 mm x 19.5 mm package body. Additional package attributes can be found in the package mechanical drawing provided in the appendix.

Figure 2-1. Package Primary Side - Iso View (Top View)



Note: Primary side components location, size, and quantity are shown for illustration purposes only. See package mechanical drawing for details and guidance.

Figure 2-2. Package Secondary Side - BGA Pattern (Bottom View)



Notes:
1. All dimensions are in millimeters.
2. All dimensions are tolerances confirm to ANSI Y14.5M-1994.

2.1 Package Mechanical Requirements

The component package has an exposed bare die which is NOT capable of sustaining a dynamic or static compressive load applied to any edge of the bare die. Mechanical load limits must not be exceeded during heatsink installation, mechanical stress testing, standard shipping conditions, and/or any other use condition.

Table 2-1. Package Mechanical Load Specifications

Parameter	Value	Notes
Maximum Allowable Static Normal Load	66.7 N [15 lbf]	1, 2, 3
Maximum Transient Compressive Package Load	111 N [25 lbf]	2, 3
Maximum Dynamic Compressive Package Load	164.6 N [37 lbf]	4, 5
Max allowable Strain Limit at BGA	400 ue	6

Notes:
1. The heatsink attach solutions must not include continuous stress onto the package with the exception of a uniform load to maintain the heatsink-to-package thermal interface.
2. These specifications apply to uniform compressive loading in a direction perpendicular to the bare die top surface.
3. These specifications are based on limited testing for design characterization. Loading limits are for the package only.
4. Dynamic compressive load applies to all board thicknesses.
5. Dynamic load is defined as an 11ms duration average load superimposed on the static load requirement.
6. Specification applies to 0.093” and 0.130” thick boards.

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3 Thermal Specifications

3.1 Thermal Design Power (TDP)

Analysis indicates that real applications are unlikely to cause the component to consume maximum power dissipation for sustained time periods. Therefore, in order to arrive at a more realistic power level for thermal design purposes, Intel characterizes power consumption based on known platform benchmark applications. The resulting power consumption is referred to as the Thermal Design Power (TDP). Hence, TDP is the design target for the thermal solution. TDP is not the maximum power that the memory buffer can dissipate. For TDP specifications, see Table 3-1.

FCBGA packages have poor heat transfer capability into the board and have minimal thermal capability without a thermal solution. Intel recommends that system designers plan for a heatsink when using Intel C102/C104 Scalable Memory Buffer.

3.2 Die Temperature

To ensure proper operation and reliability of the memory buffer, die temperature must be kept within the thermal specifications provided in Table 3-2. System and/or component level thermal solutions are required to maintain these temperature specifications.

3.2.1 Case Temperature

Tcase_max is provided for the purpose of designing a memory buffer thermal solution. Refer to Chapter 4, “Thermal Metrology,” for guidelines on accurately measuring package die temperatures. Maintaining the memory buffer case temperature at or below the Tcase_max ensures the component is operating within its functional limits.

3.2.2 Thermal Sensor

The Intel C102/C104 Scalable Memory Buffer uses a thermal sensing device on the die to monitor its temperature status in real-time. The thermal sensor output, T_{SENSOR} is in degrees Celsius, and is available over PECI through the Intel® Management Engine (Intel® ME). This enables system thermal management to monitor and to implement policies such as fan speed control to maintain the die temperature within its operation and reliability temperatures. Die temperature is also compared with the memory buffer thermal trip setpoint.

Platform compatible processors will monitor the memory buffer temperature via integrated iMC on the processor (host). Memory buffer is at its maximum operating temperature when TEMP_MID setpoint is reached. Memory buffer thermal thresholds on the processor enable the processor to implement policies in response to the changes in the die temperature.

3.2.3 Thermal Thresholds

Intel C102/C104 Scalable Memory Buffer thermal setpoints, described in Table 3-2, are programmed in the host memory controller. If enabled, the host upon reaching these thermal conditions will initiate memory throttling resulting in reduction of memory bandwidth and hence power.

TEMP_MID: Is a T_{SENSOR} based setpoint which is never to be exceeded while under any load to ensure functionality when using the sensor-based limiting specification. TEMP_MID is programmed in the processor at boot time. Additional margin, meaning lower than specified TEMP_MID value, can be programed if so desired in reducing occurrence of memory throttling.

TEMP_HI: Is a T_{SENSOR} based setpoint which is never to be exceeded while under any load to prevent damage to the component. TEMP_HI is programmed in the processor at boot time. Additional margin, meaning lower than specified TEMP_HI but greater than TEMP_MID value, can be programed to prevent damage to the component which may result from operating at higher temperature.

Table 3-1. Thermal Thresholds

Thresholds	Description	Action
TEMP_MID	T_{SENSOR} approaching functional limit	Initiate THRT_HI on connected DIMMs, reactive fan speed control, (SMI and/or MEMHOT#)
TEMP_HI	T_{SENSOR} approaching damage limit	Initiate THRT_CRIT on connected DIMMs, (SMI and/or MEMHOT#)

Note: MEMHOT# is configured and asserted with either (TEMP_MID or TEMP_HI) threshold crossing.

3.2.4 $T_{CONTROL}$

$T_{CONTROL}$ is the temperature limit which must be maintained to ensure the component operates reliably over its expected life. $T_{CONTROL}$ is a thermal monitoring setpoint which is specified based on the thermal sensor output in degrees Celsius. Its value must be compared against the thermal sensor reading. The value of the $T_{CONTROL}$ threshold is specified in Table 3-2. $T_{CONTROL}$ value applies to the full range of the memory buffer operating power. Note that no internal response is generated by the memory buffer at $T_{CONTROL}$. Long term operation above the $T_{CONTROL}$ temperature set point reduce the life of the product.

A server thermal management controller can monitor the memory buffer temperature, and use the $T_{CONTROL}$ value as the threshold at which active system thermal management can be engaged. This will ensure reliable memory buffer operation over its expected life. In the cases where maximum fan speed is reached and T_{SENSOR} cannot be maintained at or below the $T_{CONTROL}$ value, the T_{SENSOR} must still be maintained to be less than or equal to TEMP_MID.

A server thermal management controller can monitor the memory buffer temperature, and use the $T_{CONTROL}$ value as the threshold at which active system thermal management can be engaged. This will ensure reliable memory buffer operation over its expected life. In the cases where maximum fan speed is reached and T_{SENSOR} cannot be maintained at or below the $T_{CONTROL}$ value, the T_{SENSOR} must still be maintained to be less than or equal to TEMP_MID if the thermal sensor specification is used.

3.2.5 Thermal Trip

Once the thermal sensing device observes that the temperature of the die, T_{SENSOR}, has reached it catastrophic limit, the memory buffer will initiate shutdown. See 'Catastrophic Overtemp' error condition described in *Intel® C102 and C104 Scalable Memory Buffer Datasheet.*

3.2.6 Thermal Monitoring and Response

When

- $T_{SENSOR} < T_{CONTROL}$, the system can run under any desired conditions.
- $T_{SENSOR} = T_{CONTROL}$, $T_{CONTROL}$ limit attained, system must increase fan speed until $T_{CONTROL}$ limit can no longer be maintained.
- $T_{SENSOR} > T_{CONTROL}$, fan speed increase is required to maintain Tcase_max or Tsensor remain below TEMP_MID.
- T_{SENSOR}=TEMP_MID, processor will issue MEMHOT# or SMI if so configured.
- T_{SENSOR}=TEMP_HI, processor will issue MEMHOt# or SMI if so configured.

3.3 Thermal Specifications

Table 3-2. Thermal Specification

Parameter	Value	Notes
TDP	9 W	1,3,5
Idle Power	2.8 W	1,3,5,6
TEMP_MID	92 °C	1,2,3
TEMP_HI	105 °C	1,2,3
Tcase_max	92 °C	1,3, 4
Tcase_min	5 °C	1,3
Tcontrol	87 °C	1,2,3

Notes:
1. Refer to the *Intel® C102/C104 Scalable Memory Buffer* Datasheet for thermal management mechanism,
2. Temperature value is based on thermal sensor output.
3. These specifications are based on preliminary measurement and subject to change.
4. Designing to a lower T_{CASE} target will minimize the occurrences of memory throttling as a result of memory buffer over temp.
5. TDP value for the memory buffers is based on loading Quad Rank, three DIMM per Channel per Intel C102/C104 Scalable Memory Buffer.
6. Intel C102/C104 Scalable Memory Buffer idle power assumption is with the processor C3E power saving mode enabled.

Dual thermal specifications based on T_{CASE} and Digital Thermal Sensor enables the thermal solution designer to optimize the component thermal solution and the system thermal management in a way that is best suited for the integration of the memory buffer thermal management. Systems not utilizing thermal threshold must ensure compliance with T_{CASE} specifications. Equation provides a conversion between Tsensor and T_{CASE} at the memory buffer maximum operating temperature.

Equation 3-1.

T_{SENSOR} = (T_{CASE} ± 5) at T_{CASE} ranges of 87 °C to Tcase_max @ TDP

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4 Thermal Metrology

The system designer must make temperature measurements to accurately determine the thermal performance of the system. Intel has established guidelines for proper techniques to measure the component die temperatures. Section 4.1 provides guidelines on how to accurately measure the component die temperatures. Section 4.2 contains information on running an application program that will emulate anticipated maximum thermal design power.

4.1 Die Temperature Measurements

To ensure functionality and reliability, the chipset component T_{case} must be maintained at or between the maximum/minimum operating range of the temperature specification as noted in Table 3-2. The surface temperature at the geometric center of the die corresponds to T_{case}. Measuring T_{case} requires special care to ensure an accurate temperature measurement.

Temperature differences between the temperature of a surface and the surrounding local ambient air can introduce errors in the measurements. The measurement errors could be due to a poor thermal contact between the thermocouple junction and the surface of the package, heat loss by radiation and/or convection, conduction through thermocouple leads, and/or contact between the thermocouple cement and the heatsink base (if a heatsink is used). For maximum measurement accuracy, only the 0° thermocouple attach approach is recommended.

4.2 Zero Degree Angle Attach Methodology

1. Mill a 3.3 mm (0.13 in.) diameter and 1.5 mm (0.06 in.) deep hole centered on the bottom of the heatsink base.
2. Mill a 1.3 mm (0.05 in.) wide and 0.5 mm (0.02 in.) deep slot from the centered hole to one edge of the heatsink. The slot should be parallel to the heatsink fins (see Figure 4-2).
3. Attach thermal interface material (TIM) to the bottom of the heatsink base.
4. Cut out portions of the TIM to make room for the thermocouple wire and bead. The cutouts should match the slot and hole milled into the heatsink base.
5. Attach a 36 gauge or smaller calibrated K-type thermocouple bead or junction to the center of the top surface of the die using a high thermal conductivity cement. During this step, ensure no contact is present between the thermocouple cement and the heatsink base because any contact will affect the thermocouple reading. **It is critical that the thermocouple bead makes contact with the die** (see Figure 4-3).
6. Attach heatsink assembly to the component and route thermocouple wires out through the milled slot.

Figure 4-1. Thermal Solution Decision Flowchart

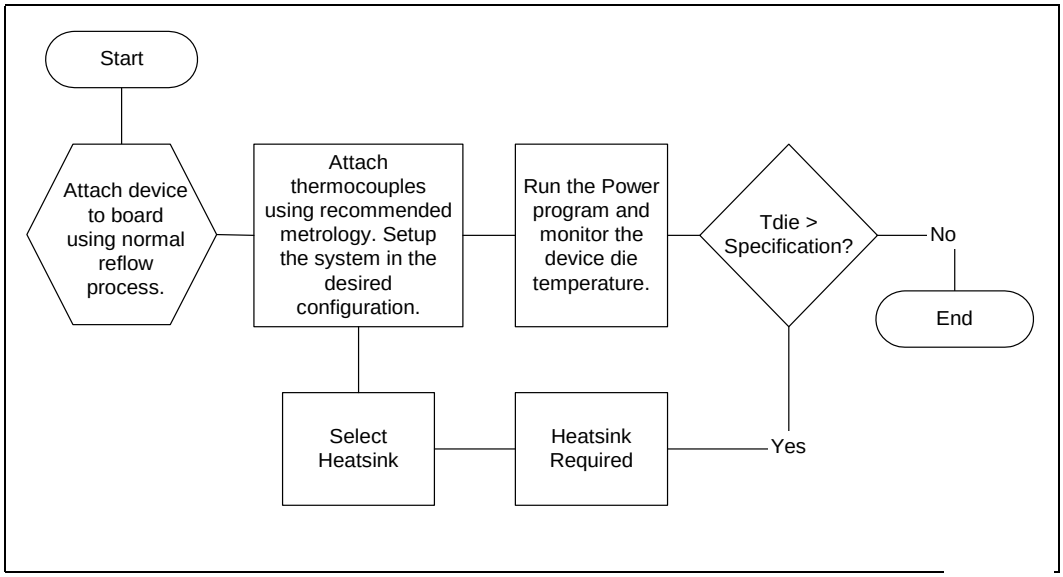
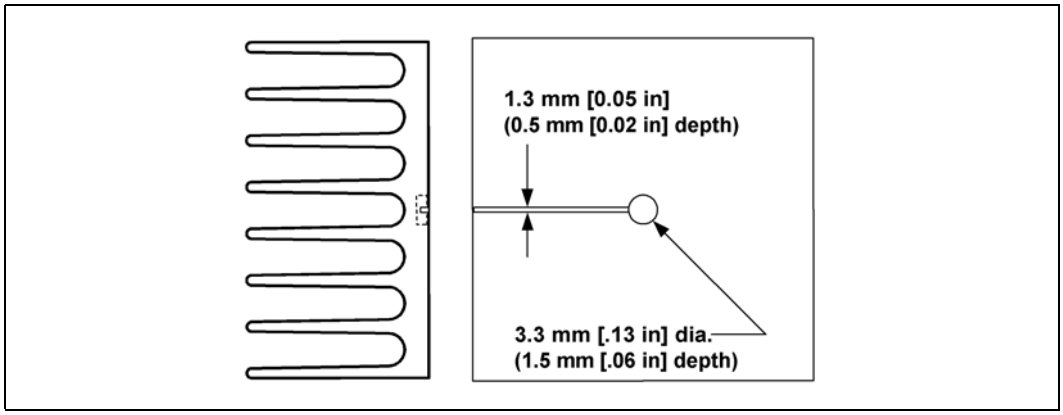
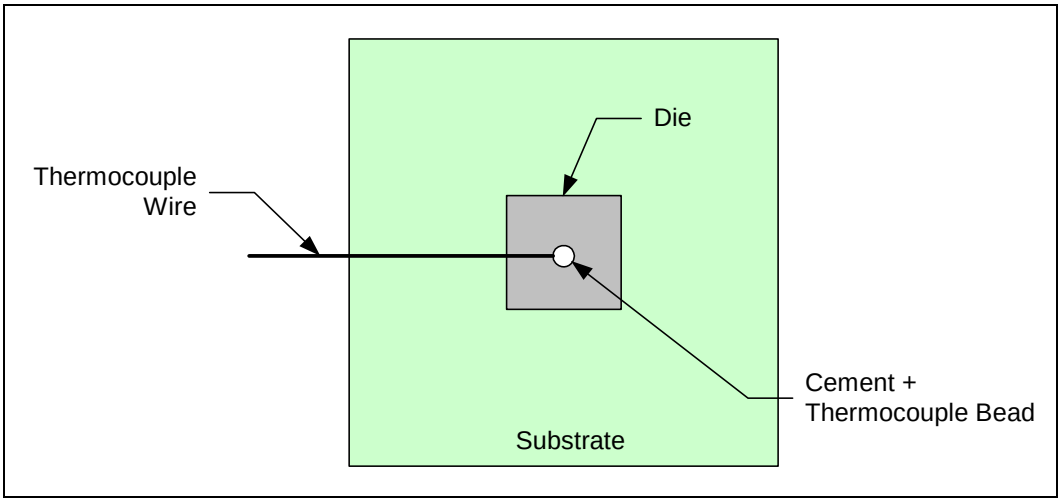


Figure 4-2. Zero Degree Angle Attach Heatsink Modifications



Note: Not to scale.

Figure 4-3. Zero Degree Angle Attach Methodology (Top View)



Note: Not to scale.

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5 Design Considerations

When designing a thermally capable system, all critical components must be simultaneously considered. The responsible engineer must determine how each component will affect another, while ensuring target performance for all components. The system design team must set these target performance goals during the design phase so that they can be achieved with the selected component layout.

The location of components and their interaction must be considered during the layout phase. A poorly cooled memory subsystem will have worse performance. The thermal engineer's responsibility is to ensure that each and every component meets its performance goals bounded by thermal and acoustic specifications but also computing performance such as memory throughput.

To develop a reliable and cost-effective thermal solution, thermal characterization and simulation should be carried out at the entire system level, accounting for the thermal requirements of each component. In addition, acoustic noise constraints may limit the size, number, placement, and types of air-movers that can be used in a particular design.

5.1 Operating Environment

The reference thermal solution design assumes both a max fan speed condition and an acoustic fan speed condition. The thermal designer must carefully select the location to measure airflow to obtain an accurate estimate. Table 6-1 provides environmental boundary conditions that are applied in defining and designing the memory buffer compatible cooling solution.

5.2 Heatsink Performance

5.2.1 Altitude Correction

The *simulated* thermal performance of a thermal solution will vary with varying the approach air velocity. For data modeled at sea level a correction factor would be required to estimate thermal performance at other altitudes. The Equation 5-1 can be used to determine the heatsink performance based on the adjusted altitude.

Equation 5-1.Altitude Correction

$$\theta_{ca} = \alpha + \beta \times Q_{alt}^{-\Upsilon\left(\frac{\rho_{alt}}{\rho_o}\right)^{-\Upsilon}}$$

α, β and γ can be obtained from the heatsink thermal performance curve versus the approach air velocity such as the one shown in Figure 5-1.

Q - "velocity through heatsink fin area (m/s)". Velocity is the value on X axis of the heatsink thermal performance curve versus the approach air velocity.

ρ_{alt} - Air density at given altitude

ρ_0 - Air density at sea level

5.2.2 Effect of Pressure on TIM Performance

As mechanical pressure increases on the TIM, the thermal resistance of the TIM decreases. This phenomenon is due to the decrease of the bond line thickness (BLT). BLT is the final settled thickness of the thermal interface material after installation of the heatsink. The effect of pressure on the thermal resistance of the Honeywell PCM45 F* TIM is shown in Table 5-1.

Intel provides both End of Line and End of Life TIM thermal resistance values for Honeywell PCM45 F*, see Table 5-1. End of Line and End of Life TIM thermal resistance values are obtained through measurement on a Test Vehicle similar to the component's physical attributes using an extruded aluminum heatsink. The End of Line value represents the TIM performance post heatsink assembly while the End of Life value is the predicted TIM performance when the product and TIM reaches its end of life. The heatsink retention provides enough pressure for the TIM to achieve an End of Line thermal resistance.

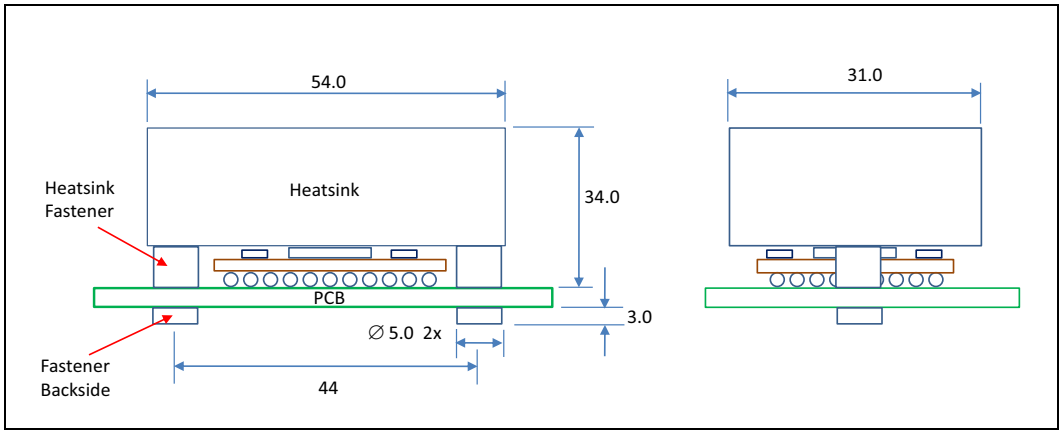
Table 5-1. Honeywell PCM45 F* TIM Performance as a Function of Attach Pressure

Pressure on Thermal Solution and Package Interface (PSI)	Thermal Resistance (°C × cm^2) / W	
	End of Line	End of Life
40	0.19	0.391

5.3 Mechanical Design Envelope

While each design may have unique mechanical volume and height restrictions or implementation requirements, the height, width, and depth constraints typically placed on the component thermal solution are shown in Figure 5-1. See PCB mechanical keep-out drawing in the appendix for additional details on components placed between the heatsink and the PCB when using heatsinks that extend beyond the memory buffer package envelope.

Figure 5-1. Heatsink Volumetric Envelope



Notes:
1. All Units in mm.
2. All heights shown are maximum values.
3. See package drawing for the package overall height pre and post SMT.
4. See PCB Mechanical Keep-out drawing for additional details.

5.4 PCB Design Consideration

5.4.1 Board-Level Components Keepout Dimensions

The location of hole patterns and keepout zones for the reference thermal solution are shown in Figure B-3. Note that additional keep-out may be necessary to address board assembly and rework process tool requirements.

5.4.2 Land Pattern Guidance

The land pattern guidance provided in this section applies to printed circuit board design. Recommendation for Printed Circuit Board (PCB) Land Patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase package reliability.

5.4.3 Pad Type Recommendations

Intel defines two types of pad types based on how they are constructed. A metal defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component.

In thermal cycling a MD pad has shown to be more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball / paste conforms to the window created by the solder mask.

For certain failure modes the MD pad may not be as robust in shock and vibration (S&V). During S&V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum but not to exceed the pad diameter and exit the pad at a 45 degree angle (parallel to the diagonal of the package). During board flexure that results from shock & vibration a SMD pad is less susceptible to a crack initiating due to the larger surface area.

Figure 5-2. Land Pattern (Top View of Board)

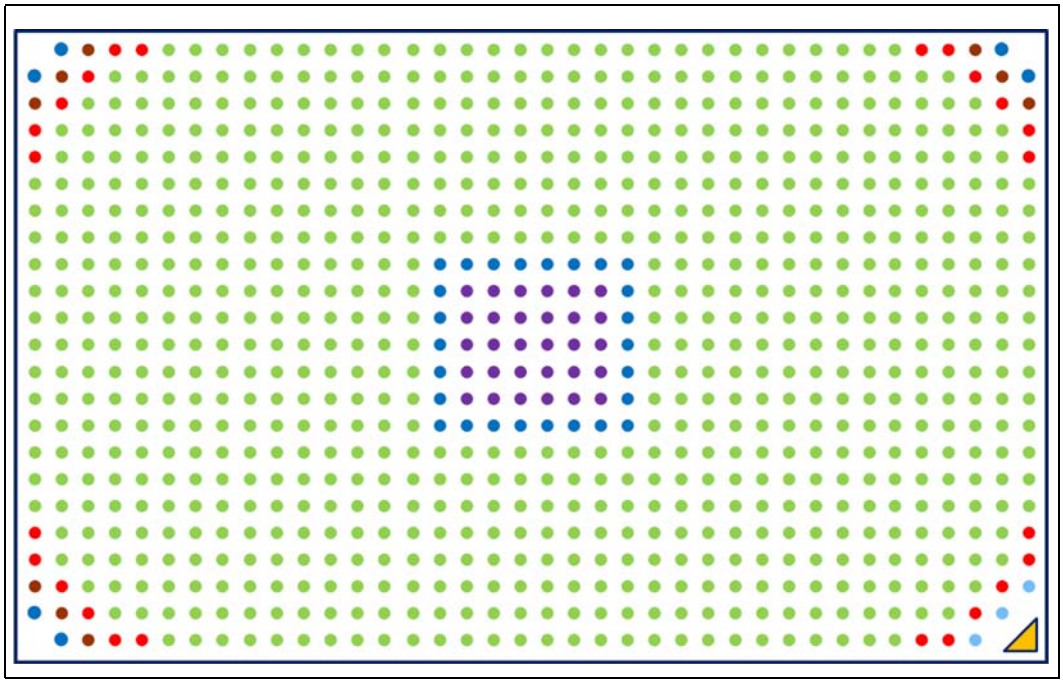


Table 5-2. Intel® C102/C104 Scalable Memory Buffer Land Pattern

Pad Type	Color Code	CTF/ NCTF	Pad Details	Pads
Solder Mask Defined		NCTF	•17 mil SRO / 23 mil pad	A37, B38 AB38, AC37 AB1, AC2
		NCTF	•15 mil	A3, B2, C1
Metal Defined with Wide Trace		NCTF	•15 mil pad w/ 14 mil wide trace at 45°	A36, B37, C38 AA38, AB37, AC36 AC3, AB2, AA1
		CTF	•15 mil pad w/ 10 mil wide trace	K17 - P22
		CTF	•15 mil pad, 4 and 10 mil traces	See Figure 5-2
Metal Defined		NCTF	•15 mil pad, 4 mil wide traces	E1, D1, C2, B3, A4, A5 A34, A35, B36, C37, D38, E38 W38, Y38, AA37, AB36, AC35, AC34 AC5, AC4, AB3, AA2, Y1, W1
		NCTF	•15 mil pad	J16-J23 K16-P16 R16-R23 K23-P23

Notes:
1. CTF: Critical to Function
2. NCTF: Non-Critical to Function
3. SRO: Solder Resist Opening

5.4.4 Strain Guidance

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance apply only to transient bend conditions seen in board manufacturing assembly environment. It should be noted that any strain metrology is sensitive to boundary conditions.

Intel recommends the use of BFI to prevent solder joint defects. For additional guidance on BFI, see *Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly*, also referred as BFI MAS (Manufacturing Advantage Services) and BFI STRAIN GUIDANCE SHEET (868-FCBGA). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your factory.

5.4.5 Board Deflection

Exceeding the maximum Board Deflection called out in Table 2-1, may result in solder joint failure. Board deflection under the package can be kept to an acceptable level by adhering to the maximum load values.

Method by which the PCB is supported with the chassis will have an impact on board deflection and resultant package solder ball stress. Customers need to assess shock for their designs as their heatsink retention, heatsink mass, and the PCB attachment mechanism may vary.

Designs that exceed the maximum Heatsink Static Compressive Load, should follow Board Deflection Measurement Methodology as outlined to assess risk to package solder joint reliability.

5.5 Reliability Guidelines

Each motherboard, heatsink and attach combination may vary the mechanical loading of the component. Based on the end user environment, the user should define the appropriate reliability test criteria and carefully evaluate the completed assembly prior to use in high volume. The reference solution is to be mounted to a fully configured system. Some general recommendations are shown in Table 5-3.

Table 5-3. Reliability Guidelines

Test	Objective	Inspection Guidelines
Mechanical Shock	50 g, board level, 11 msec, 3 shocks/axis	Visual Check and Electrical Functional Test
Random Vibration	7.3 g, board level, 45 min/axis, 50 Hz to 2000 Hz	Visual Check and Electrical Functional Test
Temperature Life	85°C, 2000 hours total, check points at 168, 500, 1000 and 2000 hours	Visual Check
Thermal Cycling	-5°C to +70°C, 500 cycles	Visual Check
Humidity	85% relative humidity, 55°C, 1000 hours	Visual Check

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6 Reference Thermal Solution

Intel has developed a reference thermal solutions to meet the cooling needs of the component under operating environments and specifications defined in this document. This chapter describes the overall requirements for the push-pinned heatsink reference thermal solution, including critical-to-function dimensions, operating environment, and validation criteria.

6.1 Operating Environment

The reference thermal solution was designed assuming both a max fan speed condition and an acoustic fan speed condition. Table 6-1 provide operating environmental conditions applied in defining and designing the reference cooling solution.

Table 6-1. Operating Environmental Boundary Conditions

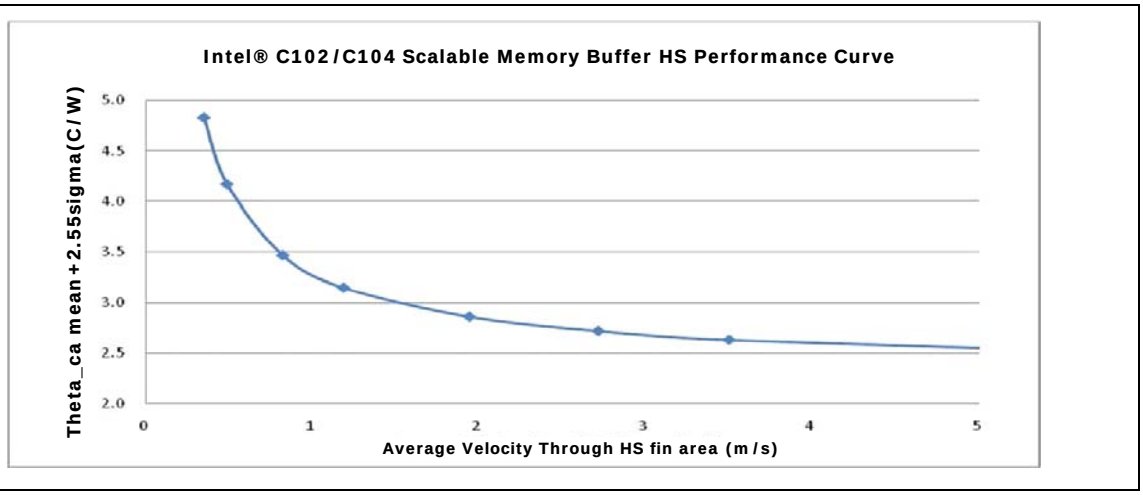
	Conditions		
Parameter	**High Fan Speed**	**Acoustic Fan Speed**	**Notes**
T_{SA}	35 °C	25 °C	1
Altitude	1500 m		
T_{LA}	60 °C	60 °C	2
Air Flow	2 m/s	> 0.65 m/s	
Power	TDP	5.9 W	3

Notes:
1. T_{SA} refers to the environment external to the system.
2. T_{LA} refers to the inlet temperature at the component heatsink.
3. Power dissipated by the device under acoustic conditions is considered to be at mid point between idle power and TDP.

6.2 Heatsink Performance

The *simulated* thermal performance of reference heatsink performance characterization is provided in Figure 6-1. Since this data was measured at sea level, a correction factor would be required to estimate thermal performance at other altitudes.

Figure 6-1. Heatsink Thermal Performance Versus Approach Velocity



Notes:
1. Where Alpha= 2.3553, Beta = 0.9315, Gamma= 0.9301
2. Thermal Interface Material (TIM): Honeywell PCM45F*
3. TIM effective end of life (EOLife) performance model derived from test results:

† Rjs=0.39C.cm2/W

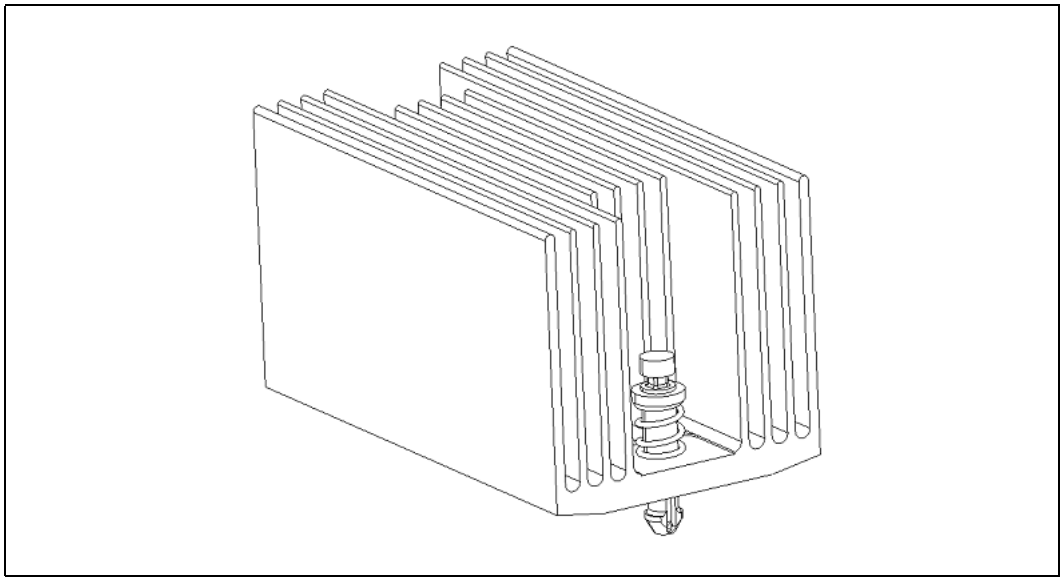
† Effective K=3.17 W/MK, 0.127 mm thickness, for pressure at 40 Psi TIM preload on bare die

6.3 Heatsink Assembly

The reference thermal solution for the components is a passive extruded heatsink with thermal interface. It is secured to the PCB using a two push-pin fasteners. Figure 6-2 shows the reference thermal solution assembly and associated components.

Full mechanical drawings of the thermal solution assembly and the heatsink clip are provided in Appendix B. Appendix A contains vendor information for each thermal solution component.

Figure 6-2. Heatsink Assembly



6.3.1 Heatsink Orientation

Since this solution is based on a unidirectional heatsink, it implies that the airflow direction must be aligned with the direction of the heatsink fins.

6.3.2 Extruded Heatsink Profiles

The reference thermal solution uses an extruded heatsink for cooling the components. Appendix A lists a supplier for this extruded heatsink. Other heatsinks with similar dimensions and increased thermal performance may be available. Full mechanical drawings of this heatsink are provided in Appendix B.

6.3.3 Mechanical Interface Material

To prevent the risk of damaging the die, Intel's reference thermal solution includes x4 standoffs at the corner of heatsink and a foam spacer that is attached to the base of heatsink surrounding the package die. The foam spacer is intended to dampen the mechanical load onto the die resulted from mechanical shock and vibration.

A pedestal at the center of heatsink base limits the area of the heatsink base that interfaces with the surface of the die, while providing clearance for the heatsink base above the package substrate top side caps during the heatsink installation process. Heatsink pedestal height also limits extend of the foam spacer compression under load. Limiting the foam compression is necessary to prevent damaging the substrate top side caps. For additional details and foam specification see manufacturer datasheet.

Table 6-2. Heatsink Foam Spacer

Parameter	Value/Part Number	Units	Notes
Material	CF-45EG		See heatsink drawing
Adhesive Material	PSA 3M 9448		See heatsink drawing
Thickness	2	mm	
Dimensions			See Heatsink drawing

6.3.4 Thermal Interface Material

A thermal interface material (TIM) provides improved conductivity between the die and heatsink. The reference thermal solution uses Honeywell PCM45F, 0.25 mm (0.010 in.) thick, 15 mm x 8 mm (0.6 in. x 0.315 in.) square.

Note: Unflowed or "dry" Honeywell PCM45F has a material thickness of 0.010 in. The flowed or "wet" Honeywell PCM45F has a material thickness of ~0.003 in. after it reaches its phase change temperature.

To achieve TIM performance target, heatsink shall apply 9.3 N [2.1 lbf]. This defines the minimum heatsink load requirement insuring minimum TIM bond line thickness (BLT) is achievable.

6.3.5 Heatsink Mass

Mass of the reference heatsink design is estimated to be 49 grams.

6.3.6 Heatsink Retention

The reference solution uses a push-pin. See Appendix B for a mechanical drawing of the clip. Push-pin supports board thickness of boards thickness 2.36 mm and 3.3 mm [0.085” and 0.093”]. See Appendix A for the supplier information.

Table 6-3. Push-Pin P/N

Part Number	Board Thickness	Board Insertion Force	Pullout Force
83FT05-20-9909	2.36 mm [0.093 in]	33.8N [7.6 lbf] Min 40.5 N [9.1 lbf] Max	> 44.5N [10 lbf]
83FT11-20-9909	3.3 mm[0.130 in]	33.8N [7.6 lbf] Min 40.5 N [9.1 lbf] Max	> 44.5N [10 lbf]

Note:

1. Push-pins are designed for specific board thickness. See supplier specifications for details.
2. Insertion and pull forces are based on limited sample size.

§

A Component Suppliers

Third-party suppliers are enabled so that reference thermal and mechanical components are available. Suppliers identified in Table A-1 have notified Intel of their intent to support the Intel® C102/C104 Scalable Memory Buffer by supplying thermal and mechanical solutions based on Intel reference design.

Notes:

1. Supplier information provided in the table was deemed accurate at the time of this document release. Customers planning on using Intel reference designs should contact the component suppliers for the latest information.
2. These vendors are listed by Intel as a convenience for its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of these devices.

Table A-1. Thermal Solution Enabled Supplier Listing (Sheet 1 of 2)

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Assembly includes: • Heatsink • Thermal Interface Material • Push-pin Assembly • Foam Spacer	E99987-003 (93mil board thickness) G44074-003 (130 mil board thickness)	Chaun-Choung Technology Corp (CCI)*	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Heatsink	E99987_CP01_HS	Chaun-Choung Technology Corp (CCI)*	Harry Lin (USA) 714-739-5797 hlinack@aol.com Monica Chih (Taiwan) 866-2-29952666, x131 monica_chih@ccic.com.tw
Thermal Interface (PCM45F)	E99987_CP02_TIM	Honeywell PCM45F* (H245F15X15MMS)	Andrew Ho (Worldwide, HK) (852)9095-4593 andrew.ho@honeywell.com David Shen (PRC) david.shen@honeywell.com 86-21-289-44064

Table A-1. Thermal Solution Enabled Supplier Listing (Sheet 2 of 2)

Part	Intel Part Number	Supplier (Part Number)	Contact Information
Heatsink Attach Fastener		ITW 83FT05-20-9909 (93mil board thickness) 83FT11-20-9909 (130mil board thickness)	ITW Electronics Business Asia Co. Ltd. A4, 3-2, K.E.PZ. Kaohsiung, Taiwan Tel. 886-7-811-9206~10 (5 lines) Fax: 886-7-811-1795 Taipei Office: 3F-7, No.193, Ching-Hsing RD., Wen-Shan District, Taipei, Taiwan Tel. 886-2-2930-8340~1 (2 lines) Fax: 886-2-2930-8342
Foam Spacer		Pad_CF45EF_2MM	Central China E-A-RTM Shock and Vibration Solutions Aearo Trading (Shenzhen) Company, Ltd. A 3M company Winson Ling (wling@mmm.com) Tel:+86 18601772976 Tiger Hu(thu@mmm.com) Tel:+86 136 0167 3448

Notes:
1. Contact the supplier directly to verify time of component availability.
2. Heatsink fastener is independent of heatsink assembly. Proper push-pin fastener selection protects the chipset heatsink from shock and vibration.

§

B Mechanical Drawings

Table B-1 lists the mechanical drawings included in this appendix.

Table B-1. Mechanical Drawing List

Drawing Description	Figure Number
Memory Buffer Package Mechanical Drawing - Sheet 1 of 2	Figure B-1
Memory Buffer Package Mechanical Drawing - Sheet 2 of 2	Figure B-2
PCB Mechanical Keep-out Drawing	Figure B-3
Heatsink Mechanical Assembly Drawing - E99987 Rev G (sheet 1 of 3)	Figure B-4
Heatsink Mechanical Assembly Drawing - E99987 Rev G (sheet 2 of 3)	Figure B-5
Heatsink Mechanical Assembly Drawing - E99987 Rev G (Sheet 3 of 3)	Figure B-6
Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 1 of 3)	Figure B-7
Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 2 of 3)	Figure B-8
Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 3 of 3)	Figure B-9

Figure B-1. Memory Buffer Package Mechanical Drawing - Sheet 1 of 2

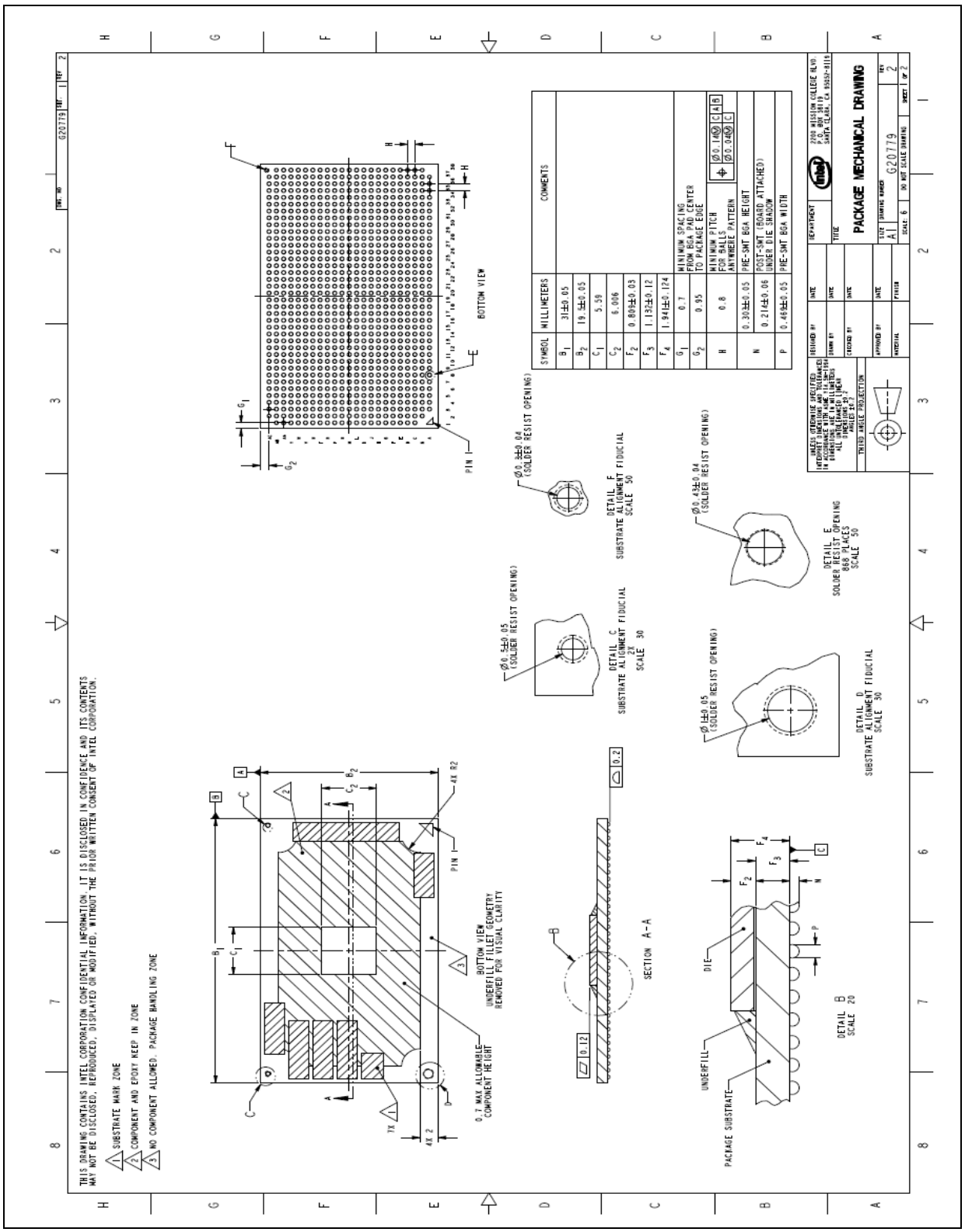


Figure B-2. Memory Buffer Package Mechanical Drawing - Sheet 2 of 2

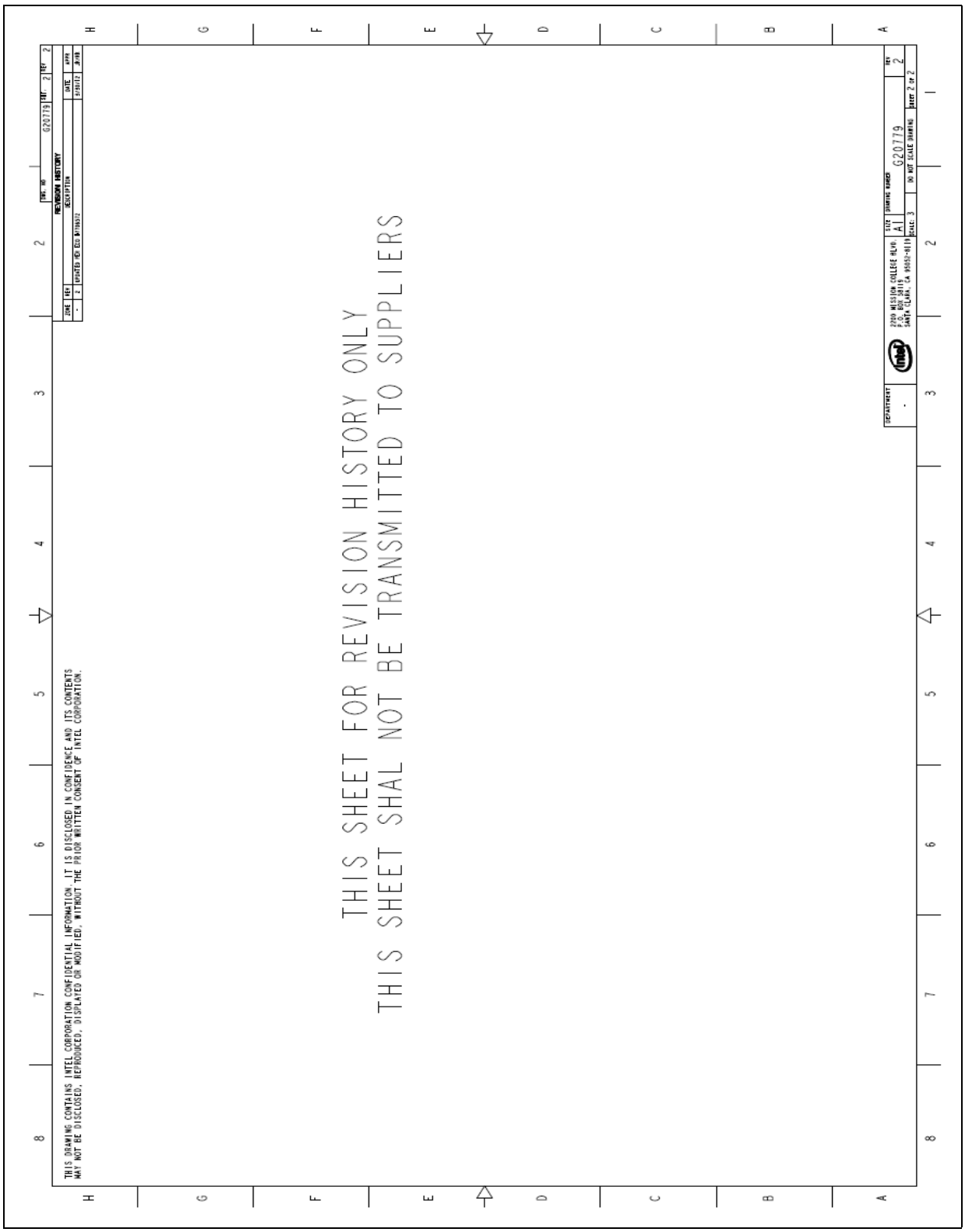


Figure B-3. PCB Mechanical Keep-out Drawing

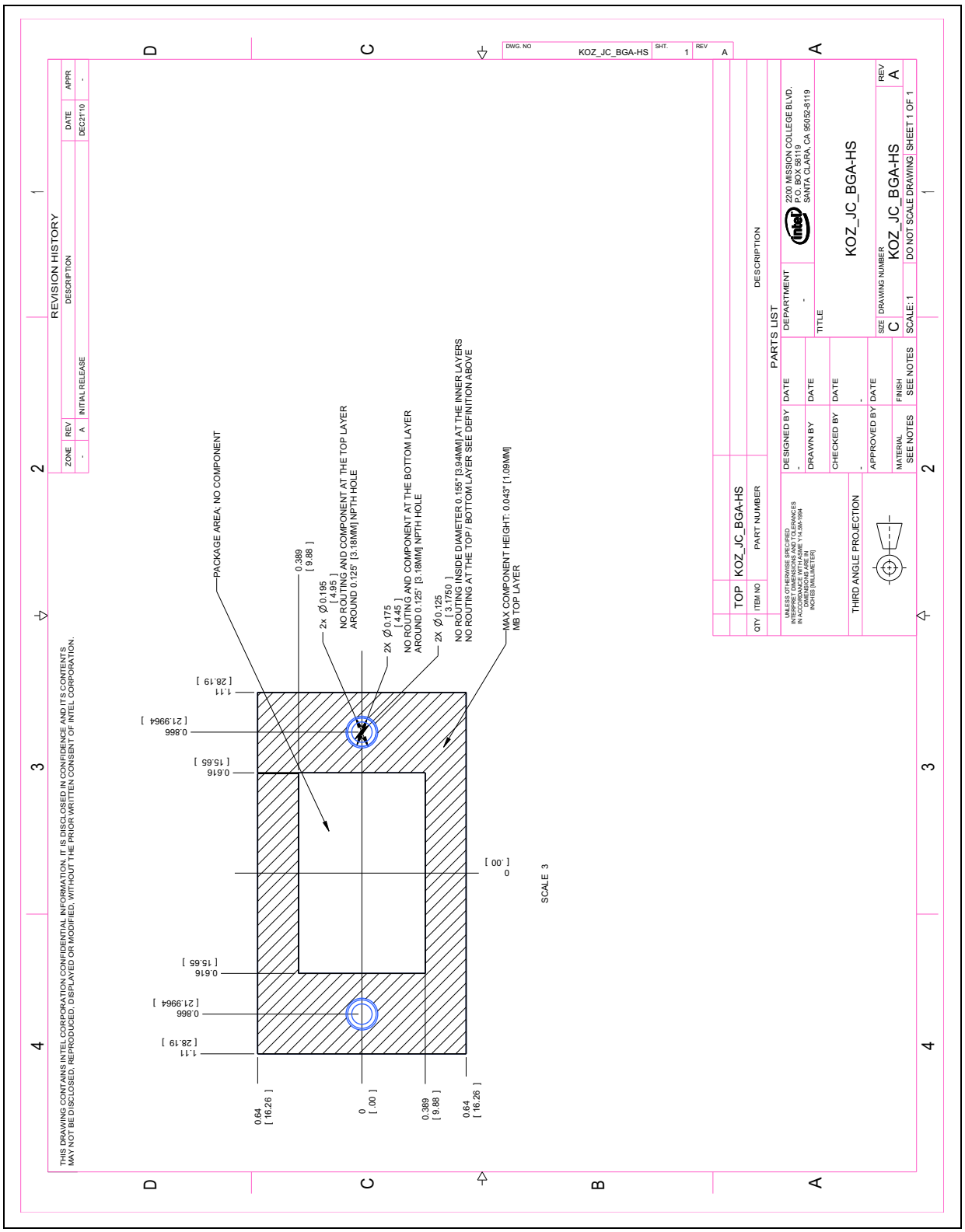


Figure B-4. Heatsink Mechanical Assembly Drawing - E99987 Rev G (sheet 1 of 3)

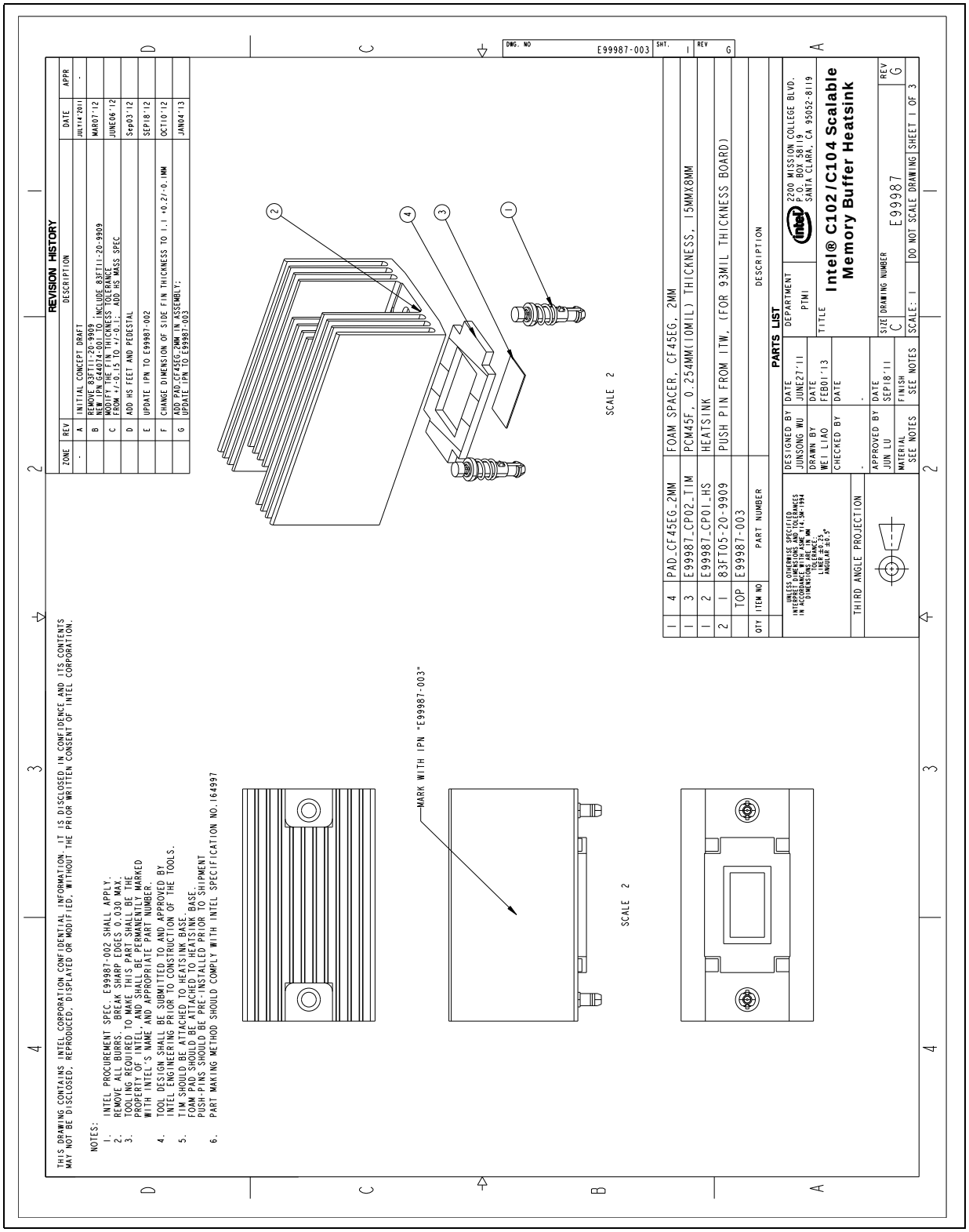


Figure B-5. Heatsink Mechanical Assembly Drawing - E99987 Rev G (sheet 2 of 3)

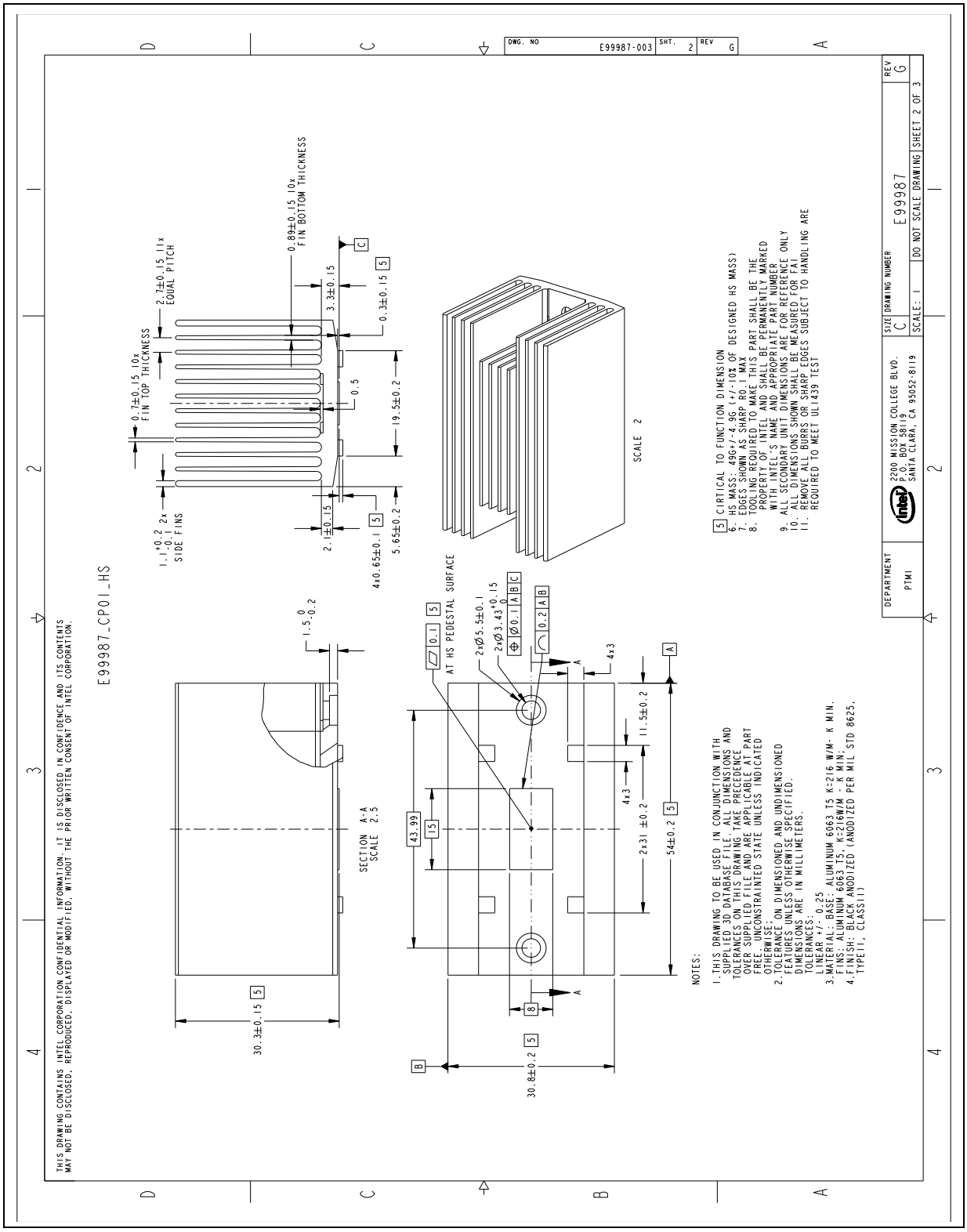


Figure B-6. Heatsink Mechanical Assembly Drawing - E99987 Rev G (Sheet 3 of 3)

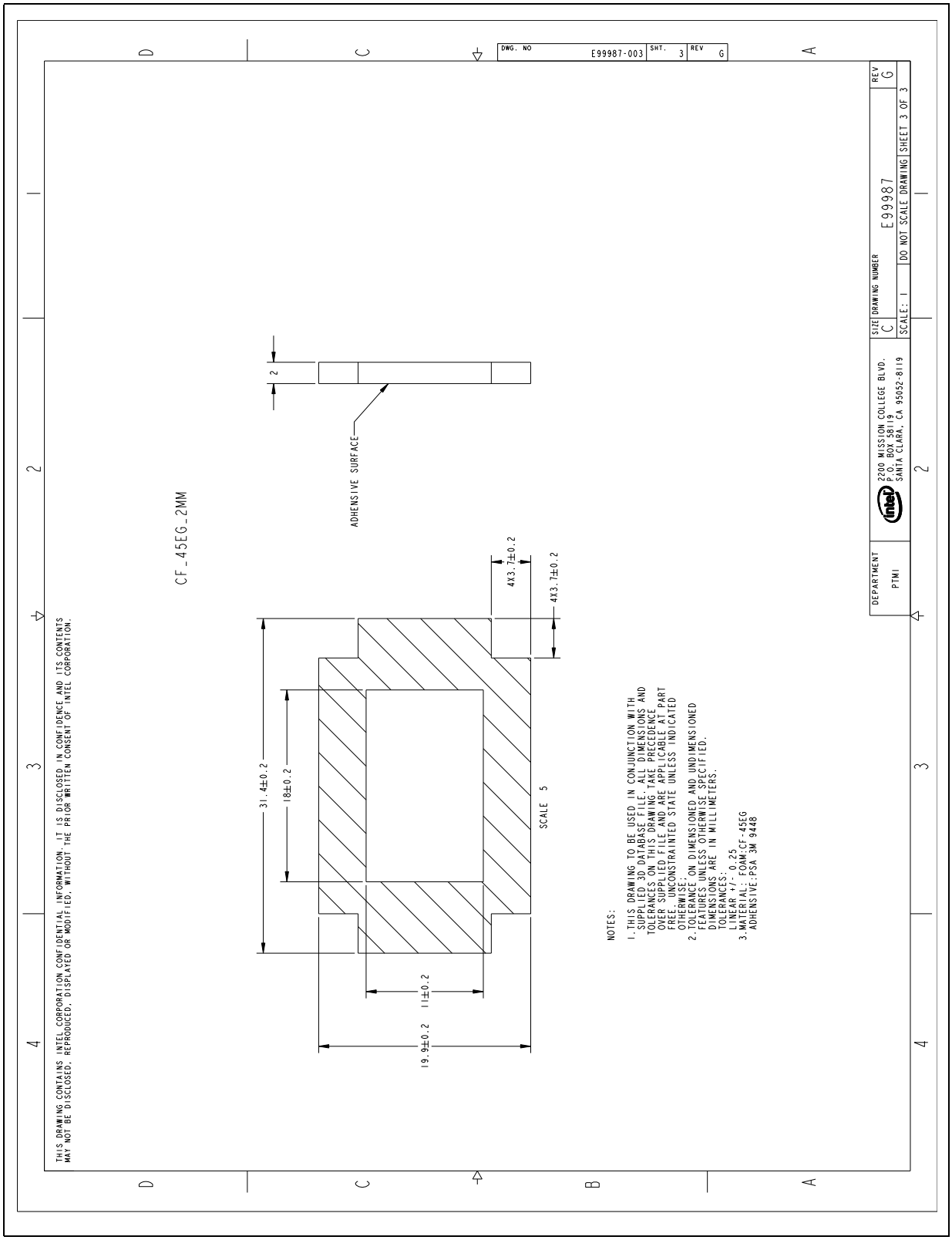


Figure B-7. Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 1 of 3)

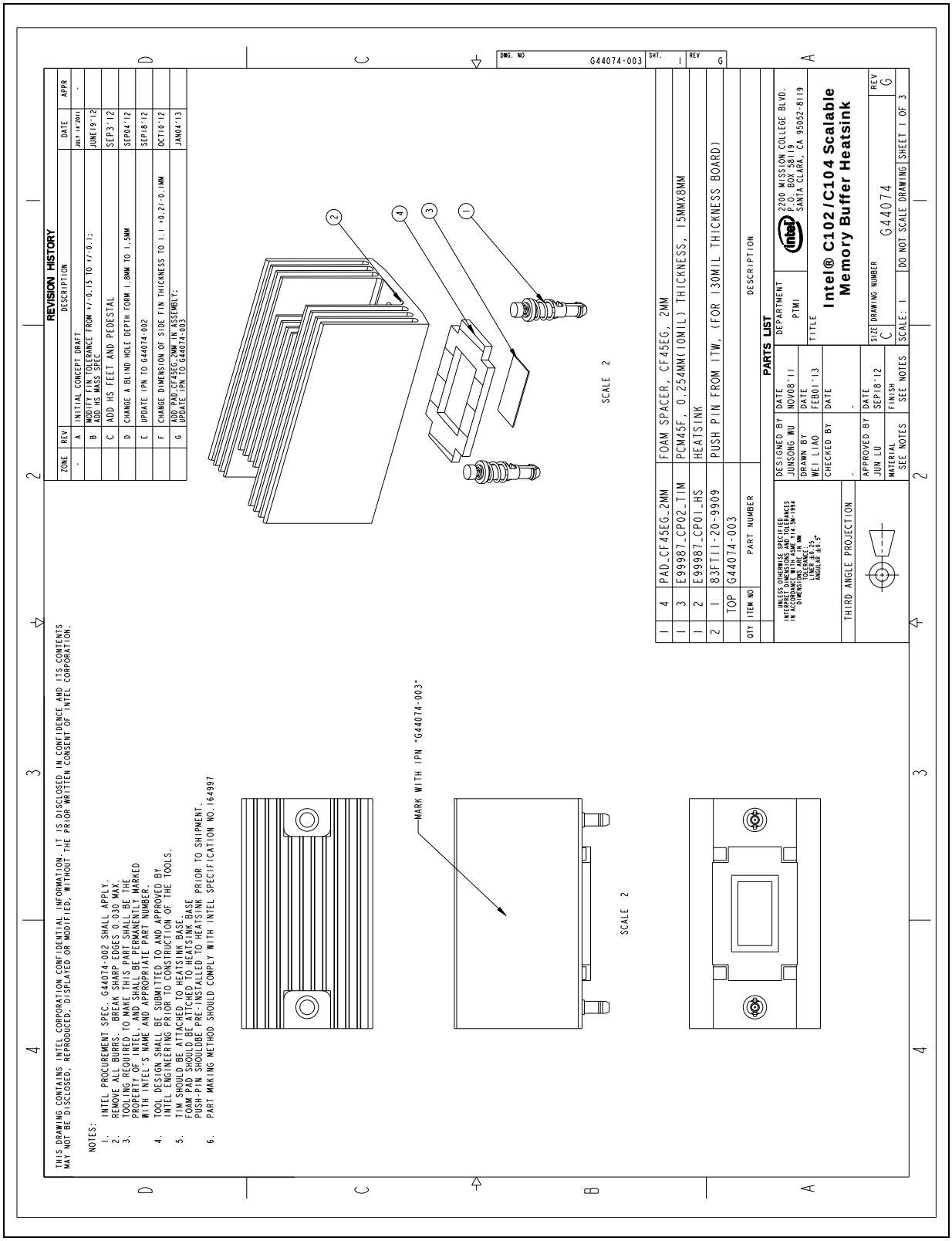


Figure B-8. Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 2 of 3)

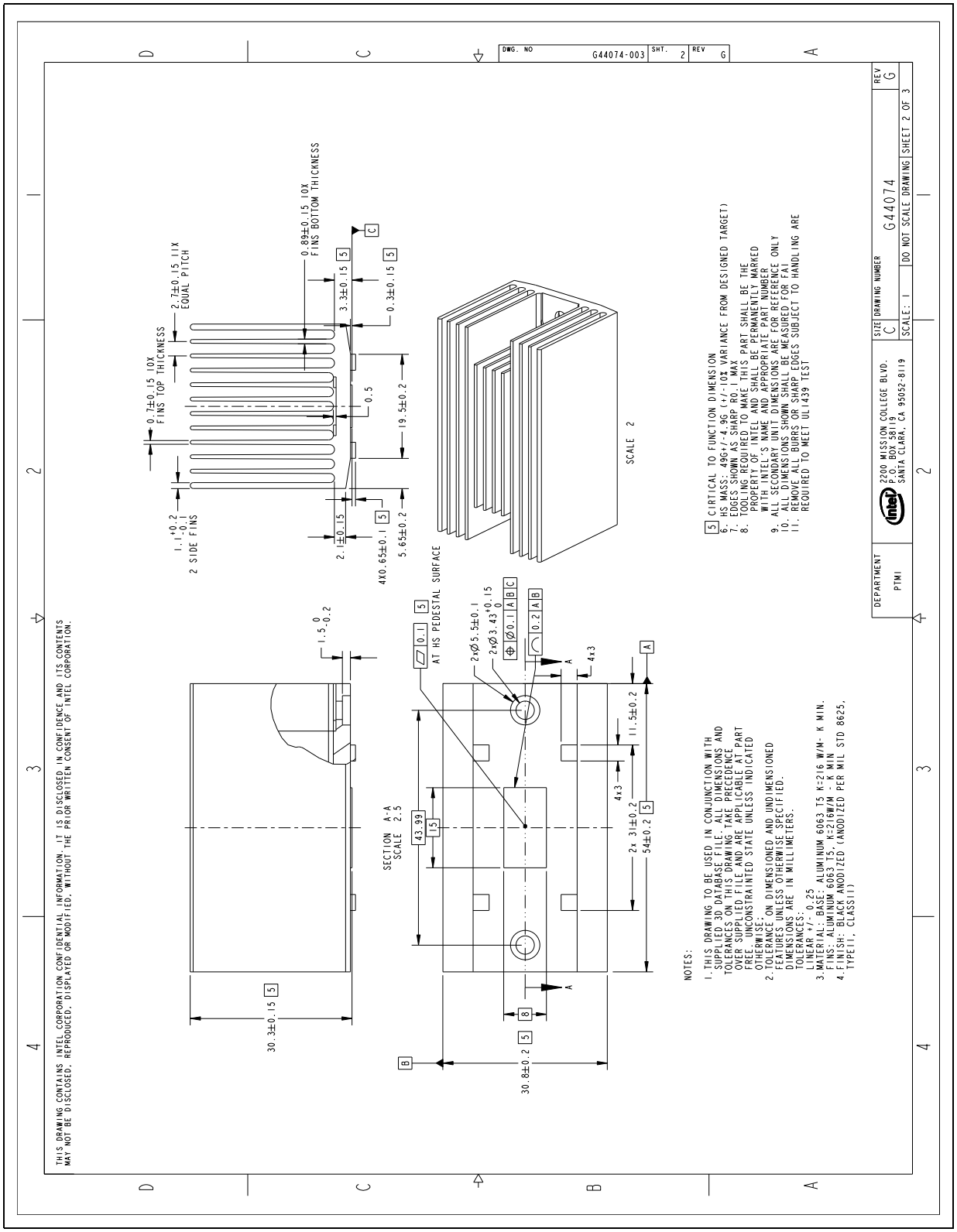


Figure B-9. Heatsink Mechanical Assembly Drawing - G44074 Rev G (Sheet 3 of 3)