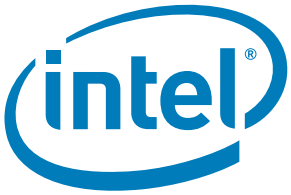


Intel® Ethernet Switch FM2212

12-Port 10G Ethernet L2 Switch Chip

Data Sheet Addendum

September, 2007 (Revision 1.1)

Legal

Table of Contents

Overview

Intel® offers multiple market- and customer-specific product variants based on the platform. This preliminary data sheet addendum documents the features and functionality of the 12-port variant of the FM2000 platform, which will be referred to in this document as the FM2212.

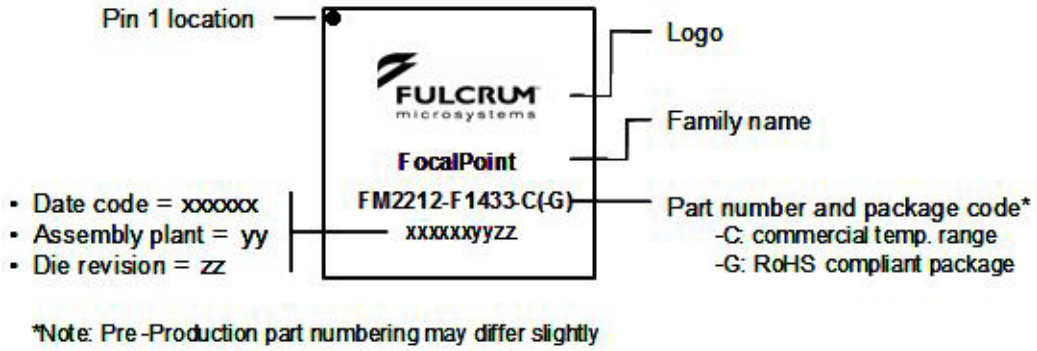
Note: This document is intended to be used in conjunction with the FM2224 Datasheet. It outlines the specification differences between the FM2212 and the original FM2224. All specifications are based on pre-production release test data and are subject to change. Rev 2.0 of this document and the FM2224 datasheet, when released, will contain complete and final specifications and will be available concurrently with the product's production release.

Document Revision History

Revision	Date	Notes
1.0	Dec 7, 2006	Initial version of Preliminary Datasheet Addendum
1.1	Sept 28, 2007	Corrected RCK to por

Product Applicability

The FM2000 part numbers are structured as follows:



Key:

- Product Family: "2" represents the Ethernet L2 switch product family, of which the FM2000 is a member.
- Port Configuration: Provides guidance on the composition of the ports in the device, as follows:
- 1: More than 50% of the interfaces are single-SerDes interfaces
- 2: More than 50% of the interfaces are quad-SerDes interfaces
- Aggregate Bandwidth: "12" represents an aggregate bandwidth of 120 Gbps.

- Temperature: "C" represents Commercial temperature grade. The grades indicate case temperatures as follows:

Grade	Designator	Tcase(min) (°C)	Tcase(max) (°C)
Commercial	-C	0	+85
Extended	-E	0	+105
Industrial	-I	-40	+115

RoHS Compliance: The presence of a "-G" means that the device is complaint with the RoHS requirements for restrictions on the use of hazardous substances. Compliance is via exemption #15 in the RoHS Directive Annex, which allows for the use of Pb (lead) in the solder bumps used for die attaché in flip-chip packages. -G parts have lead-free solder balls on the exterior of the package for PC board die attach.

Note that the non-RoHS compliant package meets the RoHS limits for the other five substances, but contains Pb in the external solder balls, which is not allowed by the RoHS directive, and in the solder bumps for die attach.

Other Related Documents and Tools

Other documents that may be useful for evaluating and using the FM2224 include:

- FM2224 Datasheet
- FM2224 Software API Specification
- FM2224 Specification Update, which contains errata and other specification and documentation changes
- FM2224 Design and Layout Guide
- FM2224 Reference Design Data Sheet
- FM2224 Design Support Package on CD

1.0 Introduction

This document is intended to be used in conjunction with the FM2224 datasheet. It outlines the specification differences between the FM2212 and the original FM2224. The FM2212 is a 20-port version of the 24-port FM2224. The primary difference between the two devices is that of the 24 ports, ports 5, 6, 9 and 10 are not used in the FM2212. The port numbers in use for the FM2212 are:

[0, 3, 4, 7, 8, 11, 12, 13, 14, 19, 20, 23, 24]

Unless information is specifically outlined in this document, the information contained in the FM2224 datasheet shall prevail.

This document is separated into three primary sections (which correspond to sections in the FM2224 datasheet), as follows:

- Electrical Specifications (corresponds to Section 4 in the FM2224 datasheet)
- Register Definitions (corresponds to Section 5 in the FM2224 datasheet)
- Signal, Ball, and Package Descriptions (corresponds to section 6 in the FM2224 datasheet)

2.0 Electrical Specifications

The following tables provide recommended operating conditions for the FM2212.

2.1 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Core Voltage	V_{DD}	-0.3	2	Volts
SerDes Supply Voltage	V_{DDX}	-0.3	2	Volts
SerDes Bias Voltage	V_{DDA}	-0.3	2	Volts
Transmitter Termination Voltage	V_{TT}	-0.3	2	Volts
LVTTL Power Supply	V_{DD33}	-0.3	3.9	Volts
PLL Analog power supply	V_{DDA33}	-0.3	3.9	Volts
Case Temp under bias		-	+130	°C
Storage Temp		-65	+150	°C
ESD		-2000	+2000	Volts

2.2 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Core Voltage	V_{DD}	1.14	1.2	1.26	Volts
SerDes Supply Voltage	V_{DDX}	1.14	1.2	1.26	Volts[1,3]
		0.95	1.0	1.1	Volts[2,3]
SerDes Bias Voltage	V_{DDA}	1.14	1.2	1.26	Volts
		0.95	1.0	1.1	Volts
LVTTL Power Supply	V_{DD33}	3.14	3.3	3.47	Volts
PLL Analog power supply	V_{DDA33}	3.14	3.3	3.47	Volts
Transmitter Termination Voltage	V_{TT}	Vdd	1.5	1.8	Volts
Operating Temp (Case)					
Commercial		0		+85	°C
Extended		0		+105	°C
Industrial		-40		+115	°C

(1) Connect a 1.2KΩ resistor from RREF to VDDX for 1.2V operation

(2) Connect a 1.0KΩ resistor from RREF to VDDX for 1.0V operation

(3) Operating with V_{DDX} and V_{DDA} = 1.0V results in less power dissipation, but operating with V_{DDX} and V_{DDA} =1.2V may be desired to avoid implementation of another supply voltage.

3.0 Register Definitions

This section provides information on the registers used in the FM2212. The base specification (FM2224) has a number of per-port register sets which are recognizable by the suffix, [1..24] or [0..24] since there are 24 ports on that device (port 0 is the LCI - Logical CPU Interface).

The same register set and register masks exist for the FM2212, but the register for ports 1, 2, 5, 6, 9, 10, 15, 16, 17, 18, 21 and 22 are not used. The port numbers in use for the FM2212 are:

[0, 3, 4, 7, 8, 11, 12, 13, 14, 19, 20, 23, 24]

With that in mind, it should be noted that for all per-port register sets, registers pertaining to ports 1, 2, 5, 6, 9, 10, 15, 16, 17, 18, 21 and 22 are not in use. Register sets containing the suffix [0..24] should be replaced by [0, 3, 4, 7, 8, 11, 12, 13, 14, 19, 20, 23, 24] and those containing [1..24] replaced with [3, 4, 7, 8, 11, 12, 13, 14, 19, 20, 23, 24].

The following register sets fall into this category:

- Table 3 PORT_CFG_1 [1..24]
- Table 4 PORT_CFG_2 [1..24]
- Table 5 TRUNK_CANONICAL [1..24]
- Table 6 RX_PRI_MAP [0..24]
- Table 7 QUEUE_CFG_1 [0..24]
- Table 8 QUEUE_CFG_2 [0..24]
- Table 9 STREAM_STATUS_1 [0..24]
- Table 10 EGRESS_SCHEDULE_1 [0..24]
- Table 11 GLOBAL_PAUSE_WM [0..24]
- Table 12 RX_PAUSE_WM [0..24]
- Table 13 SAF_MATRIX [1..24]
- Table 14 Group 2 Counters - RX Packet Counters per Size [0..24]
- Table 15 Group 3 Counters - RX Octet Counters [0..24]
- Table 16 Group 4 Counters - RX Packet Counters per Priority [0..24]
- Table 17 Group 5 Counters - RX Octet Counters per Priority [0..24]
- Table 18 Group 6 Counters - RX Packet Counters per Flow [0..24]
- Table 19 Group 7 Counters - TX Packet Counters per Type [0..24]
- Table 20 Group 8 Counters - TX Packet Counters per Size [0..24]
- Table 21 Group 9 Counters - TX Octet Counters [1..24]
- Table 22 Group 11 Counters - VLAN Octet Counters [0..31]
- Table 23 Group 12 Counters - VLAN Packet Counters [0..31]
- Table 24 SERDES_CTRL_1 [1..24]
- Table 25 SERDES_CTRL_2 [1..24]
- Table 26 SERDES_CTRL_3 [1..24]
- Table 27 SERDES_TEST_MODE [1..24]
- Table 28 SERDES_STATUS [1..24]
- Table 29 SERDES_IP [1..24]
- Table 30 SERDES_IM [1..24]
- Table 31 SERDES_BIST_ERR_CNT [1..24]
- Table 32 PCS_CFG_1 [1..24]
- Table 33 PCS_CFG_2 [1..24]
- Table 34 PCS_CFG_3 [1..24]
- Table 35 PCS_CFG_4 [1..24]
- Table 36 PCS_CFG_5 [1..24]
- Table 37 PCS_IP [1..24]
- Table 38 PCS_IM [1..24]
- Table 39 PACING_PRI_WM [0..7] [1..24]
- Table 40 PACING_RATE [1..24]
- Table 41 PACING_STAT [1..24]

- Table 42 MAC_CFG_1 [1..24]
- Table 43 MAC_CFG_2 [1..24]
- Table 44 MAC_CFG_3 [1..24]
- Table 45 MAC_CFG_4 [1..24]
- Table 46 MAC_CFG_5 [1..24]
- Table 47 MAC_CFG_6 [1..24]
- Table 48 TX_PRI_MAP_1 [1..24]
- Table 49 TX_PRI_MAP_2 [1..24]
- Table 50 MAC_STATUS [1..24]
- Table 51 MAC_IP [1..24]
- Table 52 MAC_IM [1..24]
- Table 53 EPL_INT_DETECT [1..24]
- Table 54 EPL_LED_STATUS [1..24]
- Table 55 STAT_EPL_ERROR1[1..24]
- Table 56 STAT_EPL_ERROR2[1..24]
- Table 57 STAT_RX_JABBER [1..24]
- Table 58 STAT_TX_CRC [1..24]
- Table 59 STAT_TX_PAUSE [1..24]
- Table 60 STAT_TX_BYTECOUNT [1..24]

4.0 Signal, Ball, and Package Descriptions

4.1 Package Overview

The FM2212 uses the following package:

- Overall package dimensions of 40mm x 40mm
- Flip-chip-based BGA package, with attached heat spreader
- 39 balls on a side (ball pitch of 1.0mm)
- 1,433 total balls in use

4.2 Power Mapping

Figure 1 shows a visual mapping of the power pins for the device.

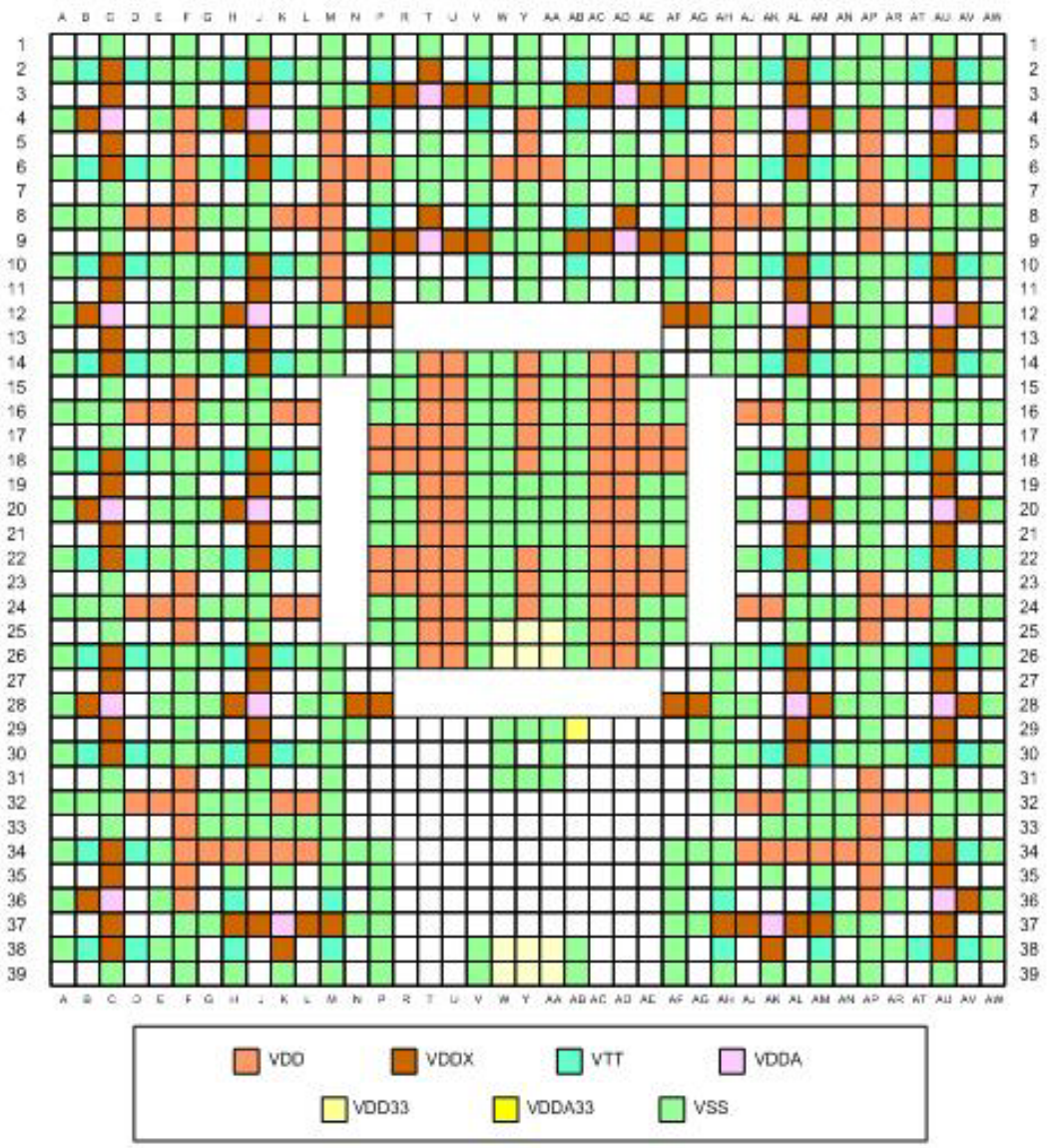


Figure 1. Power Mapping for the FM2212 1433-ball BGA Package (bottom view)

Note: Consult the FM2224 Design and Layout Guide (Intel® document number: FM2224-DG) for specific information on filtering strategies. These apply equally to the FM2212.

4.3 Interface Mapping

Figure 2 shows a visual mapping of the interface pins for the device.

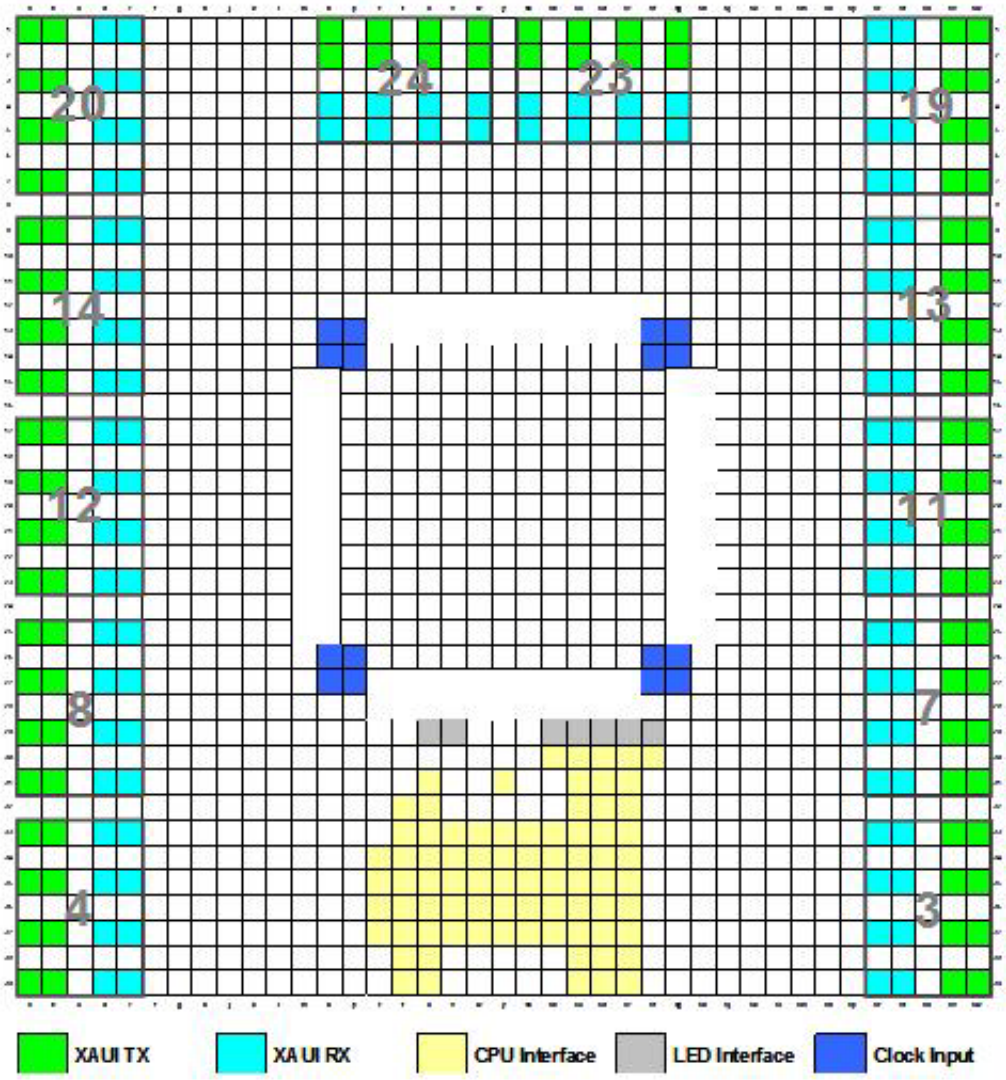


Figure 2. Interface Mapping (bottom view)

4.4 Signal Descriptions

This section describes the signals for the device, providing details on the name, ball assignment, type, and use of each signal.

4.4.1 FM2212 Signals

Table 61. FM2212 XAUI Signal Pins

Signal Name	I/O	Type	Description
Pnn_RAN [m..n]	CML	Input	Differential receive inputs for channel A -- Complement
Pnn_RAP [m..n]	CML	Input	Differential receive inputs for channel A -- True
Pnn_RBN [m..n]	CML	Input	Differential receive inputs for channel B -- Complement
Pnn_RBP [m..n]	CML	Input	Differential receive inputs for channel B -- True
Pnn_RCN [m..n]	CML	Input	Differential receive inputs for channel C -- Complement
Pnn_RCP [m..n]	CML	Input	Differential receive inputs for channel C -- True
Pnn_RDN [m..n]	CML	Input	Differential receive inputs for channel C -- Complement
Pnn_RDP [m..n]	CML	Input	Differential receive inputs for channel C -- True
Pnn_TAN [m..n]	CML	Output	Differential transmit outputs for channel A - Complement
Pnn_TAP [m..n]	CML	Output	Differential transmit outputs for channel A - True
Pnn_TBN [m..n]	CML	Output	Differential transmit outputs for channel B - Complement
Pnn_TBP [m..n]	CML	Output	Differential transmit outputs for channel B - True
Pnn_TCN [m..n]	CML	Output	Differential transmit outputs for channel C - Complement
Pnn_TCP [m..n]	CML	Output	Differential transmit outputs for channel C - True
Pnn_TDN [m..n]	CML	Output	Differential transmit outputs for channel D - Complement
Pnn_TDP [m..n]	CML	Output	Differential transmit outputs for channel D - True
RREF [m..n]	Analog	Reference	Reference resistor pad. RREF connects a 1.2KΩ external resistor to VDDA to provide a reference current for the driver and equalization circuits

Note: There are twenty XAUI interfaces in total. The "[m..n]" in the above signal names represent a port numbers [3, 4, 7, 8, 11, 12, 13, 14, 19, 20, 23, 24].

Table 62. FM2212 High-Speed Clock Signal Pins

Signal Name	I/O	Type	Description
RCK1AN	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 3, 7, 11 Complement
RCK1AP	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 3, 7, 11 True
RCK1BN	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 3, 7, 11 Complement
RCK1BP	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 3, 7, 11 True
RCK2AN	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 4, 8, 12 Complement
RCK2AP	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 4, 8, 12 True
RCK2BN	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 4, 8, 12 Complement
RCK2BP	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 4, 8, 12 True
RCK3AN	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 13, 19, 23 Complement
RCK3AP	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 13, 19, 23 True
RCK3BN	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 13, 19, 23 Complement
RCK3BP	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 13, 19, 23 True
RCK4AN	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 14, 20, 24 Complement
RCK4AP	CML (1) LVDS LVPECL	Input	Differential Reference Clock A for Ports 14, 20, 24 True
RCK4BN	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 14, 20, 24 Complement
RCK4BP	CML (1) LVDS LVPECL	Input	Differential Reference Clock B for Ports 14, 20, 24 True

Note: These pins are AC coupled and are compatible with the stated IO. For LVDS IO a 2K resistor is required between the lines on the driver side of the isolation capacitors

Table 63. FM2212 CPU Interface Signal Pins

Identical to FM2224.

Table 64. FM2212 DMA Pins

Identical to FM2224.

Table 65. FM2212 SPI Interface Signal Pins

Identical to FM2224.

Table 66. FM2212 LED Interface Signal Pins

Identical to FM2224.

Table 67. FM2212 JTAG Interface Signal Pins

Identical to FM2224.

Table 68. FM2212 Miscellaneous Signal Pins

Identical to FM2224.

Table 69. List of No Connects and Unpopulated Ball Locations

Pins	Description
ag15, ag16, ag17, ag18, ag19, ag20, ag21, ag22, ag23, ag24, ag25 ah15, ah16, ah17, ah18, ah19,ah20, ah21, ah22, ah23, ah24, ah25 m15, m16, m17, m18, m19, m20, m21,m 22, m23,m 24, m25 n15, n16, n17, n18, n19, n20,n 21, n22, n23, n24, n25 r12,r13, r27, r28 t12, t13, t27, t28 u12,u13, u27,u 28 v12, v13,v 27, v28 w12, w13, w27, w28 y12, y13, y27, y28 aa12, aa13, aa27, aa28 ab12, ab13, ab27, ab28 ac12,ac13, ac27, ac28 ad12,ad13, ad27, ad28 ae12,ae13, ae27, ae28	Ball grid locations that are not populated with solder balls
g17, g19, g21, g23, g25, g27, g29, g31 h17, h18, h19, h21, h22, h23, h25, h26, h27, h29, h30, h31, j20, j28, k17, k18, k19, k20, k21, k22, k23, k25, k26, k27, k28, k29, k30, k31, l17, l19, l21, l23, l25, l27, l29, l31, n30, p32, p33, r30, r32, r33, r38, r39 t30, v31, v32, w32, y32, aa32m ab31, ab32 af29, af31, af32, af33 ag30, ag31, ag32, ag33, aj17, aj19, aj21, aj23, aj25, aj27, aj29, aj31, ak17, ak18, ak19, ak20, ak21, ak22, ak23, ak25, ak26, ak27, ak28, ak29, ak30, ak31, al20, al28, am17, am18, am19, am21, am22, am23, am25, am26, am27, am29, am30, am31, an17, an19, an21, an23, an25, an27, an29, an31, an39, al39, aj39, ag39, an38, al38, aj38, ag38, an36, al36, aj36, ag36, an35, al35, aj35, ag35, ak36, ah36, ah38, am36, am38, ak37, n39, l39, j39, g39, n38, l38, j38, g38, n36, l36, j36, g36, n35, l35, j35, g35, k36, h36, h38, m36, m38, k37, an9, an11, an13, an15, am9, am11, am13, am15, ak9, ak11, ak13, ak15, aj9, aj11, aj13, aj15, ak12, ak10, ak14, am10, am14, al12, g15, g13, g11, g9, h15, h13, h11, h9, k15, k13, k11, k9, l15, l13, l11, l9, k12, h14, k10, k14, h10, j12, aa7, ac7, ae7, ag7, aa8, ac8, ae8, ag8, aa10, ac10, ae10, ag10, aa11, ac11, ae11, ag11, ad10, ab8, ab10, af8, af10, ad9, n7, r7, u7, w7, n8, r8, u8, w8, n10, r10, u10, w10, n11, r11, u11, w11, t10, p8, p10, v8, v10, t9, an1, an3, an5, an7, am1, am3, am5, am7, ak1, ak3, ak5, ak7, aj1, aj3, aj5, aj7, ak4, ak2, ak6, am2, am6, al4, g7, g5, g3, g1, h7, h5, h3, h1, k7, k5, k3, k1, l7, l5, l3, l1, k4, h2, h6, k2, k6, j4	No connects

4.4.2 Power Supply Pins and Recommendations

Table 70. FM2212 Power Supply Signal Descriptions

Signal Name	Quantity	Type	Description
V_{SS}	448	Power	Ground, for Core and I/O
V_{DD}	179	Power	Core VDD (1.2 V)
V_{DD33}	12	Power	I/O VDD (3.3 V), for LVTTL
V_{DDA33}	1	Power	PLL analog supply

Table 70. FM2212 Power Supply Signal Descriptions (Continued)

Signal Name	Quantity	Type	Description
V_{DDA}	12	Power	SerDes bias voltage
V_{DDX}	128	Power	SerDes supply voltage
V_{TT}	48	Power	TX termination voltage, which can be used to adjust the common mode voltage and swing of TX outputs

4.4.3 Ball Assignment

Table 71. Package Ball Assignments in Numerical Order

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
a1	P20_TDP	p1	VSS	ag1	P23_TDP
a2	VSS	p2	VTT24	ag2	P23_TDN
a3	P20_TCP	p3	VDDX	ag3	VSS
a4	VSS	p4	VTT24	ag4	P23_RDP
a5	P20_TBP	p5	VSS	ag5	P23_RDN
a6	VSS	p6	VDD	ag6	VDD
a7	P20_TAP	p7	VSS	ag7	DO NOT CONNECT
a8	VSS	p8	DO NOT CONNECT	ag8	DO NOT CONNECT
a9	P14_TDP	p9	VDDX	ag9	VSS
a10	VSS	p10	DO NOT CONNECT	ag10	DO NOT CONNECT
a11	P14_TCP	p11	VSS	ag11	DO NOT CONNECT
a12	VSS	p12	VDDX	ag12	VDDX
a13	P14_TBP	p13	RCK4AN	ag13	RCK3AN
a14	VSS	p14	RCK4BN	ag14	RCK3BN
a15	P14_TAP	p15	VSS	ag15	NO BALL
a16	VSS	p16	VSS	ag16	NO BALL
a17	P12_TDP	p17	VDD	ag17	NO BALL
a18	VSS	p18	VDD	ag18	NO BALL
a19	P12_TCP	p19	VSS	ag19	NO BALL
a20	VSS	p20	VSS	ag20	NO BALL
a21	P12_TBP	p21	VSS	ag21	NO BALL
a22	VSS	p22	VDD	ag22	NO BALL
a23	P12_TAP	p23	VDD	ag23	NO BALL
a24	VSS	p24	VSS	ag24	NO BALL
a25	P08_TDP	p25	VSS	ag25	NO BALL
a26	VSS	p26	RCK2BN	ag26	RCK1BN
a27	P08_TCP	p27	RCK2AN	ag27	RCK1AN
a28	VSS	p28	VDDX	ag28	VDDX
a29	P08_TBP	p29	LEDCLK	ag29	VSS
a30	VSS	p30	DO NOT CONNECT	ag30	DO NOT CONNECT

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
a31	P08_TAP	p31	CONT_OUT	ag31	DO NOT CONNECT
a32	VSS	p32	DO NOT CONNECT	ag32	DO NOT CONNECT
a33	P04_TDP	p33	DO NOT CONNECT	ag33	DO NOT CONNECT
a34	VSS	p34	VSS	ag34	VSS
a35	P04_TCP	p35	VSS	ag35	DO NOT CONNECT
a36	VSS	p36	VSS	ag36	DO NOT CONNECT
a37	P04_TBP	p37	VSS	ag37	VSS
a38	VSS	p38	VSS	ag38	DO NOT CONNECT
a39	P04_TAP	p39	VSS	ag39	DO NOT CONNECT
b1	P20_TDN	r1	P24_TBP	ah1	VSS
b2	VTT20	r2	P24_TBN	ah2	VSS
b3	P20_TCN	r3	VDDX	ah3	VSS
b4	VDDX	r4	P24_RBP	ah4	VDD
b5	P20_TBN	r5	P24_RBN	ah5	VDD
b6	VTT20	r6	VSS	ah6	VDD
b7	P20_TAN	r7	DO NOT CONNECT	ah7	VDD
b8	VSS	r8	DO NOT CONNECT	ah8	VDD
b9	P14_TDN	r9	VDDX	ah9	VDD
b10	VTT14	r10	DO NOT CONNECT	ah10	VDD
b11	P14_TCN	r11	DO NOT CONNECT	ah11	VDD
b12	VDDX	r12	NO BALL	ah12	VSS
b13	P14_TBN	r13	NO BALL	ah13	VSS
b14	VTT14	r14	VSS	ah14	VSS
b15	P14_TAN	r15	VSS	ah15	NO BALL
b16	VSS	r16	VSS	ah16	NO BALL
b17	P12_TDN	r17	VDD	ah17	NO BALL
b18	VTT12	r18	VDD	ah18	NO BALL
b19	P12_TCN	r19	VSS	ah19	NO BALL
b20	VDDX	r20	VSS	ah20	NO BALL
b21	P12_TBN	r21	VSS	ah21	NO BALL
b22	VTT12	r22	VDD	ah22	NO BALL
b23	P12_TAN	r23	VDD	ah23	NO BALL
b24	VSS	r24	VSS	ah24	NO BALL
b25	P08_TDN	r25	VSS	ah25	NO BALL
b26	VTT08	r26	VSS	ah26	VSS
b27	P08_TCN	r27	NO BALL	ah27	VSS
b28	VDDX	r28	NO BALL	ah28	VSS
b29	P08_TBN	r29	LED_DATA0	ah29	VSS
b30	VTT08	r30	DO NOT CONNECT	ah30	VSS
b31	P08_TAN	r31	EEPROM_EN	ah31	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
b32	VSS	r32	DO NOT CONNECT	ah32	VSS
b33	P04_TDN	r33	DO NOT CONNECT	ah33	DIODE_IN
b34	VTT04	r34	SPI_SO	ah34	VSS
b35	P04_TCN	r35	SPI_CS_N	ah35	VSS
b36	VDDX	r36	SPI_SCK	ah36	DO NOT CONNECT
b37	P04_TBN	r37	SPI_SI	ah37	VDDX
b38	VTT04	r38	DO NOT CONNECT	ah38	DO NOT CONNECT
b39	P04_TAN	r39	DO NOT CONNECT	ah39	VSS
c1	VSS	t1	VSS	aj1	DO NOT CONNECT
c2	VDDX	t2	VDDX	aj2	VSS
c3	VDDX	t3	VDDA	aj3	DO NOT CONNECT
c4	VDDA	t4	RREF24	aj4	VSS
c5	VDDX	t5	VSS	aj5	DO NOT CONNECT
c6	VDDX	t6	VSS	aj6	VSS
c7	VSS	t7	VSS	aj7	DO NOT CONNECT
c8	VSS	t8	VDDX	aj8	VDD
c9	VSS	t9	DO NOT CONNECT	aj9	DO NOT CONNECT
c10	VDDX	t10	DO NOT CONNECT	aj10	VSS
c11	VDDX	t11	VSS	aj11	DO NOT CONNECT
c12	VDDA	t12	NO BALL	aj12	VSS
c13	VDDX	t13	NO BALL	aj13	DO NOT CONNECT
c14	VDDX	t14	VDD	aj14	VSS
c15	VSS	t15	VDD	aj15	DO NOT CONNECT
c16	VSS	t16	VDD	aj16	VDD
c17	VSS	t17	VDD	aj17	DO NOT CONNECT
c18	VDDX	t18	VDD	aj18	VSS
c19	VDDX	t19	VDD	aj19	DO NOT CONNECT
c20	VDDA	t20	VDD	aj20	VSS
c21	VDDX	t21	VDD	aj21	DO NOT CONNECT
c22	VDDX	t22	VDD	aj22	VSS
c23	VSS	t23	VDD	aj23	DO NOT CONNECT
c24	VSS	t24	VDD	aj24	VDD
c25	VSS	t25	VDD	aj25	DO NOT CONNECT
c26	VDDX	t26	VDD	aj26	VSS
c27	VDDX	t27	NO BALL	aj27	DO NOT CONNECT
c28	VDDA	t28	NO BALL	aj28	VSS
c29	VDDX	t29	LED_DATA1	aj29	DO NOT CONNECT
c30	VDDX	t30	DO NOT CONNECT	aj30	VSS
c31	VSS	t31	TESTMODE	aj31	DO NOT CONNECT
c32	VSS	t32	ADDR[2]	aj32	VDD

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
c33	VSS	t33	ADDR[3]	aj33	DIODE_OUT
c34	VDDX	t34	ADDR[4]	aj34	VDD
c35	VDDX	t35	ADDR[5]	aj35	DO NOT CONNECT
c36	VDDA	t36	ADDR[6]	aj36	DO NOT CONNECT
c37	VDDX	t37	ADDR[7]	aj37	VDDX
c38	VDDX	t38	ADDR[8]	aj38	DO NOT CONNECT
c39	VSS	t39	ADDR[9]	aj39	DO NOT CONNECT
d1	P20_RDP	u1	P24_TCP	ak1	DO NOT CONNECT
d2	VTT20	u2	P24_TCN	ak2	DO NOT CONNECT
d3	P20_RCP	u3	VDDX	ak3	DO NOT CONNECT
d4	RREF20	u4	P24_RCP	ak4	DO NOT CONNECT
d5	P20_RBP	u5	P24_RCN	ak5	DO NOT CONNECT
d6	VTT20	u6	VSS	ak6	DO NOT CONNECT
d7	P20_RAP	u7	DO NOT CONNECT	ak7	DO NOT CONNECT
d8	VDD	u8	DO NOT CONNECT	ak8	VDD
d9	P14_RDP	u9	VDDX	ak9	DO NOT CONNECT
d10	VTT14	u10	DO NOT CONNECT	ak10	DO NOT CONNECT
d11	P14_RCP	u11	DO NOT CONNECT	ak11	DO NOT CONNECT
d12	RREF14	u12	NO BALL	ak12	DO NOT CONNECT
d13	P14_RBP	u13	NO BALL	ak13	DO NOT CONNECT
d14	VTT14	u14	VDD	ak14	DO NOT CONNECT
d15	P14_RAP	u15	VDD	ak15	DO NOT CONNECT
d16	VDD	u16	VDD	ak16	VDD
d17	P12_RDP	u17	VDD	ak17	DO NOT CONNECT
d18	VTT12	u18	VDD	ak18	DO NOT CONNECT
d19	P12_RCP	u19	VDD	ak19	DO NOT CONNECT
d20	RREF12	u20	VDD	ak20	DO NOT CONNECT
d21	P12_RBP	u21	VDD	ak21	DO NOT CONNECT
d22	VTT12	u22	VDD	ak22	DO NOT CONNECT
d23	P12_RAP	u23	VDD	ak23	DO NOT CONNECT
d24	VDD	u24	VDD	ak24	VDD
d25	P08_RDP	u25	VDD	ak25	DO NOT CONNECT
d26	VTT08	u26	VDD	ak26	DO NOT CONNECT
d27	P08_RCP	u27	NO BALL	ak27	DO NOT CONNECT
d28	RREF08	u28	NO BALL	ak28	DO NOT CONNECT
d29	P08_RBP	u29	LED_DATA2	ak29	DO NOT CONNECT
d30	VTT08	u30	DTACK_N	ak30	DO NOT CONNECT
d31	P08_RAP	u31	ADDR[10]	ak31	DO NOT CONNECT
d32	VDD	u32	ADDR[11]	ak32	VDD
d33	P04_RDP	u33	ADDR[12]	ak33	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
d34	VTT04	u34	ADDR[13]	ak34	VDD
d35	P04_RCP	u35	ADDR[14]	ak35	VSS
d36	RREF04	u36	ADDR[15]	ak36	DO NOT CONNECT
d37	P04_RBP	u37	ADDR[16]	ak37	DO NOT CONNECT
d38	VTT04	u38	ADDR[17]	ak38	VDDX
d39	P04_RAP	u39	ADDR[18]	ak39	VSS
e1	P20_RDN	v1	VSS	al1	VSS
e2	VSS	v2	VTT24	al2	VDDX
e3	P20_RCN	v3	VDDX	al3	VDDX
e4	VSS	v4	VTT24	al4	DO NOT CONNECT
e5	P20_RBN	v5	VSS	al5	VDDX
e6	VSS	v6	VSS	al6	VDDX
e7	P20_RAN	v7	VSS	al7	VSS
e8	VDD	v8	DO NOT CONNECT	al8	VSS
e9	P14_RDN	v9	VDDX	al9	VSS
e10	VSS	v10	DO NOT CONNECT	al10	VDDX
e11	P14_RCN	v11	VSS	al11	VDDX
e12	VSS	v12	NO BALL	al12	DO NOT CONNECT
e13	P14_RBN	v13	NO BALL	al13	VDDX
e14	VSS	v14	VSS	al14	VDDX
e15	P14_RAN	v15	VSS	al15	VSS
e16	VDD	v16	VSS	al16	VSS
e17	P12_RDN	v17	VSS	al17	VSS
e18	VSS	v18	VSS	al18	VDDX
e19	P12_RCN	v19	VSS	al19	VDDX
e20	VSS	v20	VSS	al20	DO NOT CONNECT
e21	P12_RBN	v21	VSS	al21	VDDX
e22	VSS	v22	VSS	al22	VDDX
e23	P12_RAN	v23	VSS	al23	VSS
e24	VDD	v24	VSS	al24	VSS
e25	P08_RDN	v25	VSS	al25	VSS
e26	VSS	v26	VSS	al26	VDDX
e27	P08_RCN	v27	NO BALL	al27	VDDX
e28	VSS	v28	NO BALL	al28	DO NOT CONNECT
e29	P08_RBN	v29	LED_EN	al29	VDDX
e30	VSS	v30	DERR_N	al30	VDDX
e31	P08_RAN	v31	DO NOT CONNECT	al31	VSS
e32	VDD	v32	DO NOT CONNECT	al32	VSS
e33	P04_RDN	v33	ADDR[19]	al33	VSS
e34	VSS	v34	ADDR[20]	al34	VDD

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
e35	P04_RCN	v35	ADDR[21]	al35	DO NOT CONNECT
e36	VSS	v36	ADDR[22]	al36	DO NOT CONNECT
e37	P04_RBN	v37	ADDR[23]	al37	VDDX
e38	VSS	v38	VSS	al38	DO NOT CONNECT
e39	P04_RAN	v39	VSS	al39	DO NOT CONNECT
f1	VSS	w1	P24_TDP	am1	DO NOT CONNECT
f2	VSS	w2	P24_TDN	am2	DO NOT CONNECT
f3	VSS	w3	VSS	am3	DO NOT CONNECT
f4	VDD	w4	P24_RDP	am4	VDDX
f5	VDD	w5	P24_RDN	am5	DO NOT CONNECT
f6	VDD	w6	VDD	am6	DO NOT CONNECT
f7	VDD	w7	DO NOT CONNECT	am7	DO NOT CONNECT
f8	VDD	w8	DO NOT CONNECT	am8	VSS
f9	VDD	w9	VSS	am9	DO NOT CONNECT
f10	VSS	w10	DO NOT CONNECT	am10	DO NOT CONNECT
f11	VSS	w11	DO NOT CONNECT	am11	DO NOT CONNECT
f12	VSS	w12	NO BALL	am12	VDDX
f13	VSS	w13	NO BALL	am13	DO NOT CONNECT
f14	VSS	w14	VSS	am14	DO NOT CONNECT
f15	VDD	w15	VSS	am15	DO NOT CONNECT
f16	VDD	w16	VSS	am16	VSS
f17	VDD	w17	VSS	am17	DO NOT CONNECT
f18	VSS	w18	VSS	am18	DO NOT CONNECT
f19	VSS	w19	VSS	am19	DO NOT CONNECT
f20	VSS	w20	VSS	am20	VDDX
f21	VSS	w21	VSS	am21	DO NOT CONNECT
f22	VSS	w22	VSS	am22	DO NOT CONNECT
f23	VDD	w23	VSS	am23	DO NOT CONNECT
f24	VDD	w24	VSS	am24	VSS
f25	VDD	w25	VDD33	am25	DO NOT CONNECT
f26	VSS	w26	VDD33	am26	DO NOT CONNECT
f27	VSS	w27	NO BALL	am27	DO NOT CONNECT
f28	VSS	w28	NO BALL	am28	VDDX
f29	VSS	w29	VSS	am29	DO NOT CONNECT
f30	VSS	w30	VSS	am30	DO NOT CONNECT
f31	VDD	w31	VSS	am31	DO NOT CONNECT
f32	VDD	w32	DO NOT CONNECT	am32	VSS
f33	VDD	w33	IGN_PAR	am33	VSS
f34	VDD	w34	CS_N	am34	VDD
f35	VDD	w35	AS_N	am35	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
f36	VDD	w36	INTR_N	am36	DO NOT CONNECT
f37	VSS	w37	AUTOBOOT	am37	VDDX
f38	VSS	w38	VDD33	am38	DO NOT CONNECT
f39	VSS	w39	VDD33	am39	VSS
g1	DO NOT CONNECT	y1	VSS	an1	DO NOT CONNECT
g2	VSS	y2	VSS	an2	VSS
g3	DO NOT CONNECT	y3	VSS	an3	DO NOT CONNECT
g4	VSS	y4	VDD	an4	VSS
g5	DO NOT CONNECT	y5	VDD	an5	DO NOT CONNECT
g6	VSS	y6	VDD	an6	VSS
g7	DO NOT CONNECT	y7	VSS	an7	DO NOT CONNECT
g8	VSS	y8	VSS	an8	VSS
g9	DO NOT CONNECT	y9	VSS	an9	DO NOT CONNECT
g10	VSS	y10	VSS	an10	VSS
g11	DO NOT CONNECT	y11	VSS	an11	DO NOT CONNECT
g12	VSS	y12	NO BALL	an12	VSS
g13	DO NOT CONNECT	y13	NO BALL	an13	DO NOT CONNECT
g14	VSS	y14	VDD	an14	VSS
g15	DO NOT CONNECT	y15	VDD	an15	DO NOT CONNECT
g16	VSS	y16	VDD	an16	VSS
g17	DO NOT CONNECT	y17	VDD	an17	DO NOT CONNECT
g18	VSS	y18	VDD	an18	VSS
g19	DO NOT CONNECT	y19	VSS	an19	DO NOT CONNECT
g20	VSS	y20	VSS	an20	VSS
g21	DO NOT CONNECT	y21	VSS	an21	DO NOT CONNECT
g22	VSS	y22	VDD	an22	VSS
g23	DO NOT CONNECT	y23	VDD	an23	DO NOT CONNECT
g24	VSS	y24	VDD	an24	VSS
g25	DO NOT CONNECT	y25	VDD33	an25	DO NOT CONNECT
g26	VSS	y26	VDD33	an26	VSS
g27	DO NOT CONNECT	y27	NO BALL	an27	DO NOT CONNECT
g28	VSS	y28	NO BALL	an28	VSS
g29	DO NOT CONNECT	y29	VSS	an29	DO NOT CONNECT
g30	VSS	y30	CPU_RESET_N	an30	VSS
g31	DO NOT CONNECT	y31	VSS	an31	DO NOT CONNECT
g32	VSS	y32	DO NOT CONNECT	an32	VSS
g33	VSS	y33	RXRDY	an33	VSS
g34	VDD	y34	TXRDY_N	an34	VDD
g35	DO NOT CONNECT	y35	RXEOT	an35	DO NOT CONNECT
g36	DO NOT CONNECT	y36	RW_N	an36	DO NOT CONNECT

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
g37	VSS	y37	CLK_CPU	an37	VSS
g38	DO NOT CONNECT	y38	VDD33	an38	DO NOT CONNECT
g39	DO NOT CONNECT	y39	VDD33	an39	DO NOT CONNECT
h1	DO NOT CONNECT	aa1	P23_TAP	ap1	VSS
h2	DO NOT CONNECT	aa2	P23_TAN	ap2	VSS
h3	DO NOT CONNECT	aa3	VSS	ap3	VSS
h4	VDDX	aa4	P23_RAP	ap4	VDD
h5	DO NOT CONNECT	aa5	P23_RAN	ap5	VDD
h6	DO NOT CONNECT	aa6	VDD	ap6	VDD
h7	DO NOT CONNECT	aa7	DO NOT CONNECT	ap7	VDD
h8	VSS	aa8	DO NOT CONNECT	ap8	VDD
h9	DO NOT CONNECT	aa9	VSS	ap9	VDD
h10	DO NOT CONNECT	aa10	DO NOT CONNECT	ap10	VSS
h11	DO NOT CONNECT	aa11	DO NOT CONNECT	ap11	VSS
h12	VDDX	aa12	NO BALL	ap12	VSS
h13	DO NOT CONNECT	aa13	NO BALL	ap13	VSS
h14	DO NOT CONNECT	aa14	VSS	ap14	VSS
h15	DO NOT CONNECT	aa15	VSS	ap15	VDD
h16	VSS	aa16	VSS	ap16	VDD
h17	DO NOT CONNECT	aa17	VSS	ap17	VDD
h18	DO NOT CONNECT	aa18	VSS	ap18	VSS
h19	DO NOT CONNECT	aa19	VSS	ap19	VSS
h20	VDDX	aa20	VSS	ap20	VSS
h21	DO NOT CONNECT	aa21	VSS	ap21	VSS
h22	DO NOT CONNECT	aa22	VSS	ap22	VSS
h23	DO NOT CONNECT	aa23	VSS	ap23	VDD
h24	VSS	aa24	VSS	ap24	VDD
h25	DO NOT CONNECT	aa25	VDD33	ap25	VDD
h26	DO NOT CONNECT	aa26	VDD33	ap26	VSS
h27	DO NOT CONNECT	aa27	NO BALL	ap27	VSS
h28	VDDX	aa28	NO BALL	ap28	VSS
h29	DO NOT CONNECT	aa29	VSS	ap29	VSS
h30	DO NOT CONNECT	aa30	VSS	ap30	VSS
h31	DO NOT CONNECT	aa31	VSS	ap31	VDD
h32	VSS	aa32	DO NOT CONNECT	ap32	VDD
h33	VSS	aa33	DTACK_INV	ap33	VDD
h34	VDD	aa34	PAR[0]	ap34	VDD
h35	VSS	aa35	PAR[1]	ap35	VDD
h36	DO NOT CONNECT	aa36	PAR[2]	ap36	VDD
h37	VDDX	aa37	PAR[3]	ap37	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
h38	DO NOT CONNECT	aa38	VDD33	ap38	VSS
h39	VSS	aa39	VDD33	ap39	VSS
j1	VSS	ab1	VSS	ar1	P19_RAN
j2	VDDX	ab2	VTT23	ar2	VSS
j3	VDDX	ab3	VDDX	ar3	P19_RBN
j4	DO NOT CONNECT	ab4	VTT23	ar4	VSS
j5	VDDX	ab5	VSS	ar5	P19_RCN
j6	VDDX	ab6	VSS	ar6	VSS
j7	VSS	ab7	VSS	ar7	P19_RDN
j8	VSS	ab8	DO NOT CONNECT	ar8	VDD
j9	VSS	ab9	VDDX	ar9	P13_RAN
j10	VDDX	ab10	DO NOT CONNECT	ar10	VSS
j11	VDDX	ab11	VSS	ar11	P13_RBN
j12	DO NOT CONNECT	ab12	NO BALL	ar12	VSS
j13	VDDX	ab13	NO BALL	ar13	P13_RCN
j14	VDDX	ab14	VSS	ar14	VSS
j15	VSS	ab15	VSS	ar15	P13_RDN
j16	VSS	ab16	VSS	ar16	VDD
j17	VSS	ab17	VSS	ar17	P11_RAN
j18	VDDX	ab18	VSS	ar18	VSS
j19	VDDX	ab19	VSS	ar19	P11_RBN
j20	DO NOT CONNECT	ab20	VSS	ar20	VSS
j21	VDDX	ab21	VSS	ar21	P11_RCN
j22	VDDX	ab22	VSS	ar22	VSS
j23	VSS	ab23	VSS	ar23	P11_RDN
j24	VSS	ab24	VSS	ar24	VDD
j25	VSS	ab25	VSS	ar25	P07_RAN
j26	VDDX	ab26	VSS	ar26	VSS
j27	VDDX	ab27	NO BALL	ar27	P07_RBN
j28	DO NOT CONNECT	ab28	NO BALL	ar28	VSS
j29	VDDX	ab29	VDDA33	ar29	P07_RCN
j30	VDDX	ab30	TDI	ar30	VSS
j31	VSS	ab31	DO NOT CONNECT	ar31	P07_RDN
j32	VSS	ab32	DO NOT CONNECT	ar32	VDD
j33	VSS	ab33	DATA[0]	ar33	P03_RAN
j34	VDD	ab34	DATA[1]	ar34	VSS
j35	DO NOT CONNECT	ab35	DATA[2]	ar35	P03_RBN
j36	DO NOT CONNECT	ab36	DATA[3]	ar36	VSS
j37	VDDX	ab37	DATA[4]	ar37	P03_RCN
j38	DO NOT CONNECT	ab38	VSS	ar38	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
j39	DO NOT CONNECT	ab39	VSS	ar39	P03_RDN
k1	DO NOT CONNECT	ac1	P23_TBP	at1	P19_RAP
k2	DO NOT CONNECT	ac2	P23_TBN	at2	VTT19
k3	DO NOT CONNECT	ac3	VDDX	at3	P19_RBP
k4	DO NOT CONNECT	ac4	P23_RBP	at4	RREF19
k5	DO NOT CONNECT	ac5	P23_RBN	at5	P19_RCP
k6	DO NOT CONNECT	ac6	VSS	at6	VTT19
k7	DO NOT CONNECT	ac7	DO NOT CONNECT	at7	P19_RDP
k8	VDD	ac8	DO NOT CONNECT	at8	VDD
k9	DO NOT CONNECT	ac9	VDDX	at9	P13_RAP
k10	DO NOT CONNECT	ac10	DO NOT CONNECT	at10	VTT13
k11	DO NOT CONNECT	ac11	DO NOT CONNECT	at11	P13_RBP
k12	DO NOT CONNECT	ac12	NO BALL	at12	RREF13
k13	DO NOT CONNECT	ac13	NO BALL	at13	P13_RCP
k14	DO NOT CONNECT	ac14	VDD	at14	VTT13
k15	DO NOT CONNECT	ac15	VDD	at15	P13_RDP
k16	VDD	ac16	VDD	at16	VDD
k17	DO NOT CONNECT	ac17	VDD	at17	P11_RAP
k18	DO NOT CONNECT	ac18	VDD	at18	VTT11
k19	DO NOT CONNECT	ac19	VDD	at19	P11_RBP
k20	DO NOT CONNECT	ac20	VDD	at20	RREF11
k21	DO NOT CONNECT	ac21	VDD	at21	P11_RCP
k22	DO NOT CONNECT	ac22	VDD	at22	VTT11
k23	DO NOT CONNECT	ac23	VDD	at23	P11_RDP
k24	VDD	ac24	VDD	at24	VDD
k25	DO NOT CONNECT	ac25	VDD	at25	P07_RAP
k26	DO NOT CONNECT	ac26	VDD	at26	VTT07
k27	DO NOT CONNECT	ac27	NO BALL	at27	P07_RBP
k28	DO NOT CONNECT	ac28	NO BALL	at28	RREF07
k29	DO NOT CONNECT	ac29	RW_INV	at29	P07_RCP
k30	DO NOT CONNECT	ac30	TCK	at30	VTT07
k31	DO NOT CONNECT	ac31	DATA[5]	at31	P07_RDP
k32	VDD	ac32	DATA[6]	at32	VDD
k33	VSS	ac33	DATA[7]	at33	P03_RAP
k34	VDD	ac34	DATA[8]	at34	VTT03
k35	VSS	ac35	DATA[9]	at35	P03_RBP
k36	DO NOT CONNECT	ac36	DATA[10]	at36	RREF03
k37	DO NOT CONNECT	ac37	DATA[11]	at37	P03_RCP
k38	VDDX	ac38	DATA[12]	at38	VTT03
k39	VSS	ac39	DATA[13]	at39	P03_RDP

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
l1	DO NOT CONNECT	ad1	VSS	au1	VSS
l2	VSS	ad2	VDDX	au2	VDDX
l3	DO NOT CONNECT	ad3	VDDA	au3	VDDX
l4	VSS	ad4	RREF23	au4	VDDA
l5	DO NOT CONNECT	ad5	VSS	au5	VDDX
l6	VSS	ad6	VSS	au6	VDDX
l7	DO NOT CONNECT	ad7	VSS	au7	VSS
l8	VDD	ad8	VDDX	au8	VSS
l9	DO NOT CONNECT	ad9	DO NOT CONNECT	au9	VSS
l10	VSS	ad10	DO NOT CONNECT	au10	VDDX
l11	DO NOT CONNECT	ad11	VSS	au11	VDDX
l12	VSS	ad12	NO BALL	au12	VDDA
l13	DO NOT CONNECT	ad13	NO BALL	au13	VDDX
l14	VSS	ad14	VDD	au14	VDDX
l15	DO NOT CONNECT	ad15	VDD	au15	VSS
l16	VDD	ad16	VDD	au16	VSS
l17	DO NOT CONNECT	ad17	VDD	au17	VSS
l18	VSS	ad18	VDD	au18	VDDX
l19	DO NOT CONNECT	ad19	VDD	au19	VDDX
l20	VSS	ad20	VDD	au20	VDDA
l21	DO NOT CONNECT	ad21	VDD	au21	VDDX
l22	VSS	ad22	VDD	au22	VDDX
l23	DO NOT CONNECT	ad23	VDD	au23	VSS
l24	VDD	ad24	VDD	au24	VSS
l25	DO NOT CONNECT	ad25	VDD	au25	VSS
l26	VSS	ad26	VDD	au26	VDDX
l27	DO NOT CONNECT	ad27	NO BALL	au27	VDDX
l28	VSS	ad28	NO BALL	au28	VDDA
l29	DO NOT CONNECT	ad29	FH_PLL_CLKOUT	au29	VDDX
l30	VSS	ad30	TRST_N	au30	VDDX
l31	DO NOT CONNECT	ad31	DATA[14]	au31	VSS
l32	VDD	ad32	DATA[15]	au32	VSS
l33	VSS	ad33	DATA[16]	au33	VSS
l34	VDD	ad34	DATA[17]	au34	VDDX
l35	DO NOT CONNECT	ad35	DATA[18]	au35	VDDX
l36	DO NOT CONNECT	ad36	DATA[19]	au36	VDDA
l37	VDDX	ad37	DATA[20]	au37	VDDX
l38	DO NOT CONNECT	ad38	DATA[21]	au38	VDDX
l39	DO NOT CONNECT	ad39	DATA[22]	au39	VSS
m1	VSS	ae1	P23_TCP	av1	P19_TAN

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
m2	VSS	ae2	P23_TCN	av2	VTT19
m3	VSS	ae3	VDDX	av3	P19_TBN
m4	VDD	ae4	P23_RCP	av4	VDDX
m5	VDD	ae5	P23_RCN	av5	P19_TCN
m6	VDD	ae6	VSS	av6	VTT19
m7	VDD	ae7	DO NOT CONNECT	av7	P19_TDN
m8	VDD	ae8	DO NOT CONNECT	av8	VSS
m9	VDD	ae9	VDDX	av9	P13_TAN
m10	VDD	ae10	DO NOT CONNECT	av10	VTT13
m11	VDD	ae11	DO NOT CONNECT	av11	P13_TBN
m12	VSS	ae12	NO BALL	av12	VDDX
m13	VSS	ae13	NO BALL	av13	P13_TCN
m14	VSS	ae14	VSS	av14	VTT13
m15	NO BALL	ae15	VSS	av15	P13_TDN
m16	NO BALL	ae16	VSS	av16	VSS
m17	NO BALL	ae17	VDD	av17	P11_TAN
m18	NO BALL	ae18	VDD	av18	VTT11
m19	NO BALL	ae19	VSS	av19	P11_TBN
m20	NO BALL	ae20	VSS	av20	VDDX
m21	NO BALL	ae21	VSS	av21	P11_TCN
m22	NO BALL	ae22	VDD	av22	VTT11
m23	NO BALL	ae23	VDD	av23	P11_TDN
m24	NO BALL	ae24	VSS	av24	VSS
m25	NO BALL	ae25	VSS	av25	P07_TAN
m26	VSS	ae26	VSS	av26	VTT07
m27	VSS	ae27	NO BALL	av27	P07_TBN
m28	VSS	ae28	NO BALL	av28	VDDX
m29	VSS	ae29	FH_PLL_REFCLK	av29	P07_TCN
m30	VSS	ae30	TMS	av30	VTT07
m31	VSS	ae31	DATA[23]	av31	P07_TDN
m32	VSS	ae32	DATA[24]	av32	VSS
m33	VSS	ae33	DATA[25]	av33	P03_TAN
m34	VSS	ae34	DATA[26]	av34	VTT03
m35	VSS	ae35	DATA[27]	av35	P03_TBN
m36	DO NOT CONNECT	ae36	DATA[28]	av36	VDDX
m37	VDDX	ae37	DATA[29]	av37	P03_TCN
m38	DO NOT CONNECT	ae38	DATA[30]	av38	VTT03
m39	VSS	ae39	DATA[31]	av39	P03_TDN
n1	P24_TAP	af1	VSS	aw1	P19_TAP
n2	P24_TAN	af2	VTT23	aw2	VSS

Table 71. Package Ball Assignments in Numerical Order (Continued)

Pkg Ball	Signal Name	Pkg Ball	Signal Name	Pkg Ball	Signal Name
n3	VSS	af3	VDDX	aw3	P19_TBP
n4	P24_RAP	af4	VTT23	aw4	VSS
n5	P24_RAN	af5	VSS	aw5	P19_TCP
n6	VDD	af6	VDD	aw6	VSS
n7	DO NOT CONNECT	af7	VSS	aw7	P19_TDP
n8	DO NOT CONNECT	af8	DO NOT CONNECT	aw8	VSS
n9	VSS	af9	VDDX	aw9	P13_TAP
n10	DO NOT CONNECT	af10	DO NOT CONNECT	aw10	VSS
n11	DO NOT CONNECT	af11	VSS	aw11	P13_TBP
n12	VDDX	af12	VDDX	aw12	VSS
n13	RCK4AP	af13	RCK3AP	aw13	P13_TCP
n14	RCK4BP	af14	RCK3BP	aw14	VSS
n15	NO BALL	af15	VSS	aw15	P13_TDP
n16	NO BALL	af16	VSS	aw16	VSS
n17	NO BALL	af17	VDD	aw17	P11_TAP
n18	NO BALL	af18	VDD	aw18	VSS
n19	NO BALL	af19	VSS	aw19	P11_TBP
n20	NO BALL	af20	VSS	aw20	VSS
n21	NO BALL	af21	VSS	aw21	P11_TCP
n22	NO BALL	af22	VDD	aw22	VSS
n23	NO BALL	af23	VDD	aw23	P11_TDP
n24	NO BALL	af24	VSS	aw24	VSS
n25	NO BALL	af25	VSS	aw25	P07_TAP
n26	RCK2BP	af26	RCK1BP	aw26	VSS
n27	RCK2AP	af27	RCK1AP	aw27	P07_TBP
n28	VDDX	af28	VDDX	aw28	VSS
n29	VSS	af29	DO NOT CONNECT	aw29	P07_TCP
n30	DO NOT CONNECT	af30	TDO	aw30	VSS
n31	CONT_EN	af31	DO NOT CONNECT	aw31	P07_TDP
n32	VSS	af32	DO NOT CONNECT	aw32	VSS
n33	CHIP_RESET_N	af33	DO NOT CONNECT	aw33	P03_TAP
n34	VSS	af34	VSS	aw34	VSS
n35	DO NOT CONNECT	af35	VSS	aw35	P03_TBP
n36	DO NOT CONNECT	af36	VSS	aw36	VSS
n37	VSS	af37	VSS	aw37	P03_TCP
n38	DO NOT CONNECT	af38	VSS	aw38	VSS
n39	DO NOT CONNECT	af39	VSS	aw39	P03_TDP

4.5 Power Dissipation and Heat Sinking

4.5.1 Power Dissipation

The power dissipation of the FM2212 is dependent on a number of different operational factors including:

- The number of ports in operation
- The operating rate of each port (10 Gbps, 2.5 Gbps, 1.0 Gbps, etc)
- The utilization factor of each port (the percentage of the bit stream that is actual data, vs. 8B/10B idle characters)
- The distribution of frame sizes
- SerDes drive strengths
- Use of the CPU interface
- Supply voltages
- Temperature

Though the dependencies above have a considerable effect on supply current draws and overall power dissipation, useful guidelines can be provided through measured data under two operating conditions. One condition consists of the most aggressive possible values for the parameters that have the most impact, namely utilization percentage and frame size. Other parameters such as SerDes drive strength, supply voltages and case temperatures are kept at nominal values. A second, more typical use model assumes more moderate values for frame sizes and utilization percentages, while keeping the other parameters at their nominal values. The test conditions and resulting current draws and overall power dissipation values are shown in Table 72 and Table 73.

Table 72. Conditions for Power Measurements

Parameter	Aggressive Case	Typical
Operating ports	20	20
Operating rate, all ports	10 Gbps	10 Gbps
Utilization factor	100%	50%
Frame size	64B	256B
SerDes drive parameters	Nominal	Nominal
CPU utilization	Not in use	Not in use
Supply voltages	Nominal	Nominal
Temperature, case	~60ºC	~60ºC
Frame handler clock	360 MHz	360 MHz

Table 73. FM2212 Currents and Power

	Power Supply Currents (A)			
	I_{DD}	I_{DDX}	I_{TT}	Total Power (W)
	(V_{DD}=1.2V)	(V_{DDX}=1.0V)	(V_{TT}=1.5V)	
Typical Use	8.65	3.05	1.3	15.4
Most Aggressive	14.0	3.05	1.3	21.8

Notes: (1) I_{DDA} is approximately 10 mA per port and is measured as a part of IDDX.

(2) V_{DDA33} is approximately 4 mA.

(3) V_{DD33} is used for the CPU interface and no current is drawn when not in use.

(4) Using V_{DDX} = 1.2V will raise power dissipations by up to 3.5W, depending on use parameters.

5.0 Document Revision Information

The following table lists the changes made to the FM2224 Datasheet resulting in the publication of a new revision.

5.1 Nomenclature

Document revisions are placed in either of two categories to allow the user to quickly focus on changes of a substantive nature (Category 1), that is, changes that may have an impact on system or board level design.

Category 1 changes are specification clarifications or changes and include modifications to the current published specifications, or describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications and changes will be incorporated in any new release of the specification or other affected document.

Category 2 changes are documentation changes and include corrections for typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

5.2 Rev 1.0 to 1.1 changes

	Page	Category		Description
		1	2	
1	15		X	Table 69: removed pin af30 from list of no-connect pins. It is TDO.
2	14	X		Table 62: Corrected RCK to port assignments for the 4 port groups.
3	15		X	Table 60: Add pin G23 to list of no-connects.

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