

# Intel® Celeron® M Processor 530

Addendum to Intel® Celeron® M Processor 500 Series for Mobile  
Intel® 945 Express Chipset Family Datasheet

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*August 2007*



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## Revision History

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Date	Revision	Description
August 2007	001	Initial release



## 1.0 Introduction

This document is an addendum to the Intel® Celeron® M Processor 500 Series for Mobile Intel® 945 Express Chipset Family Datasheet.

The purpose of this addendum is to document the mechanical packaging and thermal features specific to the Intel® Celeron M processor 530 and available only to Intel embedded customers. Please refer to the master Intel® Celeron M Processor 500 Series Datasheet for all other specifications relating to this processor.

In this document, the Intel® Celeron® M Processor 530 will be referred to as the processor.

The following list provides some of the key features of this processor:

- Supported by the Intel® 945 Express Chipset Family
- Single Core
- On-die, primary 32-kB instruction cache and 32-kB write-back data cache
- On-die, 1-MB second level shared cache with Advanced Transfer Cache Architecture
- 533-MHz Source-Synchronous Front Side Bus (FSB)
- Supports Intel Architecture with Dynamic Execution
- Data Prefetch Logic
- Supports both Micro-FCPGA and Micro-FCBGA packaging technology
- MMX, Streaming SIMD Extensions (SSE), Streaming SIMD Extensions 2 (SSE2), Streaming SIMD Extensions 3 (SSE3), and Supplemental Streaming SIMD Extensions 3 (SSSE3)
- Digital Thermal Sensor (DTS)
- Execute Disable Bit support for enhanced security
- Intel® 64 architecture (formerly Intel® EM64T)
- Architectural and performance enhancements to the Core micro-architecture.

*Note:* Intel® 64 requires a computer system with a processor, chipset, BIOS, operating system, device drivers and applications enabled for Intel 64. The processor will not operate (including 32-bit operation) without an Intel 64-enabled BIOS. Performance will vary depending on your hardware and software configurations. See <http://developer.intel.com/technology/architecture-silicon/intel64/> for more information including details on which processors support Intel 64 or consult with your system vendor for more information.

*Note:* Unless specified otherwise, all references to the processor in this document are references to the Intel Celeron M processor 530 with a 533-MHz FSB.



## 1.1 Terminology

Term	Definition
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the chipset components).
Intel® 64	64-bit memory extensions to the IA-32 architecture.
FCPGA	Micro flip-chip Pin Grid Array Package
FCBGA	Micro flip-chip Ball Grid Array Package

## 1.2 References

The following documents should be used as references for this document:

Document	Order Number <sup>1</sup>
<i>Intel® Celeron® M 500 Series For Mobile Intel® 945 Express Chipset Family Datasheet</i>	316205

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## 2.0 Package Mechanical Specifications Addendum

The processor is available in two packages: 478-pin Micro-FCPGA and 479-pin Micro-FCBGA. Package mechanical dimensions are shown in [Figure 1](#) through [Figure 4](#) and provide details on processor keep-out zones, package loading specifications, and processor mass specifications.

### 2.1 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted in the keep-out areas. The location and quantity of the capacitors may change but will remain within the component keep-in. See [Figure 2](#) and [Figure 4](#) for keep-out zones.

### 2.2 Package Loading Specifications

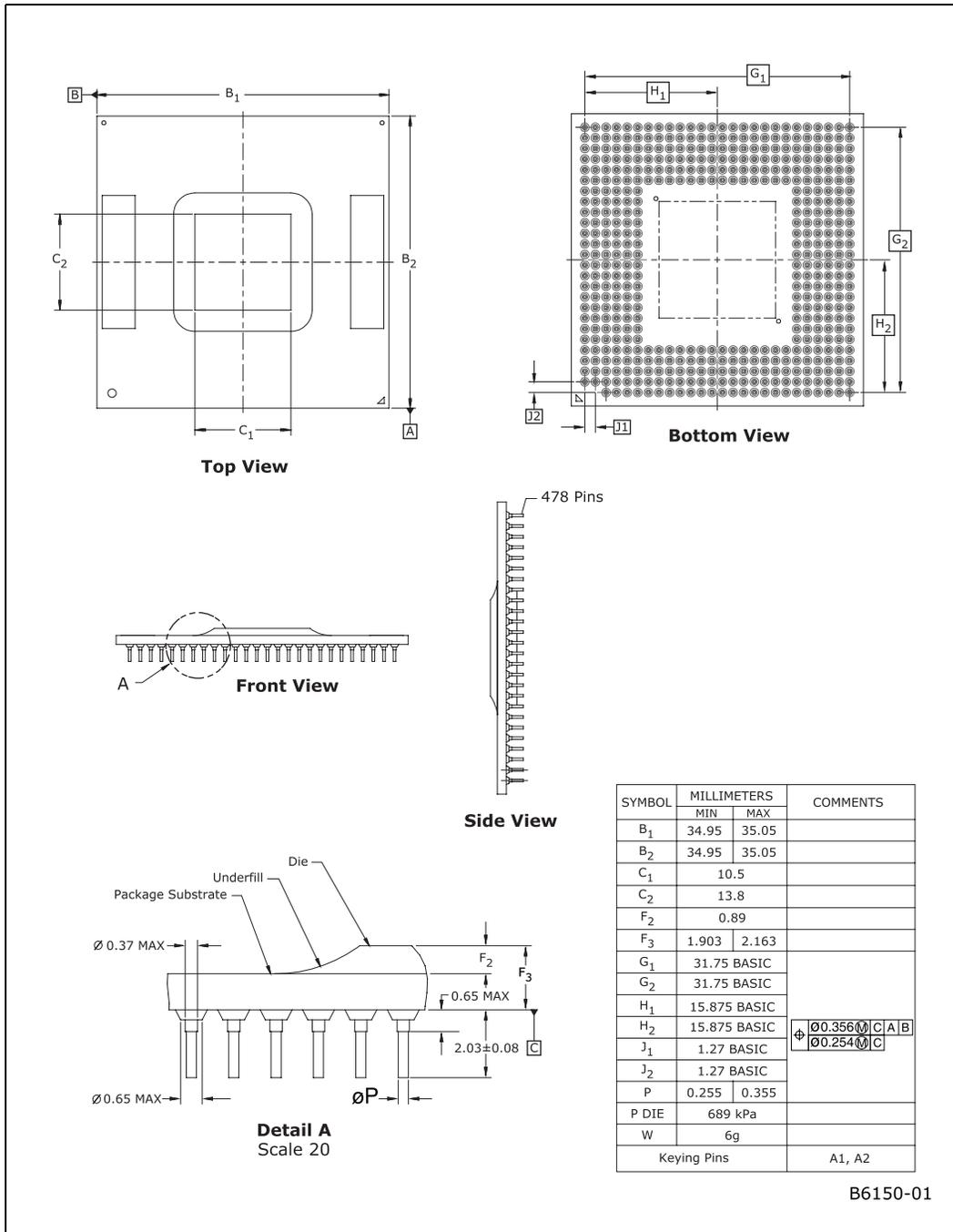
Maximum mechanical package loading specifications are given in [Figure 1](#) and [Figure 3](#) for the Micro-FCPGA and the Micro-FCBGA packages respectively. These specifications are static compressive loading in the direction normal to the processor. This maximum load limit should not be exceeded during shipping conditions, standard use condition, or by the thermal solution. In addition, there are additional load limitations against transient bend, shock, and tensile loading. These limitations are more platform specific and should be obtained by contacting your field support. Moreover, the processor package substrate should not be used as a mechanical reference or load-bearing surface for the thermal or mechanical solution.

### 2.3 Processor Mass Specifications

The typical mass of the Micro-FCPGA and the Micro-FCBGA packages are given in [Figure 1](#) and [Figure 3](#). This mass includes all the components that are included in the package.



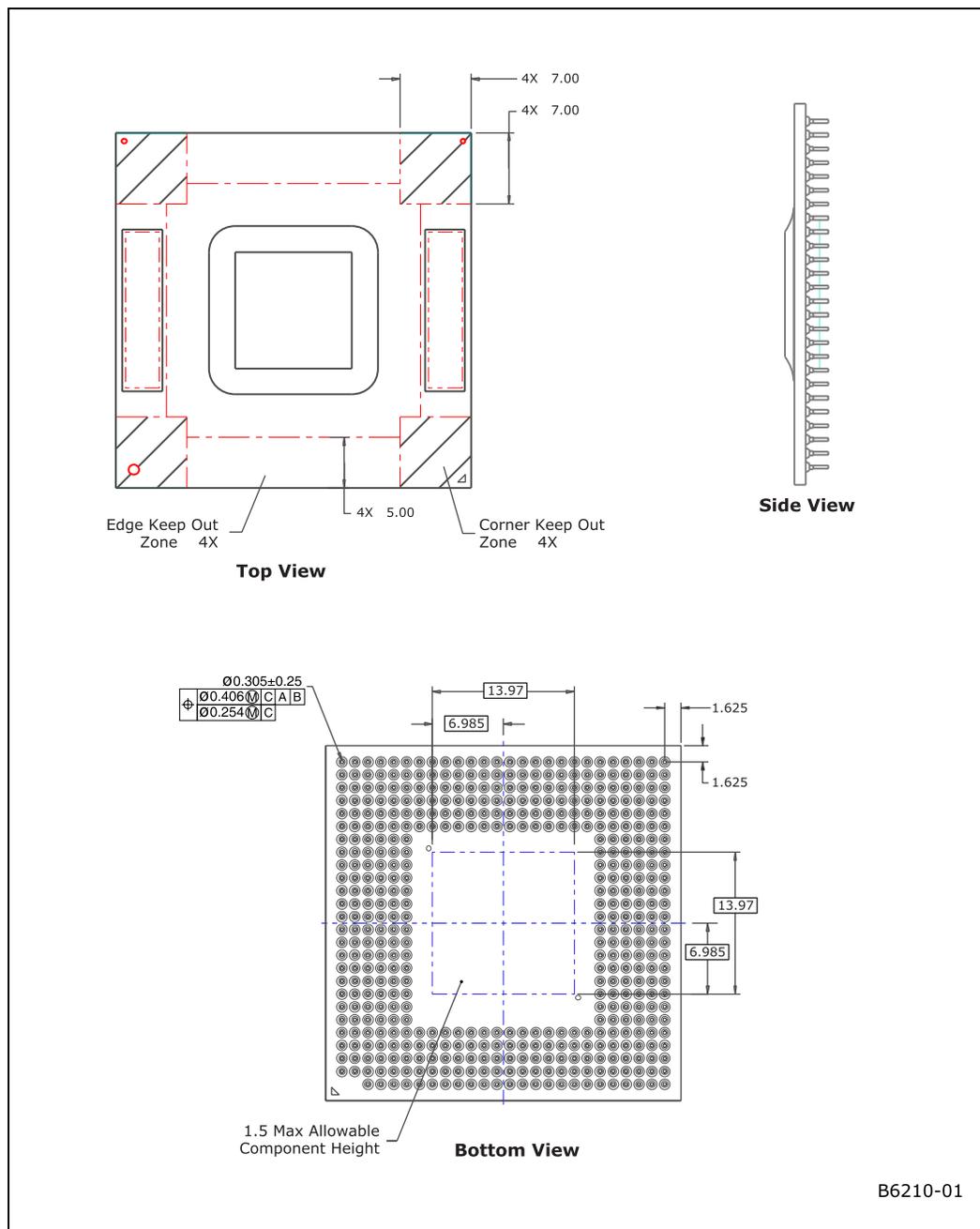
Figure 1. 1-MB Configuration Micro-FCPGA Processor Package Drawing (1 of 2)



B6150-01



Figure 2. 1-MB Configuration Micro-FCPGA Processor Package Drawing (2 of 2)



B6210-01



Figure 3. 1-MB Configuration Micro-FCBGA Processor Package Drawing (1 of 2)

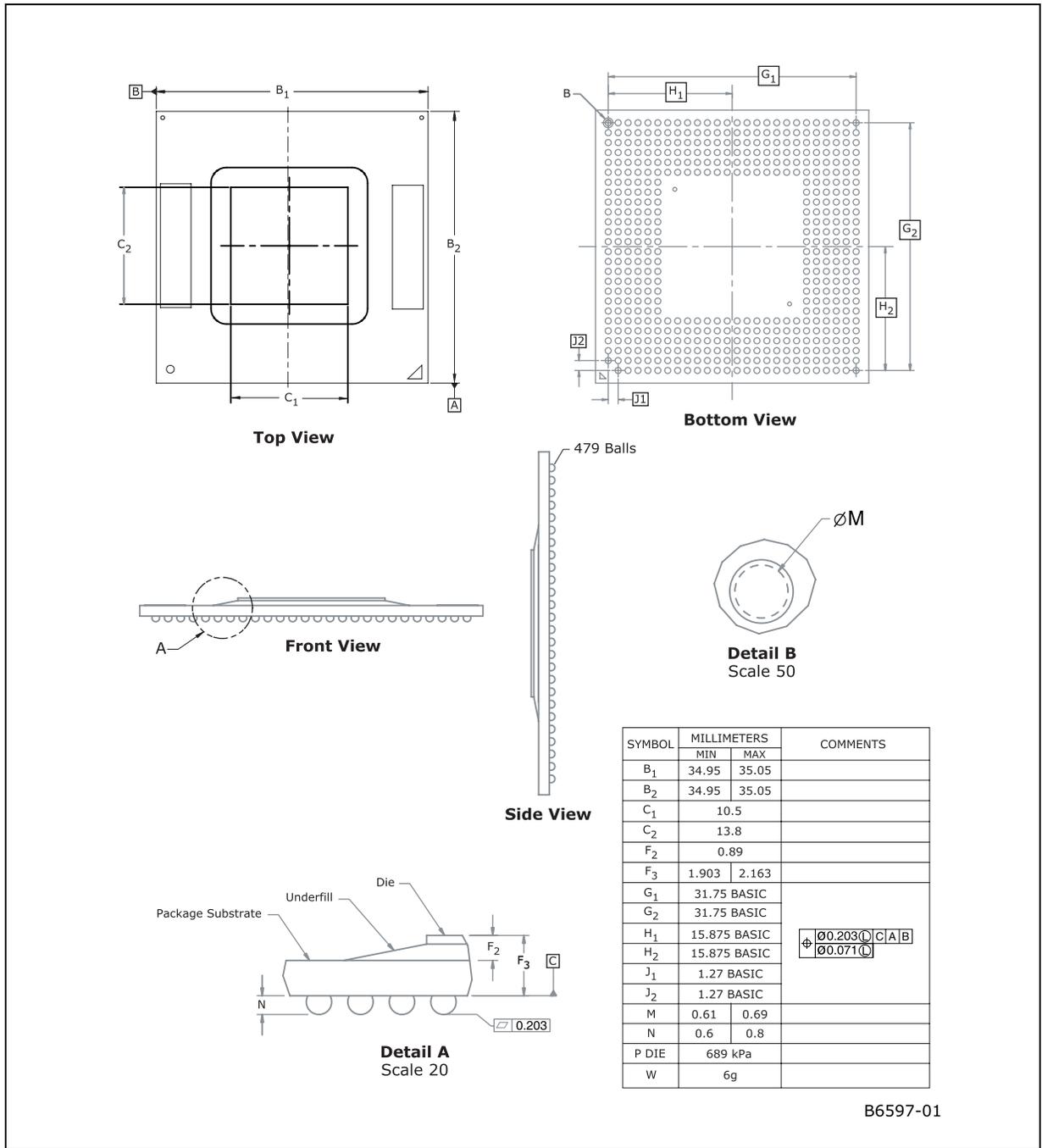
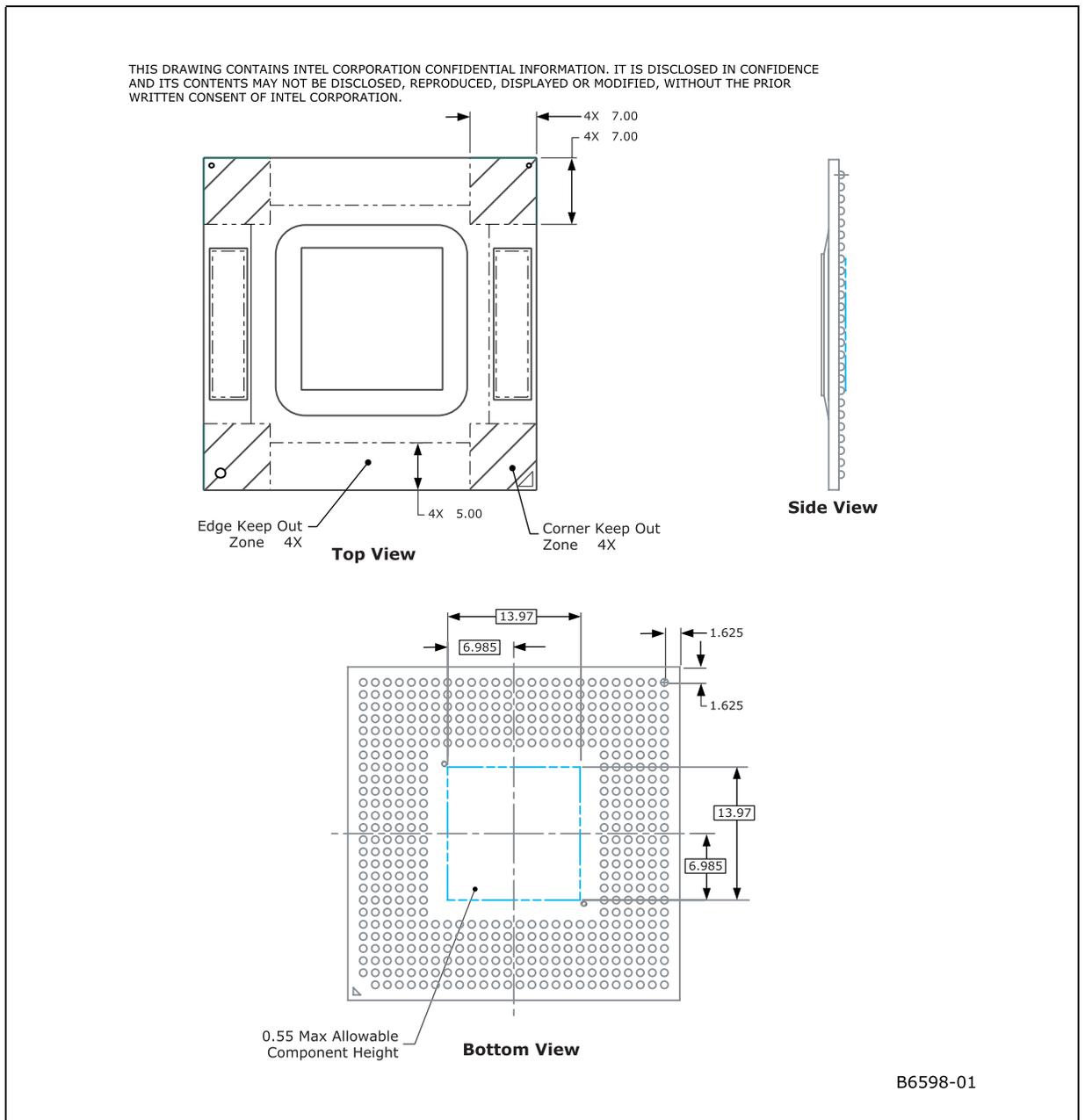




Figure 4. 1 MB Configuration Micro-FCBGA Processor Package Drawing (2 of 2)



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### 3.0 Thermal Specifications Addendum

A complete thermal solution includes both component and system level thermal management features. The processor requires a thermal solution to maintain temperatures within operating limits.

**Caution:** Any attempt to operate the processor outside operating limits may result in permanent damage to the processor and potentially other components in the system.

The system/processor thermal solution should remain within the minimum and maximum junction temperature (Tj) specifications at the corresponding thermal design power (TDP) value listed in Table 1.

**Table 1. Thermal Specifications**

Symbol	Processor Number	Core Frequency & Voltage	Die Variant	Thermal Design Power	Unit	Notes
TDP	530	1.73GHz	1M Configuration	31	W	1,2,3,4

*Note:*

1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
3. At Tj at 100°C
4. The units will display processor family ID 06F6h

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