Intel® Atom™ Processor S1200 Product Family for Microserver

Datasheet, Volume 2 of 2

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Revision History

Date	Revision	Description
November 2012	1.0	Initial Release..

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No Figures Used At This Time

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1 Introduction

The Intel® Atom™ Processor S1200 Product Family for Microserver is the new generation of System-On-Chip (SoC) 64-bit processor; dual-core processors built on 32-nanometer process technology. Throughout this document, the Intel® Atom™ Processor S1200 Product Family for Microserver is also referred to as simply the processor or S12x0.

This document relates to the following products:

Table 1. Intel® Atom™ Processor S1200 Product Family

SKU Name	TDP
Intel® Atom™ Processor S1260	8.5W
Intel® Atom™ Processor S1240	6.3W
Intel® Atom™ Processor S1220	8.1W

1.1 Overview

Volume 2 of the S12x0 Datasheet documents the Configuration Status Registers (CSRs) of each functional block in the UnCore logic. This document is intended to be distributed as a part of the complete datasheet set. CSRs are the basic hardware elements that configure the uncore logic to support various system topologies, memory configuration and densities and all the hardware hooks required for RAS operations. The S12x0 makes no assumption about the programmed value into the CSRs, therefore proper operation requires accurate programming of the CSRs.

The S12x0 contains registers that are located in the processor I/O space and memory space and sets of PCI configuration registers that are located in PCI configuration space. This document describes the S12x0 I/O and memory maps at the register-set level. Register access is also described. Register-level address maps and Individual register bit descriptions are also provided.

1.2 Terminology

A '_N', '#', '_B', or 'B' symbol after a signal name refers to an active low signal indicating a signal is in the active state when driven to a low level. When RESETB, for example, is low, a reset has been requested.

Table 1-2. Terminology (Sheet 1 of 2)

Term	Description
DDR3	Third generation Double Data Rate SDRAM memory technology that is the successor to DDR2 SDRAM
DMA	Direct Memory Access
ECC	Error Correction Code
Enhanced Intel SpeedStep® Technology	Allows the operating system to reduce power consumption when performance is not needed.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
IIO	The Integrated I/O Controller. An I/O controller that is integrated in the processor die.
iMC	The Integrated Memory Controller. A Memory Controller that is integrated in the processor die.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture. Further details on Intel 64 architecture and programming model can be found at http://developer.intel.com/technology/intel64/.
Intel® Virtualization Technology (Intel® VT)	Processor Virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
Integrated Heat Spreader (IHS)	A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Jitter	Any timing variation of a transition edge or edges from the defined Unit Interval (UI).
LLC	Last Level Cache
LRU	Least Recently Used. A term used in conjunction with cache hierarchy.
MLC	Mid Level Cache
PCODE	Power Management Unit micro-code
PMU	Power Management Unit
PCI Express*	PCI Express Generation 2
Processor	The 64-bit, single-core or multi-core component (package)
Processor Core	The term "processor core" refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 512-KB L2 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a DDR3 DIMM.
SSE	Intel® Streaming SIMD Extensions (Intel® SSE)
So-DIMM	Small outline Dual In-line Memory Module

Table 1-2. Terminology (Sheet 2 of 2)

Term	Description
SMBus	System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I2C* two-wire serial bus from NXP Semiconductors*.
TAC	Thermal Averaging Constant
TDP	Thermal Design Power
TSOD	Temperature Sensor On DIMM
UDIMM	Unbuffered Dual In-line Memory Module
Unit Interval	Signaling convention that is binary and unidirectional. In this binary signaling, one bit is sent for every edge of the forwarded clock, whether it be a rising edge or a falling edge. If a number of edges are collected at instances t_1, t_2, t_n,...., t_k then the UI at instance “n” is defined as: $UI_n = t_n - t_{n-1}$
V_{CC}	Processor core power supply
V_{SS}	Processor ground
V_{DDQ}	DDR3 power rail
x1	Refers to a Link or Port with one Physical Lane
x4	Refers to a Link or Port with four Physical Lanes
x8	Refers to a Link or Port with eight Physical Lanes

1.3 Related Documents

Refer to the following documents for additional information.

Table 1-3. Related Documents

Document†	Document Number/Location
Processor Documents	
Intel® Atom™ Processor S1200 Product Family for Microserver Datasheet, Volume 1 of 2	328194
Intel® Atom™ Processor S1200 Product Family for Microserver Thermal/Mechanical Design Guide (TMDG)	328196
Intel® Atom™ Processor S1200 Product Family for Microserver Boundary Scan Description Language (BSDL) File	328197
Intel® Atom™ Processor S1200 Product Family for MicroserverSpecification Update	328198
Public Specifications	
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info
PCI Local Bus Specification, Revision 3.0 (February 3, 2004) *PCI Local Bus Specification*, Revision 2.1 (November 18, 2010; plus Errata)	http://www.pcisig.com/specifications
PCI Express Base Specification, Revision 3.0 (November 10, 2010)	
PCI-to-PCI Bridge Architecture Specification, Revision 1.2 (June 9, 2003)	
PCI Bus Power Management Interface Specification, Revision 1.2 (March 3, 2004)	
DDR3 SDRAM Specification	http://www.jedec.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide Intel® 64 and IA-32 Architectures Optimization Reference Manual	http://www.intel.com/products/processor/manuals/index.htm

† Document may be Intel classified, or not be available at the time of this release; see the Intel representative.

1.4 State of Data

The data contained within this document is preliminary. It is the most accurate information available as of the publication date of this document. The information in this revision of the document is based on early simulation data. Values may change prior to production. Electrical AC/DC specifications are based on estimated I/O buffer behavior. Mechanical data is based on the final package.

1.5 Register Attribute Definitions

The bits in the configuration register descriptions have an assigned attribute, compliant to the RegEx design automation tool, made up of a Base Attribute from the first table below and possibly an Attribute Modifier from the second table below. The combined Attribute describes the basic behavior of the bits from a software interface point of view.

Table 1-4. Register Attribute Definitions

Attr	Description
RO	**Read Only:** These bits can only be read by software, writes have no affect. The value of the bits is determined by the hardware only.
RW	**Read / Write:** These bits can be read and written by software.
RW1C	**Read / Write 1 to Clear:** These bits can be read and cleared by software. Writing a 1 to a bit clears it, while writing a 0 to a bit has no affect. Hardware sets these bits.
WO	**Write Only:** These bits can only be written by software, reads return zero. ***Note:*** Use of this attribute type is deprecated and can only be used to describe bits without persistent state.
RC	**Read Clear:** These bits can only be read by software, but a read causes the bits to be cleared. Hardware sets these bits. ***Note:*** Use of this attribute type is only allowed on legacy functions, as side-effects on reads are not desirable.
RCW	**Read Clear / Write:** These bits can be read and written by software, but a read causes the bits to be cleared. ***Note:*** Use of this attribute type is only allowed on legacy functions, as side-effects on reads are not desirable.
RV	**Reserved:** These bits are reserved for future expansion and their value must not be modified by software. When writing these bits, software must preserve the value read. The bits are read-only must return 0 when read.

Attribute Modifiers specify additional information about the behavior of register bits when used in conjunction with applicable Base Attributes. Bits without a Sticky attribute modifier are set to their default value by a hard reset.

Table 1-5. Attribute Modifiers

Attribute Modifier	Applicable Attribute	Description
S	RO (w/ -V), RW, RW1C	**Sticky:** These bits are only reinitialized to their default value by a PWRGD reset. ***Note:*** Does not apply to RO (constant) bits.
-K	RW, WO	**Key:** These bits control the ability to write other bits (identified with a Lock modifier).
-L	RW, WO	**Lock:** Hardware can make these bits Read Only via a separate configuration bit or other logic. ***Note:*** Mutually exclusive with Once modifier.
-O	RW, WO	**Once:** After reset, these bits can only be written by software once, after which the bits becomes Read Only. ***Note:*** Mutually exclusive with Lock modifier and does not make sense with Variant or Restricted modifiers.
-R	RW	**Restricted:** On a write, the value of these bits may differ from what is provided by software. ***Note:*** The use of this modifier is limited to only where absolutely necessary.
-V	RO, RW	**Variant:** The value of these bits can be updated by hardware. ***Note:*** RW1C and RC bits are variant by definition and therefore do not need to be modified.

Modifiers without a leading dash are appended to the end of the Base Attribute for compatibility with industry specs. Modifiers with a leading dash are appended (in alphabetical order) after a single dash when more than one apply. Some Modifiers may be used together to accurately describe the register bit behavior.

If the reset domain is not specified in the attribute column, the register field is reinitialized to its default value on all reset types (PWRGD, Primary or Secondary).

Table 1-6. Re-Initializing Register Fields

Attribute	Description
S	**Sticky:** These bits are only reinitialized to their default value by a PWRGD reset.
PRST	**Primary Reset:** These bits are only reinitialized to their default value by a PWRGD or Primary reset signal. These bits are not reset on link down, hot reset, or secondary bus reset initiated from an upstream Bridge's BCTL Control Register.
FLR	**Function Level Reset:** These bits are reinitialized to their default value by on any reset including a Function Level Reset initiated from the function's EXPDEV Control Registers.
NFLRST	**Not Function Level Reset:** These bits are reinitialized to their default value by power good or warm reset but are not affected by a Function Level Reset initiated from the function's DEVCTL.IFLR register. These special bits are tagged with attribute NFLRST so that it is not reset when an FLR is invoked.

1.6 Register Bit Nomenclature

Register bits may be referred to simply by the defined register name or with 'RegisterName.RegisterBitName' in the register bit field descriptions.

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2 Configuration Process and Registers

2.1 Device Mapping

Each component in the processor is uniquely identified by a PCI bus address consisting of Bus Number, Device Number and Function Number. Device configuration is based on the PCI Type 0 configuration conventions. All processor registers appear on the PCI bus assigned for the processor socket. Bus number is derived by the maximum bus range setting and processor socket number.

All Bus, Device and Function numbers shown in this document are written as decimal numbers.

Table 2-1. Local PCI Hierarchy

Device Number, Function Number (Decimal)	Internal ID (Hexadecimal)	Integrated Device Name	Comments
D:0, F:0	0x0C7x	Internal	Used for SKU configuration: Intel® AtomTM Processor S1220 = 0x0C72 Intel® AtomTM Processor S1220 = 0x0C73 Intel® AtomTM Processor S1260 = 0x0C75
D:1, F:0	0x0C46	PCIe* Root Port 1	PCIe controller 0 of x8 RP unit 0
D:2, F:0	0x0C47	PCIe Root Port 2	PCIe controller 1 of x8 RP unit 0
D:3, F:0	0x0C48	PCIe Root Port 3	PCIe controller 2 of x8 RP unit 0
D:4, F:0	0x0C49	PCIe Root Port 4	PCIe controller 3 of x8 RP unit 0
D:14, F:0	0x0C54	Internal	Internal management.
D:15, F:0	0x0C55	DFX 1	Reserved for debug
D:16, F:0	0x0C56	DFX 2	Reserved for debug
D:19, F:0	0x0C59	SMBus 2.0 Controller 0	SMBD. SMBus for PCIe mass-storage devices
D:19, F:1	0x0C5A	SMBus 2.0 Controller 1	SMBM. SMBus for enclosure maintenance
D:19, F:2	0x0C5B	SMBus Controller 2	Allocated for future use
D:19, F:3	0x0C5C	SMBus Controller 3	Allocated for future use
D:19, F:4	0x0C5D	SMBus Controller 4	Allocated for future use
D:19, F:5	0x0C5E	SMBus Controller 5	Allocated for future use
D:20, F:0	0x0C5F	UART	Integrated High-Speed UART
D:31, F:0	0x0C60	ILB	Integrated PCI-to-ISA Bridge for Intel Legacy Block devices and LPC interface

2.2 Processor PCI Devices (CPUBUSNO(0))

The S12x0 contains PCI devices which are categorized as processor Integrated I/O (IIO) devices and Processor Uncore devices. The configuration registers for these devices are mapped as devices residing on PCI Bus CPUBUSNO(0), where CPUBUSNO(0) is programmable by BIOS. The PCIe* Gen 2 Root Ports, SMBus 2.0, HS-UART and Intel Legacy Block are S12x0 IIO devices. The integrated Memory Controller, RAS and Power Management Unit (PMU) are S12x0 Uncore devices. Some configuration registers for these devices may also be in the Memory Address Space and I/O Address Space.

- Device 1-4: x8 PCI Express Gen2 Root Port Unit. Device 1-4 Function 0 contains PCIe Controllers 0, 1, 2, and 3 of the x8 RP Unit 0 configuration registers.
- Device 14: Internal Management. Device 14 Function 0 contains Power Management and RAS configuration registers.
- Device 19: SMBus Message Transport (SMT). Device 19 Function 0-1 contains independent SMBus master/slave controller configuration registers.
- Device 20: Integrated HS-UART. Device 20 Function 0 contains registers for HS-UART configuration registers.
- Device 31: Integrated PCI-to-ISA Bridge for Intel Legacy Block devices and LPC interface. Device 31 Function 0 contains LPC 1.1 configuration registers.

2.3 Configuration Register Rules

2.3.1 PCI Configuration Space Registers (CSRs)

CSRs are control and status registers that are located in PCI defined address space.

2.3.2 CSR Access

Configuration space registers are accessed via the well known configuration transaction mechanism defined in the PCI specification. It uses the bus, device, and function number concept to address a specific device's configuration space.

All configuration register accesses are made over sideband signals through the internal SoC fabric, but might come from a variety of different sources:

- Local cores
- JTAG

This unit supports PCI configuration space access as defined in the *PCI Express Base Specification*, Revision 2.0. Configuration registers can be read or written in Byte, WORD (16-bit), or DWORD (32-bit) quantities. *Accesses larger than a DWORD to PCI Express configuration space results in unexpected behavior.* All multi-byte numeric fields use "little-endian" ordering (that is, lower addresses contain the least-significant parts of the field)

2.4 Configuration Mechanisms

The processor is the originator of configuration cycles. Internal to the processor, transactions received through both of the below configuration mechanisms are translated to the same format.

2.4.1 Standard PCI Express Configuration Mechanism

The following is the mechanism for translating processor I/O bus cycles to configuration cycles.

The PCI specification defines a slot based “configuration space” that allows each device to contain up to eight functions, with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the processor. Configuration space is supported by a mapping mechanism implemented within the processor.

The memory-mapped registers are accessible via memory transactions on the PCI Express interface or by local CPU. Their location is relative to the respective device BAR.

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3 Processor Integrated I/O (IIO) Registers

Table 3-1. Register Summary

Offset (h)	Size (bits)	Name
404	32	“HMBound (HMBOUND)”
408	32	“HMBound High (HMBOUNDHI)”
40C	32	“Bifurcation Control (BIFCTL)”

3.1 Fabric Registers

The S12x0 SoC Fabric (SOCF) implements the interconnect of all internal functional blocks. SOCF implements the bus 0 interconnect of a PCIe* Root Complex and is a software-visible PCIe function.

This section contains Fabric Register information.

Table 3-2. HMBound (HMBOUND)

SOCF_HMBOUND
Bus: 0 Device: 14 Function: 0 Offset: 404h

Bit	Attribute	Default	Description
31:27	RW-L	08h	**HMBound (HMBOUND):** 10_0000h <= address < HMBOUND route to memory. HMBOUND is compared to address[31:27], with all other address bits compared to 0.
26:1	RV	0h	Reserved
0	RW-KL	0b	**Lock**: When set, HMBOUND register is locked and can not be modified.

Table 3-3. HMBound High (HMBOUNDHI)

SOCF_HMBOUNDHI
Bus: 0 Device: 14 Function: 0 Offset: 408h

Bit	Attribute	Default	Description
31:28	RV	0h	Reserved
27:24	RW-L	8h	**HMBound High (HMBOUNDHI)**: 1_0000_0000h <= address < HMBOUNDHI route to memory. HMBOUND is compared to address[35:32], with all other address bits compared to 0.
23:1	RV	0h	Reserved
0	RW-KL	0b	**Lock**: When set, HMBOUNDHI register is locked and can not be modified.

Table 3-4. Bifurcation Control (BIFCTL) (Sheet 1 of 2)

RP_BIFCTL
Bus: 0 Device: 14 Function: 0 Offset: 40Ch

Bit	Attribute	Default	Description
31:17	RV	0b	Reserved
16	RW	0b	**Link Train 0 (LINKTRN0)**: Enable training/bifurcation using values programmed in BIFCTL0. LINKTRN0 must not assert until after BIFCTL0 is programmed. Root ports must be strapped to load LINKTRN0 continuously.

Table 3-4. Bifurcation Control (BIFCTL) (Sheet 2 of 2)

RP_BIFCTL
Bus: 0 Device: 14 Function: 0 Offset: 40Ch

Bit	Attribute	Default	Description
15:3	RV	0h	Reserved
2:0	RW	100b	**Bifurcation Control 0 (BIFCTL0)**: Bifurcation of RP Unit 0 into PCIe* Ports. See table below.

Table 3-5. Bifurcation Control Field Decode

BIFCTL0	Port 3 Lane Width	Port 2 Lane Width	Port 1 Lane Width	Port 0 Lane Width
000	x2	x2	x2	x2
001	x2	x2		x4
010		x4	x2	x2
011		x4		x4
100 (default)				x8
101	Reserved			
110	Reserved			
111	Reserved			

Table 3-6. RTFCGCTRL Register (RTFCGCTRL)

RTFCGCTRL
Bus: 0 Device: 14 Function: 0 Offset: 570h

Bit	Attribute	Default	Description
31	RW	0b	**Clock Gate Enable (CGEN):** This is to enable the Clock Gating. 0 = Disable clock gate by default 1 = When set, enable clock gating
30	RWL	0b	**Alarm Timer Enable (ATEN):** This is to enable the Alarm Timer. 0 = Disable alarm timer by default 1 = When set, enable alarm timer
29:20	RV	0h	Reserved
19:10	RW	10h	**Idle Timer (ITMR):** These two bit values are for the Idle Tmer.
94	RV	0h	Reserved
3:00	RW	0h	**GRCG Multiplier (GRCGM):** These four bit values are for the Gradual Reduction Clock Gating Multiplier.

3.2 PCI Express Root Port Registers (RP)

There is one integrated PCIe* Root Port Unit with four ports. The ports are single-Function PCI Devices 1, 2, 3, and 4. Each device has a set of registers in Configuration Space as listed in Table 3-7.

Table 3-7. Register Summary (Sheet 1 of 3)

Offset (h)	Size (bits)	Name
00	16	"Vendor Identification Register (VID)" on page 33
02	16	"Device Identification Register (DID)" on page 33
04	16	"PCI Command Register (PCICMD)" on page 34
06	16	"PCI Status Register (PCISTS)" on page 35
08	8	"Revision Identification Register (RID)" on page 35
09	24	"Class Code Register (CCR)" on page 36
0C	8	"Cacheline Size Register (CLS)" on page 36
0D	8	"Primary Latency Timer (PLAT)" on page 36
0E	8	"Header Type Register (HDR)" on page 36
0F	8	"Built-In Self Test (BIST)" on page 37
18	8	"Primary Bus Number Register (PRIBUS)" on page 37
19	8	"Secondary Bus Number Register (SECBUS)" on page 37
1A	8	"Subordinate Bus Number Register (SUBBUS)" on page 37
1C	8	"I/O Base Register (IOBASE)" on page 37
1D	8	"I/O Limit Register (IOLIMIT)" on page 38
1E	16	"Secondary Status Register (SECSTS)" on page 38
20	16	"Memory Base Register (MEMBASE)" on page 39
22	16	"Memory Limit Register (MEMLIMIT)" on page 39
24	16	"Prefetchable Memory Base Register (PFBASE)" on page 39
26	16	"Prefetchable Memory Limit Register (PFLIMIT)" on page 39
28	32	"Prefetchable Memory Base Upper 32 Bits Register (PFBASEU)" on page 39
2C	32	"Prefetchable Memory Limit Upper 32 Bits Register (PFLIMITU)" on page 40
34	8	"Capabilities Pointer Register (CAPPTR)" on page 40
3C	8	"Interrupt Line Register (INTL)" on page 40
3D	8	"Interrupt Pin Register (INTP)" on page 40
3E	16	"Bridge Control Register (BCTL)" on page 41
40	16	"PCI Express Capability List Register (EXPCAPLST)" on page 41
42	16	"PCI Express Capabilities Register (EXPCAP)" on page 42
44	32	"Device Capabilities Register (DEVCAP)" on page 42
48	16	"Device Control Register (DEVCTL)" on page 43
4A	16	"Device Status Register (DEVSTS)" on page 44
4C	32	"Link Capabilities Register (LINKCAP)" on page 45
50	16	"Link Control Register (LINKCTL)" on page 46
52	16	"Link Status Register (LINKSTS)" on page 47
54	32	"Slot Capabilities Register (SLOTCAP)" on page 48
58	10	"Slot Control Register (SLOTCTL)" on page 49

Table 3-7. Register Summary (Sheet 2 of 3)

Offset (h)	Size (bits)	Name
5A	16	"Slot Status Register (SLOTSTS)" on page 50
5C	16	"Root Control Register (ROOTCTL)" on page 51
5E	16	"Root Capabilities Register (ROOTCAP)" on page 51
60	32	"Root Status Register (ROOTSTS)" on page 51
64	32	"Device Capabilities 2 Register (DEVCAP2)" on page 52
68	16	"Device Control 2 Register (DEVCTL2)" on page 52
6A	16	"Device Status 2 Register (DEVSTS2)" on page 52
70	16	"Link Control 2 Register (LINKCTL2)" on page 53
72	16	"Link Status 2 Register (LINKSTS2)" on page 54
80	16	"Power Management Capability List Register (PMCAPLST)" on page 54
82	16	"Power Management Capabilities Register (PMCAP)" on page 55
84	16	"Power Management Control/Status Register (PMCSR)" on page 56
86	8	"Power Management Bridge Support Extensions Register (PMBSE)" on page 56
88	16	"Subsystem Capability List Register (SSCAPLST)" on page 56
8C	16	"Subsystem Vendor Identification Register (SSVID)" on page 57
8E	16	"Subsystem Identification Register (SSID)" on page 57
90	16	"MSI Capability List Register (MSICAPLST)" on page 57
92	16	"MSI Message Control Register (MSICTL)" on page 57
94	32	"MSI Message Address Register (MSIADDR)" on page 57
98	32	"MSI Message Data Register (MSIDATA)" on page 58
9C	32	"MSI Mask Bit Register (MSIMSK)" on page 58
A0	32	"MSI Pending Bit Register (MSIPENDING)" on page 58
100	32	"Advanced Error Reporting Extended Capability Header (AERCAPHDR)" on page 58
104	32	"Uncorrectable Error Status Register (ERRUNCSTS)" on page 59
108	32	"Uncorrectable Error Mask Register (ERRUNCMSK)" on page 60
10C	32	"Uncorrectable Error Severity Register (ERRUNCSEV)" on page 61
110	32	"Correctable Error Status Register (ERRCORSTS)" on page 62
114	32	"Correctable Error Mask Register (ERRCORMSK)" on page 62
118	32	"Advanced Error Capabilities and Control Register (AERCAPCTL)" on page 63
11C 120 124 128	32 32 32 32	"Header Log Register (AERHDRLOG[1-4])" on page 63
12C	32	"Root Error Command Register (ROOTERRCMD)" on page 63
130	32	"Root Error Status Register (ROOTERRSTS)" on page 64
134	32	"Error Source Identification Register (ERRSRCID)" on page 64
138	32	"Access Control Services Extended Capability Header (ACSCAPHDR)" on page 64
13C	16	"Access Control Services Capability Register (ACSCAP)" on page 65
13E	16	"Access Control Services Control Register (ACSCTL)" on page 66
140	32	"Uncorrectable Error Detect Mask Register (ERRUNCDETMSK)" on page 67
144	32	"Correctable Error Detect Mask Register (ERRCORDETMSK)" on page 67
148	32	"Root Error Detect Mask Register (ROOTERRDETMSK)" on page 68

Table 3-7. Register Summary (Sheet 3 of 3)

Offset (h)	Size (bits)	Name
D0	16	“Stop and Scream Control Register (SSCTL)” on page 69
D4	32	“PCIe Port Definition Control Register 0 (PPD0)” on page 70
EA	16	“Personality Lock Key Control Register (PLKCTL)” on page 72
FC	32	“Configuration Agent Error Register (CFGAGTERR)” on page 72
F8	8	“Legacy PCI Interrupt Swizzle Control Register (INTXSWZCTL)” on page 72

3.2.1 Introduction

The S12x0 provides up to four integrated Root Port (RP) links through one x8 RP Unit. The RP Unit is default-set as one x8 link. The RP Unit can be bifurcated to use the eight links as multiple x2 and x4 PCIe* links. Each bifurcated link has its own set of PCI Configuration and Capabilities registers.

Each PCI Express* configuration space has three regions:

- Standard PCI Header - This region is the standard PCI-to-PCI bridge Type 1 header providing legacy OS compatibility and resource management.
- PCI Device Dependent Region - This region is also part of standard PCI configuration space and contains the PCI capability structures and other port specific registers. The supported capabilities are as following:
  - SVID/SID Capability
  - Message Signalled Interrupts (MSI capability)
  - Power Management
  - PCI Express Capability
- PCI Express Extended Configuration Space - This space is an enhancement beyond standard PCI and only accessible with PCI Express aware software.
  - Advanced Error Reporting Capability
  - Access Control Services

The internal SoC fabric which interconnects the various functional blocks in the design may also be referred to as the “backbone” in some register field descriptions.

3.2.2 PCI Standard Header Registers

This section describes the PCI Configuration Space registers that make up the standard Type 1 header for PCI to PCI Bridges. Some information from the specification is repeated here as an aid to the reader or to describe implementation choice. Refer to the *PCI Express Base Specification 2.1*, the PCI-to-PCI Bridge Architecture Specification and the PCI Local Bus Specification 3.0 for the full register descriptions and additional information regarding their operation.

Table 3-8. Vendor Identification Register (VID)

VID
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 00h**

Bit	Attribute	Default	Description
15:0	RO	8086h	**Vendor ID (VID):** This 16 bit field identifies Intel as the manufacturer of the device.

Table 3-9. Device Identification Register (DID)

DID
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 02h**

Bit	Attribute	Default	Description
15:0	RO-V	Dev 1: 0C46h 2: 0C47h 3: 0C48h 4: 0C49h	**Device ID (DID):** This 16-bit field identifies the device ID for the S12x0Root Port link.
15:0	RO-V	Dev ? 0: 0C61h	**Device ID (DID):** This field identifies the particular function as allocated by Intel.

Table 3-10. PCI Command Register (PCICMD)

PCICMD **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 04h**			
Bit	**Attribute**	**Default**	**Description**
15:11	RV	00h	Reserved
10	RW	0b	**Interrupt Disable (INTxD):** This bit controls the ability of the PCI Express* Root port to generate legacy INTx# interrupts on enabled Hot Plug and power management events.This bit has no affect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages are not generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages are still forwarded to the internal interrupt controllers if this bit is set.
9	RO	0b	**Fast Back-to-back enable (FBE):** Not supported, Hardwired to 0.
8	RW	0b	**SERR# Enable (SEE):** 0 = Disable. 1 = Enables the root port to generate an SERR# message when PCISTS.SSE is set.
7	RO	0b	**Wait Cycle Control (WCC):** Not supported. Hardwired to 0.
6	RW	0b	**Parity Error Response Enable (PERE):** 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master PCIE function on the internal SoC fabric.
5	RO	0b	**VGA Palette Snoop Enable (VGA_PSE):** Not supported. Hardwired to 0.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not supported. Hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not supported. Hardwired to 0.
2	RW	0b	**Bus Master Enable (BME):** 0 = Disable. Memory and I/O requests received at a Root Port must be handled as Unsupported Requests. 1 = Enable. Allows the root port to forward memory and I/O requests onto the internal SoC fabric from a PCI Express device. ***Note:*** This bit does not affect forwarding of completions in either upstream or downstream direction nor controls forwarding of requests other than memory or I/O requests.
1	RW	0b	**Memory Space Enable (MSE):** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are handled as Unsupported Request by Root Port and aborted. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express device.
0	RW	0b	**I/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express device.
0	RO	0b	**I/O Space Enable (IOSE):** This bit controls the function’s response to I/O Space accesses. When this bit is 0b, the function does handle memory transactions targeting the Function as an Unsupported Request (UR). For Type 1 Configuration Space headers, this bit controls the primary side response to I/O Space accesses targeting the secondary side. When this bit is 0b, every memory transaction targeting a secondary interface is handled as an Unsupported Request (UR). For Non-posted requests, a completion with UR completion status must be returned.

Table 3-11. PCI Status Register (PCISTS)

PCISTS Bus: 0 Device: 1-4 Function: 0 Offset: 06h			
Bit	**Attribute**	**Default**	**Description**
15	RW1C	0b	**Detected Parity Error (DPE):** 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCICMD.PERE is not set.
14	RW1C	0b	**Signaled System Error (SSE):** 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	RW1C	0b	**Received Master Abort (RMA):** 0 = Root port has not received a completion with unsupported request status from the backbone. 1 = Set when the root port receives a completion with unsupported request status from the backbone.
12	RW1C	0b	**Received Target Abort (RTA):** 0 = Root port has not received a completion with completer abort from the backbone. 1 = Set when the root port receives a completion with completer abort from the backbone.
11	RW1C	0b	**Signaled Target Abort (STA):** 0 = No target abort received. 1 = Set whenever the root port forwards a target abort received from the downstream device onto the backbone.
10:9	RO	00b	**DEVSEL# Timing (DVT):** Not supported. These bits are hardwired to 0.
8	RW1C	0b	**Master Data Parity Error Detected (MDPD):** 0 = No data parity error received. 1 = Set when the root port receives a completion with a data parity error on the backbone and PCICMD.PERE is set.
7	RO	0b	**Fast Back-to-Back Capable (FBC):** Not supported. Hardwired to 0.
6	RV	0b	Reserved
5	RO	0b	**66 MHz Capable (C66):** Not supported. Hardwired to 0.
4	RO	1b	**Capabilities List Enable (CAPE):** Hardwired to 1. Indicates the presence of a capabilities list.
3	RO-V	0b	**Interrupt Status (INTS):** Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.INTxD bit.
2:0	RV	0h	Reserved

Table 3-12. Revision Identification Register (RID)

RID Bus: 0 Device: 1-4 Function: 0 Offset: 08h			
Bit	**Attribute**	**Default**	**Description**
7:0	ROS-V	00h	**Revision ID (RID):** This field specifies the specific revision of this function and is viewed as a extension to the Device ID.

Table 3-13. Class Code Register (CCR)

CCR **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 09h**
Bit	**Attribute**	**Default**	**Description**
23:16	RW-L PRST	06h	**Base Class (BC):** The value of 06h indicates that this is a bridge device.
15:8	RW-L PRST	04h	**Sub-Class (SC):** This 8-bit value indicates that this device is a PCI-to-PCI Bridge.
7:0	RW-L PRST	00h	**Register-Level Programming Interface (RLPI):** This bit indicates that this device is standard (non-subtractive) PCI-to-PCI Bridge.

Table 3-14. Cacheline Size Register (CLS)

CLS **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 0Ch**
Bit	**Attribute**	**Default**	**Description**
7:0	RW	00h	**Cache Line Size (CLS):** This is read/write but contains no functionality, per the *PCI Express* Base Specification*.

Table 3-15. Primary Latency Timer (PLAT)

PLAT **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 0Dh**
Bit	**Attribute**	**Default**	**Description**
7:0	RO	0h	**Primary Latency Timer (Prim_Lat_timer):** Not supported. Hardwired to 00h.

Table 3-16. Header Type Register (HDR)

HDR **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 0Eh**
Bit	**Attribute**	**Default**	**Description**
7	RW-L PRST	0	**Multi-function device (MFD):** Set the value 1 to indicate that the end point is a multifunction device although only function 0 is defined in this IAS document. ***Note:*** This is a single function device only.
7	RW-L PRST	0	**Multi-function device (MFD):** 0 = Single-function device 0 = Multi-function device
6:0	RW-L PRST	01h	**Header Type (HTYPE):** These bits define the layout of addresses 10h through 3Fh in the configuration space. These bits read as 01h to indicate that the register layout conforms to the standard PCI-to-PCI Bridge layout.
6:0	RW-L PRST	00h	**Header Type (HTYPE):** These bits define the layout of addresses 10h through 3Fh in the configuration space. For an end point device, default is 00h indicating a conventional type 00h PCI header.

Table 3-17. Built-In Self Test (BIST)

BIST **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 0Fh**			
Bit	**Attr**	**Default**	**Description**
7:0	RO	0h	**BIST Tests (BIST_TST):** Not supported. Hard-wired to 0h

Table 3-18. Primary Bus Number Register (PRIBUS)

PRIBUS **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 18h**			
Bit	**Attribute**	**Default**	**Description**
7:0	RW	0h	**Primary Bus Number (PBN):** Indicates the bus number of the backbone.

Table 3-19. Secondary Bus Number Register (SECBUS)

SECBUS **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 19h**			
Bit	**Attribute**	**Default**	**Description**
7:0	RW	00h	**Secondary Bus Number (SCBN):** These bits indicate the bus number of the PCI device to which the secondary interface is connected.

Table 3-20. Subordinate Bus Number Register (SUBBUS)

SUBBUS **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 1Ah**			
Bit	**Attribute**	**Default**	**Description**
7:0	RW	00h	**Subordinate Bus Number (SBBN):** Indicates the highest PCI bus number below the bridge.

Table 3-21. I/O Base Register (IOBASE)

IOBASE **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 1Ch**			
Bit	**Attribute**	**Default**	**Description**
7:4	RW	0h	**I/O Base Address Bits (IOBA):** I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to 000h.
3:0	RO	0h	**I/O Base Addressing Capability (IOBC):** Each of these bits is hard-wired to 0, indicating support for 16-bit I/O addressing only.

Table 3-22. I/O Limit Register (IOLIMIT)

IOLIMIT **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 1Dh**			
Bit	**Attribute**	**Default**	**Description**
7:4	RW	0h	**I/O Limit Address Bits (IOLA):** I/O Base bits corresponding to address lines 15:12 for 4-KB alignment. Bits 11:0 are assumed to be padded to FFFh.
3:0	RO	0h	**I/O Limit Addressing Capability (IOLC):** Indicates that the bridge does not support 32-bit I/O addressing.

Table 3-23. Secondary Status Register (SECSTS)

SECSTS **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 1Eh**			
Bit	**Attribute**	**Default**	**Description**
15	RW1C	0b	**Detected Parity Error (DPE):** 0 = No error. 1 = The port received a poisoned TLP.
14	RW1C	0b	**Received System Error (RSE):** 0 = No error. 1 = The port received an ERR_FATAL or ERR_NONFATAL message from the device.
13	RW1C	0b	**Received Master Abort (RMA):** 0 = Unsupported Request not received. 1 = The port received a completion with Unsupported Request status from the device.
12	RW1C	0b	**Received Target Abort (RTA):** 0 = Completion Abort not received. 1 = The port received a completion with Completion Abort status from the device.
11	RW1C	0b	**Signaled Target Abort (STA):** 0 = Completion Abort not sent. 1 = The port generated a completion with Completion Abort status to the device.
10:9	RO	00b	**DEVSEL# Timing (DVT):** Not Supported. Hardwired to 0.
8	RW1C	0b	**Master Data Parity Error Detected (MDPD):** 0 = Conditions below did not occur. 1 = Set when the PCICMD.PERE is set, and either of the following two conditions occurs: • Port receives completion marked poisoned. • Port poisons a write request to the secondary side.
7	RO	0b	**Fast Back-to-Back Capable (FBC):** Not Supported. Hardwired to 0.
6	RV	0b	Reserved
5	RO	0b	**66 MHz Capable (C66):** Not Supported. Hardwired to 0.
4:0	RV	0h	Reserved

Table 3-24. Memory Base Register (MEMBASE)

MEMBASE **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 20h**			
Bit	**Attribute**	**Default**	**Description**
15:4	RW	000h	**Memory Base (MB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	RV	0h	Reserved

Table 3-25. Memory Limit Register (MEMLIMIT)

MEMLIMIT **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 22h**			
Bit	**Attribute**	**Default**	**Description**
15:4	RW	000h	**Memory Limit (ML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
3:0	RV	0h	Reserved

Table 3-26. Prefetchable Memory Base Register (PFBASE)

PFBASE **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 24h**			
Bit	**Attribute**	**Default**	**Description**
15:4	RW	000h	**Prefetchable Memory Base (PMB):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1-MB aligned value of the range.
3:0	RO	1h	**Prefetchable Memory Base Address Capability (PFMCAP):** Indicates support for 64-bit addressing.

Table 3-27. Prefetchable Memory Limit Register (PFLIMIT)

PFLIMIT **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 26h**			
Bit	**Attribute**	**Default**	**Description**
15:4	RW	000h	**Prefetchable Memory Limit (PML):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1-MB aligned value of the range.
3:0	RO	1h	**Prefetchable Memory Limit Address Capability (PMLC):** Indicates support for 64-bit addressing.

Table 3-28. Prefetchable Memory Base Upper 32 Bits Register (PFBASEU)

PFBASEU **Bus: 0** **Device: 1-4** **Function: 0** **Offset: 28h**			
Bit	**Attribute**	**Default**	**Description**
31:0	RW	0h	**Prefetchable Memory Base Upper Portion (PMBU):** Upper 32-bits of the prefetchable address base.

Table 3-29. Prefetchable Memory Limit Upper 32 Bits Register (PFLIMITU)

PFLIMITU
Bus: 0 Device: 1-4 Function: 0 Offset: 2Ch

Bit	Attribute	Default	Description
31:0	RW	0h	**Prefetchable Memory Limit Upper Portion (PMLU):** Upper 32-bits of the prefetchable address limit.

Table 3-30. Capabilities Pointer Register (CAPPTR)

CAPPTR
Bus: 0 Device: 1-4 Function: 0 Offset: 34h

Bit	Attribute	Default	Description
7:0	RO	40h	**Capabilities Pointer (CPTR):** Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

Table 3-31. Interrupt Line Register (INTL)

INTL
Bus: 0 Device: 1-4 Function: 0 Offset: 3Ch

Bit	Attribute	Default	Description
7:0	RW	00h	**Interrupt Line (INTL):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.

Table 3-32. Interrupt Pin Register (INTP)

INTP
Bus: 0 Device: 1-4 Function: 0 Offset: 3Dh

Bit	Attribute	Default	Description
7:0	RW-L PRST	01h	**Interrupt Pin (INTP):** This register tells which interrupt pin the function uses. 01h: Generate INTA 02h: Generate INTB 03h: Generate INTC 04h: Generate INTD Others: Reserved BIOS has the ability to write this register once during boot to setup the correct interrupt for the Function.

Table 3-33. Bridge Control Register (BCTL)

BCTL **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 3Eh**

Bit	Attribute	Default	Description
15:12	RV	0h	Reserved
11	RO	0b	**Discard Timer SERR# Enable (DTSE):** Not Supported. Hardwired to 0.
10	RO	0b	**Discard Timer Status (DTS):** Not Supported. Hardwired to 0.
9	RO	0b	**Secondary Discard Timer (SDT):** Not Supported. Hardwired to 0.
8	RO	0b	**Primary Discard Timer (PDT):** Not Supported. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Enable (FBE):** Not Supported. Hardwired to 0.
6	RW	0b	**Secondary Bus Reset (SBR):** ***Note:*** Triggers a hot reset on the PCI Express* port.
5	RO	0b	**Master Abort Mode (MAM):** Not Supported. Hardwired to 0.
4	RW	0b	**VGA 16-bit Decode (VGA16BD):** 0 = VGA range is enabled. 1 = The I/O aliases of the VGA range are not enabled, and only the base I/O ranges can be decoded.
3	RW	0b	**VGA Enable (VGAE):** 0 = The ranges below are not claimed off the backbone by the root port. 1 = The following ranges are claimed off the backbone by the root port: • Memory ranges A0000h-BFFFFh • I/O ranges 3B0h – 3BBh and 3C0h – 3DFh, and all aliases of bits 15:10 in any combination of 1s
2	RW	0b	**ISA Enable (IE):** This bit only applies to I/O addresses that are enabled by the I/O Base and I/O Limit registers and are in the first 64 KB of PCI I/O space. 0 = The root port does not block any forwarding from the backbone as described below. 1 = The root port does block any forwarding from the backbone to the device of I/O transactions addressing the last 768 bytes in each 1-KB block (offsets 100h to 3FFh).
1	RW	0b	**SERR# Enable (SE):** 0 = The messages described below are not forwarded to the backbone. 1 = ERR_COR, ERR_NONFATAL, and ERR_FATAL messages received are forwarded to the backbone.
0	RW	0b	**Parity Error Response Enable (PERE):** This bit controls the response to poisoned TLPs in the PCI Express port. 1 = Enables reporting of poisoned TLP errors. 0 = Disables reporting of poisoned TLP errors.

Table 3-34. PCI Express Capability List Register (EXPCAPLST)

EXPCAPLST **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 40h**

Bit	Attribute	Default	Description
15:8	RO	80h	**Next Pointer (NP):** Value of 80h indicates the location of the next pointer.
7:0	RO	10h	**Capability ID (CAPID):** Identifies the function as PCI Express* capable.

Table 3-35. PCI Express Capabilities Register (EXPCAP)

EXPCAP **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 42h**
Bit	**Attribute**	**Default**	**Description**
15:14	RV	0h	Reserved
13:9	RO-V	0h	**Interrupt Message Number (IMN):** The Root Port does not have multiple MSI interrupt numbers.
8	RW-L PRST	0	**Slot Implemented (SI):** Indicates whether the root port is connected to a slot. Slot support is platform specific. BIOS programs this field, and it is maintained until a platform reset.
7:4	RO	4h	**Device/Port Type (DT):** Indicates this is a PCI Express* root port.
3:0	RO	2h	**Version Number (VN):** Indicates PCI Express 2.0.

Table 3-36. Device Capabilities Register (DEVCAP)

DEVCAP **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 44h**
Bit	**Attribute**	**Default**	**Description**
31:29	RV	0h	Reserved
28	RV	0b	**Function Level Reset Capability (FLR):** Field not applicable for Root Port. Hardwired to 0b.
27:26	RO	00b	**Captured Slot Power Limit Scale** (CSPLS): Field not applicable for Root Port. These bits are hardwired to 0.
25:18	RO	0h	**Captured Slot Power Limit Value** (CSPLV): Field not applicable for Root Port. These bits are hardwired to 0.
17:16	RV	00b	Reserved
15	RO	1b	**Role-Based Error Reporting (RBER):** Indicates that this device implements the functionality defined in the Error Reporting ECN as required by the *PCI Express* 2.0 Specification*.
14:12	RO	0h	Undefined
11:9	RO	000b	**Endpoint L1 Acceptable Latency (EPL1AL):** Field not applicable for Root Port. These bits are hardwired to 0.
8:6	RO	000b	**Endpoint L0s Acceptable Latency (EPL0AL):** Field not applicable for Root Port. These bits are hardwired to 0.
5	RW-L PRST	1b	**Extended Tag Field Supported (ETFG):** Indicates that 8-bit tag fields are supported.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not supported, These bits are hardwired to 0
2:0	RW-L PRST	001	**Max Payload size Supported (MPSS):** Indicates the maximum payload size supported is 256B.

Table 3-37. Device Control Register (DEVCTL)

DEVCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 48h**

Bit	Attribute	Default	Description
15	RV	0b	Reserved
14:12	RW	010b	**Max_Read_Request_Size (MRRS):** Indicates maximum read request size. The supports max read request size of 256 bytes or lower.
11	RO	0b	**Enable No Snoop (ENOSNP):** Not supported. Hardwired to 0.
11	RW	1b	**Enable No Snoop (ENOSNP):** If this bit this is set, the function is permitted to set the No Snoop bit in the Requester attributes of transactions it initiates that do not require hardware enforced cache coherency.
10	RO	0b	**Auxiliary Power PM Enable (AUXPME):** Not supported. Hardwired to 0.
9	RO	0b	**Phantom Function Enable (PFE):** Not supported. Hardwired to 0.
8	RW	0b	**Extended Tag Field Enable (ETFE):** When set, this bit enables a function to use an 8-bit tag field as a Requester. Functions that do not implement this capability hardwire this bit to 0b.
7:5	RW	000b	**Maximum Payload Size (MPS):** ***Note:*** Indicates maximum TLP payload size for the Root Port. The S12x0 can support up to 256B as max payload size. 000 - 128 bytes maximum payload size (Default) 001 - 256 bytes maximum payload size Others - Unsupported/Reserved
4	RO	0b	**Enable Relaxed Ordering (ENRO):** Not supported. Hardwired to 0.
3	RW	0b	**Unsupported Request Reporting Enable (URRE):** 0 = The root port does ignore unsupported request errors. 1 = Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked Advisory Non-Fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-Advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	RW	0b	**Fatal Error Reporting Enable (FERE):** 0 = The root port does ignore fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	RW	0b	**NonFatal Error Reporting Enable (NFERE):** 0 = The root port does ignore non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW	0b	**Correctable Error Reporting Enable (CERE):** 0 = The root port does ignore correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Table 3-38. Device Status Register (DEVSTS)

DEVSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 4Ah**

Bit	Attribute	Default	Description
15:6	RV	000h	Reserved
5	RO-V	0b	**Transactions Pending (TP):** Root Port does not issue Non-Posted requests. Hardwired to 0.
4	RO	0b	**Auxiliary Power Detected (APD):** Not supported. Hardwired to 0.
3	RW1C	0b	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
2	RW1C	0b	**Fatal Error Detected (FED):** Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	RW1C	0b	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	RW1C	0b	**Correctable Error Detected (CED):** Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors / framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

Table 3-39. Link Capabilities Register (LINKCAP)

LINKCAP
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 4Ch**

Bit	Attribute	Default	Description
31:24	RW-LV PRST	Dev 1: 01h 2: 02h 3: 03h 4: 04h	**Port Number (PN):** This field indicates the PCI Express* port number assigned to the Root Port.
23:21	RV	0b	Reserved
20	RW-L PRST	1b	**Data Link Layer Active Error Reporting Capable (DLLERC):** RO. Hardwired to 1 to indicate that this port supports the optional capability of reporting the DL_Active state of the Data Link Control and Management State Machine.
19	RW-L PRST	1b	Reserved
18	RO	0b	**Clock Power Management Capable (CPMC):** Not supported. Hardwired to 0.
17:15	RW-L PRST	010b	**L1 Exit Latency (L1EL):** This field indicates the L1 exit latency for the given PCI Express Link. It indicates the length of time this port requires to complete transition from L1 to L0. 000: Less than 1 µs 001: 1 µs to less than 2 µs 010: 2 µs to less than 4 µs 011: 4 µs to less than 8 µs 100: 8 µs to less than 16 µs 101: 16 µs to less than 32 µs 110: 32 µs to less than 64 µs 111: More than 64 µs
14:12	RW-L PRST	100b	**L0s Exit Latency (L0sEL):** This field indicates the L0s exit latency for the given PCI Express Link. It indicates the length of time this port requires to complete transition from L0s to L0. 000b: Less than 64ns 001b: 64 ns to less than 128 ns 010b: 128 ns to less than 256 ns 011b: 256 ns to less than 512 ns 100b 512 ns to less than 1 µs 101b: 1 µs to less than 2 µs 110b: 2 µs to less than 4 µs 111b: More than 4 µs ***Note:*** L0s is not supported by the Root Ports and so the value is undefined.
11:10	RW-L PRST	11b	**ASPM Support (ASPMSUP):** This field indicates the level of ASPM supported on the root port. 00b: No ASPM Support 01b: L0s Not Supported 10b: L1 Supported 11b: L0s and L1 Supported ***Note:*** Only L1 ASPM is supported by the Root Ports while L0s ASPM is not supported. The BIOS initializes this field to “10b” before link training and locks-in this value.
9:4	RO-V	08h	**Maximum Link Width (MLW):** This field indicates the maximum link width of x8 is implemented by Root Port.
3:0	RO-V	2h	**Maximum Link Speed (MLS):** This field indicates the 5.0 Gb/s and 2.5 Gb/s supported link speed by Root Port.

Table 3-40. Link Control Register (LINKCTL)

LINKCTL
Bus: 0 Device: 1-4 Function: 0 Offset: 50h

Bit	Attribute	Default	Description
15:10	RV	0h	Reserved
9	RW	0b	**Hardware Autonomous Width Disable (HAWD):** When set, this bit disables hardware from changing the Link width for reasons other than attempting to correct unreliable Link operation by reducing Link width. Components that do not implement the ability autonomously to change Link width are permitted to hardwire this bit to 0b.
8	RO	0b	**Enable Clock Power Management (ECPM):** Not supported. Hardwire to 0.
7	RW	0b	**Extended Synch (ES):** 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	RW	0b	**Common Clock Configuration (CCCFG):** 0 = The S12x0 and device are not using a common reference clock. 1 = The S12x0 and device are operating with a distributed common reference clock.
5	RW-V	0b	**Retrain Link (RL):** When set, this bit initiates link retraining by directing the physical layer LTSSM to recovery state. If the LTSSM is already in REcovery or configuration, re-entering Recovery is permitted but not required. Reads of this bit always return 0b.
4	RW	0b	**Link Disable (LD):** 0 = Link enabled. 1 = The root port does disable the link.
3	RO	0b	**Read Completion Boundary (RCB):** This bit indicates 64 byte RCB value for Root Port.
2	RV	0b	Reserved
1:0	RW	00b	**ASPM Control (ASPMCTL):** Indicates whether the root port enters L0s or L1 or both. 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled

Table 3-41. Link Status Register (LINKSTS)

LINKSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 52h**

Bit	Attribute	Default	Description
15:14	RW1C	0b	Reserved
13	RO-V	0b	**Data Link Layer Link Active (DLLLA):** 0 = Data Link Control and Management State Machine is not in the DL_Active state. 1 = Data Link Control and Management State Machine is in the DL_Active state.
12	RW-L PRST	1b	**Slot Clock Configuration (SCC):** Set to 1b to indicate that the S12x0 uses the same reference clock as on the platform and does not generate its own clock.
11	RO-V	0	**Link Training (LT):** 0 = Link training completed. 1 = Link training is occurring.
10	RO	0	**Undefined:** Not applicable. Hardwired to 0.
9:4	RO-V	0h	**Negotiated Link Width (NLW):** This field indicates the negotiated width of the RootPort link. 00 0001b: x1 00 0010b: X2 00 0100b: x4 00 1000b: X8 All other values are reserved. ***Note:*** The value in this field is undefined when the link is not up.
3:0	RO-V	1h	**Current Link Speed (CLS):** This field indicates the negotiated Link speed of the given PCI Express* link. 0001b: 2.5 Gb/s PCI Express Link 0010b: 5.0 Gb/s PCI Express Link Others: Reserved The encoding is the binary value of the bit location in the Supported Link Speeds Vector (in the Link Capabilities 2 register) that corresponds to the current Link speed. The value in this field is undefined when the link is not up.

Table 3-42. Slot Capabilities Register (SLOTCAP)

SLOTCAP
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 54h**

Bit	Attribute	Default	Description
31:19	RW-L PRST	0h	**Physical Slot Number (PSN):** This is a value that is unique to the slot number. BIOS sets this field and it remains set until a platform reset.
18:17	RW-L PRST	0b	Reserved
16:15	RW-L PRST	00b	**Slot Power Limit Scale (SPLS):** Specifies the scale used for the slot power limit value. BIOS sets this field and it remains set until a platform reset.
14:7	RW-L PRST	00h	**Slot Power Limit Value (SPLV):** Specifies the upper limit (in conjunction with SLS value), on the upper limit on power supplied by the slot. The two values together indicate the amount of power in watts allowed for the slot. BIOS sets this field and it remains set until a platform reset.
6	RW-L PRST	0b	**Hot-plug Capable (HPC):** This field defines hot-plug support capabilities for the Root port. 0 = Indicates that this slot is not capable of supporting Hot-plug operations. 1 = Indicates that this slot is capable of supporting Hot-plug operations.
5	RW-L PRST	0b	**Hot-plug Surprise (HPS):** This field indicates that a device in this slot may be removed from the system without prior notification. 0 = Indicates that hot-plug surprise is not supported. 1 = Indicates that hot-plug surprise is supported.
4	RW-L PRST	0b	**Power Indicator Present (PIP):** This bit indicates that a Power Indicator is implemented on the chassis for this slot. 0 = Indicates that Power Indicator is not present. 1 = Indicates that Power Indicator is present.
3	RW-L PRST	0b	**Attention Indicator Present (AIP):** This bit indicates that an Attention Indicator is implemented on the chassis for this slot. 0 = Indicates that an Attention Indicator is not present. 1 = Indicates that an Attention Indicator is present.
2	RW-L PRST	0b	**MRL Sensor Present (MRLSP):** This bit indicates that an MRL Sensor is implemented on the chassis for this slot. 0 = Indicates that an MRL Sensor is not present. 1 = Indicates that an MRL Sensor is present.
1	RW-L PRST	0b	**Power Controller Present (PCP):** This bit indicates that a Power Controller is implemented on the chassis for this slot. 0 = Indicates that a Power Controller is not present. 1 = Indicates that a Power Controller is present.
0	RW-L PRST	0b	**Attention Button Present (ABP):** This bit indicates that an Attention Button is implemented on the chassis for this slot. 0 = Indicates that an Attention Button is not present. 1 = Indicates that an Attention Button is present.

Table 3-43. Slot Control Register (SLOTCTL)

SLOTCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 58h**

Bit	Attribute	Default	Description
15:13	RV	0h	Reserved
12	RW	0	**Data Link Layer State Changed Enable (DLLSCE):** When set to 1, this field enables software notification when Data Link Layer Link Active reporting field is changed.
11	RW-V	0	Reserved
10	RW	0	**Power Controller Control (PCC):** This bit indicates the current state of the Power applied to the slot of the PCI Express* port. Reads of this field must reflect the value from the latest write, even if the corresponding Hot-Plug command is not executed yet at the VPP, unless software issues a write without waiting for the previous command to complete in which case the read value is undefined. 0 = Power On 1 = Power Off
9:6	RW	11	Reserved
5	RW	0	**Hot-plug Interrupt Enable (HPIE):** 0 = Hot plug interrupts based on Hot-Plug events is disabled. 1 = Enables generation of a Hot-Plug interrupt on enabled Hot-Plug events.
4	RW	0	Reserved
3	RW	0	**Presence Detect Changed Interrupt Enable (PDCIE):** 0 = Hot-plug interrupts based on presence detect logic changes is disabled. 1 = Enables the generation of a Hot-Plug interrupt or wake message when the presence detect logic changes state.
2:0	RW	0	Reserved

Table 3-44. Slot Status Register (SLOTSTS)

SLOTSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 5Ah**

Bit	Attribute	Default	Description
15:9	RV	0	Reserved
8	RW1C	0	**Data Link layer State Changed Status (DLLSCS):** This bit is set (if it is not already set) when the state of the Data Link Layer Link Active bit in the Link Status register has changed. Software must read Data Link Layer Active field to determine the link state before initiating configuration cycles to the hot plugged device.
7	RO-V	0	Reserved
6	RO-V	1	**Presence Detect State (PDS):** If EXPCAP.SI is set (indicating that this root port spawns a slot), then this bit: 0 = Indicates the slot is empty. 1 = Indicates the slot has a device connected. Otherwise, if EXPCAP.SI is cleared, this bit is always set (1).
5	RO-V	0	**MRL Sensor State (MRLSS):** Not supported. Hardwired to 0.
4	RW1C	0	**Command Completed (CCS):** This bit is set when the hot-plug controller completes an issued command and is ready to accept a new command. It is subsequently cleared by software after the field has been read and processed. If Command Completed notification is supported, then the No Command Completed Support bit in the Slot Capabilities register is 0.
3	RW1C	0	**Presence Detect Changed (PDCS):** 0 = No change in the PDS bit. 1 = The PDS bit changed states.
2	RW1C	0	**MRL Sensor Changed (MRLSC):** Reserved as the MRL sensor is not implemented.
1	RW1C	0	**Power Fault Detected (PFD):** Reserved as a power controller is not implemented.
0	RW1C	0	Reserved

Table 3-45. Root Control Register (ROOTCTL)

ROOTCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 5Ch**

Bit	Attribute	Default	Description
15:4	RV	0	Reserved
3	RW	0	**PME Interrupt Enable (PMEIE):** 0 = Interrupt generation disabled. 1 = Interrupt generation enabled when PCISTS INTS is in a set state.
2	RW	0	**System Error on Fatal Error Enable (SEFEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming PCICMD.SEE is set, if a fatal error is reported by any of the devices in the hierarchy of this root port, including fatal errors in this root port.
1	RW	0	**System Error on Non-Fatal Error Enable (SENFEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming PCICMD.SEE is set, if a non-fatal error is reported by any of the devices in the hierarchy of this root port, including non-fatal errors in this root port.
0	RW	0	**System Error on Correctable Error Enable (SECEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming PCICMD.SEE if a correctable error is reported by any of the devices in the hierarchy of this root port, including correctable errors in this root port.

Table 3-46. Root Capabilities Register (ROOTCAP)

ROOTCAP
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 5Eh**

Bit	Attr	Default	Description
15:1	RV	0	*Reserved*
0	RW-L PRST	1	**CRS Software Visibility (CRSSV):** This bit, when set, indicates that the Root Port is capable of returning Configuration Retry Status (CRS) on completions to software. ***Note:*** The CRSSV field is not supported. BIOS must clear the field to 0 before locking this register to ensure that the Root Ports do not advertize as being CRSSV capable.

Table 3-47. Root Status Register (ROOTSTS)

ROOTSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 60h**

Bit	Attribute	Default	Description
31:18	RV	0	Reserved
17	RO-V	0	**PME Pending (PMEPEND):** 0 = When the original PME is cleared by software, it is set again, the requestor ID is updated, and this bit is cleared. 1 = Indicates another PME is pending when the PME status bit is set.
16	RW1C	0h	**PME Status (PMESTS):** 0 = PME was not asserted. 1 = Indicates that PME was asserted by the requestor ID in RID. Subsequent PMEs are kept pending until this bit is cleared.
15:0	RO-V	0h	**PME Requester ID (PMERID):** This field indicates the PCI requester ID of the last PME requestor.

Table 3-48. Device Capabilities 2 Register (DEVCAP2)

DEVCAP2
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 64h**

Bit	Attribute	Default	Description
31:5	RV	0h	Reserved
4	RW-L PRST	1	**Completion Timeout Disable Support (CTDS):** A value of 1b indicates support for the completion Timeout Disable Mechanism. The S12x0 Root Port supports completions timeout disable.
3:0	RW-L PRST	0111	**Completion Timeout Range Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. The default value indicates support for the following time value ranges: 50 µs to 10 ms 10 ms to 250 ms, 250 ms to 4s

Table 3-49. Device Control 2 Register (DEVCTL2)

DEVCTL2
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 68h**

Bit	Attribute	Default	Description
15:5	RO	0	Reserved
4	RW	0	**Completion Timeout Disable (CTD):** 1 = Disable the completions timeout mechanism for all NP transactions. 0 = Completion timeout is enabled for all NP transactions.
3:0	RW	0000b	**Completion Timeout Value (CTV):** This field allows system software to modify the Completion Timeout value. 0000b: 50 µs to 50 ms (16.8 ms - 25.2 ms based on core clk period) 0001b: 50 µs to 100 µs (65.5 µs - 99.3 µs based on core clk period) 0010b: 1 ms to 10 ms (4.2 ms - 6.3 ms based on core clk period) 0101b: 16 ms to 55 ms (33.6 ms - 50.3 ms based on core clk period) 0110b: 65 ms to 210 ms (134.2 ms - 201.3 ms based on core clk period) 1001b: 260 ms to 900 ms (536.9 ms - 805.3 ms based on core clk period) 1010b: 1s to 3.5s (2.1s - 3.2s based on core clk period) 1101b: 4s to 13s (8.6s - 12.9s based on core clk period) 1110b: 17s to 64s (34.4s - 51.5s based on core clk period) All others are reserved. ***Note:*** It is highly recommended that the completion timeout value not be less then 10 ms or greater. A small completion timeout value may result in premature completion timeout for slower responding devices. If a greater than 25 ms timeout value is required.

Table 3-50. Device Status 2 Register (DEVSTS2)

DEVSTS2
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 6Ah**

Bit	Attr	Default	Description
15:0	RV	0	*Reserved*

Table 3-51. Link Control 2 Register (LINKCTL2)

LINKCTL2
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 70h**

Bit	Attribute	Default	Description
15:12	RWS	0h	**Compliance Preset/De-emphasis (CD):** For 5 GT/s: This bit sets the transmitter preset level for Polling.Compliance state if the entry occurred due to the Enter Compliance bit being 1b. The Encoding are defined as follows: 5 GT/s Rate: 001b: -3.5dB 000b: -6 dB All other are reserved. When the link is operating at 2.5 Gb/s, the setting of this bit has no effect. Components that support only 2.5 GT/s speed are permitted to hardwire this bit to 0b.
11	RWS	0b	**Compliance SOS (CSOS):** When set to 1b, the LTSSM is required to send Skip Ordered Sets periodically in between the (modified) compliance patterns.
10:7	RWS	0b	**Reserved**
6	RW-L PRST	0b	**Selectable De-emphasis (SD):** Applicable to RootPorts and downstream ports of PCI Express to PCIe bridges. When the link is operating at 5 Gb/s speed, this bit selects the level of deemphasis for an Downstream Port. Encodings: 1b -3.5 dB 0b -6 dB When the Link is operating at 2.5 GT/s speed, the setting of this bit has no effect.
5	RWS	0b	**Hardware Autonomous Speed Disable (HASD):** When set, this bit disables hardware from changing the link speed for device specific reasons other than attempting to correct unreliable link operation by reducing link speed for device-specific reasons other than attempting to correct unreliable link operations by reducing link speed. Initial transition to the highest supported common link speed is not blocked by this bit.
4	RV	0b	**Reserved**
3:0	RWS	2h	**Target Link Speed (TLS):** This field sets an upper limit on Link operational speed by restricting the values advertised by the upstream component in its training sequences. 0001b: 2.5 Gb/s Target Link Speed 0010b: 5.0 Gb/s Target Link Speed Others: Reserved

Table 3-52. Link Status 2 Register (LINKSTS2)

LINKSTS2 **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 72h**
Bit	**Attr**	**Default**	**Description**
15:6	RV	0h	*Reserved*
5	RW1CS	0b	**Link Equalization Request (LNKEQREQ)**: This bit is set by hardware to request the Link equalization process to be performed on the Link.
4	ROS-V	0b	**Equalization Phase 3 Successful (EQPH3SUCC)**: When set to 1b, this bit indicates that Phase 3 of the Transmitter Equalization procedure has successfully completed.
3	ROS-V	0b	**Equalization Phase 2 Successful (EQPH2SUCC)**: When set to 1b, this bit indicates that Phase 2 of the Transmitter Equalization procedure has successfully completed.
2	ROS-V	0b	**Equalization Phase 1 Successful (EQPH1SUCC)**: When set to 1b, this bit indicates that Phase 1 of the Transmitter Equalization procedure has successfully completed.
1	ROS-V	0b	**Equalization Complete (EQCMPLT)**: When set to 1b, this bit indicates that the Transmitter Equalization procedure has successfully completed.
0	RO-V	0b	**Current De-emphasis Level (CDL):** When the link is operating at 5 GT/s speed, this bit reflects the level of de-emphasis. 1b: -3.5 dB 0b: -6dB The value in this bit is undefined when the Link is not operating at 5.0 GT/s speed. Components that support only the 2.5 GT/s are permitted to hardwire this bit to 0b.

Table 3-53. Power Management Capability List Register (PMCAPLST)

PMCAPLST **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 80h**
Bit	**Attribute**	**Default**	**Description**
15:8	RO	88h	**Next Pointer:** Contains the offset of the next item in the capabilities list.
7:0	RO	01h	**Capability ID:** Identifies the function as PCI Power Management capable.

Table 3-54. Power Management Capabilities Register (PMCAP)

PMCAP **Bus: 0**		**Device: 1-4**	**Function: 0** **Offset: 82h**
Bit	**Attribute**	**Default**	**Description**
15:11	RO	19h	**PME_Support (PMES):** Indicates PME# is supported for states $D3_{HOT}$ and $D3_{COLD}$. The root port does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind this root port.
10	RO	0b	**D2 Support (D2S):** Not supported. Hardwired to 0.
9	RO	0b	**D1 Support (D1S):** Not supported. Hardwired to 0.
8:6	RO	000b	**Auxiliary Current (AC):** Not supported. This bits are hardwired to 0.
5	RO	0b	**Device Specific Initialization (DSI):** Not supported. Hardwired to 0.
4	RV	0b	Reserved
3	RO	0b	**PME Clock (PMECLK):** Not supported. Hardwired to 0.
2:0	RO	3h	**Version (VER):** The PM implementation in the PCIe* Root Port is compliant with *PCI Bus Power Management Interface Specification*, Revision 1.2.

Table 3-55. Power Management Control/Status Register (PMCSR)

PMCSR
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 84h**

Bit	Attribute	Default	Description
15	RW1CS	0	**PME Status (PMESTS)**
14:13	RO	0h	**Data Scale (DC):** Not supported. Hardwired to 0.
12:9	RO	0h	**Data Select (DS):** Not supported. Hardwired to 0.
8	RWS	0	**PME Enable (PMEEN):** 1 = Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	RV	0h	Reserved
1:0	RW-R	0h	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state If software attempts to write an unsupported, optional state to this field, the write operation must complete normally; however, the data is discarded and no state change occurs.

Table 3-56. Power Management Bridge Support Extensions Register (PMBSE)

PMBSE
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 86h**

Bit	Attr	Default	Description
7	RO	0b	**Bus Power/Clock Control Enable (BPCC_EN):** Neither bus or clock control of PCI is supported when in D3hot state. This bit is hard-wired to 0.
6	RO	0b	**B2/B3# (B23EN):** Not supported. This bit has no meaning since the BPCC_En bit is hard-wired to 0.
5:0	RV	00h	*Reserved*

Table 3-57. Subsystem Capability List Register (SSCAPLST)

SSCAPLST
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 88h**

Bit	Attribute	Default	Description
15:8	RO	90h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list. (MSICAPLST)
7:0	RO	0Dh	**Capability ID (CAPID):** Identifies the function as Subsystem Identification capable.

Table 3-58. Subsystem Vendor Identification Register (SSVID)

SSVID **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 8Ch**
Bit	**Attribute**	**Default**	**Description**
15:0	RW-L PRST	8086h	**Subsystem Vendor Identifier (SSVID):** Assigned by PCI-SIG for vendor ID.

Table 3-59. Subsystem Identification Register (SSID)

SSID **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 8Eh**
Bit	**Attribute**	**Default**	**Description**
15:0	RW-L PRST	0000h	**Subsystem Identifier (SSID):** Assigned to uniquely identify the subsystem vendor.

Table 3-60. MSI Capability List Register (MSICAPLST)

MSICAPLST **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 90h**
Bit	**Attribute**	**Default**	**Description**
15:8	RO	00h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list. A null value is used to indicate that this is the last capability.
7:0	RO	05h	**Capability ID (CAPID):** Identifies the function as MSI capable.

Table 3-61. MSI Message Control Register (MSICTL)

MSICTL **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 92h**
Bit	**Attribute**	**Default**	**Description**
15:8	RV	01h	Reserved
7	RO	0b	**Address 64-Bit Capable (AD64C):** Not supported. Hardwired to 0. Capable of generating a 32-bit message only.
6:4	RW	000b	**Multiple Message Enable (MMEN):** Only one message is supported. These bits are R/W for software compatibility.
3:1	RO	000b	**Multiple Message Capable (MMC):** Only one message is supported.
0	RW	0b	**MSI Enable (MSIE):** When set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

Table 3-62. MSI Message Address Register (MSIADDR)

MSIADDR **Bus: 0**	**Device: 1-4**	**Function: 0**	**Offset: 94h**
Bit	**Attribute**	**Default**	**Description**
31:2	RW	0h	**Address:** Message address specified by the system, always DWORD aligned.
1:0	RV	00b	Reserved

Table 3-63. MSI Message Data Register (MSIDATA)

MSIDATA
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 98h**

Bit	Attribute	Default	Description
31:16	RV	0000h	Reserved
15:0	RW	0h	**Data (DATA):** R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

Table 3-64. MSI Mask Bit Register (MSIMSK)

MSIMSK
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 9Ch**

Bit	Attr	Default	Description
31:1	RV	0h	*Reserved*
0	RW	00b	**Mask Bits (MSKB):** For each Mask bit that is set, the PCI Express port is prohibited from sending the associated message. Corresponding bits are masked if set to ‘1’

Table 3-65. MSI Pending Bit Register (MSIPENDING)

MSIPENDING
Bus: 0 **Device: 1-4** **Function: 0** **Offset: A0h**

Bit	Attr	Default	Description
31:1	RV	0h	*Reserved*
0	RO-V	0h	**Pending Bits (PB):** For each Pending bit that is set, the PCI Express port has a pending associated message. Corresponding bits are pending if set to ‘1’

Table 3-66. Advanced Error Reporting Extended Capability Header (AERCAPHDR)

AERCAPHDR
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 100h**

Bit	Attribute	Default	Description
31:20	RW-L PRST	138h	**Next Capability Offset (NCO):** Contains the offset of the next structure in the Extended Capabilities list. (ACSCAPHDR)
19:16	RO	1h	**Capability Version (CV):** Indicates the version of the Capability structure present.
15:0	RO	0001h	**Extended Capability ID (EXCAPID):** Identifies the function as Advanced Error Reporting capable.

Table 3-67. Uncorrectable Error Status Register (ERRUNCSTS)

ERRUNCSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 104h**

Bit	Attribute	Default	Description
31:21	RV	000h	Reserved
20	RW1CS	0b	**Unsupported Request Error (URE):** This bit is set whenever an unsupported request is detected on PCI Express* port.
19	RO	0b	**ECRC Check Error (ECRCE):** ECRC Checking not supported. Hardwired to 0.
18	RW1CS	0b	**Malformed TLP Error (MTLPE):** This bit is set when it receives a malformed TLP. Header logging is performed.
17	RW1CS	0b	**Receiver Overflow Error (ROE):** This bit is set when the PCI Express interface receive buffers overflow.
16	RW1CS	0b	**Unexpected Completion Error (UCE):** Indicates an unexpected completion was received.
15	RW1CS	0b	**Completer Abort Error (CAE):** Indicates a completer abort was received.
14	RW1CS	0b	**Completion Timeout Error (CTE):** Indicates a completion timed out. This bit is set if Completion Timeout is enabled and a completion is not returned within the time specified by the Completion Timeout Value.
13	RW1CS	0b	**Flow Control Error (FCE):** This bit is set when a flow control protocol error is detected.
12	RW1CS	0b	**Poisoned TLP Error (PTLPE):** Indicates a poisoned TLP was received.
11:5	RV	00h	Reserved
4	RW1CS	0b	**Data Link Protocol Error (DLPE):** This bit is set when a data link protocol error is detected.
3:0	RV	000b	Reserved

Table 3-68. Uncorrectable Error Mask Register (ERRUNCMSK)

ERRUNCMSK
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 108h**

Bit	Attribute	Default	Description
31:21	RV	000h	Reserved
20	RWS	0b	**Unsupported Request Error Mask (UREM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
19	RO	0b	**ECRC Check Error Mask (ECRCEM):** Not supported.
18	RWS	0b	**Malformed TLP Error Mask (MTLPEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
17	RWS	0b	**Receiver Overflow Error Mask (ROEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
16	RWS	0b	**Unexpected Completion Error Mask (UCEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
15	RWS	0b	**Completer Abort Error Mask (CAEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
14	RWS	0b	**Completion Timeout Error Mask (CTEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
13	RWS	0b	**Flow Control Error Mask (FCEM)**
12	RWS	0b	**Poisoned TLP Error Mask (PTLPEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
11:5	RV	00h	Reserved
4	RWS	0b	**Data Link Protocol Error Mask (DLPEM):** 0 = The corresponding error in the ERRUNCSTS register is enabled. 1 = The corresponding error in the ERRUNCSTS register is masked.
3:0	RV	000b	Reserved

Table 3-69. Uncorrectable Error Severity Register (ERRUNCSEV)

ERRUNCSEV
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 10Ch**

Bit	Attribute	Default	Description
31:21	RV	000h	Reserved
20	RWS	0b	**Unsupported Request Error Status Severity (URES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	RO	0b	**ECRC Check Error Severity (ECRCES):** Not supported. Hardwired to 0.
18	RWS	1b	**Malformed TLP Error Severity (MTLPES):** 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	RWS	1b	**Receiver Overflow Error Severity (ROES):** 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
16	RWS	0b	**Unexpected Completion Error Severity (UCES)**
15	RWS	0b	**Completer Abort Error Severity (CAES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
14	RWS	0b	**Completion Timeout Error Severity (CTES)**
13	RWS	1b	**Flow Control Error Severity (FCES)**
12	RWS	0b	**Poisoned TLP Error Severity (PTLPES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
11:5	RV	00h	Reserved
4	RWS	1b	**Data Link Protocol Error Severity (DLPES):** 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:0	RV	000b	Reserved

Table 3-70. Correctable Error Status Register (ERRCORSTS)

ERRCORSTS
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 110h**

Bit	Attribute	Default	Description
31:14	RV	0h	Reserved
13	RW1CS	0	**Advisory Non-Fatal Error (ANFE):** 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	RW1CS	0	**Replay Timer Timeout Error (RTTE):** The PCIe* sets this bit when replay timer time-out occurs.
11:9	RV	0h	Reserved
8	RW1CS	0	**Replay Number Rollover Error (RNRE):** The PCIe sets this bit when the replay number rolls over from 11 to 00.
7	RW1CS	0	**Bad DLLP Error (BDLLPE):** The switch sets this bit on CRC errors on DLLP.
6	RW1CS	0	**Bad TLP Error (BTLPE):** The switch sets this bit on CRC errors on TLP.
5:1	RV	0h	Reserved
0	RW1CS	0	**Receiver Error (RE):** The PCIe sets this bit when the physical layer detects a receiver error.

Table 3-71. Correctable Error Mask Register (ERRCORMSK)

ERRCORMSK
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 114h**

Bit	Attribute	Default	Description
31:14	RV	0h	Reserved
13	RWS	1	**Advisory Non-Fatal Error Mask (ANFEM):** 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from (a) signaling ERR_COR to the device control register and (b) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. ***Note:*** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	RWS	0	**Replay Timer Timeout Error Mask (RTTEM):** Mask for replay timer timeout.
11:9	RV	0h	Reserved
8	RWS	0	**Replay Number Rollover Error Mask (RNREM):** Mask for replay number rollover.
7	RWS	0	**Bad DLLP Error Mask (BDLLPEM):** Mask for bad DLLP reception.
6	RWS	0	**Bad TLP Error Mask (BTLPEM):** Mask for bad TLP reception.
5:1	RV	0h	Reserved
0	RWS	0	**Receiver Error Mask (REM):** Mask for receiver errors.

Table 3-72. Advanced Error Capabilities and Control Register (AERCAPCTL)

AERCAPCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 118h**

Bit	Attribute	Default	Description
31:9	RV	0	Reserved
8	RO	0	**ECRC Check Enable (ECE):** Not supported. Hardwired to 0.
7	RO	0	**ECRC Check Capable (ECC):** Not supported. Hardwired to 0.
6	RO	0	**ECRC Generation Enable (EGE):** Not supported. Hardwired to 0.
5	RO	0	**ECRC Generation Capable (EGC):** Not supported. Hardwired to 0.
4:0	ROS-V	0h	**First Error Pointer (FEP):** Identifies the bit position of the last error reported in the Uncorrectable Error Status Register.

Table 3-73. Header Log Register (AERHDRLOG[1-4])

AERHDRLOG
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 11Ch - 128h by 4h**

Bit	Attr	Default	Description
31:0	ROS-V	0	**TLP Header Log (TLPHDRLOG):** As soon as an error is logged in this register, it remains locked for further error-logging until the software clears the status bit that caused the header log (in other words, until the error pointer is re-armed for logging again).

Table 3-74. Root Error Command Register (ROOTERRCMD)

ROOTERRCMD
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 12Ch**

Bit	Attr	Default	Description
31:3	RV	0h	Reserved
2	RW	0h	**Fatal Error Reporting Enable (FERE):** When set, this bit enables the generation of an interrupt when a Fatal error is reported by any of the functions in the hierarchy associated with this Root Port.
1	RW	0h	**Non-Fatal Error Reporting Enable (NFERE):** When set, this bit enables the generation of an interrupt when a Non-Fatal error is reported by any of the functions in the hierarchy associated with this Root Port.
0	RW	0h	**Correctable Error Reporting Enable (CERE):** When set, this bit enables the generation of an interrupt when a Correctable error is reported by any of the functions in the hierarchy associated with this Root Port.

Table 3-75. Root Error Status Register (ROOTERRSTS)

ROOTERRSTS
Bus: 0 Device: 1-4 Function: 0 Offset: 130h

Bit	Attribute	Default	Description
31:27	RO-V	0h	**Advanced Error Interrupt Message Number (AEMN):** Not supported. Hardwired to 0.
26:7	RV	0h	Reserved
6	RW1CS	0	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	RW1CS	0	**Non-Fatal Error message Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received.
4	RW1CS	0	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	RW1CS	0	**Multiple Error Fatal/Non-Fatal Received (MEFR):** For the S12x0, only one error is captured.
2	RW1CS	0	**Error Fatal/Non-Fatal Received (EFR):** 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	RW1CS	0	**Multiple Error Correctable Error Received (MCER):** For the S12x0, only one error is captured.
0	RW1CS	0	**Correctable Error Received (CER):** 0 = No error message received. 1 = A correctable error message is received.

Table 3-76. Error Source Identification Register (ERRSRCID)

ERRSRCID
Bus: 0 Device: 1-4 Function: 0 Offset: 134h

Bit	Attribute	Default	Description
31:16	ROS-V	0	Fatal/Non-Fatal Error Source ID (EFSID): Requester ID of the source when a Fatal or Non-Fatal Error is received and the Fatal Error Message Received (FEMR) or Non-Fatal Error message Received (NFEMR) bit is not already set.
15:0	ROS-V	0	Correctable Error Source ID (ECSID): Requester ID of the source when a correctable error is received and the Correctable Error Received (CER) bit is not already set.

Table 3-77. Access Control Services Extended Capability Header (ACSCAPHDR)

ACSCAPHDR
Bus: 0 Device: 1-4 Function: 0 Offset: 138h

Bit	Attribute	Default	Description
31:20	RW-L PRST	150h	**Next Capability Offset (NCO):** Contains the offset of the next structure in the Extended Capabilities list. A value of 000h is used to indicate that this is the last capability.
19:16	RO	1h	**Capability Version (CV):** Indicates the version of the Capability structure present.
15:0	RO	000Dh	**Extended Capability ID (ECID):** Identifies the function as Access Control Services capable.

Table 3-78. Access Control Services Capability Register (ACSCAP)

ACSCAP Bus: 0		Device: 1-4	Function: 0 Offset: 13Ch
Bit	**Attribute**	**Default**	**Description**
15:8	RO	00h	**Egress Control Vector Size (ECVS):** Indicates the number of bits in the Egress Control Vector. This is set to 00h as ACS P2P Egress Control (ACSP2PEC) bit 5 in this register is 0b. These bits are hardwired to 0.
7	RV	0	Reserved
6	RO	1	**ACS Direct Translated P2P (T) (ACSDTP2P):** Indicates that the component does implement ACS Direct Translated P2P. ***Note:*** Required for Root Ports that support Address Translation Services (ATS) and also support peer-to-peer traffic with other Root Ports; required for Switch Downstream Ports.
5	RO	0	**ACS P2P Egress Control (E) (ACSP2PEC):** Hardwired to 0.Indicates that the component does not implement ACS P2P Egress Control.
4	RO	1	**ACS Upstream Forwarding (U) (ACSUF):** Indicates that the component implements ACS Upstream Forwarding.
3	RO	1	**ACS P2P Completion Redirect (C) (ACSP2PRR):** Indicates that the component implements ACS P2P Completion Redirect. ***Note:*** This includes Read Completions, AtomicOp Completions, and other Completions, either with or without data.
2	RO	1	**ACS P2P Request Redirect (R) (ACSP2PRR):** Indicates that the component implements ACS P2P Request Redirect.
1	RO	1	**ACS Translation Blocking (B) (ACSTB):** Indicates that the component implements ACS Translation Blocking.
0	RO	1	**ACS Source Validation (V) (ACSSV):** Indicates that the component implements ACS Source Validation.

Table 3-79. Access Control Services Control Register (ACSCTL)

ACSCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 13Eh**

Bit	Attribute	Default	Description
15:7	RV	00h	Reserved
6	RW	0	**ACS Direct Translated P2P Enable (T) (ACSP2PECE):** When Set, overrides the ACS P2P Request Redirect and ACS P2P Egress Control mechanisms with peer-to-peer Memory Requests whose Address Translation (AT) field indicates a Translated address. ***Note:*** This bit is ignored if ACS Translation Blocking (B) is enabled.
5	RO	0	**ACS P2P Egress Control Enable (E) (ACSP2PECE):** This is hardwired to 0b as the component does not implement ACS P2P Egress Control.
4	RW	0	**ACS Upstream Forwarding Enable (U) (ACSUFE):** When set, the component forwards upstream any Request or Completion TLPs it receives that were redirected upstream by a component lower in the hierarchy. ***Note:*** The U bit only applies to upstream TLPs arriving at a Downstream Port, and whose normal routing targets the same Downstream Port.
3	RW	0	**ACS P2P Completion Redirect Enable (C) (ACSP2PCRE):** Determines when the component redirects peer-to-peer Completions upstream; applicable only to Read Completions whose Relaxed Ordering Attribute is clear.
2	RW	0	**ACS P2P Request Redirect Enable (R) (ACSP2PRRE):** This bit determines when the component redirects peer-to-peer Requests upstream.
1	RW	0	**ACS Translation Blocking Enable (B) (ACSTBE):** When set, the component blocks all upstream Memory Requests whose Address Translation (AT) field is not set to the default value.
0	RW	0	**ACS Source Validation Enable (V) (ACSSVE):** When set, the component validates the Bus Number from the Requester ID of upstream Requests against the secondary/subordinate Bus Numbers.

Table 3-80. Uncorrectable Error Detect Mask Register (ERRUNCDETMSK)

ERRUNCDETMSK
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 140h**

Bit	Attribute	Default	Description
31:25	RV	000h	Reserved
24	RWS	0b	**AtomicOp Egress Blocked Error Detect Mask (AEBEDM)**
23	RWS	0b	**MC Blocked TLP Error Detect Mask (MCEDM)**
22	RWS	0b	**Uncorrectable Internal Error Detect Mask (UIEDM)**
21	RWS	0b	**ACS Violation Error Detect Mask (ACSEDM)**
20	RWS	0b	**Unsupported Request Error Detect Mask (UREDM)**
19	RWS	1b	**ECRC Check Error Mask (ECRCEDM):** Supported
18	RWS	0b	**Malformed TLP Error Detect Mask (MTLPEDM)**
17	RWS	0b	**Receiver Overflow Error Detect Mask (ROEDM)**
16	RWS	0b	**Unexpected Completion Error Detect Mask (UCEDM)**
15	RWS	0b	**Completer Abort Error Detect Mask (CAEDM)**
14	RWS	0b	**Completion Timeout Error Detect Mask (CTEDM)**
13	RWS	0b	**Flow Control Error Detect Mask (FCEDM)**
12	RWS	0b	**Poisoned TLP Error Detect Mask (PTLPEDM)**
11:6	RV	00h	Reserved
5	RWS	0b	**Surprise Link Down Error Detect Mask (SLDEDM)**
4	RWS	0b	**Data Link Protocol Error Detect Mask (DLPEDM)**
3:0	RV	000b	Reserved

Table 3-81. Correctable Error Detect Mask Register (ERRCORDETMSK)

ERRCORDETMSK
Bus: 0 **Device: 1-4** **Function: 0** **Offset: 144h**

Bit	Attribute	Default	Description
31:16	RV	0h	Reserved
15	RWS	0b	**Header Log Overflow Error Detect Mask (HLOEDM)**
14	RWS	0b	**Correctable Internal Error Detect Mask (CIEDM)**
13	RWS	0b	**Advisory Non-Fatal Error Detect Mask (ANFEDM)**
12	RWS	0b	**Replay Timer Timeout Error Detect Mask (RTTEDM)**
11:9	RV	0h	Reserved
8	RWS	0b	**Replay Number Rollover Error Detect Mask (RNREDM)**
7	RWS	0b	**Bad DLLP Error Detect Mask (BDLLPEDM)**
6	RWS	0b	**Bad TLP Error Detect Mask (BTLPEDM)**
5:1	RV	0h	Reserved
0	RWS	0b	**Receiver Error Detect Mask (REDM)**

Table 3-82. Root Error Detect Mask Register (ROOTERRDETMSK)

ROOTERRDETMSK
Bus: 0 Device: 1-4 Function: 0 Offset: 148h

Bit	Attribute	Default	Description
31:3	RV	0h	Reserved
2	RWS	0b	**Received Fatal Message Detect Mask (RFMDM)**
1	RWS	0b	**Received Non-Fatal Message Detect Mask (RNFMDM)**
0	RWS	0b	**Received Correctable Message Detect Mask (RCEMDM)**

3.2.3 Implementation Specific Registers

This section describes the PCI Express* Configuration Space registers that are specific to the S12x0 implementation. These registers are unique to the device.

Table 3-83. Stop and Scream Control Register (SSCTL)

SSCTL
Bus: 0 **Device: 1-4** **Function: 0** **Offset: D0h**

Bit	Attribute	Default	Description
15:9	RV	0h	Reserved
8	RW1CS	0b	**Stop and Scream Event Status (SSES)**: This bit indicates that a stop and scream event has occurred on the Tx side of the PCI Express* port due to a header or data parity error.
7:2	RV	0h	Reserved
1	RW PRST	0b	**Stop and Scream LTSSM Operation (SSLTOP):** 0 = PCIe* sets the affected link to ìlink.disabledî state when the stop and scream condition is signaled by the Transaction Layer due to poisoned data. 1 = PCIe sets the affected link to “link.disabled” state and then provide feedback to the Transaction Layer. The transaction layer then initiates a link retraining sequence via the LTSSM to bring it back alive. Sometimes the PCI Express port is not able to return to normal operation due to the nature of the error that initiated the stop and scream mechanism.
0	RW PRST	0b	**Stop and Scream Enable (SSEN):** 0 = Disable Stop and Scream (normal/default operation) 1 = Enables the link to perform Stop and Scream functionality. When this bit is set, if PCIe root port or downstream port encounters a poisoned data traversing the outbound path, the cluster stops the data, sets the link_down condition internally and places the link in disable. Inbound/outbound paths are blocked and all outstanding requests are master aborted including Memory, I/O and configuration requests.

Table 3-84. PCIe Port Definition Control Register 0 (PPD0) (Sheet 1 of 2)

PPD0 **Bus: 0** **Device: 1-4** **Function: 0** **Offset: D4h**			
Bit	**Attribute**	**Default**	**Description**
31:14	RV	0h	Reserved
13	RV	0h	Reserved
12:8	RV	0h	Reserved
7:4	RV	0h	Reserved
3	RW-LV PRST	0	**Initiate Link Training 0 (ILINKTRN0):** This bit controls PCI Express* port link training for associated ports. A value of 1 initiates link training on ports 0, 1, 2, and 3. After writing this bit to a a 1, software can poll the Data Link Layer link active bit in the LNKSTS register to determine if a port is up and running. The associated ports do not automatically initiate link training after reset unless soft strap default values have already set this bit to 1. A write of 0 has no affect. A write of 1 locks this register bit down and initiate link training. 0 = The associated PCI Express ports have not initiated link training. 1 = The associated PCI Express ports are initiating link training or have trained. ***Note:*** This bit can be written to a 1 in the same write that changes values for bits 2:0 in this register. The new value from the write to bits 2:0 take affect. The default value is determined by soft straps.
2:0	RW-LV PRST	0h	**Bifurcation Control 0 (BIFCTL0):** PPD0.BIFCTL0 is the source of bifurcation control located within the PCIe* Root Port; however, the Fabric's RP_BIFCTL register is responsible for setting up bifurcation of the PCIe Root Port Unit. 111-101: Reserved 100: x8 011: x4x4 010: x4x2x2 001: x2x2x4 000: x2x2x2x2 A write of 1 on the ILINKTRN0 locks this register field down as bifurcation control status information. ***Note:*** The default value is determined by soft straps (DSP only)
31	RWS	0b	**Disable APIC EOI Message (DEOIM):** This bit when set to 1b disables downstream forwarding of the End of Interrupt (EOI) message by the switch port. The EOI message is silently dropped.
30	RWS	0b	**GPE Enable (GPEE):** 1b: Enables "Assert GPE" (Deassert_GPE) messages to be sent from Root Port. 0b: Disables "Assert GPE" (Deassert_GPE) messages. This bit has an overriding affect to generate an ACPI HP event over traditional interrupts.
29:26	RWS	0h	**Virtual Pin Port Number (VPPN):** This field is used to identify the SMBus device and port number of the 9555 SMBus components. [29:27] = SMBus Address [26] = IO Port
25	RWS	0b	**Enable Virtual Pin Port (DVPP):** This bit when set to 1b enables the VPP pins for the given PCI Express port. 1b: VPP is enable for this PCI Express port. 0b: VPP is disable for this PCI Express port.

Table 3-84. PCIe Port Definition Control Register 0 (PPD0) (Sheet 2 of 2)

PPD0
Bus: 0 **Device: 1-4** **Function: 0** **Offset: D4h**

Bit	Attribute	Default	Description
24	RWS	0b	**Hot Plug Form Factor (HPFF):** This bit determines the what hot plug form-factor a particular port. 0: CEM/Cable 1: SIOM This bit is used to interpret bit 6 in the VPP serial stream for the port as either MRL# (CEM/Cable) or EMILS (SIOM) input.
23:18	RWS	0h	**Undefined:** Design Specific Control bits
17	RWS	0b	**Select Override Enable (SOE):** This bit when 1b enables the VPP Select Override field to program the 9555 I/O pin direction.
16	RWS	0b	**Inversion Override Enable (IOE):** This bit when 1b enables the VPP Inversion Override field to program the 9555 I/O pin polarity.
15:8	RWS	00h	**VPP Select Override (VPPSELOV):** This field is used by the HP SMBus controller to program the 9555 I/O pin direction. Each bit corresponds to a pin for the VPP. 0b: indicates input 1b: indicates output pin
7:0	RWS	00h	**VPP Inversion Override (VPPIOV):** This field is used by the HP SMBus controller to program the 9555 I/O pin polarity. Each bit corresponds to a pin for the VPP. 1b: Invert Polarity. 0b: Polarity not inverted.

Table 3-85. Personality Lock Key Control Register (PLKCTL)

PLKCTL
Bus: 0 Device: 1-4 Function: 0 Offset: EAh

Bit	Attribute	Default	Description
15:1	RV	0h	Reserved
0	RW-KL PRST	0b	**Capability Lock (CL):** Lock key bit for all RW-L bits (capabilities, next capability pointer, SSID/SVID, slot register, etc.) bits for the function. 1b: Lock 0b: Unlocked ***Note:*** This bit is self-locking. Once this bit is set to a 1b, this key bit can not be unlocked. Writing a 0b has no affect on this bit.

Table 3-86. Legacy PCI Interrupt Swizzle Control Register (INTXSWZCTL)

INTXSWZCTL
Bus: 0 Device: 1-4 Function: 0 Offset: F8h

Bit	Attribute	Default	Description
7:3	RV	0h	Reserved
2:0	RW-L PRST	0h	**INTx Swizzle (INTXSWZ):** The encoding below defines the target INTx type to which the incoming INTx message is mapped to for that port. 000b:INTA=>INTA, INTB=>INTB, INTC=>INTC, INTD=>INTD; 001b:INTA=>INTB, INTB=>INTC, INTC=>INTD, INTD=>INTA; 010b:INTA=>INTC, INTB=>INTD, INTC=>INTA, INTD=>INTB; 011b:INTA=>INTD, INTB=>INTA, INTC=>INTB, INTD=>INTC; 100b:INTA=>INTA, INTB=>INTA, INTC=>INTA, INTD=>INTA;

Table 3-87. Configuration Agent Error Register (CFGAGTERR)

CFGAGTERR
Bus: 0 Device: 1-4 Function: 0 Offset: FCh

Bit	Attribute	Default	Description
31:12	RV	0h	Reserved
11	RV	0b	Reserved
10	RW1CS	0b	**Data Parity Error Status (DPES)**
9	RV	0b	Reserved
8	RW1CS	0b	**Transaction Layer Internal Parity Error Status (TLIPES)**
7	RW1CS	0b	**Link Layer Internal Parity Error Status (LLIPES)**
6	RW1CS	0b	**Physical Layer Internal Parity Error Status (PLIPES)**
5	RV	0b	Reserved
4	RWS	0b	**Data Parity Error Mask (DPEM)**
3	RV	0b	Reserved
2	RWS	0b	**Transaction Layer Internal Parity Error Mask (TLIPEM)**
1	RWS	0b	**Link Layer Internal Parity Error Mask (LLIPEM)**
0	RWS	0b	**Physical Layer Internal Parity Error Mask (PLIPEM)**

3.3 SMBus 2.0 Controller Registers

Table 3-88. Register Summary

Offset (h)	Size (bits)	Name
00	16	"Vendor Identification Register (VID)" on page 74
02	16	"Device Identification Register (DID)" on page 74
04	16	"PCI Command Register (PCICMD)" on page 75
06	16	"PCI Status Register (PCISTS)" on page 76
08	8	"Revision Identification Register (RID)" on page 76
09	24	"Class Code Register (CCR)" on page 77
10	64	"SMBus Base Address Register (SMBus ControllerBAR)" on page 77
2C	16	"Subsystem Vendor Identification Register (SVID)" on page 77
2E	16	"Subsystem Identification Register (SID)" on page 77
34	8	"Capabilities Pointer Register (CAPPTR)" on page 78
3C	8	"Interrupt Line Register (INTL)" on page 78
3D	8	"Interrupt Pin Register (INTP)" on page 78
40	16	""PCI Express Capability List Register (EXPCAPLST)" on page 78
42	16	"PCI Express Capabilities Register (EXPCAP)" on page 79
44	32	"Device Capabilities Register (DEVCAP)" on page 79
48	16	"Device Control Register (DEVCTL)" on page 80
4A	16	"Device Status Register (DEVSTS)" on page 81
64	32	"Device Capabilities 2 Register (DEVCAP2)" on page 82
68	16	"Device Control 2 Register (DEVCTL2)" on page 83
6A	16	"Device Status 2 Register (DEVSTS2)" on page 83
80	16	"Power Management Capability List Register (PMCAPLST)" on page 83
82	16	"Power Management Capabilities Register (PMCAP)" on page 84
84	32	"Power Management Control/Status Register (PMCSR)" on page 85
8C	16	"MSI Capability List Register (MSICAPLST)" on page 85
8E	16	"MSI Message Control Register (MSICTL)" on page 86
90	64	"MSI Message Address Register (MSIADDR)" on page 86
98	32	"MSI Message Data Register (MSIDATA)" on page 87
9C	32	"MSI Mask Bit Register (MSIMSK)" on page 87
A0	32	"MSI Pending Bit Register (MSIPENDING)" on page 87
EA	16	"Personality Lock Key Control Register (PLKCTL)" on page 88
100	16	"Advanced Error Reporting Extended Capability Header (AERCAPHDR)" on page 88
104	32	"Uncorrectable Error Status Register (ERRUNCSTS)" on page 89
108	32	"Uncorrectable Error Mask Register (ERRUNCMSK)" on page 90
10C	32	"Uncorrectable Error Severity Register (ERRUNCSEV)" on page 91
110	32	"Correctable Error Status Register (ERRCORSTS)" on page 92
114	32	"Correctable Error Mask Register (ERRCORMSK)" on page 92
118	32	"Advanced Error Capabilities and Control Register (AERCAPCTL)" on page 93
11C	32	"Header Log Register (AERHDRLOG[1-4])" on page 93

3.3.1 PCI Configuration Registers (SMBus—Bus 0:D19:F0-1)

Table 3-89. Vendor Identification Register (VID)

VID **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 00h**			
Bit	**Attribute**	**Default**	**Description**
15:00	RO	8086h	**Vendor ID (VID):** This is the standard 16-bit value assigned to Intel by PCI-SIG.

Table 3-90. Device Identification Register (DID)

DID **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 02h**			
Bit	**Attribute**	**Default**	**Description**
15:00	RO-V	Fun 0: 0C59h 1: 0C5Ah	**Device ID (DID):** This is a 16-bit value assigned to the S12x0 SMBus controller.

Table 3-91. PCI Command Register (PCICMD)

PCICMD
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 04h**

Bit	Attribute	Default	Description
15:11	RV	00000b	Reserved
10	RW	0b	**Interrupt Disable (INTxD):** Controls the ability to generate legacy INTx interrupt messages. 0 = Enable. 1 = Disables SMBus to assert its PIRQB# signal.
9	RO	0b	**Fast Back to Back Enable (FBE):** Hardwired to 0
8	RW	0b	**SERR# Enable (SEE):** This bit indicates whether the device is allowed to signal a PCIe* SERR condition. 0 = Enables SERR# generation. 1 = Disables SERR# generation.
7	RO	0b	**Wait Cycle Control (WCC)**: Hardwired to 0.
6	RW	0b	**Parity Error Response (PERE):** This bit controls the setting of the master data parity error bit in the Status Register in response to a parity error received. 0 = Disable. 1 = Enable to report parity errors.
5	RO	0b	**VGA Palette Snoop Enable (VGA_PSE):** Hardwired to 0.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE)**: Hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Hardwired to 0.
2	RW	0b	**Bus Master Enable (BME):** Controls the ability of this device to initiate transactions to memory including MMIO. 0 = Not allowed to issue any memory requests. 1 = Allowed to issue memory requests.
1	RW	0b	**Memory Space Enable (MSE):** Controls whether the device responds to memory space transactions as located by its memory space Base Address Register (BAR). 0 = Disables memory mapped config space. 1 = Enables memory mapped config space.
0	RO	0b	**I/O Space Enable (IOSE):** I/O BAR not used. Hardwired to 0.

Table 3-92. PCI Status Register (PCISTS)

PCISTS
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 06h**

Bit	Attribute	Default	Description
15	RW1C	0b	**Detected Parity Error (DPE):** 0 = No parity error detected. 1 = Parity error detected.
14	RW1C	0b	**SERR# Asserted (SSE):** 0 = No system error detected. 1 = System error detected.
13	RW1C	0b	**Received Master Abort (RMA):** 0 = No Master Abort received. 1 = Master abort on a transaction it has mastered.
12	RW1C	0b	**Received Target Abort (RTA):** This bit is set when device accesses to SoC Fabric return a failed completion status. 0 = No Target Abort received. 1 = Failed completion status received.
11	RW1C	0b	**Signaled Target Abort (STA):** The IPI interface of the SMBus Controller flags a completer abort for requests to its MMIO space that are greater than 8B in length. 0 = No Signaled Target Abort. 1 = Request to SMBUS MMIO space greater than 8B in length.
10:9	RO	00b	**DEVSEL# Timing (DVT):** Hardwired to 0.
8	RW1C	0b	**Master Data Parity Error (MDPD):** This bit is set if the Parity Error Response bit in the PCI Command register set is set and it receives a completion with poisoned data from SoC Fabric. 0 = No data parity error. 1 = Received completion with poisoned data when Parity Error Response but is set.
7	RO	0b	**Fast Back-to-Back (FBC):** Hardwired to 0.
6	RV	0b	Reserved
5	RO	0b	**66 MHz Capable (C66):** Hardwired to 0.
4	RO	1b	**Capabilities List (CAPE):** This bit indicates that this device implements a PCI Capability list. See offset 34h which indicates the offset for the first entry in the linked list of capabilities.
3	RO-V	0b	**Interrupt Status (INTS):** Hardwired to 0.
2:0	RV	000b	Reserved

Table 3-93. Revision Identification Register (RID)

RID
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 08h**

Bit	Attribute	Default	Description
7:0	ROS-V	00h	**Revision ID (RID):** This value is initially 0 for the first release and is incremented for subsequent releases in order to identify any changes.

Table 3-94. Class Code Register (CCR)

CCR
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 09h**

Bit	Attribute	Default	Description
23:16	RW-O PRST	08h	**Base Class (BASE):** Indicates it is a “Generic System Peripheral.”
15:8	RW-O PRST	80h	**Sub Class (SUB):** Indicates “Other System Peripheral.”
7:0	RW-O PRST	00h	**Register-Level Programming Interface (RLPI):** This field is hardwired to 00h.

Table 3-95. SMBus Base Address Register (SMBus ControllerBAR)

SMBus ControllerBAR
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 10h**

Bit	Attribute	Default	Description
63:10	RW	000000h	**Base Address (MBA):** Provides Memory Base address of SMBus control registers.
9:4	RO	0h	**Memory Size (MS):** Reserved
3	RO	0b	**Prefetchable (PFMEM):** This bit is hardwired to 0b to indicate non-prefetchable.
2:1	RO	10b	**Type (MTYPE):** The SMBus MMIO registers have the ability to be relocated anywhere within 64-bit address space.
0	RO	0b	**Memory space indicator (MSI):** Hardwired to 0 to indicate that this is a memory space BAR.

Table 3-96. Subsystem Vendor Identification Register (SVID)

SVID
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 2Ch**

Bit	Attribute	Default	Description
15:0	RW-O PRST	8086h	**Subsystem Vendor ID (SVID):** This register uniquely identifies the add-in board or subsystem vendor.

Table 3-97. Subsystem Identification Register (SID)

SID
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 2Eh**

Bit	Attribute	Default	Description
15:0	RW-O PRST	0000h	**Subsystem ID (SID):** Uniquely identifies the add-in board or subsystem.

Table 3-98. Capabilities Pointer Register (CAPPTR)

CAPPTR
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 34h**

Bit	Attribute	Default	Description
7:0	RW-O PRST	40h	**Capability List Pointer (CPTR):** This provides an offset in the SMBus controller configuration space that points to the PCI Bus Power Management extended capability (Table 3-34, "PCI Express Capability List Register (EXPCAPLST)" on page 41).

Table 3-99. Interrupt Line Register (INTL)

INTL
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 3Ch**

Bit	Attribute	Default	Description
7:0	RW	0h	**Interrupt Assigned (INTL):** system-assigned value identifies which system interrupt controller's interrupt request has the device's PCI interrupt request routed to it (as specified in the interrupt pin register). A value of FFH signifies "no connection" or "unknown."

Table 3-100. Interrupt Pin Register (INTP)

INTP
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 3Dh**
(LockKey: PLKCTL)

Bit	Attribute	Default	Description
7:0	RW-L PRST	01h	**Interrupt Pin (INTP):** Indicates which INTx assert/deassert legacy interrupt messages are used. 01h: Generate INTA 02h: Generate INTB 03h: Generate INTC 04h: Generate INTD Others: Reserved BIOS has the ability to write this register once during boot to setup the correct interrupt for the function.

Table 3-101."PCI Express Capability List Register (EXPCAPLST)

EXPCAPLST
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 40h**

Bit	Attribute	Default	Description
15:8	RO	80h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list (Table 3-53, "Power Management Capability List Register (PMCAPLST)" on page 54).
7:0	RO	10h	**Capability ID (CAPID):** Identifies the function as PCI Express* capable.

Table 3-102. PCI Express Capabilities Register (EXPCAP)

EXPCAP
Bus: 0 Device: 19 Function: 0-1 Offset: 42h

Bit	Attribute	Default	Description
15:14	RV	0h	Reserved
13:9	RO	0h	**Interrupt Message Number (IMN):** Hardwired to 0.
8	RO	0b	**Slot Implemented (SI):** Hardwired to 0.
7:4	RO	1001b	**Device/Port Type (DT):** SMBus controller represents a Root Complex Integrated Endpoint.
3:0	RO	2h	**Version Number (VN):** These bits indicate the version number of the PCI Express capability structure.

Table 3-103. Device Capabilities Register (DEVCAP)

DEVCAP
Bus: 0 Device: 19 Function: 0-1 Offset: 44h

Bit	Attribute	Default	Description
31:29	RV	0h	Reserved
28	RW-KO PRST	1b	**Function Level Reset Capability (FLR):** This field when set indicates this function supports function Level Reset mechanism. Lock key bit for DEVCTL.IFLR. 0b: Lock 1b: Unlocked
27:26	RO	00b	**Captured Slot Power Limit Scale** (CSPLS): Hardwired to 0.
25:18	RO	0h	**Captured Slot Power Limit Value** (CSPLV): Hardwired to 0.
17:16	RV	00b	Reserved
15	RO	1b	**Role-Based Error Reporting (RBER):** The SMBus Controller supports Role-based Error Reporting.
14:12	RO	0h	Undefined
11:9	RO	000b	**Endpoint L1 Acceptable Latency (EPL1AL):** These bits are hardwired to 0.
8:6	RO	000b	**Endpoint L0s Acceptable Latency (EPL0AL):** These bits are hardwired to 0.
5	RO	0b	**Extended Tag Field Supported (ETFG):** Hardwired to 0.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Phantom functions not supported. Hardwired to 0.
2:0	RO	001	**Max Payload Size Supported (MPSS):** Maximum supported payload is 256 byte packets.

Table 3-104. Device Control Register (DEVCTL)

DEVCTL **Bus: 0**	**Device: 19**	**Function: 0-1**	**Offset: 48h**
Bit	**Attribute**	**Default**	**Description**
15	RW-LV NFLRST	0b	**Initiate Function Level Reset (IFLR):** A write of 1 initiates Function Level Reset. The value read by software from this bit is always 0b.
14:12	RO	000b	**Max_Read_Request_Size (MRRS):** Functions that do not generate Read Requests larger than 128B and functions that do not generate Read Requests on their own behalf are permitted to implement this field as Read Only (RO) with a value of 000b. These bits are hardwired to 0.
11	RW	0b	**Enable No Snoop (ENOSNP):** 0 = SMBUs Controller not allowed to set the No Snoop Bit. 1 = SMBus Controller is permitted to set the No Snoop bit in the Requester attributes of transactions it initiates that do not require hardware enforced cache coherency.
10	RO	0b	**Auxiliary Power PM Enable (AUXPME):** Not supported.
9	RO	0b	**Phantom Function Enable (PFE):** Phantom Functions not supported. Hardwired this bit to 0b.
8	RO	0b	**Extended Tag Field Enable (ETFE):** ETFE not supported. Hardwire this bit to 0b.
7:5	RW NFLRST	000b	**Maximum Payload Size (MPS):** This field sets maximum TLP payload size for the function. 000b: 128 bytes maximum payload size (default) 001b: 256 bytes maximum payload size Others: Reserved
4	RO	0b	**Enable Relaxed Ordering (ENRO):** ENRO not supported. Hardwire this bit to 0b.
3	RW	0b	**Unsupported Request Reporting Enable (URRE):** This bit controls the enabling of ERR_CORR, ERR_NONFATAL, or ERR_FATAL messages for reporting “Unsupported Request” errors.
2	RW	0b	**Fatal Error Reporting Enable (FERE):** When this bit is set, generation of the ERR_FATAL message is enabled.
1	RW	0b	**NonFatal Error Reporting Enable (NFERE):** When this bit is set, generation of the ERR_NONFATAL message is enabled.
0	RW	0b	**Correctable Error Reporting Enable (CERE):** When this bit is set, generation of the ERR_CORR message is enabled.

Table 3-105. Device Status Register (DEVSTS)

DEVSTS
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 4Ah**

Bit	Attribute	Default	Description
15:6	RV	000h	Reserved
5	RO-V	0b	**Transactions Pending (TP):** When set, this bit indicates that the device has issued non-posted PCI Express* transactions which have not yet completed. When all pending non-posted transactions have completed, this bit gets cleared by the hardware.
4	RO	0b	**Auxiliary Power Detected (APD):** Auxiliary Power is not supported.
3	RW1C	0b	**Unsupported Request Detected (URD):** This bit indicates that this function received an unsupported request from PCI Express link. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
2	RW1C	0b	**Fatal Error Detected (FED):** This bit indicates that the function has detected a Fatal error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	RW1C	0b	**Non-Fatal Error Detected (NFED):** This bit indicates that the function has detected a Non-Fatal error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	RW1C	0b	**Correctable Error Detected (CED):** This bit indicates that the function has detected a Correctable error. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.

Table 3-106. Device Capabilities 2 Register (DEVCAP2)

DEVCAP2
Bus: 0 Device: 19 Function: 0-1 Offset: 64h

Bit	Attribute	Default	Description
31:20	RV	0	Reserved
19:18	RO	00b	**OBFF Supported (OBFFS):** 00b: OBFF Not Supported 01b: OBFF supported using Message signaling only 10b: Reserved 11b: OBFF supported using WAKE# and Message signaling Applicable only to Root Ports, Switch Ports, and Endpoints that support this capability. Must be 00b for other function types.
17:14	RV	0h	Reserved
13:12	RO	00b	**TPH Completer Supported (TPHCS):** TPH and Extended TPH Completer not supported. Hardwired to 0.
11	RO	0b	**LTBWR Mechanism Supported (LTBWRMS):** Hardwired to 0.
10	RO	0b	**No RO-enabled PR-PR Passing (NROEPRPASS):** Hardwired to 0.
9	RO	0	**AD128 CAS Completer Supported (AD128ACS):** Hardwired to 0.
8	RO	0	**AD64-bit AtomicOp Completer Supported (AD64ACS):** Hardwired to 0.
7	RO	0	**AD32 bit AtomicOp Completer Supported (AD32ACS):** Hardwired to 0.
6	RO	0	**AtomicOp Routing Supported (ARS):** Hardwired to 0.
5	RO	0	**Alternative RID Interpretation Capable (ARI):** Hardwired to 0.
4	RO	1	**Completion Timeout Disable Support (CTDS):** A value of 1b indicates support for the completion Timeout Disable Mechanism. SMBus Controller supports completions timeout disable.
3:0	RW-L PRST	0000b	**Completion Timeout Range Supported (CTRS):** This field indicates device support for the optional Completion Timeout programmability mechanism. This mechanism allows system software to modify the Completion Timeout value. This field is applicable only to Endpoints that issue requests on their own behalf, and PCI Express* to PCI/PCI-X Bridges that take ownership of request issues on PCI Express. Four time values ranges are defined in PCI Express 2.0: Range A: 50 µs to 10 ms Range B: 10 ms to 250 ms Range C: 250 ms to 4s Range D: 4s to 64s The SMBus Controller supports the following ranges for completion timeout 0000: Completion Timeout not supported (see DEVCTL2.CTV) 0001: Range A 0010: Range B 0011: Ranges A and B Others: Reserved

Table 3-107. Device Control 2 Register (DEVCTL2)

DEVCTL2
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 68h**

Bit	Attribute	Default	Description
15	RV	0	Reserved
14:13	RO	00b	**OBFF Enable (OBFFE):** Hardwired to 0.
12:11	RV	0	Reserved
10	RO	0b	**LTBWR Mechanism Enable (LTBWRME):** Hardwired to 0.
9	RO	0b	**IDO Completion Enable (IDOCE):** Hardwired to 0.
8	RO	0b	**IDO Request Enable (IDORE):** Hardwired to 0.
7	RO	0	**AtomicOp Egress Blocking (AEB):** Hardwired to 0.
6	RO	0	**AtomicOp Requester Enable (ARE):** Hardwired to 0.
5	RO	0	**Alternative RID Interpretation Enable (ARIE):** Hardwired to 0.
4	RW	0	**Completion Timeout Disable (CTD):** 1 = Disable the completions timeout mechanism for all NP transactions. 0 = Completion timeout is enabled for all NP transactions.
3:0	RW	0000b	**Completion Timeout Value (CTV):** In devices that support completion timeout programmability, this field allows system software to modify the completion timeout range. Supported values are: 0000b: 50 µs - 50 ms (default) 0001b: 50 µs - 100 µs (Range A) 0010b: 1 ms - 10 ms (Range A) 0101b: 16 ms - 55 ms (Range B) 0110b: 65 ms - 210 ms (Range B) All other values are reserved.

Table 3-108. Device Status 2 Register (DEVSTS2)

DEVSTS2
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 6Ah**

Bit	Attribute	Default	Description
15:0	RV	0	Reserved

Table 3-109. Power Management Capability List Register (PMCAPLST)

PMCAPLST
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 80h**

Bit	Attribute	Default	Description
15:8	RO	8Ch	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list (Table 3-60, “MSI Capability List Register (MSICAPLST)” on page 57).
7:0	RO	01h	**Capability ID (CAPID):** Identifies the function as PCI Power Management capable.

Table 3-110. Power Management Capabilities Register (PMCAP)

PMCAP
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 82h**

Bit	Attribute	Default	Description
15:11	RO	0h	**PME_Support (PMES):** These bits are hardwired to 0.
10	RO	0b	**D2 Support (D2S):** Not supported.
9	RO	0b	**D1 Support (D1S):** Not supported.
8:6	RO	000b	**Auxiliary Current (AC):** Auxiliary power is not supported.
5	RO	0b	**Device Specific Initialization (DSI):** Device-specific initialization is not required when transitioning to D0 from D3hot state. This bit is hardwired to 0.
4	RV	0b	Reserved
3	RO	0b	**PME Clock (PMECLK):** Does not apply to PCI Express*. Hardwired to 0.
2:0	RO	3h	**Version (VER):** The PM implementation in the PCIe* cluster is compliant with *PCI Bus Power Management Interface Specification*, Revision 1.2.

Table 3-111. Power Management Control/Status Register (PMCSR)

PMCSR **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 84h** **(LockKey: PLKCTL)**			
Bit	**Attribute**	**Default**	**Description**
31:24	RO	00h	**Data (Data):** This does not apply to SMBus Controller.
23	RO	0b	**Bus Power/Clock Control Enable (BPCC_EN):** Neither bus or clock control of PCI is supported when in D3hot state. This bit is hardwired to 0.
22	RO	0b	**B2/B3# (B23EN):** Not supported. This bit has no meaning since the BPCC_EN bit is hardwired to 0.
21:16	RV	00h	Reserved
15	RO	0	**PME Status (PMESTS):** Applies only to RPs. This bit has no meaning for SMBus Controller.
14:13	RO	0h	**Data Scale (DC):** Not supported.
12:9	RO	0h	**Data Select (DS):** Not supported.
8	RWS	0	**PME En (PMEEN):** Gates assertion of the PME message. 0 = Disable ability to send PME messages when an event occurs 1 = Enables ability to send PME messages when an event occurs ***Note:*** This bit has no meaning for SMBus Controller.
7:4	RV	0h	Reserved
3	RW-L PRST	1b	**No Soft Reset (NSR)**: This bit when 1b indicates that a device transitioning from D3hot to D0 does not perform an internal reset. The configuration context is preserved. ***Note:*** BIOS must lock the register after loading the correct value needed. Preferred value is 1.
2	RV	0h	Reserved
1:0	RW-R	0h	**Power State (PS):** This field is used both to determine the current power state of a function and to set the function into a new power state. The definition of the supported values is given below: 00: D0 01: D1 (not supported by SMBus Controller) 10: D2 (not supported by SMBus Controller) 11: D3_hot If software tries to write 01 or 10 to this field, the power state does not change from the existing power state (which is either D0 or D3hot) and nor do these bits 1:0 change value. ("Restricted" register definition.) As an aside, all devices respond to only Type 0 configuration transactions when in D3hot state and do not respond to memory and I/O transactions (i.e., D3hot state is equivalent to MSE/IOSE bits being clear) as target and do not generate any memory, I/O, and configuration transactions as initiator on the primary bus (messages are still allowed to pass through). ***Note:*** The SMBus Controller design can implement power optimization in D3hot including but not limited to schemes such as clock gating (coarse/fine grain), PLL shutoff, and CPPM.

Table 3-112. MSI Capability List Register (MSICAPLST)

MSICAPLST **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 8Ch**			
Bit	**Attribute**	**Default**	**Description**
15:8	RO	00h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list.
7:0	RO	05h	**Capability ID (CAPID):** Identifies the function as MSI capable.

Table 3-113. MSI Message Control Register (MSICTL)

MSICTL
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 8Eh**

Bit	Attribute	Default	Description
15:9	RV	00h	Reserved
8	RO	1b	**Per-vector masking capable (PVM):** This bit indicates that this device supports MSI per-vector masking.
7	RO	1b	**Address 64-Bit Capable (AD64C):** When set, this bit indicates that this function is capable of generating a 64-bit message address. 1 = Function is capable of sending 64-bit message address. 0 = Function is not capable of sending 64-bit message address.
6:4	RW	000b	**Multiple Message Enable (MMEN):** These bits are R/W for software compatibility. SMBus Controller supports only one message. 000b = 1 Message others = Reserved
3:1	RO	000b	**Multiple Message Capable (MMC):** SMBus Controller supports only one MSI message. (power of 2) There is no option of supporting multiple messages.
0	RW	0b	**MSI Enable (MSIE):** When set, MSI is enabled and traditional interrupt pins are not used to generate interrupts. ***Note:*** Software must disable INTx and MSI-X for this device when using MSI.

Table 3-114. MSI Message Address Register (MSIADDR)

MSIADDR
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 90h**

Bit	Attribute	Default	Description
63:2	RW	00000000h	**Address (ADDR):** Message address specified by the system, always Dword aligned.
1:0	RV	00b	Reserved

Table 3-115. MSI Message Data Register (MSIDATA)

MSIDATA **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 98h**			
Bit	**Attribute**	**Default**	**Description**
31:16	RV	0000h	Reserved
15	RW	0h	**Trigger Mode (TM):** 0 = Edge Triggered 1 = Level Triggered
14	RW	0h	**Level (LVL):** If TM is 0h, then this field is a (don't care). Edge-triggered messages are always treated as assert messages. If TM is 1h, then: 0 = Deassert Messages 1 = Assert Messages For level-triggered interrupts, this bit reflects the state of the interrupt input.
13:12	RW	0h	**Future (Future):** These bits are (don't care) for an IOxAPIC interrupt message data field specification.
11:8	RW	0h	**Delivery Mode (DM):** 0000: Fixed: Trigger Mode can be edge or level. 0001: Lowest Priority: Trigger Mode can be edge or level. 0010: SMI/PMI/MCA - Not supported via MSI of root port 0011: Reserved - Not supported via MSI of root port 0100: NMI - Not supported via MSI of root port 0101: INIT - Not supported via MSI of root port 0110: Reserved 0111: ExtINT - Not supported via MSI of primary port 1000 -1111 - Reserved
7:0	RW	0h	**Interrupt Vector (IV):** The interrupt vector (LSB) is modified by the IIO to provide context-sensitive interrupt information for different events that require attention from the processor. e.g Hot plug, Power Management and RAS error events.

Table 3-116. MSI Mask Bit Register (MSIMSK)

MSIMSK **Bus: 0** **Device: 19** **Function: 0-1** **Offset: 9Ch**			
Bit	**Attribute**	**Default**	**Description**
31:1	RV	0h	Reserved
0	RW	0b	**Mask Bits (MSKB):** For each Mask bit that is set, the PCI Express* port is prohibited from sending the associated message. The SMBus Controller supports 1 MSI message. Corresponding bits are masked if set to 1.

Table 3-117. MSI Pending Bit Register (MSIPENDING)

MSIPENDING **Bus: 0** **Device: 19** **Function: 0-1** **Offset: A0h**			
Bit	**Attribute**	**Default**	**Description**
31:1	RV	0h	Reserved
0	RO-V	0h	**Pending Bits (PB):** For each Pending bit that is set, the PCI Express* port has a pending associated message.

Table 3-118. Personality Lock Key Control Register (PLKCTL)

PLKCTL
Bus: 0 **Device: 19** **Function: 0-1** **Offset: EAh**

Bit	Attribute	Default	Description
15:1	RV	0h	Reserved
0	RW-KL PRST	0b	**Capability Lock (CL):** Lock key bit for all RW-L bits (capabilities, next capability pointer, SSID/SVID, slot register, etc.) bits for the function.This bit is self-locking. Once this bit is set to a 1b, this key bit can not be unlocked. Writing a 0b has no affect on this bit. 1b: Lock 0b: Unlocked

Table 3-119. Advanced Error Reporting Extended Capability Header (AERCAPHDR)

AERCAPHDR
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 100h**
(LockKey: PLKCTL)

Bit	Attribute	Default	Description
31:20	RW-L PRST	0h	**Next Capability Offset (NCO):** Contains the offset of the next structure in the Extended Capabilities list. Hardwired to 0.
19:16	RO	1h	**Capability Version (CV):** Indicates the version of the Capability structure present.
15:0	RO	0001h	**Extended Capability ID (EXCAPID):** Identifies the function as Advanced Error Reporting capable.

Table 3-120. Uncorrectable Error Status Register (ERRUNCSTS)

ERRUNCSTS
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 104h**

Bit	Attribute	Default	Description
31:23	RV	000h	Reserved
22	RW1CS	0b	**Uncorrectable Internal Error (UIE):** This bit is set whenever the SMBus Controller detects an uncorrectable internal error specific to the unit. Refer to the SMBus Controller chapter for internal errors.
21	RO	0b	**ACS Violation Error (ACSE):** This bit is set whenever an ACS violation is detected by the PCI Express* port. Not applicable to SMBus Controller. Hardwired to 0.
20	RW1CS	0b	**Unsupported Request Error (URE):** As a receiver, the SMBus Controller sets this bit whenever an unsupported request (negatively decoded transaction) is detected. The Header is logged.
19	RO	0b	**ECRC Check Error (ECRCE):** The SMBus Controller does not support ECRC checks. Hardwired to 0.
18	RW1CS	0b	**Malformed TLP Error (MTLPE):** The SMBus Controller sets this bit if a malformed TLP is detected on the internal SoC Fabric interface. (e.g., Max Payload violation or other packet errors.) The Header is logged.
17	RO	0b	**Receiver Overflow Error (ROE):** Not applicable to SMBus Controller. Hardwired to 0.
16	RW1CS	0b	**Unexpected Completion Error (UCE):** This bit is set whenever a completion is received with a requestor ID or tag that does not match. Header logging is performed.
15	RW1CS	0b	**Completer Abort Error (CAE):** This bit is set when the internal agent signals a data abort to the unit. The header is logged.
14	RW1CS	0b	**Completion Timeout Error (CTE):** The SMBus Controller issues completion timeout at the IPI interface when the timer rolls over for unreturned NP transactions.
13	RO	0b	**Flow Control Error (FCE):** Not applicable to SMBus Controller. Hardwired to 0.
12	RW1CS	0b	**Poisoned TLP Error (PTLPE):** This bit is set and the SMBus Controller logs the header when a poisoned TLP is received from the internal fabric.
11:6	RV	00h	Reserved
5	RO	0b	**Surprise Link Down Error (SLDE):** Hardwired to 0.
4:0	RV	000b	Reserved

Table 3-121. Uncorrectable Error Mask Register (ERRUNCMSK)

ERRUNCMSK
Bus: 0 Device: 19 Function: 0-1 Offset: 108h

Bit	Attribute	Default	Description
31:25	RV	0h	Reserved
24	RO	0b	**AtomicOp Egress Blocked Error Mask (AEBEM)**: Not supported.
23	RO	0b	**MC Blocked TLP Error Mask (MCEM):** Not supported.
22	RWS	0b	**Uncorrectable Internal Error Mask (UIEM)**
21	RO	0b	**ACS Violation Error Mask (ACSEM):** Not supported.
20	RWS	0b	**Unsupported Request Error Mask (UREM)**
19	RO	0b	**ECRC Check Error Mask (ECRCEM):** Not supported.
18	RWS	0b	**Malformed TLP Error Mask (MTLPEM)**
17	RO	0b	**Receiver Overflow Error Mask (ROEM):** Not supported.
16	RWS	0b	**Unexpected Completion Error Mask (UCEM)**
15	RWS	0b	**Completer Abort Error Mask (CAEM)**
14	RWS	0b	**Completion Timeout Error Mask (CTEM)**
13	RO	0b	**Flow Control Error Mask (FCEM):** Not supported.
12	RWS	0b	**Poisoned TLP Error Mask (PTLPEM)**
11:6	RV	00h	Reserved
5	RO	0b	**Surprise Link Down Error Mask (SLDEM)**: Not supported.
4	RO	0b	**Data Link Protocol Error Mask (DLPEM):** Not supported.
3:0	RV	000b	Reserved

Table 3-122. Uncorrectable Error Severity Register (ERRUNCSEV)

ERRUNCSEV **Bus: 0**		**Device: 19**	**Function: 0-1** **Offset: 10Ch**
Bit	**Attribute**	**Default**	**Description**
31:25	RV	000h	Reserved
24	RO	0b	**AtomicOp Egress Blocked Severity (AEBES)**
23	RO	0b	**MC Blocked TLP Error Severity (MCES):** Not supported.
22	RWS	1b	**Uncorrectable Internal Error Severity (UIES)**
21	RO	0b	**ACS Violation Error Severity (ACSES):** Not supported.
20	RWS	0b	**Unsupported Request Error Status Severity (URES)**
19	RO	0b	**ECRC Check Error Severity (ECRCES):** Not supported.
18	RWS	1b	**Malformed TLP Error Severity (MTLPES)**
17	RO	0b	**Receiver Overflow Error Severity (ROES):** Not supported.
16	RWS	0b	**Unexpected Completion Error Severity (UCES)**
15	RWS	0b	**Completer Abort Error Severity (CAES)**
14	RWS	0b	**Completion Timeout Error Severity (CTES)**
13	RO	0b	**Flow Control Error Severity (FCES)**
12	RWS	0b	**Poisoned TLP Error Severity (PTLPES)**
11:6	RV	00h	Reserved
5	RO	0b	Surprise Link Down Severity (SLDES)
4	RO	0b	**Data Link Protocol Error Severity (DLPES)**
3:0	RV	000b	Reserved

Table 3-123. Correctable Error Status Register (ERRCORSTS)

ERRCORSTS
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 110h**

Bit	Attribute	Default	Description
31:16	RV	0h	Reserved
15	RO	0	**Header Log Overflow Error (HLOE)**
14	RW1CS	0	**Correctable Internal Error (CIE):** The SMBus Controller logs this bit for any local storage (SRAM) ECC correctable errors during data read operations. This can be used for QRE and other statistical analysis on soft errors and frequency of occurrence in the block.
13	RW1CS	0	**Advisory Non-Fatal Error (ANFE)**
12	RO	0	**Replay Timer Timeout Error (RTTE):** The PCIe* sets this bit when replay timer time-out occurs.
11:9	RV	0h	Reserved
8	RO	0	**Replay Number Rollover Error (RNRE):** The PCIe sets this bit when the replay number rolls over from 11 to 00.
7	RO	0	**Bad DLLP Error (BDLLPE):** The switch sets this bit on CRC errors on DLLP.
6	RO	0	**Bad TLP Error (BTLPE):** The switch sets this bit on CRC errors on TLP.
5:1	RV	0h	Reserved
0	RO	0	**Receiver Error (RE):** The PCIe sets this bit when the physical layer detects a receiver error.

Table 3-124. Correctable Error Mask Register (ERRCORMSK)

ERRCORMSK
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 114h**

Bit	Attribute	Default	Description
31:16	RV	0h	Reserved
15	RO	0	**Header Log Overflow Error Mask (HLOEM)**
14	RWS	0	**Correctable Internal Error Mask (CIEM)**
13	RWS	1	**Advisory Non-Fatal Error Mask (ANFEM)**
12	RO	0	**Replay Timer Timeout Error Mask (RTTEM)**
11:9	RV	0h	Reserved
8	RO	0	**Replay Number Rollover Error Mask (RNREM)**
7	RO	0	**Bad DLLP Error Mask (BDLLPEM)**
6	RO	0	**Bad TLP Error Mask (BTLPEM)**
5:1	RV	0h	Reserved
0	RO	0	**Receiver Error Mask (REM)**

Table 3-125. Advanced Error Capabilities and Control Register (AERCAPCTL)

AERCAPCTL
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 118h**

Bit	Attribute	Default	Description
31:11	RV	0	Reserved
10	RO	0	**Multiple Header Recording Enable (MHRE):** Not supported. Hardwired to 0.
9	RO	0	**Multiple Header Recording Capable (MHRC):** Not supported. Hardwired to 0
8	RO	0	**ECRC Check Enable (ECE):** Not supported. Hardwired to 0.
7	RO	0	**ECRC Check Capable (ECC):** Not supported. Hardwired to 0.
6	RO	0	**ECRC Generation Enable (EGE):** Not supported. Hardwired to 0.
5	RO	0	**ECRC Generation Capable (EGC):** Not supported. Hardwired to 0.
4:0	ROS-V	0h	**First Error Pointer (FEP):** This field identifies the bit position of the first error reported in the Uncorrectable Error Status Register. This register re-arms itself (which does not change its current value) as soon as the error status bit indicated by the pointer is cleared by the software by writing a 1 to that status bit.

Table 3-126. Header Log Register (AERHDRLOG[1-4])

AERHDRLOG
Bus: 0 **Device: 19** **Function: 0-1** **Offset: 11Ch - 128h by 4h**

Bit	Attribute	Default	Description
31:0	ROS-V	0	**TLP Header Log (TLPHDRLOG):** As soon as an error is logged in this register, it remains locked for further error-logging until the software clears the status bit that caused the header log (in other words, until the error pointer is re-armed for logging again).

3.4 SMBus Memory-Mapped Registers

Table 3-127. SMBus Memory Mapped Registers (Sheet 1 of 2)

Address Offset	Register Section, Name, Page
+000H	"General Control Register (GCTRL)"
+004H	Reserved
+008H	"SMT Interrupt Cause Location Register (SMTICL)"
+010H	"Error Interrupt Mask Register (ERRINTMSK)"
+014H	"Error AER Mask Register (ERRAERMSK)"
+018H	"Error Status Register (ERRSTS)"
+01CH	"Error Information Register (ERRINFO)"
+020H +0FCH	Reserved
+100H	"Master Descriptor Base Address Register (MDBA)"
+108H	"Master Control Register (MCTRL)"
+10CH	"Master Status Register (MSTS)"
+110H	"Master Descriptor Size Register (MDS)"
+114H	"Retry Policy Register (RPOLICY)"
+118H +1FCH	Reserved
+200H	"Target Buffer Base Address Register (TBBA)"
+208H	"Target Control Register (TCTRL)"
+20CH	"Target Status Register (TSTS)"
+210H	"Target Buffer Size Register (TBS)"
+214H	Reserved
+218H	"Hardware Target Head Pointer Register (HTHP)"
+21CH	"Firmware Target Tail Pointer Register (FTTP)"
+220H	"Target Receive Control Register (TRxCTRL)"
+224H	"Target Receive Status Register (TRxSTS)"
+228H	"Target Address Control Register (TACTRL)"
+22CH	"Target Policy Register (TPOLICY)"
+230H +23CH	Reserved
+240H	"General Purpose Block Read Control Register (GPBRCTRL)"
+244H	"Generic Programmable Read Data Buffer Register (GPBRDBUF)"
+248H +27CH	Reserved
+280H	"SMBus Controller Address Resolution Protocol Control Register (SMBus Controller ARPCTRL)"
+284H +28CH	Reserved
+290H	"UDID0 Data Register (UDID0)"
+298H	"UDID0 Upper Data Register (UUDID0)"
+2A0H	"UDID1 Data Register (UDID1)"

Table 3-127. SMBus Memory Mapped Registers (Sheet 2 of 2)

Address Offset	Register Section, Name, Page
+2A8H	"UDID1 Upper Data Register (UUDID1)"
+2ACH +2BCH	Reserved
+2C0H +2FCH	Reserved
+300H	"SMBus PHY Global Timing Register (SPGT)"
+304H	"SMBus PHY Master Timing Register (SPMT)"
+308H	"SMBus PHY Slave Timing Register (SPST)"
+30CH	"SMBus Fair Timing Register (SMBFT)"
+310H	"Clock-Low Timeout Control Register (CLTC)"
+314H	"Data-Low Timeout Control Register (DLTC)"
+318H +37CH	Reserved

The above table lists the SMBus Controller memory mapped registers. The following subsections contain the memory mapped register definition.

Table 3-128. General Control Register (GCTRL)

GCTRL
Base: SMBus ControllerBAR **Offset: 000h**

Bit	Attribute	Default	Description
31:7	RV	0	Reserved
6	RWS-V	0	**SRST (Soft Reset):** 0 = The HW resets this bit to 0 when SMBus reset operation is completed. 1 = The SMBus state machine and logic is reset.
5	RV	0	Reserved
4	RV	0	Reserved. FW must not write 1 to this register.
3	RWS-V	0	**KILL (KILL)**: FW sets the bit to cause HW to cause clock-low timeout on the SMBus and generate stop after the timeout. The duration of the clock-low is programmed by FW in CLTC.CNT. KILL applies only to master cycles; and in-progress target cycle is not affected. HW auto-clears this bit once this sequence is complete. 0 = Normal SMBus host controller functionality. 1 = Kills the current host transaction taking place, sets the FAILED status bit, and asserts the interrupt (or SMI#). This bit, once set, must be cleared by software to allow the SMBus host controller to function normally.
2	RWS-V	0	**Target Reset (TRST):** 0 = Normal SMBus Host controller functionality. 1 = In progress target cycle is gracefully terminated at a byte boundary and follows all SMBus protocol and timings. Bit cleared after target reset is complete.
1:0	RV	0	Reserved

Table 3-129. SMT Interrupt Cause Location Register (SMTICL)

SMTICL
Base: SMBus ControllerBAR **Offset: 008h**

Bit	Attr	Default	Description
63:2	RW	0000000h	**Base Address (BA):** Base address of SMT interrupt cause.
1:0	RO	00b	**Memory Size (MS):** Reserved

Table 3-130. Error Interrupt Mask Register (ERRINTMSK)

ERRINTMSK
Base: SMBus ControllerBAR **Offset: 010h**

Bit	Attr	Default	Description
31:26	RV	0	Reserved
25	RWS	0	**SMBus Data-Low Timeout Error Interrupt Mask (DTLTO)**: FW sets this bit to mask HW from generating an interrupt due to ERRSTS.DTLTO being set.
24	RWS	0	**SMBus Clock-Low Timeout Error Interrupt Mask (CKLTO)**: FW sets this bit to mask HW from generating an interrupt due to ERRSTS.CKLTO being set.
23:18	RV	0	Reserved
17	RWS	0	**Target Ring Buffer Full Error Interrupt Mask (TRBF)**: FW sets this bit to mask HW from generating an interrupt due to ERRSTS.TRBF being set.
16	RWS	0	**Target Ring Buffer Almost Full Error Interrupt Mask (TRBAF)**: FW sets this bit to mask HW from generating an interrupt due to ERRSTS.TRBAF being set.
15:11	RV	0	Reserved
10	RWS	0	**IPI Transmit Error Interrupt Mask (ITE):** FW sets this bit to mask HW from generating an interrupt due to ERRSTS.ITE being set.
9	RWS	0	**IPI Receive Data Parity Error Interrupt Mask (IRDPE):** FW sets this bit to mask HW from generating an interrupt due to ERRSTS.IRDPE being set.
8	RWS	0	**IPI Receive Error Interrupt Mask (IRE):** FW sets this bit to mask HW from generating an interrupt due to ERRSTS.IRE being set.
7:1	RV	0	Reserved
0	RWS	0	**CSR Parity Error Interrupt Mask (CPE):** FW sets this bit to mask HW from generating an interrupt due to ERRSTS.CPE being set.

Table 3-131. Error AER Mask Register (ERRAERMSK)

ERRAERMSK
Base: SMBus ControllerBAR **Offset: 014h**

Bit	Attr	Default	Description
31:26	RV	0	Reserved
25	RWS	0	**SMBus Data-Low Timeout Error AER Mask (DTLTO)**: FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.DTLTO being set.
24	RWS	0	**SMBus Clock-Low Timeout Error AER Mask (CKLTO)**: FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.CKLTO being set.
23:18	RV	0	Reserved
17	RWS	0	**Target Ring Buffer Full Error AER Mask (TRBF)**: FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.TRBF being set.
16	RWS	0	**Target Ring Buffer Almost Full Error AER Mask (TRBAF)**: FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.TRBAF being set.
15:11	RV	0	Reserved
10	RWS	0	**IPI Transmit Error AER Mask (ITE):** FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.ITE being set.
9	RWS	0	**IPI Receive Data Parity Error AER Mask (IRDPE):** FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.IRDPE being set.
8	RWS	0	**IPI Receive Error AER Mask (IRE):** FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.IRE being set.
7:1	RV	0	Reserved
0	RWS	0	**CSR Parity Error AER Mask (CPE):** FW sets this bit to mask HW from escalating through AER Uncorrectable Internal Error due to ERRSTS.CPE being set.

Table 3-132. Error Status Register (ERRSTS)

ERRSTS
Base: SMBus ControllerBAR **Offset: 018h**

Bit	Attr	Default	Description
31:26	RV	0	Reserved
25	RW1 CS	0	**SMBus Data-Low Timeout Error Status (DTLTO)**: This bit is set by HW when SMBus data signal is seen low for the time programmed in DLTC.CNT. FW clears this register by writing 1. This status bit is enabled by SUSCHKB.DLTOE.
24	RW1 CS	0	**SMBus Clock-Low Timeout Error Status (CKLTO)**: This bit is set by HW when SMBus clock is seen low for the time programmed in CLTC.CNT. FW clears this register by writing 1.
23:18	RV	0	Reserved
17	RW1 CS	0	**Target Ring Buffer Full Error Status (TRBF)**: HW sets this bit when it needs to write data and/or header to memory and does not have enough free space in the ring buffer in memory. Once the ring buffer full status bit is set, HW does silently NACK all incoming target transactions on the command phase to indicate that it is busy. FW clears this register by writing 1.
16	RW1 CS	0	**Target Ring Buffer Almost Full Error Status (TRBAF)**: HW sets this bit after it has completed writing data and/or header to memory and checks if there is less than 85B of free space in the ring buffer. FW clears this register by writing 1.
15:11	RV	0	Reserved
10	RW1 CS	0	**IPI Transmit Error Status (ITE):** HW sets this bit if an error is detected in any IPI transmit transaction. FW clears this register by writing 1.
9	RW1 CS	0	**IPI Receive Data Parity Error Status (IRDPE):** HW sets this bit if a data parity error is detected in any IPI receive transaction. FW clears this register by writing 1.
8	RW1 CS	0	**IPI Receive Error Status (IRE):** HW sets this bit if an error is detected in any IPI receive transaction. FW clears this register by writing 1.
7:1	RV	0	Reserved
0	RW1 CS	0	**CSR Parity Error Status (CPE):** HW sets this bit if a parity error is detected in any CSR. FW clears this register by writing 1.

Table 3-133. Error Information Register (ERRINFO)

ERRINFO
Base: SMBus ControllerBAR **Offset: 01Ch**

Bit	Attr	Default	Description
31:16	RV	0	Reserved
15:13	ROS-V	0	**Second Error Info (SERRINFO):** Scratchpad
12:8	ROS-V	0	**Second Error Pointer (SERRPTR):** Upon the second occurrence of any error, as included in ERRSTS, HW sets this register to point to the specific bit which was set.
7:5	ROS-V	0	**First Error Info (FERRINFO):** Scratchpad
4:0	ROS-V	0	**First Error Pointer (FERRPTR):** Upon the first occurrence of any error, as included in ERRSTS, HW sets this register to point to the specific bit which was set.

Table 3-134. Master Descriptor Base Address Register (MDBA)

MDBA
Base: SMBus ControllerBAR **Offset: 100h**

Bit	Attr	Default	Description
63:6	RW	0	**Master Descriptor Base Address (MDBA)**: 64-Byte aligned base address of the master descriptor ring buffer in FW memory. HW uses this base to add to MSTS.HMTP to calculate the physical address of the memory location it wants to access. FW must update this register only when MCTRL.SS and MSTS.IP bits are cleared.
5:0	RV	0	Reserved

Table 3-135. Master Control Register (MCTRL)

MCTRL
Base: SMBus ControllerBAR **Offset: 108h**

Bit	Attr	Default	Description
31:24	RV	0	Reserved
23:16	RW	00h	**Firmware Master Head Pointer (FMHP):** Address offset of the number of descriptors available in the descriptor ring. Updated by FW when it has programmed one or more new descriptors in the master descriptor ring buffer. Always points to the descriptor offset that FW writes to next. FW can increment this register at most to be “MSTS.HMTP - 1” thus implying that Master Descriptor Ring Buffer can only hold “MDS – 1” valid descriptors. FW must roll this register to 0 after MDS is reached.
15:5	RV	0	Reserved
4	RW	0	**Master Error Interrupt Enable (MEIE)**: Set by FW to enable HW to generate MSI (if MSICTL.MSIE set) if MSTS.MEIS bit is set.
3:1	RV	0	Reserved
0	RW-V	0	**Start/Stop (SS):** Set by the FW when it has programmed at least one descriptor in the descriptor ring. Cleared by FW when it wants HW to stop processing more descriptors. FW must monitor the MSTS.IP bit which indicates that HW is truly stopped. HW clears this register for the following fatal error scenario, regardless of Stop-on-Error (SOE) bit in the master descriptor: • HW receives unsuccessful completion on internal IOSF. HW clears this register for the following non-fatal scenario: • Master descriptor SOE bit was set and the transaction was unsuccessful for any condition as reported in the Status WB Dword.

Table 3-136. Master Status Register (MSTS)

MSTS
Base: SMBus ControllerBAR **Offset: 10Ch**

Bit	Attr	Default	Description
31:24	RV	0	Reserved
23:16	RW-V	00h	**Hardware Master Tail Pointer (HMTP):** Descriptor offset in the descriptor ring. Incremented by HW and points to the descriptor that HW is currently processing or processes next. Initialized by FW with the descriptor location where it wants the master to start transaction from (typically 0). This register must only be written by FW when the MCTRL.SS bit is 0 and the MSTS.IP bit is 0. HW must not increment this pointer in the case that due to the failure of a descriptor-initiated cycle, HW clears the MCTRL.SS bit. HW uses MSTS.HMTP and MCTRL.FMHP to calculate full and empty conditions. FW must never initialize this buffer to a value greater than MDS.
15:6	RV	0	Reserved
5	RW1C	0	**Master Interrupt Status (MIS)**: Set by HW to indicate that the descriptor that was being processed was successfully done over SMBus. HW proceeds normally to process the next descriptor if the MCTRL.SS bit is set. HW auto-clears this register if INT bit in the descriptor which it finished processing is set and the associated MSI is sent. If INT bit in descriptor is cleared, FW clears this bit by writing 1.
4	RW1C	0	**Master Error Interrupt Status (MEIS)**: Set by HW to indicate that the descriptor that was being processed was not successfully done on SMBus. HW halts the descriptor engine by clearing the MCTRL.SS bit if this bit is set and the SOE bit in the descriptor which was processed was set. HW auto-clears this register if MCTRL.MEIE register is set and the associated Master Error MSI is sent. If MCTRL.MEIE is cleared, FW clears this bit by writing 1.
3:1	RV	0	Reserved
0	RO-V	0	**In Progress (IP):** Set by the HW to indicate that its DMA engine is active meaning that it is processing a descriptor. HW clears this bit **after** it has finished processing the current descriptor (which is the completion of the descriptor status write back into memory **and Interrupt if enabled is sent)**. This is to aid the stopping of HW even if there are multiple descriptors to be processed.

Table 3-137. Master Descriptor Size Register (MDS)

MDS
Base: SMBus ControllerBAR **Offset: 110h**

Bit	Attr	Default	Description
31:8	RV	0	Reserved
7:0	RW	0	**Master Descriptor Size (MDS):** Defines the size of the master descriptor ring buffer that is pointed to by MDBA. 0-based number of 16B descriptors. The top of the ring buffer is MDBA+MDS including the last location. A value of 1 represents a total possible capacity of 2 descriptors in the ring, and a value of 255 represents capacity of 256 descriptors in the ring. Used by HW to calculate if it has reached the top of the buffer and must wrap back to 0. ***Note:*** **SW Programming Guidelines**: Software sets up a minimum of 2 descriptors for SMBUS operation i.e., allowed range is 2-256 descriptors for the SMBUS engine. This means valid encoding range is 1-255 for this field in the MDS register. ***Note:*** A value of 0 in this register is considered invalid and leads to no execution.

Table 3-138. Retry Policy Register (RPOLICY) (Sheet 1 of 2)

RPOLICY
Base: SMBus ControllerBAR **Offset: 114h**

Bit	Attr	Default	Description
31:24	RV	0	Reserved
23:16	RW	06h	**Time Between Retry Clock Count (TBRCLKCNT)**: This register is programmed by the FW to set the retry timer clock count. The reference clock used for this timer count is specified by FW in RPOLICY.TBRBCLK. The combination of the setting in this register and the reference tick used in RPOLICY.TBRBCLK determines how long the HW waits before issuing an automatic retry for master transactions. A value of 0 indicates HW retries the transaction without any additional delay. ***Note:*** • Retry count is not applicable for retries due to collision on SMBus. Those must be retried as soon as SMBus is free. • This timer must be reloaded every time HW attempts a retry or a completely new cycle is initiated by FW. ***FW Note:*** Since the timer ticks in register RPOLICY.TBRBCLK are free running and not independently generated by HW, there is a possibility of inaccuracy in delay time. This inaccuracy is at most 1 complete duration of the timer tick, e.g., if 1 ms tick is chosen the inaccuracy is never greater than 1 ms. Hence, FW uses its judgement in which timer tick is selected. Recommendation would be to use a faster tick so that the inaccuracy is smaller.
15:14	RV	0	Reserved
13:11	RW	010	**Collision Retry (COLRTRY)**: This field allows the FW to set the number of times master transactions are retried before HW gives up. HW decrements this count after it attempts a master transaction and loses arbitration on SMBus. This timer must be reloaded by HW whenever the RPOLICY.RETRY count is changed (i.e., decremented due to retry or reloaded due to new master cycle initiated). “000”: Reserved “001”: Retry once (total attempts = 2) “010”: Retry 2 times (total attempts = 3) “011”: Retry 3 times (total attempts = 4) “100”: Retry 4 times (total attempts =5) “101”: Retry 5 times (total attempts = 6) “110”: Retry 6 times (total attempts = 7) “111”: Retry 7 times (total attempts = 8)

Table 3-138. Retry Policy Register (RPOLICY) (Sheet 2 of 2)

RPOLICY
Base: SMBus ControllerBAR **Offset: 114h**

Bit	Attr	Default	Description
10:8	RW	000b	**Time Between Retry Base Clock (TBRBCLK):** This register allows the FW to choose the granularity of the timer tick. 000: 10 µs 001: 100 µs 010: 1 ms 011: 10 ms 100: 100 ms 101: Reserved 110: Reserved 111: Reserved The combination of this register and the RPOLICY.TBRCLKCNT register allows the FW to set mean time between retries on SMBus.
7:4	RW	0010b	**RETRY (RETRY):** HW decodes this field to determine the number of times to retry before HW gives up. HW must not decrement this count for cycles that are retried because of collision. HW must reload this count every time it starts a new master cycle. HW must not retry cycles if the cycle was unsuccessful due to a clock-low or data-low timeout on the SMBus. “0000”: No retries “0001”: Retry once (total attempts = 2) “0010”: Retry 2 times (total attempts = 3) “0011”: Retry 3 times (Default: total attempts = 4) “0100”: ... . . . “1111”: Retry 15 times (Total attempts = 16)
3:0	RV	0000b	Reserved

Table 3-139. Target Buffer Base Address Register (TBBA)

TBBA
Base: SMBus ControllerBAR **Offset: 200h**

Bit	Attr	Default	Description
63:6	RW	0	**Target Buffer Base Address (TBBA)**: 64B aligned base address of the target ring buffer. HW uses this base to add to the HTHP to calculate the physical address of the memory location it wants to access. FW must update this register only when target is disabled and TSTS.IP bit is cleared.
5:0	RV	0	Reserved

Table 3-140. Target Control Register (TCTRL)

TCTRL
Base: SMBus ControllerBAR **Offset: 208h**

Bit	Attr	Default	Description
31:7	RV	0	Reserved
6	RW	0	**Un-Successful Received Target Writes Policy (URxTWP)**: FW sets this bit to enable the HW to send data and header for **unsuccessful** write cycles received by the HW as a target. Since HW is responsible only for writing the payload to memory and sending a descriptor to FW, it is FW responsibility to inspect the transaction data to determine protocol type, payload, etc. The following cycles fall under this policy umbrella: SMBus Host Notify ARP Notify ARP Master ARP Prepare to ARP ARP Assign Address ARP General Reset Device command ARP Directed Reset Device command to TACTRL.ADDR0 or TACTRL.ADDR1 SMBus Send Byte command to TACTRL.ADDR0 or TACTRL.ADDR1 SMBus Write Byte/Word command to TACTRL.ADDR0 or TACTRL.ADDR1 SMBus Block Write command to TACTRL.ADDR0 or TACTRL.ADDR1 I^{2}C Master-TX writes Slave-RX to TACTRL.ADDR0 or TACTRL.ADDR1 The header bits define the transaction size (PBC and RBC), cycle type (MTYPE and TTYPE), and why the cycle was unsuccessful (TSTS!=0000b). When this bit is cleared, HW only sends data and header to FW of cycles which were successful.
5	RW	0	**Un-Successful Completion Header WB Policy (UCHWBP)**: FW sets this bit to enable the HW to send a header for programmed FW cycles that were **unsuccessfully** completed as a target. The following cycles fall under this policy umbrella: SMBus Block Reads to GPBR Address (GPBRCTRL.GPTRADR) SMBus Quick Command to TACTRL.ADDR0 or TACTRL.ADDR1 ARP Directed Get UDID command to TACTRL.ADDR0 or TACTRL.ADDR1 ARP General Get UDID command The header bits define the transaction size (PBC and RBC), cycle type (MTYPE and TTYPE), and why the cycle was unsuccessful (TSTS!=0000b). When this bit is cleared, no header writeback is done by HW. ***Note:*** If General Get UDID command is received and that UDID Address Resolved (AR) flag is set, HW does NACK the ARP command byte to indicate it has a valid assigned slave address (its ARP is complete), and it does not send any unsuccessful completion header to FW.
4	RW	1	**Successful Completion Header WB Policy (SCHWBP)**: FW sets this bit to enable the HW to send a header for programmed FW cycles that were **successfully** completed as target on SMBus. The following cycles fall under this policy umbrella: SMBus Block Reads to GPBR Address (GPBRCTRL.GPTRADR) Cycles to ADDR0 or ADDR1 (TACTRL.ADDR0 or TACTRL.ADDR1) Cycles to Default Address (C2h) Cycles to SMBus or ARP Host (10h) The header bits define the transaction size (PBC and RBC), cycle type (MTYPE and TTYPE), and successful completion status (TSTS=0000b). When this bit is cleared, no header writeback is done by HW.
3:1	RV	0	Reserved
0	RW	0	**Target Interrupt Enable (TIE)**: FW sets this bit to enable HW to send MSI when it writes header to memory, i.e., when TSTS.TIS is set.

Table 3-141. Target Status Register (TSTS)

TSTS
Base: SMBus ControllerBAR **Offset: 20Ch**

Bit	Attr	Default	Description
31:12	RV	0	Reserved
11:8	RO-V	0	**Target Cycle In Progress (TCIP)**: This field allows FW to check which logical target address HW is currently servicing as a target. This field is set by HW at the same time as TSTS.IP transitions from 0 to 1. 0000: Default SMBus transaction to C2h 0001: Transaction targeting address (TACTRL.ADDR0) of UDID0 0010: Transaction targeting address (TACTRL.ADDR1) of UDID1 0100: Host Notify transaction targeting 10h 0101: Generic Programmable Block Read to programmed address in GPBRCTRL.GPTRADR Others: reserved ***Note:*** This field is valid only when the TSTS.IP bit is set. ***Note:*** This field is consistent with Target Header Descriptor TTYPE field.
7:2	RV	0	Reserved
1	RO-V	0	**In Progress (IP)**: This bit is set by HW when it is processing a target cycle received on SMBus. This is the phase after the HW has ACK'ed a matching address until Stop is asserted by the external initiator, target buffer is emptied, and interrupt if enabled is sent to FW. This bit is cleared otherwise.
0	RW1C	0	**Target Interrupt Status (TIS)**: This bit is set by HW after it has written status header in target ring buffer as an indication of interrupt generation. The conditions which result in a status header being written are governed by these policies: • TCTRL.SCHWBP: upon successful completion • TCTRL.UCHWBP: upon unsuccessful completion • TCTRL.URxTWP: upon unsuccessful completion of writes to target If TCTRL.TIE is cleared, FW must write 1 to clear this bit. It TCTRL.TIE register is set and global MSICTL.MSIE is set, HW sends the MSI and auto-clears this bit.

Table 3-142. Target Buffer Size Register (TBS)

TBS
Base: SMBus ControllerBAR **Offset: 210h;**

Bit	Attr	Default	Description
31:16	RV	0	Reserved
15:2	RW	0	**Target Buffer Size (TBS)**: Defines the size in bytes of the target ring buffer in memory which must be Dword aligned. Bits[1:0] are reserved such that FW always provides HW a buffer in granularity of 4 Bytes. 0x0000: 4B 0x0004: 8B ... 0xFFFC: 65536B (~64KB)
1:0	RV	0	Reserved

Table 3-143. Hardware Target Head Pointer Register (HTHP)

HTHP
Base: SMBus ControllerBAR **Offset: 218h**

Bit	Attr	Default	Description
31:16	RV	0	Reserved
15:2	RW-V	0	**Hardware Target Buffer Head Pointer (HTBHP):** Dword offset from the base address within the target ring buffer. Updated by HW to indicate the offset within the ring buffer where the HW is writing payload data/header or is writing to next. HW uses HTHP and FTTP and TBS to calculate buffer full, empty, and wrap conditions. FW must never initialize this to a value greater than TBS.TBS or undefined HW behavior may occur.
1:0	RV	0	Reserved

Table 3-144. Firmware Target Tail Pointer Register (FTTP)

FTTP
Base: SMBus ControllerBAR **Offset: 21Ch**

Bit	Attr	Default	Description
31:16	RV	0	Reserved
15:2	RW	0	**Firmware Target Buffer Tail Pointer (FTBTP):** Dword offset from the base address within the target ring buffer. Updated by FW and points to the offset FW is reading from or is reading from next. FW must never increment this register beyond the value of the HTHP.HTBHP register.
1:0	RV	0	Reserved

Table 3-145. Target Receive Control Register (TRxCTRL)

TRxCTRL
Base: SMBus ControllerBAR **Offset: 220h**

Bit	Attr	Default	Description
31:8	RV	0	Reserved
7:0	RW	88d	**Max Receive Bytes (MRxB):** This register sets the limit for the maximum number of bytes (**address included**) that SMT can receive as a target of write transactions. Once this limit is reached, HW must NACK the following received bytes. The encoding is 0s based, i.e., 0 means 1 byte (address only) and 255 means 256 bytes. 00h:Reserved 01h: 2 bytes (address + 1 additional byte) ... EFh: 240 bytes (address + 239 additional bytes) F0h: Reserved ... FFh: Reserved ***Note:*** HW must always track the received number of bytes for I^2C transactions to ensure that it never overflows the count programmed in this register. When this count is met, HW must NACK any following received bytes. (It is expected that bounded protocols, like SMBus which announces a byte count, provide protocol-level control to ensure write count is not exceeded. The responsibility of the bus master is to recover and retry if HW does NACK such an overflowing transaction.) ***Note:*** Default is defined for MCTP with 80B MCTP packet payload: (8B) MCTP SMBus Packet Header (includes 4B SMBus medium-specific header and 4B MCTP transport header) (80B) MCTP Packet Payload (1B) SMBus PEC = 89B --> 88d (0s-based encoding)

Table 3-146. Target Receive Status Register (TRxSTS)

TRxSTS
Base: SMBus ControllerBAR **Offset: 224h**

Bit	Attr	Default	Description
31:24	RO-V	0	**Payload Byte Count (PBC)**: HW updates this field to indicate how many bytes were ACK'ed on SMBus sent by the external master and stored within the target buffer locally. For writes coming in, this data includes the sum total of all bytes ACK'ed from start to stop. For error scenarios where the master drives more data than expected or command code does not match, HW updates the count with all bytes ACK'ed on SMBus from start until the first byte NACK'ed by HW (this byte is not added to the count).
23:22	RV	0	Reserved
21:16	RO-V	0	**Read Byte Count (RBC)**: This byte count is for externally generated read transactions only. HW updates this field to indicate the sum total of data bytes it successfully provided over SMBus to the external master.
15:12	RV	0	Reserved
11:8	RO-V	0	**MTYPE (MTYPE)**: Check the Target header description.
7:4	RO-V	0	**TSTS (TSTS)**: Check the Target header description.
3:0	RO-V	0	**TTYPE (TTYPE)**: Check the Target header description.

Table 3-147. Target Address Control Register (TACTRL)

TACTRL
Base: SMBus ControllerBAR **Offset: 228h**

Bit	Attr	Default	Description
31:16	RV	0	Reserved
15:9	RW	0	**Address1 (ADDR1)**: FW programs this field with an address of the SMT logic. If FW needs to override the default value, then FW must program this before enabling the target interface. All transactions targeting this address is ACK'ed by the HW if the TPOLICY.ADDR1_EN register is set.
8	RV	0	Reserved
7:1	RW	0	**Address0 (ADDR0)**: FW programs this field with an address of the SMT logic. If FW needs to override the default value, then FW must program this before enabling the target interface. All transactions targeting this address is ACK'ed by the HW if the TPOLICY.ADDR0_EN register is set.
0	RV	0	Reserved

Note: Addresses TACTRL.ADDR0, TACTRL.ADDR1, and GPBRCTRL.GPTRADR must not be programmed to an SMBus reserved address (e.g., 10h or C2h). Also each address must be unique and not the same as any other enabled address on the same segment.

Table 3-148. Target Policy Register (TPOLICY)

TPOLICY
Base: SMBus ControllerBAR **Offset: 22Ch**

Bit	Attr	Default	Description
31	RWS-V	0	**Target Policy Update Request (PTUREQ)**: FW sets this bit to indicate to the HW that it wants to update registers/policies in the target interface. The new policy that the FW needs is programmed in the lower word of this register. HW clears this bit when it has updated the new policy. When this bit is cleared the other registers indicate the current policy in effect in HW.
30:11	RV	0	Reserved
10	RW	0	**C2_BSY (C2_BSY)**: When set forces HW to ACK only matching C2h address byte and NACK in any subsequent bytes to indicate device is busy.
9	RW	0	**Host Busy (HOSTBSY)**: When set forces HW to ACK only matching 10h address byte and NACK in any subsequent bytes to indicate device is busy.
8	RW	0	**ADDR1 Busy (ADDR1BSY)**: When set forces HW to ACK only matching ADDR1 address byte and NACK in any subsequent bytes to indicate device is busy.
7	RV	0	Reserved
6	RW	0	**ADDR0 Busy (ADDR0BSY)**: When set forces HW to ACK only matching ADDR0 address byte and NACK in any subsequent bytes to indicate device is busy.
5	RV	0	Reserved
4	RWS-V	0	**Device Address0 Enable (ADDR0_EN):** When set, enables target logic to ACK ADDR0 address on the SMBus.
3	RWS-V	0	**Host SMBus Address Enable (Host_SMBADDR_EN)**: When set, enables HW to accept write cycles targeting address 10h. This bit must be set to 1 when Intel® Atom™ Processor S1200 Product Family is the SMBus Segment Owner.
2	RW	0	**Default SMBus Address Enable (DEF_SMBADDR_EN):** When set, enables HW to ACK cycles targeting address C2h, which is the SMBus default address.
1	RWS-V	0	**Device Address1 Enable (ADDR1_EN):** When set, enables target logic to ACK ADDR1 address on the SMBus.
0	RW	0	**Target Enable (TGTEN)**: Set to 1 by the FW after it has programmed the base address in the Target Data Ring Buffer and updated target policies. While in default state 0 all bytes is NACK'ed on SMBus **including** the address byte of the enabled addresses. ***Note:*** TGTEN applies to all target addresses: ADDR0_EN, ADDR1_EN, Host_SMBADDR_EN, DEF_SMBADDR_EN, and GPBRCTRL.EN.

Table 3-149. General Purpose Block Read Control Register (GPBRCTRL)

GPBRCTRL
Base: SMBus ControllerBAR **Offset: 240h**

Bit	Attribute	Default	Description
31	RWS-V	0	**Enable (EN):** This bit is set by FW to enable HW to respond to a block read command to address GPBRCTRL.GPTRADR and command GPBRCTRL.CMD. HW clears this bit after HW ACKs the command code (CMD) on the Block Read command if GPBRCTRL.HWCLRDIS is cleared.
30	RW	0	**PEC Enable (PECEN)**: This bit is set by FW to indicate that HW must provide PEC at the end of the transaction to the external master.
29	RW	0	**HW Clear Disable (HWCLRDIS)**: This bit is set by FW to disable the HW from clearing of the GPBRCTRL.EN bit. This functionality allows HW to continuously provide current data in the GPRDx registers to the external master without FW involvement. ***Note:*** When this bit is set, HW must start sending data from byte 0 (of the buffer behind GPBRDBUF) when responding to a new Block Read cycle.
28	RW-V	0	**GPBR Buffer Contents Reset (BUFRST):** This bit is set by FW to reset (zero) the contents of the GPBR buffer. (See also GPBRDBUF.) HW clears this bit after it has reset the GPBR buffer contents.
27	RW-V	0	**GPBR Buffer Pointer Reset (PTRRST):** This bit is set by FW to reset the pointer into the GPBR buffer. (See also GPBRDBUF.) HW clears this bit after it has reset the GPBR buffer pointer.
26:24	RV	00h	Reserved
23:16	RW	00h	**Byte Count (BC):** Byte count indicating how many bytes are programmed in the Generic Read Data buffer (GPBRDBUF) by FW. The maximum count is 32B, which is the maximum number of bytes that the buffer can hold. On the block read, after HW matches the address and command, HW sends the contents of this byte on the SMBus and then sends out those many bytes from the Generic Read Data Buffer starting from the LSB of GPBRDBUF0 register, i.e., the byte 0 of GPBRDBUF0.
15:8	RW	00h	**Command (CMD):** Command byte of the block read command.
7:0	RWS-V	00h	**General Purpose Target Read Address (GPTRADR):** Target address of the externally initiated Block Read command cycle. ***Note:*** Bit[0] of this register is the "Enable" for this address. HW does not take any action based on the value of bit[0]. It is simply provided to FW for reading.

Note: Addresses TACTRL.ADDR0, TACTRL.ADDR1, and GPBRCTRL.GPTRADR must not be programmed to an SMBus reserved address (e.g., 10h or C2h). Also each address must be unique and not the same as any other enabled address on the same segment.

Table 3-150. Generic Programmable Read Data Buffer Register (GPBRDBUF)

GPBRDBUF
Base: SMBus ControllerBAR **Offset: 244h**

Bit	Attribute	Default	Description
31:0	RW-V	0	**Data DWORD (GPBRD)**

Table 3-151. SMBus Controller Address Resolution Protocol Control Register (SMBus Controller ARPCTRL)

SMBus Controller ARPCTRL
Base: SMBus ControllerBAR **Offset: 280h**

Bit	Attribute	Default	Description
31	RW	0b	**Disable "Notify ARP Master" (NOTIFYD):** If asserted, the SMBus Controller issues a "Notify ARP Master" command. Otherwise, if SMBus Controller is not the ARP Host, it is permitted to issue a Notify ARP Master command.
30:8	RV	0000000h	Reserved
7	RV	0	Reserved
6	RW	0b	**Address Resolved (AR1):** If asserted, the device slave address has been resolved by the ARP Master.
5	RW	0b	**Address Valid (AV1):** If asserted, the device slave address is valid.
4	RW	0b	**UDID1 Enable (UDID1E):** If cleared, the SMBus Controller does not ACK or respond to ARP transactions directed to UDID1.
3	RV	0	Reserved
2	RW	0b	**Address Resolved (AR0):** If asserted, the device slave address has been resolved by the ARP Master.
1	RW	0b	**Address Valid (AV0):** If asserted, the device slave address is valid.
0	RW	0b	**UDID0 Enable (UDID0E):** If cleared, the SMBus Controller does not ACK or respond to ARP transactions directed to UDID0.

Table 3-152. UDID0 Data Register (UDID0)

UDID0
Base: SMBus ControllerBAR **Offset: 290h**

Bit	Attribute	Default	Description
63:48	RO	8086h	**Subsystem Vendor ID (SVID):** Subsystem Vendor ID indicates that the device subsystem vendor is Intel.
47:32	RO	0	**Subsystem Device ID (SDID):** Subsystem Device ID.
31:0	RWS-V	0000_0000h	**Vendor Specific ID (VSID):** Vendor Specific ID must uniquely identify this device when dynamic, volatile addressing is enabled.

Table 3-153. UDID0 Upper Data Register (UUDID0)

UUDID0
Base: SMBus ControllerBAR **Offset: 298h**

Bit	Attribute	Default	Description
63:56	RW	81h	**Device Capabilities (DEVCAP):** Device Capabilities by default indicate that the device is a dynamic and volatile address device which supports PEC. FW may modify the capability, for instance to behave as a fixed-address device.
55:48	RO	08h	**Version/Revision (RID):** Version/Revision indicating UDID version 1 and Revision 0 of the silicon.
47:32	RO	8086h	**Vendor ID (VID):** Vendor ID indicates that the device vendor is Intel.
31:16	RO	0000h	**Device ID (DID):** Device ID
15:0	RW	0024h	**Interface (INTF):** Interface field indicates that the device supports SMBus 2.0 and its ASF capabilities bit set.

Table 3-154. UDID1 Data Register (UDID1)

UDID1
Base: SMBus ControllerBAR **Offset: 2A0h**

Bit	Attribute	Default	Description
63:48	RO	8086h	**Subsystem Vendor ID (SVID):** Subsystem Vendor ID indicates that the device subsystem vendor is Intel.
47:32	RO	0	**Subsystem Device ID (SDID):** Subsystem Device ID.
31:0	RWS-V	0000_0000h	**Vendor Specific ID (VSID):** Vendor Specific ID must uniquely identify this device when dynamic, volatile addressing is enabled.

Table 3-155. UDID1 Upper Data Register (UUDID1)

UUDID1
Base: SMBus ControllerBAR **Offset: 2A8h**

Bit	Attribute	Default	Description
63:56	RW	81h	**Device Capabilities (DEVCAP):** Device Capabilities by default indicate that the device is a dynamic and volatile address device which supports PEC. FW may modify the capability, for instance to behave as a fixed-address device.
55:48	RO	08h	**Version/Revision (RID):** Version/ Revision indicating UDID version 1 and Revision 0 of the silicon.
47:32	RO	8086h	**Vendor ID (VID):** Vendor ID indicates that the device vendor is Intel.
31:16	RO	0000h	**Device ID (DID):** Device ID
15:0	RW	0024h	**Interface (INTF):** Interface field indicates that the device supports SMBus 2.0 and its ASF capabilities bit set.

Table 3-156. SMBus PHY Global Timing Register (SPGT)

SPGT
Base: SMBus ControllerBAR **Offset: 300h**

Bit	Attr	Default	Description
31:30	RWS-V	0	**SMBus Speed (SPD):** Value to indicate what speed physical bus must operate. It is up to the system designer to ensure that all devices on the same SMBus segment are capable of operating at the programmed speed. 00: Standard (80 kHz) 01: Standard (100 kHz) 10: Fast Mode (400 kHz) 11: Fast Mode Plus (1 MHz)
29	RW	0	**Speed Lock (SPDLK)**: FW sets this register if it overrides the settings of SPGT.SPD register. If this bit is set, HW must not load the SPGT.SPD from the soft strap.
28:20	RV	0	Reserved
19:16	RW	0h	**T-Hold Data (THDDAT)**: The value in this field is added to the Thddat timing parameter as defined in the SMBus 2.0 Specification. 0000: 0 Clocks (0 ns) 0001: 1 Clocks (10 ns) 0010: 2 Clocks (20 ns) ... 1111: 15 Clocks (150 ns)
15:12	RV	0	Reserved
11:8	RW	0h	**T-Setup Data (TSUDAT)**: The value in this field is added to the Tsudat timing parameter as defined in the SMBus 2.0 Specification. 0000: 0 Clocks (0 ns) 0001: 1 Clocks (10 ns) 0010: 2 Clocks (20 ns) ... 1111: 15 Clocks (150 ns)
7:0	RW	5h	**De-Glitch (DG)**: The value in this field defines the minimum de-glitch pulse that the de-glitch logic rejects from the SMBus clock and data lines. 000000xx: No de-glitch 00000100: 4 Clocks (40 ns glitch pulse) 00000101: 5 Clocks (50 ns glitch pulse) . . 11111111: 255 Clocks (2550 ns glitch pulse)

Table 3-157. SMBus PHY Master Timing Register (SPMT)

SPMT
Base: SMBus ControllerBAR **Offset: 304h**

Bit	Attr	Default	Description
31:24	RW	08h	**Time High (Thigh)**: The value in this field is added/subtracted to the Thigh timing parameter as defined in the SMBus 2.0 Specification. 00000000: 0 Clock (0 ns) 00000001: -1 Clock (-10 ns) ... 00000111: -7 Clocks (-70 ns) 00001000: 0 Clock (0 ns) 00001001: +1 Clock (+10 ns) ... 11111111: +247 Clocks (+2,470 ns) ***Note:*** These are offsets that control the range of the nominal Thigh value in the PHY layers.
23:16	RW	08h	**Time Low (Tlow)**: The value in this field is added/subtracted to the Tlow timing parameter as defined in SMBus 2.0 Specification. See Thigh field above for encoding.
15:12	RW	0h	**Thdsta (Thdsta)**: The time value in this field is added/subtracted to the Thdsta timing parameter as defined in SMBus 2.0 Specification. 1111: -7 Clocks (-70 ns) 1110: -6 Clocks (-60 ns) ... x000: 0 Clock (0 ns) 0001: +1 Clock (+10 ns) ... 0111: +7 Clocks (+70 ns)
11:8	RW	0h	**Tsusta (Tsusta)**: The time value in this field is added/subtracted to the Tsusta timing parameter as defined in SMBus 2.0 Specification. See Thdsta field above.
7:4	RW	0h	**Tbuf (Tbuf)**: The time value in this field is added/subtracted to the Tbuf timing parameter as defined in SMBus 2.0 Specification. See Thdsta field above.
3:0	RW	0h	**Tsusto (Tsusto)**: The time value in this field is added/subtracted to the Tsusto timing parameter as defined in SMBus 2.0 Specification. See Thdsta field above.

Table 3-158. SMBus PHY Slave Timing Register (SPST)

SPST
Base: SMBus ControllerBAR **Offset: 308h**

Bit	Attr	Default	Description
31:24	RW	00h	**Slave Tlow Extension (Slave_Tlow_Ext)**: The time value in this field is added to the SMBCLK Tlow extension timing parameter on a per bit basis. 00000000: 0 Clock (0 ns) 00000001: 1 Clock (10 ns) ---- 11111111: 255 Clocks (2,550 ns)
23:12	RV	0	Reserved
11:8	RW	0h	**Slave Tsusta (Slave_Tsusta)**: The time value in this field is added/subtracted to the detection of Tsusta timing parameter as defined in SMBus 2.0 Specification. 1111: -7 Clocks (-70 ns) 1110: -6 Clocks (-60 ns) ---- x000: 0 Clock (0 ns) 0001: +1 Clock (+10 ns) ---- 0111: +7 Clocks (+70 ns)
7:4	RW	0h	**Slave Tthdsta (Slave_Tthdsta)**: The time value in this field is added/subtracted to the detection of Thdsta timing parameter as defined in SMBus 2.0 Specification. See Slave_Tsusta field above.
3:0	RW	0h	**Slave Ttsusto (Slave_Ttsusto)**: The time value in this field is added/subtracted to the detection of Tsusto timing parameter as defined in SMBus 2.0 Specification. See Slave_Tsusta field above.

Table 3-159. SMBus Fair Timing Register (SMBFT)

SMBFT **Base: SMBus ControllerBAR**			**Offset: 30Ch**
Bit	**Attr**	**Default**	**Description**
31	RO-V	0	**Fair Flag (FF)**: HW sets this bit when it has mastered a cycle by processing a descriptor in which "FAIR" control bit was set. This flag when set is an internal state for the HW to wait longer before it attempts to master the next cycle on SMBus. The next cycle does not necessarily have to be descriptor-based or have the "FAIR" bit set in the descriptor if it is descriptor-based. Mastering a cycle is defined as when HW attempts to do a SMBus block write and in the data phase following byte count it sees its own SMBus address (with RW bit = 1) on the SMBus. This is per MCTP HW clears this flag after the expiry of SMBFT.SFIC.
30:16	RV	0	Reserved
15:8	RW	20h	**SMBus Start Delay (SSD):** This count is the number of ticks (in increments of 1 µs) that HW must count after SMBFT.FF is cleared before it can attempt to master another SMBus cycle. HW must look for transition of SMBFT.FF bit to transition from 1->0 before it starts counting off this delay time. 0h: reserved (see note) 1h: reserved (see note) 2h: 2 µs ... FFh: 255 µs
7:0	RW	24h	**SMBus Fair Idle Count (SFIC)**: This count represents the minimum SMBus Idle Time (in increments of 1us) that the HW must detect after SMBus Stop is seen before clearing the SMBFT.FF register. 0h: reserved (see note) 1h: reserved (see note) 2h: 2 µs ... FFh: 255 µs

Table 3-160. Clock-Low Timeout Control Register (CLTC)

CLTC
Base: SMBus ControllerBAR **Offset: 310h**

Bit	Attr	Default	Description
31:16	RV	0000h	Reserved
15:4	RW	15Eh	**Count (CNT)**: FW sets this to the desired count that the HW must count while SMBus clock is low before flagging SMBus Clock-Low Timeout. 0h: Reserved (see note for BCLK) 1h: Reserved (see note for BCLK) Others: count per BCLK Default value is set to provide 35ms clock-low timeout detection (for default 100 µs BCLK).
3	RV	0	Reserved
2:0	RW	001b	**Base Clock (BCLK)**: FW programs this register to set the granularity of the count. The value in this register selects which timer ticks are used to count off the value programmed in CLTC.CNT register. 000: 10 µs 001: 100 µs (default) 010: 1 ms 011: 10 ms 100: 100 ms Others: Reserved ***Note:*** The timer ticks are not internally generated by HW hence the count could be off by 1 timer tick.

Table 3-161. Data-Low Timeout Control Register (DLTC)

DLTC
Base: SMBus ControllerBAR **Offset: 314h**

Bit	Attr	Default	Description
31:16	RV	0000h	Reserved
15:4	RW	0C8h	**Count (CNT)**: FW sets this to the desired count that the HW must count while SMBus data is low before flagging SMBus Data-Low Timeout. 0h: reserved (see note for BCLK) 1h: reserved (see note for BCLK) Others: count per BCLK Default value is set to provide 2sec data-low timeout detection (for default 10 ms BCLK).
3	RV	0	Reserved
2:0	RW	011b	**Base Clock (BCLK)**:FW programs this register to set the granularity of the count. The value in this register selects which timer ticks are used to count off the value programmed in DLTC.CNT register. 000: 10 µs 001: 100 µs 010: 1 ms 011: 10 ms (default) 100: 100 ms Others: Reserved

3.5 Intel Legacy Block

Table 3-162. Register Summary (Sheet 1 of 4)

Offset (h)	Size (bits)	Name
0	32	“Root Complex Topology Capabilities List (RCTCL)” on page 126
04	32	“Element Self Description (ESD)” on page 126
00	16	“Power Management 1 Status (PM1S)” on page 127
02	16	“Power Management 1 Enables (PM1E)” on page 128
04	32	“Power Management 1 Controls (PM1C)” on page 129
08	32	“Power Management 1 Timer (PM1T)” on page 129
00	32	“General Purpose Event 0 Status (GPE0S)” on page 131
04	32	“General Purpose Event 0 Enable (GPE0E)” on page 132
10	32	“SMI Enable (SMIE)” on page 133
14	32	“SMI Status Register (SMIS)” on page 134
18	32	“General Purpose Event Control (GPEC)” on page 134
20	32	“C3/C4 Residency Register (C34R)” on page 135
24	32	“C5/C6 Residency Register (C56R)” on page 135
28	32	“Power Management Configuration Core Well (PMCW)” on page 135
2C	32	“Power Management Configuration Suspend/Resume Well (PMSW)” on page 136
30	32	“Power Management Configuration RTC Well (PMRW)” on page 137
34	32	“High Precision Event Timer Registers” on page 138
FED0_0000	64	“General Capabilities and ID (GCID)” on page 138
FED0_0010	64	“General Configuration (GC)” on page 139
FED0_0020	64	“General Interrupt Status (GIS)” on page 139
FED0_00F0	64	“Main Counter Value (MCV)” on page 139
FED0_0100	64	“Timer 0 Config and Capabilities (T0C)” on page 140
FED0_0120	64	“Timer 1 Config and Capabilities (T1C)” on page 141
FED0_0140	64	“Timer 2 Config and Capabilities (T2C)” on page 142
FED0_0108	64	“Timer 0 Comparator Value(T0CV)” on page 143
FED0_0128	64	“Timer 1 Comparator Value(T1CV)” on page 143
FED0_0148	64	“Timer 2 Comparator Value(T2CV)” on page 143
43	8	“Timer I/O Registers” on page 145
No Offset	8	“Timer Control Word Register (TCW)” on page 145
No Offset	8	“Read Back Command (RBC)” on page 146
No Offset	8	“Counter Latch Command (CLC)” on page 146
40	8	“Interval Timer Status Byte Format Register (ITSTS[0-2])” on page 147
40	8	“Counter Access Ports Register (CAP[0-2])” on page 147
70	8	“RTC Index Register (RTCIDX)” on page 149
71	8	“RTC Window Register (RTCWDW)” on page 149
0A	8	“General Configuration Register A (RTCA)” on page 150
0B	8	“General Configuration Register B (RTCB)” on page 151
0C	8	“Flag Register C (RTCC)” on page 151
0D	8	“Flag Register D (RTCD)” on page 152

Table 3-162. Register Summary (Sheet 2 of 4)

Offset (h)	Size (bits)	Name
20	8	“Master/Slave Initialization Command Word 1 ([M,S]ICW1)” on page 154
21	8	“Master/Slave Initialization Command Word 2 ([M,S]ICW2)” on page 155
21	8	“Master Initialization Command Word 3 (MICW3)” on page 155
A1	8	“Slave Initialization Command Word 3 (SICW3)” on page 156
21	8	“Master/Slave Initialization Command Word 4 Register ([M,S]ICW4)” on page 156
21	8	“Master/Slave Operational Control Word 1 ([M,S]OCW1)” on page 156
20	8	“Master/Slave Operational Control Word 2 ([M,S]OCW2)” on page 157
20	8	“Master/Slave Operational Control Word 3 ([M,S]OCW3)” on page 157
20	8	“Master Edge/Level Control (ECLR1)” on page 158
20	8	“Slave Edge/Level Control (ECLR2)” on page 158
FEC0_0000	8	“Index Register (IDX)” on page 159
FEC0_0010	32	“Window Register (WDW)” on page 159
FEC0_0040	32	“EOI Register (EOI)” on page 159
00	32	“Identification Register (ID)” on page 160
01	32	“Version Register (VS)” on page 160
10	32	“Redirection Table Entry Low DWord(RTEL[0-23])” on page 161
11	32	“Redirection Table Entry High DWord (RTEH[0-23])” on page 161
00	32	“Identifiers (ID)” on page 163
04	16	“Device Command (CMD)” on page 163
06	16	“Status (STS)” on page 164
08	8	“Revision ID (RID)” on page 164
09	24	“Class Code (CC)” on page 164
0E	8	“Header Type (HTYPE)” on page 164
2C	32	“Sub System Identifiers (SS)” on page 164
40	32	“SMBus Base Address (SMBA)” on page 165
44	32	“GPIO Base Address (GBA)” on page 165
48	32	“Base Address (PM1BLK)” on page 165
4C	32	“Base Address (GPE0BLK)” on page 165
58	32	“ACPI Control (ACTL)” on page 166
60	8	“PIRQx Routing Control (P[A,B,C,D,E,F,G,H]RC)” on page 166
68	8	“Serial IRQ Control (SCNT)” on page 167
84	32	“WDT Base Address (WDTBA)” on page 167
D0	32	“FWH ID Select (FS)” on page 167
D4	32	“BIOS Decode Enable (BDE)” on page 168
D8	32	“BIOS Control (BC)” on page 168
F0	32	“Root Complex Base Address (RCBA)” on page 169
3020	16	“SPI Status (SPISTS)” on page 171
3022	16	“SPI Control (SPICTL)” on page 172
3024	32	“SPI Address (SPIADDR)” on page 173
3028	64	“SPI Data 0 (SPID0)” on page 173

Table 3-162. Register Summary (Sheet 3 of 4)

Offset (h)	Size (bits)	Name
3030	64	“SPI Data N (SPID[1-7])” on page 173
3070	32	“BIOS Base Address (BBAR)” on page 174
3074	16	“Prefix Opcode Configuration (PREOP)” on page 174
3076	16	“Opcode Type Configuration (OPTYPE)” on page 175
3078	64	“Opcode Menu Configuration (OPMENU)” on page 175
3080	32	“Protected BIOS Range N (PBR[0-2])” on page 176
00	8	“Host Control Register (HCTL)” on page 177
01	8	“Host Status Register (HSTS)” on page 179
02	16	“Host Clock Divider (HCLK)” on page 179
04	8	“Transmit Slave Address (TSA)” on page 179
20	64	“Host Data Block (HBD[0-3])” on page 180
00	32	“Core Well GPIO Enable (CGEN)” on page 181
04	32	“Core Well GPIO Input/Output Select (CGIO)” on page 181
08	32	“Core Well GPIO Level for Input or Output (CGLVL)” on page 182
0C	32	“Core Well GPIO Trigger Positive Edge Enable (CGTPE)” on page 182
10	32	“Core Well GPIO Trigger Negative Edge Enable (CGTNE)” on page 182
14	32	“Core Well GPIO GPE Enable (CGGPE)” on page 182
18	32	“Core Well GPIO SMI Enable (CGSMI)” on page 183
1C	32	“Core Well GPIO Trigger Status (CGTS)” on page 183
40	32	“Core Well NMI Enable (CNMIEN)” on page 183
20	32	“Resume Well GPIO Enable (RGEN)” on page 184
24	32	“Resume Well GPIO Input/Output Select (RGIO)” on page 184
28	32	“Resume Well GPIO Level for Input or Output (RGLVL)” on page 185
2C	32	“Resume Well GPIO Trigger Positive Edge Enable (RGTPE)” on page 185
30	32	“Resume Well GPIO Trigger Negative Edge Enable (RGTNE)” on page 185
34	32	“Resume Well GPIO GPE Enable (RGGPE)” on page 185
38	32	“Resume Well GPIO SMI Enable (RGSMI)” on page 186
3C	32	“Resume Well GPIO Trigger Status (RGTS)” on page 186
44	32	“Resume Well NMI Enable (RNMIEN)” on page 186
00	8	“Preload Value 1 Register 0 (PV1R0)” on page 188
01	8	“Preload Value 1 Register 1 (PV1R1)” on page 188
02	8	“Preload Value 1 Register 2 (PV1R2)” on page 188
04	8	“Preload Value 2 Register 0 (PV2R0)” on page 188
05	8	“Preload Value 2 Register 1 (PV2R1)” on page 189
06	8	“Preload Value 2 Register 2 (PV2R2)” on page 189
0C	8	“Reload Register 0 (RR0)” on page 189
0D	8	“Reload Register 1 (RR1)” on page 189
10	8	“WDT Configuration Register (WDTCR)” on page 190
14	8	“Down Counter Register 0 (DCR0)” on page 190
15	8	“Down Counter Register 1 (DCR1)” on page 190

Table 3-162. Register Summary (Sheet 4 of 4)

Offset (h)	Size (bits)	Name
16	8	"Down Counter Register 2 (DCR2)" on page 190
18	8	"WDT Lock Register (WDTLR)" on page 191
61	8	"NMI Status and Control Register (NSC)" on page 192
70	8	"NMIE – NMI Enable (NMIE)" on page 192
CF9	8	"Reset Control Register (RSTC)" on page 193

3.5.1 Introduction

The Intel Legacy Block consists of legacy modules some of which are required for Windows and other PC OS hardware compatibility.

The Intel Legacy Block consists of modules like Real Time Clock, Timers, Interrupt controllers, General purpose I/O, LPC interface, etc.

- Timers
  - 8254 Timer
  - RTC
  - HPET
- Interrupt Controller
  - 8259 PIC
  - IOxAPIC 1.1
- Interfaces
  - LPC 1.1
  - SPI
  - SMBus 1.0
  - GPIO
- Miscellaneous
  - Interrupt Routing
  - GPIO Functional Muxing
  - SOCF Sideband Message mapping

The Intel Legacy Block has an SoC fabric (SOCF) primary and an SOCF sideband interface.

3.5.1.1 ILB Modules

3.5.1.1.1 Root Complex Register Block

This describes all registers and base functionality that are related to processor configuration, but not a specific interface. It contains the root complex register block. This block is mapped into memory space using RCBA. Accesses in this space are limited to 32-bit quantities. Burst accesses are not allowed.

Table 3-163. Root Complex Topology Capabilities List (RCTCL)

RCTCL
Base: RCBA **Offset: 0h**

Bit	Attribute	Default	Definition
31:20	RO	0	**Next Capability:** Indicates next item in the list.
19:16	RO	1h	**Capability Version:** Indicates the version of the capability structure.
15:00	RO	5h	**Capability ID:** Indicates this is a PCI Express* link capability section of an RCRB

Table 3-164. Element Self Description (ESD)

ESD
Base: RCBA **Offset: 04h**

Bit	Attribute	Default	Definition
31:24	RO	0h	**Port Number:** A value of 0 to indicate the egress port.
23:16	RW-O	0h	**Component ID:** Indicates the component ID assigned to this element by software. This is written once by platform BIOS and is locked until a platform reset.
15:8	RO	1h	**Number of Link Entries:** Indicates that one link entry is described by this RCRB.
7:4	RV	0h	Reserved
3:0	RO	2h	**Element Type:** Indicates that the element type is a root complex internal link.

3.5.1.2 Legacy ACPI

There are five independent regions related to power management. Each has its own I/O space and base address register.

Table 3-165. Register Region Table

Location PCI Dev/Fn	Register Address	Register Name	Register Block
D31:F0	48h	PM1BLK	PM1 Block
D31:F0	4Ch	GPE0BLK	ACPI General Purpose Event 0 Block, and non-ACPI block

Table 3-166. ACPI PM1 Block (PM1BLK)

Address	ByteLength	Symbol	Register Name
Base + 00h	2	PM1S	PM1 Status
Base + 02h	2	PM1E	PM1 Enable
Base + 04h	4	PM1C	PM1 Control
Base + 08h	4	PM1T	PM1 Timer

Table 3-167. Power Management 1 Status (PM1S)

PM1S
I/O Base: PM1BLK Offset: 00h

Bit	Attribute	Default	Definition
15	RW1C	0	**Wake Status (WAKE):** Resume Well. This bit is set when the system is in an Sx state and an enable wake event occurs. Upon setting this bit, the overlay transitions the system to the S0 state. This bit is not affected by warm resets.
14:12	RV	0	Reserved
11	RO	0	**Power Button Override Status (PBOR):** Not reported by the Overlay. Handled by external EC.
10	RW1C	0	**RTC Status (RTC):** Resume Well. This bit is set when the RTC asserts IRQ8#, and is not affected by any other enable bit. This bit is not affected by warm resets.
9	RV	0	Reserved
8	RO	0	**Power Button Status (PB):** Not reported by the Overlay. Handled by external EC.
7:6	RV	0	Reserved
5	RW1C	0	**Global Status (GLOB):** Set when SMIS.BRLS is written to 1. It always cause an SCI (regardless of PM1C.SCIEN).
4	RO	0	**Bus Master Status (BM):** This bit is always read as a 0.
3:1	RV	0	Reserved
0	RW1C	0	**Timer Overflow Status (TO):** Set anytime bit 22 of PM1T goes low. See PM1E.TO for the effect of this bit being set.

Table 3-168. Power Management 1 Enables (PM1E)

PM1E
I/O Base: PM1BLK Offset: 02h

Bit	Attribute	Default	Definition
15	RV	0	Reserved
14	RW	0	**PCIe WAKE Disable (PWAKED)**: This bit disables the inputs to the PCIEWSTS bit for waking the system. Modification of this bit has no impact on the value of the PCIEWSTS bit.
13:11	RV	0	Reserved
10	RW	0	**RTC Enable (RTC):** Resume Well. When set, and PM1S.RTC is set, an SMI#/SCI is generated. This bit is not cleared by any reset other than RTCRST#, CPU/internal thermal Trip, or internal watchdog trip.
9	RV	0	Reserved
8	RO	0	**Power Button (PB):** Not handled by the Overlay. Handled by external EC.
7:6	RV	0	Reserved
5	RW	0	**Global Enable (GLOB):** When this bit and PM1S.GLOB are set, SMI#/SCI is generated.
4	RO	0	**Bus Master Status (BM):** This bit is always reads as a 0.
3:1	RV	0	Reserved
0	RW	0	**Timer Overflow Enable (TO):** When set, and PM1S.TO is set, an SMI#/SCI is generated.

Table 3-169. Power Management 1 Controls (PM1C)

<table>
<tr><td colspan="4">PM1C
I/O Base: PM1BLK Offset: 04h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>31:14</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>13</td><td>WO</td><td>0</td><td>Sleep Enable (SLPEN): Reads to this bit always return 0. Setting this bit causes the system to sequence into the Sleep state defined by SLPTYP.</td></tr>
<tr><td>12:10</td><td>RW</td><td>0</td><td>Sleep Type (SLPTYP): Resume Well. This field defines the type of sleep the system enters when SLPEN is set. These bits are reset by RTCRST#.
<table>
<tr><th>Bits</th><th>Function</th></tr>
<tr><td>000h</td><td>S0-on</td></tr>
<tr><td>001 - 100h</td><td>Reserved</td></tr>
<tr><td>101h</td><td>S3- Suspend to RAM</td></tr>
<tr><td>110h</td><td>S4- Suspend to Disk</td></tr>
<tr><td>111h</td><td>S5- Soft Off</td></tr>
</table></td></tr>
<tr><td>9:3</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>2</td><td>WO</td><td>0</td><td>Global Release (GRLS): Sets SMIS.BIOS when written to 1. This bit always reads as 0.</td></tr>
<tr><td>1</td><td>RW</td><td>0</td><td>Bus Master Reload (BMRLD): This is treated as a scratchpad bit and has no functionality.</td></tr>
<tr><td>0</td><td>RW</td><td>0</td><td>SCI Enable (SCIEN): When set, events in GPE0_BLK generate SCI. When cleared, events generate SMI#.</td></tr>
</table>

Table 3-170. Power Management 1 Timer (PM1T)

<table>
<tr><td colspan="4">PM1T
I/O Base: PM1BLK Offset: 08h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>31:24</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>23:0</td><td>RO</td><td>0</td><td>Timer Value (VAL): Returns the running count of the PM timer. This counter runs off a 3.579545 MHz clock (derived from 14.31818 MHz divided by 4). It is reset on a platform reset, and runs continuously in S0. Any time bit 22 goes 1‘-to-0‘, PM1S.TO is set.</td></tr>
</table>

3.5.1.3 ACPI GPE0 Block (GPE0BLK)

Table 3-171. ACPI GPE0 Block (GPE0BLK)

Start	End	Offset	Register
00h	03h	GPE0S	General Purpose Event 0 Status
04h	07h	GPE0E	General Purpose Event 0 Enable
10h	13h	SMIE	SMI# Enables
14h	17h	SMIS	SMI# Status
18h	1Bh	GPEC	General Purpose Event Control
20h	23h	C34R	C3/C4 Residency
24h	27h	C56R	C5/C6 Residency
28h	2Bh	PMCW	Power Management Configuration Core Well
2Ch	2Fh	PMSW	Power Management Configuration Suspend Well
30h	33h	PMRW	Power Management Configuration RTC Well
34h	37h	TRC	TRC Register in RTC well

3.5.1.3.1 General Purpose Event 0 Status (GPE0S)

Table 3-172. General Purpose Event 0 Status (GPE0S)

GPE0S **I/O Base: GPE0BLK** **Offset: 00h**			
Bit	**Attribute**	**Default**	**Description**
31:30	RV	0h	Reserved
29	RW1C	0h	**SCIAGT28:** Set when a Assert SCI SB message from PCIe* RP 1 (SB Port ID 0x28) is received.
28	RW1C	0h	**SCIAGT29:** Set when a Assert SCI SB message from PCIe RP 2 (SB Port ID 0x29) is received.
27	RW1C	0h	**SCIAGT2A:** Set when a Assert SCI SB message from PCIe RP 3 (SB Port ID 0x2A) is received.
26	RW1C	0h	**SCIAGT2B:** Set when a Assert SCI SB message from PCIe RP 4 (SB Port ID 0x2B) is received.
16	RW1C	0h	**SCIAGT4:** Set when a Assert SCI SB message from Power Management unit (SB Port ID 0x4) is received.
15	RV	0h	Reserved
14	RW1C	0h	**GPIO:** Set when a GPIO configured for GPE goes active.
13	RW1C	0h	Reserved
12	RW1C	0h	**Thermal Status:** Set anytime THRM# is received at the state defined by GPEC.TPOL.
11	RW1C	0h	**Software GPE Status:** Set when GPEC.SWGPE is set.
10	RW1C	0h	**LPC Error Status:** Set when error occurs on LPC interface.
9:0	RV	0h	Reserved

This is symmetrical to the GPE0E Register. If the corresponding bit in GPE0E is set, the status bit being set generates SCI if PM1C.SC1EN is set, or SMI# if PM1C.SC1EN is cleared.

Table 3-173. General Purpose Event 0 Enable (GPE0E)

GPE0E
I/O Base: GPE0BLK **Offset: 04h**

Bit	Attribute	Default	Description
31:30	RV	0h	Reserved
29	RW	0h	**SCIAGT28:** When set, enables GPE0S.SCIAGENT28 to generate SCI/SMI#.
28	RW	0h	**SCIAGT29:** When set, enables GPE0S.SCIAGENT29 to generate SCI/SMI#.
27	RW	0h	**SCIAGT2A:** When set, enables GPE0S.SCIAGENT2A to generate SCI/SMI#.
26	RW	0h	**SCIAGT2B:** When set, enables GPE0S.SCIAGENT2B to generate SCI/SMI#.
16	RW	0h	**SCIAGT4:** When set, enables GPE0S.SCIAGENT4 to generate SCI/SMI#.
15	RV	0h	Reserved
14	RW	0h	**GPIO:** Enables GPE0S.GPIO to generate SCI/SMI#.
13	RW	0h	Reserved
12	RW	0h	**Thermal Enable:** Enables GPE0S.THRM to generate SCI/SMI#.
11	RW	0h	**Software GPE Enable:** When set, enables GPE0S.SWGPE to cause an SCI/SMI#.
10	RW	0h	**LPC Error GPE Enable:** When set, enables GPE0S, LPCERR to cause an SCI/SMI#.
9:0	RV	0h	Reserved

This register is in the *Resume well.*

Table 3-174. SMI Enable (SMIE)

SMIE
I/O Base: GPE0BLK Offset: 10h

Bit	Attribute	Default	Description
31:18	RV	0h	Reserved
17	RW	0h	**SMIAGT4:** Enables SMIS.SMIAGENT4 to generate SMI.
16	RW	0h	**SMIAGT24:** Enables SMIS.SMIAGENT24 to generate SMI.
15:12	RV	0h	Reserved
11	RW	0h	**INTERNAL_MONITOR_TRAP:** Enables SMIS.INTERNAL_MONITOR_TRAP to generate SMI.
10	RW	0h	**DO_SERR (SERR):** Enables SMIS.SERR to generate SMI#.
9	RW	0h	**GPIO (GPIO):** Enables SMIS.GPIO to generate SMI#.
8	RW	0h	**Internal Use Only (IUO)**
7	RW	0h	**SM Bus Command Complete (SCC):** Enables SMIS.SCC to generate SMI#.
6	RW	0h	**SM Bus Alert (SMBA):** Enables SMIS.SMBA to generate SMI#.
5	RW	0h	**Serial IRQ Enable (SIRQ):** Enables SMIS.SIRQ to generate SMI#.
4	RW	0h	**APM Enable (APM):** Enables SMIS.APM to generate SMI#.
3	RW	0h	**SPI:** Enables SMIS.SPI to generate SMI#.
2	RW	0h	**Sleep (SLP):** Enables SMIS.SLP to cause SMI#.
1	RW	0h	**Software Timer (SWT):** Enables SMIS.SWT to cause SMI#.
0	RW	0h	**BIOS (BIOS):** Enables SMIS.BIOS to cause SMI#.

Table 3-175. SMI Status Register (SMIS)

SMIS
I/O Base: GPE0BLK Offset: 14h

Bit	Attribute	Default	Description
31	RW	0h	**End of SMI (EOS):** This bit is present only in the SMI Status register and not in SMI Enable register. When set, ILB de-asserts SMI#. Cleared when ILB asserts SMI#.
30	WO	0h	**BIOS Release (BRLS):** This bit is present only in the SMI Status register and not in SMI Enable register. Causes SCI to be generated by the ILB. Always reads 0.
29:18	RV	0h	Reserved
17	RW1C	0h	**SMIAGT4:** Set when a Assert SMI SB or SMI Trap SB message from the Power Management Unit (SB Port ID 0x4) is received.
16	RW1C	0h	**SMIAGT24:** Set when a Assert SMI SB or SMI Trap SB message from Root Fabric (RTF, SB Port ID 0x24) is received.
15:12	RV	0h	Reserved
11	RW1C	0h	**INTERNAL_MONITOR_TRAP:** Set when I/O Trapping on Internal Monitor trap register occurs.
10	RW1C	0h	**DO_SERR (SERR):** Set when DO_SERR message arrives on SOCF SB.
9	RW1C	0h	**GPIO (GPIO):** Set when a GPIO configured for SMI occurs.
8	RV	0h	**Internal Use Only (IUO):** Always set to 0h by HW.
7	RW1C	0h	**SM Bus Command Complete (SCC):** Set when SMBus generates SMI due to command completion.
6	RW1C	0h	**SM Bus Alert (SMBA):** Set when the SMBALERT# pin goes low.
5	RW1C	0h	**Serial IRQ Enable (SIRQ):** Set when SMI# was asserted in the Serial IRQ stream.
4	RW1C	0h	**APM Enable (APM):** Set when a write to SWSMICTL is performed.
3	RW1C	0h	**SPI:** Set when SPI logic is requesting an SMI.
2	RW1C	0h	**Sleep (SLP):** Set when a write occurs to PM1C.SLPEN.
1	RW1C	0h	**Software Timer (SWT):** When set, the software SMI# has expired.
0	RW1C	0h	**BIOS (BIOS):** Set when software sets PM1C.GRLS.

Table 3-176. General Purpose Event Control (GPEC)

GPEC
I/O Base: GPE0BLK Offset: 18h

Bit	Attribute	Default	Definition
31:2	RV	0	Reserved
1	WO	0	**Software GPE (SWGPE):** When set, SCH sets GPE0S.SWGPE. This bit always reads back as 0.
0	RW	0	**Thermal Polarity (TPOL):** This bit controls the polarity of THRM# needed to set GPE0S.THRM. When set, a HIGH value on THRM# sets GPE0S.THRM. When cleared, a LOW value on THRM# sets GPE0S.THRM.

Table 3-177. C3/C4 Residency Register (C34R)

C34R
I/O Base: GPE0BLK **Offset: 20h**

Bit	Attribute	Default	Definition
31:24	RV	0	Reserved
23:0	RO	0	**Residency (RES):** Increments at the rate of the PM timer while the CPU is in a C3 or C4 state.

Table 3-178. C5/C6 Residency Register (C56R)

C56R
I/O Base: GPE0BLK **Offset: 24h**

Bit	Attribute	Default	Definition
31:24	RV	0	Reserved
23:0	RO	0	**Residency (RES):** Increments at the rate of the PM timer while the CPU is in a C5 or C6 state.

Table 3-179. Power Management Configuration Core Well (PMCW)

PMCW
I/O Base: GPE0BLK **Offset: 28h**

Bit	Attribute	Default	Definition
31	RW	0	**Periodic SMI Enable (PSE):** When set, an SMIS.SWT is set by the rate specified by PSRS.
30:4	RV	0	Reserved
3	RW-O	0	**SMI Lock (SMIL):** When set, writes to SMIE. have no affect. This bit is only cleared by RESETB.
2:0	RW	0	**Periodic SMI Rate Selection (PSRS):** Indicates when the timer times out and causes an SMI#. All values are +/- 30 us (1 RTC clock). Valid values are:

Bits	Time	Bits	Time
000	1.5 ms	100	8 sec
001	16 ms	101	16 sec
010	32 ms	110	32 sec
011	64 ms	111	64 sec

Table 3-180. Power Management Configuration Suspend/Resume Well (PMSW)

PMSW **I/O Base: GPE0BLK**			**Offset: 2Ch**
Bit	**Attribute**	**Default**	**Definition**
31:2	RV	0	Reserved
1	RW	0	**CPU BIST Enable (CBE):** CPU BIST enable INIT functionality not supported.
0	RW	0	**DRAM Initialization Scratchpad (DRAMI):** This bit does not affect hardware functionality. It is provided as a BIOS scratchpad bit that is maintained through warm resets.

All bits in the above register are in the *resume well*.

Table 3-181. Power Management Configuration RTC Well (PMRW)

PMRW
I/O Base: GPE0BLK **Offset: 30h**

Bit	Attribute	Default	Definition
31:12	RV	0	Reserved
11	RW	0	**Top Swap (TS):** When set, SCH inverts A16 for cycles going to the BIOS space. When cleared, SCH does not invert A16. This bit is only reset by RTCRST#.
10	RV	0	Reserved
9	RW1C	0	**CMC Watchdog Trip Status (WDTS):** This bit is set when the CMC watchdog timer expires, causing a system shutdown. It is reset by warm and cold resets. It is maintained through the shutdown sequence that is initiated via this trip.
8:5	RV	0	Reserved
4:0	RW	0	The RTC Bias Resistor function of bits [4:0] is de-featured. Bit 4 can be used for software to indicate an RTC power loss event by writing a “1” when RTC power is present. The bit will be reset by the hardware to “0” after a loss of RTC power, for example, when replacing the RTC battery.

All bits in the above register are in the *RTC well.*

Table 3-182. TRC Register in RTC well (TRC)

TRC
I/O Base: GPE0BLK **Offset: 34h**

Bit	Attribute	Default	Definition
31:2	RV	0	Reserved
1	RW	1	**RTC ortcos32fend**: When asserted, the signal on pad RTCX1 is sent out on the pin osc32fout. Otherwise osc32fout is always 0.
0	RW	0	**RTC ortcdswen**: When asserted (test mode) RTCIO is programmed to be in deep sleep.

All bits in the above register are in the *RTC well.*

3.5.2 High Precision Event Timer – HPET

This function provides a set of timers used by the operating system for timing events. One timer block is implemented containing one counter and three timers.

The register space is memory mapped to a 1 k block at address FED00000h. All registers are in the core well and reset by RESETB. Accesses that cross register boundaries result in undefined behavior.

Table 3-183. High Precision Event Timer Registers

Start	End	Offset	Register
000	007	GCID	General Capabilities and ID
010	017	GC	General Configuration
020	027	GIS	General Interrupt Status
0F0	0F7	MCV	Main Counter Value
100	107	T0C	Timer 0 Config and Capabilities
108	10F	T0CV	Timer 0 Comparator Value
120	127	T1C	Timer 1 Config and Capabilities
128	12F	T1CV	Timer 1 Comparator Value
140	147	T2C	Timer 2 Config and Capabilities
148	14F	T2CV	Timer 2 Comparator Value

Table 3-184. General Capabilities and ID (GCID)

GCID
Address: FED0_0000h

Bit	Attribute	Default	Definition
63:32	RO	0429B17Fh	**Counter Tick Period (CTP):** Indicates a period of 69.841279 ns, (14.1318 MHz clock period).
31:16	RO	8086h	**Vendor ID (VID):** Value of 8086h indicates Intel.
15	RO	1	**Legacy Route Capable (LRC):** Indicates support for Legacy Interrupt Route.
14	RV	0	Reserved
13	RO	1	**Counter Size (CS):** This bit is set to indicate that the main counter is 64 bits wide.
12:08	RO	02h	**Number of Timers (NT):** Indicates that 3 timers are supported.
07:00	RO	01h	**Revision ID (RID):** Indicates that revision 1.0 of the specification is implemented.

Table 3-185. General Configuration (GC)

GC
Address: FED0_0010h

Bit	Attribute	Default	Definition
63:2	RV	0	Reserved
1	RW	0	**Legacy Route Enable (LRE):** When set, interrupts are routed as follows: • Timer 0 routes to IRQ0 in 8259 or IRQ2 in the I/O APIC. • Timer 1 routes to IRQ8 in 8259 and I/O APIC. • Timer 2 is routed as per the routing in T2C. When set, the T[0-1]C.IR has no impact for timers 0 and 1.
0	RW	0	**Overall Enable (EN):** When set, the timers can generate interrupts. When cleared, the main counter halts and no interrupts are caused by any timer. For level-triggered interrupts, if an interrupt is pending when this bit is cleared, the GIS.Tx is not cleared.

Table 3-186. General Interrupt Status (GIS)

GIS
Address: FED0_0020h

Bit	Attribute	Default	Definition
63:03	RV	0	Reserved
02	RW1C	0	**Timer 2 Status (T2):** Same functionality as T0, for timer 2.
01	RW1C	0	**Timer 1 Status (T1):** Same functionality as T0, for timer 1.
00	RW1C	0	**Timer 0 Status (T0):** In edge triggered mode, this bit always reads as 0. In level triggered mode, this bit is set when an interrupt is active.

Table 3-187. Main Counter Value (MCV)

MCV
Address: FED0_00F0h

Bit	Attribute	Default	Definition
63:00	RW	0	**Counter Value (CV):** Reads return the current value of the counter. Writes load the new value to the counter. Timers 1 and 2 return 0 for the upper 32-bits of this register.

Table 3-188. Timer 0 Config and Capabilities (T0C)

T0C
Address: FED0_0100h

Bit	Attribute	Default	Definition
63:32	RO	00f0000 0h	**Interrupt Route Capability (IRC):** Indicates I/OxAPIC interrupts the timer can use: • Timer 0: 00f00000h. Indicates support for IRQ20, 21, 22, 23
31:16	RV	0	Reserved
15	RO	0	**FSB Interrupt Delivery (FID):** Not supported.
14	RO	0	**FSB Enable (FE):** Not supported, since FID is not supported.
13:9	RW	00h	**Interrupt Route (IR):** Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back does not match what is written. If GC.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no affect.
08	RW	0	**Timer 32-bit Mode (T32M):** When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit is read/write and defaults to 0. For timers 1 and 2, this bit is read only 0.
07	RV	0	Reserved
06	RW	0	**Timer Value Set (TVS):** This bit returns 0 when read. Writes only affect Timer 0 if it is set to periodic mode. Writes have no affect for Timers 1 and 2.
05	RO	1	**Timer Size (TS):** 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
04	RO	1	**Periodic Interrupt Capable (PIC):** When set, hardware supports a periodic mode for this timer interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
03	RW	0	**Timer Type (TYP):** If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
02	RW	0	**Interrupt Enable (IE):** When set, enables the timer to cause an interrupt when it times out. When cleared, the timer counts and generates status bits, but does not cause an interrupt.
01	RW	0	**Timer Interrupt Type (IT):** When cleared, interrupt is edge triggered. When set, interrupt is level triggered and held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
00	RV	0	Reserved

Table 3-189. Timer 1 Config and Capabilities (T1C)

T1C
Address: FED0_0120h

Bit	Attribute	Default	Definition
63:32	RO	00f00000h	**Interrupt Route Capability (IRC):** Indicates I/OxAPIC interrupts the timer can use: • Timer 0,1: 00f00000h. Indicates support for IRQ20, 21, 22, 23
31:16	RV	0	Reserved
15	RO	0	**FSB Interrupt Delivery (FID):** Not supported.
14	RO	0	**FSB Enable (FE):** Not supported, since FID is not supported.
13:9	RW	00h	**Interrupt Route (IR):** Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back does not match what is written. If GC.LRE is set, then Timers 0 and 1 have a fixed routing, and this field has no affect.
08	RO	0	**Timer 32-bit Mode (T32M):** When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit is a read/write and defaults to 0. For timers 1 and 2, this bit is read only 0.
07	RV	0	Reserved
06	RO	0	**Timer Value Set (TVS):** This bit returns 0 when read. Writes only have an affect for Timer 0 if it is set to periodic mode. Writes have no affect for Timers 1 and 2.
05	RO	0	**Timer Size (TS):** 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
04	RO	0	**Periodic Interrupt Capable (PIC):** When set, hardware supports a periodic mode for this timer interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
03	RO	0	**Timer Type (TYP):** If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
02	RW	0	**Interrupt Enable (IE):** When set, enables the timer to cause an interrupt when it times out. When cleared, the timer counts and generates status bits, but does not cause an interrupt.
01	RW	0	**Timer Interrupt Type (IT):** When cleared, interrupt is edge triggered. When set, interrupt is level triggered and held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
00	RV	0	Reserved

Table 3-190. Timer 2 Config and Capabilities (T2C)

T2C
Address: FED0_0140h

Bit	Attribute	Default	Definition
63:32	RO	00f00800h	**Interrupt Route Capability (IRC):** Indicates I/OxAPIC interrupts the timer can use: • Timer 2: 00f00800h. Indicates support for IRQ11, 20, 21, 22, and 23
31:16	RV	0	Reserved
15	RO	0	**FSB Interrupt Delivery (FID):** Not supported
14	RO	0	**FSB Enable (FE):** Not supported, since FID is not supported.
13:9	RW	00h	**Interrupt Route (IR):** Indicates the routing for the interrupt to the IOxAPIC. If the value is not supported by this particular timer, the value read back does not match what is written.
08	RO	0	**Timer 32-bit Mode (T32M):** When set, this bit forces a 64-bit timer to behave as a 32-bit timer. For timer 0, this bit is read/write and defaults to 0. For timers 1 and 2, this bit is read only 0.
07	RV	0	Reserved
06	RO	0	**Timer Value Set (TVS):** This bit returns 0 when read. Writes only have an affect for Timer 0 if it is set to periodic mode. Writes have no affect for Timers 1 and 2.
05	RO	0	**Timer Size (TS):** 1 = 64-bits, 0 = 32-bits. Set for timer 0. Cleared for timers 1 and 2.
04	RO	0	**Periodic Interrupt Capable (PIC):** When set, hardware supports a periodic mode for this timer interrupt. This bit is set for timer 0, and cleared for timers 1 and 2.
03	RO	0	**Timer Type (TYP):** If PIC is set, this bit is read/write, and can be used to enable the timer to generate a periodic interrupt. This bit is RW for timer 0, and RO for timers 1 and 2.
02	RW	0	**Interrupt Enable (IE):** When set, enables the timer to cause an interrupt when it times out. When cleared, the timer counts and generates status bits, but does not cause an interrupt.
01	RW	0	**Timer Interrupt Type (IT):** When cleared, interrupt is edge triggered. When set, interrupt is level triggered and held active until it is cleared by writing 1 to GIS.Tn. If another interrupt occurs before the interrupt is cleared, the interrupt remains active.
00	RV	0	Reserved

3.5.3 T0CV, T1CV, T2CV – Timer N Comparator Value

Reading this register returns the current value of the comparator. The default value for each timer is all 1s for the bits that are implemented. Timer 0 is 64-bits wide. Timers 1 and 2 are 32-bits wide.

Table 3-191. Timer 0 Comparator Value(T0CV)

T0CV
Address: FED0_0108h

Bit	Attribute	Default	Definition
63:0	RW-V	FFFF_FFFF_FFFF_FFFFh	**Current Comparator Value (CCV):** Reads returns the current comparator value.

Table 3-192. Timer 1 Comparator Value(T1CV)

T1CV
Address: FED0_0128h

Bit	Attribute	Default	Definition
63:0	RW	0000_0000_FFFF_FFFFh	**Current Comparator Value (CCV):** Reads returns the current comparator value, only bits [31:0] are implemented.

Table 3-193. Timer 2 Comparator Value(T2CV)

T2CV
Address: FED0_0148h

Bit	Attribute	Default	Definition
63:0	RW	0000_0000_FFFF_FFFFh	**Current Comparator Value (CCV):** Reads returns the current comparator value, only bits [31:0] are implemented.

3.5.4 8254 Timer

The 8254 contains three counters which have fixed uses. All registers are in the core well and clocked by a 14.31818 MHz clock.

3.5.4.1 Counter 0, System Timer

This counter functions as the system timer by controlling the state of IRQ0 and is programmed for Mode 3 operation. The counter produces a square wave with a period equal to the product of the counter period (838 ns) and the initial count value. The counter loads the initial count value one counter period after software writes the count value to the counter I/O address. The counter initially asserts IRQ0 and decrements the count value by two each counter period. The counter negates IRQ0 when the count value reaches 0. It then reloads the initial count value and again decrements the initial count value by two each counter period. The counter then asserts IRQ0 when the count value reaches 0, reloads the initial count value, and repeats the cycle, alternately asserting and negating IRQ0.

3.5.4.2 Counter 1, Refresh Request Signal

This counter is programmed for Mode 2 operation and impacts the period of the NSC.RTS (NMI Status and Control Register, bit 4, Refresh Cycle Toggle Status). Programming the counter to anything other than Mode 2 results in undefined behavior.

3.5.4.3 Counter 2, Speaker Tone

This counter is programmed for Mode 3 operation.

3.5.5 Timer I/O Registers

Table 3-194. Timer I/O Registers

Port	Register Name/Function	Default Value	Type
40h/50h	Counter 0 Interval Time Status Byte Format	0XXXXXXXb	Read Only
	Counter 0 Counter Access Port Register	Undefined	Read/Write
41h/51h	Counter 1 Interval Time Status Byte Format	0XXXXXXXb	Read Only
	Counter 1 Counter Access Port Register	Undefined	Read/Write
42h/52h	Counter 2 Interval Time Status Byte Format	0XXXXXXXb	Read Only
	Counter 2 Counter Access Port Register	Undefined	Read/Write
43h/53h	Timer Control Word Register	Undefined	Write Only
	Timer Control Word Register Read Back	XXXXXXX0b	Write Only
	Counter Latch Command	X0h	Write Only

Table 3-195. Timer Control Word Register (TCW)

TCW
I/O Address: 43h

Bit	Attribute	Default	Definition
07:06	WO	undef	**Counter Select (CS):** The Counter Selection bits select the counter the control word acts upon as shown below. The Read Back Command is selected when bits[7:6] are both 1. • 00 Counter 0 select • 01 Counter 1 select • 10 Counter 2 select • 11 Read Back Command
05:04	WO	undef	**Read/Write Select (RWS):** The counter programming is done through the counter port (40h for counter 0, 41h for counter 1, and 42h for counter 2). • 00 Counter Latch Command • 01 Read/Write Least Significant Byte (LSB) • 10 Read/Write Most Significant Byte (MSB) • 11 Read/Write LSB then MSB
03:01	WO	undef	**Counter Mode Selection (CMS):** Selects one of six modes of operation for the selected counter. • 000 = Out signal on end of count (=0) • 001 = Hardware retriggerable one-shot • x10 = Rate generator (divide by n counter) • x11 = Square wave output • 100 = Software triggered strobe • 101 = Hardware triggered strobe
00	WO	undef	**Binary/BCD Countdown Select (BCS):** 0 = Binary countdown is used. The largest possible binary count is 2. 1 = Binary coded decimal (BCD) count is used. The largest possible BCD count is 10.

The above register is programmed prior to any counter being accessed to specify counter modes. Following reset, the control words for each register are undefined and each counter output is 0. Each timer must be programmed to bring it into a known state.

There are two special commands that can be issued to the counters through this register, the Read Back Command and the Counter Latch Command. When these commands are chosen, several bits within this register are redefined. These register formats are described in Table 3-82, “Root Error Detect Mask Register (ROOTERRDETMSK)” on page 68.

Table 3-196. Read Back Command (RBC)

Bit	Attribute	Default	Definition
07:06	RW	00	**Read Back Command (RBC):** Must be 11 to select the Read Back Command.
05	RW	0	**Latch Count (LC):** When cleared, the current count value of the selected counters is latched.
04	RW	0	**Latch Status (LS):** When cleared, the status of the selected counters is latched.
03	RW	0	**Counter 2 Select (C2S):** When set to 1, Counter 2 count and/or status is latched.
02	RW	0	**Counter 1 Select (C1S):** When set to 1, Counter 1 count and/or status is latched.
01	RW	0	**Counter 0 Select (C0S):** When set to 1, Counter 0 count and/or status is latched.
00	RV	0	Reserved

This is used to determine the count value, programmed mode, and current states of the OUT pin and Null count flag of the selected counter or counters. Status and/or count may be latched in any or all of the counters by selecting the counter during the register write. The count and status remain latched until read, and further latch commands are ignored until the count is read.

Both count and status of the selected counters may be latched simultaneously by setting both bit 5 and bit 4 to 0. If both are latched, the first read operation from that counter returns the latched status. The next one or two reads, depending on whether the counter is programmed for one or two byte counts, returns the latched count. Subsequent reads return an unlatched count.

Table 3-197. Counter Latch Command (CLC)

Bit	Attribute	Default	Definition
07:06	RW	00	**Counter Selection (CL):** Selects the counter for latching. If 11 is written, then the write is interpreted as a read back command. 00 = Counter 0 01 = Counter 1 10 = Counter 2
05:04	RW	00	**Counter Latch Command:** Write 00 to select the Counter Latch Command.
03:00	RV	0	Reserved. Must be 0.

This latches the current count value and is used to ensure the count read from the counter is accurate. The count value is then read from each counter's count register through the Counter Ports Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2). The count must be read according to the programmed format, i.e., if the counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other (read, write, or programming operations for other counters may be inserted between the reads). If a counter is latched once and then latched again before the count is read, the second Counter Latch Command is ignored.

Each counter status byte can be read following a Read Back Command. If latch status is chosen (bit 4=0, Read Back Command) as a read back option for a given counter, the next read from the counter's Counter Access Ports Register (40h for counter 0, 41h for counter 1, and 42h for counter 2) returns the status byte. The status byte returns the following.

Table 3-198. Interval Timer Status Byte Format Register (ITSTS[0-2])

<table>
<tr><td colspan="4">ITSTS
I/O Address: 40h, 41h, 42h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07</td><td>RO</td><td>0</td><td>Counter State (CS): When set, OUT of the counter is set. When cleared, OUT of the counter is 0.</td></tr>
<tr><td>06</td><td>RO</td><td>undef</td><td>Count Register: When cleared, indicates when the last count written to the Count Register (CR) has been loaded into the counting element (CE) and is available for reading. The time this happens depends on the counter mode. This is undefined until Read Back Command is issued.</td></tr>
<tr><td>05:04</td><td>RO</td><td>undef</td><td>Read/Write Selection: These reflect the read/write selection made through bits[5:4] of the control register. The binary codes returned during the status read match the codes used to program the counter read/write selection.
00 Counter Latch Command
01 Read/Write Least Significant Byte (LSB)
10 Read/Write Most Significant Byte (MSB)
11 Read/Write LSB then MSB</td></tr>
<tr><td>03:01</td><td>RO</td><td>undef</td><td>Mode: Returns the counter mode programming. The binary code returned matches the code used to program the counter mode, as listed under the bit function above.
<table>
<tr><th>Bits</th><th>Mode</th><th>Description</th></tr>
<tr><td>000</td><td>0</td><td>Out signal on end of count (=0)</td></tr>
<tr><td>001</td><td>1</td><td>Hardware retriggerable one-shot</td></tr>
<tr><td>x10</td><td>2</td><td>Rate generator (divide by n counter)</td></tr>
<tr><td>x11</td><td>3</td><td>Square wave output</td></tr>
<tr><td>100</td><td>4</td><td>Software triggered strobe</td></tr>
<tr><td>101</td><td>5</td><td>Hardware triggered strobe</td></tr>
</table></td></tr>
<tr><td>00</td><td>RO</td><td>undef</td><td>Countdown Type: 0 for binary countdown or a 1 for binary coded decimal (BCD) countdown.</td></tr>
</table>

Table 3-199. Counter Access Ports Register (CAP[0-2])

<table>
<tr><td colspan="4">CAP
I/O Address: 40h, 41h, 42h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07:00</td><td>RW</td><td>undef</td><td>Counter Port: Each counter port address is used to program the 16-bit Count Register. The order of programming, either LSB only, MSB only, or LSB then MSB, is defined with the Interval Counter Control Register at port 43h. The counter port is also used to read the current count from the Count Register, and return the status of the counter programming following a Read Back Command.</td></tr>
</table>

3.5.6 Real Time Clock – RTC

The Real Time Clock (RTC) module provides a battery backed-up date and time keeping device. Three interrupt features are available: time of day alarm with once a second to once a month range, periodic rates of 122µs to 500ms, and end of update cycle notification. Seconds, minutes, hours, days, day of week, month, and year are counted. The hour is represented in twelve or twenty-four hour format, and data can be represented in BCD or binary format. The design is meant to be functionally compatible with the Motorola MS146818B. The time keeping comes from a 32.768 kHz oscillating source, which is divided to achieve an update every second. The lower 14 bytes on the lower RAM block have very specific functions. The first ten are for time and date information. The next four (0Ah to 0Dh) are registers, which configure and report RTC functions. A host-initiated write takes precedence over a hardware update in the event of a collision.

3.5.6.1 I/O Registers

The RTC internal registers and RAM are organized as two banks of 128 bytes each, called the standard and extended banks. The first 14 bytes of the standard bank contain the RTC time and date information along with four registers, A - D, that are used for configuration of the RTC. The extended bank contains a full 128 bytes of battery backed SRAM. All data movement between the host CPU and the RTC is done through registers mapped to the standard I/O space. The register map appears below.

Table 3-200. I/O Registers

I/O Locations	Function
70h and 74h	Real-Time Clock (Standard RAM) Index Register ***Note:*** Writes to 72h, 74h, and 76h do not affect the NMI enable (bit 7 of 70h)
71h and 75h	Real-Time Clock (Standard RAM) Target Register
72h and 76h	Extended RAM Index Register (if enabled)
73h and 77h	Extended RAM Target Register (if enabled)

I/O locations 70h and 71h are the standard ISA locations for the real-time clock. Locations 72h and 73h are for accessing the extended RAM. The extended RAM bank is also accessed using an indexed scheme. I/O address 72h is used as the address pointer and I/O address 73h is used as the data register. Index addresses above 127~~h~~ are not valid.

3.5.6.2 Indexed Registers

The RTC contains two sets of indexed registers that are accessed using the two separate Index and Target registers (70/71h or 72/73h), as shown below.

Table 3-201. Indexed Registers (Sheet 1 of 2)

Start	End	Name
00h	00h	Seconds
01h	01h	Seconds Alarm
02h	02h	Minutes
03h	03h	Minutes Alarm
04h	04h	Hours
05h	05h	Hours Alarm
06h	06h	Day of Week

Table 3-201. Indexed Registers (Sheet 2 of 2)

Start	End	Name
07h	07h	Day of Month
08h	08h	Month
09h	09h	Year
0Ah	0Ah	Register A
0Bh	0Bh	Register B
0Ch	0Ch	Register C
0Dh	0Dh	Register D
0Eh	7Fh	114 Bytes of User RAM

Table 3-202. RTC Index Register (RTCIDX)

RTCIDX
I/O Address: 70h

Bit	Attribute	Default	Definition
07:00	RW	0	**RTC Register Index (RRI):** Specify which RTC register to be read/written via the RTCWDW register.

Table 3-203. RTC Window Register (RTCWDW)

RTCWDW
I/O Address: 71h **Select: RTCIDX.RRI**

Bit	Attribute	Default	Definition
7:0	RW	0	**RTC Register Data (RRD):** Access to the RTC register pointed to by RTCIDX register.

This 8-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

Table 3-204. General Configuration Register A (RTCA)

<table>
<tr><td colspan="4">RTCA
Window: RTCWDW Index: 0Ah</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07</td><td>RW</td><td>undef</td><td>Update in progress (UIP): When set, an update is in progress. When cleared, the update cycle does not start for at least 488 µs. The time, calendar, and alarm information in RAM is always available when this bit is cleared.</td></tr>
<tr><td>06:04</td><td>RW</td><td>undef</td><td>Division Chain Select (DV): Controls the divider chain for the oscillator, and are not affected by RSMRST# or any other reset signal.
<table>
<tr><th>Bits</th><th>Function</th><th>Bits</th><th>Function</th></tr>
<tr><td>0h</td><td>Invalid</td><td>4h</td><td>Bypass 10 stages (test mode only)</td></tr>
<tr><td>1h</td><td>Invalid</td><td>5h</td><td>Bypass 15 stages (test mode only)</td></tr>
<tr><td>2h</td><td>Normal Operation</td><td>6h</td><td>Divider Reset</td></tr>
<tr><td>3h</td><td>Bypass 5stages (test mode only)</td><td>7h</td><td>Divider Reset</td></tr>
</table>
</td></tr>
<tr><td>03:00</td><td>RW</td><td>undef</td><td>Rate Select (RS): Selects one of 13 taps of the 15 stage divider chain. The selected tap can generate a periodic interrupt if B.PIE bit is set. Otherwise this tap is set C.PF.
<table>
<tr><th>Bits</th><th>Periodic Rate</th><th>Bits</th><th>Periodic Rate</th></tr>
<tr><td>0h</td><td>Interrupt never toggles</td><td>8h</td><td>3.90625 ms</td></tr>
<tr><td>1h</td><td>3.90625 ms</td><td>9h</td><td>7.8125 ms</td></tr>
<tr><td>2h</td><td>7.8125 ms</td><td>Ah</td><td>15.625 ms</td></tr>
<tr><td>3h</td><td>122.070 µs</td><td>Bh</td><td>31.25 ms</td></tr>
<tr><td>4h</td><td>244.141 µs</td><td>Ch</td><td>62.5 ms</td></tr>
<tr><td>5h</td><td>488.281 µs</td><td>Dh</td><td>125 ms</td></tr>
<tr><td>6h</td><td>976.5625 µs</td><td>Eh</td><td>250 ms</td></tr>
<tr><td>7h</td><td>1.953125 ms</td><td>Fh</td><td>500 ms</td></tr>
</table>
</td></tr>
</table>

This register is in the RTC well, and is used for general configuration of the RTC functions. None of the bits are affected by RSMRST# or any other reset signal.

Table 3-205. General Configuration Register B (RTCB)

RTCB **Window: RTCWDW**			**Index: 0Bh**
Bit	**Attribute**	**Default**	**Definition**
07	RW	undef	**Update Cycle Inhibit (SET):** When cleared, an update cycle occurs once each second. If set, a current update cycle aborts and subsequent update cycles do not occur until SET is returned to zero. When set, SW may initialize time and calendar bytes safely.
06	RW	0	**Periodic Interrupt Enable (PIE):** When set, and C.PF is set, an interrupt is generated.
05	RW	undef	**Alarm Interrupt Enable (AIE):** When set, and C.AF is set, an interrupt is generated.
04	RW	0	**Update-ended Interrupt Enable (UIE):** When set and C.UF is set, an interrupt is generated.
03	RW	0	**Square Wave Enable (SQWE):** Not implemented.
02	RW	undef	**Data Mode (DM):** When set, represents binary representation. When cleared, denotes BCD.
01	RW	undef	**Hour Format (HF):** When set, twenty-four hour mode is selected. When cleared, twelve-hour mode is selected. In twelve hour mode, the seventh bit represents AM (cleared) and PM (set).
00	RW	undef	**Daylight Savings Enable (DSE):** Only RW bit present.

This register resides in the RTC well. Bits are reset by RTCRST#.

Table 3-206. Flag Register C (RTCC)

RTCC **Window: RTCWDW**			**Index: 0Ch**
Bit	**Attribute**	**Default**	**Definition**
07	RC	0	**Interrupt Request Flag (IRQF)**: This bit is an AND of the flag with its corresponding interrupt enable in register B, and causes the RTC Interrupt to be asserted.
06	RC	0	**Periodic Interrupt Flag (PF):** Set when the tap as specified by A.RS is one.
05	RC	undef	**Alarm Flag (AF):** Set after all Alarm values match the current time.
04	RC	0	**Update-ended Flag (UF):** Set immediately following an update cycle for each second.
03:00	RV	0	Reserved

All bits in this register are cleared when this register is read. This register is cleared upon RSMRST#.

Table 3-207. Flag Register D (RTCD)

RTCD **Window: RTCWDW**			**Index: 0Dh**
Bit	**Attribute**	**Default**	**Definition**
07	RO	1	**Valid RAM and Time Bit (VRT):** This bit is always written as a 0 for write cycle; however, the bit returns a 1 for read cycles.
06	RV	0	Reserved. This bit always returns a 0 and be set to 0 for write cycles.
05:00	RW	0	**Date Alarm (DA): T**hese bits store the date of month alarm value. If set to 000000, then a (don't care) state is assumed. If the date alarm is not enabled, these bits return zeros to mimic the functionality of the Motorola 146818B. These bits are not affected by any reset assertion.

3.5.7 8259 Programmable Interrupt Controller

The ISA compatible interrupt controller (8259) incorporates the functionality of two 8259 interrupt controllers. The following table shows how the cores are connected.

Table 3-208. Master 8259 Input Mapping

8259 Input	Connected Pin / Function
0	Internal Timer / Counter 0 output or HPET Timer #0
1	IRQ1 via SERIRQ
2	Slave Controller INTR output
3	IRQ3 via SERIRQ, PIRQx
4	IRQ4 via SERIRQ, PIRQx
5	IRQ5 via SERIRQ, PIRQx
6	IRQ6 via SERIRQ, PIRQx
7	IRQ7 via SERIRQ, PIRQx

Table 3-209. Slave 8259 Input Mapping

8259 Input	Connected Pin / Function
0	Inverted IRQ8# from internal RTC or HPET Timer #1
1	IRQ9 via SERIRQ, SCI, or PIRQx
2	IRQ10 via SERIRQ, SCI, or PIRQx
3	IRQ11 via SERIRQ, SCI, or PIRQx, HPET timer #2
4	IRQ12 via SERIRQ or PIRQx
5	PIRQx
6	SERIRQ, PIRQx
7	PIRQx

The slave controller is cascaded onto the master controller through master controller interrupt input 2. Interrupts can individually be programmed to be the edge or level triggered, except for IRQ0, IRQ2, IRQ8#. Active-low interrupt sources, such as the PIRQ#, are internally inverted before being sent to the 8259. In the following descriptions of the 8259s, the interrupt levels are in reference to the signals at the internal interface of the 8259s, after the required inversions have occurred. Therefore, the term “high” indicates “active”, which means “low” on an originating PIRQ#.

3.5.7.1 I/O Registers

The interrupt controller registers are located at 20h and 21h for the master controller (IRQ0 - 7), and at A0h and A1h for the slave controller (IRQ8 - 13). These registers have multiple functions, depending upon the data written to them. Below is a description of the different register possibilities for each address.

Table 3-210. I/O Registers

Port	Aliases	Register Name/Function
20h	24h, 28h, 2Ch, 30h, 34h, 38h, 3Ch	Master 8259 ICW1 Init. Cmd Word 1 Register
		Master 8259 OCW2 Op Ctrl Word 2 Register
		Master 8259 OCW3 Op Ctrl Word 3 Register
21h	25h, 29h, 2Dh, 31h, 35h, 39h, 3Dh	Master 8259 ICW2 Init. Cmd Word 2 Register
		Master 8259 ICW3 Init. Cmd Word 3 Register
		Master 8259 ICW4 Init. Cmd Word 4 Register
		Master 8259 OCW1 Op Ctrl Word 1 Register
A0h	A4h, A8h, ACh, B0h, B4h, B8h, BCh	Slave 8259 ICW1 Init. Cmd Word 1 Register
		Slave 8259 OCW2 Op Ctrl Word 2 Register
		Slave 8259 OCW3 Op Ctrl Word 3 Register
A1h	A5h, A9h, ADh, B1h, B5h, B9h, BDh	Slave 8259 ICW2 Init. Cmd Word 2 Register
		Slave 8259 ICW3 Init. Cmd Word 3 Register
		Slave 8259 ICW4 Init. Cmd Word 4 Register
		Slave 8259 OCW1 Op Ctrl Word 1 Register
4D0h	-	Master 8259 Edge/Level Triggered Register
4D1h	-	Slave 8259 Edge/Level Triggered Register

Table 3-211. Master/Slave Initialization Command Word 1 ([M,S]ICW1)

[M,S]ICW1
I/O Address: 20h, A0h

Bit	Attribute	Default	Definition
07:05	WO	undef	**MCS85:** These bits are MCS-85 specific and not needed. They are programmed to 000.
04	WO	undef	**ICW/OCW select:** This bit must be a 1 to select ICW1 and enable the ICW2, ICW3, and ICW4 sequence.
03	WO	undef	**Edge/Level Bank Select (LTIM):** Disabled. Replaced by ELCR1 and ELCR2.
02	WO	undef	Reserved. Set to 0.
01	WO	undef	**Single or Cascade (SNGL):** Must be programmed to a 0 to indicate two controllers operating in cascade mode.
00	WO	undef	**wICW4 Write Required (IC4):** This bit must be programmed to a 1 to indicate that ICW4 needs to be programmed.

A write to Initialization Command Word 1 starts the interrupt controller initialization sequence, during which the following occurs:

- The Interrupt Mask register is cleared.
- IRQ7 input is assigned priority 7.
- The slave mode address is set to 7.
- Special Mask Mode is cleared and Status Read is set to IRR.

Once this write occurs the controller expects writes to ICW2, ICW3, and ICW4 to complete the initialization sequence.

Table 3-212. Master/Slave Initialization Command Word 2 ([M,S]ICW2)

<table>
<tr><td colspan="4">[M,S]ICW2
I/O Address: 21h, A1h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07:03</td><td>WO</td><td>undef</td><td>Interrupt Vector Base Address: Bits [7:3] define the base address in the interrupt vector table for the interrupt routines associated with each interrupt request level input.</td></tr>
<tr><td>02:00</td><td>WO</td><td>undef</td><td>Interrupt Request Level: When writing ICW2, these bits are all 0. During an interrupt acknowledge cycle, these bits are programmed by the interrupt controller with the interrupt to be serviced. This is combined with bits [7:3] to form the interrupt vector driven onto the data bus during the second INTA# cycle. The code is a three bit binary code:
<table>
<tr><th>Code</th><th>Master Interrupt</th><th>Slave Interrupt</th></tr>
<tr><td>000</td><td>IRQ0</td><td>IRQ8</td></tr>
<tr><td>001</td><td>IRQ1</td><td>IRQ9</td></tr>
<tr><td>010</td><td>IRQ2</td><td>IRQ10</td></tr>
<tr><td>011</td><td>IRQ3</td><td>IRQ11</td></tr>
<tr><td>100</td><td>IRQ4</td><td>IRQ12</td></tr>
<tr><td>101</td><td>IRQ5</td><td>IRQ13</td></tr>
<tr><td>110</td><td>IRQ6</td><td>IRQ14</td></tr>
<tr><td>111</td><td>IRQ7</td><td>IRQ15</td></tr>
</table></td></tr>
</table>

ICW2 is used to initialize the interrupt controller with the five most significant bits of the interrupt vector address. The value programmed for bits[7:3] is used by the CPU to define the base address in the interrupt vector table for the interrupt routines associated with each IRQ on the controller. Typical ISA ICW2 values are 08h for the master controller and 70h for the slave controller.

Table 3-213. Master Initialization Command Word 3 (MICW3)

<table>
<tr><td colspan="4">MICW3
I/O Address: 21h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07:03</td><td>WO</td><td>undef</td><td>These bits must be programmed to zero.</td></tr>
<tr><td>02</td><td>WO</td><td>undef</td><td>Cascaded Controller Connection (CCC): This bit must always be programmed to a 1 to indicate the slave controller for interrupts 8 15 is cascaded on IRQ2.</td></tr>
<tr><td>01:00</td><td>WO</td><td>undef</td><td>These bits must be programmed to zero.</td></tr>
</table>

Table 3-214. Slave Initialization Command Word 3 (SICW3)

SICW3
I/O Address: A1h

Bit	Attribute	Default	Definition
07:03	RV	0	Reserved. Must be 0.
02:00	WO	0	**Slave Identification Code:** This field must be programmed to 02h to match the code broadcast by the master controller during the INTA# sequence.

Table 3-215. Master/Slave Initialization Command Word 4 Register ([M,S]ICW4)

[M,S]ICW4
I/O Address: 21h, A1h

Bit	Attribute	Default	Definition
07:05	RV	0	Reserved. Must be 0.
04	WO	0	**Special Fully Nested Mode (SFNM):** Normally is disabled by writing a 0 to this bit. If SFNM=1, the special fully nested mode is programmed.
03	WO	0	**Buffered Mode (BUF):** Must be cleared for non-buffered mode. Writing 1 results in undefined behavior.
02	WO	0	**Master/Slave in Buffered Mode (MSBM):** Not used. Always programmed to 0.
01	WO	0	**Automatic End of Interrupt (AEOI):** This bit normally is programmed to 0. This is the normal end of interrupt. If this bit is 1, the automatic end of interrupt mode is programmed.
00	WO	1	**Microprocessor Mode (MM):** This bit must be written to 1 to indicate that the controller is operating in an Intel Architecture-based system. Writing 0 results in undefined behavior.

Table 3-216. Master/Slave Operational Control Word 1 ([M,S]OCW1)

[M,S]OCW1
I/O Address: 21h, A1h

Bit	Attribute	Default	Definition
07:00	RW	00h	**Interrupt Request Mask (IRM):** When a 1 is written to any bit in this register, the corresponding IRQ line is masked. When a 0 is written to any bit in this register, the corresponding IRQ mask bit is cleared, and interrupt requests again are accepted by the controller. Masking IRQ2 on the master controller also mask the interrupt requests from the slave controller.

Table 3-217. Master/Slave Operational Control Word 2 ([M,S]OCW2)

<table>
<tr><td colspan="4">[M,S]OCW2
I/O Address: 20h, A0h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07:05</td><td>WO</td><td>001</td><td>Rotate and EOI Codes: R, SL, EOI - These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations is listed above under the bit definition.
• 000 - Rotate in Auto EOI Mode (Clear)
• 001 - Non-specific EOI command
• 010 - No Operation
• 011 - *Specific EOI Command
• 100 - Rotate in Auto EOI Mode (Set)
• 101 - Rotate on Non-Specific EOI Command
• 110 - *Set Priority Command
• 111 - *Rotate on Specific EOI Command
*L0 - L2 Are Used</td></tr>
<tr><td>04:03</td><td>WO</td><td>undef</td><td>OCW2 Select: When selecting OCW2, bits 4:3 = 00.</td></tr>
<tr><td>02:00</td><td>WO</td><td>undef</td><td>Interrupt Level Select (L2, L1, L0): L2, L1, and L0 determine the interrupt level acted upon when the SL bit is active. A simple binary code, outlined above, selects the channel for the command to act upon. When the SL bit is inactive, these bits do not have a defined function; programming L2, L1 and L0 to 0 is sufficient in this case.
<table>
<tr><th>Bits</th><th>Interrupt Level</th><th>Bits</th><th>Interrupt Level</th></tr>
<tr><td>000</td><td>IRQ0/8</td><td>100</td><td>IRQ4/12</td></tr>
<tr><td>001</td><td>IRQ1/9</td><td>101</td><td>IRQ5/13</td></tr>
<tr><td>010</td><td>IRQ2/10</td><td>110</td><td>IRQ6/14</td></tr>
<tr><td>011</td><td>IRQ3/11</td><td>111</td><td>IRQ7/15</td></tr>
</table></td></tr>
</table>

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Table 3-218. Master/Slave Operational Control Word 3 ([M,S]OCW3) (Sheet 1 of 2)

<table>
<tr><td colspan="4">[M,S]OCW3
I/O Address: 20h, A0h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>07</td><td>RV</td><td>0</td><td>Reserved. Must be 0.</td></tr>
<tr><td>06</td><td>WO</td><td>0</td><td>Special Mask Mode (SMM): If this bit is set, the Special Mask Mode can be used by an interrupt service routine to dynamically alter the system priority structure while the routine is executing, through selective enabling/ disabling of the other channel's mask bits. Bit 6, the ESMM bit, must be set for this bit to have any meaning.</td></tr>
<tr><td>05</td><td>WO</td><td>1</td><td>Enable Special Mask Mode (ESMM): When set, the SMM bit is enabled to set or reset the Special Mask Mode. When cleared, the SMM bit becomes a (don’t care).</td></tr>
</table>

Table 3-218. Master/Slave Operational Control Word 3 ([M,S]OCW3) (Sheet 2 of 2)

[M,S]OCW3
I/O Address: 20h, A0h

Bit	Attribute	Default	Definition
04:03	WO	undef	**OCW3 Select (O3S):** When selecting OCW3, bits 4:3 = 01.
02	WO	undef	**Poll Mode Command (PMC):** When cleared, poll command is not issued. When set, the next I/O read to the interrupt controller is treated as an interrupt acknowledge cycle. An encoded byte is driven onto the data bus, representing the highest priority level requesting service.
01:00	WO	10	**Register Read Command (RRC):** These bits provide control for reading the ISR and Interrupt IRR. When bit 1=0, bit 0 does not affect the register read selection. Following ICW initialization, the default OCW3 port address read is read IRR. To retain the current selection (read ISR or read IRR), always write a 0 to bit 1 when programming this register. The selected register can be read repeatedly without reprogramming OCW3. To select a new status register, OCW3 must be reprogrammed prior to attempting the read. 00 No Action 01 No Action 10 Read IRQ Register 11 Read IS Register

Table 3-219. Master Edge/Level Control (ECLR1)

ECLR1
I/O Address: 4D0

Bit	Attribute	Default	Definition
07:03	RW	0	**Edge Level Control (ECL[7:3])**: In edge mode, (bit cleared), the interrupt is recognized by a low-to-high transition. In level mode (bit set), the interrupt is recognized by a high level.
02:00	RV	0	Reserved. The cascade channel, IRQ2, heart beat timer (IRQ0), and keyboard controller (IRQ1), cannot be put into level mode.

Table 3-220. Slave Edge/Level Control (ECLR2)

ECLR2
I/O Address: 4D1

Bit	Attribute	Default	Definition
07:06	RW	0	**Edge Level Control (ECL[15:14]):** In edge mode, (bit cleared), the interrupt is recognized by a low-to-high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 7 applies to IRQ15, and bit 6 to IRQ14.
05	RV	0	Reserved. The FERR# (IRQ13), cannot be programmed for level mode.
04:01	RW	0	**Edge Level Control (ECL[12:9]:** In edge mode, (bit cleared), the interrupt is recognized by a low-to-high transition. In level mode (bit set), the interrupt is recognized by a high level. Bit 4 applies to IRQ12, bit 3 to IRQ11, bit 2 to IRQ10, and bit 1 to IRQ9.
00	RV	0	Reserved. The Real Time Clock (IRQ8#) cannot be programmed for level mode.

3.5.8 IOxAPIC 1.1

The APIC is accessed via an indirect addressing scheme. These registers are mapped into memory space. The registers are shown below.

Table 3-221. IOxAPIC 1.1 Registers

Address	Symbol	Register
FEC00000h	IDX	Index Register
FEC00010h	WDW	Window Register
FEC00040h	EOI	EOI Register

Table 3-222. Index Register (IDX)

IDX **Address: FEC0_0000h**			
Bit	Attribute	Default	Definition
7:0	RW	0	**APIC Register Index (ARI):** Specify which IOAPIC register to be read/written via the WDW register.

This 8-bit register selects which indirect register appears in the window register to be manipulated by software. Software programs this register to select the desired APIC internal register.

Table 3-223. Window Register (WDW)

WDW **Address: FEC0_0010h** **Select: IDX.ARI**			
Bit	Attribute	Default	Definition
31:0	RW	0	**APIC Register Data (ARD):** Access to the IOAPIC register pointed to by IDX register.

This 32-bit register specifies the data to be read or written to the register pointed to by the IDX register. This register can be accessed only in DW quantities.

Table 3-224. EOI Register (EOI)

EOI **Address: FEC0_0040h**			
Bit	Attribute	Default	Definition
31:8	RV	0	Reserved
7:0	RW	0	**EOI Vector (EV):** Used for matching RTE to be cleared.

When a write is issued to this register, the IOxAPIC checks the lower 8 bits written to this register, and compare it with the vector field for each entry in the I/O Redirection Table. When a match is found, RTE.RIRR for that entry is cleared. If multiple entries have the same vector, each of those entries have RTE.RIRR cleared. Only bits 7:0 are used. Bits 31:08 are ignored.

3.5.8.1 Index Registers

The registers listed below are accessed via the IDX register. When accessing these registers, DWords must be used. Acesses not done this way result in unspecified behavior. Software does not attempt to write to registers. Some registers may return non-zero values when read.

Table 3-225. Index Registers

Offset	Symbol	Register
00	ID	Identification
01	VS	Version
02-0F	-	Reserved
10 11	RTE0	Redirection Table 0
12 13	RTE1	Redirection Table 1
...	...	...
3E 3F	RTE23	Redirection Table 23
40-FF	-	Reserved

Table 3-226. Identification Register (ID)

ID
Window: WDW Index: 00h

Bit	Attribute	Default	Definition
31:28	RV	0	Reserved
27:24	RW	0h	**APIC Identification (AID):** Software must program this value before using the APIC.
23:16	RV	0	Reserved
15	RW	0	Scratchpad
14	RV	0	Reserved
13:0	RV	0	Reserved

Table 3-227. Version Register (VS)

VS
Window: WDW Index: 01h

Bit	Attribute	Default	Definition
31:24	RV	0	Reserved
23:16	RO	17h	**Maximum Redirection Entries (MRE):** This is the entry number (0 being the lowest entry) of the highest entry in the redirection table. This field is hardwired to 17h to indicate 24 interrupts.
15	RO	0	**Pin Assertion Register Supported (PRQ):** The IOxAPIC does not implement the Pin Assertion Register.
14:08	RV	0	Reserved
07:00	RO	20h	**Version (VS):** Identifies the implementation version as IOxAPIC.

Table 3-228. Redirection Table Entry Low DWord(RTEL[0-23])

RTEL[0-23]
Window: WDW Index: 10h - 3Eh by 2h

Bit	Attribute	Default	Definition
31:17	RV	0	Reserved
16	RW	1	**Mask (MSK):** When set, interrupts are not delivered nor held pending. When cleared, and edge or level on this interrupt results in the delivery of the interrupt.
15	RW	undef	**Trigger Mode (TM):** When cleared, the interrupt is edge sensitive. When set, the interrupt is level sensitive.
14	RW	undef	**Remote IRR (RIRR):** This is used for level triggered interrupts its meaning is undefined for edge triggered interrupts. This bit is set when IOxAPIC sends the level interrupt message to the CPU. This bit is cleared when an EOI message is received that matches the VCT field. This bit is never set for SMI, NMI, INIT, or ExtINT delivery modes.
13	RW	undef	**Polarity (POL):** This specifies the polarity of each interrupt input. When cleared, the signal is active high. When set, the signal is active low.
12	RO	undef	**Delivery Status (DS):** This field contains the current status of the delivery of this interrupt. When set, an interrupt is pending and not yet delivered. When cleared, there is no activity for this entry.
11	RW	undef	**Destination Mode (DSM)**: This field is used by the local Epic to determine whether it is the destination of the message.
10:08	RW	undef	**Delivery Mode (DLM):** This field specifies how the APICs listed in the destination field act upon reception of this signal. Certain Delivery Modes only operate as intended when used in conjunction with a specific trigger mode. These encodings are: • 000 Fixed • 001 Lowest Priority • 010 SMI – Not supported • 011 Reserved • 100 NMI – Not supported • 101 INIT – Not supported • 110 Reserved • 111 ExtINT
07:00	RW	undef	**Vector (VCT):** This field contains the interrupt vector for this interrupt. Values range between 10h and FEh.

Table 3-229. Redirection Table Entry High DWord (RTEH[0-23])

RTEH[0-23]
Window: WDW Index: 11h - 3Fh by 2h

Bit	Attribute	Default	Definition
31:24	RW	undef	**Destination ID (DID):** Destination ID of the local APIC.
23:16	RW	undef	**Extended Destination ID (EDID):** Extended destination ID of the local APIC.
15:00	RV	0	Reserved

3.5.9 Interrupt Delivery - Interrupt Message Format

ILB writes the message on the backbone as a 32-bit memory write cycle. It uses the following formats the Address and Data.

Table 3-230. Interrupt Delivery Address Value

Bit	Description
31:20	FEEh
19:12	**Destination ID:** RTE[x].DID
11:04	**Extended Destination ID:** RTE[x].EDID
03	**Redirection Hint:** If RTE[x].DLM = “Lowest Priority” (001), this bit is set. Otherwise, this bit is cleared.
02	**Destination Mode:** RTE[x].DSM
01:00	00

Table 3-231. Interrupt Delivery Data Value

Bit	Description
31:16	0000h
15	**Trigger Mode:** RTE[x].TM
14	**Delivery Status:** 1 = Assert, 0 = Deassert. Only Assert messages are sent. This bit is always set to 1.
13:12	00
11	**Destination Mode:** RTE[x].DSM
10:08	**Delivery Mode:** RTE[x].DLM
07:00	**Vector:** RTE[x].VCT

3.5.10 LPC 1.1

3.5.10.1 PCI Header

Table 3-232. PCI Header Registers

Start	End	Symbol	Register Name
00	03	ID	Identifiers
04	05	CMD	Command
06	07	STS	Device Status
08	08	RID	Revision ID
09	0B	CC	Class Code
0E	0E	HTYPE	Header Type
2C	2F	SS	Subsystem Identifiers
40	43	SMBA	SM Bus Base Address
44	47	GBA	GPIO Base Address
48	4B	PM1BLK	PM1_BLK Base Address
4C	4F	GPE0BLK	GPE0_BLK Base Address
58	5B	ACTL	ACPI Control
5C	5F	MC	Miscellaneous Control
60	67	PxRC	PIRQx Routing Control where x is [A-H]
68	6B	SCNT	Serial IRQ Control
84	87	WDTBA	Watch Dog timer Base Address
D0	D3	FS	FWH ID Select
D4	D7	BDE	BIOS Decode Enable
D8	DB	BC	BIOS Control
F0	F3	RCBA	Root Complex Base Address

Table 3-233. Identifiers (ID)

ID **Bus: 0**	**Device: 31**	**Function: 0**	**Offset: 00h**
Bit	**Attribute**	**Default**	**Definition**
31:16	RO	0C60h	**Device Identification (DID):** PCI device ID assigned for the S12x0 LPC.
15:0	RO	8086h	**Vendor Identification (VID)**: Indicates Intel.

Table 3-234. Device Command (CMD)

CMD **Bus: 0**	**Device: 31**	**Function: 0**	**Offset: 04h**
Bit	**Attribute**	**Default**	**Definition**
15:2	RV	0	Reserved
1	RO	1	**Memory Space Enable (MSE):** Memory space cannot be disabled on LPC.
0	RO	1	**I/O Space Enable (IOSE)**: I/O space cannot be disabled on LPC.

Table 3-235. Status (STS)

STS **Bus: 0** **Device: 31** **Function: 0** **Offset: 06h**			
Bit	**Attribute**	**Default**	**Definition**
15:00	RV	0	Reserved

Table 3-236. Revision ID (RID)

RID **Bus: 0** **Device: 31** **Function: 0** **Offset: 08h**			
Bit	**Attribute**	**Default**	**Definition**
7:0	RW-O	00h	**Revision ID (RID):** Refer to the S12x0 Specification update for the value of the Revision ID Register.

Table 3-237. Class Code (CC)

CC **Bus: 0** **Device: 31** **Function: 0** **Offset: 09h**			
Bit	**Attribute**	**Default**	**Definition**
23:16	RO	06h	**Base Class Code (BCC):** Indicates the device is a bridge device.
15:08	RO	01h	**Sub-Class Code (SCC):** Indicates the device a PCI to ISA bridge.
07:00	RO	00h	**Programming Interface (PI):** The LPC bridge has no programming interface.

Table 3-238. Header Type (HTYPE)

HTYPE **Bus: 0** **Device: 31** **Function: 0** **Offset: 0Eh**			
Bit	**Attribute**	**Default**	**Definition**
07	RO	0	**Multi-function Device (MFD):** This bit is 0 to indicate a single function device.
06:00	RO	00h	**Header Type (HTYPE):** Identifies the header layout is a generic device.

Table 3-239. Sub System Identifiers (SS)

SS **Bus: 0** **Device: 31** **Function: 0** **Offset: 2Ch**			
Bit	**Attribute**	**Default**	**Definition**
31:16	RW-O	0000h	**Subsystem ID (SSID):** This is written by BIOS. No hardware action taken.
15:00	RW-O	0000h	**Subsystem Vendor ID (SSVID):** Default value can be written by BIOS. No hardware action is taken.

This register is initialized to logic 0 by the assertion of RESETB. This register can be written only once after RESETB de-assertion.

Table 3-240. SMBus Base Address (SMBA)

SMBA **Bus: 0** **Device: 31** **Function: 0** **Offset: 40h**			
Bit	**Attribute**	**Default**	**Definition**
31	RW	0	**Enable (EN):** When set, decode of the I/O range pointed to by the BA is enabled.
30:16	RV	0	Reserved. Always 0.
15:6	RW	0	**Base Address (BA):** Provides the 64 bytes of I/O space for SM Bus.
5:0	RV	0	Reserved. Always 0.

Table 3-241. GPIO Base Address (GBA)

GBA **Bus:0** **Device:31** **Function:0** **Offset: 44h**			
Bit	**Attribute**	**Default**	**Definition**
31	RW	0	**Enable (EN):** When set, decode of the I/O range pointed to by the BA is enabled.
30:16	RV	0	Reserved. Always 0.
15:7	RW	0	**Base Address (BA):** Provides the 128 bytes of I/O space for GPIO.
6:0	RV	0	Reserved. Always 0.

Table 3-242. Base Address (PM1BLK)

PM1BLK **Bus: 0** **Device: 31** **Function: 0** **Offset: 48h**			
Bit	**Attribute**	**Default**	**Definition**
31	RW	0	**Enable (EN):** When set, decode of the I/O range pointed to by the BA is enabled.
30:16	RV	0	Reserved. Always 0.
15:4	RW	0	**Base Address (BA):** Provides the 16 bytes of I/O space for PM1_BLK.
3:0	RV	0	Reserved. Always 0.

Table 3-243. Base Address (GPE0BLK)

GPE0BLK **Bus: 0** **Device: 31** **Function: 0** **Offset: 4Ch**			
Bit	**Attribute**	**Default**	**Definition**
31	RW	0	**Enable (EN):** When set, decode of the I/O range pointed to by the BA is enabled.
30:16	RV	0	Reserved. Always 0.
15:6	RW	0	**Base Address (BA):** Provides the 64 bytes of I/O space for GPE0_BLK.
5:0	RV	0	Reserved. Always 0.

Table 3-244. ACPI Control (ACTL)

<table>
<tr><td colspan="4">ACTL
Bus: 0 Device: 31 Function: 0 Offset: 58h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>31:3</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>2:0</td><td>RW</td><td>011</td><td>SCI IRQ Select (SCIS): Specifies to which IRQ the SCI is routed. If not using APIC, SCI must be routed to IRQ9-11, and that interrupt is not shared with SERIRQ, but is shared with other interrupts. If using APIC, SCI can be mapped to IRQ20-23, and can be shared with other interrupts.
<table>
<tr><th>Bits</th><th>SCI Map</th><th>Bits</th><th>SCI Map</th></tr>
<tr><td>000</td><td>IRQ9</td><td>100</td><td>IRQ20</td></tr>
<tr><td>001</td><td>IRQ10</td><td>101</td><td>IRQ21</td></tr>
<tr><td>010</td><td>IRQ11</td><td>110</td><td>IRQ22</td></tr>
<tr><td>011</td><td>SCI Disabled</td><td>111</td><td>IRQ23</td></tr>
</table>
When the interrupt is mapped to APIC interrupts 9, 10 or 11, APIC must be programmed for active-high reception. When the interrupt is mapped to APIC interrupt 20 through 23, APIC must be programmed for active-low reception.</td></tr>
</table>

Table 3-245. PIRQx Routing Control (P[A,B,C,D,E,F,G,H]RC)

<table>
<tr><td colspan="4">P[A,B,C,D,E,F,G,H]RC
Bus: 0 Device: 31 Function: 0 Offset: 60h - 67h by 1h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>7</td><td>RW</td><td>1</td><td>Interrupt Routing Enable (REN): When cleared, the corresponding PIRQx is routed to one of the legacy interrupts specified in bits[3:0]. When set, the PIRQx is not routed to the 8259.</td></tr>
<tr><td>6:4</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>3:0</td><td>RW</td><td>0</td><td>IRQ Routing (IR): Indicates how to route PIRQx#.
<table>
<tr><th>Bits</th><th>Mapping</th><th>Bits</th><th>Mapping</th></tr>
<tr><td>0h</td><td>Reserved</td><td>8h</td><td>Reserved</td></tr>
<tr><td>1h</td><td>Reserved</td><td>9h</td><td>IRQ9</td></tr>
<tr><td>2h</td><td>Reserved</td><td>Ah</td><td>IRQ10</td></tr>
<tr><td>3h</td><td>IRQ3</td><td>Bh</td><td>IRQ11</td></tr>
<tr><td>4h</td><td>IRQ4</td><td>Ch</td><td>IRQ12</td></tr>
<tr><td>5h</td><td>IRQ5</td><td>Dh</td><td>Reserved</td></tr>
<tr><td>6h</td><td>IRQ6</td><td>Eh</td><td>IRQ14</td></tr>
<tr><td>7h</td><td>IRQ7</td><td>Fh</td><td>IRQ15</td></tr>
</table></td></tr>
</table>

Offset 60h routes PIRQA, 61h routes PIRQB, 62h routes PIRQC, 63h routes PIRQD, 64h routes PIRQE, 65h routes PIRQF, 66h routes PIRQG, and 67h routes PIRQH.

Table 3-246. Serial IRQ Control (SCNT)

SCNT **Bus: 0**		**Device: 31**	**Function: 0** **Offset: 68h**
Bit	**Attribute**	**Default**	**Definition**
7	RW	0	**Mode (MD):** When set, the SIRQ is in continuous mode. When cleared, SIRQ is in quiet mode. This bit must be set to guarantee that the first action of SIRQ is a start frame.
6:0	RV	00	Reserved

Table 3-247. WDT Base Address (WDTBA)

WDTBA **Bus: 0**		**Device: 31**	**Function: 0** **Offset: 84h**
Bit	**Attribute**	**Default**	**Definition**
31	RW	0	**Enable:** When set, decode of the I/O range pointed to by the BA is enabled.
30:16	RV	0	**Reserved**
15:6	RW	0	**Base Address:** Provides the 64 bytes of I/O space for WDT.
5:0	RV	00	Reserved

Table 3-248. FWH ID Select (FS)

FS **Bus: 0**		**Device: 31**	**Function: 0** **Offset: D0h**
Bit	**Attribute**	**Default**	**Definition**
31:28	RO	0h	**F8-FF IDSEL (IF8):** IDSEL to use in FWH cycle for range enabled by BDE.EF8. The Address ranges are: FFF80000h – FFFFFFFFh, FFB80000h – FFBFFFFFh and 000E0000h – 000FFFFFh.
27:24	RW	0h	**F0-F7 IDSEL (IF0):** IDSEL to use in FWH cycle for range enabled by BDE.EF0. The Address ranges are: FFF00000h – FFF7FFFFh, FFB00000h – FFB7FFFFh.
23:20	RW	1h	**E8-EF IDSEL (IE8):** IDSEL to use in FWH cycle for range enabled by BDE.EE8. The Address ranges are: FFE80000h – FFEFFFFFh, FFA80000h – FFAFFFFFh.
19:16	RW	1h	**E0-E7 IDSEL (IE0):** IDSEL to use in FWH cycle for range enabled by BDE.EE0. The Address ranges are: FFE00000h – FFE7FFFFh, FFA00000h – FFA7FFFFh.
15:12	RW	2h	**D8-DF IDSEL (ID8): I**DSEL to use in FWH cycle for range enabled by BDE.ED8. The Address ranges are: FFD80000h – FFDFFFFFh, FF980000h – FF9FFFFFh.
11:08	RW	2h	**D0-D7 IDSEL (ID0):** IDSEL to use in FWH cycle for range enabled by BDE.ED0. The Address ranges are: FFD00000h – FFD7FFFFh, FF900000h – FF97FFFFh.
7:4	RW	3h	**C8-CF IDSEL (IC8):** IDSEL to use in FWH cycle for range enabled by BDE.EC8. The Address ranges are: FFC80000h – FFCFFFFFh, FF880000h – FF8FFFFFh.
3:0	RW	3h	**C0-C7 IDSEL (IC0):** IDSEL to use in FWH cycle for range enabled by BDE.EC0. The Address ranges are: FFC00000h – FFC7FFFFh, FF800000h – FF87FFFFh.

This register contains the IDSEL fields the LPC Bridge uses for memory cycles going to the FWH.

Table 3-249. BIOS Decode Enable (BDE)

BDE
Bus: 0 **Device: 31** **Function: 0** **Offset: D4h**

Bit	Attribute	Default	Definition
31	RO	1	**F8-FF Enable (EF8):** Enables decoding of BIOS range FFF80000h – FFFFFFFFh and FFB80000h – FFBFFFFFh. 0 = Disable, 1 = Enable.
30	RW	1	**F0-F8 Enable (EF0):** Enables decoding of BIOS range FFF00000h – FFF7FFFFh and FFB00000h – FFB7FFFFh. 0 = Disable, 1 = Enable.
29	RW	1	**E8-EF Enable (EE8):** Enables decoding of BIOS range FFE80000h – FFEFFFFFh and FFA80000h - FFAFFFFFh. 0 = Disable, 1 = Enable.
28	RW	1	**E0-E8 Enable (EE0):** Enables decoding of BIOS range FFE00000h – FFE7FFFFh and FFA00000h – FFA7FFFFh. 0 = Disable, 1 = Enable.
27	RW	1	**D8-DF Enable (ED8):** Enables decoding of BIOS range FFD80000h – FFDFFFFFh and FF980000h – FF9FFFFFh. 0 = Disable, 1 = Enable.
26	RW	1	**D0-D7 Enable (ED0):** Enables decoding of BIOS range FFD00000h – FFD7FFFFh and FF900000h – FF97FFFFh. 0 = Disable, 1 = Enable.
25	RW	1	**C8-CF Enable (EC8):** Enables decoding of BIOS range FFC80000h – FFCFFFFFh and FF880000h – FF8FFFFFh. 0 = Disable, 1 = Enable.
24	RW	1	**C0-C7 Enable (EC0):** Enables decoding of BIOS range FFC00000h – FFC7FFFFh and FF800000h – FF87FFFFh. 0 = Disable, 1 = Enable.
23:00	RV	0	Reserved

Table 3-250. BIOS Control (BC)

BCE
Bus: 0 **Device: 31** **Function: 0** **Offset: D8h**

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8	RW	1	**Prefetch Enable (PFE):** When set, BIOS prefetching is enabled. An access to BIOS causes a 64-byte fetch of the line starting at that region. Subsequent accesses within that region result in data being returned from the prefetch buffer. The prefetch buffer is invalidated when this bit is cleared, or a BIOS access occurs to a different line than what is currently in the buffer.
7	RW-L	0	**SMM BIOS Write Protect (SMM_BWP)**: When this bit is set to a 1, the BIOS region is not writable until SMM sets CF9 bit 7. This ensures that BIOS can only be modified inside SMM. When set to a 0, SMM SPI Flash write protection is disabled BC[1]. Locked when LE in this register is set to a 1.
6:3	RV	0	Reserved
2	RW	0	**Cache Disable:** Enable caching in read buffer for direct memory read.
1	RW-L	0	**Lock Enable (LE):** When set, setting the WP bit causes SMIs. When set, the SMM_BWP bit in this register is locked. When cleared, setting the WP bit does not cause SMIs. Once set, this bit can only be cleared by a RESET#.
0	RW	0	**Write Protect Disable (WPD):** When set, access to BIOS is enabled for both read and write cycles. When cleared, only read cycles are permitted to BIOS. When written from a 0 to a 1 and LE is also set, an SMI# is generated. This ensures that only SMM code can update BIOS.

3.5.11 Root Complex Register Block Configuration

Table 3-251. Root Complex Base Address (RCBA)

RCBA **Bus: 0**	**Device: 31**	**Function: 0**	**Offset: F0h**
Bit	**Attribute**	**Default**	**Definition**
31:14	RW	0	**Base Address (BA):** Base Address for the root complex register block decode range. This address is aligned on a 16 KB boundary.
13:01	RV	0	Reserved
00	RW	0	**Enable (EN):** When set, enables the range specified in BA to be claimed as the RCRB.

3.5.12 SPI - Host Interface Registers

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system flash versus the Firmware Hub interface that is available on the LPC pins.

The SPI Host Interface are memory-mapped in the RCRB Chipset Memory Space in offset range 3020h to 308Fh.

Warning: Address locations that are not listed are considered reserved register locations. Reads to reserved registers may return non-zero values. Writes to reserved locations may cause system failure.

Table 3-252. SPI Host Interface Registers

Offset Start	Offset End	Register ID Description (offset w.r.t. 0x3020)	Default Value
3020	3021	Offset 00h: SPIS – SPI Status	0001h
3022	3023	Offset 02h: SPIC – SPI Control	2005h
3024	3027	Offset 04h: SPIA – SPI Address	0
3028	302F	Offset 08h: SPID0 – SPI Data 0	0
3030	3067	Offset 10h, 18h, 20h, 28h, 30h, 38h and 40h: SPID[1-7] – SPI Data [1-7]	00000000_00000000h each SPID
3070	3073	Offset 50h: BBAR – BIOS Base Address	0
3074	3075	Offset 54h: PREOP – Prefix Opcode Configuration	0004h
3076	3077	Offset 56h: OPTYPE – Opcode Type	0
3078	307F	Offset 58h: OPMENU – Opcode Menu Configuration	00000005h
3080	3083	Offset 60h: PBR0 – Protected BIOS Range 0	00000000h
3084	3087	Offset 64h: PBR1 – Protected BIOS Range 1	00000000h
3088	308B	Offset 68h: PBR2– Protected BIOS Range 2	00000000h

Table 3-253. SPI Status (SPISTS)

SPISTS
Base: RCBA Offset: 3020h

Bit	Attribute	Default	Definition
15	RW-L	0h	**SPI Configuration Lock-Down:** When set to 1, the SPI Static Configuration information in offsets 50h through 6Bh can not be overwritten. Once set to 1, this bit can only be cleared by a hardware reset.
14:4	RV	0h	Reserved
3	RW1C	0h	**Blocked Access Status:** Hardware sets this bit to 1 when an access is blocked from running on the SPI interface due to one of the protection policies or when any of the programmed cycle registers are written while a programmed access is already in progress. This bit is set for both programmed accesses and direct memory reads that get blocked. This bit remains asserted until cleared by software writing a 1 or hardware reset.
2	RW1C	0h	**Cycle Done Status:** The sets this bit to 1 when the SPI Cycle completes (i.e., SCIP bit is 0) after software sets the GO bit. This bit remains asserted until cleared by software writing a 1 or hardware reset. When this bit is set and the SPI bit in Offset 02h: SPIC – SPI Control is set, an internal signal is asserted to the SMI# generation block. Software must make sure this bit is cleared prior to enabling the SPI SMI# assertion for a new programmed access. This bit gets set after the Status Register Polling sequence completes after reset deasserts. It is cleared before and during that sequence.
1	RV	0h	Reserved
0	RO	0h	**SPI Cycle In Progress:** Hardware sets this bit when software sets the SPI Cycle Go bit in the Offset 02h: SPIC – SPI Control. This bit remains set until the cycle completes on the SPI interface. Hardware automatically sets and clears this bit so that software can determine when read data is valid and/or when it is safe to begin programming the next command. Software must only program the next command when this bit is 0. This bit reports 1b during the Status Register Polling sequence after reset deasserts; it is cleared when that sequence completes.

Table 3-254. SPI Control (SPICTL)

SPICTL
Base: RCBA　**Offset: 3022h**

Bit	Attribute	Default	Definition
15	RW	0	**SPI SMI# Enable:** When set to 1, the SPI asserts an SMI# request whenever the Cycle Done Status bit is 1.
14	RW	1	**Data Cycle:** When set to 1, there is data that corresponds to this transaction. When 0, no data is delivered for this cycle, and the DBC and data fields themselves are do not cares.
13:08	RW	0	**Data Byte Count:** This field specifies the number of bytes to shift in or out during the data portion of the SPI cycle. The valid settings (in decimal) are any value from 0 to 63. The number of bytes transferred is the value of this field plus 1. ***Note:*** When this field is 00_0000b, then there is 1 byte to transfer and that 11_1111b means there are 64 bytes to transfer.
7	RV	0	Reserved
6:4	RW	0	**Cycle Opcode Pointer:** This field selects one of the programmed opcodes in the Offset 58h: OPMENU – Opcode Menu Configuration to be used as the SPI Command/Opcode. In the case of an Atomic Cycle Sequence, this determines the second command.
3	RW	0	**Sequence Prefix Opcode Pointer:** This field selects one of the two programmed prefix opcodes for use when performing an Atomic Cycle Sequence. A value of 0 points to the opcode in the least significant byte of the Offset 54h: PREOP – Prefix Opcode Configuration register. By making this programmable, the processor supports flash devices that have different opcodes for enabling writes to the data space vs. status register.
2	RW	1	**Atomic Cycle Sequence:** When set to 1 along with the SCGO assertion, the processor executes a sequence of commands on the SPI interface without allowing the other SPI master component to arbitrate and interleave cycles. The sequence is composed of: • Atomic Sequence Prefix Command (8-bit opcode only) • Primary Command specified by software (can include address and data) • Polling the Flash Status Register (opcode 05h) until bit 0 becomes 0b The SPI Cycle in Progress bit remains set and the Cycle Done Status bit in Offset 00h: SPIS – SPI Status register remains not set until the Busy bit in the Flash Status Register returns 0.
1	RWS	0	**SPI Cycle Go:** This bit always returns 0 on reads. However, a write to this register with a 1 in this bit starts the SPI cycle defined by the other bits of this register. The SPI Cycle in Progress (SCIP) bit in Offset 00h: SPIS – SPI Status register gets set by this action. Hardware must ignore writes to this bit while the SPI Cycle In Progress bit is set. Hardware allows other bits in this register to be programmed for the same transaction when writing this bit to 1. This saves an additional memory write.
0	RW	1	**SPI Access Request:** This bit is used by the software to request that the other SPI master stop initiating long transactions on the SPI bus. This bit defaults to a 1 and must be cleared by BIOS after completing the accesses for the boot process.

Table 3-255. SPI Address (SPIADDR)

SPIADDR
Base: RCBA **Offset: 3024h**

Bit	Attribute	Default	Definition
31:30	RW	0	**SPI Chip Select (CS) Control:** These two bits control which SPI Chip Select is used. Default 00 must always select SS0. Direct read mode always uses SS0. 00: SS0 01: SS1 10: Reserved 11: Reserved SS0 drive out SPI_CSB[0] signals for SPI chip select 0. SS1 drive out SPI_CSB[1] signals for SPI chip select 1.
29:24	RV	0	Reserved
23:0	RW	0	**SPI Cycle Address:** This field is shifted out as the SPI Address (MSB first).

Table 3-256. SPI Data 0 (SPID0)

SPID0
Base: RCBA **Offset: 3028h**

Bit	Attribute	Default	Definition
63:0	RW	0	**SPI Cycle Data 0 (SCD0):** This field is shifted out as the SPI Data on the Master-Out Slave-In Data pin (SPI_MOSI) during the data portion of the SPI cycle. This register also shifts in the data from the Master-In Slave-Out pin (SPI_MISO) into this register during the data portion of the SPI cycle. The data is always shifted starting with the least significant byte, MSB to LSB, followed by the next least significant byte, MSB to LSB, etc. Specifically, the shift order on SPI in terms of bits within this register is: 7-6-5-4-3-2-1-0-15-14-13- 8-23-22- 16-31...24-39...32...etc. Bit 56 is the last bit shifted out/in. There are no alignment assumptions; byte 0 always represents the value specified by the cycle address. ***Note:*** The data in this register may be modified by the hardware during any programmed SPI transaction. Direct Memory Reads do not modify the contents of this register.(This last requirement is needed in order to properly handle the collision case.) This register is initialized to 0 by the reset assertion. However, the least significant byte of this register is loaded with the first Status Register read of the Atomic Cycle Sequence that the hardware automatically runs out of reset. Therefore, bit 0 of this register can be read later to determine if the platform encountered the boundary case in which the SPI flash was busy with an internal instruction when the platform reset deasserted.

Table 3-257. SPI Data N (SPID[1-7])

SPID [1-7]
Base: RCBA **Offset: 3030h - 3060h by 8h**

Bit	Attribute	Default	Definition
63:0	RW	0	**SPI Cycle Data N (SCD[N]):** Similar definition as SPI Cycle Data. However, this register does not begin shifting until SPID[N-1] has completely shifted in/out.

Table 3-258. BIOS Base Address (BBAR)

BBAR
Base: RCBA **Offset: 3070h**

Bit	Attribute	Default	Definition
31:24	RV	0	Reserved
23:8	RWS	0	**Bottom of System Flash:** This field determines the bottom of the System BIOS. The processor does not run Programmed commands nor memory reads whose address field is less than this value. This field corresponds to bits 23:8 of the 3-byte address; bits 7:0 are assumed to be 00h for this vector when comparing to a potential SPI address. Software must always program 1s into the upper, (don't care) bits of this field based on the flash size. Hardware does not know the size of the flash array and relies upon the correct programming by software. The default value of 0000h results in all cycles allowed. ***Note:*** The SPI Host Controller prevents any Programmed cycle using the Address Register with an address less than the value in this register. Some flash devices specify that the Read ID command must have an address of 0000h or 0001h. If this command must be supported with these devices, it must be performed with the BBAR - BIOS Base Address programmed to 0h. Some of these devices have actually been observed to ignore the upper address bits of the Read ID command.
7:0	RV	0	Reserved

This register is not writable when the SPI Configuration Lock-Down bit in Offset 00h: SPIS – SPI Status register is set.

Table 3-259. Prefix Opcode Configuration (PREOP)

PREOP
Base: RCBA **Offset: 3074h**

Bit	Attribute	Default	Definition
15:08	RW	0h	**Prefix Opcode 1:** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.
7:0	RW	4h	**Prefix Opcode 2:** Software programs an SPI opcode into this field that is permitted to run as the first command in an atomic cycle sequence.

This register is not writable when the SPI Configuration Lock-Down bit in Offset 00h: SPIS – SPI Status register is set.

Table 3-260. Opcode Type Configuration (OPTYPE)

OPTYPE
Base: RCBA Offset: 3076h

Bit	Attribute	Default	Definition
15:14	RWS	0h	**Opcode Type 7:** See the description for bits 1:0.
13:12	RWS	0h	**Opcode Type 6:** See the description for bits 1:0.
11:10	RWS	0h	**Opcode Type 5:** See the description for bits 1:0.
9:8	RWS	0	**Opcode Type 4:** See the description for bits 1:0.
7:6	RWS	0	**Opcode Type 3:** See the description for bits 1:0.
5:4	RWS	0	**Opcode Type 2:** See the description for bits 1:0.
3:2	RWS	0	**Opcode Type 1:** See the description for bits 1:0.
1:0	RWS	0	**Opcode Type 0:** This field specifies information about the corresponding Opcode 0. This information allows the hardware to: 1. know whether to use the address field, and 2. provide BIOS protection capabilities. The hardware implementation also uses the read vs. write information for modifying the behavior of the SPI interface logic. The encoding of the two bits is: 00 = No Address associated with this Opcode and Read Cycle type 01 = No Address associated with this Opcode and Write Cycle type 10 = Address required; Read cycle type 11 = Address required; Write cycle type

This register is not writable when the SPI Configuration Lock-Down bit in Offset 00h: SPIS – SPI Status register is set. Entries in this register correspond to the entries in the Offset 58h: OPMENU – Opcode Menu Configuration register.

Note: The definition below only provides write protection for opcodes that have addresses associated with them. Therefore, any erase or write opcodes that do not use an address are avoided (for example, Chip Erase and Auto-Address Increment Byte Program).

Table 3-261. Opcode Menu Configuration (OPMENU)

OPMENU
Base: RCBA Offset: 3078h

Bit	Attribute	Default	Definition
63:56	RWS	0	**Allowable Opcode 7:** See the description for bits 7:0.
55:48	RWS	0	**Allowable Opcode 6:** See the description for bits 7:0.
47:40	RWS	0	**Allowable Opcode 5:** See the description for bits 7:0.
39:32	RWS	0	**Allowable Opcode 4:** See the description for bits 7:0.
31:24	RWS	0	**Allowable Opcode 3:** See the description for bits 7:0.
23:16	RWS	0	**Allowable Opcode 2:** See the description for bits 7:0.
15:8	RWS	0	**Allowable Opcode 1:** See the description for bits 7:0.
7:0	RWS	05h	**Allowable Opcode 0:** Software programs an SPI opcode into this field for use when initiating SPI commands through the Control Register.

This register is not writable when the SPI Configuration Lock-Down bit in Offset 00h: SPIS – SPI Status register is set. Eight entries are available in this register to give BIOS a sufficient set of commands for communicating with the flash device, while also restricting what malicious software can do. This keeps the hardware flexible enough to operate with a wide variety of SPI devices.

It is recommended that BIOS avoid programming Write Enable opcodes in this menu. Malicious software could then perform writes and erases to the SPI flash without using the atomic cycle mechanism. Write Enable opcodes are only programmed in the Offset 54h: PREOP – Prefix Opcode Configuration.

Table 3-262. Protected BIOS Range N (PBR[0-2])

PBR[0-2]
Base: RCBA **Offset: 3080h - 3088h by 4h**

Bit	Attribute	Default	Definition
31	RW-L	0	**Write Protection Enable:** When set, this bit indicates that the Base and Limit fields in this register are valid and that writes directed to addresses between them (inclusive) must be blocked by hardware. The base and limit fields are ignored when this bit is cleared.
30:24	RV	0	Reserved
23:12	RW-L	0	**Protected Range Limit:** This field corresponds to SPI address bits 23:12 and specifies the upper limit of the protected range. Address bits 11:0 are assumed to be FFFh for the limit comparison. Any address greater than the value programmed in this field is unaffected by this protected range.
11:0	RW-L	0	**Protected Range Base:** This field corresponds to SPI address bits 23:12 and specifies the lower base of the protected range. Address bits 11:0 are assumed to be 000h for the base comparison. Any address less than the value programmed in this field is unaffected by this protected range.

These registers can not be written when the SPI Configuration Lock-Down bit in Offset 00h: SPIS – SPI Status register is set to 1.

3.5.13 SMBus 1.0

The SMBus controller in the S12x0 is used by BIOS for DIMM SPD discovery in platforms with DIMM.

The S12x0 processor provides an SMBus 1.0-compliant host controller. The host controller provides a mechanism for the CPU to initiate communications with SMB peripherals (slaves).

3.5.13.1 I/O Registers

Table 3-263. I/O Registers

Start	End	Symbol	Register Name/Function
00	00	HCTL	Host Control
01	01	HSTS	Host Status
02	03	HCLK	Host Clock Divider
04	04	TSA	Transmit Slave Address
05	05	HCMD	Host Command
06	06	HD0	Host Data 0
07	07	HD1	Host Data 1
20	3F	HBD	Host Block Data

Table 3-264. Host Control Register (HCTL) (Sheet 1 of 2)

HCTL
I/O Base: SMBA **Offset: 00h**

Bit	Attribute	Default	Definition
07	RW	0	**SMI Enable (SE):** Enable generation of an SMI# upon completion of the command.
06	RV	0	Reserved
05	RW	0	**Alert Enable (AE):** Software sets this bit to enable an interrupt/SMI# due to SMBALERT#.

Table 3-264. Host Control Register (HCTL) (Sheet 2 of 2)

<table>
<tr><td colspan="4">HCTL
I/O Base: SMBA Offset: 00h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>04</td><td>RW</td><td>0</td><td>Start/Stop (ST): Initiates the command described in the CMD field. This bit always reads zero. HSTS.BSY identifies when ILB has finished the command.</td></tr>
<tr><td>03</td><td>RV</td><td>0</td><td>Reserved</td></tr>
<tr><td>02:00</td><td>RW</td><td>0</td><td>Command (CMD): Indicates the command ILB is to perform. If enabled, ILB generates an interrupt or SMI# when the command has completed If a command is issued, ILB sets HSTS.DE and perform no command, and does not operate until HSTS.DE is cleared.
<table>
<tr><th>Bits</th><th>Command Description</th></tr>
<tr><td>000</td><td>Quick: Uses TSA.</td></tr>
<tr><td>001</td><td>Byte: Uses TSA and CMD registers. TSA.R determines the direction.</td></tr>
<tr><td>010</td><td>Byte Data: Uses TSA, CMD, and HD0 registers. TSA.R determines the direction. If a read, HD0 contains the read data.</td></tr>
<tr><td>011</td><td>Word Data: Uses TSA, CMD, HD0 and HD1 registers. TSA.R determines the direction. If a read, HD0 and HD1 contain the read data.</td></tr>
<tr><td>100</td><td>Process Call: Uses TSA, HCMD, HD0 and HD1 registers. TSA.R determines the direction. Upon completion, HD0 and HD1 contain the read data.</td></tr>
<tr><td>101</td><td>Block: Uses TSA, CMD, HD0 and HBD registers. For writes, the count is stored in HD0 and indicates how many bytes of data is transferred. For reads, the count is received and stored in HD0. TSA.R determines the direction. For writes, data is retrieved from the first n (where n is equal to the specified count) addresses of HBD. For reads, the data is stored in HBD.</td></tr>
<tr><td>110-111</td><td>Reserved</td></tr>
</table></td></tr>
</table>

Table 3-265. Host Status Register (HSTS)

HSTS
I/O Base: SMBA **Offset: 01h**

Bit	Attribute	Default	Definition
07:04	RV	0	Reserved
03	RO	0	**Busy (BSY)**: When set, indicates the processor is running a command. No SMB registers are accessed while this bit is set.
02	RW1C	0	**Bus Error (BE)**: When set, indicates a transaction collision.
01	RW1C	0	**Device Error (DE)**: When set, this indicates one of the following: Illegal Command Field, an unclaimed cycle, or a time-out error.
00	RW1C	0	**Completion Status (CS):** When BSY is cleared, if this bit is set, the command completed successfully. If cleared, the command did not complete successfully.

Table 3-266. Host Clock Divider (HCLK)

HCLK
I/O Base: SMBA **Offset: 02h**

<table>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Definition</th></tr>
<tr><td>15:00</td><td>RW</td><td>0</td><td>Divider (DIV): This controls how many backbone clocks are counted for the generation of SMBCLK. Recommended values are listed below:
<table>
<tr><th rowspan="2">SM Bus Frequency</th><th colspan="2">Backbone Frequency</th></tr>
<tr><th>33 MHz</th><th>25 MHz</th></tr>
<tr><td>1 kHz</td><td>208Eh</td><td>106Ah</td></tr>
<tr><td>10 kHz</td><td>0342h</td><td>0271h</td></tr>
<tr><td>50 kHz</td><td>00A7h</td><td>007Dh</td></tr>
<tr><td>100 kHz</td><td>0054h</td><td>003Fh</td></tr>
<tr><td>400 kHz</td><td>0015h</td><td>0010h</td></tr>
<tr><td>1 MHz</td><td>0009h</td><td>0007h</td></tr>
</table>
</td></tr>
</table>

Table 3-267. Transmit Slave Address (TSA)

TSA
I/O Base: SMBA **Offset: 04h**

Bit	Attribute	Default	Definition
07:01	RW	0	**Address (AD):** 7-bit address of the targeted slave.
00	RW	0	**Read (R):** Direction of the host transfer. 1 = read, 0 = write

This register contains the address of the intended target.

3.5.13.2 Command Register (CMD)

This field is transmitted in the command field of the SMB protocol during the execution of any command.

3.5.13.3 HD0 - Data 0 (HD0)

This field is transmitted in the DATA0 field of an SM Bus cycle. For block writes, this register reflects the number of bytes to transfer. This register is programmed to a value between 1h (1 bytes) and 20h (32 bytes) for block counts. A count of 00h or above 20h results in no transfer and HSTS.CS is cleared, indicating a failure.

3.5.13.4 HD1 - Data 1 (HD1)

This field is transmitted in the DATA1 field of an SM Bus cycle.

Table 3-268. Host Data Block (HBD[0-3])

HBD[0-3]
I/O Base: SMBA **Offset: 20h - 38h by 8h**

Bit	Attribute	Default	Definition
63:00	RW	0	**Data (D):** This contains block data to be sent on a block write command, or received block data, on a block read command. Any data received over 32-bytes is lost.

3.5.14 GPIO

3.5.14.1 Core Well GPIO I/O Registers

The control for the general purpose I/O signals is handled through an independent 128-byte I/O space. The base offset for this space is selected by the GPIO_BAR register in D31:F0 config space.

Table 3-269. Core Well GPIO I/O Registers

Start	End	Name
00	03	CGEN – Core Well GPIO Enable
04	07	CGIO – Core Well GPIO Input / Output Select
08	0B	CGLV – Core Well GPIO Level for Input or Output
0C	0F	CGTPE – Core Well GPIO Trigger Positive Edge Enable
10	13	CGTNE – Core Well GPIO Trigger Negative Edge Enable
14	17	CGGPE – Core Well GPIO GPE Enable
18	1B	CGSMI – Core Well GPIO SMI Enable
1C	1F	CGTS – Core Well GPIO Trigger Status
40	43	CNMIEN - Core Well NMI Enable

If a bit is allocated for a GPIO that does not exist, unless otherwise indicated, the bit is always read as 0 and values written to that bit have no effect.

All core well bits are reset by the standard conditions that assert RESETB, and all suspend well bits are reset by the standard conditions that clear internal suspend registers.

Table 3-270. Core Well GPIO Enable (CGEN)

CGEN
I/O Base: GBA Offset: 00h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	1F_FFFF h	**Enable (EN):** Used to enable GPIO pins. 0: Disable 1: Enable

Table 3-271. Core Well GPIO Input/Output Select (CGIO)

CGIO
I/O Base: GBA Offset: 04h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	1F_FFFF h	**Input/Output (IO):** When set, the GPIO signal (if enabled) is programmed as an input. When cleared, the GPIO signal is programmed as an output. If the pin is muxed, and not enabled, writes to these bits have no affect.

Table 3-272. Core Well GPIO Level for Input or Output (CGLVL)

CGLVL
I/O Base: GBA Offset: 08h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	0	**Level (LVL):** If the GPIO is programmed to be an output (CGIO.IO[n] cleared), then this bit is used by software to drive a value on the pin. 1 = high, 0 = low. If the GPIO is programmed as an input, then this bit reflects the state of the input signal (1 = high, 0 = low.) and writes have no affect. The value of this bit has no meaning if the GPIO is disabled (CGEN.EN[n] = 0).

Table 3-273. Core Well GPIO Trigger Positive Edge Enable (CGTPE)

CGTPE
I/O Base: GBA Offset: 0Ch

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	0	**Trigger Enable (TE):** When set, the corresponding GPIO, if enabled as input via CGIO.IO[n], does case an SMI#/SCI when a 0 to 1 transition occurs. When cleared, the GPIO is not enabled to trigger an SMI#/SCI on a 0 to 1 transition. This bit has no meaning if CGIO.IO[n] is cleared (i.e., programmed for output)

Table 3-274. Core Well GPIO Trigger Negative Edge Enable (CGTNE)

CGTNE
I/O Base: GBA Offset: 10h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	0	**Trigger Enable (TE):** When set, the corresponding GPIO, if enabled as input via CGIO.IO[n], does case an SMI#/SCI when a 1 to 0 transition occurs. When cleared, the GPIO is not enabled to trigger an SMI#/SCI on a 1 to 0 transition. This bit has no meaning if CGIO.IO[n] is cleared (i.e., programmed for output)

Table 3-275. Core Well GPIO GPE Enable (CGGPE)

CGGPE
I/O Base: GBA Offset: 14h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	00	**Enable (EN):** When bit n is set and when CGTS.TS[n] is set, the bit 14 of GPE0 Status register of GPE0 Block is set.

Table 3-276. Core Well GPIO SMI Enable (CGSMI)

CGSMI
I/O Base: GBA Offset: 18h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW	00	**Enable (EN):** When bit n is set and when CGTS.TS[n] is set, the bit 9 of SMI Status register of GPE0 Block is set.

Table 3-277. Core Well GPIO Trigger Status (CGTS)

CGTS
I/O Base: GBA Offset: 1Ch

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW1C	0	**Trigger Status (TS)**: When set, the corresponding GPIO, if enabled as input via CGIO.IO[n], triggered an SMI#/SCI. This is set if a 0 to 1 transition occurred and CGTPE.TE[n] was set, or a 1 to 0 transition occurred and CGTNE.TE[n] was set. If both CGTPE.TE[n] and CGTNE.TE[n] are set, then this bit is set on both a 0 to 1 and a 1 to 0 transition. This bit is not set if the GPIO is configured as an output.

Table 3-278. Core Well NMI Enable (CNMIEN)

CNMIEN
I/O Base: GBA Offset: 40h

Bit	Attribute	Default	Definition
31:21	RV	0	Reserved
20:00	RW1C	0h	**CNMIEN:** Enables Core well GPIO's to generate NMI.

3.5.14.2 Resume Well GPIO I/O Registers

Table 3-279. Resume Well GPIO I/O Registers

Start	End	Name
20	23	RGEN – Resume Well GPIO Enable
24	27	RGIO – Resume Well GPIO Input / Output Select
28	2B	RGLV – Resume Well GPIO Level for Input or Output
2C	2F	RGTPE – Resume Well GPIO Trigger Positive Edge Enable
30	33	RGTNE – Resume Well GPIO Trigger Negative Edge Enable
34	37	RGGPE – Resume Well GPIO GPE Enable
38	3B	RGSMI – Resume Well GPIO SMI Enable
3C	3F	RGTS – Resume Well GPIO Trigger Status
44	47	RNMIEN - Resume Well NMI Enable

The control for the general purpose I/O signals is handled through an independent 64-byte I/O space. The base offset for this space is selected by the GPIO_BAR register in D31:F0 config space.

The format of these registers is the same as their core well counter parts. These registers reside in the resume well, and this is the difference.

Table 3-280. Resume Well GPIO Enable (RGEN)

RGEN
I/O Base: GBA Offset: 20h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	1FFh	**Enable (EN):** Used to enable GPIO pins. 0 = Disable 1 = Enable

Table 3-281. Resume Well GPIO Input/Output Select (RGIO)

RGIO
I/O Base: GBA Offset: 24h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	1FFh	**Input/Output (IO):** When set, the GPIO signal (if enabled) is programmed as an input. When cleared, the GPIO signal is programmed as an output. If the pin is muxed, and not enabled, writes to these bits have no affect.

Table 3-282. Resume Well GPIO Level for Input or Output (RGLVL)

RGLVL
I/O Base: GBA Offset: 28h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	0	**Level (LVL):** If the GPIO is programmed to be an output (RGIO.IO[n] cleared), then this bit is used by software to drive a value on the pin. 1 = high, 0 = low. If the GPIO is programmed as an input, then this bit reflects the state of the input signal (1 = high, 0 = low.) and writes have no affect. The value of this bit has no meaning if the GPIO is disabled (RGEN.EN[n] = 0).

Table 3-283. Resume Well GPIO Trigger Positive Edge Enable (RGTPE)

RGTPE
I/O Base: GBA Offset: 2Ch

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	0	**Trigger Enable (TE):** When set, the corresponding GPIO, if enabled as input via RGIO.IO[n], does case an SMI#/SCI when a 0 to 1 transition occurs. When cleared, the GPIO is not enabled to trigger an SMI#/SCI on a 0 to 1 transition. This bit has no meaning if RGIO.IO[n] is cleared (i.e., programmed for output).

Table 3-284. Resume Well GPIO Trigger Negative Edge Enable (RGTNE)

RGTNE
I/O Base: GBA Offset: 30h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	0	**Trigger Enable (TE):** When set, the corresponding GPIO, if enabled as input via RGIO.IO[n], does case an SMI#/SCI when a 1 to 0 transition occurs. When cleared, the GPIO is not enabled to trigger an SMI#/SCI on a 1 to 0 transition. This bit has no meaning if RGIO.IO[n] is cleared (i.e., programmed for output).

Table 3-285. Resume Well GPIO GPE Enable (RGGPE)

RGGPE
I/O Base: GBA Offset: 34h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	00	**Enable (EN):** When bit n is set and when RGTS.TS[n] is set, the bit 14 of GPE0 Status register of GPE0 Block is set.

Table 3-286. Resume Well GPIO SMI Enable (RGSMI)

RGSMI
I/O Base: GBA Offset: 38h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW	00	**Enable (EN):** When bit n is set and when RGTS.TS[n] is set, the bit 9 of SMI Status register of GPE0 Block is set.

Table 3-287. Resume Well GPIO Trigger Status (RGTS)

RGTS
I/O Base: GBA Offset: 3Ch

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW1C	0	**Trigger Status (TS):** When set, the corresponding GPIO, if enabled as input via RGIO.IO[n], triggered an SMI#/SCI. This is set if a 0 to 1 transition occurred and RGTPE.TE[n] was set, or a 1 to 0 transition occurred and RGTNE.TE[n] was set. If both RGTPE.TE[n] and RGTNE.TE[n] are set, then this bit is set on both a 0 to 1 and a 1 to 0 transition. This bit is not set if the GPIO is configured as an output.

Table 3-288. Resume Well NMI Enable (RNMIEN)

RNMIEN
I/O Base: GBA Offset: 44h

Bit	Attribute	Default	Definition
31:9	RV	0	Reserved
8:0	RW1C	0h	**RNMIEN:** Enables Resume Well GPIO's to generate NMI.

3.5.15 Watch Dog Timer

This Watchdog timer provides a resolution that ranges from 1us to ~16 minutes. The timer uses a 35-bit down-counter.

The counter is loaded with the value from the 1st Preload register. The timer is then enabled and it starts counting down. The time at which the WDT first starts counting down is called the first stage. If the host fails to reload the WDT before the 35-bit down counter reaches zero, the WDT generates an internal interrupt within WDT.

After the internal interrupt is generated when the first stage has counted down to zero, the WDT loads the value from the 2nd Preload register into the WDT 35-bit Down-Counter and starts counting down. The WDT is now in the second stage. If the host still fails to reload the WDT before the second timeout, the WDT drives the output signal "owdtout" pin high and sets the timeout bit (WDT_TIMEOUT). This bit indicates that the System has become unstable. The output signal "owdtout" pin is held high until the system is Reset or the WDT times out again. The process of reloading the WDT involves the following sequence of writes:

- Write 80 to offset WDTBA + 0Ch
- Write 86 to offset WDTBA + 0Ch
- Write 1 to WDT_RELOAD in Reload Register.

The same process is used for setting the values in the preload registers. The only difference exists in step 3. Instead of writing a 1 to the WDT_RELOAD, write the desired preload value into the corresponding Preload register. This value is not loaded into the 35-bit down counter until the next time the WDT reenters the stage. For example, if Preload Value 2 is changed, it is not loaded into the 35-bit down counter until the next time the WDT enters the second stage.

Output signal "OWDTOUT" is used for WDT output (WDT_TIMEOUT).

Table 3-289. Watchdog Timer Register Details

Offset Start	Offset End	Register ID Description	Default Value
00	00	PVR10: Preload Value 1 Register 0	FFh
01	01	PVR11: Preload Value 1 Register 1	FFh
02	02	PVR12: Preload Value 1 Register 2	0Fh
04	04	PVR20: Preload Value 2 Register 0	FFh
05	05	PVR21: Preload Value 2 Register 1	FFh
06	06	PVR22: Preload Value 2 Register 2	0Fh
0C	0C	RR0: Reload Register 0	00h
0D	0D	RR1: Reload Register 1	00h
10	10	WDCR: Watch Dog Configuration Register	00h
14	14	DCR0: Down Counter Register 0	00h
15	15	DCR1: Down Counter Register 1	00h
16	16	DCR2: Down Counter Register 2	00h
18	18	WDTLR: Watch Dog Timer Lock Register	00h

All registers not mentioned are reserved.

Note: Base Address for the Watchdog Timer registers, listed in this section, is configurable.

Table 3-290. Preload Value 1 Register 0 (PV1R0)

PV1R0
I/O Base: WDTBA **Offset: 00h**

Bit	Attribute	Default	Definition
7:0	RW	FFh	**Preload_Value_1 [7:0]:** This register is used to hold the bits 0 through 7 of the preload value 1 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-291. Preload Value 1 Register 1 (PV1R1)

PV1R1
I/O Base: WDTBA **Offset: 01h**

Bit	Attribute	Default	Definition
7:0	RW	FFh	**Preload_Value_1 [15:8]:** This register is used to hold the bits 8 through 15 of the preload value 1 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-292. Preload Value 1 Register 2 (PV1R2)

PV1R2
I/O Base: WDTBA **Offset: 02h**

Bit	Attribute	Default	Definition
7:0	RW	Fh	**Preload_Value_1 [19:16]:** This register is used to hold the bits 16 through 19 of the preload value 1 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-293. Preload Value 2 Register 0 (PV2R0)

PV2R0
I/O Base: WDTBA **Offset: 04h**

Bit	Attribute	Default	Definition
7:0	RW	FFh	**Preload_Value_2 [7:0]:** This register is used to hold the bits 0 through 7 of the preload value 2 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-294. Preload Value 2 Register 1 (PV2R1)

PV2R1
I/O Base: WDTBA **Offset: 05h**

Bit	Attribute	Default	Definition
7:0	RW	FFh	**Preload_Value_2 [15:8]:** This register is used to hold the bits 8 through 15 of the preload value 2 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-295. Preload Value 2 Register 2 (PV2R2)

PV2R2
I/O Base: WDTBA **Offset: 06h**

Bit	Attribute	Default	Definition
7:0	RW	Fh	**Preload_Value_2 [19:16]:** This register is used to hold the bits 16 through 19 of the preload value 2 for the WDT Timer. The Value in the Preload Register is Automatically transferred into the 35-bit down counter every time the WDT enters the first stage. The value loaded into the preload register needs to be one less than the intended period. This is because the timer makes use of zero-based counting (i.e., zero is counted as part of the decrement).

Table 3-296. Reload Register 0 (RR0)

RR0
I/O Base: WDTBA **Offset: 0Ch**

Bit	Attribute	Default	Definition
7:0	WO	0h	**RR0_Write:**The reload sequence is only necessary for the Reload register and Preload_Value registers.

Table 3-297. Reload Register 1 (RR1)

RR1
I/O Base: WDTBA **Offset: 0Dh**

Bit	Attribute	Default	Definition
7:2	RV	0h	Reserved
1	RW1C	0h	**WDT_TIMEOUT:** This bit is located in the RTC Well and the value is not lost if the host resets the system. It is set to 1 if the host fails to reset the WDT before the 35-bit Down-Counter reaches zero for the second time in a row. This bit is cleared by performing the Register Unlocking Sequence followed by a 1 to this bit. 0 = Normal (Default). 1 = System has become unstable.
0	RW	0h	**WDT_RELOAD:** To prevent a timeout the host must perform the Register Unlocking Sequence followed by a 1 to this bit.

Table 3-298. WDT Configuration Register (WDTCR)

WDTCR
I/O Base: WDTBA **Offset: 10h**

Bit	Attribute	Default	Definition
7:6	RV	0h	Reserved
5	RW	0h	**WDT Timeout Output Enable:** This bit indicates whether or not the WDT toggles the OWDTOUT output pin if the WDT times out. 0 = Enabled (Default). 1 = Disabled.
4	RW	0h	**WDT Reset Enable:** When this bit is enable (set to 1), it allows internal reset to be trigger when WDT time-out in the second stage. It either trigger COLD or WARM reset depend on WDT_RESET_SEL (WDT Reset Select) bit. 0 = Disable internal reset (Default). 1 = Enable internal COLD or WARM reset.
3	RW	0h	**WDT Reset Select:** This determines which reset to be triggered when WDT_RESET_EN (WDT Reset Enable) is set. 0 = Cold Reset (Default). 1 = Warm Reset.
2	RW	0h	**WDT Prescaler Select:** The WDT provides two options for prescaling the main Down Counter. The preload values are loaded into the main down counter right justified. The prescaler adjusts the starting point of the 35-bit down counter. 0 = The 20-bit Preload Value is loaded into bits 34:15 of the main down counter. The resulting timer clock is the PCI Clock (33 MHz) divided by 2^{15}. The approximate clock generated is 1 kHz, (1 ms to ~16 min). (Default) 1 = The 20-bit Preload Value is loaded into bits 24:05 of the main down counter. The resulting timer clock is the PCI Clock (33 MHz) divided by 2^{5}. The approximate clock generated is 1 MHz, (1 µs to 1 sec).
1:0	RV	0	Reserved

Table 3-299. Down Counter Register 0 (DCR0)

DCR0
I/O Base: WDTBA **Offset: 14h**

Bit	Attribute	Default	Definition
7:0	RO	0h	Reserved

Table 3-300. Down Counter Register 1 (DCR1)

DCR1
I/O Base: WDTBA **Offset: 15h**

Bit	Attribute	Default	Definition
7:0	RO	0h	Reserved

Table 3-301. Down Counter Register 2 (DCR2)

DCR2
I/O Base: WDTBA **Offset: 16h**

Bit	Attribute	Default	Definition
7:0	RO	0h	Reserved

Table 3-302. WDT Lock Register (WDTLR)

WDTLR
I/O Base: WDTBA **Offset: 18h**

Bit	Attribute	Default	Definition
7:3	RV	0h	Reserved
2	RW	0h	**WDT Timeout Configuration:** This register is used to choose the functionality of the timer. 0 = Watchdog Timer Mode: When enabled (i.e., WDT_ENABLE goes from 0 to 1) the timer reloads Preload Value 1 and start decrementing. (Default) Upon reaching the second stage timeout the OWDTOUT pin is driven high once and does not change again until Power is cycled or a hard reset occurs. 1 = Reserved.
1	RW	0h	**Watchdog Timer Enable:** The following bit enables or disables the WDT. 0 = Disabled (Default). 1 = Enabled. ***Notes:*** This bit cannot be modified if WDT_LOCK (Watchdog Timer Lock) has been set. In WDT mode Preload Value 1 is reloaded every time WDT_ENABLE goes from 0 to 1 or the WDT_RELOAD bit is written using the proper sequence of writes (See Register Unlocking Sequence). When the WDT second stage time-out occurs, a reset must happen if programmed. Software must guarantee that a timeout is not about to occur before disabling the timer. A reload sequence is suggested.
0	RW-L	0h	**Watchdog Timer Lock:** Setting this bit locks the values of this register until a hard-reset occurs or power is cycled. 0 = Unlocked (Default). 1 = Locked. ***Note:*** Writing a 0 has no affect on this bit. Write is only allowed from 0 to 1 once. It cannot be changed until either power is cycled or a hard reset occurs.

3.5.16 CPU Interface I/O Registers

Table 3-303. NMI Status and Control Register (NSC)

NSC
I/O Address: 61h

Bit	Attribute	Default	Definition
7	RO	0h	**SERR# NMI Status:** Set on errors from a PCIe port or internal functions that generate SERR#. SNE in this register must be cleared in order for this bit to be set. To reset the interrupt, set bit 2 to 1 and then set it to 0.
6	RO	0h	**IOCHK NMI Status:** Set when SERIRQ asserts IOCHK# and INE in this register is cleared. To reset the interrupt, set bit 3 to 1 and then set it to 0.
5	RO	0h	**Timer Counter 2 Status:** Reflects the current state of the 8254 counter 2 output. Counter 2 must be programmed for this bit to have a determinate value.
4	RO	0h	**Refresh Cycle Toggle Status:** Reflects the current state of 8254 counter 1.
3	RW	0h	**IOCHK NMI Enable:** When set, IOCHK# NMIs are disabled. When cleared, IOCHK# NMIs re-enabled.
2	RW	0h	**SERR# NMI Enable:** When set, SERR# NMIs are disabled. When cleared, SERR# NMIs are enabled.
1	RW	0h	**Speaker Data Enable:** When this bit is a 0, the SPKR output is a 0. When this bit is a 1, the SPKR output is equivalent to the Counter 2 OUT signal value.
0	RW	0h	**Timer Counter 2 Enable:** When cleared, counter 2 counting is disabled. When set, counting is enabled.

Table 3-304. NMIE – NMI Enable (NMIE)

NMIE
I/O Address: 70h

Bit	Attribute	Default	Definition
7	WO	1h	**NMI Enable:** When set, NMI sources disabled. When cleared, NMI sources enabled.
6:0	WO	0h	**Real Time Clock Index:** Selects RTC register or CMOS RAM address to access.

Table 3-305. Reset Control Register (RSTC)

RSTC
I/O Address: CF9h

Bit	Attribute	Default	Definition
7	RW	0h	**BIOS Write Enable (BIOS_WE):** When BC.SMM_BWP = 1, RSTC.BIOS_WE must be set to a 1 to enable SPI Flash write or erasure cycle operations. When BC.SMM_BWP = 0, RSTC.BIOS_WE is not required to be set to a 1 to enable SPI controller write and erasure cycle requests.
6:5	RV	0h	Reserved
4	WO	0h	**INIT:** Writing a 1 to this bit, sends an upstream SetINIT message to P-unit.
3	RW	0h	**Cold Reset:** This bit causes SLPMODE, and RSTRDY# to be driven low, while SLPRDY# remains high. In response to this, the platform performs a full power cycle.
2	RV	0h	Reserved
1	RW	0h	**Warm Reset:** This bit causes RSTRDY# to be driven low, with SLPMODE high, while SLPRDY# remains high. In response to this, the platform pulses RESETB low to reset the CPU and all peripherals.
0	RV	0	Reserved

A write to this register with RSTC.COLD or RSTC.WARM set initiates a reset. Software must only write to one of these bits at a time, else the behavior is undefined.

These bits automatically clear once the reset occurs, so there is no need for software to clear them.

3.5.16.1 Software SMI Control Port (SWSMICTL: IO address B2h)

This port is used to pass a command between the OS and the SMI handler. Writes to this port store data, set APM bit of SMI Status register of GPE0 Block, and generate SMI# when APM is set.

3.5.16.2 Software SMI Status Port (SWSMISTS: IO address B3h)

This port is used to pass data between the OS and the SMI handler. This is a scratchpad register.

3.5.17 Interrupt Queue Agents

Table 3-306. Centerton Implementation of Interrupt Queue Agents

Interrupt Agent Number	Device
27	P-Unit
26	GPIO to Sideband
25	JTAG to Sideband
24	Reserved
23	Root Fabric (RTF)
22	Reserved
21	Reserved
20	Reserved
19	Reserved
18	PCIe RP 1
17	PCIe RP 2
16	PCIe RP 3
15	PCIe RP 4
14	Reserved
13	Reserved
12	Reserved
11	Reserved
10	Reserved
9	Reserved
8	Reserved
7	Reserved
6	Reserved
5	Reserved
4	RTF-attached SMBus Controller 0
3	RTF-attached SMBus Controller 1
2	Reserved
1	Reserved
0	UART

Table 3-307. Interrupt Queue Agent (IRQAgent[0-27])

IRQAgent **Base: RCBA**			**Offset: 3140h-3176h by 2h**
Bit	**Attr**	**Default**	**Description**
15:12	RW	0h	**InterruptD Pin Route(INTD_PR):** Indicates which routing used for INTD# of device IRQAGENT. Legal values are [0x0-0x7] corresponding to PIRQ[A-H]. For example, INTD from IRQAGENT will be routed to PIRQG if this field is set to 0x6.
11:8	RW	0h	**InterruptC Pin Route(INTC_PR):** Indicates which routing used for INTC# of device IRQAGENT. Legal values are [0x0-0x7] corresponding to PIRQ[A-H]. For example, INTC from IRQAGENT will be routed to PIRQG if this field is set to 0x6.
7:4	RW	0h	**InterruptB Pin Route(INTB_PR):** Indicates which routing used for INTB# of device IRQAGENT. Legal values are [0x0-0x7] corresponding to PIRQ[A-H]. For example, INTA from IRQAGENT will be routed to PIRQG if this field is set to 0x6.
3:0	RW	0h	**InterruptA Pin Route(INTA_PR):** Indicates which routing used for INTA# of device IRQAGENT. Legal values are [0x0-0x7] corresponding to PIRQ[A-H]. For example, INTA from IRQAGENT will be routed to PIRQG if this field is set to 0x6.

3.6 High Speed UART Controller

Table 3-308. Register Summary

Offset (h)	Size (bits)	Name
00	32	"Identifiers (ID)" on page 198
04	16	"Command (CMD)" on page 199
06	16	"Status (STS)" on page 199
08	32	"Class Codes (CC)" on page 200
0E	8	"Header Type (HTYPE)" on page 200
10	32	"I/O Base Address (BAR0)" on page 200
14	32	"Base Lower Address (BAR1)" on page 200
2C	32	"Subsystem IDs (SSID)" on page 201
34	8	"Capabilities Pointer (CAP_PTR)" on page 201
3C	16	"Interrupts (INT)" on page 201
40	32	"MSI (MSI)" on page 201
44	32	"MSI Message Address (MSIMA)" on page 202
48	16	"MSI Message Data (MSIMD)" on page 202
50	32	"PM Capability (PMC)" on page 202
54	32	"PM Control and Status (PMCS)" on page 203
60	32	"Device Specific Control and Status (DSCSTS)" on page 204
0000	32	"Receive Buffer Register (RBR)" on page 206
0000	32	"Transmit Holding Register (THR)" on page 206
0000	32	"DLAB Low Register (DLL)" on page 207
0004	32	"DLAB High Register (DLH)" on page 207
0004	32	"Interrupt-Enable Register (IER)" on page 208
0008	32	"Interrupt-Identification Register (IIR)" on page 209
0008	32	"FIFO Control Register (FCR)" on page 210
0020	32	"FOR—Receive FIFO Occupancy Register (FOR)" on page 210
000C	32	"LCR—Line-Control Register (LCR)" on page 211
0024	32	"Auto-Baud Control Register (ABR)" on page 211
0014	32	"Line-Status Register (LSR)" on page 212
0010	32	"Modem-Control Register (MCR)" on page 213
0018	32	"Modem Status Register (MSR)" on page 214
001C	32	"SPR—Scratchpad Register (SPR)" on page 214
0028	32	"Auto-Baud Count Register (ACR)" on page 214
0030	32	"Pre-Scalar Register (PSR)" on page 215
0034	32	"DDS Multiplier Register (DDSMR)" on page 215
0038	32	"DDS Divisor Register (DDSDR)" on page 216
003C	32	"SIR Control Register (SCR)" on page 216
003C	32	"Status Register (SSR)" on page 216

3.6.1 High Speed UART Controller Registers

3.6.1.1 PCI Configuration Space

Table 3-309. PCI Register Maps

Start	End	Symbol	Full Name
00	03	ID	Identifiers
04	05	CMD	Command Register
06	07	STS	Device Status
08	0B	CC	Class Codes
0E	0E	HTYPE	Header Type
0F	0F	BIST	Built-in Self Test
10	17	BAR	Base Address (Memory)
2C	2D	SVID	Subsystem Vendor Identifier
2E	2F	SID	Subsystem Identifier
34	34	CAP_PTR	Capabilities Pointer
3C	3C	Int	Interrupts
3D	3D	INTPN	Interrupt Pin

Table 3-310. Identifiers (ID)

ID
Bus: 0 **Device: 20** **Function: 0** **Offset: 00h**

Bit	Type	Default	Description
31:16	RO-V	0000h	**Device ID (DID):** Identifier assigned to the device.
15:00	RO	8086h	**Vendor ID (VID):** This 16-bit field identifies Intel as the manufacturer of the device.

Table 3-311. Command (CMD)

CMD
Bus: 0 **Device: 20** **Function: 0** **Offset: 04h**

Bit	Attribute	Default	Description
15:11	RO	0h	Reserved
10	RW	0h	**Interrupt Disable (ID):** Enables the device to assert an interrupt. When set, the UART asserts INTA messages.
9	RO	0h	Reserved
8	RW	0h	**SEN (SERR Enable):** Setting this bit enables the generation of System Error message, when required through sideband interface. Error message sent by UART device are always Non-Fatal.
7:3	RO	0h	Reserved
2	RW	0h	**BME (Bus Master Enable):** When set enables the ability to issue Memory or IO requests, including MSI.
1	RW	0h	**Memory Space Enable (MSE):** When set, enables memory space accesses to the UART controller.
0	RW	0h	**IOS (I/O Space):** When set, IO space Decoding is enabled and IO transactions targeting the device are accepted.

Table 3-312. Status (STS)

STS
Bus: 0 **Device: 20** **Function: 0** **Offset: 06h**

Bit	Attribute	Default	Description
15	RO	0h	Reserved
14	RW	0h	**Signal System Error (SSE):** This bit is set when the device has detected an un-correctable error and reported it via SERR message over sideband. This requires SERR Enable bit to be set in Command register.
13	RW	0h	**Received Master Abort (RMA):** This bit is set when device receives a Completion transaction with “Unsupported Request” completion status. No error will be reported.
12	RW	0h	**Received Target Abort (RTA):** This bit is set when device receives a Completion transaction with “Completer Abort” completion status. No error will be reported
11	RW	0h	**Signaled Target Abort (STA):** Set by the device when aborting a request that violates the device programming model. When SERR Enable is set SERR message will be send over sideband.
10:5	RO	0h	Reserved
4	RO	1h	**Capabilities List Exists (CLIST):** Indicates the controller contains a capabilities pointer list and the capability pointer register is implemented at offset 0x40 in the configuration space.
3	RO	0h	**Interrupt Status (IS):** Reflects the state of the interrupt pin at the input of the enable/disable circuit. when the interrupt is asserted, and cleared when the interrupt is cleared (independent of the state of Interrupt Disable bit in command register. This bit is only associated with the INTx messages and has no meaning if the device is using MSI
2:0	RO	0h	Reserved

Table 3-313. Class Codes (CC)

CC
Bus: 0 **Device: 20** **Function: 0** **Offset: 08h**

Bit	Attribute	Default	Description
31:24	RO	0Ch	**Base Class Code (BCC):** This register indicates that the function implements a Serial Bus Controller device.
23:16	RO	03h	**Sub Class Code (SCC):** This indicates the device is an UART.
15:8	RO	80h	**Programming Interface (PI):** Universal Serial Bus with no specific programming interface.
7:0	RO	00h	**Revision ID (RID):** Indicates the device specific revision identifier derived from strap.

Table 3-314. Header Type (HTYPE)

HTYPE
Bus: 0 **Device: 20** **Function: 0** **Offset: 0Eh**

Bit	Attribute	Default	Description
7:0	RO	00h	**Header Type (HTYPE):** Implements a Type 0 Configuration header.

Table 3-315. I/O Base Address (BAR0)

BAR0
Bus: 0 **Device: 20** **Function: 0** **Offset: 10h**

Bit	Attribute	Default	Description
31:3	RW	00h	**Base Address:** I/O decoder base address.
2:1	RO	0h	Hardwired to 0. Indicates 8bytes are requested.
0	RO	1h	**Space Type (SPTY):** Value of 1 indicates the BAR is located in I/O space.

Table 3-316. Base Lower Address (BAR1)

BAR1
Bus: 0 **Device: 20** **Function: 0** **Offset: 14h**

Bit	Attribute	Default	Description
31:8	RW	0h	**Lower Address (LA):** Base address for the UART memory mapped configuration registers. 256 bytes are requested by hardwiring bits 7:4 to 0s.
7:4	RO	0h	Hardwired to 0s. To request the 256-bytes of memory space.
3	RO	0h	**Prefetchable (PREF):** Indicates that this BAR is NOT pre-fetchable.
2:1	RO	0h	**Address Range (ADDRNG):** Indicates that this BAR can be located anywhere in lower 32 bit address space.
0	RO	0h	**Space Type (SPTYP):** Indicates that this BAR is located in memory space.

Table 3-317. Subsystem IDs (SSID)

SSID
Bus: 0 **Device: 20** **Function: 0** **Offset: 2Ch**

Bit	Attribute	Default	Description
31:16	RW	0000h	**Subsystem ID (SSID):** These RW bits have no hardware functionality.
15:0	RW	8086h	**Subsystem Vendor ID (SVID):** These RW bits have no hardware functionality.

Table 3-318. Capabilities Pointer (CAP_PTR)

CAP_PTR
Bus: 0 **Device: 20** **Function: 0** **Offset: 34h**

Bit	Attribute	Default	Description
7:0	RO	00h	**Capability Pointer (CP).** Set to 0 indicates no capability list exists.

Table 3-319. Interrupts (INT)

INT
Bus: 0 **Device: 20** **Function: 0** **Offset: 3Ch**

Bit	Attribute	Default	Description
15:8	RO	01h	**Interrupt Pin (INTP):** Indicates the functions interrupt pin is bonded to INTA.
7:0	RW	00h	**Interrupt Line (LINE):** Hardware does not use this field. It is used to communicate to software about the connection of interrupt pin and the interrupt line.

Table 3-320. MSI (MSI)

MSI
Bus: 0 **Device: 20** **Function: 0** **Offset: 40h**

Bit	Attribute	Default	Description
31:24	RO	00000	Reserved
23	RO	0	**64-bit Address Capable (AC64B):** Value of 0 indicates the function does not implement the upper 32-bits of the message address register and is incapable of generating a 64-bit memory address.
22:20	RW	0h	**Multiple Message Enable (MME):** Indicates the number of messages allocated to the device.
19:17	RO	0h	**Multiple Message Capable (MMC):** Value of 0 indicates the device only support single interrupt message.
16	RW	0h	**MSI Enable (MSIE):** If set, MSI is enabled and the legacy interrupts message is not generated.
15:8	RO	50h	**MSI Next Capability Pointer (MSINCP):** Hardwired to 50h to point to the location of power management capability register set.
7:0	RO	05h	**MSI Capability ID (MSICID):** A value of 05h indicates the presence of MSI capability register set.

Table 3-321. MSI Message Address (MSIMA)

MSIMA **Bus: 0** **Device: 20** **Function: 0** **Offset: 44h**			
Bit	**Attribute**	**Default**	**Description**
31:2	RW	00h	**MSI Message Address (MSIMA):** Lower 32-bits of system software assigned message address to the device.
1:0	RO	0h	Set to a value of 0 indicates the memory address is always DW aligned.

Table 3-322. MSI Message Data (MSIMD)

MSIMD **Bus: 0** **Device: 20** **Function: 0** **Offset: 48h**			
Bit	**Attribute**	**Default**	**Description**
15:0	RW	00h	**MSI Message Data (MSIMD):** A 16-bit message data pattern assigned by the system software to the device. When MSI is generated the actual data is 32-bit and the upper 16 bits are always 0.

Table 3-323. PM Capability (PMC)

PMC **Bus: 0** **Device: 20** **Function: 0** **Offset: 50h**			
Bit	**Attribute**	**Default**	**Description**
31:27	RO	00h	**PME Support:** The value of 0 indicates the function is not capable of generating PME messages from any of the PM states.
26	RO	0h	**D2 Support:** The value of 0 indicates the function does not support D2 PM states.
25	RO	0h	**D1 Support:** The value of 0 indicates the function does not support D2 PM states.
24:22	RO	0h	**Aux Current:** Reserved
21	RO	0h	**Device Specific Initialization (DSI):** The value of 0 indicates no device specific initialization is required.
20	RO	0h	Reserved
19	RO	0h	**PME Clock (PMEC):** Does not apply. Hardwired to 0.
18:16	RO	3h	**Version (VS):** Indicates support for Revision 1.2 of the PCI Power Management Specifications.
15:8	RO	00h	**PM Next Capability Pointer (PMNCP):** Value of 0 indicates there are no further capabilities i.e., the capability linked list is ended.
7:0	RO	01h	**PM Capability ID (PMCID):** Value of 01h indicates the device implements PM capability register set.

Table 3-324. PM Control and Status (PMCS)

PMCS
Bus: 0 **Device: 20** **Function: 0** **Offset: 54h**

Bit	Attribute	Default	Description
31:24	RO	00h	**Data:** No data.
23	RO	0h	**Bus Power Clock Control Enable (BPCCE):** Does not apply. Hardwired to 0.
22	RO	0h	**B2/B3 Support (B23):** Does not apply. Hardwired to 0.
21:16	RV	0h	Reserved
15	RO	0h	**PME Status (PMES):** Reserved
14:9	RV	0h	Reserved
8	RO	0h	**PME Enable (PMEE):** Hardwired to 0 as function does not support PME.
7:4	RV	0h	Reserved
3	RO	1h	**No Soft Reset:** These bits are used to indicate whether devices transitioning from D3HOT state to D0 state perform an internal reset. 0 = Device transitioning from D3HOT state to D0 state perform an internal reset. 1 = Device transitioning from D3HOT state to D0 state do not perform an internal reset. Configuration content is preserved. Upon transition from the D3HOT state to D0 state initialized state, no additional operating system intervention is required to preserve configuration context beyond writing to the PowerState bits. Regardless of this bit, the controller transition from D3HOT state to D0 state by a system or bus segment reset returns to the state D0 un-initialized with only PME context preserved if PME is supported and enabled.
2	RV	0h	Reserved
1:0	RW	0h	**Power State (PS):** This field is used both to determine the current power state of the UART and set a new power state. The values are: 00: D0 state 11: D3hot state If software attempts to write a value of 10b or 01b in to this field, the write operation must complete normally; however, the data is discarded and no state change occurs. When in D3hot, the UART configuration space is available, but the i/O and memory spaces are not. Additionally, interrupts are blocked.

Table 3-325. Device Specific Control and Status (DSCSTS)

DSCSTS
Bus: 0 **Device: 20** **Function: 0** **Offset: 60h**

Bit	Attribute	Default	Description
31:20	RV	00h	Reserved
19	RW1C	0h	**Unsupported Request Detect (URD):** This bit is set when an unsupported request is detected.
18:16	RV	0h	Reserved
15:4	RV	0h	Reserved
3	RW	0h	**Unsupported Request Reporting Enable (URRE):** When set, this bit enables the reporting of Non-Fatal error.
2:0	RV	0h	Reserved

3.6.1.2 UART Memory-Mapped Registers

The table below shows the mapping of registers to memory-mapped addresses.

Table 3-326. UART Memory-Mapped Registers

Address Space Register Offset	Block Name	DLAB Bit Value	Symbol	Description	Access
0000	UART0	0	U0_RBR	Receive Buffer Register	RO
0000		0	U0_THR	Transmit Holding Register	WO
0004		0	U0_IER	Interrupt Enable Register	RW
0008		X	U0_IIR	Interrupt ID Register	RO
0008		X	U0_FCR	FIFO Control Register	WO
000C		X	U0_LCR	Line Control Register	RW
0010		X	U0_MCR	Modem Control Register	RW
0014		X	U0_LSR	Line Status Register	RO
0018		X	U0_MSR	Modem Status Register	RO
001C		X	U0_SPR	Scratch Pad Register	RW
0000		1	U0_DLL	Divisor Latch Reg. Low Byte	RW
0004		1	U0_DLH	Divisor Latch Reg. High Byte	RW
0020		X	U0_FOR	FIFO Occupancy Register	RO
0024		X	U0_ABR	Autobaud Control Register	RW
0028		X	U0_ACR	Autobaud Count Reg.	RO
0030		X	U0_PS	Pre-Scalar	RW
0034		X	U0_MUL	DDS Multiplier	RW
0038		X	U0_DIV	DDS Divisor	RW
003C		X	U0_SIRCR	SIR Control Register	RW
0040		X	U0_SIRSR	SIR Status Register	RO

3.6.1.3 Receive/Transmit Registers

Table 3-327. Receive Buffer Register (RBR)

RBR
Base: BAR **Offset: 0000h**

Bits	Type	Reset	Description
7:0	RO	0	Received Data Byte

Table 3-328. Transmit Holding Register (THR)

THR
Base: BAR **Offset: 0000h**

Bits	Type	Reset	Description
7:0	WO	0	Transmit Data Byte

3.6.1.4 Divisor Latch Registers

Table 3-329. DLAB Low Register (DLL)

DLL
Base: BAR **Offset: 0000h**

Bits	Symbol	Default	Access	Description
7:0	DLL	02h	RV	DLAB bits [7:0] for baud rate selection.

Table 3-330. DLAB High Register (DLH)

DLH
Base: BAR **Offset: 0001h**

Bits	Symbol	Default	Access	Description
7:0	DLH	00h	RV	DLAB bits [15:8] for baud rate selection.

Table 3-331. Interrupt-Enable Register (IER)

IER
Base: BAR **Offset: 0001h**

Bits	Symbol	Default	Access	Description
7:4	RV	0b	RO	**Reserved.**
3	MIE	0b	RW	**Modem Interrupt Enable:** (Source IIR[IID]) 0 = Modem Status Interrupt disabled. 1 = Modem Status Interrupt enabled.
2	RLSE	0b	RW	**Receiver Line Status Interrupt Enable:** (Source IIR[IID]) 0 = Receiver Line Status Interrupt disabled. 1 = Receiver Line Status Interrupt enabled.
1	TIE	0b	RW	**Transmit Data Request Interrupt Enable:** (Source IIR[IID]) 0 = Transmit FIFO Data Request Interrupt disabled. 1 = Transmit FIFO Data Request Interrupt enabled.
0	RAVIE	0b	RW	**Receiver Data Available Interrupt Enable:** (Source IIR[IID]) 0 = Receiver Data Available (Trigger level reached) Interrupt disabled. 1 = Receiver Data Available (Trigger level reached) Interrupt enabled.

Table 3-332. Interrupt-Identification Register (IIR)

IIR
Base: BAR **Offset: 0002h**

Bits	Symbol	Default	Access	Description
7:6	FIFOES[1:0]	00b	RO	**FIFO Mode Enable Status:** 00: Non-FIFO mode is selected 01: Reserved 10: Reserved 11: FIFO mode is selected (TRFIFOE = 1)
5	RV	0	RO	**Reserved**
4	ABL	0b	RO	**Autobaud Lock:** 0 = Autobaud circuitry has not programmed Divisor Latch registers (DLR). 1 = Divisor Latch registers (DLR) programmed by auto-baud circuitry.
3	TOD	0b	RO	**Time Out Detected:** 0 = No time out Interrupt is pending. 1 = Time out Interrupt is pending. (FIFO mode only)
2:1	IID[1:0]	0b	RO	**Interrupt Source Encoded:** 00: Modem Status (CTS, DSR, RI, DCD modem signals changed state) 01: Transmit FIFO requests data 10: Received Data Available 11: Receive error (overrun, parity, framing, break, FIFO error
0	nIP	1b	RO	Interrupt Pending: 0 = Interrupt is pending. (Active low) 1 = No Interrupt is pending.

Table 3-333. FIFO Control Register (FCR)

FCR
Base: BAR **Offset: 0002h**

Bits	Symbol	Default	Access	Description
7:6	ITL	00b	WO	**Interrupt Threshold Level** 00: 1 byte or more in Receive FIFO causes Interrupt 01: 8 bytes or more in Receive FIFO causes Interrupt and DMA request 10: 16 bytes or more in Receive FIFO causes Interrupt and DMA request 11: 32 bytes or more in Receive FIFO causes Interrupt and DMA request
5	Reserved	0b	WO	**FIFO Size (FS):** FS selects the size of the FIFO. 0: 16 bytes 1: 64 bytes
4	Reserved	0b	WO	Trailing Bytes are always removed by the Processor.
3	TIL	0b	WO	**DMA Signaling Mode:** Not used as per 16550 specifications.
2	RESETTF	0b	WO	**Reset Transmitter FIFO** 0 = No affect. 1 = Transmitter FIFO is cleared. After clearing, this bit is automatically reset to 0. ***Note:*** Software checks that the LSR[TEMT] bit is set, to ensure that the Transmit Shift Register, Transmit Holding Register, and Transmit FIFO are all empty, before setting the RESETTF bit. If the RESETTF bit is set and the LSR[TEMT] bit is not set, then the results are undefined.
1	RESETRF	0b	WO	**Reset Receiver FIFO** 0 = No affect. 1 = Receiver FIFO is cleared. After clearing this bit is automatically reset to 0.
0	TRIFIFOE	0b	WO	**Transmit and Receive FIFO Enable** 0 = FIFOs are disabled. 1 = FIFOs are enabled.

Table 3-334. FOR—Receive FIFO Occupancy Register (FOR)

FOR
Base: BAR **Offset: 0020h**

Bits	Symbol	Default	Access	Description
31:7	Reserved	000000h	RV	
6:0		0	RO	**Byte Count:** Number of bytes (0-64) remaining in the Receiver FIFO.

Table 3-335. LCR—Line-Control Register (LCR)

LCR
Base: BAR **Offset: 0003h**

Bits	Symbol	Default	Access	Description
7	DLAB	0b	RW	0 = Access Transmit Holding Register (THR), Receive Buffer Register (RBR) and Interrupt Enable Register. 1 = Access Divisor Latch Registers (DLL and DLH).
6	SB	0b	RW	0 = No affect on TXD output. 1 = Forces TXD output to 0 (space).
5	STKYP	0b	RW	0 = No affect on parity bit. 1 = Forces parity bit to be opposite of EPS bit value.
4	EPS	0b	RW	0 = Sends and checks for odd parity. 1 = Sends and checks for even parity.
3	PEN	0b	RW	0 = No parity function. 1 = Allows parity generation and checking.
2	STB	0b	RW	0 = 1 stop bit. 1 = 2 stop bits, except for 5-bit character then 1-1/2 bits.
1:0	WLS[1:0]	00b	RW	00: 5-bit character (default) 01: 6-bit character 10: 7-bit character 11: 8-bit character

Table 3-336. Auto-Baud Control Register (ABR)

ABR
Base: BAR **Offset: 0024h**

Bits	Symbol	Default	Access	Description
31:4	Reserved		RV	Reserved
3	Reserved ABT	0b	RW	0 = Formula used to calculate baud rates allowing all possible baud rates to be chosen by UART as dictated.
2	ABUP	0b	RW	0 = Processor Programs Divisor Latch Registers. 1 = UART Programs Divisor Latch Registers.
1	ABLIE	0b	RW	0 = Autobaud Lock Interrupt disabled (Source IIR[ABL]). 1 = Autobaud Lock Interrupt enabled (Source IIR[ABL]).
0	ABE	0b	RW	0 = Autobaud Disabled. 1 = Autobaud Enabled.

Table 3-337. Line-Status Register (LSR)

LSR
Base: BAR **Offset: 0005h**

Bits	Symbol	Default	Access	Description
7	FIFOE	0b	Read	0 = No errors exist in the Receive FIFO. 1 = At least one character in Receiver FIFO has errors.
6	TEMT	1b	Read	0 = There is data in the Transmit Shift register, the Transmit Holding register, or the FIFO (in FIFO mode). 1 = All the data in the transmitter has been shifted out.
5	TDRQ	1b	Read	0 = The UART is NOT ready to receive data for transmission. 1 = The UART is ready to receive data for transmission.
4	BI	0b	RC	0 = No break signal has been received. 1 = Break signal has been received.
3	FE	0b	RC	0 = No Framing error. 1 = Framing error has occurred.
2	PE	0b	RC	0 = No Parity error. 1 = Parity error has occurred.
1	OE	0b	RC	0 = No overflow error. Data has not been lost. 1 = Overflow error. Receive data has been lost.
0	DR	0b	Read	0 = No data has been received. 1 = Data is available in RBR or the FIFO.

Table 3-338. Modem-Control Register (MCR)

MCR
Base: BAR **Offset: 0004h**

Bits	Symbol	Default	Access	Description
7:6	Reserved	0	RV	Reserved
5	AFE	0b	RW	0 = Auto-RTS and auto-CTS are disabled. 1 = Auto-CTS is enabled. If MCR[RTS] is also set, both auto-CTS and auto-RTS is enabled.
4	LOOP	0b	RW	0 = Normal UART operation. 1 = Loop-back Test mode operation.
3	OUT2	0b	RW	0 = nDCD UART pin input set low when in Loop-back mode. Disable UART interrupts when NOT in Loop-back mode. 1 = nDCD UART pin input set high when in Loop-back mode. Enable UART interrupts when NOT in Loop-back mode.
2	OUT1	0b	RW	0 = nRI UART pin input set low when in Loop-back mode. 1 = nRI UART pin input set high when in Loop-back mode.
1	RTS	0b	RW	0 = Non-autoflow mode. nRTS pin is 1. nRTS pin is 0. 1 = Autoflow mode. Auto-RTS disabled. Auto flow works only with auto-CTS. Auto-RTS enabled. Auto flow works with both auto-CTS and auto-RTS.
0	DTR	0b	RW	0 = nDTR pin is 1. 1 = nDTR pin is 0.

Table 3-339. Modem Status Register (MSR)

MSR
Base: BAR **Offset: 0006h**

Bits	Symbol	Default	Access	Description
7	DCD	0b	RO	**Data Center Detect:** 0 = nDCD pin value is currently a 1. 1 = nDCD pin value is currently a 0.
6	RI	0b	RO	**Ring Indicator:** 0 = nRI pin value is currently a 1. 1 = nRI pin value is currently a 0.
5	DSR	0b	RO	**Data Set Ready:** 0 = nDSR pin value is a 1. 1 = nDSR pin value is a 0.
4	CTS	0b	RO	**Clear to Send:** 0 = nCTS pin value is currently a 1. 1 = nCTS pin value is currently a 0.
3	DDCD	0b	RO	**Delta Data Set Ready:** 0 = No change in nDSR pin since last read of MSR. 1 = nDSR pin has changed state.
2	TERI	0b	RO	**Trailing Edge Ring Indicator:** 0 = nRI pin has not changed from 0 to 1 since last read of MSR. 1 = nRI pin has changed state.
1	DDSR	0b	RO	**Delta Data Set Ready:** 0 = No change in nDSR pin since last read of MSR. 1 = nDSR pin has changed state.
0	DCTS	0b	RO	**Delta Clear To Send:** 0 = No change in nCTS pin since last read of MSR. 1 = nCTS pin has change state.

Table 3-340. SPR—Scratchpad Register (SPR)

SPR
Base: BAR **Offset: 0007h**

Bits	Symbol	Default	Access	Description
7:0	SCRATCH	00h	RW	Scratchpad. Writing to this field does not affect the operation of the UART in any way.

Table 3-341. Auto-Baud Count Register (ACR)

ACR
Base: BAR **Offset: 0028h**

Bits	Symbol	Default	Access	Description
31:16	Reserved	0	RV	Reserved
15:0	ACR[15:0]	0000h	RO	Number of 50 MHz clock cycles within a start bit pulse.

Table 3-342. Pre-Scalar Register (PSR)

PSR
Base: BAR **Offset: 0030h**

Bits	Symbol	Default	Access	Description
31:16	Reserved	0	RV	Reserved
15:0	PS[15:0]	0010h	RW	Number of sample per baud rate within a bit pulse.

Table 3-343. DDS Multiplier Register (DDSMR)

DDSMR
Base: BAR **Offset: 0034h**

Bits	Symbol	Default	Access	Description
31:24	Reserved	0	RV	Reserved
23:0	MUL[23:0]	576d	RW	Multiplier Number of the DDS.

Table 3-344. DDS Divisor Register (DDSDR)

DDSDR
Base: BAR **Offset: 0038h**

Bits	Symbol	Default	Access	Description
31:24	Reserved	o	RV	Reserved
23:0	DIV[23:0]	15625d	RW	Divisor Number of the DDS.

Table 3-345. SIR Control Register (SCR)

SCR
Base: BAR **Offset: 003Ch**

Bits	Symbol	Default	Access	Description
31:5	Reserved	o	RV	Reserved
4	RX_RAWD	0	RO	RX Raw Data
3	TX_RAWD	0	RW	TX Raw Data
2	BYPASS	0	RW	Raw data bypass: 0 = Disable 1 = Enable Software can send/receive raw data through TXD and RXD pins.
1	SIRPW	0	RW	Pulse Width Selector: 0 = 3/16 1 = 1.6 µs
0	SIREN	0	RW	SIR Enable: 0 = Disable SIR 1 = Enable SIR

Table 3-346. Status Register (SSR)

SIR
Base: BAR **Offset: 003Ch**

Bits	Symbol	Default	Access	Description
31:0	Reserved	00000000	RV	Reserved

3.7 S12x0 Intel® Atom™ Core Model Specific Registers

The Model Specific Registers are unique to each execution thread (per core).

3.7.1 Model Specific Registers

The Model Specific Registers (MSRs) for the S12x0 processor are similar to those of the Pentium® M processor. Key MSR definitions are included in this chapter. For supplemental information regarding MSRs, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Combined Volumes: 1, 2A, 2B, 3A, and 3B*.

The second column in the MSR descriptions titled 'S' represents the scope of the bit field within the MSR as below:

S: The bit field is shared among the logical processors.

U: The bit field is unique to each logical processor within a package.

Table 3-347. IA32_PLATFORM_ID—Platform Identification Status Register

MSR Address: 017h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read only

Bit	Attribute	Reset Value	Description
63:53	RV	Xs	Reserved
52:50	RO	XXX	**Platform ID Bits:** The field gives information concerning the intended platform for the processor.
49:29	RV	Xs	Reserved
28	RO	X	**Mobile:** A value of 1 indicates the part is a mobile processor, a value of 0 indicates the part is not a mobile processor.
27	RO	X	**Production:** A value of 0 indicates the part is intended for production, a value of 1indicates the part is a pre-production sample.
26:20	RV	Xs	Reserved
19	RO	X	**Intel® Thermal Monitor Disabled:** A value of 1 indicates that the processor does not support any type of thermal monitoring. A value of 0 indicates that some type of Intel® Thermal Monitor functionality is available. See Intel® Thermal Monitor capability for further information.
18	RV	X	Reserved
17	RO	X	**Enhanced Intel SpeedStep® Technology Disabled:** A value of 1 indicates that the processor is not Enhanced Intel SpeedStep Technology capable. A value of 0 indicates that the processor is capable of this feature.
16	RV	X	Reserved
15	RO	X	**Ratio Locked:** A value of 1 in this field indicates that the processor maximum bus ratio is at a fixed value and cannot be changed. A value of 0 in this field indicates that the processor maximum bus ratio is a limit value only, and software can set a lower maximum bus ratio by using the flexible bus ratio controls.
14:13	RV	XX	Reserved
12:8	RO	Xs	**Maximum Frequency:** The maximum allowed bus ratio.
7:6	RV	XX	Reserved
5:0	RO	Xs	**Maximum V_{CC}:** The maximum allowed VID.

Table 3-348. IA32_FEATURE_CONTROL—Feature Control Register

MSR Address: 03Ah Accessed as a Qword
Reset Value: XXXX XXXX XXX0 0000h
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:17	RV	Xs	Reserved
16	RW	0	**C-State SMI:** When set causes Monitor to be retained and Monitor/MWAIT instructions to be converted to PAUSE instructions during SMI execution. Used for C-State/SMI interaction under power management.
15	RW	0	**SENTER Global Enable:** When set, global SENTER is enabled. ***Note:*** BIOS must set this bit only when the CPUID function 1 returns SMX feature flag set (ECX bit 6).
14:8	RW	0000000	**SENTER Local Function Enables:** When set, SENTER local functions are enabled. Valid Values are: All ones if Bit 15 is 1. All zeros if Bit 15 is 0. Any other value raises a general protection fault exception. ***Note:*** BIOS must set this bit only when the CPUID function 1 returns SMX feature flag set (ECX bit 6).
7:4	RV	Xs	Reserved
3	RW	0	**SMRR Enable (R/WL):** When this bit and the Lock bit (Bit 0 of this MSR) are set, the SMRR feature is enabled.
2	RW	0	**Enable VMX outside SMX Operation:** This bit enables Intel® Virtualization Technology in an environment that may not include Intel® Trusted Execution Technology (Intel® TXT) technology support. ***Note:*** BIOS must set this bit only when the CPUID function 1 returns VMX feature flag set (ECX bit 5).
1	RW	0	**Enable VMX inside SMX Operation:** This bit enables Intel Virtualization Technology in an environment that includes Intel Trusted Execution Technology (Intel TXT) technology support. ***Note:*** BIOS must set this bit only when the CPUID function 1 returns VMX feature flag and SMX feature flag set (ECX bits 5 and 6 respectively).
0	RW	0	**Lock bit:** (1 = locked). When set, locks this MSR from being written, writes to this bit results in GP(0). ***Note:*** Once the Lock bit is set, the contents of this register cannot be modified. Therefore the lock bit must be set after configuring support for Intel Virtualization Technology and prior to transferring control to an option ROM or the OS. Hence, once the Lock bit is set, the entire IA32_FEATURE_CONTROL_MSR contents are preserved across RESET when PWRGOOD is not de-asserted.

Table 3-349. IA32_TEMPERATURE_OFFSET—Thermal Diode Offset

MSR Address: 03Fh Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
63:8	RV	Xs	Reserved
7:0	RO	Xs	**Thermal Diode Offset:** A read only binary signed value indicating temperature offset in 0.5 °C resolution. This value need to be subtracted from the diode reading in order to get the actual die temperature. Values are: 00000000 = 0 °C 00000010 = +1 °C 11111110 = -1.0 °C 10000000 = -64 °C

Table 3-350. CLOCK_CR_GEYSIII_VCC_3

MSR Address: 0CFh Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
63:18	RV	Xs	Reserved
17:12	RO	Xs	**GUAR_VID:** The fused CPU VID at which the TDP for this part is guaranteed. This value is not used directly by hardware but is available for software use. For P-States higher than this ratio/vid, the CPU is considered to be in Burst Mode and TDP is not guaranteed. For SKUs with Burst mode disabled, this value equals MAX_VID.
11:7	RO	Xs	**GUAR_RATIO:** The fused CPU to internal FSB ratio at which the TDP for this part is guaranteed. This value is not used directly by hardware but is available for software use. For P-States higher than this ratio/vid, the CPU is considered to be in Burst Mode and TDP is not guaranteed. For SKUs with Burst mode disabled, this value equals MAX_RATIO.
6:0	RO	Xs	**C6 VID:** A read only binary value reflecting the fused VID voltage used for C6.

Table 3-351. SMM_CST_MISC_INFO—C-State Information in SMM

MSR Address: 0E1h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
63:32	RO	Xs	Reserved
31:28	RO	Xs	**Package C-State:** The Coordinated C-State of the Package when the SMI was detected. Represents the target state if SC_SMI (bit 0) is 1 or the actual state if SC_SMI (bit 0) is 0. 1111b = C0 0000b = C1 0001b = C2 0011b = C4 0101b = C6 All others **Reserved** on the S12x0 processor.
27:24	RO	XXX	**Package Frequency:** The Frequency state of the Package when the SMI was detected. 0000b = Non – LFM Frequency 0001b = LFM Frequency 1000b = No L2 Shrink All others reserved on the S12x0 processor.
23:20	RO	XXX	**Thread C-State:** The C-State of the thread when the SMI was detected. 1111b = C0 0000b = C1 0001b = C2 0011b = C4 0101b = C6 1110b = Auto Halt All others reserved on the S12x0 processor.
19:17	RO	XXX	**L2 Shrink State:** L2 Shrink state of the thread when the SMI was detected. 001 = Thread Full Shrink L2 100 = Thread No Shrink L2 All others reserved on the S12x0 processor**.**
16	RO	X	**Thread Frequency:** The Frequency state of the thread when the SMI was detected. 0b = Non – LFM Frequency 1b = LFM Frequency All others reserved on the S12x0 processor.
15	RO	X	**Block SMI:** When set to ‘1b’, prevents SMI generation internally upon C-State transitions.
14:8	RV	Xs	Reserved
7:4	RO	XXXX	**I/O Type:** Identifies the C-State SMI information in SMRAM. Set to 1010b’ when thread C-State is TC1 to TC6 (excluding AHLT).
3:1	RV	XXX	Reserved
0	RO	X	**SC_SMI:** Identifies whether the SMI had occurred as a result of a C-State mechanism. 1b = Going into a C2/C4/C6 state 0b = In a stable C-State or runtime

Table 3-352. PMG_CST_CONFIG_CONTROL—C-State Configuration (Sheet 1 of 2)

MSR Address: 0E2h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:26	RV	Xs	Reserved
25	RW	X	**C6 Demotion Enable:** When set, enables the S12x0 processor C-State policy to demote the C-State to C6 when conditions allow.
24:21	RV	XXXX	Reserved
20:16	RW	XXXXX	**L2 Shrink Threshold:** L2 shrinking is allowed only when current bus ratio is below or equal to this ratio. When the current bus ratio is above this threshold, L2 expansion does occur. A value of 0 results in a ratio being excluded from the L2 cache shrinking decision by the processor. Reset Value is 00110b' (6h).
15	RW	X	**CFG Lock:** When set, locks bits [15:0] in this register for further writes until the next reset occurs. It is expected that the BIOS sets this bit to lock the power management configuration settings in this MSR prior to OS boot.
14:12	RV	XXX	Reserved
11	RW	X	**Enhanced Intel SpeedStep® Technology Hardware Coordination Disable:** When set, disables hardware coordination of Enhanced Intel SpeedStep Technology requests from the two logical processors. BIOS ONLY sets this bit when the operating system supports software coordination of performance states.
10	RW	X	**I/O MWAIT Redirection Enable:** When set, maps I/O read instructions sent to I/O registers at PMG_IO_BASE_ADDR.PMB0 to MWAIT (C2/C4/C6) instructions.
9	RWL	X	**STPGNT Issue:** Specifies the number of Stop Grant cycles that the processor issues upon a STPCLK (a Stop Grant request). For Dual Core Intel® Atom™ Processor: CPU0: 0 = Issues a single Stop Grant cycle from CPU0 (master) upon a STPCLK. 1 = Issues a single Stop Grant cycle from CPU0 (master) upon a STPCLK. CPU1: 0 = Issues NO Stop Grant cycle from CPU1 (slave) upon a STPCLK. 1 = Issues a single Stop Grant cycle from CPU1 (slave) upon a STPCLK. ***Note:*** For dual-core Intel® Atom™ Processor there is only 1 (default) or 2 (programmable) STPGNT cycles, (even though we have 4 threads). CPU0/CPU1 = [00] = 1 total stop grant cycle CPU0/CPU1 = [01] = 2 total stop grant cycles CPU0/CPU1 = [10] = 1 total stop grant cycle CPU0/CPU1 = [11] = 2 total stop grant cycles
8:7	RV	XX	Reserved

Table 3-352. PMG_CST_CONFIG_CONTROL—C-State Configuration (Sheet 2 of 2)

MSR Address: 0E2h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
6:4	RWL	XXX	**CSM Trigger:** Specifies the request-resolved state from which SMI is triggered. When both logic processors enter the C-State specified in this register, the I/O port address PMB1 (Bits [31:16] in PMG_IO_BASE_ADDR MSR) is accessed in order to generate an SMI. 000b = Disabled 001b = C1 010b = C2 100b = C4 110b = C6 111b = AutoHalt All others reserved on the S12x0 processor.
3	RWL	X	**Dynamic L2 Enable:** When set, enables automatic L2 size reduction when the processor enters C4/C6.
2:0	RWL	XXX	**Package CState Limit:** Specifies the lowest C-State the package can go to. 000b = No Limit 001b = C1 010b = C2 100b = C4 110b = C6 All others reserved on the S12x0 processor.

Table 3-353. PMG_IO_BASE_ADDR—C-State Redirection I/O Base Address

MSR Address: 0E3h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:32	RW	Xs	Reserved
31:16	RW	Xs	**PMB1**: I/O port address in the Intel® Atom™ core Logic enabled to generate SMIs. This value is used by the power management logic to generate SMIs. When both logical processors enter the state specified by the CSM Trigger in PMG_CST_CONFIG_CONTROL, the SMI is generated by issuing a read to the I/O port specified by this field.
15:0	RW	Xs	**PMB0**: I/O port address used by the power management logic for coordinated LVL_x I/O reads when enabled. This field specifies the base of the I/O range read by the processor power management logic to transition the whole package to a particular C-State (refer to Intel® 64 and IA-32 Architectures Software Developer's Manuals when both logical processors enter a low power C-State through the I/O MWAIT redirection or through an MWAIT (Cx) instruction. PMB0 is programmed to the chipset level_2 IO address.

Table 3-354. PMG_IO_CAPTURE_ADDR—C-State I/O Capture Base Address

MSR Address: 0E4h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:23	RV	Xs	Reserved
22:16	RW	Xs	**CST Range**: I/O port block size in which I/O redirection is executed (0-127). This zero-based value corresponds to the number of LVL_x registers supported by the Atom cores. For example, if the chipset supports LVL_2, LVL_3, LVL_4, this register would be programmed to 2).
15:0	RW	Xs	**LVL_2 Base Address**: Base address of the LVL_2 register visible to software. If I/O MWAIT Redirection is enabled, reads to this address is consumed by the power management logic and decoded to MWAIT instructions. When I/O port address redirection is enabled, this is the I/O port address reported to the OS/software.

Table 3-355. IA32_MPERF—Maximum Frequency Clock Count

MSR Address: 0E7h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:0	RW	Xs	***Note:*** **C0_MCNT**: C0 maximum frequency clock count: Increments at maximum clock frequency (as allowed by the Resolved Ratio) when thread is in C0. Cleared by a write to the MCNT, the ACNT and upon overflow/wrap-around of this counter.

Table 3-356. IA32_APERF—Actual Frequency Clock Count

MSR Address: 0E8h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:0	RW	Xs	**C0_ACNT:** C0 actual frequency clock count: Accumulates thread clock counts – at the coordinated clock frequency, when thread is in C0. Cleared by a write to this field or the MCNT.

Table 3-357. BBL_CR_CTL3—Control Register 3

MSR Address: 011Eh Accessed as a Qword
Reset Value: High Dword, XXXX XXXXh
Low Dword, XXXX XXXXh
Attribute: Read Only, Read/Write

Bit	Attribute	Reset Value	Description
63:32	RV	Xs	Reserved
31:30	RWL	XX	**L2 Way Shrink Minimum:** Minimum L2 size, beyond which no shrinking is done. 00b = minimum 0 and stay in 0 when leaving TC4/CC6 01b = minimum 0 and auto expand 2 ways in TC0 10b = minimum 2 (default) 11b = minimum 4
29:28	RWL	XX	**L2 Way Shrink Rate:** Number of ways to be shrunk in each C4 /C6 entry. 00b = 0 01b = 1 10b = 2 11b = 4 (default)
27:25	RWL	XXX	**L2 Way Chunk Size:** Size of minimal portion of L2 way that has to be flushed before opening a window for interrupts. 000b = 1 way 001b = 1/2 way 010b = 1/4 way 011b = 1/8 way 100b = 1/16 way 101b = 1/32 way 110b = 1/64 way 111b = 1/128 way (default) It is not recommended to change this value when L2 is partially shrunk.
24	RWL	X	**L2 Reduction Configuration Lock:** When set, bits 31:24 cannot be changed until next reset.
23	RO	X	**L2 Not Present:** This bit reflects L2 not present. A value of 0 = L2 Present, 1 = L2 Not Present.
22:18	RV	Xs	Reserved
17:13	RO	XXXXX	**Size of Way:** Indicates the size of each way 00000b = 64 Kbytes (default).
12:9	RV	XXXX	Reserved
8	RW	X	**L2 Enabled** 0 = Disabled. 1 = Enabled (default). Until this bit is set the processor does not respond to the WBINVD instruction or the assertion of the FLUSH# input.
7:5	RV	X	Reserved
4:1	RZ	XXXX	**Number of Ways:** Indicates number of ways of L2 cache. 0001b = 2 low ways 0011b = 4 low ways 1111b = 8 ways
0	RO	X	**L2 Hardware Enabled:** This bit is set to a 1 if the L2 is hardware-enabled. A value of 0 indicates that the L2 is hardware-disabled.

Table 3-358. IA32_PERF_STS—Performance Status Register (Sheet 1 of 2)

MSR Address: 0198h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
63:61	RV	XXX	Reserved
60:56	RO	XXXXX	**BUS_RATIO_BOOT:** This field indicates the boot bus ratio (as encoded by bus ratio table) of the processor.
55	RV	X	Reserved
54:48	RO	XXXXXXX	**VID_BOOT:** This field indicates the boot V_{CC} (as encoded by VID table) of the processor. See the appropriate processor datasheet or EMTS for the allowable VID values for the particular processor; not all voltages are supported.
47:45	RV	XXX	Reserved
44:40	RO	XXXXX	**BUS_RATIO_MAX:** This field indicates the maximum bus ratio (as encoded by bus ratio table) that is supported by the processor.
39	RV	X	Reserved
38:32	RO	XXXXXXX	**VID_MAX:** This field indicates the maximum V_{CC} that is supported by the processor.
31:29	RV	XXX	Reserved
28:24	RO	XXXXX	**BUS_RATIO_MIN:** This field indicates the minimum bus ratio (600 or 800 MHz) that is supported by the processor.
23:22	RV	X	Reserved
21	RO	X	**TS:** This bit indicates that an Enhanced Intel SpeedStep® Technology transition has been started by the software writing a new value to the PERF_CTRL register, or due to a thermal trip event on the internal sensor. This bit is read-only and cleared once all pending voltage changes have been completed.
20	RO	X	**CMD_SEEK:** This bit indicates that the processor is currently performing an Enhanced Intel SpeedStep Technology transition. This bit is read-only and cleared once all pending voltage and frequency changes have been completed.
19	RO	X	**THERM_THROT:** This bit indicates that the processor has initiated a cold to hot performance state transition to the Intel® Thermal Monitor performance state. This bit is read-only and remains set until the thermal condition has ended.
18	RO	X	**TT:** Thermal trip indicator event is active. This indicates that the processor is above the recommended operating temperature. This bit is read-only and cleared once the temperature drops below recommended operating temperature.
17	RO	X	**VIP:** Voltage transition pending. This bit indicates that the processor currently has a pending voltage transition. This bit is read-only and cleared once all pending voltage changes have been completed.
16	RO	X	**FIP:** Frequency change pending. This bit indicates that the processor currently has a pending frequency transition. This bit is read-only and cleared once all pending frequency changes have been completed.
15:13	RV	XX	Reserved

Table 3-358. IA32_PERF_STS—Performance Status Register (Sheet 2 of 2)

MSR Address: 0198h Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
12:8	RO	XXXXX	**BUS_RATIO_STS:** Current bus ratio of the processor as encoded by bus ratio table. This field is updated dynamically as processor performance state transitions are completed.
7	RV	X	Reserved
6:0	RO	XXXXXXX	**VID_STS:** Current V_{CC} as encoded by the VID table. This field is updated dynamically as processor performance state transitions are completed. See Appendix E for the allowable VID values for the Intel® Atom™ Processor S1200 Product Family processor; not all voltages are supported.

Table 3-359. IA32_PERF_CTL—Performance Control Register

MSR Address: 0199h Accessed as a Qword
Reset Value: High Dword, XXXX XXXXh
Low Dword: XXXX XXXX XXXX XXXX XXX0 0000 X00 0000h
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:13	RV	Xs	Reserved
12:8	RW	Xs	**BUS_RATIO_SEL (R/W)**: Requested Bus Ratio. The BUS_RATIO_MAX field in the IA32_PERF_STS register specifies the maximum possible bus ratio. Specifying a higher value causes a transition to the BUS_RATIO_MAX value. The BUS_RATIO_MIN field in the IA32_PERF_STS register specifies the minimum possible bus ratio. Specifying a lower value causes a transition to the BUS_RATIO_MIN value.
7	RV	XX	Reserved
6:0	RW	Xs	**VID_SEL:** Requested V_{CC} as encoded by VID table. The requested value is checked against VID_MAX, and truncated to VID_MAX if higher. The VID_MAX field in the IA32_PERF_STS register specifies the maximum possible voltage. Specifying a higher value causes a transition to the VID_MAX value.

Table 3-360. IA32_CLOCK_MODULATION—ACPI Intel® Thermal Monitor Control Register

MSR Address: 019Ah Accessed as a Qword
Reset Value: High Dword XXXX XXXXh
Low Dword: XXXX XXXX XXXX XXXX XXXX XXXX XXX0 001Xb
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:5	RV	Xs	Reserved
4	RW	XXXX	**On-Demand Thermal Control Circuit Enable**: This bit allows the BIOS to activate or deactivate the On-Demand Thermal Control Circuit (TCC) portion of the Intel® Thermal Monitor feature. A value = 0 (default) disables the on-demand TCC, and a value = 1 enables the on-demand TCC. The On-Demand TCC does not depend on temperature (only automatic TCC depends on temperature). If both the “on-demand” thermal control circuit and the automatic thermal control circuit are enabled, the automatic TCC takes precedence.
3:1	RW	XXX	**On-Demand Clock Modulation Duty Cycle (R/W)**: This field provides the on-demand clock modulation duty cycle. It indicates the clock on to clock off interval ratio. The Reset Value for this field is 001b, indicating that the period in which the clock is running is 12.5% of the overall time. Bits[3:1] Duty Cycle 000b Reserved 001b 12.5% 010b 25.0% 011b 37.5% 100b 50.0% 101b 62.5% 110b 75.0% 111b 87.5%
0	RV	X	Reserved

Table 3-361. IA32_THERM_INTERRUPT – ACPI Intel® Thermal Monitor Interrupt Control Register

MSR Address: 019Bh Accessed as a Qword
Reset Value: High Dword XXXX XXXXh
Low Dword: XXXX XXXX XXXX XXXX XXXX XXXX XXXX XX00b
Attribute: Read/Write

Bit	Attribute	Reset Value	Description
63:24	RV	Xs	Reserved
23	RW	X	**Threshold #2 Interrupt Enable:** Enables the generation of an interrupt when the actual temperature relative to T_{jmax} reaches the value specified in Threshold #2 value. 0 = Disabled 1 = Enabled
22:16	RW	Xs	**Threshold #2 Value:** A temperature relative to T_{jmax} used to generate an interrupt when the Threshold #2 Interrupt Enable bit is set and the actual relative temperature reaches or crosses this value. ***Note:*** The resolution of this value is 1°C with the accuracy of ±1 °C.
15	RW	X	**Threshold #1 Interrupt Enable:** Enables the generation of an interrupt when the actual temperature relative to T_{jmax} reaches the value specified in Threshold #1 value. 0 = Disabled 1 = Enabled
14:8	RW	Xs	**Threshold #1 Value:** A temperature relative to T_{jmax} used to generate an interrupt when the Threshold #1 Interrupt Enable bit is set and the actual relative temperature reaches or crosses this value. ***Note:*** The resolution of this value is 1 °C with the accuracy of ±1 °C.
7:5	RV	XXX	Reserved
4	RW	X	**Overheat Interrupt Enable:** Enables the generation of an interrupt when an Overheat temperature (>Tj) is reached. 0 = Disabled 1 = Enabled
3	RW	X	**FORCPR# Interrupt Enable:** This bit allows the BIOS to enable the interrupt on the assertion of an external FORCEPR .
2	RW	X	**THERMTRIP# Interrupt Enable:** When a catastrophic cooling failure occurs, the processor automatically shuts down. 0 = Disabled 1 = Enabled
1	RW	X	**Low-Temperature Interrupt Enable:** This bit allows the BIOS to enable the generation of an interrupt on the transition from high-temperature to a low-temperature. A value = 0 (default) disables interrupts, and a value = 1 enables interrupts.
0	RW	X	**High-Temperature Interrupt Enable:** This bit allows the BIOS to enable the generation of an interrupt on the transition from low-temperature to a high-temperature threshold. A value = 0 (default) disables interrupts, and a value = 1 enables interrupts.

Table 3-362. IA32_THERM_STATUS—ACPI Intel® Thermal Monitor Status Register (Sheet 1 of 2)

MSR Address: 019Ch Accessed as a Qword
Reset Value: High Dword, XXXX XXXXh
Low Dword: XXXX XXXX XXXX XXXX XXXX XXXX XXXX XX00b
Attribute: Read/Write, Read Only

Bit	Attribute	Reset Value	Description
63:32	RV	XXXXX	Reserved
31	RO	X	Reading Valid
30:27	RO	XXXX	Resolution in ^oC
26:23	RV	XXXX	Reserved
22:16	RO	Xs	**Digital Readout:** Digital temperature reading in 1 °C relative to T_{jmax}. 0 = T_{jmax}; 1 = T_{jmax} – 1 ^oC; etc. See the EMTS for details regarding T_{jmax}. The resolution of this value is 1 °C with the accuracy of ±1 °C. The minimum valid readout is 1. A value of 0 indicates the out of specification condition.
15:10	RV	Xs	Reserved
9	RWC0	X	**Thermal Threshold #2 Log:** Sticky bit that indicates whether the Thermal Threshold #2 has been reached since the last clearing of this bit or reset. Reading 0 = has not been active; Reading 1 = has been active; This bit may be cleared by software by writing a 0.
8	RO	X	**Thermal Threshold #2 Status:** Indicates whether the actual temperature is currently higher than the value set in Thermal Threshold #2. Actual temperature higher = 0; Actual temperature greater or equal = 1.
7	RWC0	X	**Thermal Threshold #1 Log:** Sticky bit that indicates whether the Thermal Threshold #1 has been reached since the last clearing of this bit or reset. Reading 0 = has not been active; Reading 1 = has been active; This bit may be cleared by software by writing a 0.
6	RO	X	**Thermal Threshold #1 Status:** Indicates whether the actual temperature is currently higher than the value set in Thermal Threshold #1. Actual temperature lower = 0; Actual temperature greater or equal = 1.
5	RWC0	X	**Out Of Spec Status Log:** Sticky bit that indicates whether the overheat detector output signal has been asserted since the last clearing of this bit or reset. Reading 0 = has not been active; Reading 1 = has been active; This bit may be cleared by software by writing a 0.
4	RO	X	**Out Of Spec Status:** Indicates whether the overheat detector output signal is currently active. Active = 1; Inactive = 0;
3	RWC0	X	**PROCHOT# or FORCEPR# Log:** Sticky bit that indicates whether PROCHOT# or FORCEPR# has been asserted since the last clearing of this bit or reset. Reading 0 = has not been active; Reading 1 = has been active; This bit may be cleared by software by writing a 0.

Table 3-362. IA32_THERM_STATUS—ACPI Intel® Thermal Monitor Status Register (Sheet 2 of 2)

MSR Address: 019Ch Accessed as a Qword
Reset Value: High Dword, XXXX XXXXh
Low Dword: XXXX XXXX XXXX XXXX XXXX XXXX XXXX XX00b
Attribute: Read/Write, Read Only

Bit	Attribute	Reset Value	Description
2	RO	X	**PROCHOT# or FORCEPR# Event:** Indicates whether PROCHOT# or FORCEPR# is being asserted. Active = 1; Inactive = 0. ***Note:*** Due to the asynchronous nature of thermal notification, the actual value of this bit set by the processor in a thermal event could be delayed by 1 bus clock.
1	RWC0	X	**Thermal Status Log:** This is a sticky bit that indicates the history of the thermal sensor high temperature output signal (PROCHOT#). This bit is set to 1 if PROCHOT# has been asserted since either the previous RESET or the last time software cleared this bit. A value = 0 indicates not active, and a value = 1 indicates active. This bit may be cleared by software by writing a 0.
0	RO	X	**Thermal Status:** This bit indicates whether the thermal sensor high-temperature output signal (PROCHOT#) is currently active. A value = 0 indicates not active, and a value = 1 indicates active. This bit may not be written by software.

Table 3-363. MSR_THERM2_CTL—Intel® Thermal Monitor Control Register

MSR Address: 019Dh Accessed as a Qword
Reset Value: XXXX XXXX XXXX XXXXh
Attribute: Read Only

Bit	Attribute	Reset Value	Description
63:13	RV	Xs	Reserved
12:8	RO	XXXXX	**BUS_RATIO_THROT:** Throttling bus ratio as encoded by bus ratio table. If the Intel® Thermal Monitor 2 is enabled, this field represents the frequency (bus ratio) of the throttled performance state that is initiated when the on-die sensor goes from not hot to hot.
7:6	RV	XX	Reserved
5:0	RO	XXXXXX	**VID_THROT:** Throttling V_{CC} as encoded by VID table. If the Intel Thermal Monitor 2 is enabled, this field represents the voltage of the throttled performance state that is initiated when the on-die sensor goes from not hot to hot.

Table 3-364. IA32_MISC_ENABLES – Miscellaneous Enables Register (Sheet 1 of 2)

MSR Address: 01A0h Accessed as a Qword
Default Value: High Dword, XXXX XXXXh
Low Dword: XXXX XXXXh
Access: Write Once, Read/Write, Read Only

Bit	S	Description
63:35	S	
34	U	**Execute-Disable Bit Disable (R/W):** When set, this bit causes the CPUID instruction to return Execute-Disable Bit Capability not available. This bit is set by default, and must be cleared by BIOS to enable this feature. To enable Execute-Disable Bit, software must clear this bit in all processors in the HT configuration. Also software must make sure that this bit gets restored when the system comes out of the S3 and S4.
33	S	**Hard C4E Enable (R/W):** When set, sets the Package C4/Intel® Enhanced Deeper Sleep exit VIDs to the minimum Enhanced Intel SpeedStep®Technology operating point upon DPRSLP assertion. The CPU switches back to the original operating point once either execution thread exits to C0.
32	S	**C4E Enable (R/W):** When set, enables the CPU to switch to the minimum Enhanced Intel SpeedStep Technology operating point when both execution threads enter MWAIT (C4). The processor performs the frequency transition before the Level4 read cycle is issued. The CPU switches back to the original operating point once either execution thread exits to C0. ***Note:*** For dual core LCC, this feature must be enabled on both cores when the C4 state is supported.
31:28	S	Reserved
27	U	**ACNT2 Enable (R/W):** Setting this bit allow SW to use the ACNT2/MCNT2 feature. Feature enable allows the OSPM to better monitor actual CPU utilization in order to determine the correct operating point request.
26	S	**C2E Enable (R/W):** When set, enables the CPU to switch to the minimum Enhanced Intel SpeedStep Technology operating point when both execution threads enter MWAIT (C2). The processor performs the frequency transition before the Level2 read cycle is issued. The CPU switches back to the original operating points once either execution thread exits to C0.
25	S	**C1E Enable (R/W):** When set, enables the CPU to switch to the minimum Enhanced Intel SpeedStep Technology operating point when both execution threads enter MWAIT (C1). Frequency transition switches immediately, followed by gradual Voltage switching. The CPU switches back to the original operating point once either execution thread exits to C0.
24:23	S	Reserved
22	U	**Limit CPUID Maxval (R/W):** When set to 1, this causes the CPUID instruction function 0 to return a maximum value in EAX[7:0] of 3. When set to a 0 (default) the CPUID instruction function 0 returns the number corresponding to the maximum standard function supported. Some operating systems like Microsoft Windows NT* cannot handle a Maxval > 3. BIOS contains a setup option that allows the user to specify when an older OS is installed that does not support CPUID function > 3. Before setting this bit, BIOS must execute the CPUID instruction with EAX=0 and examine the maximum value returned in the EAX[7:0]. If the maximum value is > 3, then this bit is supported, otherwise this bit is not supported, and BIOS must not alter the contents of this bit location. Writing this bit when the maximum value is < 3 may generate a #GP exception.
21	S	**FORCEPR Input Enable (R/W)**: When set, this bit enables FORCEPR as an active input. This allows an external device to force throttling when asserted. ***Note:*** This bit is enabled for processor dual-core configurations to facilitate thermal monitor (TM) coordination between CPUs. 0 = (Default) FORCEPR input is disabled.

Table 3-364. IA32_MISC_ENABLES – Miscellaneous Enables Register (Sheet 2 of 2)

MSR Address: 01A0h Accessed as a Qword
Default Value: High Dword, XXXX XXXXh
Low Dword: XXXX XXXXh
Access: Write Once, Read/Write, Read Only

Bit	S	Description
20	S	**Enhanced Intel SpeedStep Technology Select Lock (R/WO):** When set, this bit causes the following bits to become read-only: Enhanced Intel SpeedStep® Technology Select Lock (this bit) and the Enhanced Intel SpeedStep Technology Enable bit. This bit must be set before an Enhanced Intel SpeedStep Technology transition is requested. This bit is cleared by Reset.
19	S	Reserved
18	S	**Enable Monitor FSM (R/W):** When set to 0 the MONITOR feature flag ECX[3] returned by the CPUID instruction when executed with EAX = 1 is cleared indicating that the MONITOR and MWAIT instructions are not supported. An Illegal Instruction Exception is generated if software attempts to execute either the MONITOR or MWAIT instruction when this bit is 0.
17	S	**Bi-Directional PROCHOT# Enable (RO):** Do not use this bit.
16	S	**Enhanced Intel SpeedStep Technology Enable (R/W):** Setting this bit enables the Enhanced Intel SpeedStep Technology mechanism. Software can set this bit only if IA32_PLATFORM_ID[17] is 0, IA32_PLATFORM_ID[50] is 1, and the Enhanced Intel SpeedStep Technology Select Lock bit is 0.
15:14	S	Reserved
13	S	**TM2 Enable (R/W):** When this bit is set to a 1, and the thermal sensor indicates that the die temperature is at the pre-determined threshold, the Enhanced TCC is engaged. This mechanism reduces the bus to core ratio to the value contained in the Intel® Thermal Monitor Core to Bus Ratio field in the MSR_THERM2_CTL register, and then step the operating voltage down to the value contained in the Intel Thermal Monitor VID field in the MSR_THERM2_CTL register. When this bit is set to a 0, the processor does not change the VID signals or the bus to core ratio when the processor enters a thermal managed state. The processor is operating out of spec if both this bit and the TM1 bit are set to disabled states.
12:11	S	Reserved
10	S	**FERR# Multiplexing Enable (R/W):** When this bit is set to a 1, FERR# is asserted by the processor to indicate a pending break event within the processor. A value of 0 indicates compatible FERR# signaling behavior. Used to enable breaking out of stopclk state via FERR assertion. ***Note:*** This bit must be set to 1 to support XAPIC interrupt model usage.
9:8	S	Reserved
7	S	**Performance Monitoring Available (RO):** When set, performance monitoring is enabled; when clear, performance monitoring is disabled.
6:4	S	Reserved
3	U	**TM1 Enable (R/W):** Setting this bit enables the Intel® Thermal Monitor 1. Enabling this bit allows the processor clocks to be automatically modulated based on the processor thermal sensor operation. A value = 0 (default) indicates disabled, and a value = 1 indicates enabled.
2:1	S	Reserved
0	U	**Fast String Enable (R/W):** Setting this bit enables fast strings for REP MOVS and REP STORS. A value = 0 indicates disabled, and a value = 1 (default) indicates enabled.

3.7.2 System Management Mode Range Register (SMRR)

The System Management Mode Range Register (SMRR) is an enhancement to the IA-32 Intel architecture that constrains SMM cacheability controls to SMM code. BIOS must be aware of processors that support the SMRR capability and can enable the SMRR when it is present.

After the microcode update has been loaded and during the SMM relocation phase of the POST, BIOS must detect if the processor supports SMRR by examining the SMRR_CAP bit (IA32_MTRR_CAP[11]). If the SMRR_CAP bit is set (1), the processor supports the SMRR feature. If the SMRR_CAP bit is clear (0), then the processor does not support the SMRR feature.

If the SMRR is supported, it must be enabled by setting bit 3 in the IA32_FEATURE_CONTROL MSR (MSR 3Ah) together with the lock bit (bit 0) of the same MSR.

Note: The CPU SMRR description does not exactly match what is documented in the *Intel® 64 and IA-32 Architectures Software Developer's Manuals*. The description in this manual overrides the SDM.

Table 3-365. IA32_MTRRCAP – MTRR Capability Register

MSR Address: 0FEh Accessed as a Qword
Default Value: XXXX XXXXh
Access: Read/Write

Bit	S	Description
63:12		Reserved
11	U	**SMRR supported (RO):** System Management Mode Range Registers supported.
10	U	**Write-Combining (RO):** Write-combining memory type supported.
9		Reserved
8	U	**FIX (RO):** Fixed range registers.
7:0	U	**VCNT (RO):** Number of variable range registers supported. This field may change value after the appropriate microcode update has been loaded and when SMRR has been enabled in the IA32_FEATURE_CONTROL MSR. BIOS uses this value to understand the number of variable range MTRR available and does not make an assumption about it.

Table 3-366. SMRR_PHYS_BASE – System Management Mode Base Address Register

MSR Address: 0A0h Accessed as a Qword
Default Value: XXXX XXXX XXXX XXXXh
Access: Read/Write

Bit	S	Description
63:32		Reserved
31:12	U	**PhysBase (R/W):** System Management Mode Memory range base address. The PhysBase must be aligned with the base of TSEG as configured by BIOS in the chipset.
11:0		Reserved

Table 3-367. SMRR_PHYS_MASK – System Management Mode Mask Register

MSR Address: 0A1h Accessed as a Qword
Default Value: XXXX XXXX XXXX XXXXh
Access: Read/Write

Bit	S	Description
63:32		Reserved
31:12	U	**PhysMask (R/W):** System Management Mode Memory range address mask. The size must be aligned to the TSEG size defined in the chipset
11	U	**Valid (R/W):** Valid bit, when set to a 1 by software, the range is enabled. When this bit is set to a 0 this SMRR range decoding is disabled.
10:0		Reserved

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4 Processor UnCore Registers

Table 4-1. Register Summary

Offset (h)	Size (bits)	Name
00	32	"DRAM Rank Population Register (DRP)" on page 239
01	32	"DRAM Timing Register 0 (DTR0)" on page 240
02	32	"DRAM Timing Register 1 (DTR1)" on page 242
03	32	"DRAM Timing Register 2 (DTR2)" on page 245
04	32	"DRAM Timing Register 3 (DTR3)" on page 247
06	32	"DRAM Power Management Control Register 0 (DPMC0)" on page 249
07	32	"DRAM Power Management Control Register 1 (DPMC1)" on page 251
08	32	"DRAM Refresh Control Register (DRFC)" on page 252
0A	32	"DRAM Calibration Control Register (DCAL)" on page 254
0B	32	"DRAM Reset Management Control (DRMC)" on page 254
0C	32	"Power Management Status (PMSTS)" on page 255
0F	32	"DRAM Controller Operation Register (DCO)" on page 256
14	32	"DRAM Gearing Register 0 (DGR0)" on page 257
15	32	"DRAM Gearing Register 1 (DGR1)" on page 258
16	32	"DRAM Gearing Register 2 (DGR2)" on page 259
18	32	"DRAM Address Map Register 0 (DMAP0)" on page 260
19	32	"DRAM Address Map Register 1 (DMAP1)" on page 261
1C	32	"DRAM Patrol Scrub Engine Register (DSCRUB)" on page 262
1D	32	"DRAM Patrol Scrub Address Register (DSADDR)" on page 262
1E	32	"DRAM Data Scrambler Register (DSCRMBL)" on page 263
20	32	"DRAM Status Register (DSTAT)" on page 263
4A	32	"Sticky Scratch Pad 0 Register (SSKPD0)" on page 263
4B	32	"Sticky Scratch Pad 1 Register (SSKPD1)" on page 263
60	32	"ECC and Parity Control Register (DECCCTL)" on page 264
61	32	"First Error and Next Error Register (FERRNERR)" on page 266
62	32	"Single Bit Error Logging Register (SBELOG)" on page 266
63	32	"Uncorrectable Read Error Logging Register (UCELOG)" on page 267
64	32	"Rank 0 Single Bit Error Count (SBECNT0)" on page 267
65	32	"Rank 1 Single Bit Error Count (SBECNT1)" on page 267
68	32	"Single Bit Error Accumulator Register (SBEACC)" on page 268
6A	32	"Error Status Register (DERRSTS)" on page 268
6B	32	"Error Mask and Severity Register (DERRMSKSEV)" on page 269
6C	32	"Uncorrectable Error Count Selection Register (DERRCNTSEL)" on page 270
6D	32	"Uncorrectable Error Count Register (DERRCNT)" on page 270

4.1 Memory Controller Registers

4.1.1 Private Space Registers

Table 4-2. Private Space Registers

Port-ID	Offset	Private Space Unit
87h	00h through FFFFh	Reserved. DDR3 PHY Private Space
8Ah	00h through FFh	Reserved. DDR3 CPGC Engine Private Space
01h	00h through FFh	DDR3 Memory Controller Private Space

4.1.1.1 DRAM Registers

Table 4-3. DRAM Rank Population Register (DRP)

DRP
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 00h

Bit	Attribute	Default	Description
31:21	RV	0	Reserved
20	RWS-L	0	**Mirrored Address Mapping to Rank 1 (RANK1_MIRROR):** BIOS writes value defined in SPD Byte 63. Used as indication to Power Management Unit to flip MRS opcode to 2nd rank on DIMM0. For soldered down devices with no SPD, BIOS sets this bit to match the board layout which is known to use either the standard or mirrored address mapping. For more details refer to the definition of byte 63 in the JEDEC DDR3 SPD specification. This bit has no functional impact on Memory Controller Unit. 0 = Standard 1 = Mirrored
19:13	RV	0	Reserved
12	RWS-L	0	**Address Map Select (ADDRMAP):** 0 = Map 0: The rank selection address bit is always the most significant address bit that is not out of range. Example, for a 4GB memory configuration with two ranks, A[31] selects the rank. 1 = Map 1: The rank selection address bit is defined by DMAP1[31:28] for dual rank configurations, and row address bit 7 is the most significant address bit that is not out of range; For single rank configurations, DMAP1[31:28] selects the address bit for row address bit.
11:7	RV	0	Reserved
6:5	RWS-L	0	**DRAM Density (DDEN):** This sets the density of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 0h - 1 Gbit 1h - 2 Gbit 2h - 4 Gbit 3h - Reserved
4	RWS-L	0	**DRAM Width (DWID):** Indicates the width of the DRAM devices populated in DIMM 0 (Rank 0 and Rank 1). 0 = x8 1 = x16
3:2	RV	0	Reserved
1	RWS-L	0	**Rank 1 Enable (RKEN1):** Rank 1 Enable: This bit is set to 1 when rank 1 is populated to enable use of this rank, otherwise it must be set to 0.
0	RWS-L	0	**Rank 0 Enable (RKEN0):** Rank 0 Enable: This bit is set to 1 when rank 0 is populated to enable use of this rank, otherwise it must be set to 0.

This register identifies the type of memory populated on each of the 2 memory ranks. These values must be configured during initialization and are then locked by writing to DCO bit 0.

Table 4-4. DRAM Timing Register 0 (DTR0) (Sheet 1 of 2)

DTR0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 01h

Bit	Attribute	Default	Description
31:28	RW	4h	**Additional Delay Between CK/CKB Start and SRX Command (CKE_DLY):** This delay is needed for clock to stabilize to meet JEDEC requirements. Delay is CKEDLY x 256 DRAM Clocks. 0ns to 7,200 ns (DDR3-1066) 0ns to 5,760 ns (DDR3-1333)
27:26	RV	0	Reserved
25:24	RW	3h	**DRAM Clocks Delay Between SR Entry Command and Power-Mode Message to DDRIO (PME_DLY):** 0h - 6 DRAM Clocks 1h - 8 DRAM Clocks 2h - 10 DRAM Clocks 3h - 12 DRAM Clocks
23	RV	0	Reserved
22	RW	0	**DRAM Clocks Delay Between ZQC-Long Command to Any Command (tZQCL):** The ZQCL command during DRAM Init flow requires longer latency, which is controlled by BIOS. 0 = 256 DRAM Clocks 1 = 384 DRAM Clocks
21	RV	0	Reserved
20	RW	0	**DRAM Clocks Delay Between a ZQC-Short Command to Any Command (tZQCS):** 0 = 64 DRAM Clocks 1 = 96 DRAM Clocks
19	RV	0	Reserved
18	RW	0	**DRAM Clocks Delay Between SRX Command to Any Command Requiring Locked DLL (tXSDLL):** In the S12x0, only ZQCL can be sent before tXSDLL is done. 0 = tXS + 256 DRAM Clocks 1 = tXS + 384 DRAM Clocks
17	RV	0	Reserved
16	RW	0	**DRAM Clocks Delay Between SRX Command to Command Not Requiring Locked DLL (tXS):** In the S12x0, the Memory Controller Unit can send a ZQCL command after tXS. JEDEC defines MAX(5CK, tRFC(min)+10 ns) so both of the S12x0 values take safety margin. 0 = 256 DRAM Clocks 0 = 384 DRAM Clocks
15	RV	0	Reserved
14:12	RW	1h	**CAS Latency (tCL):** Specifies the delay, in DRAM clocks, between the issue of a RD command and the return of valid data on the DQ bus. 0h - Not Supported 1h - 6 DRAM Clocks (DDR3-1066) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333) 4h - 9 DRAM Clocks (DDR3-1333) 5h - 10 DRAM Clocks (DDR3-1333) 6h - Not supported 7h - Reserved
11	RV	0	Reserved

Table 4-4. DRAM Timing Register 0 (DTR0) (Sheet 2 of 2)

DTR0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 01h

Bit	Attribute	Default	Description
10:8	RW	1h	**Activate (RAS) to CAS Delay (tRCD):** Specifies the delay, in DRAM clocks, between an ACT command and a RD/WR command to the same bank. 0h - Not Supported 1h - 6 DRAM Clocks (DDR3-1066) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333) 4h - 9 DRAM Clocks (DDR3-1333) 5h - 10 DRAM Clocks (DDR3-1333) 6h - Not Supported 7h - Reserved
7	RV	0	Reserved
6:4	RW	1h	**Precharge to Activate Delay (tRP):** Specifies the delay, in DRAM clocks, between a PRE command and an ACT command to the same bank. 0h - Not Supported 1h - 6 DRAM Clocks (DDR3-1066) 2h - 7 DRAM Clocks (DDR3-1066, 1333) 3h - 8 DRAM Clocks (DDR3-1066, 1333) 4h - 9 DRAM Clocks (DDR3-1333) 5h - 10 DRAM Clocks (DDR3-1333) 6h - Not Supported 7h - Reserved
3:2	RV	0	Reserved
1:0	RW	0	**DRAM Frequency (DFREQ):** Specifies the frequency used for computing proper cycle to cycle timings. It has no control on the actual DRAM CK and CKB frequency. 0h - Not Supported 1h - DDR3-1066 2h - DDR3-1333 3h - Not Supported

DTR0 identifies timing parameters used to interface with the DRAM devices. This information is based on the specifications for the populated memory devices as well as specifications driven by the system requirements. The value is not changed after initialization. The initialization complete bit is set in the DCO register.

Table 4-5. DRAM Timing Register 1 (DTR1) (Sheet 1 of 3)

DTR1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 02h

Bit	Attribute	Default	Description
31:30	RV	0	Reserved
29:28	RW	0	**Read to Precharge Delay (tRTP):** The time interval between a read and a precharge command. 0h - 4 DRAM Clocks (DDR3-1066) 1h - 5 DRAM Clocks (DDR3-1333) 2h - Not Supported 3h - Reserved
27:26	RV	0	Reserved
25:24	RW	2h	**Row Activation to Row Activation Delay (tRRD):** The minimal time interval between 2 ACT commands to any bank in the same DRAM device. Limits peak current profile. 0h - 4 DRAM Clocks 1h - 5 DRAM Clocks 2h - 6 DRAM Clocks 3h - 7 DRAM Clocks DDR3-1066 x8 devices:max (4nCK, 7.5 ns) = 4 DRAM Clocks DDR3-1066 x16 devices:max (4nCK, 10 ns) = 6 DRAM Clocks DDR3-1333 x8 devices:max (4nCK, 6 ns) = 4 DRAM Clocks DDR3-1333 x16 devices:max (4nCK, 7.5 ns) = 6 DRAM Clocks
23:20	RW	6h	**Row Activation Period (tRAS):** The minimal delay, in DRAM clocks, between ACT command and PRE command to same bank. 0h - 14 DRAM Clocks 1h - 15 DRAM Clocks 2h - 16 DRAM Clocks 3h - 17 DRAM Clocks 4h - 18 DRAM Clocks 5h - 19 DRAM Clocks 6h - 20 DRAM Clocks (DDR3-1066: tRAS = 37.5 ns) 7h - 21 DRAM Clocks 8h - 22 DRAM Clocks 9h - 23 DRAM Clocks Ah - 24 DRAM Clocks.(DDR3-1333: tRAS = 36 ns) Bh - 25 DRAM Clocks Ch - 26 DRAM Clocks Dh - 27 DRAM Clocks Eh - 28 DRAM Clocks Fh - 29 DRAM Clocks

Table 4-5. DRAM Timing Register 1 (DTR1) (Sheet 2 of 3)

DTR1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 02h

Bit	Attribute	Default	Description
19:16	RW	9h	**Four Bank Activation Window (tFAW):** A rolling time-frame, in which a maximum of 4 ACT commands (per rank) can be sent. Limits peak current profile. 0h - Reserved 1h - Reserved 2h - 14 DRAM Clocks 3h - 16 DRAM Clocks 4h - 18 DRAM Clocks 5h - 20 DRAM Clocks 6h - 22 DRAM Clocks 7h - 24 DRAM Clocks 8h - 26 DRAM Clocks 9h - 28 DRAM Clocks Ah - 30 DRAM Clocks Bh - 32 DRAM Clocks Ch - Reserved Dh - Reserved Eh - Reserved Fh - Reserved DDR3-1066 x8 devices: tFAW = 37.5 ns = 20 DRAM Clocks DDR3-1066 x16 devices: tFAW = 50.0 ns = 28 DRAM Clocks (27 not supported) DDR3-1333 x8 devices: tFAW = 30.0 ns = 20 DRAM Clocks DDR3-1333 x16 devices: tFAW = 45.0 ns = 30 DRAM Clocks
15:14	RV	0	Reserved
13:12	RW	0	**CAS to CAS delay (tCCD):** The minimum delay, in DRAM clocks, between 2 RD/WR commands. 0h - 4 DRAM Clocks. Functional mode. 1h - Reserved 2h - Reserved 3h - Reserved
11:8	RW	3h	**Write to Prechange (tWTP):** The minimum delay, in DRAM clocks, between a WR command and a PRE command to the same bank. Value is computed as 4 + tWCL + tWR. 0h - 15 DRAM Clocks 1h - 16 DRAM Clocks 2h - 17 DRAM Clocks 3h - 18 DRAM Clocks (DDR3-1067: tWCL = 6, tWR = 15 ns = 8 DRAM Clocks) 4h - 19 DRAM Clocks 5h - 20 DRAM Clocks 6h - 21 DRAM Clocks (DDR3-1333: tWCL = 7, tWR = 15 ns = 10 DRAM Clocks) 7h - 22 DRAM Clocks 8h - 23 DRAM Clocks 9h - 24 DRAM Clocks Ah - 25 DRAM Clocks
7:6	RV	0	Reserved

Table 4-5. DRAM Timing Register 1 (DTR1) (Sheet 3 of 3)

DTR1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 02h

Bit	Attribute	Default	Description
5:4	RW	2h	**Command Transport Duration (tCMD):** The time period, in DRAM clocks, that a command occupies the DRAM command bus. 1N is the DDR3 basic requirement. 2N and 3N are extended modes for board signal-integrity. 0h - 1 DRAM Clock (1N) 1h - 2 DRAM Clocks (2N) 2h - 3 DRAM Clocks (3N) 3h - Reserved
3:2	RV	0	Reserved
1:0	RW	0	**Write CAS Latency (tWCL):** The delay, in DRAM clocks, between the internal write command and the availability of the first bit of DRAM input data. 0h - Not Supported 1h - 6 DRAM Clocks (DDR3-1066) 2h - 7 DRAM Clocks (DDR3-1333) 3h - Not Supported

Table 4-6. DRAM Timing Register 2 (DTR2) (Sheet 1 of 2)

DTR2
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 03h

Bit	Attribute	Default	Description
31	RW	0	**Pre-Charge Power Down Slow Exit (PPWD_SLOWEXIT):** 0 = Fast exit from pre-charge power down is selected (MR0 A12=1) 1 = Slow exit from pre-charge power down is selected (MR0 A12=0). The following tXPDLL timer value is used to add the appropriate pre-charge power down exit latency to commands that require the DLL.
30:28	RW	0	**Exit Precharge Power Down with DLL Frozen to cOmmands Requiring a Locked DLL (tXPDLL):** 0h - 10 DDR Clocks 1h - 11 DDR Clocks 2h - 13 DDR Clocks (DDR3-1066) 3h - 14 DDR Clocks 4h - 16 DDR Clocks (DDR3-1333) 5h - 17 DDR Clocks 6h - 20 DDR Clocks 7h - 21 DDR Clocks
27:24	RW	6h	**Power Down Entry Idle Timer (PWD_DLY):** This value multiplied by 4 specifies the number of DDR clocks after the last read/write command was issued to enter power down and no other requests are pending for the rank (de-asserted CKE). Non-JEDEC delay for performance enhancement.
23:22	RW	1h	**Delay From CKE Asserted High to Any DRAM Command (tXP):** (Exit from active power down or fast exit from pre-charge power down.) 0h - Not Supported 1h - 4 DRAM Clocks (DDR3-1066, DDR3-1333) 2h - Not Supported 3h - Not Supported
21:19	RW	1h	**Write to Read Same Rank Command Delay (tWRSR):** Is set to 4 + tWCL + tWTR. 0h - 13 DRAM Clocks 1h - 14 DRAM Clocks 2h - 15 DRAM Clocks 3h - 16 DRAM Clocks 4h - 17 DRAM Clocks 5h - 18 DRAM Clocks 6h - 19 DRAM Clocks 7h - 20 DRAM Clocks
18:16	RW	2h	**Read to Write Same Rank Command Delay (tRWSR):** The minimum command separation for a BL8 read to a write to the same rank is tRWSRmin = tCL - tWCL + tCCD + 2tCK, which results in a 6 clock minimum spacing (tCCD=4) between the read/write commands when the read/write latencies are equal. The tRWSR value allows for extra command separation for board design considerations. 0h - 6 DRAM Clocks 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks 4h - 10 DRAM Clocks 5h - 11 DRAM Clocks 6h - 12 DRAM Clocks 7h - 13 DRAM Clocks
15:14	RW	3h	Reserved

Table 4-6. DRAM Timing Register 2 (DTR2) (Sheet 2 of 2)

DTR2
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 03h

Bit	Attribute	Default	Description
13:12	RW	3h	**Write to Read Different Rank Command Delay (tWRDR):** The minimum command separation for a BL8 write to a read to a different rank is tWRDRmin = tWCL - tCL + tCCD + 2tCK, which results in a 6 clock minimum spacing (tCCD=4) between the write/read commands when the write/read latencies are equal. The tWRDR value allows for extra command separation for board design considerations (not a DDR specific requirement). 0h - max(tWRDRmin, 4) 1h - tWRDRmin + 1 2h - tWRDRmin + 2 3h - tWRDRmin + 3 ***Note:*** For 0h, the minimum write command to read command spacing is limited to 4. tWRDRmin can only be 3 for DDR3-1333 10-10-10 optional speed bin. For these cases the minimum write to read different rank spacing is 4 cycles.
11:10	RW	3h	Reserved
9:8	RW	3h	**Read to Write Different Rank Command Delay (tRWDR):** The minimum command separation for a BL8 read to a write to a different rank is tRWDRmin = tCL - tWCL + tCCD + 2tCK, which results in a 6 clock minimum spacing (tCCD=4) between the read/write commands when the read/write latencies are equal. The tRWDR value allows for extra command separation for board design considerations (not a DDR specific requirement): 0h - tRWDRmin 1h - tRWDRmin + 1 2h - tRWDRmin + 2 3h - tRWDRmin + 3
7:6	RW	3h	Reserved
5:4	RW	3h	**Write to Write Different Rank Command Delay (tWWDR):** The minimum command separation for a BL8 write to a write to a different rank is tWWDRmin = 6tCK. The tWWDR value allows for extra command separation for board design considerations (not a DDR specific requirement): 0h - 6 DRAM Clocks 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks
3:2	RW	3h	Reserved
1:0	RW	3h	**Read to Read Different Rank Command Delay (tRRDR):** The minimum command separation for a BL8 read to a read to a different rank is tRRDRmin = 6tCK. The tRRDR value allows for extra command separation for board design considerations (not a DDR specific requirement): 0h - 6 DRAM Clocks 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks

Table 4-7. DRAM Timing Register 3 (DTR3) (Sheet 1 of 2)

DTR3
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 04h

Bit	Attribute	Default	Description
31:25	RV	0	Reserved
24	RW	0	**ODT Signal Configuration (two_sr_dimm):** This bit configures the ODT signals for either 1 DIMM or 2 DIMMs. 0 = The board is populated with a single DIMM, either one SR (single rank) DIMM or one DR (dual rank) DIMM. 1 = The board is populated with two SR DIMMs.
23:17	RV	0	Reserved
16	RW	0	Reserved
15	RV	0	Reserved
14:12	RW	3h	**Read Command to ODT De-Assert Delay (rdodt_stop):** Config setting is set to: RDODTSTRT+6+(WRODTSTOP-WRODTSTRT). 0h - 6 DRAM Clocks 1h - 7 DRAM Clocks 2h - 8 DRAM Clocks 3h - 9 DRAM Clocks 4h - 10 DRAM Clocks 5h - 11 DRAM Clocks 6h - 12 DRAM Clocks 7h - 13 DRAM Clocks Other - Reserved
11	RV	0	Reserved
10:8	RW	3h	**Read Command to ODT Assert Delay (rdodt_start):** Config setting is set to tCMD+tCL-tWCL-ODT_PULLIN, where ODT_PULLIN must have the same value as in WRODTSTRT. 0h - 0 DRAM Clocks 1h - 1 DRAM Clocks 2h - 2 DRAM Clocks 3h - 3 DRAM Clocks 4h - 4 DRAM Clocks 5h - 5 DRAM Clocks Other - Reserved
7	RV	0	Reserved

Table 4-7. DRAM Timing Register 3 (DTR3) (Sheet 2 of 2)

DTR3
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 04h

Bit	Attribute	Default	Description
6:4	RW	2h	**Write Command to ODT De-Assert Delay (wrodt_stop):** wrodt_stoptCMD=1NtCMD=2NtCMD=3N 0h WR+6ReservedReserved 1h WR+7WR+6Reserved 2h WR+8WR+7WR+6 3h ReservedWR+8WR+7 4h ReservedReservedWR+8 5h ReservedReservedReserved 6h ReservedReservedReserved 7h ReservedReservedReserved
3:2	RV	0	Reserved
1:0	RW	2h	**WR Command to ODT Assert Delay (wrodt_start):** For dynamic ODT in write, ODT pin is asserted with the WR command. The memory controller allows to pull-in ODT assertion by 1 clock in 2N mode and by 1 or 2 clocks in 3N mode. For most DIMM configurations, this register is programmed to same value as tCMD. A value of tCMD - ODT_PULLIN can be used according to the table below which shows the ODT command assertion with respect to the WR command assertion. wrodt_starttCMD=1NtCMD=2NtCMD=3N 0h WR+0WR-1WR-2 1h ReservedWR+0WR-1 2h ReservedReservedWR+0 3h ReservedReservedReserved

Table 4-8. DRAM Power Management Control Register 0 (DPMC0) (Sheet 1 of 2)

DPMC0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 06h

Bit	Attribute	Default	Description
31:26	RV	0	Reserved
25	RW	1	**Disable CKE Power Down States (DISPWRDN):** When set, this disables the CKE power down states; active power down and precharge power down. This does not apply to self refresh. May be used by BIOS during init flow and is set to 0 for functional mode.
24	RW	1	**Clock Gating Disabled (CLKGTDIS):** Setting this bit to 0 allows a large number of internal memory controller clocks to be gated when there is no activity in order to save power. When set to 1, internal clock-gating is disabled. 0 = Enable 1 = Disable
23	RW	0	**Dynamic Self-Refresh Enable (DYNSREN):** Setting this bit to 1, enables automatic SR command to DRAM and PM message to DDRIO when the PRI bus is idle, all pending requests have been served and the and PRI status is less than 2, SREDLY has timed-out, and all JEDEC requirements are satisfied. This register may be changed by BIOS/FW on-the-fly.
22	RV	0	Reserved
21	RW	0	**Send Precharge All Command to a Rank Before PD-Enter (PREAPWDEN):** Setting this bit to 1 allows sending a PREA command before PDE command. 0 = Disable 1 = Enable ***Note:*** The PREA command is opportunistic and may not be sent if other commands occupy the time-slot before rank enters PD.
20	RW	0	**Wake Allowed for Page Close Timeout (PCLSWKOK):** Setting this bit to 1 indicates the Memory Controller can send DRAM devices a PD-Exit command in order to close single bank if the page timer expired. ***Note:*** This bit applies only to cases where at least one other bank in the same rank is open but not timed-out. If all banks in the rank timed-out, a PD-Exit command is sent regardless of this bit. Must be set to 0 during init/training mode. 0 = Disable 1 = Enable
19	RV	0	Reserved
18:16	RW	0	**Page Close Timeout Period (PCLSTO):** Specifies the time frame, in ns, from last access to a DRAM page until that page may be scheduled for closing (by sending a PRE command). 0h - Disable page close timer (init/training) 1h - Immediate page close 2h - 30-60 ns to page close 3h - 60-120 ns to page close 4h - 120-240 ns to page close 5h - 240-480 ns to page close 6h - 480-960 ns to page close 7h - 1-2 µs to page close

Table 4-8. DRAM Power Management Control Register 0 (DPMC0) (Sheet 2 of 2)

DPMC0
MCU Private: **S12x0_PRIV_SPACE1**
Port: 01h **Offset: 06h**

Bit	Attribute	Default	Description
15:13	RV	0	Reserved
12:8	RW	0	**SPID Power Mode Opcode (PMOP):** The PM Message ID the memory controller sends to DDRIO on ispid_pm_pm bus after SR Entry command to DRAM. This message defines the DDRIO power-mode during SR period. Value can be changed on-the-fly to allow different power-modes (for example, deeper PM for S3 than for C6). Power saving and Entry/Exit latencies are described in the MODMEM HAS. Refer to CMD_PM_CONFIG0 for a description of the valid PMOP encodings.
7:0	RW	0	**Self-Refresh Entry delay (SREDLY):** The delay, in core-clocks, between PRI idle (no pending requests and PRI status is less than 2) and SR Entry when the memory controller is in Dynamic SR mode.

Table 4-9. DRAM Power Management Control Register 1 (DPMC1)

DPMC1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 07h

Bit	Attribute	Default	Description
31:22	RV	0	Reserved
21:20	RO	0h	Reserved
19:6	RV	0	Reserved
5:4	RW	1h	**Tri-State Command (TRICMD):** Tri-state command (RAS#, CAS#, WE#), address and bank address bus to DRAM. 0h - CMD/ADDR are never tristated. 1h - CMD/ADDR are tristated only when all CKE are low. 2h - CMD/ADDR are tristated when no valid command. 3h - CMD/ADDR are tristated when no valid command but may never be tristated for less than 2 DRAM clocks. This mode is only valid when tCMD is set to 0h (1N mode).
3:1	RW	0	Reserved
0	RW	1	**Tri-state Chip Selects (TRICS):** 0 = Never tri-state 1 = From SRE to SRX+tXS DDRIO may tri-state chip selects during SR.

Table 4-10. DRAM Refresh Control Register (DRFC) (Sheet 1 of 2)

DRFC
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 08h

Bit	Attribute	Default	Description
31:22	RV	0	Reserved
21	RW	0	**Clear Refresh Debit before SR Entry (REFDBTCLR):** When this bit is set, if enough REF commands are pulled-in, memory controller does not send additional REF commands before SR Entry. 0h - Disabled 1h - Enabled
20	RW	0	**Refresh Counters (REFSLOTDIS):** Refresh counters may be increased in 2 policies - skewed or simultaneously. 0h - Counters are updated per rank every ¼ tREFI. 1h - All counters are updated every tREFI.
19:18	RV	0	Reserved
17:16	RW	1h	**Refresh Max tREFI Interval (MAXtREFI):** The maximum interval between ant two REF commands per rank. JEDEC allows a maximum of 9 x tREFI intervals. 0h - 6 x tREFI 1h - 7 x tREFI 2h - 8 x tREFI 3h - 9 x tREFI. For validation only. Is not changed after initial setting.
15:14	RV	0	Reserved
13:12	RW	2h	**Refresh Period (tREFI):** Specifies the average time between sending REF commands to DRAM. The memory controller guarantees that the average time is met, but maintains a certain degree of flexibility in the exact REF scheduling in order to increase overall performance. 0h - Refresh disabled 1h - Reserved for pre-silicon simulation 2h - 3.9 µs (Extended Temperature Range, 85-95 °C) 3h - 7.8 µs (Normal Temperature Range, 0-85 °C)

Table 4-10. DRAM Refresh Control Register (DRFC) (Sheet 2 of 2)

DRFC MCU Private: Port: 01h			S12x0_PRIV_SPACE1 Offset: 08h
Bit	**Attribute**	**Default**	**Description**
11:8	RW	Ch	**Refresh Panic Watermark (REFWMPNC):** When the refresh debit counter, per rank, is greater than this value, the memory controller sends a REF command even if there are some pending requests and regardless of the PRI status level. See DDR3 specification for refresh postponing/pulling-in flexibility. May be changed to functional value after init sequence. Value is greater than, or equal, to REFWMHI. 0-5h - Reserved 6h - Allow REF command every tREFI 7h - Postpone 2 REF commands 8h - Postpone 3 REF commands 9h - Postpone 4 REF commands Ah - Postpone 5 REF commands Bh - Postpone 6 REF commands Ch - Postpone 7 REF commands Dh - Postpone 8 REF commands E-Fh - Reserved
7:4	RW	Ah	**Refresh High Watermark (REFWMHI):** When the refresh debit counter, per rank, is greater than this value, the memory controller sends a REF command even if there are some pending requests to the rank but not if the PRI status is equal to 3. See DDR3 specification for refresh postponing/pulling-in flexibility. May be changed to functional value after init sequence. Value is greater than, or equal, to REFWMLO. 0-5h - Reserved 6h - Allow REF command every tREFI 7h - Postpone 1 REF commands 8h - Postpone 2 REF commands 9h - Postpone 3 REF commands Ah - Postpone 4 REF commands Bh - Postpone 5 REF commands Ch - Postpone 6 REF commands Dh - Postpone 7 REF commands E-Fh - Reserved
3:0	RW	7h	**Opportunistic Refresh Watermark (REFWMLO):** When the refresh debit counter, per rank, is greater than this value, the memory controller sends a REF command only if there are no pending requests to the rank and the PRI status is less than 3. See DDR3 specification for refresh postponing/pulling-in flexibility. May be changed to functional value after init sequence. 0-3h - Reserved 4h - Allow pulling-in 2 REF commands 5h - Allow pulling-in 1 REF commands 6h - Allow REF command every tREFI 7h - Postpone 1 REF commands 8h - Postpone 2 REF commands 9h - Postpone 3 REF commands Ah - Postpone 4 REF commands Bh - Postpone 5 REF commands Ch - Postpone 6 REF commands Dh - Postpone 7 REF commands E-Fh - Reserved

Table 4-11. DRAM Calibration Control Register (DCAL)

DCAL
MCU Private: **S12x0_PRIV_SPACE1**
Port: 01h **Offset: 0Ah**

Bit	Attribute	Default	Description
31:14	RV	0	Reserved
13:12	RWS	1h	**ZQ Calibration Long After SR Exit Control (SRX_ZQCL):** 0h - ZQCL commands after SRX are sent in parallel. 1h - ZQCL commands are sent serially to ranks. 2h - No ZQCL is sent after SR Exit. 3h - Reserved
11	RV	0	Reserved
10:8	RWS	3h	**ZQ Calibration Short Interval (ZQCINT):** The time interval, in ms, between ZQCS commands to a DRAM device. ZQCS commands are sent to a single DRAM device and commands to ranks are distributed evenly and non-overlapping in the interval. 0h - Disabled 1h - 62 µs (for pre-silicon simulation only) 2h - 31 ms 3h - 63 ms 4h - 126 ms 5-7h - Reserved May be changed on-the-fly.
7:0	RV	0	Reserved

Table 4-12. DRAM Reset Management Control (DRMC)

DRMC
MCU Private: **S12x0_PRIV_SPACE1**
Port: 01h **Offset: 0Bh**

Bit	Attribute	Default	Description
31:17	RV	0	Reserved
16	RW	0	**Cold Wake (COLDWAKE):** The BIOS sets this bit to 1 before sending WAKE command to the memory controller after cold reset. For S3 Exit, or any other mode in which the DRAM is in SR, this bit must be set to 0.
15:13	RV	0	Reserved
12	RW	0	**ODT Control Mode (ODTMODE):** 0 = Memory Controller 1 = SW override
11:10	RV	0	Reserved
9:8	RW	0	**ODT Value (ODTVAL):** When ODTMODE is set to 1, ODT pins to DRAM are overridden by ODTVAL. Used only during init flow by BIOS.
7:0	RV	0	Reserved

Table 4-13. Power Management Status (PMSTS)

PMSTS
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 0Ch

Bit	Attribute	Default	Description
31:9	RV	0	Reserved
8	RWS	0	**Warm Reset Occurred (WRO):** Set by the power management unit whenever a reset warn is received, and cleared by powergood=0. 0h:No Warm reset occurred. 1h:Warm reset occurred. BIOS Requirement. BIOS can check and clear this bit whenever executing POST code. This way BIOS knows that if the bit is set, then DISR indicates whether DRAM entered Self-Refresh.
7:1	RV	0	Reserved
0	RW1CS	0	**DRAM In Self-Refresh (DISR):** Set by memory controller hardware after channel is placed in self refresh as a result of a power state or a reset warn sequence. Cleared by memory controller hardware before starting channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the BIOS by writing 1 in a warm reset (RESETB asserted while PWROK is asserted) exit sequence. 0 = DRAM not guaranteed to be in self-refresh 1 = DRAM in self-refresh

Table 4-14. DRAM Controller Operation Register (DCO)

DCO
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 0Fh

Bit	Attribute	Default	Description
31	RW	0	**Memory Controller Initialization Complete (IC):** This bit is set by BIOS after memory controller programming is complete and memory controller is ready to accept PRI requests and perform DRAM maintenance operations.
30	RO-V	0	**Status indication that DDRIO initialization is complete (DIOIC):** Reflects ospid_init_complete. This bit is also required to be set before the memory controller accepts requests from the internal buffer or CPGC.
29	RV	0	Reserved
28	RW	0	**PRI Control Select (PRICTL):** 0h - PRI is owned by internal buffer. 1h - PRI is owned by CPGC. Whenever this bit is toggled, the memory controller flushes all pending DRAM requests from previous owner before it accepts requests from new owner. This bit is also used when CPGC is disabled in order to gracefully flush pending request and putting DRAM into IDLE state before sending MRS commands in functional mode.
27:9	RV	0	Reserved
8	RWS-L	0	**REUT/CPGC LOCK (REUT_LOCK):** After this bit is set to 1, CPGC is locked and cannot be used. REUT_LOCK can be set only once, and is cleared by a warm reset and all other resets.
7:1	RV	0	Reserved
0	RWS-L	0	**DRP Register Lock (DRP_LOCK):** When written to 1, the DRP, DMAP0 and DMAP1 registers are locked and can not be changed.

Table 4-15. DRAM Gearing Register 0 (DGR0)

DGR0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 14h

Bit	Attribute	Default	Description
31	RW	0	**Low Latency Gearing Path Enable (GEAREN):** Enable for the all of the low latency gearing paths. 0 = Gearing is disabled. 1 = Gearing is enabled. ***Note:*** The gearing registers must be written to the appropriate value with DGR0 written last, setting the GEAREN bit before the initialization complete bit is set (DCO[31]).
30	RW	0	**Basic Gearing Configuration (BDSYNC):** Configures how the basic (non-latency sensitive) gearing is performed. 0 = Clock crossing occurs when the clock sync signal is active. 1 = Clock crossing occurs when the internal buffer/memory controller clocks align. For 1:1 gearing (BD4TO5=0) this occurs every clock cycle. For 4:5 gearing (BD4TO5=1) this occurs every 4th internal buffer clock and every 5th memory controller clock.
29:28	RW	0	**Gearing Ratio (BDRATIO):** 00 - 1:1 Gearing: DDR3-1067 10 - 4:5 Gearing: DDR3-1333 01 - Reserved 11 - Reserved
27:16	RV	0	Reserved
15:12	RW	0	**Configure Gearing Output 1 Clock Phases (D2BRQ_OUTEN1):** Configures which (internal buffer) clock phases are valid for gearing output 1. 0000 - 1:1 Gearing (DDR3-1066) 1000 - 4:5 Gearing (DDR3-1333)
11:8	RW	1h	**Configure Gearing Output 0 Clock Phases (D2BRQ_OUTEN0):** Configures which (internal buffer) clock phases are valid for gearing output 0. 0001 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)
7:4	RW	1h	**Initial Read Pointer (D2BRQ_INITPTR):** Selects the initial read pointer when gearing is enabled. 0001 - 1:1 Gearing (DDR3-1066) 0001 - 4:5 Gearing (DDR3-1333)
3:0	RW	0	**Advance Read Pointer (D2BRQ_ADVPTR):** Selects the (internal buffer) clock phases when the read pointer advances. 0000 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)

Table 4-16. DRAM Gearing Register 1 (DGR1)

DGR1
MCU Private: **S12x0_PRIV_SPACE1**
Port: 01h **Offset: 15h**

Bit	Attribute	Default	Description
31:28	RW	0	**Configure Gearing Output 1 Valid Clock Phases (D2BPM_OUTEN1):** Configures which (internal buffer) clock phases are valid for gearing output 1. 0000 - 1:1 Gearing (DDR3-1066) 0001 - 4:5 Gearing (DDR3-1333)
27:24	RW	1h	**Configure Gearing Output 0 Valid Clock Phases (D2BPM_OUTEN0):** Configures which (internal buffer) clock phases are valid for gearing output 0. 0001 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)
23:20	RW	1h	**Gearing Enabled Initial Read Pointer (D2BPM_INITPTR):** Selects the initial read pointer when gearing is enabled. 0001 - 1:1 Gearing (DDR3-1066) 1000 - 4:5 Gearing (DDR3-1333)
19:16	RW	0	**Gearing Enabled Advance Read Pointer (D2BPM_ADVPTR):** Selects the (internal buffer) clock phases when the read pointer advances. 0000 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)
15:12	RW	0	**Configure Gearing Output 1 Valid Clock Phases (D2BRD_OUTEN1):** Configures which (internal buffer) clock phases are valid for gearing output 1. 0000 - 1:1 Gearing (DDR3-1066) 1000 - 4:5 Gearing (DDR3-1333)
11:8	RW	1h	**Configure Gearing Output 0 Valid Clock Phases (D2BRD_OUTEN0):** Configures which (internal buffer) clock phases are valid for gearing output 0. 0001 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)
7:4	RW	1h	**Gearing Enabled Initial Read Pointer (D2BRD_INITPTR):** Selects the initial read pointer when gearing is enabled. 0001 - 1:1 Gearing (DDR3-1066) 0001 - 4:5 Gearing (DDR3-1333)
3:0	RW	0	**Gearing Enabled Advance Read Pointer (D2BRD_ADVPTR):** Selects the (internal buffer) clock phases when the read pointer advances. 0000 - 1:1 Gearing (DDR3-1066) 1111 - 4:5 Gearing (DDR3-1333)

Table 4-17. DRAM Gearing Register 2 (DGR2)

DGR2
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 16h

Bit	Attribute	Default	Description
31:24	RV	0	Reserved
23:20	RW	0	**Write Request Count (B2DWR_RQCNT):** Selects the number of write requests (1 cycle transfer) that the are allowed to be accepted into the memory controller ahead of the associated write data (1 or 2 cycle transfer). 1111 - 1:1 Gearing; This maximizes the pipelining, since there is no write data queue underflow issue. 0011 - 4:5 Gearing; This is the maximum allowed value for DDR3-1333 (CWL=7). 0000 - Required for any gearing ratio if out-of-order writes are enabled (DSCH[10,8]=0).
19:18	RV	0	Reserved
17:13	RW	1h	**Valid Clock Phase Configuration for Gearing Output 1 (B2DRQ_OUTEN1):** Configures which (memory controller) clock phases are valid for the gearing output. 00001 - 1:1 Gearing (DDR3-1066) 11111 - 4:5 Gearing (DDR3-1333)
12:8	RW	1h	**Valid Clock Phase Configuration for Gearing Output 0(B2DRQ_OUTEN0):** Configures which (memory controller) clock phases are valid for the gearing output. 00001 - 1:1 Gearing (DDR3-1066) 11101 - 4:5 Gearing (DDR3-1333)
7:5	RW	1h	**Gearing Enabled Initial Read Pointer (B2DRQ_INITPTR):** Selects the initial read pointer when gearing is enabled. 001 - 1:1 Gearing (DDR3-1066) 001 - 4:5 Gearing (DDR3-1333)
4:0	RW	0	**Gearing Enabled Advance Read Pointer (B2DRQ_ADVPTR):** Selects the (memory controller) clock phases when the read pointer advances. 00000 - 1:1 Gearing (DDR3-1066) 11110 - 4:5 Gearing (DDR3-1333)

Table 4-18. DRAM Address Map Register 0 (DMAP0)

DMAP0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 18h

Bit	Attribute	Default	Description
31:28	RV	0	Reserved
27:24	RWS-L	5h	**Bank Address Bit 2 Selection (BANK2SEL):** Address bit selection for bank address bit 2.
23:20	RWS-L	4h	**Bank Address Bit 1 Selection (BANK1SEL):** Address bit selection for bank address bit 1.
19:16	RWS-L	3h	**Bank Address Bit 0 Selection (BANK0SEL):** Address bit selection for bank address bit 0.
15:12	RWS-L	2h	**Column address bit 9 Selection (COL9SEL):** Address bit selection for column address bit 9.
11:8	RWS-L	1h	**Column address bit 8 Selection (COL8SEL):** Address bit selection for column address bit 8.
7:4	RWS-L	0h	**Column address bit 7 Selection (COL7SEL):** Address bit selection for column address bit 7. Below are the encodings that are used by all fields in DMAP0 and DMAP1: 0000 - A[10] 0001 - A[11] 0010 - A[12] 0011 - A[13] 0100 - A[14] 0101 - A[15] 0110 - A[16] 0111 - A[17] 1000 - A[18] 1001 - A[19] 1010 - A[20] 1011 - A[21] 1100 - A[22] 1101 - A[23] 1110 - Reserved 1111 - Reserved
3:0	RV	0	Reserved

Note: The 4-bit address selections within DMAP0 and DMAP1 must be unique; there are 14 address bit selections and 14 valid encodings. Each of the 14 valid encodings must be specified in either DMAP0 or DMAP1. The default values specify a valid configuration, where each unique valid encoding is used once and only once in the DMAP[1:0] registers. This register is locked by DCO[0].

Table 4-19. DRAM Address Map Register 1 (DMAP1)

DMAP1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 19h

Bit	Attribute	Default	Description
31:28	RWS-L	Dh	**Row address bit 7 Selection (ROW7RANKSEL):** For ADDRMAP=0 (DRP[12]) or for single rank configurations, this is used as the address bit selection for row address bit 7. The rank selection address bit for dual rank configurations is the most significant in-range address bit; for example A[32] would be used for the rank selection for an 8GB memory capacity with 2 ranks. For dual rank configurations with ADDRMAP=1, this is used as the address bit selection that determines the selected rank. Row address bit 7 is assigned the most significant in-range address bit.
27:24	RWS-L	Ch	**Row address bit 6 Selection (ROW6SEL):** Address bit selection for row address bit 6.
23:20	RWS-L	Bh	**Row address bit 5 Selection (ROW5SEL):** Address bit selection for row address bit 5.
19:16	RWS-L	Ah	**Row address bit 4 Selection (ROW4SEL):** Address bit selection for row address bit 4.
15:12	RWS-L	9h	**Row address bit 3 Selection (ROW3SEL):** Address bit selection for row address bit 3.
11:8	RWS-L	8h	**Row address bit 2 Selection (ROW2SEL):** Address bit selection for row address bit 2.
7:4	RWS-L	7h	**Row address bit 1 Selection (ROW1SEL):** Address bit selection for row address bit 1.
3:0	RWS-L	6h	**Row address bit 0 Selection (ROW0SEL):** Address bit selection for row address bit 0.

Refer to DMAP0 for the 4-bit encoding definitions. This register is locked by DCO[0].

Table 4-20. DRAM Patrol Scrub Engine Register (DSCRUB)

DSCRUB
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 1Ch

Bit	Attribute	Default	Description
31:27	RW	08h	**I/O Region Address (IORGN):** This defines the address of the I/O region below 4GB that is forward down to PCIe* space. This corresponds to A[31:27], with A[26:0] implied to be all zero. All addresses greater than or equal to IORGN and below 4 GB is skipped by the scrub engine. This is programmed to the same value as the SOCF HMBOUND[31:27].
26:21	RV	0	Reserved
20	RW	0	**Disable I/O Region (IORGNDIS):** If set, the I/O region is disabled and the patrol scrub engine simply generates a linear address. If the I/O region is enabled (IORGNDIS=0) then the patrol scrub engine adjusts all addresses greater than or equal to IORGN by adding in the size of the IORGN (4GB - IORGN). When these requests are delivered to the memory controller from the internal buffer, the I/O region has been reclaimed (original linear address before adding the I/O region size).
19:16	RV	0	Reserved
15:4	RW	11Eh	**Scrub Period (SCRUBPER):** The selected scrub period for the cache line (64B) read requests. The scrub period equals 600 core clock cycles (600 * 3.75 ns = 2.25 µsec) times the value in SCRUBPER. For example, in order to scrub 8 GB in 24 hours, the SCRUBPER is set to 011Eh (286 decimal) which results in: 8 GB * 286 * 2.25 µsec /transaction / (64B/transaction) = 86369 sec = 24 hours ***Note:*** This is the minimum time that it would take to scrub memory. This time increases if the memory controller enter self-refresh.
3:1	RO-V	0	**Current Patrol Scrub Engine State (STATE):** IDLE = 000, any other value indicates that the patrol scrub engine is active. After disabling the patrol scrub engine, BIOS/FW can read this field to ensure that the patrol scrub engine has suspended and returned to the IDLE state. This takes approximately 2.5 µsec for the patrol scrub engine to suspend after it has been disabled.
0	RW	0	**Patrol Scrub Engine Enable (SCRUBEN):** 0 = Disabled 1 = Enabled

Table 4-21. DRAM Patrol Scrub Address Register (DSADDR)

DSADDR
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 1Dh

Bit	Attribute	Default	Description
31:2	RW-V	0	**Current Scrub Address Bits (SCRUBADDR):** The current scrub address bits [35:6], which represents the physical DRAM address after the I/O region has been reclaimed; a contiguous address that ranges from 0 to the total amount of DRAM present. This register is typically written by BIOS/FW when the patrol scrub engine is disabled and idle (DSCRUB[3:0]=0) to set the patrol scrub starting address and then is updated by the patrol scrub engine while enabled with the current scrub address. If S3 is supported, BIOS/FW needs to disable the patrol scrub engine and save the current scrub address in NVM prior to entering S3. When resuming from S3, the current scrub address is restored into DSADDR and then the patrol scrub engine is re-enabled, in order to resume scrubbing from the same address where scrubbing was suspended.
1:0	RV	0	Reserved

Table 4-22. DRAM Data Scrambler Register (DSCRMBL)

DSCRMBL
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 1Eh

Bit	Attribute	Default	Description
31:17	RV	0	Reserved
16	RW	0	**Scrambling Enable (ScrambleEn):** When set to 1, the data lanes (DDR3_DQ[63:0]) and the ECC lanes (DDR3_DQECC[7:0]) are scrambled, otherwise no scrambling occurs.
15:0	WO	0	**Scrambling Key (ScrambleKey):** This is a random 16-bit value written by BIOS that is used to randomize the data scrambler seed.

Table 4-23. DRAM Status Register (DSTAT)

DSTAT
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 20h

Bit	Attribute	Default	Description
31:30	RV	0	Reserved
29:28	RO	3h	**Maximum Supported Memory (MAXMEM):** This reads the maximum supported memory.
27:0	RV	0	Reserved

Table 4-24. Sticky Scratch Pad 0 Register (SSKPD0)

SSKPD0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 4Ah

Bit	Attribute	Default	Description
31:0	RWS	0	General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

Table 4-25. Sticky Scratch Pad 1 Register (SSKPD1)

SSKPD1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 4Bh

Bit	Attribute	Default	Description
31:0	RWS	0	General Purpose Scratchpad. May be used for BIOS for data storage. Value is preserved in warm-reset.

Table 4-26. ECC and Parity Control Register (DECCCTL) (Sheet 1 of 2)

DECCCTRL
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 60h

Bit	Attribute	Default	Description
31:26	RV	0	Reserved
25	RW	0	**Clear Rank 1 Single Bit Error Counter (SBECNT1CLR):** When set, the single bit error counter for rank 1 (SBECNT1) is cleared. When this bit is cleared, SBECNT1 counts the number of single bit errors that occur on reads to rank 1.
24	RW	0	**Clear Rank 0 Single Bit Error Counter (SBECNT0CLR):** When set, the single bit error counter for rank 0 (SBECNT0) is cleared. When this bit is cleared, SBECNT0 counts the number of single bit errors that occur on reads to rank 0.
23:18	RV	0	Reserved
17	RW	0	**Generate ECC Lanes Patterns (GENECC4CPGC):** 0 = CPGC generates patterns for the ECC lanes. This mode is used during testing and training of the DDR interface. 1 = CPGC generates only the data lane patterns and correct ECC is generated by the memory controller. This mode is used when the CPGC engine is used initialize (zero) the contents of memory prior to booting the OS.
16	RW	0	**ECC Override Enable (ECCOVREN):** 0 = Normal ECC is generated. 1 = ECC override enabled, the value in ECCOVR is used for the ECC code.
15:8	RW	0	**ECC Override (ECCOVR):** ECC override code to be used on writes if enabled by ECCOVREN.
7:5	RW	0	**Filter Uncorrectable Error (UCE_FILTER):** x00 - Normal mode; All 8 byte ECC checks/corrections are performed independently, no anti-aliasing filters are applied. 001 - First-level filter mode; An uncorrectable error that is detected in any 8 byte ECC check causes all four parallel 8 byte ECC checks to be treated as uncorrectable errors. x10 - Second-level filter mode; In addition to level 1, any two or more of the 8 byte ECC checks that result in correctable errors from different x8 devices cause all four parallel 8 byte ECC checks to be treated as uncorrectable errors. x11 - Third-level filter; In addition to levels 1 and 2, any two or more of the 8 byte ECC checks that result in correctable errors from different bit lanes cause all four parallel 8 byte ECC checks to be treated as uncorrectable errors. 1xx - Address bit 4 (column address bit 1) failure filter enable. A4 is intended to always be 0, so an error on A4 would be a 1 if/when it occurs. With the data scrambler this type of error leads to a few cases where the expect/actual scramble code differences that result in either all four bursts aliasing to a correctable error in the same bit lane, or just the even bursts aliasing to a correctable error in the same bit lane and the odd bursts aliasing to no error (or vice versa). ***Note:*** A3 (column address bit 0) does not cause the same type of error as A4 as long as the DRAM devices are programmed for sequential address order instead of interleaved address order (MR0 A3=0).
4	RW	0	**Enable Data Path Parity (DPAREN):** When set, data path parity is enabled. The write data parity is checked at the point when ECC is generated and read data parity is generated at the point that ECC is checked.
3	RW	0	Reserved

Table 4-26. ECC and Parity Control Register (DECCCTL) (Sheet 2 of 2)

DECCCTRL
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 60h

Bit	Attribute	Default	Description
2	RW	0	**Signal Uncorrectable ECC Errors (DERREN):** When set, uncorrectable ECC errors are signalled to the internal buffer.
1	RW	0	**Signal correctable ECC Errors (SERREN):** When set, correctable ECC errors are signalled to the internal buffer which indicates that the read data needs to be written back to memory. This causes the DRAM cell with the single bit error to be scrubbed.
0	RW	0	**ECC Enable (ECCEN):** When set, single bit error correction and double bit error detection (SEC/DED ECC) is enabled. The ECC is an 8 bit protection code for every 64 bits of data stored in DRAM. ECC is generated on writes and checked on reads, requiring a 72 bit DDR3 data bus width.

Table 4-27. First Error and Next Error Register (FERRNERR)

FERRNERR
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 61h

Bit	Attribute	Default	Description
31:20	RV	0	Reserved
19	ROS-V	0	**First Error Detected is Parity Error (FERRWPE):** When set, the first error detected was a parity error on the write data received from the internal buffer.
18	ROS-V	0	Reserved
17	ROS-V	0	**First Error Detected is Uncorrectable Error (FERRUCE):** When set, the first error detected was an uncorrectable error.
16	ROS-V	0	**First Error Detected is Single Bit Error (FERRSBE):** When set, the first error detected was a single bit error and the error was corrected.
15:4	RV	0	Reserved
3	ROS-V	0	**Second Error Detected is Parity Error (NERRWPE):** When set, the second error detected was a parity error on the write data received from the internal buffer.
2	ROS-V	0	Reserved
1	ROS-V	0	**Second Error Detected is Uncorrectable Error (NERRUCE):** When set, the second error detected was an uncorrectable error.
0	ROS-V	0	**Second Error Detected is Single Bit Error (NERRSBE):** When set, the second error detected was a single bit error and the error was corrected.

Table 4-28. Single Bit Error Logging Register (SBELOG)

SBELOG
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 62h

Bit	Attribute	Default	Description
31:21	RV	0	Reserved
20	ROS-V	0	**Single-Bit Error Rank Address (SBERNK):** The rank address of the single bit error.
19	RV	0	Reserved
18:16	ROS-V	0	**Single-Bit Error Bank Address (SBEBNK):** The bank address of the single bit error.
15	RV	0	Reserved
14	ROS-V	0	**Single-Bit Error Last Burst (SBELAST):** If this bit is set, then the error occurred within that last four DQ bus bursts before a DQ bus turn-around cycle.
13	ROS-V	0	**Single-Bit Error First Burst (SBEFIRST):** If this bit is set, then the error occurred within the first four DQ bus bursts after a DQ bus turn-around cycle.
12	ROS-V	0	**Address Bit 5 of Original Request (SBEA5):** This is address[5] from the original request.
11	ROS-V	0	**Single-Bit Error on Read Size (SBEBL8):** 0 = The single bit error was encountered on a 32B read (BC4). 1 = The single bit error was encountered on a 64B read (BL8).
10:8	ROS-V	0	**Single-Bit Error Burst Offset (SBEBOFF):** The burst offset of the single bit error.
7:0	ROS-V	0	**Single-Bit Error Syndrome (SBESYND):** Single-bit error syndrome captured when DERRSTS-SBE is set.

Table 4-29. Uncorrectable Read Error Logging Register (UCELOG)

UCELOG
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 63h

Bit	Attribute	Default	Description
31:21	RV	0	Reserved
20	ROS-V	0	**Uncorrectable Error Rank Address (UCERNK):** The rank address of the uncorrectable error.
19	RV	0	Reserved
18:16	ROS-V	0	**Uncorrectable Error Bank Address (UCEBNK):** The bank address of the uncorrectable error.
15	RV	0	Reserved
14	ROS-V	0	**Uncorrectable Error Last Burst (UCELAST):** If this bit is set, then the error occurred within that last four DQ bus bursts before a DQ bus turn-around cycle.
13	ROS-V	0	**Uncorrectable Error First Burst (UCEFIRST):** If this bit is set, then the error occurred within the first four DQ bus bursts after a DQ bus turn-around cycle.
12	ROS-V	0	**Address Bit 5 of Original request (UCEA5):** This is address[5] from the original request.
11	ROS-V	0	**Uncorrectable Error on Read Size (UCEBL8):** 0 = The uncorrectable error was encountered on a 32B read (BC4). 1 = The uncorrectable error was encountered on a 64B read (BL8).
10:8	ROS-V	0	**Uncorrectable Error Burst Offset (UCEBOFF):** The burst offset of the uncorrectable error.
7:0	ROS-V	0	**Uncorrectable Error Syndrome (UCESYND):** Uncorrectable error syndrome captured when DERRSTS-UCE is set.

This register logs information associate with the first uncorrectable read error, which occurs when either DERRSTS[2] or DERRSTS[1] get set to a 1.

Table 4-30. Rank 0 Single Bit Error Count (SBECNT0)

SBECNT0
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 64h

Bit	Attribute	Default	Description
31:0	RO-V	0	Single-bit error count for rank 0. This count is cleared by writing a 1 to DECCCTL[24].

Table 4-31. Rank 1 Single Bit Error Count (SBECNT1)

SBECNT1
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 65h

Bit	Attribute	Default	Description
31:0	RO-V	0	Single-bit error count for rank 1. This count is cleared by writing a 1 to DECCCTL[25].

Table 4-32. Single Bit Error Accumulator Register (SBEACC)

SBEACC
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 68h

Bit	Attribute	Default	Description
31:25	RV	0	Reserved
24:16	RW1CS	0	Rank 1 9 byte lanes single-bit error accumulator (SBER1B[8:0])
15:9	RV	0	Reserved
8:0	RW1CS	0	Rank 0 9 byte lanes single-bit error accumulator (SBER0B[8:0])

Table 4-33. Error Status Register (DERRSTS)

DERRSTS
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 6Ah

Bit	Attribute	Default	Description
31:4	RV	0	Reserved
3	RW1CS	0	**Detect Uncorrectable Write Data Parity Error (WPE):** When set, the an uncorrectable write data parity error was detected.
2	RW1CS	0	Reserved
1	RW1CS	0	**Detect Uncorrectable Read Data Parity Error (UCE):** When set, an uncorrectable error was detected in the read data.
0	RW1CS	0	**Detect Single-Bit Correctable Read Data Parity Error (SBE):** When set, a single-bit (correctable) error was detected in the read data.

Table 4-34. Error Mask and Severity Register (DERRMSKSEV)

DERRMSKSEV
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 6Bh

Bit	Attribute	Default	Description
31:20	RV	0	Reserved
19	RWS	0	**Mask Uncorrectable Write Data Parity Errors (MSK_WPE):** When set, uncorrectable Write Data Parity (WPE) errors are not logged in DERRSTS.
18	RWS	0	Reserved
17	RWS	0	**Mask Uncorrectable Errors (MSK_UCE):** When set, Uncorrectable Errors (UCE) are not logged in DERRSTS.
16	RWS	0	**Mask Single-Bit Correctable Errors (MSK_SBE):** When set, single-bit (correctable) errors are not logged in DERRSTS.
15:4	RV	0	Reserved
3	RWS	0	**Severity of Write Data Parity Errors (SEV_WPE):** When set, WPE errors logged in DERRSTS[3] are escalated to the global error logic as a fatal error; otherwise, it is escalated as a non-fatal error.
2	RWS	0	Reserved
1	RWS	0	**Severity of Uncorrectable Errors (SEV_UCE):** When set, UCE errors logged in DERRSTS[1] are escalated to the global error logic as a fatal error; otherwise, it is escalated as a non-fatal error.
0	RV	0	Reserved

Table 4-35. Uncorrectable Error Count Selection Register (DERRCNTSEL)

DERRCNTSEL
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 6Ch

Bit	Attribute	Default	Description
31:4	RV	0	Reserved
3	RWS	0	**Count Write Data Parity Errors (CNTSEL_WPE):** When set, WPE errors logged in DERRSTS[3] are counted in DERRCNT.
2	RWS	0	Reserved
1	RWS	0	**Count Uncorrectable Errors (CNTSEL_UCE):** When set, UCE errors logged in DERRSTS[1] are counted in DERRCNT.
0	RV	0	Reserved

Table 4-36. Uncorrectable Error Count Register (DERRCNT)

DERRCNT
MCU Private: S12x0_PRIV_SPACE1
Port: 01h Offset: 6Dh

Bit	Attribute	Default	Description
31:8	RV	0	Reserved
7:0	RW1CS	0	**Uncorrectable Error Count (UNCCNT):** The count of uncorrectable errors that have occurred since the last time the count was cleared. The count limit is 128 (80h) and the count is cleared by writing ones to all bits (FFh). The type of uncorrectable errors that are counted is determined by the DERRCNTSEL register.

4.2 RAS Registers

Table 4-37. Register Summary (Sheet 1 of 2)

Offset (h)	Size (bits)	Name
00	16	“Vendor Identification Register (VID)” on page 272
02	16	“Device Identification Register (DID)” on page 272
04	16	“PCI Command Register (PCICMD)” on page 273
06	16	“PCI Status Register (PCISTS)” on page 274
08	8	“Revision Identification Register (RID)” on page 274
09	24	“Class Code Register (CC)” on page 274
0C	8	“Cacheline Size Register (CLS)” on page 275
0E	8	“Header Type Register (HDR)” on page 275
2C	16	“Subsystem Vendor ID Register (SVID)” on page 275
2E	16	“Subsystem ID Register (SID)” on page 275
34	8	“Capabilities Pointer Register (CAPPTR)” on page 275
3C	8	“Interrupt Line Register (INTL)” on page 276
3D	8	“Interrupt Pin Register (INTP)” on page 276
40	16	“PCI Express Capability List Register (EXPCAPLST)” on page 276
42	16	“PCI Express Capabilities Register (EXPCAP)” on page 276
44	32	“Device Capabilities Register (DEVCAP)” on page 277
48	16	“Device Control Register (DEVCTL)” on page 278
4A	16	“Device Status Register (DEVSTS)” on page 279
4C	32	“Link Capabilities Register (LINKCAP)” on page 280
50	16	“Link Control Register (LINKCTL)” on page 281
52	16	“Link Status Register (LINKSTS)” on page 281
5C	16	“Root Control Register (ROOTCTL)” on page 282
80	16	“Power Management Capability List Register (PMCAPLST)” on page 282
82	16	“Power Management Capabilities Register (PMCAP)” on page 282
84	16	“Power Management Control / Status Register (PMCSR)” on page 283
90	16	“MSI Capability List Register (MSICAPLST)” on page 283
92	16	“MSI Message Control Register (MSICTL)” on page 283
94	32	“MSI Message Address Register (MSIADDR)” on page 284
98	32	“MSI Message Data Register (MSIDATA)” on page 284
100	32	“Advanced Error Reporting Extended Capability Header (AERCAPHDR)” on page 284
104	32	“Uncorrectable Error Status Register (ERRUNCSTS)” on page 285
108	32	“Uncorrectable Error Mask Register (ERRUNCMSK)” on page 285
10C	32	“Uncorrectable Error Severity Register (ERRUNCSEV)” on page 286
110	32	“Correctable Error Status Register (ERRCORSTS)” on page 287
114	32	“Correctable Error Mask Register (ERRCORMSK)” on page 287
118	32	“Advanced Error Capabilities and Control Register (AERCAPCTL)” on page 288
130	32	“Root Error Status Register (ROOTERRSTS)” on page 288
150	32	“Root Complex Event Collector Endpoint Association Extended Capability Header (RCECEPACAPHDR)” on page 289

Table 4-37. Register Summary (Sheet 2 of 2)

Offset (h)	Size (bits)	Name
154	32	"Association Bitmap for Root Complex Integrated Endpoints Register (ABMRCIEP)" on page 290
200	32	"Global Correctable Error Status Register (GCORERRSTS)" on page 290
204	32	"Global Nonfatal Error Status Register (GNERRSTS)" on page 291
208	32	"Global Fatal Error Status Register (GFERRSTS)" on page 291
20C	32	"Global Error Mask Register (GERRMSK)" on page 292
210	32	"Global Correctable FERR Status Register (GCORFERRSTS)" on page 292
214	32	"Global Correctable NERR Status Register (GCORNERRSTS)" on page 293
218	32	"Global Non-Fatal FERR Status Register (GNFERRSTS)" on page 293
21C	32	"Global Nonfatal NERR Status Register (GNNERRSTS)" on page 294
220	32	"Global Fatal FERR Status Register (GFFERRSTS)" on page 294
224	32	"Global Fatal NERR Status Register (GFNERRSTS)" on page 295
228	64	"Global Error Timer Register (GTIME)" on page 295
230	64	"Global Correctable FERR Error Time Stamp Register (GCORFERRTIME)" on page 295
238	64	"Global Nonfatal FERR Error Time Stamp Register (GNFERRTIME)" on page 295
240	64	"Global Fatal FERR Error Time Stamp Register (GFFERRTIME)" on page 296
248	32	"Global System Event Status Register (GSYSEVTSTS)" on page 296
24C	32	"Global System Event Mask Register (GSYSEVTMSK)" on page 296
250	32	"Global System Event Map Register (GSYSEVTMAP)" on page 297
254	32	"Error Pin Control Register (ERRPINCTRL)" on page 298
258	32	"Error Pin Status Register (ERRPINSTS)" on page 298
25C	32	"Error Pin Data Register (ERRPINDATA)" on page 299

Table 4-38. Vendor Identification Register (VID)

VID **Bus: 0** **Device: 14** **Function: 0** **Offset: 00h**			
Bit	**Attribute**	**Default**	**Description**
15:0	RO	8086h	**Vendor ID (VID):** This field identifies Intel as the manufacturer of the device.

Table 4-39. Device Identification Register (DID)

DID **Bus: 0** **Device: 14** **Function: 0** **Offset: 02h**			
Bit	**Attribute**	**Default**	**Description**
15:0	RO	0C54h	**Device ID (DID):** This field identifies the RAS Unit as allocated by Intel.

Table 4-40. PCI Command Register (PCICMD)

PCICMD Bus: 0	Device: 14	Function: 0	Offset: 04h
Bit	**Attribute**	**Default**	**Description**
15:11	RO	00h	Reserved
10	RW	0b	**Interrupt Disable (INTxD):** This disables pin-based INTx# interrupts on enabled Hot-Plug and power management events. This bit has no affect on MSI operation. 0 = Internal INTx# messages are generated if there is an interrupt for Hot-Plug or power management and MSI is not enabled. 1 = Internal INTx# messages are not generated. This bit does not affect interrupt forwarding from devices connected to the root port. Assert_INTx and Deassert_INTx messages are still forwarded to the internal interrupt controllers if this bit is set.
9	RO	0b	**Fast Back-to-back enable (FBE):** Not supported. Hardwired to 0.
8	RW	0b	**SERR# Enable (SEE):** 0 = Disable. 1 = Enables the root port to generate an SERR# message when PSTS.SSE is set.
7	RO	0b	**Wait Cycle Control (WCC):** Not supported. Hardwired to 0.
6	RW	0b	**Parity Error Response Enable (PERE):** 0 = Disable. 1 = Indicates that the device is capable of reporting parity errors as a master on the backbone.
5	RO	0b	**VGA Palette Snoop Enable (VGA_PSE):** Not supported. Hardwired to 0.
4	RO	0b	**Memory Write and Invalidate Enable (MWIE):** Not supported. Hardwired to 0.
3	RO	0b	**Special Cycle Enable (SCE):** Not supported. Hardwired to 0.
2	RW	0b	**Bus Master Enable (BME):** 0 = Disable. Memory and I/O requests received at a root port must be handled as unsupported requests. 1 = Enable. Allows the root port to forward cycles onto the backbone from a PCI Express* device. ***Note:*** This bit does not affect forwarding of completions in either upstream or downstream direction nor controls forwarding of requests other than memory or I/O PCI Express.
1	RO	0b	**Memory Space Enable (MSE):** 0 = Disable. Memory cycles within the range specified by the memory base and limit registers are master aborted on the backbone. 1 = Enable. Allows memory cycles within the range specified by the memory base and limit registers can be forwarded to the PCI Express* device.
0	RO	0b	**I/O Space Enable (IOSE):** This bit controls access to the I/O space registers. 0 = Disable. I/O cycles within the range specified by the I/O base and limit registers are master aborted on the backbone. 1 = Enable. Allows I/O cycles within the range specified by the I/O base and limit registers can be forwarded to the PCI Express* device.

Table 4-41. PCI Status Register (PCISTS)

PCISTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 06h**

Bit	Attribute	Default	Description
15	RW1C	0b	**Detected Parity Error (DPE):** 0 = No parity error detected. 1 = Set when the root port receives a command or data from the backbone with a parity error. This is set even if PCIMD.PER is not set.
14	RW1C	0b	**Signaled System Error (SSE):** 0 = No system error signaled. 1 = Set when the root port signals a system error to the internal SERR# logic.
13	RO	0b	**Received Master Abort (RMA):** Not supported. Hardwired to 0.
12	RO	0b	**Received Target Abort (RTA):** Not supported. Hardwired to 0.
11	RO	0b	**Signaled Target Abort (STA):** Not supported. Hardwired to 0.
10:9	RO	00b	**DEVSEL# Timing (DVT):** Not supported. These bits are hardwired to 0.
8	RO	0b	**Master Data Parity Error Detected (MDPD):** Not supported. Hardwired to 0.
7	RO	0b	**Fast Back-to-Back Capable (FBC):** Not supported. Hardwired to 0.
6	RV	0b	Reserved
5	RO	0b	**66 MHz Capable (C66):** Not supported. Hardwired to 0.
4	RO	1b	**Capabilities List Enable (CAPE):** Hardwired to 1. Indicates the presence of a capabilities list.
3	RO-V	0b	**Interrupt Status (INTS):** Indicates status of Hot-Plug and power management interrupts on the root port that result in INTx# message generation. 0 = Interrupt is deasserted. 1 = Interrupt is asserted. This bit is not set if MSI is enabled. If MSI is not enabled, this bit is set regardless of the state of PCICMD.Interrupt Disable bit.
2:0	RV	0h	Reserved

Table 4-42. Revision Identification Register (RID)

RID
Bus: 0 **Device: 14** **Function: 0** **Offset: 08h**

Bit	Attribute	Default	Description
7:0	ROS-V	00h	**Revision ID (RID):** This field specifies the specific revision of this function and is viewed as a extension to the Device ID.

Table 4-43. Class Code Register (CC)

CC
Bus: 0 **Device: 14** **Function: 0** **Offset: 09h**

Bit	Attribute	Default	Description
23:16	RO	08h	**Base Class (BC)**
15:8	RO	06h	**Sub-Class (SC):** Root Complex Event Collector
7:0	RO	00h	**Register-Level Programming Interface (RLPI)**

Table 4-44. Cacheline Size Register (CLS)

CLS
Bus: 0 **Device: 14** **Function: 0** **Offset: 0Ch**

Bit	Attribute	Default	Description
7:0	RW	00h	**Cache Line Size (CLS):** This is read/write but contains no functionality, per the *PCI Express* Base Specification*.

Table 4-45. Header Type Register (HDR)

HDR
Bus: 0 **Device: 14** **Function: 0** **Offset: 0Eh**

Bit	Attribute	Default	Description
7	RO	0b	**Multi-function device (MFD):** 0 = Single-function device. 1 = Multi-function device
6:0	RO	00h	**Header Type (HTYPE):** These bits define the layout of addresses 10h through 3Fh in the configuration space.

Table 4-46. Subsystem Vendor ID Register (SVID)

SVID
Bus: 0 **Device: 14** **Function: 0** **Offset: 2Ch**

Bit	Attribute	Default	Description
15:0	RW-O	8086h	**Subsystem Vendor ID (SVID):** This field identifies Intel as the manufacturer of the device.

Table 4-47. Subsystem ID Register (SID)

SID
Bus: 0 **Device: 14** **Function: 0** **Offset: 2Eh**

Bit	Attribute	Default	Description
15:0	RW-O	0000h	**Subsystem ID (SID):** This field identifies the particular function as allocated by Intel.

Table 4-48. Capabilities Pointer Register (CAPPTR)

CAPPTR
Bus: 0 **Device: 14** **Function: 0** **Offset: 34h**

Bit	Attribute	Default	Description
7:0	RO	40h	**Capabilities Pointer (CPTR):** Indicates that the pointer for the first entry in the capabilities list is at 40h in configuration space.

Table 4-49. Interrupt Line Register (INTL)

INTL **Bus: 0** **Device: 14** **Function: 0** **Offset: 3Ch**			
Bit	**Attribute**	**Default**	**Description**
7:0	RW	00h	**Interrupt Line (INTL):** Software written value to indicate which interrupt line (vector) the interrupt is connected to. No hardware action is taken on this register. These bits are not reset by FLR.

Table 4-50. Interrupt Pin Register (INTP)

INTP **Bus: 0** **Device: 14** **Function: 0** **Offset: 3Dh**			
Bit	**Attribute**	**Default**	**Description**
7:0	RO	01h	**Interrupt Pin (INTP):** As a single function device, this device specifies INTA as its interrupt pin.

Table 4-51. PCI Express Capability List Register (EXPCAPLST)

EXPCAPLST **Bus: 0** **Device: 14** **Function: 0** **Offset: 40h**			
Bit	**Attribute**	**Default**	**Description**
15:8	RO	80h	**Next Pointer (NP):** Value of 80h indicates the location of the next pointer.
7:0	RO	10h	**Capability ID (CAPID):** Identifies the function as PCI Express* capable.

Table 4-52. PCI Express Capabilities Register (EXPCAP)

EXPCAP **Bus: 0** **Device: 14** **Function: 0** **Offset: 42h**			
Bit	**Attribute**	**Default**	**Description**
15:14	RV	0h	Reserved
13:9	RO	0h	**Interrupt Message Number (IMN):** Does not have multiple MSI interrupt numbers. Hardwired to 0.
8	RO	0	**Slot Implemented (SI):** Indicates no slot is connected. Hardwired to 0.
7:4	RO	Ah	**Device/Port Type (DT):** Value of 1010b indicates Root Complex Event Collector.
3:0	RO	2h	**Version Number (VN):** Indicates PCI Express* 2.0.

Table 4-53. Device Capabilities Register (DEVCAP)

DEVCAP
Bus: 0 **Device: 14** **Function: 0** **Offset: 44h**

Bit	Attribute	Default	Description
31:29	RV	0h	Reserved
28	RO	0b	**Function Level Reset Capability (FLR):** Not applicable. Hardwired to 0.
27:26	RO	00b	**Captured Slot Power Limit Scale (CSPLS):** Not applicable. Hardwired to 0.
25:18	RO	0h	**Captured Slot Power Limit Value (CSPLV):** Not applicable. Hardwired to 0.
17:16	RV	00b	Reserved
15	RO	0b	**Role-Based Error Reporting (RBER):** Not supported. Hardwired to 0.
14:12	RO	0h	Undefined
11:9	RO	000b	**Endpoint L1 Acceptable Latency (EPL1AL):** L1 ASPM is not supported. These bits are hardwired to 0.
8:6	RO	000b	**Endpoint L0s Acceptable Latency (EPL0AL):** The least latency possible out of L0s is supported. Hardwired to 0.
5	RO	0b	**Extended Tag Field Supported (ETFS):** Only a 5-bit tag is supported. Hardwired to 0.
4:3	RO	00b	**Phantom Functions Supported (PFS):** Not supported. Hardwired to 0.
2:0	RO	001b	**Max Payload Size Supported (MPSS):** Indicates the maximum payload size supported is 256B.

Table 4-54. Device Control Register (DEVCTL)

DEVCTL
Bus: 0 Device: 14 Function: 0 Offset: 48h

Bit	Attribute	Default	Description
15	RV	0b	Reserved
14:12	RO	000b	**Max_Read_Request_Size (MRRS):** Indicates maximum read request size. The S12x0 RAS supports max read request size of 128 bytes or lower.
11	RO	0b	**Enable No Snoop (ENOSNP):** Not supported. Hardwired to 0.
10	RO	0b	**Auxiliary Power PM Enable (AUXPME):** Not supported. Hardwired to 0.
9	RO	0b	**Phantom Function Enable (PFE):** Not supported. Hardwired to 0.
8	RO	0b	**Extended Tag Field Enable (ETFE):** Not supported. Hardwired to 0.
7:5	RW	000b	**Maximum Payload Size (MPS):** Indicates maximum TLP payload size of 128 bytes for the S12x0 RAS.
4	RO	0b	**Enable Relaxed Ordering (ENRO):** Not supported. Hardwired to 0.
3	RW	0b	**Unsupported Request Reporting Enable (URRE):** 0 = The root port ignores unsupported request errors. 1 = Allows signaling ERR_NONFATAL, ERR_FATAL, or ERR_COR to the Root Control register when detecting an unmasked Unsupported Request (UR). An ERR_COR is signaled when a unmasked advisory non-fatal UR is received. An ERR_FATAL, ERR_or NONFATAL, is sent to the Root Control Register when an uncorrectable non-advisory UR is received with the severity set by the Uncorrectable Error Severity register.
2	RW	0b	**Fatal Error Reporting Enable (FERE):** 0 = The root port ignores fatal errors. 1 = Enables signaling of ERR_FATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
1	RW	0b	**NonFatal Error Reporting Enable (NFERE):** 0 = The root port ignores non-fatal errors. 1 = Enables signaling of ERR_NONFATAL to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.
0	RW	0b	**Correctable Error Reporting Enable (CERE):** 0 = The root port ignores correctable errors. 1 = Enables signaling of ERR_CORR to the Root Control register due to internally detected errors or error messages received across the link. Other bits also control the full scope of related error reporting.

Table 4-55. Device Status Register (DEVSTS)

DEVSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 4Ah**

Bit	Attribute	Default	Description
15:6	RV	000h	Reserved
5	RO	0b	**Transactions Pending (TP):** RAS unit does not issue non-posted requests. Hardwired this bit to 0b.
4	RO	0b	**Auxiliary Power Detected (APD):** Auxiliary Power is not supported.
3	RW1C	0b	**Unsupported Request Detected (URD):** Indicates an unsupported request was detected.
2	RW1C	0b	**Fatal Error Detected (FED):** Indicates a fatal error was detected. 0 = Fatal has not occurred. 1 = A fatal error occurred from a data link protocol error, link training error, buffer overflow, or malformed TLP.
1	RW1C	0b	**Non-Fatal Error Detected (NFED):** Indicates a non-fatal error was detected. 0 = Non-fatal has not occurred. 1 = A non-fatal error occurred from a poisoned TLP, unexpected completions, unsupported requests, completer abort, or completer timeout.
0	RW1C	0b	**Correctable Error Detected (CED):** Indicates a correctable error was detected. 0 = Correctable has not occurred. 1 = The port received an internal correctable error from receiver errors/framing errors, TLP CRC error, DLLP CRC error, replay num rollover, replay timeout.

Table 4-56. Link Capabilities Register (LINKCAP)

LINKCAP
Bus: 0 **Device: 14** **Function: 0** **Offset: 4Ch**

Bit	Attribute	Default	Description
31:24	RO	00h	**Port Number (PN):** This field indicates the PCI Express* port number assigned to the RAS Unit.
23:21	RV	00b	Reserved
20	RO	0b	**Data Link Layer Active Error Reporting Capable (DLLERC)**: Not supported. Hardwired to 0.
19	RO	0b	**Surprise Link Down Error Reporting Capable (SLDERC)**: Not supported. Hardwired to 0.
18	RO	0b	**Clock Power Management Capable (CPMC)**: Not supported. Hardwired to 0.
17:15	RO	000b	**L1 Exit Latency(L1EL):** This field indicates the L1 exit latency for the given PCI Express Link. It indicates the length of time this port requires to complete transition from L1 to L0. 000: Less than 1 µs 001: 1 µs to less than 2 µs 010: 2 µs to less than 4 µs 011: 4 µs to less than 8 µs 100: 8 µs to less than 16 µs 101: 16 µs to less than 32 µs 110: 32 µs to less than 64 µs 111: More than 64 µs
14:12	RO	000b	**L0s Exit Latency(L0sEL):** This field indicates the L0s exit latency for the given PCI Express Link. It indicates the length of time this port requires to complete transition from L0s to L0. 000b: Less than 64 ns 001b: 64 ns to less than 128 ns 010b: 128 ns to less than 256 ns 011b: 256 ns to less than 1 µs 101b: 1 µs to less than 2 µs 110b: 2 µs to less than 4 µs 111b: More than 4 µs
11:10	RO	11b	**ASPM Support (ASPMSUP):** This field indicates the level of ASPM supported on the given PCI Express Link. 00b: Reserved 01b: L0s Entry Supported 10b: Reserved 11b: L0s and L1 Supported
9:4	RO	01h	**Maximum Link Width (MLW):** This field indicates the maximum link width of x1 implemented by the RAS PCI Express Link.
3:0	RO	1h	**Maximum Link Speed (MLS):** This field indicates the 2.5 Gb/s supported link speed for the RAS PCIE port.

Table 4-57. Link Control Register (LINKCTL)

LINKCTL
Bus: 0 Device: 14 Function: 0 Offset: 50h

Bit	Attribute	Default	Description
15:10	RV	0h	Reserved
9	RO	0b	**Hardware Autonomous Width Disable (HAWD)**: Hardwire this bit to 0b.
8	RO	0b	**Enable Clock Power Management (ECPM)**: Not Applicable. Hardwired to 0.
7	RW	0b	**Extended Synch (ES):** 0 = Extended synch disabled. 1 = Forces extended transmission of FTS ordered sets in FTS and extra TS2 at exit from L1 prior to entering L0.
6	RW	1b	**Common Clock Configuration (CCCFG):** 0 = The S12x0 and device are not using a common reference clock. 1 = The S12x0 and device are operating with a distributed common reference clock.
5	RO	0b	**Retrain Link (RL):** When set, this bit initiates link retraining by directing the physical layer LTSSM to recovery state. If the LTSSM is already in recovery or configuration, re-entering recovery is permitted but not required. Reads of this bit always return 0b.
4	RO	0b	**Disable Link (DL):** 0 = Link enabled. 1 = The root port disables the link.
3	RO	0b	**Read Completion Boundary (RCB):** This bit indicates 64 byte RCB value for RAS Unit.
2	RV	0b	Reserved
1:0	RW	00b	**ASPM Control (ASPMCTL):** Indicates whether the RAS port enters L0s or L1 or both. 00b: Disabled 01b: L0s Entry Enabled 10b: L1 Entry Enabled 11b: L0s and L1 Entry Enabled

Table 4-58. Link Status Register (LINKSTS)

LINKSTS
Bus: 0 Device: 14 Function: 0 Offset: 52h

Bit	Attribute	Default	Description
15:14	RO	0b	Reserved
13	RO	0b	**Data Link Layer Link Active (DLLLA):** Hardwire this bit to 0b.
12	RO	1b	**Slot Clock Configuration (SCC):** Set to 1b to indicate that the S12x0 uses the same reference lock as on the platform and does not generate its own clock.
11	RO	0	**Link Training (LT):** Not supported. Hardwire this bit to 0b.
10	RO	0	Reserved
9:4	RO	1h	**Negotiated Link Width (NLW):** This field indicates the negotiated width of x1 for the PCI Express link.
3:0	RO	1h	**Current Link Speed (CLS):** This field indicates the negotiated link speed of 2.5 Gb/s PCI Express link.

Table 4-59. Root Control Register (ROOTCTL)

ROOTCTL
Bus: 0 Device: 14 Function: 0 Offset: 5Ch

Bit	Attribute	Default	Description
15:4	RV	0	Reserved
3	RO	0	**PME Interrupt Enable (PMEIE):** Not supported. Hardwire this bit to 0b.
2	RW	0	**System Error on Fatal Error Enable (SEFEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming CMD.SEE is set, if a fatal error is reported by any of the devices in the hierarchy of the RAS port, including fatal errors in the RAS port.
1	RW	0	**System Error on Non-Fatal Error Enable (SENFEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming CMD.SEE is set, if a non-fatal error is reported by any of the devices in the hierarchy of the RAS port, including non-fatal errors in the RAS port.
0	RW	0	**System Error on Correctable Error Enable (SECEE):** 0 = An SERR# is not generated. 1 = An SERR# is generated, assuming CMD.SEE if a correctable error is reported by any of the devices in the hierarchy of the RAS port, including correctable errors in the RAS port.

Table 4-60. Power Management Capability List Register (PMCAPLST)

PMCAPLST
Bus: 0 Device: 14 Function: 0 Offset: 80h

Bit	Attribute	Default	Description
15:8	RO	90h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list (MSICAPLST).
7:0	RO	01h	**Capability ID (CAPID):** Identifies the function as PCI Power Management capable.

Table 4-61. Power Management Capabilities Register (PMCAP)

PMCAP
Bus: 0 Device: 14 Function: 0 Offset: 82h

Bit	Attribute	Default	Description
15:11	RO	19h	**PME_Support (PMESUP):** Indicates PME# is supported for states D3HOT and D3COLD. The RAS Unit does not generate PME#, but reporting that it does is necessary for some legacy operating systems to enable PME# in devices connected behind the RAS port.
10	RO	0b	**D2 Support (D2S):** Not supported. Hardwired to 0.
9	RO	0b	**D1 Support (D1S):** Not supported. Hardwired to 0.
8:6	RO	000b	**Auxiliary Current (AC):** Not supported. Hardwired to 0.
5	RO	0b	**Device Specific Initialization (DSI):** Not supported. Hardwired to 0.
4	RV	0b	Reserved
3	RO	0b	**PME Clock (PMECLK):** Not supported. Hardwired to 0.
2:0	RO	3h	**Version (VER):** PM implementation is compliant with *PCI Bus Power Management Interface Specification*, Revision 1.2.

Table 4-62. Power Management Control / Status Register (PMCSR)

PMCSR
Bus: 0 Device: 14 Function: 0 Offset: 84h

Bit	Attribute	Default	Description
15	RW1CS	0	**PME Status (PMESTS)**
14:13	RO	0h	**Data Scale (DC):** Not supported. Hardwired to 0.
12:9	RO	0h	**Data Select (DS):** Not supported. Hardwired to 0.
8	RWS	0	**PME Enable (PMEEN):** 1 = Indicates PME is enabled. The root port takes no action on this bit, but it must be R/W for some legacy operating systems to enable PME# on devices connected to this root port. This bit is sticky and resides in the resume well. The reset for this bit is RSMRST# which is not asserted during a warm reset.
7:2	RV	0h	Reserved
1:0	RW-R	0h	**Power State (PS):** This field is used both to determine the current power state of the root port and to set a new power state. The values are: 00 = D0 state 11 = D3HOT state

Table 4-63. MSI Capability List Register (MSICAPLST)

MSICAPLST
Bus: 0 Device: 14 Function: 0 Offset: 90h

Bit	Attribute	Default	Description
15:8	RO	00h	**Next Pointer (NP):** Contains the offset of the next item in the capabilities list. A null value is used to indicate that this is the last capability.
7:0	RO	05h	**Capability ID (CAPID):** Identifies the RAS Unit as MSI capable.

Table 4-64. MSI Message Control Register (MSICTL)

MSICTL
Bus: 0 Device: 14 Function: 0 Offset: 92h

Bit	Attribute	Default	Description
15:8	RV	00h	Reserved
7	RO	0b	**Address 64-Bit Capable (AD64C):** Not supported. Hardwired to 0. Capable of generating a 32-bit message only.
6:4	RW	000b	**Multiple Message Enable (MMEN):** Only one message is supported. These bits are R/W for software compatibility.
3:1	RO	000b	**Multiple Message Capable (MMC):** Only one message is supported.
0	RW	0b	**MSI Enable (MSIE):** When set, MSI is enabled and traditional interrupt pins are not used to generate interrupts.

Table 4-65. MSI Message Address Register (MSIADDR)

MSIADDR
Bus: 0 Device: 14 Function: 0 Offset: 94h

Bit	Attribute	Default	Description
31:2	RW	0h	**Address:** Message address specified by the system, always DWORD aligned.
1:0	RO	00b	Reserved

Table 4-66. MSI Message Data Register (MSIDATA)

MSIDATA
Bus: 0 Device: 14 Function: 0 Offset: 98h

Bit	Attribute	Default	Description
31:16	RV	0000h	Reserved
15:0	RW	0h	**Data (DATA):** R/W. This 16-bit field is programmed by system software if MSI is enabled. Its content is driven onto the lower word (PCI AD[15:0]) during the data phase of the MSI memory write transaction.

Table 4-67. Advanced Error Reporting Extended Capability Header (AERCAPHDR)

AERCAPHDR
Bus: 0 Device: 14 Function: 0 Offset: 100h

Bit	Attribute	Default	Description
31:20	RO	150h	**Next Capability Offset (NCO):** Contains the offset of the next structure in the Extended Capabilities list (RCECEPACAPHDR).
19:16	RO	1h	**Capability Version (CV):** Indicates the version of the Capability structure present.
15:0	RO	0001h	**Extended Capability ID (EXCAPID):** Identifies the function as Advanced Error Reporting capable.

Table 4-68. Uncorrectable Error Status Register (ERRUNCSTS)

ERRUNCSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 104h**

Bit	Attribute	Default	Description
31:21	RV	000h	Reserved
20	RW1CS	0b	**Unsupported Request Error (URE):** As a receiver, set whenever an unsupported request (negatively decoded transaction) is detected. The header is logged.
19	RV	0b	Reserved
18	RW1CS	0b	**Malformed TLP**: As a receiver, set whenever a malformed TLP (Length not equal to 000000001b for config requests) is detected. The header is logged.
17	RV	0b	Reserved
16	RW1CS	0b	**Unexpected Completion:** As a receiver, set whenever a completion is received that does not match the requestor ID or outstanding tag. The header is logged.
15:13	RV	000b	Reserved
12	RW1CS	0b	**Poisoned TLP Error (PTLPE):** Not supported.
11:6	RV	00h	Reserved
5	RO	0b	**Surprise Link Down Error (SLDE):** This bit is set when a surprise link down error is detected. ***Note:*** This bit does not apply to the upstream port.
5	RV	0b	Reserved
4	RV	0b	**Data Link Protocol Error (DLPE):** This bit is set when a data link protocol error is detected.
3:0	RV	000b	Reserved

Table 4-69. Uncorrectable Error Mask Register (ERRUNCMSK)

ERRUNCMSK **Bus: 0** **Device: 14** **Function: 0** **Offset: 108h**			
Bit	**Attribute**	**Default**	**Description**
31:25	RV	0h	Reserved
24	RO	0b	**AtomicOp Egress Blocked Error Mask (AEBEM):** Not supported.
23	RO	0b	**MC Blocked TLP Error Mask (MCEM):** Not supported.
22	RWS	0b	**Uncorrectable Internal Error Mask (UIEM):** Uncorrectable Internal Error Mask.
21	RO	0b	**ACS Violation Error Mask (ACSEM):** Not supported.
20	RWS	0b	**Unsupported Request Error Mask (UREM):** Unsupported Request Error Mask.
19	RO	0b	**ECRC Check Error Mask (ECRCEM):** Not supported.
18	RWS	0b	**Malformed TLP Error Mask (MTLPEM):** Malformed TLP Error Mask.
17	RO	0b	**Receiver Overflow Error Mask (ROEM):** Not supported.
16	RWS	0b	**Unexpected Completion Error Mask (UCEM):** Unexpected Completion Error Mask
15	RO	0b	**Completer Abort Error Mask (CAEM):** Not supported.
14	RO	0b	**Completion Timeout Error Mask (CTEM):** Not supported.
13	RO	0b	**Flow Control Error Mask (FCEM):** Not supported.
12	RWS	0b	**Poisoned TLP Error Mask (PTLPEM):** Not supported.
11:6	RV	00h	Reserved
5	RO	0b	**Surprise Link Down Error Mask (SLDEM)**: Not supported.
4	RO	0b	**Data Link Protocol Error Mask (DLPEM):** Not supported.
3:0	RV	000b	Reserved

Table 4-70. Uncorrectable Error Severity Register (ERRUNCSEV)

ERRUNCSEV
Bus: 0 Device: 14 Function: 0 Offset: 10Ch

Bit	Attribute	Default	Description
31:21	RV	000h	Reserved
20	RWS	0b	**Unsupported Request Error Status Severity (URES):** 0 = Error considered non-fatal. (Default) 1 = Error is fatal.
19	RO	0b	**ECRC Check Error Severity (ECRCES):** Not supported. Hardwired to 0b.
18	RWS	1b	**Malformed TLP Error Severity (MTLPES):** 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
17	RO	1b	**Receiver Overflow Error Severity (ROES):** Not supported.
16	RWS	0b	**Unexpected Completion Error Severity (UCES)**
15	RO	0b	**Completer Abort Error Severity (CAES):** Not supported. Hardwired to 0b.
14	RO	0b	**Completion Timeout Error Severity (CTES):** Not supported. Hardwired to 0b.
13	RO	1b	**Flow Control Error Severity (FCES)**
12	RWS	0b	**Poisoned TLP Error Severity (PTLPES):** Not supported.
11:5	RV	00h	Reserved
5	RO	0b	**Surprise Link Down Severity (SLDES)**: This bit does not apply to the upstream port or end point.
4	RO	1b	**Data Link Protocol Error Severity (DLPES):** 0 = Error considered non-fatal. 1 = Error is fatal. (Default)
3:0	RV	000b	Reserved

Table 4-71. Correctable Error Status Register (ERRCORSTS)

ERRCORSTS
Bus: 0 Device: 14 Function: 0 Offset: 110h

Bit	Attribute	Default	Description
31:14	RV	0h	Reserved
13	RW1CS	0	**Advisory Non-Fatal Error (ANFE):** 0 = Advisory Non-Fatal Error did not occur. 1 = Advisory Non-Fatal Error did occur.
12	RO	0	**Replay Timer Timeout Error (RTTE):** Not supported. Hardwired to 0.
11:9	RV	0h	Reserved
8	RO	0	**Replay Number Rollover Error (RNRE):** Not supported. Hardwired to 0.
7	RO	0	**Bad DLLP Error (BDLLPE):** Not supported. Hardwired to 0.
6	RO	0	**Bad TLP Error (BTLPE):** Not supported. Hardwired to 0.
5:1	RV	0h	Reserved
0	RO	0	**Receiver Error (RE):** Not supported. Hardwired to 0.

Table 4-72. Correctable Error Mask Register (ERRCORMSK)

ERRCORMSK **Bus: 0** **Device: 14** **Function: 0** **Offset: 114h**			
Bit	**Attribute**	**Default**	**Description**
31:14	RV	3h	Reserved
13	RWS	1	**Advisory Non-Fatal Error Mask (ANFEM):** 0 = Does not mask Advisory Non-Fatal errors. 1 = Masks Advisory Non-Fatal errors from: (a.) signaling ERR_COR to the device control register and (b.) updating the Uncorrectable Error Status register. This register is set by default to enable compatibility with software that does not comprehend Role-Based Error Reporting. ***Note:*** The correctable error detected bit in device status register is set whenever the Advisory Non-Fatal error is detected, independent of this mask bit.
12	RO	0	**Replay Timer Timeout Error Mask (RTTEM):** Not supported. Hardwired to 0.
11:9	RV	0h	Reserved
8	RO	0	**Replay Number Rollover Error Mask (RNREM):** Not supported. Hardwired to 0.
7	RO	0	**Bad DLLP Error Mask (BDLLPEM):** Not supported. Hardwired to 0.
6	RO	0	**Bad TLP Error Mask (BTLPEM):** Not supported. Hardwired to 0.
5:1	RV	0h	Reserved
0	RO	0	**Receiver Error Mask (REM):** Not supported. Hardwired to 0.

Table 4-73. Advanced Error Capabilities and Control Register (AERCAPCTL)

AERCAPCTL **Bus: 0** **Device: 14** **Function: 0** **Offset: 118h**			
Bit	**Attribute**	**Default**	**Description**
31:11	RV	0	Reserved
10	RO	0	**Multiple Header Recording Enable (MHRE):** Not supported. Hardwired to 0.
9	RO	0	**Multiple Header Recording Capable (MHRC):** Not supported. Hardwired to 0.
8	RO	0	**ECRC Check Enable (ECE):** Not supported. Hardwired to 0.
7	RO	0	**ECRC Check Capable (ECC):** Not supported. Hardwired to 0.
6	RO	0	**ECRC Generation Enable (EGE):** Not supported. Hardwired to 0.
5	RO	0	**ECRC Generation Capable (EGC):** Not supported. Hardwired to 0.
4:0	ROS-V	0h	**First Error Pointer (FEP):** Identifies the bit position of the last error reported in the Uncorrectable Error Status register.

Table 4-74. Root Error Status Register (ROOTERRSTS)

ROOTERRSTS
Bus: 0 Device: 14 Function: 0 Offset: 130h

Bit	Attribute	Default	Description
31:27	RO	0h	**Advanced Error Interrupt Message Number (AEMN):** Not supported. Hardwired to 0.
26:7	RV	0h	Reserved
6	RW1CS	0	**Fatal Error Message Received (FEMR):** Set when one or more Fatal Uncorrectable Error Messages have been received.
5	RW1CS	0	**Non-Fatal Error message Received (NFEMR):** Set when one or more Non-Fatal Uncorrectable error messages have been received.
4	RW1CS	0	**First Uncorrectable Fatal (FUF):** Set when the first Uncorrectable Error message received is for a fatal error.
3	RW1CS	0	**Multiple Error Fatal/Non-Fatal Received (MEFR):** For the S12x0, only one error is captured.
2	RW1CS	0	**Error Fatal/Non-Fatal Received (EFR):** 0 = No error message received. 1 = Either a fatal or a non-fatal error message is received.
1	RW1CS	0	**Multiple Error Correctable Error Received (MCER):** For the S12x0, only one error is captured.
0	RW1CS	0	**Correctable Error Received (CER):** 0 = No error message received. 1 = A correctable error message is received.

Table 4-75. Root Complex Event Collector Endpoint Association Extended Capability Header (RCECEPACAPHDR)

RCECEPACAPHDR
Bus: 0 Device: 14 Function: 0 Offset: 150h

Bit	Attribute	Default	Description
31:20	RO	000h	**Next Capability Offset (NCO):** This field contains 000h indicating the end of the extended capability list.
19:16	RO	1h	**Capability Version (CV):** Indicates the version of the capability structure present.
15:0	RO	0007h	**Extended Capability ID (ECID):** Identifies the function supports Root Complex Event Collector Endpoint Association capability.

Table 4-76. Association Bitmap for Root Complex Integrated Endpoints Register (ABMRCIEP)

ABMRCIEP
Bus: 0 **Device: 14** **Function: 0** **Offset: 154h**

Bit	Attribute	Default	Description
31:20	RV	0h	Reserved
19	RO	1	**Device 19 (SMBus 2.0) supported by RCEC (RCEC_D19):** Hardwired to 1. Indicates that the device 19 is supported by the RCEC.
18	RV	0	Reserved
17	RO	1	Reserved
16:15	RV	0	Reserved
14	RO	1	**Device 14 supported by RCEC (RCEC_D14):** Hardwired to 1. Indicates that the device 14 is supported by the RCEC.
13	RO	1	Reserved
12:1	RV	0	Reserved
0	RO	1	• Reserved

Table 4-77. Global Correctable Error Status Register (GCORERRSTS)

GCORERRSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 200h**

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	RW1CS	0	**PCIe RP[4] Error Status (PCIeRP4_CORR_STS):** This bit indicates that PCIe* RP[4] has detected an error.
5	RW1CS	0	**PCIe RP[3] Error Status (PCIeRP3_CORR_STS):** This bit indicates that PCIe RP[3] has detected an error.
4	RW1CS	0	**PCIe RP[2] Error Status (PCIeRP2_CORR_STS):** This bit indicates that PCIe RP[2] has detected an error.
3	RW1CS	0	**PCIe RP[1] Error Status (PCIeRP1_CORR_STS):** This bit indicates that PCIe RP[1] has detected an error.
2	RW1CS	0	**RCEC Error Status (RCEC_CORR_STS):** This bit indicates that RCEC has detected an error.
1	RW1CS	0	**Memory Controller Unit Error Status (MCU_CORR_STS):** This bit indicates that Memory Controller Unit has detected an error.
0	RW1CS	0	**Internal Buffer Unit Error Status (BU_CORR_STS):** This bit indicates that Internal Buffer Unit has detected an error.

Table 4-78. Global Nonfatal Error Status Register (GNERRSTS)

GNERRSTS
Bus: 0 Device: 14 Function: 0 Offset: 204h

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	RW1CS	0	**PCIe RP[4] Error Status (PCIeRP4_NF_STS):** This bit indicates that PCIe* RP[4] has detected an error.
5	RW1CS	0	**PCIe RP[3] Error Status (PCIeRP3_NF_STS):** This bit indicates that PCIe RP[3] has detected an error.
4	RW1CS	0	**PCIe RP[2] Error Status (PCIeRP2_NF_STS):** This bit indicates that PCIe RP[2] has detected an error.
3	RW1CS	0	**PCIe RP[1] Error Status (PCIeRP1_NF_STS):** This bit indicates that PCIe RP[1] has detected an error.
2	RW1CS	0	**RCEC Error Status (RCEC_NF_STS):** This bit indicates that RCEC has detected an error.
1	RW1CS	0	**Memory Controller Unit Error Status (MCU_NF_STS):** This bit indicates that Memory Controller Unit (MCU) has detected an error.
0	RW1CS	0	**Internal Buffer Unit Error Status (BU_NF_STS):** This bit indicates that MCU buffer unit has detected an error.

Table 4-79. Global Fatal Error Status Register (GFERRSTS)

GFERRSTS
Bus: 0 Device: 14 Function: 0 Offset: 208h

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	RW1CS	0	**PCIe RP[4] Error Status (PCIeRP4_F_STS):** This bit indicates that PCIe* RP[4] has detected an error.
5	RW1CS	0	**PCIe RP[3] Error Status (PCIeRP3_F_STS):** This bit indicates that PCIe RP[3] has detected an error.
4	RW1CS	0	**PCIe RP[2] Error Status (PCIeRP2_F_STS):** This bit indicates that PCIe RP[2] has detected an error.
3	RW1CS	0	**PCIe RP[1] Error Status (PCIeRP1_F_STS):** This bit indicates that PCIe RP[1] has detected an error.
2	RW1CS	0	**RCEC Error Status (RCEC_F_STS):** This bit indicates that RCEC has detected an error.
1	RW1CS	0	**Memory Controller Unit Error Status (MCU_F_STS):** This bit indicates that Memory Controller Unit (MCU) has detected an error.
0	RW1CS	0	**Internal Buffer Unit Error Status (BU_F_STS):** This bit indicates that MCU buffer unit has detected an error.

Table 4-80. Global Error Mask Register (GERRMSK)

GERRMSK Bus: 0 Device: 14 Function: 0 Offset: 20Ch			
Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	RWS	0	**PCIe RP[4] Error Mask (PCIeRP4_M):** This bit masks the error detected in the PCIe* RP[4].
5	RWS	0	**PCIe RP[3] Error Mask (PCIeRP3_M):** This bit masks the error detected in the PCIe RP[3].
4	RWS	0	**PCIe RP[2] Error Mask (PCIeRP2_M):** This bit masks the error detected in the PCIe RP[2].
3	RWS	0	**PCIe RP[1] Error Mask (PCIeRP1_M):** This bit masks the error detected in the PCIe RP[1].
2	RWS	0	**RCEC Error Mask (RCEC_M):** This bit masks the error detected in the RCEC.
1	RWS	0	**Memory Controller Unit Error Mask (MCU_M):** This bit masks the error detected in the Memory Controller Unit (MCU).
0	RWS	0	**Internal Buffer Unit Error Mask (BU_M):** This bit masks the error detected in the MCUs Buffer unit. 1 = Mask Error Reporting 0 = Unmask Error Reporting

Table 4-81. Global Correctable FERR Status Register (GCORFERRSTS)

GCORFERRSTS Bus: 0 Device: 14 Function: 0 Offset: 210h			
Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] CORRFERR Log (PCIeRP4_CORR_FERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] CORRFERR Log (PCIeRP3_CORR_FERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] CORRFERR Log (PCIeRP2_CORR_FERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	**PCIe RP[1] CORRFERR Log (PCIeRP1_CORR_FERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC CORRFERR Log (RCEC_CORR_FERR):** This bit indicates that RCEC has reported the first correctable error to the global error logic.
1	ROS-V	0	**Memory Controller Unit CORRFERR Log (MCU_CORR_FERR):** This bit indicates that Memory Controller Unit (MCU) has reported the first correctable error to the global error logic.
0	ROS-V	0	**Internal Buffer Unit CORRFERR Log (BU_CORR_FERR):** This bit indicates that MCU Buffer Unit has reported the first correctable error to the global error logic.

Table 4-82. Global Correctable NERR Status Register (GCORNERRSTS)

GCORNERRSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 214h**

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] CORRFERR Log (PCIeRP4_CORR_FERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] CORRFERR Log (PCIeRP3_CORR_FERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] CORRFERR Log (PCIeRP2_CORR_FERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	**PCIe RP[1] CORRFERR Log (PCIeRP1_CORR_FERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC CORRFERR Log (RCEC_CORR_NERR):** This bit indicates that RCEC has reported the next correctable error to the global error logic.
1	ROS-V	0	**Memory Controller Unit CORRFERR Log (MCU_CORR_NERR):** This bit indicates that Memory Controller Unit (MCU) has reported the next correctable error to the global error logic.
0	ROS-V	0	**Internal Buffer Unit CORRFERR Log (BU_CORR_NERR):** This bit indicates that MCU Buffer Unit has reported the next correctable error to the global error logic.

Table 4-83. Global Non-Fatal FERR Status Register (GNFERRSTS)

GNFERRSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 218h**

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] NFERR Log (PCIeRP4_N_FERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] NFERR Log (PCIeRP3_N_FERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] NFERR Log (PCIeRP2_N_FERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	P**CIe RP[1] NFERR Log (PCIeRP1_N_FERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC NFERR Log (RCEC_N_FERR):** This bit indicates that RCEC has detected an error.
1	ROS-V	0	**Memory Controller Unit NFERR Log (MCU_N_FERR):** This bit indicates that Memory Controller Unit (MCU) has reported the first non-fatal error to the global error logic.
0	ROS-V	0	**Internal Buffer Unit NFERR Log (BU_N_FERR):** This bit indicates that MCU Buffer Unit has reported the first non-fatal error to the global error logic.

Table 4-84. Global Nonfatal NERR Status Register (GNNERRSTS)

GNNERRSTS
Bus: 0 Device: 14 Function: 0 Offset: 21Ch

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] NNERR Log (PCIeRP4_N_NERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] NNERR Log (PCIeRP3_N_NERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] NNERR Log (PCIeRP2_N_NERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	**PCIe RP[1] NNERR Log (PCIeRP1_N_NERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC NNERR Log (RCEC_N_NERR):** This bit indicates that RCEC has detected an error.
1	ROS-V	0	**Memory Controller Unit NNERR Log (MCU_N_NERR):** This bit indicates that Memory Controller Unit (MCU) has reported the next non-fatal error to the global error logic.
0	ROS-V	0	**Internal Buffer Unit NNERR Log (BU_N_NERR):** This bit indicates that MCU Buffer Unit has reported the next non-fatal error to the global error logic.

Table 4-85. Global Fatal FERR Status Register (GFFERRSTS)

GFFERRSTS
Bus: 0 Device: 14 Function: 0 Offset: 220h

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] FFERR Log (PCIeRP4_F_FERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] FFERR Log (PCIeRP3_F_FERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] FFERR Log (PCIeRP2_F_FERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	**PCIe RP[1] FFERR Log (PCIeRP1_F_FERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC FFERR Log (RCEC_F_FERR):** This bit indicates that RCEC has reported the first fatal error to the global error logic.
1	ROS-V	0	**Memory Controller Unit FFERR Log (MCU_F_FERR):** This bit indicates that Memory Controller Unit (MCU) has reported the first fatal error to the global error logic.
0	ROS-V	0	**Internal Buffer Unit FFERR Log (BU_F_FERR):** This bit indicates that MCU Buffer Unit has reported the first fatal error to the global error logic.

Table 4-86. Global Fatal NERR Status Register (GFNERRSTS)

GFNERRSTS
Bus: 0 **Device: 14** **Function: 0** **Offset: 224h**

Bit	Attribute	Default	Description
31:7	RO	0	Reserved
6	ROS-V	0	**PCIe RP[4] FNERR Log (PCIeRP4_F_NERR):** This bit indicates that PCIe* RP[4] has detected an error.
5	ROS-V	0	**PCIe RP[3] FNERR Log (PCIeRP3_F_NERR):** This bit indicates that PCIe RP[3] has detected an error.
4	ROS-V	0	**PCIe RP[2] FNERR Log (PCIeRP2_F_NERR):** This bit indicates that PCIe RP[2] has detected an error.
3	ROS-V	0	**PCIe RP[1] FNERR Log (PCIeRP1_F_NERR):** This bit indicates that PCIe RP[1] has detected an error.
2	ROS-V	0	**RCEC FNERR Log (RCEC_F_NERR):** This bit indicates that RCEC has detected an error.
1	ROS-V	0	**Memory Controller Unit FNERR Log (MCU_F_NERR):** This bit indicates that Memory Controller Unit (MCU) has detected an error.
0	ROS-V	0	**Internal Buffer Unit FNERR Log (BU_F_NERR):** This bit indicates that MCU Buffer Unit has reported the next fatal error to the global error logic.

Table 4-87. Global Error Timer Register (GTIME)

GTIME
Bus: 0 **Device: 14** **Function: 0** **Offset: 228h**

Bit	Attribute	Default	Description
63:0	ROS-V	0	**Global Error Timer Value (GTIME_Value):** This is the 64-bit free running counter.

Table 4-88. Global Correctable FERR Error Time Stamp Register (GCORFERRTIME)

GCORFERRTIME
Bus: 0 **Device: 14** **Function: 0** **Offset: 230h**

Bit	Attribute	Default	Description
63:0	ROS-V	0	**Global CORFERR Time Stamp (G_CORFERR_TIME):** The time stamp register logs the 64-bit free running counter when the first correctable error was logged.

Table 4-89. Global Nonfatal FERR Error Time Stamp Register (GNFERRTIME)

GNFERRTIME
Bus: 0 **Device: 14** **Function: 0** **Offset: 238h**

Bit	Attribute	Default	Description
63:0	ROS-V	0	**Global NFERR Time Stamp (G_NFERR_TIME):** The time stamp register logs the 64-bit free running counter when the first non-fatal error was logged.

Table 4-90. Global Fatal FERR Error Time Stamp Register (GFFERRTIME)

GFFERRTIME Bus: 0 Device: 14 Function: 0 Offset: 240h			
Bit	**Attribute**	**Default**	**Description**
63:0	ROS-V	0	**Global FFERR Time Stamp (G_FFERR_TIME):** The time stamp register logs the 64-bit free running counter when the first fatal error was logged.

Table 4-91. Global System Event Status Register (GSYSEVTSTS)

GSYSEVTSTS Bus: 0 Device: 14 Function: 0 Offset: 248h			
Bit	**Attribute**	**Default**	**Description**
31:03	RO	0	Reserved
2	ROS-V	0	**Fatal Error Status (F_SYSEV_STS):** When set, processor has detected a fatal error.
1	ROS-V	0	**Nonfatal Error Status (NF_SYSEV_STS):** When set, processor has detected a nonfatal error.
0	ROS-V	0	**Correctable Error Status (CORR_SYSEV_STS):** When set, processor has detected a correctable error.

Table 4-92. Global System Event Mask Register (GSYSEVTMSK)

GSYSEVTMSK Bus: 0 Device: 14 Function: 0 Offset: 24Ch			
Bit	**Attribute**	**Default**	**Description**
31:03	RO	0	Reserved
2	RWS	0	**Fatal Error System Event Mask (F_SYSEV_M):** Fatal Error System Event Mask 0 = Unmask system event reporting of the fatal error 1 = Mask system event reporting of the fatal error
1	RWS	0	**Nonfatal Error System Event Mask (NF_SYSEV_M):** Nonfatal Error System Event Mask 0 = Unmask system event reporting of the nonfatal error 1 = Mask system event reporting of the nonfatal error
0	RWS	0	**Correctable Error System Event Mask (CORR_SYSEV_M):** Correctable Error System Event Mask 0 = Unmask system event reporting of the correctable error 1 = Mask system event reporting of the correctable error

Table 4-93. Global System Event Map Register (GSYSEVTMAP)

GSYSEVTMAP
Bus: 0 **Device: 14** **Function: 0** **Offset: 250h**

Bit	Attribute	Default	Description
31:06	RO	0	Reserved
5:4	RWS	10	**Fatal Error System Event Map (F_SYSEV_MAP):** 11: Reserved 10: Generate NMI 01: Generate SMI 00: No system event generation ***Note:*** NMIE.NMI=1 and NSC.SERR#_NMI_enable=1 to generate an NMI.
3:2	RWS	01	**Nonfatal Error System Event Map (NF_SYSEV_MAP):** 11: Reserved 10: Generate NMI 01 Generate SMI 00: No system event generation ***Note:*** NMIE.NMI=1 and NSC.SERR#_NMI_enable=1 to generate an NMI.
1:0	RWS	01	**Correctable Error System Event Map (CORR_SYSEV_MAP):** 11: Reserved 10: Generate NMI 01 Generate SMI 00: No system event generation ***Note:*** NMIE.NMI=1 and NSC.SERR#_NMI_enable=1 to generate an NMI.

Table 4-94. Error Pin Control Register (ERRPINCTRL)

ERRPINCTRL **Bus: 0**	**Device: 14**	**Function: 0**	**Offset: 254h**
Bit	**Attribute**	**Default**	**Description**
31:06	RO	0	Reserved
5:4	RWS	10	**ERR[2] Pin Assertion Enable (ERR[2]_ENABLE):** 11: Reserved 10: Assert error pin when fatal error is set in the system event status reg. 01: Assert and deassert error pin according to Error Pin Data register. 00: Disable error pin assertion.
3:2	RWS	01	**ERR[1] Pin Assertion Enable (ERR[1]_ENABLE):** 11: Reserved 10: Assert error pin when non-fatal error is set in the system event status reg. 01: Assert and deassert error pin according to Error Pin Data register. 00: Disable error pin assertion.
1:0	RWS	01	**ERR[0] Pin Assertion Enable (ERR[0]_ENABLE):** 11: Reserved 10: Assert error pin when correctable error is set in the system event status reg. 01: Assert and deassert error pin according to Error Pin Data register. 00: Disable error pin assertion.

Table 4-95. Error Pin Status Register (ERRPINSTS)

ERRPINSTS **Bus: 0**	**Device: 14**	**Function: 0**	**Offset: 258h**
Bit	**Attribute**	**Default**	**Description**
31:03	RO	0	Reserved
2	RW1CS	0	**ERR[2] Pin Status (ERR[2]_STS):** This bit is set upon the transition of deassertion to assertion of the error pin. Software writes 1 to clear the status.
1	RW1CS	0	**ERR[1] Pin Status (ERR[1]_STS):** This bit is set upon the transition of deassertion to assertion of the error pin. Software writes 1 to clear the status.
0	RW1CS	0	**ERR[0] Pin Status (ERR[0]_STS):** This bit is set upon the transition of deassertion to assertion of the error pin. Software writes 1 to clear the status.

Table 4-96. Error Pin Data Register (ERRPINDATA)

ERRPINDATA
Bus: 0 **Device: 14** **Function: 0** **Offset: 25Ch**

Bit	Attribute	Default	Description
31:03	RO	0	Reserved
2	RW	0	**ERR[2] Pin Status (ERR[2]_PINDATA):** (applies when ERRPINCTL[5:4]=01; otherwise reserved) This bit acts as the general purpose output for the ERR[2] pin. ERR [2] pin value follows the value programmed in ERR[2] Pin Data register. This bit applies only when ERRPINCTRL[5:4]=01; otherwise it is reserved. 0 = Deassert ERR[2] pin 1 = Assert ERR[2] pin This value only applies to the pin when ERRPINCNTL[5:4]=01.
1	RW	0	**ERR[1] Pin Status (ERR[1]_PINDATA):** (applies when ERRPINCTL[3:2]=01; otherwise reserved) This bit acts as the general purpose output for the ERR[1] pin. ERR [1] pin value follows the value programmed in ERR[1] Pin Data register. This bit applies only when ERRPINCTRL[3:2]=01; otherwise it is reserved. 0 = Deassert ERR[1] pin 1 = Assert ERR[1] pin This value only applies to the pin when ERRPINCTL[3:2]=01.
0	RW	0	**ERR[0] Pin Data (ERR[0]_PINDATA):** (applies when ERRPINCNTL[1:0]=01; otherwise reserved) This bit acts as the general purpose output for the ERR[0] pin. Error [0] pin value follows the value programmed in ERR[0] Pin Data register. This bit applies only when ERRPINCTRL[1:0]=01; otherwise it is reserved. 0 = Deassert ERR[0] pin 1 = Assert ERR[0] pin This value only applies to the pin when ERRPINCTL[1:0]=01.

4.3 Power Management Registers

Table 4-97. Register Summary (Sheet 1 of 2)

Offset (h)	Size (bits)	Name
70	32	“PMU Power Management I/O Base Addr (PPMBA)” on page 305
71	32	“PMU Control Registers (PCR)” on page 305
74	32	“PMU 8051 Watchdog Timer Control Register (PWDTC)” on page 306
75	32	“PMU 8051 Watchdog Timer Value Register (PWDTV)” on page 306
78	32	“PMU OS Power Management I/O Base Address (POSPMBA)” on page 306
79	32	“PMU PSMI I/O Base Address (PPSMIBA)” on page 307
7A	32	“PMU Active Power Management I/O Base Address (PAPMBA)” on page 307
80	32	“PMU Thermal Management Control (PTMC)” on page 308
81	32	“PMU Rank0 BW Trip Threshold (PTTR0)” on page 308
82	32	“PMU Rank1 BW Trip Threshold (PTTR1)” on page 309
83	32	“PMU BW Trip Threshold (PTTS)” on page 309
84	32	“PMU Default Thermal Enforcement for Bandwidth Trips (PDTELB)” on page 309
85	32	“PMU Default Thermal Enforcement for Thermal Trips (PDTELT)” on page 310
86	32	“PMU Lowest Thermal Enforcement Limits (PLTEL)” on page 310
B1	32	“PMU Thermometer Read Register (PTRR)” on page 311
B2	32	“PMU Thermal Trip Point Target Value Setting (PTPSTC)” on page 311
B3	32	“PMU Auxiliary Thermal Trip Point Setting (PTPSA)” on page 312
B4	32	“PMU Clear Point Settings Auxiliary (PCPSA)” on page 312
B5	32	“PMU Thermal Sensor and Interrupt Status (PTSIS)” on page 313
B6	32	“PMU Thermal Trip Behavior (PTTB)” on page 315
C0	32	“PMU Thermal Sensor In-use bits (PTSIU0)” on page 316
C1	32	“PMU Thermal Sensor In-Use Bits (PTSIU1)” on page 316
C2	32	“PMU Thermal Sensor In-Use Bits (PTSIU2)” on page 316
C3	32	“PMU Thermal Sensor In-use bits (PTSIU3)” on page 316
C4	32	“PMU Thermal Sensor In-use bits (PTSIU4)” on page 317
C5	32	“PMU Thermal MSI Address (PTMA)” on page 317
C6	32	“PMU Thermal MSI Data Register (PTMD)” on page 317
00	32	“PMU Processor Control (PPCNT)” on page 318
04	8	“PMU Level 2 Register (PLVL2)” on page 318
05	8	“PMU Level 3 Register (PLVL3)” on page 318
06	8	“PMU Level 4 Register (PLVL4)” on page 318
07	8	“PMU Level 5 Register (PLVL5)” on page 319
08	8	“PMU Level 6 Register (PLVL6)” on page 319
0C	32	“PMU C6 Control (PC6C)” on page 319
04	32	“PMU PM Command Register (PPM_CMD)” on page 320
08	32	“PMU PM Interrupt Control and Status Register (PPM_ICS)” on page 321
20	32	“PMU PM Subsystem Configuration (PPM_SSC)” on page 322
30	32	“PMU PM Subsystem Status (PPM_SSS)” on page 324
00	32	“PMU PMU Status (PPM_STS)” on page 325

Table 4-97. Register Summary (Sheet 2 of 2)

Offset (h)	Size (bits)	Name
00	32	"PMU PSMI Prepare Register (PPSMI_PREP)" on page 325
04	32	"PMU PSMI Save Register (PPSMI_SAVE)" on page 325
08	32	"PMU PSMI Restore Register (PPSMI_RESTORE)" on page 326
0C	32	"PMU PSMI Save Base Address Register (PPSMI_SAVE_BASE_ADDR)" on page 326

4.3.1 Power Management Related Registers

The Power Management Unit (PMU) implements most of its registers in the private space.

Table 4-98. Power Management Unit Private Space

Port-ID	Offset	Private Space Unit
04H	+50H through +E9H	PMU Private Space (PMPS)

The table below lists all the private registers in the PMU.

Table 4-99. Power Management Unit Private Registers (Sheet 1 of 2)

Offset	Register Name
70h	Section 4-100, “PMU Power Management I/O Base Addr (PPMBA)”
71h	Section 4-101, “PMU Control Registers (PCR)”
74h	Section 4-102, “PMU 8051 Watchdog Timer Control Register (PWDTC)”
75h	Section 4-103, “PMU 8051 Watchdog Timer Value Register (PWDTV)”
78h	Section 4-104, “PMU OS Power Management I/O Base Address (POSPMBA)”
79h	Section 4-105, “PMU PSMI I/O Base Address (PPSMIBA)”
7Ah	Section 4-106, “PMU Active Power Management I/O Base Address (PAPMBA)”
80h	Section 4-107, “PMU Thermal Management Control (PTMC)”
81h	Section 4-108, “PMU Rank0 BW Trip Threshold (PTTR0)”
82h	Section 4-109, “PMU Rank1 BW Trip Threshold (PTTR1)”
83h	Section 4-110, “PMU BW Trip Threshold (PTTS)”
84h	Section 4-111, “PMU Default Thermal Enforcement for Bandwidth Trips (PDTELB)”
85h	Section 4-112, “PMU Default Thermal Enforcement for Thermal Trips (PDTELT)”
86h	Section 4-113, “PMU Lowest Thermal Enforcement Limits (PLTEL)”
B1h	Section 4-114, “PMU Thermometer Read Register (PTRR)”
B2h	Section 4-115, “PMU Thermal Trip Point Target Value Setting (PTPSTC)”
B3h	Section 4-116, “PMU Auxiliary Thermal Trip Point Setting (PTPSA)”
B4h	Section 4-117, “PMU Clear Point Settings Auxiliary (PCPSA)”
B5h	Section 4-118, “PMU Thermal Sensor and Interrupt Status (PTSIS)”
B6h	Section 4-119, “PMU Thermal Trip Behavior (PTTB)”
C0h	Section 4-120, “PMU Thermal Sensor In-use bits (PTSIU0)”
C1h	Section 4-121, “PMU Thermal Sensor In-Use Bits (PTSIU1)”
C2h	Section 4-122, “PMU Thermal Sensor In-Use Bits (PTSIU2)”
C3h	Section 4-123, “PMU Thermal Sensor In-use bits (PTSIU3)”
C4h	Section 4-124, “PMU Thermal Sensor In-use bits (PTSIU4)”
C5h	Section 4-125, “PMU Thermal MSI Address (PTMA)”
C6h	Section 4-126, “PMU Thermal MSI Data Register (PTMD)”
PPMBA+00h	Section 4-127, “PMU Processor Control (PPCNT)”
PPMBA+04h	Section 4-128, “PMU Level 2 Register (PLVL2)”
PPMBA+05h	Section 4-129, “PMU Level 3 Register (PLVL3)”
PPMBA+06h	Section 4-130, “PMU Level 4 Register (PLVL4)”

Table 4-99. Power Management Unit Private Registers (Sheet 2 of 2)

Offset	Register Name
PPMBA+07H	Section 4-131, "PMU Level 5 Register (PLVL5)"
PPMBA+08h	Section 4-132, "PMU Level 6 Register (PLVL6)"
PPMBA+0Ch	Section 4-133, "PMU C6 Control (PC6C)"
POSPMBA+00h	Section 4-138, "PMU PMU Status (PPM_STS)"
POSPMBA+04h	Section 4-134, "PMU PM Command Register (PPM_CMD)"
POSPMBA+08h	Section 4-135, "PMU PM Interrupt Control and Status Register (PPM_ICS)"
POSPMBA+20h	Section 4-136, "PMU PM Subsystem Configuration (PPM_SSC)"
POSPMBA+30h	Section 4-137, "PMU PM Subsystem Status (PPM_SSS)"
PPSMIBA+00h	Section 4-139, "PMU PSMI Prepare Register (PPSMI_PREP)"
PPSMIBA+04h	Section 4-140, "PMU PSMI Save Register (PPSMI_SAVE)"
PPSMIBA+08h	Section 4-141, "PMU PSMI Restore Register (PPSMI_RESTORE)"
PPSMIBA+0Ch	Section 4-142, "PMU PSMI Save Base Address Register (PPSMI_SAVE_BASE_ADDR)"

Table 4-100. PMU Power Management I/O Base Addr (PPMBA)

PPMBA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 70h

Bit	Attribute	Default	Description
31	RW	0b	**ENABLE_EN:** When set, the range pointed to by ADDR enables a 16B I/O range for decode.
30:16	RO	0000h	Reserved
15:0	RW	0000h	**ADDRESS_ADDR:** Points to a 16B aligned I/O space. When enabled via EN, I/O cycles that match address bits 15:4 are decoded by the power management block.

Table 4-101. PMU Control Registers (PCR)

PCR
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 71h

Bit	Attribute	Default	Description
31:9	RW	000000h	Reserved
8	WO	0b	Reserved
7	RW	0b	**CSTATE_HIT_DISABLE_BIT:** When set, STPCLK assertion is disabled.
6	RW-O	0b	**THERMAL_SENSOR_AUXILIARY_CONTROL_LOCK_TSALC:** When set, some thermal management registers (as noted in their description), are locked. This bit can be written to 1 only once, and cannot be unlocked without a platform reset.
5	RW-O	0b	**THERMAL_SENSOR_CONTROL_LOCK_TSLC:** When set, some thermal management registers (as noted in their description), are locked. This bit can be written to 1 only once, and cannot be unlocked without a platform reset.
4	RW	0b	Reserved
3	RW	1b	Reserved
2	RW	0b	Reserved
1	RW	0b	**CONTROLLER_CLOCK_GATING_ENABLE:** When set, enables clock gating for the PMU.
0	RW	1b	**UNIT_CLOCK_GATING_DISABLED:** When set, this disables local clock gating for this unit.

Table 4-102. PMU 8051 Watchdog Timer Control Register (PWDTC)

PWDTC
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 74h

Bit	Attribute	Default	Description
31:18	RO	0000	Reserved
17	RW	0b	**POWERDOWN_ENABLE:** When set to 1, enables the mode that causes a power down on a WDT timeout.
16	RW	0b	**ENABLE:** When set to 1, the watchdog timer decrements and asserts warning interrupts to the microcontroller.
15:8	RW	00h	**WARNING_POINT:** Value the upper byte of the watchdog timer is compared to assert a warning interrupt to the microcontroller. It is set to a value higher than the latency to service the watchdog warning interrupt. This value is effectively in 256 µs granularity.
7:0	RW	00h	**RESET_VALUE:** Value to which the upper byte of the watchdog timer gets reset when pinged by the microcontroller. This value is effectively in 256 µs granularity.

Table 4-103. PMU 8051 Watchdog Timer Value Register (PWDTV)

PWDTV
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 75h

Bit	Attribute	Default	Description
31:16	RO	0000h	Reserved
15:8	RO	00h	**WATCHDOG_TIMER_UPPER_BYTE:** Value of the upper byte of the watchdog timer, used for warning point comparison, and reset to default value. This value is effectively in 256 µs granularity.
7:0	RO	FFh	**WATCHDOG_TIMER_LOWER_BYTE:** Value of the lower byte of the watchdog timer. This value is in 1 µs granularity.

Table 4-104. PMU OS Power Management I/O Base Address (POSPMBA)

POSPMBA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 78h

Bit	Attribute	Default	Description
31	RW	0b	**ENABLE_EN:** When set, the range pointed to by ADDRESS_ADDR enables a 64B I/O range for decode.
30:16	RO	0000h	Reserved
15:0	RW	0000h	**ADDRESS_ADDR:** Points to a 64B aligned I/O space. When enabled via ENABLE_EN, I/O cycles that match address bits 15:6 are decoded by the power management block.

Table 4-105. PMU PSMI I/O Base Address (PPSMIBA)

PPSMIBA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 79h

Bit	Attribute	Default	Description
31	RW	0b	**ENABLE_EN:** When set, the range pointed to by ADDRESS_ADDR enables a 16B I/O range for decode.
30:16	RO	0000h	Reserved
15:0	RW	0000h	**ADDRESS_ADDR:** Points to a 16B aligned I/O space. When enabled via ENABLE_EN, I/O cycles that match address bits 15:4 are decoded by the power management block.

Table 4-106. PMU Active Power Management I/O Base Address (PAPMBA)

PAPMBA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 7Ah

Bit	Attribute	Default	Description
31	RW	0b	**ENABLE_EN:** When set, the range pointed to by ADDRESS_ADDR enables a 16B I/O range for decode.
30:16	RO	0000h	Reserved
15:0	RW	0000h	**ADDRESS_ADDR:** Points to a 16B aligned I/O space. When enabled via ENABLE_EN, I/O cycles that match address bits 15:4 are decoded by the power management block.

Table 4-107. PMU Thermal Management Control (PTMC)

PTMC
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 80h

Bit	Attribute	Default	Description
31:28	RW	0	Reserved
27	RW	0	CPU_PROCHOT_THROTTLE_EN_CPTE: When set, treats PROCHOT assertion from CPU as HOT trip indication from the PTSIS.
26	RW	0	EXT_PROCHOT_THROTTLE_EN_EPTE: When set, treats external PROCHOT assertion as HOT trip indication from the PTSIS.
25	RW	0	DYNAMIC_THROTTLE_STRENGTH_CONTROL_DTSC: When set, SCH dynamically changes Throttle Enforcement Limits based on whether the condition continues and present activity. When cleared, defaults are used as static settings.
24	RW	0	Reserved
23	RW	0	SCH_BANDWIDTH_TRIP_THRESHOLD_ENABLE_STTE : When set, the event counters are used to compare against the TTSW and TTSR to trip throttling enforcement. When set to 0, the TTS has no effect. When enabled in conjunction with Thermal Trips, the most aggressive resultant
22:16	RW	0	Reserved
15	RW	0	BANDWIDTH_TRIP_THRESHOLD_RANK1_ENABLE_T TR1: Same definition as STTE, but for rank 1 counters.
14:8	RW	0	Reserved
7	RW	0	BANDWIDTH_TRIP_THRESHOLD_RANK0_TTR0: Same definition as PTTR1, for rank 0.
6:0	RW	0	Reserved

Table 4-108. PMU Rank0 BW Trip Threshold (PTTR0)

PTTR0
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 81h

Bit	Attribute	Default	Description
31:16	RW	0	Reserved
15:8	RW	0	WRITE_THRESHHOLD_W: Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank1 Write count from the event counters when there is no external thermal sensor configured for DRAM protection.
7:0	RW	0	READ_THRESHHOLD__R_: Indicates (in absence of a thermal sensor) a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Rank1 Read count from the event counters when there is no external thermal sensor configured for DRAM protection.

This holds the value to compare against the active event counts when bandwidth evaluation is enabled. It is programmed as a limit for traffic by BIOS to stay within thermal limits. It is recommended only using these in absence of thermal sensors.

Table 4-109. PMU Rank1 BW Trip Threshold (PTTR1)

PTTR1
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 82h

Bit	Attribute	Default	Description
31:0	RW	0	Reserved

Table 4-110. PMU BW Trip Threshold (PTTS)

PTTS
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 83h

Bit	Attribute	Default	Description
31:16	RW	0	Reserved
15:8	RW	0	WRITE_THRESHOLD: Indicates a threshold to initiate a trip for the throttle mechanism. This value will be compared against the total Write count FOR BOTH RANKS from the event counters when there is no internal thermal sensor configured for SCH protection.
7:0	RW	0	READ_THRESHOLD: Same as Write Threshold but for Reads from BOTH RANKS.

This register uses the sum of both ranks (if populated) to compare against this threshold, and shares the enforcement across the masks for both ranks.

Table 4-111. PMU Default Thermal Enforcement for Bandwidth Trips (PDTELB)

PDTELB
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 84h

Bit	Attribute	Default	Description
31:24	RW	0	SCH_WRITE_MASK: Sets the default throttle mask value loaded when using bandwidth-based trip mechanism for throttling SCH Total Writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime. ***Note:*** If there are two ranks, this number will be divided by two and split evenly to each rank. Therefore, performance may suffer more than needed if the requested traffic is all to one rank. The mechanism is not optimized for bandwidth enforcement to protect the SCH since it is recommended to use the internal thermal sensor as a trip mechanism.
23:16	RW	0	SCH_READ_MASK: Same definition as SCH Write Mask, but for SCH Total reads.
15:8	RW	0	MEMORY_RANK_WRITE_MASK: Sets the default throttle mask value loaded when using bandwidth-based trip mechanism for throttling Rank1 or Rank0 writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime.
7:0	RW	0	MEMORY_RANK_READ_MASK: Same definition as Memory Rank Write Mask, but for reads.

This contains default enforcement limits for the power management controller to load when Bandwidth Evaluation is enabled, and the threshold has been exceeded. It is a starting point each time entering throttling. The power management controller may adjust the strength dynamically.

Table 4-112. PMU Default Thermal Enforcement for Thermal Trips (PDTELT)

PDTELT
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 85h

Bit	Attribute	Default	Description
31:24	RW	00h	**Write Mask:** Sets the default throttle mask value loaded when using thermal-based trip mechanism for throttling total writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime. ***Note:*** If there are two ranks, this number is divided by two and split evenly to each rank. Therefore, performance may suffer more than needed if the requested traffic is all to one rank. It is recommended to use the internal thermal sensor as a trip mechanism.
23:16	RW	00h	**Read Mask:** Same as write mask, but for total reads.
15:8	RW	00h	**Memory Rank Write Mask:** Sets the default throttle mask value loaded when using thermal-based trip mechanism for throttling Rank1 or Rank0 writes. It provides a starting point to the throttle algorithm, which may change the enforcement dynamically during runtime.
7:0	RW	00h	**Memory Rank Read Mask:** Same definition as Memory Rank Write Mask, but for reads.

Same as DTELB, but for Thermal based trips.

Table 4-113. PMU Lowest Thermal Enforcement Limits (PLTEL)

PLTEL
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: 86h

Bit	Attribute	Default	Description
31:0	RW	0	**SCH_WRITE_MASK**
23:16	RW	0	**SCH_READ_MASK**
15:8	RW	0	**MEMORY_RANK_WRITE_MASK**
7:0	RW	0	**MEMORY_RANK_READ_MASK**

The same fields as defined in DTELB and DTELT, but this register defines the LOWEST limit the power management controller enforces for both bandwidth-based or thermal-based enforcement.

Table 4-114. PMU Thermometer Read Register (PTRR)

PTRR **MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B1h**			
Bit	**Attribute**	**Default**	**Description**
31:24	RO	00h	Reserved
23:16	RO	7Fh	**RELATIVE_TEMPERATURE_0_RELT0:** In thermometer mode, the RELATIVE_TEMPERATURE_0_RELT0 field of this register reports the relative temperature of the processor thermal sensor 0. Provides a two's complement value of the thermal sensor relative to the Hot Trip Point. Temperature above the Hot Trip Point is positive. RELATIVE_TEMPERATURE_0_RELT0 is clipped between +/-127 to keep it a 8 bit number
15:8	RO	00h	Reserved
7:0	RO	FFh	Reserved

This register generally provides the calibrated current temperature(s) from the thermometer circuit when the Thermometer mode is enabled.

Table 4-115. PMU Thermal Trip Point Target Value Setting (PTPSTC)

PTPSTC **MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B2h**			
Bit	**Attribute**	**Default**	**Description**
31:24	RW-L	00h	**HOT_CLEAR_POINT_SETTING_HCPS:** Sets the target value for the hot clear point.
23:16	RW-L	00h	**CATASTROPHIC_CLEAR_POINT_SETTING_CCPS:** These bits are set to 00h. THRMTRIP# is asserted on catastrophic thermal event.
15:8	RW-L	00h	**HOT_TRIP_POINT_SETTING_HTPS:** Sets the target value for the hot trip point.
7:0	RW-L	FFh	**CATASTROPHIC_TRIP_POINT_SETTING_CTPS:** Sets the target for the catastrophic trip point. These bits are set to FFh. THRMTRIP# is asserted on catastrophic thermal event.

All bits in this register are lockable via PCR.THERMAL_SENSOR_CONTROL_LOCK_TSLC.

Table 4-116. PMU Auxiliary Thermal Trip Point Setting (PTPSA)

PTPSA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B3h

Bit	Attribute	Default	Description
31:24	RW-L	00h	**AUX3_TRIP_POINT_A3TP:** Sets the target value for the Aux3 trip point.
23:16	RW-L	00h	**AUX2_TRIP_POINT_A2TP:** Sets the target value for the Aux2 trip point.
15:8	RW-L	00h	**AUX1_TRIP_POINT_A1TP:** Sets the target value for the Aux1 trip point.
7:0	RW-L	00h	**AUX0_TRIP_POINT_A0TP:** Sets the target value for the Aux0 trip point.

This register provides the Auxiliary trip point settings for both sensors together.

Table 4-117. PMU Clear Point Settings Auxiliary (PCPSA)

PCPSA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B4h

Bit	Attribute	Default	Description
31:24	RW-L	00h	**AUX3_CLEAR_POINT_A3CP**: Sets the target value for the Aux3 clear point.
23:16	RW-L	00h	**AUX2_CLEAR_POINT_A2CP**: Sets the target value for the Aux2 clear point.
15:8	RW-L	00h	**AUX1_CLEAR_POINT_A1CP**: Sets the target value for the Aux1 clear point.
7:0	RW-L	00h	**AUX0_CLEAR_POINT_A0CP**: Sets the target value for the Aux0 clear point.

This register provides the Auxiliary clear point settings for both sensors together. The clear point is the value where a trip indication is de-asserted after it has tripped.

Table 4-118. PMU Thermal Sensor and Interrupt Status (PTSIS) (Sheet 1 of 2)

PTSIS
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B5h

Bit	Attribute	Default	Description
31:27	RO	00h	Reserved
26	RO	0b	**DIRECT_CATASTROPHIC_COMPARATOR_READ_DCCR:** This bit reads the output of the catastrophic comparator directly, without latching via the thermometer mode circuit. Used for testing.
25	RO	0b	**DIRECT_HOT_COMPARATOR_READ_DHCR:** This bit reads the output of the hot comparator directly, without latching via the thermometer mode circuit. Used for testing.
24	RO	0b	**THERMOMETER_MODE_OUTPUT_VALID_TMOV:** 1 = Indicates the thermometer mode is able to converge to a temperature and that the TR register is reporting a reasonable estimate of the thermal sensor temperature. 0 = Indicates the thermometer mode is off, or that temperature is out of range, or that the TR register is being looked at before a temperature conversion has had time to complete.
23:22	RO	00b	Reserved
21	RO	0b	**CATASTROPHIC_TRIP_INDICATOR_CTI:** Live trip status for catastrophic setting. When 1, indicates an internal thermal sensor temperature has gone above the catastrophic trip point setting, and has not gone below the clear point setting.
20	RO	0b	**HOT_TRIP_INDICATOR_HTI:** Same as CTI, but for the hot setting.
19	RO	0b	**AUX3_TRIP_INDICATOR_A3TI:** Same as CTI, but for the Aux3 setting.
18	RO	0b	**AUX2_TRIP_INDICATOR_A2TI:** Same as CTI, but for the Aux2 setting.
17	RO	0b	**AUX1_TRIP_INDICATOR_A1TI:** Same as CTI, but for the Aux1 setting.
16	RO	0b	**AUX0_TRIP_INDICATOR_A0TI:** Same as CTI, but for the Aux0 setting.
15:14	RW1C	00b	Reserved
13	RW1C	0b	**CATASTROPHIC_HIGHER_TO_LOWER_INTERRUPT_CHLI:** Programmable catastrophic trip changed from 1 to 0
12	RW1C	0b	**HOT_HIGHER_TO_LOWER_INTERRUPT_HHLI:** When set, indicates that programmable hot trip changed from 1 to 0.
11	RW1C	0b	**AUX3_HIGHER_TO_LOWER_INTERRUPT_A3HLI:** When set, indicates that programmable aux3 trip changed from 1 to 0.
10	RW1C	0b	**AUX2_HIGHER_TO_LOWER_INTERRUPT_A2HLI:** When set, indicates that programmable aux2 trip changed from 1 to 0.
9	RW1C	0b	**AUX1_HIGHER_TO_LOWER_INTERRUPT_A1HLI:** When set, indicates that programmable aux1 trip changed from 1 to 0.
8	RW1C	0b	**AUX0_HIGHER_TO_LOWER_INTERRUPT_A0HLI:** When set, indicates that programmable aux0 trip changed from 1 to 0.
7:6	RW1C	00b	Reserved
5	RW1C	0b	**CATASTROPHIC_LOWER_TO_HIGHER_INTERRUPT_CLHI:** When set, indicates that programmable catastrophic trip changed from 0 to 1.
4	RW1C	0b	**HOT_LOWER_TO_HIGHER_INTERRUPT_HLHI:** When set, indicates that programmable hot trip changed from 0 to 1.
3	RW1C	0b	**AUX3_LOWER_TO_HIGHER_INTERRUPT_A3LHI:** When set, indicates that programmable aux3 trip changed from 0 to 1.

Table 4-118. PMU Thermal Sensor and Interrupt Status (PTSIS) (Sheet 2 of 2)

PTSIS
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B5h

Bit	Attribute	Default	Description
2	RW1C	0b	**AUX2_LOWER_TO_HIGHER_INTERRUPT_A2LHI:** When set, indicates that programmable aux2 trip changed from 0 to 1.
1	RW1C	0b	**AUX1_LOWER_TO_HIGHER_INTERRUPT_A1LHI:** When set, indicates that programmable aux1 trip changed from 0 to 1.
0	RW1C	0b	**AUX0_LOWER_TO_HIGHER_INTERRUPT_A0LHI:** When set, indicates that programmable aux0 trip changed from 0 to 1.

This contains status events for interrupts and which trip mechanisms are actively engaged. It does not distinguish which sensor was the source of the trip. TRR can be read to determine which zone each sensor is in, if necessary.

Table 4-119. PMU Thermal Trip Behavior (PTTB)

PTTB
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: B6h

Bit	Attribute	Default	Description
31	RW	0b	**INTERNAL_THERMAL_HARDWARE_THROTTLING_ENABLE_BIT_ITHTE:** This is a master enable for internal thermal sensor-based hardware throttling. Interrupts are not affected by this bit. This is for hot trip throttling only.
30:29	RW	0b	Reserved
28	RW	1b	Reserved
27:26	RW	01b	Reserved
25	RW	0b	**SELF_REFRESH_2X_ENABLE_SR2E:** When set, the DRAM controller enters 2x refresh rate, in order to support DRAM devices rated at 1x refresh rate up to 85 °C (most are rated to 95 °C). It is entered based on Aux0 trip.
24:5	RW	00000h	Reserved
4	RW	0b	**MSI_ON_HOT_TRIP_SCHT:** When set, an MSI is generated on a hot trip.
3	RW	0b	**MSI_ON_AUX3_TRIP_SCA3T:** When set, an MSI is generated on an Aux3 trip.
2	RW	0b	**MSI_ON_AUX2_TRIP_SCA2T:** When set, an MSI is generated on an Aux2 trip.
1	RW	0b	**MSI_ON_AUX1_TRIP_SCA1T:** When set, an MSI is generated on an Aux1 trip.
0	RW	0b	**MSI_ON_AUX0_TRIP_SCA0T:** When set, an MSI is generated on an Aux0 trip.

Table 4-120. PMU Thermal Sensor In-use bits (PTSIU0)

PTSIU0
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C0h

Bit	Attribute	Default	Description
31:1	RO	00000000h	Reserved
0	RW1CS	0b	**IN_USE_BIT_0_IU0:** After a full SCH reset, a read to this bit returns a 0. After the first read, subsequent reads return a 1. A write of a 1 to this bit resets the next read value to 0. Writing a 0 to this bit has no affect.

Table 4-121. PMU Thermal Sensor In-Use Bits (PTSIU1)

PTSIU1
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C1h

Bit	Attribute	Default	Description
31:1	RO	00000000h	Reserved
0	RW1CS	0b	**IN_USE_BIT_1_IU1:** After a full SCH reset, a read to this bit returns a 0. After the first read, subsequent reads returns a 1. A write of a 1 to this bit resets the next read value to 0. Writing a 0 to this bit has no affect.

Table 4-122. PMU Thermal Sensor In-Use Bits (PTSIU2)

PTSIU2
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C2h

Bit	Attribute	Default	Description
31:1	RO	00000000h	Reserved
0	RW1CS	0b	**IN_USE_BIT_2_IU2:** After a full SCH reset, a read to this bit returns a 0. After the first read, subsequent reads returns a 1. A write of a 1 to this bit resets the next read value to 0. Writing a 0 to this bit has no affect.

Table 4-123. PMU Thermal Sensor In-use bits (PTSIU3)

PTSIU3
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C3h

Bit	Attribute	Default	Description
31:1	RO	00000000h	Reserved
0	RW1CS	0b	**IN_USE_BIT_3_IU3:** After a full SCH reset, a read to this bit returns a 0. After the first read, subsequent reads returns a 1. A write of a 1 to this bit resets the next read value to 0. Writing a 0 to this bit has no affect.

Table 4-124. PMU Thermal Sensor In-use bits (PTSIU4)

PTSIU4
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C4h

Bit	Attribute	Default	Description
31:1	RO	00000000h	Reserved
0	RW1CS	0b	**IN_USE_BIT_4_IU4:** After a full SCH reset, a read to this bit returns a 0. After the first read, subsequent reads returns a 1. A write of a 1 to this bit resets the next read value to 0. Writing a 0 to this bit has no affect.

Table 4-125. PMU Thermal MSI Address (PTMA)

PTMA
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C5h

Bit	Attribute	Default	Description
31:2	RW	0h	**TMA_ADDR:** Address for thermal MSI
1:0	RW	0h	Reserved

Address register for thermal and IMR MSI.

Table 4-126. PMU Thermal MSI Data Register (PTMD)

PTMD
MCU Private: S12x0_PRIV_SPACE4 Port: 4h Offset: C6h

Bit	Attribute	Default	Description
31:16	RW	0000h	**IMR_DATA**
15:0	RW	0000h	**TMD_DATA**

Data register for thermal and IMR MSI.

Table 4-127. PMU Processor Control (PPCNT)

<table>
<tr><td colspan="4">PPCNT
Base: PPMBA Offset: 00h</td></tr>
<tr><th>Bit</th><th>Attribute</th><th>Default</th><th>Description</th></tr>
<tr><td>31:5</td><td>RO</td><td>0000000h</td><td>Reserved</td></tr>
<tr><td>4</td><td>RW</td><td>0b</td><td>PCNT_TEN: When set and the processor is in C0, it enables software-controlled STPCLK# throttling. The duty cycle is selected via TDTY. It remains in effect on each re-entry to C0 as long as enabled.</td></tr>
<tr><td>3:1</td><td>RW</td><td>000b</td><td>Throttle Duty: This field determines the duty cycle of throttling (percentage of time iSTPCLK_B asserted) when PCNT_TEN is set. The throttle period is approximately 8 µs.
<table>
<tr><th>Bits</th><th>Throttle Mode</th><th>Bits</th><th>Throttle Mode</th></tr>
<tr><td>000</td><td>50% (Default)</td><td>100</td><td>50%</td></tr>
<tr><td>001</td><td>87.75%</td><td>101</td><td>37.5%</td></tr>
<tr><td>010</td><td>75%</td><td>110</td><td>25%</td></tr>
<tr><td>011</td><td>62.5%</td><td>111</td><td>12.5%</td></tr>
</table></td></tr>
<tr><td>0</td><td>RO</td><td>0b</td><td>Reserved</td></tr>
</table>

Table 4-128. PMU Level 2 Register (PLVL2)

PLVL2
Base: PPMBA Offset: 04h

Bit	Attribute	Default	Description
7:0	RO	00h	Reserved

Table 4-129. PMU Level 3 Register (PLVL3)

PLVL3
Base: PPMBA Offset: 05h

Bit	Attribute	Default	Description
7:0	RO	00h	Reserved

Table 4-130. PMU Level 4 Register (PLVL4)

PLVL4
Base: PPMBA Offset: 06h

Bit	Attribute	Default	Description
7:0	RO	00h	Reserved

Table 4-131. PMU Level 5 Register (PLVL5)

PLVL5
Base: PPMBA Offset: 07h

Bit	Attribute	Default	Description
7:0	RO	00h	Reserved

Table 4-132. PMU Level 6 Register (PLVL6)

PLVL6
Base: PPMBA Offset: 08h

Bit	Attribute	Default	Description
7:0	RO	00h	Reserved

Table 4-133. PMU C6 Control (PC6C)

PC6C
Base: PPMBA Offset: 0Ch

Bit	Attribute	Default	Description
31	RO	0b	Reserved
30:27	RO	0000b	**LAST_ENTERED_C_STATE:** Once SCH transitions from C0 to C2/C3/C4/C5 or C6 state, it updates this register. It is used by SCH u-code to match the c-state residency with a target C-state.; 0000: C0 - added for uniformity but not expected to be tracked; 0001: C1 - added for uniformity but not expected to be tracked; 0010: C2 0011: C3 0100: C4 0101: C5 0110: C6 0111-1111: Reserved
26:0	RO	0000000h	**C_STATE_RESIDENCY:** This register reports the residency in the last entered C2/C3/C4/C5 or C6 state. The granularity used is in µ-seconds.

Table 4-134. PMU PM Command Register (PPM_CMD)

PCR_CMD
Base: POSPMBA Offset: 04h

Bit	Attribute	Default	Description
31:25	RO	00h	**Reserved.** Read accesses ignore this field and write accesses preserve current contents.
24:21	RW	0h	**MODE_ID:** SW defined value which identifies the mode associating with the current configuration. This value is provided in the PM Status Register upon successful completion of the set config command
20:17	RW	0000b	**CFG_TRIGGER:** Specifies a trigger to be used to start the sequencing of subsystems to the states specified in the SCW. 0000b = No trigger. Invalid if used in combination with mode specifying trigger initiated mode. 0001b = Trigger on LPM event from subsystem specified in the SUBSYS field of the command. 0010b = Trigger on external input from GPIO subsystem. 0011b = Trigger on C-state transition. 0100b = Trigger on DMI message.
16:13	RW	0000b	**CFG_DELAY:** Valid only if the CFG_MODE = CFG_DELAY. Specifies the number of delay cycles (1 cycle = ~250uSec) before starting the sequencing to enter the specified configuration.
12:9	RW	0000b	**CFG_MODE:** Specifies the mode use to start the configuration process. 0000b = CM_NOP. The PMU immediately indicates the operation is complete. Interrupt is generated if the IOC flag is set. 0001b = CM_IMMEDIATE. The PMU immediately starts the process to configure the subsystems as specified in the SCW. 0010b = CM_DELAY. The PMU uses the CFG_DELAY field to determine how long to delay before proceeding with the configuration process. Useful if there are conditions where a fixed period of time can be used for synchronization purposes. 0011b = CM_TRIGGER.
8	RW	0b	**IOC:** Interrupt on completion. Upon completion of the specified command, the PMU generates an interrupt. The interrupt status and control register contain information about the source of the interrupt. 1 = Interrupt when command complete 0 = Interrupt not generated upon completion
7:0	RW	00h	**PMUC_CMD:** Encoded command value;00000001b = Set config command

Table 4-135. PMU PM Interrupt Control and Status Register (PPM_ICS)

PPM_ICS
Base: POSPMBA   Offset: 08h

Bit	Attribute	Default	Description
31:10	RO	000000h	**Reserved.** Read accesses ignore this field and write accesses preserve current contents.
9	RW	0b	**IP:** Interrupt Pending. Indicates the PMU has generated an interrupt and the interrupt status register is valid. The bit must be written to a 1 to clear the interrupt pending condition. 0 = No interrupt pending 1 = Interrupt Pending
8	RW	0b	**IE:** Interrupt Enable. Enables an interrupt pending condition to generate a interrupt to the host. 0 = Interrupt disabled 1 = Interrupt enabled
7:0	RW	00h	**INT_STATUS:** Encoded field indicating the reason for the interrupt. The IP bit must be checked before using this interrupt status. If the IP bit is not set, the interrupt status is not valid.The following are the encoded values for the INT_STATUS: 0 = Invalid. 1 = Command Complete. If the IOC bit is set in the PM_CMD register this interrupt status is presented when the command completes. 2 = Command Error. An invalid command or parameter was received by the PMU. 3 = Wake Event received. The PM_WCS register is checked for the source of the wake event.

Table 4-136. PMU PM Subsystem Configuration (PPM_SSC) (Sheet 1 of 2)

PPM_SSC
Base: POSPMBA Offset: 20h

Bit	Attribute	Default	Description
31:30	RW	00b	**SS15C:** Subsystem 15 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
29:28	RW	00b	**SS14C:** Subsystem 14 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
27:26	RW	00b	**SS13C:** Subsystem 13 configuration word 00 = i0 01 = i1 10 = i2
25:24	RW	00b	**SS12C:** Subsystem 12 configuration word; 00 = i0 01 = i1 10 = i2 11 = D3
23:22	RW	00b	**SS11C:** Subsystem 11 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
21:20	RW	00b	**SS10C:** Subsystem 10 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
19:18	RW	00b	**SS09C:** Subsystem 09 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
17:16	RW	00b	**SS08C:** Subsystem 08 configuration word; 00 = i0 01 = i1 10 = i2 11 = D3
15:14	RW	00b	**SS07C:** Subsystem 07 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
13:12	RW	00b	**SS06C:** Subsystem 06 configuration word 00 = i0 01 = i1 10 = i2 11 = D3

Table 4-136. PMU PM Subsystem Configuration (PPM_SSC) (Sheet 2 of 2)

PPM_SSC
Base: POSPMBA Offset: 20h

Bit	Attribute	Default	Description
11:10	RW	00b	**SS05C:** Subsystem 05 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
9:8	RW	00b	**SS04C:** Subsystem 04 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
7:6	RW	00b	**SS03C:** Subsystem 03 configuration word 00 = i0 01 = i1 10 = i2 11 = D3
5:4	RW	00b	**SS02C:** Subsystem 02 configuration word 00 = i0. No clock gating or power gating. 01 = i1. Clock gating. 10 = i2. Power gating with HW state retention. 11 = D3 Power gated with no HW state retention.
3:2	RW	00b	**SS01C:** Subsystem 01 configuration word 00 = i0. No clock gating or power gating. 01 = i1. Clock gating. 10 = i2. Power gating with HW state retention. 11 = D3 Power gated with no HW state retention.
1:0	RW	00b	**SS00C:** Subsystem 00 configuration word 00 = i0. No clock gating or power gating. 01 = i1. Clock gating. 10 = i2. Power gating with HW state retention. 11 = D3 Power gated with no HW state retention.

Table 4-137. PMU PM Subsystem Status (PPM_SSS)

PPM_SSS
Base: POSPMBA **Offset: 30h**

Bit	Attribute	Default	Description
31:30	RW	00b	**SS15S:** Subsystem 15 status 00 = i0. Active. Local clock gating allowed. 01 = i1. Clock gated (Subsystem IDLE). 10 = i2. Power gated with HW state retention. 11 = i3/D3 Power gated with no HW state retention.
29:28	RW	00b	**SS14S:** Subsystem 14 status 00 = i0. Active. Local clock gating allowed. 01 = i1. Clock gated (Subsystem IDLE). 10 = i2. Power gated with HW state retention. 11 = i3/D3 Power gated with no HW state retention.
27:26	RW	00b	**SS13S:** Subsystem 13 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
25:24	RW	00b	**SS12S:** Subsystem 12 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention
23:22	RW	00b	**SS11S:** Subsystem 11 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
21:20	RW	00b	**SS10S:** Subsystem 10 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
19:18	RW	00b	**SS09S:** Subsystem 09 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
17:16	RW	00b	**SS08S:** Subsystem 08 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
15:14	RW	00b	**SS07S:** Subsystem 07 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
13:12	RW	00b	**SS06S:** Subsystem 06 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention
11:10	RW	00b	**SS05S:** Subsystem 05 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
9:8	RO	00b	**SS04S:** Subsystem 04 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
7:6	RO	00b	**SS03S:** Subsystem 03 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
5:4	RO	00b	**SS02S:** Subsystem 02 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
3:2	RO	00b	**SS01S:** Subsystem 01 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.
1:0	RW	00b	**SS00S:** Subsystem 00 status;00 = i0. Active. Local clock gating allowed;01 = i1. Clock gated (Subsystem IDLE);10 = i2. Power gated with HW state retention.;11 = i3/D3 Power gated with no HW state retention.

Table 4-138. PMU PMU Status (PPM_STS)

PPM_STS
Base: POSPMBA Offset: 00h

Bit	Attribute	Default	Description
31:13	RO	00000h	Reserved. Read accesses ignore this field and write accesses preserve current contents.
12:9	RO	0000b	**MODE_ID:** Encoded Mode ID. This value is updated by the PMU whenever a set config command is completed. This value is provided in the set config command. The PMU does not interpret or act on this value.
8	RO	0b	**PMU_BUSY:** PMU Busy status indication 0 = PMU Idle 1 = PMU Busy
7:0	RO	00h	**PMU_REV:** PMU Revision Information

Table 4-139. PMU PSMI Prepare Register (PPSMI_PREP)

PPSMI_PREP
Base: PPSMIBA Offset: 00h

Bit	Attribute	Default	Description
31:0	RO	0h	PSMI_PREP_0

Table 4-140. PMU PSMI Save Register (PPSMI_SAVE)

PPSMI_SAVE
Base: PPSMIBA Offset: 04h

Bit	Attribute	Default	Description
31:0	RO	0h	PSMI_SAVE_0

Table 4-141. PMU PSMI Restore Register (PPSMI_RESTORE)

PPSMI_RESTORE
Base: PPSMIBA Offset: 08h

Bit	Attribute	Default	Description
31:0	RO	0h	PSMI_RESTORE_0

Table 4-142. PMU PSMI Save Base Address Register (PPSMI_SAVE_BASE_ADDR)

PPSMI_SAVE_BASE_ADDR
Base: PPSMIBA Offset: 0Ch

Bit	Attribute	Default	Description
31:0	RO	0h	PSMI_SAVE_BASE_ADDR

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5 Sideband Register Access

The IOSF Sideband registers are accessed indirectly by writing/reading the Sideband Packet Register (NCSPR), the Sideband Data Register (NCSDR) and the Sideband Packet Extension Register (NCSPER) that are located at Bus 0, Device 0, Function 0, offset D0h through DBh.

The IOSF Sideband registers are used to access the IOSF Private Registers of the SoC.

5.1 Accessing the IOSF Sideband Registers

The IOSF Sideband register read/write data is accessed through the NCSDR and the IOSF Sideband register address and command are written to NCSPR and NCSPER. All accesses to these three registers must be DWord.

To write to an IOSF Sideband register:

1. Update NCSPER if accessing a register offset that is more than 256 bytes.
2. Update NCSDR with Data. NCSDR and NCSPER can be written in any order.
3. Finally update NCSPR. This executes the sideband command.

To read to an IOSF Sideband register:

1. Update NCSPER if accessing a register offset that is more than 256 bytes.
2. Update NCSPR. This executes the sideband command.
3. Read to NCSDR obtains the register contents.

Table 5-1. IOSF Sideband Register Access

Register	Register Name	Number of bits	Bus 0, Device 0, Function 0 Offset
Sideband Packet Register	NCSPR	32	D0h
Sideband Data Register	NCSDR	32	D4h
Sideband Extension Register	NCSPRE	32	D8h

The NCSDR is written as a full DWord as follows:

- NCSPR[31:24] - Sideband Opcode, is set to 06h for a read and 07h for a write.
- NCSPR[23:16] - The 8-bit IOSF Sideband Port ID.
- NCSPR[15:8] - Bits 7:0 of the IOSF Sideband register offset. Bits 31:8 of the OSF Sideband register offset must be first updated in NCSPRE[31:8].
- NCSPR[7:4] - Fh, full DWord read or write.
- NCSPR[3:0] - 0h, reserved field.

Table 5-2. Sideband Packet Register (NCSPR)

NCSPR
Bus: 0 **Device: 0** **Function: 0** **Offset: D0h**

Bit	Attr	Default	Description
31:24	WO	00h	**Sideband Opcode:** The operation to be performed on the target port. Valid OpCodes: • 06h - Read • 07h - Write • All other OpCodes are Reserved.
23:16	WO	00h	**Sideband Port:** The device or unit to be targeted by Sideband transaction.
15:08	WO	00h	**Sideband Offset:** Bits 7:0 of the private register offset to be targeted by the Sideband transaction. This field applies only to register read and writes.
07:04	WO	0h	**Sideband Byte Enable:** The sideband byte enables to be used by the triggered transaction. This field applies only to register read and writes.
03:00	RV	0h	Reserved

Table 5-3. Sideband Data Register (NCSDR)

NCSDR
Bus: 0 **Device: 0** **Function: 0** **Offset: D4h**

Bit	Attr	Default	Description
31:00	RW	00000000h	**Sideband Data:** Sideband data register is used as the place to store the data.

Table 5-4. Sideband Packet Register Extension (NCSPRE)

NCSPER
Bus: 0 **Device: 0** **Function: 0** **Offset: D8h**

Bit	Attr	Default	Description
31:08	RW	000000h	**Sideband Address Extension:** Bits 31:8 of the offset field
7:0	RV	00h	Reserved

5.2 IOSF Private Registers

Table 5-5. Aunit Enhanced Configuration Space (AEC)

AEC
IOSF Private: RWD_PRIV_SPACE0 Port: 0h Offset: 00h

Bit	Attr	Default	Description
31:28	RW	0h	**ECBase:** When ECBase matches bits [31:28] of a system memory address that has been forwarded and enhanced configuration operations are enabled, the corresponding operation is treated as an Enhanced Configuration Space Access.
27:01	RV	00000h	Reserved
0	RW	0h	**Enable:** Enables Enhanced Configuration Space Access operation.

Table 5-6. Host Miscellaneous Control 2 (HMISC2)

HMISC2
IOSF Private: RWD_PRIV_SPACE2 Port: 02h Offset: 03h

Bit	Attr	Default	Description
31:25	RV	00h	Reserved
24	RO	0b	Processor Break Event (PBE) status from CPU.
23:21	RV	0h	Reserved
20:16	RW	17h	**OR PM signals from ICH:** When set, the SoC does OR the Power Management (PM) signals driven by an ICH with the internal values generated by Power Management Unit (PMU) mechanisms. This field specifies, on a signal-by-signal basis, whether a given bit is driven via a (68h) message from PMU or via a direct pin from the ICH. Put another way, when the corresponding bit is clear, the ICH signal does not affect the signal driven to the core. The ICH signals are enabled as follows: 20 Reserved 19 SMI -- BIOS needs to set this bit after SMI handler is loaded. 18 NMI 17 INIT 16 INTR
15:12	RV	0h	Reserved
11:8	RW	Fh	**Route PM signals directly from ICH:** When set, the SoC does forward the Power Management (PM) signals driven by an ICH, instead of the internal values generated by Power Management Unit (PMU) mechanisms. This field specifies, on a signal-by-signal basis, whether a given bit is driven via a (68h) message from PMU or via a direct pin from the ICH. The ICH signals are enabled as follows: 11 DPSTP 10 STPCLK 9 DPSLP 8 SLP/PM Sync
7	RW	0b	**Force_SLP:** When set, force SLP to be taken from a GPIO pin used for PSMI replay.
6	RV	0b	Reserved
5	RW	0b	**Disable I/O Per-Core Fairness Mechanism (DisableCoreFairness):** When this bit is set, the mechanism that enforces fairness between processor cores is disabled.
4	RW	0b	**Read A and B Segments from DRAM (ABSegmentReadFromDRAM):** When this bit is set, accesses targeting A and B segments are routed to DRAM.
3	RW	0b	**Random Redirect Enable (RandomRedirectEnable):** When this bit is zero, all re-directable inter-processor interrupts (RIPIs) are routed to the logical processor whose agent ID = 00b. When it is set, interrupts are sent in a round robin fashion to the two processor local APICs.
2	RW	0b	**Read FSeg from DRAM (FSegmentReadFromDRAM):** When this bit is set, reads.targeting F-segment are routed to DRAM.
1	RW	0b	**Read ESeg from DRAM (ESegmentReadFromDRAM):** When this bit is set, reads targeting E-segment are routed to DRAM.
0	RW	1b	**Fail NonDRAM Locks (FailNonDRAMLocks):** When this bit is set, locks targeting addresses above the range specified in the host/memory boundary register does result in a hard fail.

Table 5-7. Host System Management Mode Controls (HSMMCTL)

HSMMCTL
IOSF Private: RWD_PRIV_SPACE2 Port: 02h Offset: 04h

Bit	Attr	Default	Description
31:20	RW	000h	**Upper Bound (SMMEnd):** These bits are compared with bits 31:20 of the incoming address to determine the upper 1MB aligned value of the protected range when SMMEnabled is set.
19:16	RV	0h	**Reserved**
15:4	RW-L	000h	**Lower Bound (SMMStart):** These bits are compared with bits 31:20 of the incoming address to determine the lower 1MB aligned value of the protected range when EnableCFO is set. LockKey: HSMMCTL.SMMLocked
3	RV	0b	Reserved
2	RW-L	1b	**Allow non-SMM writes to SMM Space (SMMWritesOpen):** This allows processor writes to the SMM space defined by the SMMStart and SMMEnd fields even when the SMM bit is not set in the host request. LockKey: HSMMCTL.SMMLocked
1	RW-L	1b	**Allow non-SMM reads to SMM Space (SMMReadsOpen):** This allows processor reads to the SMM space defined by the SMMStart and SMMEnd fields even when the SMM bit is not set in the host request. LockKey: HSMMCTL.SMMLocked
0	RW-KL	0b	**SMM Locked (SMMLocked):** Locks this register and doesn't allow its fields to be changed until the system is reset.

Table 5-8. Host Extended Configuration Space Config (HECREG)

HECREG
IOSF Private: RWD_PRIV_SPACE2 Port: 02h Offset: 09h

Bit	Attr	Default	Description
31:28	RW	08h	**EC Boundary (ECBase):** Describes bits [31:28] of the range being used to access memory-mapped configuration space through the AUnit. ***Note:*** HECREG matches AEC.
27:1	RV	0000000h	Reserved
0	RW	0b	**EC Enable (ECEnable):** When set, causes the ECBase range to be compared to incoming accesses. If bits [31:28] of the access match the ECBase value, then a posted memory operation is treated as a non-posted operation and the deferred transaction buffer is locked until a signal comes from the Aunit indicating that the transaction completion has been received. ***Note:*** HECREG matches AEC.

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