Embedded 4th Generation Intel® Core™ Processor, Intel® Pentium® Processor, Intel® Celeron® and Intel® Xeon® Processor E3-1200 v3 Product Families

Datasheet Addendum

November 2014

Number: 331059-002US

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Revision History

Date	Revision	Description
August 2014	001	Initial release
November 2014	002	Updates to Table 15 and Table 19

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1.0 Feature Summary

1.1 Introduction

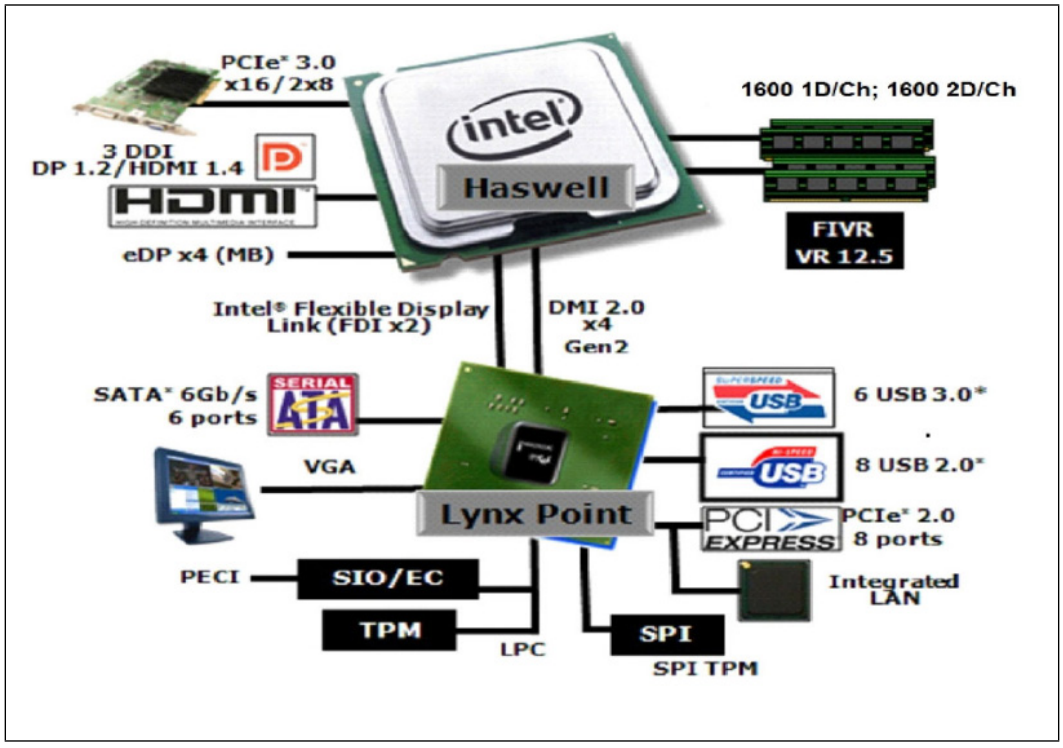
This Datasheet Addendum is a supplement to the 4th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v3 Family datasheets. It contains the additional electrical specifications, signal information, interface functional descriptions, additional feature information and configuration registers pertinent to the implementation and operation of the Embedded 4th Generation Intel® Core™ Processor Family and Intel® Xeon® Processor E3-1200 v3 and their respective platform.

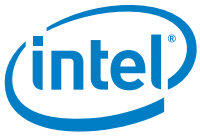
Note: Throughout this document, the 4th Generation Intel® Core™ Processor and Intel® Xeon® Processor E3-1200 v3 may be referred to simply as "processor".

Note: Throughout this document, the Intel® 8 Series chipset and Intel® C22x Series chipset may be referred to simply as "PCH".

Note: This document contains information on interfaces that differ from the 4th Generation Intel® Core™ Processor (non-ECC Processor). This processor is the next generation of the 64-bit, multi-core processor built on 22-nanometer process technology.

Figure 1. Embedded Sharkbay and Denlow Platforms





1.2 Related Documents

Refer to the documents in the tables below for additional information.

https://www-ssl.intel.com/content/www/us/en/library/find-content.html

Table 1. Processor Documents

Documents	Document No./Location
Haswell Mobile Platform Design Guide	486713
Haswell Desktop and Denlow-WS Platform Design Guide	486711
Haswell All-In-One Platform Design Guide	486712
Haswell U/Y Platform Design Guide	502636
[Shark Bay] Mobile Platform Power Delivery Design Guide	487822
Desktop 4th Generation Intel® Core™ Processor Family, Desktop Intel®Pentium® Processor Family, and Desktop Intel® Celeron® Processor Family - Datasheet, Volumes 1 and 2	328897 328898
Intel® Xeon® Processor E3-1200 v3 Product Family - Datasheet, Volumes 1 and 2	328907 329000
Embedded Shark Bay + ECC Platform Design Guide Addendum for Haswell-Mbl_ECC Processor and Lynx Point-Mbl Platform Controller Hub	505347
VR12.5 Pulse Width Modulation (PWM) Haswell Input VR Enabling-Product Specification	453513
RS - Platform Environment Control Interface (PECI) Specification[1]	25891
[Haswell] Mobile - I/O Buffer Information Specification (IBIS) Models	491321
[Shark Bay-M + ECC] Platform Symbol Files	508615
Haswell Mobile Processor +ECC BGA 1364 Ballout	505026
Haswell Mobile Processor Thermal Design Guide for Embedded Applications	503979
Haswell Desktop Processors for Embedded Applications Thermal and Mechanical Design Guide	518804
[Haswell-EP/EP 4S] Processor - External Design Specifications (EDS) Vol.3: Electrical	507850
4th Generation Intel® Core™ Processors and Intel® Xeon® Processor E3-1200 v3 Product Family Package - Mechanical Drawings	503752
Note: 1. Contact your Intel representative for the latest revision of this item.	

Table 2. Platform Controller Hub (PCH) Documents

Document	Document No./Location
Intel® Lynx Point Chipset for Desktop - Thermal Mechanical Specifications and Design Guidelines (TMSDG)	487848

Table 3. Public Specification

Document	Document No./Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Express* Base Specification 2.0 PCI Express* Base Specification 3.0	http://www.pcisig.com

Table 3. Public Specification

Document	Document No./Location
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm

1.3 Terminology

Term	Description
BGA	Ball Grid Array
DMI	Direct Media Interface
ECC	Error Correcting Code
EDS	External Design Specification
LGA	Land Grid Array
MCP	Multi Chip Package
DDR3L	Third Generation Double Data Rate SDRAM memory technology
ECC	Error Correction Code
IMC	Integrated Memory Controller
ODT	On-Die Termination
PCH	Platform Controller Hub. The new 2013 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. The PCH may also be referred to as Intel® 8 Series Chipset Family (formerly code-named Lynx Point).
*PCIe**	PCI Express*
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term "processor core" refers to Si die itself, which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
U-DIMM	Unbuffered Dual In-line Memory Module
SO-DIMM	Small Outline Dual In-line Memory Module
SPI	Serial Peripheral Interface

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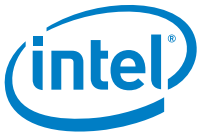


2.0 Interface

2.1 System Memory Design Guidelines

2.1.1 Embedded Desktop/Workstation LGA Processor

- Follow the *Haswell Desktop and Denlow-WS Platform Design Guide* for U-DIMM design guidelines for non-ECC system memory.
- Follow the *Haswell Desktop and Denlow-WS Platform Design Guide* for U-DIMM design guidelines for system memory with ECC when paired with Haswell Workstation PCH.
- Follow the *Haswell All-In-One Platform Design Guide* for SO-DIMM design guidelines for non-ECC system memory.
- Follow the *Embedded Shark Bay + ECC Platform Design Guide Addendum for Haswell-Mbl_ECC Processor and Lynx Point-Mbl Platform Controller Hub* for SO-DIMM design guidelines for system memory with ECC.

2.1.2 Embedded Mobile BGA Processor

- Follow the *Embedded Shark Bay + ECC Platform Design Guide Addendum for Haswell-Mbl_ECC Processor and Lynx Point-Mbl Platform Controller Hub* for U-DIMM, SO-DIMM & Memory Down design guidelines for ECC & non-ECC system memory.

2.1.3 Embedded U/Y Series MCP Processor

- Follow the *Haswell U/Y Platform Design Guide* for SO-DIMM & Memory Down design guidelines for non-ECC system memory.

2.2 System Memory Interface

The System Memory Interface consists of one or two channels of DDR3L memory with a maximum of four ranks per channel.

- DDR3L memory may be implemented as:
  - — ECC or non-ECC unbuffered SODIMM
  - — ECC or non-ECC unbuffered DIMM
  - — ECC or non-ECC memory down (following unbuffered DIMM topologies)
- Single-channel and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- DDR3L I/O Voltage of 1.35V
- 64-bit wide channels
- Theoretical maximum memory bandwidth of:
  - — 21.3 GB/s in dual-channel mode assuming DDR3L 1333 MT/s
  - — 25.6 GB/s in dual-channel mode assuming DDR3L 1600 MT/s
- One or two memory channels of DDR3L memory with unbuffered ECC SO-DIMM with a maximum of two DIMMs per channel. Two DIMMs per channel is only supported with Intel® quad-core processor SKUs.
- Mixing of ECC and Non-ECC DIMMS is not supported

2.2.1 System Memory Technology Support

The Integrated Memory Controller (IMC) supports DDR3L protocols with two independent, 64-bit wide channels each accessing up to four ranks.

Note: Four ranks per channel is only supported in Intel® quad-core processor SKUs.

For more information, please refer to the *Desktop 4th Generation Intel® Core™ Processor Family, Desktop Intel® Pentium® Processor Family, and Desktop Intel® Celeron® Processor Family - Datasheet*, Volumes 1 and 2 (Document Numbers: 328897 and 328898).

Table 4. Mobile Memory Rank Support Summary by Product

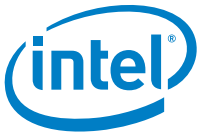
Processors	Package	Ranks per channel	DDR3L
Intel® dual-core processor	BGA	≤ 2	1333/1600
Intel® quad-core processor	BGA	≤ 2	1333/1600
		≤ 4	1333/1600

2.2.1.1 DDR3L Data Transfer Rates

- 1333 MT/s (PC3-10600), 1600 MT/s (PC3-12800)

2.2.1.2 DDR3L SO-DIMM Modules

- Raw Card B – Single Rank x8 unbuffered non-ECC
- Raw Card C – Single Rank x8 unbuffered ECC
- Raw Card D – Dual Rank x8 (planar) unbuffered ECC
- Raw Card F – Dual Rank x8 (planar) unbuffered non-ECC



2.2.1.3 DDR3L DIMM Modules

- Raw Card A – Single Rank x8 unbuffered non-ECC
- Raw Card B – Dual Rank x8 unbuffered non-ECC
- Raw Card D – Single Rank x8 unbuffered ECC
- Raw Card E – Dual Rank x8 unbuffered ECC

2.2.1.4 DDR3L Memory Down

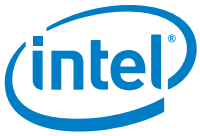
- Single Rank x8 unbuffered non-ECC
- Dual Rank x8 unbuffered non-ECC
- Single Rank x8 unbuffered ECC

2.2.1.5 DRAM Device Technology

- Standard 1-Gb, 2-Gb, and 4-Gb technologies and addressing are supported for x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 5. Supported Memory Configurations

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row/ Col Address Bits	# of Banks Inside DRAM	Page Size
Non-ECC SODIMMs								
B	1 GB	1 Gb	128 M X 8	8	1	14/10	8	8K
	2 GB	2 Gb	256 M X 8	8	1	15/10	8	8K
F	2 GB	1 Gb	128 M X 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M X 8	16	2	15/10	8	8K
	8 GB	4 Gb	512 M X 8	16	2	16/10	8	8K
ECC SODIMMs								
C	1 GB	1 Gb	128 M X 8	9	1	14/10	8	8K
	2 GB	2 Gb	256 M X 8	9	1	15/10	8	8K
D	2 GB	1 Gb	128 M X 8	18	2	14/10	8	8K
	4 GB	2 Gb	256 M X 8	18	2	15/10	8	8K
	8 GB	4 Gb	512 M X 8	18	2	16/10	8	8K
Non-ECC DIMMs / Non-ECC Memory Down								
A	1 GB	1 Gb	128 M X 8	8	1	14/10	8	8K
	4 GB	4 Gb	512 M X 8	8	1	16/10	8	8K
B	2 GB	1 Gb	128 M X 8	16	2	14/10	8	8K
	4 GB	2 Gb	256 M X 8	16	2	15/10	8	8K
	8 GB	4 Gb	512 M X 8	16	2	16/10	8	8K
ECC DIMMs / ECC Memory Down								
D	1 GB	1 Gb	128 M X 8	9	1	14/10	8	8K
	2 GB	2 Gb	256 M X 8	9	1	15/10	8	8K
E	2 GB	1 Gb	128 M X 8	18	2	14/10	8	8K
	4 GB	2 Gb	256 M X 8	18	2	15/10	8	8K
	8 GB	4 Gb	512 M X 8	18	2	16/10	8	8K



2.2.2 System Memory Timing Support for BGA + ECC Processors

The IMC supports the following DDR3L Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1N indicates a new command may be issued every clock and 2N indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Note: System memory timing support is based on availability and is subject to change.

Table 6. DDR3L System Memory Timing Support

Segment	Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	DPC	CMD Mode	Notes
Intel® quad-core processor, BGA with GT2 Graphics	1333	8/9	8/9	8/9	7	1	1N/2N	
						2	2N	
	1600	10/11	10/11	10/11	8	1	1N/2N	
						2	2N	
Intel® dual-core processor, BGA with GT2/GT1 Graphics	1333	8/9	8/9	8/9	7	1	1N/2N	
	1600	10/11	10/11	10/11	8	1	1N/2N	

2.2.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the ranks are populated in each memory channel, a number of different configurations can exist.

2.2.3.1 Single-Channel Mode

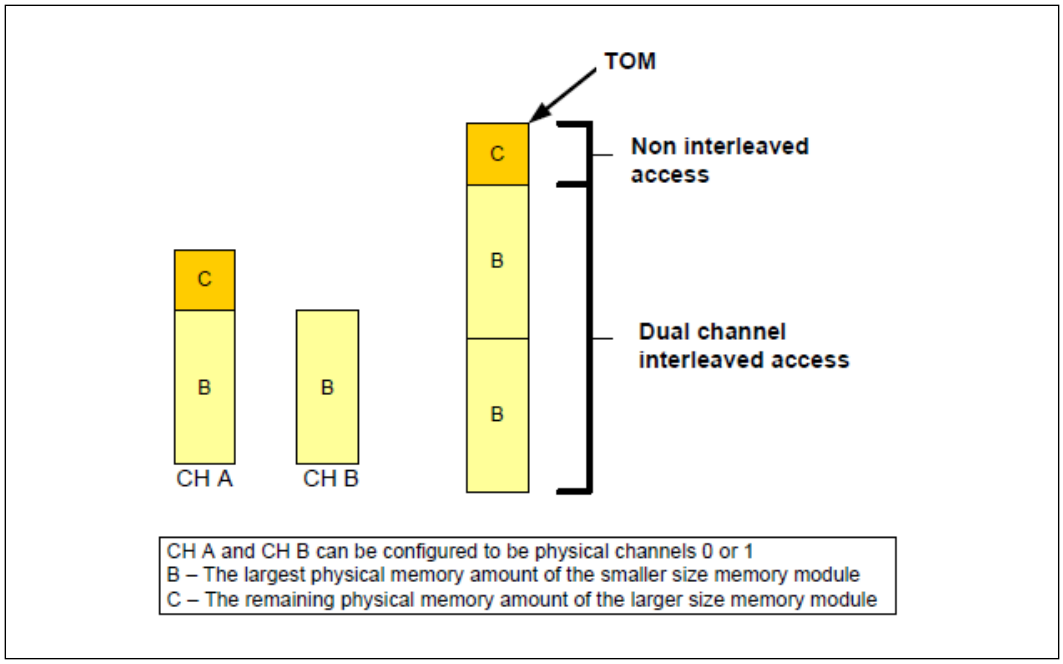
In this mode, all memory cycles are directed to a single-channel. The single-channel mode is used when only one of the channels (A/B) is populated, in any order. If both channels A and B are fully populated, the system no longer behaves in the single channel mode.

2.2.3.2 Dual-Channel Mode - Intel® Flex Memory Technology Mode

The IMC supports the Intel® Flex Memory Technology Mode. Memory is divided into symmetric and asymmetric zones. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Note: Channels A and B can be mapped for physical channel 0 and 1 respectively or vice versa; however, channel A size must be greater or equal to channel B size.

Figure 2. Intel® Flex Memory Technology Operations



2.2.3.3 Dual-Channel Symmetric Mode

The Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use the Dual-Channel Symmetric mode when both Channel A and Channel B ranks are populated in any order, with the total amount of memory in each channel being the same.

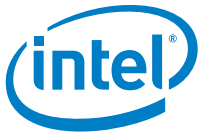
When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in the Dual-Channel Symmetric mode.

Note: The DRAM device technology and width may vary from one channel to the other.

2.2.4 System Memory Frequency

2.2.4.1 DIMM or SODIMM Modules, Memory Down Topologies (Implementing SPD)

In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports up to two DIMM connectors per channel. If DIMMs with different latency are populated across the channels, the BIOS will use the slower of the two latencies for both channels. For dual-channel modes both channels must have a DIMM connector populated. For single-channel mode, only a single-channel can have a DIMM connector populated.



2.2.4.2 Memory Down Topologies (Not Implementing SPD)

In all modes, the frequency of system memory is the lowest frequency of all memory devices placed in the system, as determined through the relevant modification of the memory reference code. The system memory controller supports up to four ranks per channel. If memory devices with different latencies are populated across the channels, the memory reference should be modified to use the slower of the latencies for both channels. For dual-channel modes both channels must have at least one rank populated. For single-channel mode, only a single-channel can have a rank populated.

2.2.5 Technology Enhancements of Intel® Fast Memory Access

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel® Fast Memory Access (Intel® FMA) technology enhancements.

2.2.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.

2.2.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Pre-charge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.2.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.2.6 Data Scrambling

The memory controller incorporates a DDR3L Data Scrambling feature to minimize the impact of excessive di/dt on the platform DDR3L VRs due to successive 1s and 0s on the data bus. Past experience has demonstrated that traffic on the data bus is not random and can have energy concentrated at specific spectral harmonics creating high di/dt which is generally limited by data patterns that excite resonance between the package inductance and on die capacitances. As a result the memory controller uses a data scrambling feature to create pseudo-random patterns on the DDR3L data bus to reduce the impact of any excessive di/dt.

2.2.7 DRAM Clock Generation

Every supported rank has one differential clock pair. There are a total of four clock pairs per channel driven directly by the processor to four ranks.

2.2.8 DDR3L Reference Voltage Generation

The memory controller has the capability of generating the DDR3L Reference Voltage (VREF) internally for both read (RDVREF) and write (VREFDQ) operations. The generated VREF can be changed in small steps, and an optimum VREF value is determined for both during a cold boot through advanced DDR3L training procedures in order to provide the best voltage and signal margins.

2.3 Lane Reversal and Polarity Inversion Support

Lane Reversal and Polarity Inversion are independent of each other. DMI supports Lane Reversal and Polarity Inversion but only on the PCH side. This is enabled via a soft strap. Refer to the latest PCH EDS for more details. Also refer to the latest silicon sighting reports for silicon stepping limitations regarding these capabilities.

As Polarity Inversion is auto-detected for DMI and PCIe*, no strapping is required. Lane Reversal is not detected automatically for DMI and PCIe* and must be set up correctly via strap. If DMI or FDI needs to be reversed, one soft strap should be used. The DMI and FDI share the same soft strap through PCHSTRP9. Refer to the 489495, *[Lynx Point] Chipset Intel® 8 Series Chipset Family SPI Programming Guide* for more details.

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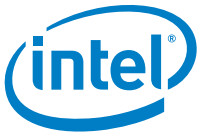

3.0 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type.

Notation	Signal Type
I	Input pin
O	Output pin
I/O	Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal (see Table 7).

Table 7. Signal Description Buffer Types

Signal	Description
DDR3L	DDR3L buffers: 1.35-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation

3.1 System Memory Interface for the Processor

Table 8. Memory Channel A (Sheet 1 of 2)

Signal Name	Description	Direction	Buffer Type
SA_BS[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	O	DDR3L
SA_WE#	Write Enable Control Signal: Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O	DDR3L
SA_RAS#	RAS Control Signal: Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SDRAM Commands.	O	DDR3L
SA_CAS#	CAS Control Signal: Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SDRAM Commands.	O	DDR3L
SA_DQSP[7:0] SA_DQSN[7:0]	Data Strobes: SA_DQSP[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQSP[7:0] and its SA_DQSN[7:0] during read and write transactions.	I/O	DDR3L
SA_DQSP[8] SA_DQSN[8]	ECC Check Bit Data Strobes: SA_DQSP[8] and its complement signal make up a differential strobe pair. The data is captured at the crossing point of SA_DQSP[8] and its SA_DQSN[8] during read and write transactions[1].	I/O	DDR3L
SA_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O	DDR3L

Table 8. Memory Channel A (Sheet 2 of 2)

Signal Name	Description	Direction	Buffer Type
SA_DQ[71:64]	ECC Check Bit Data Bus: Channel A data signal interface to the SDRAM data bus[1].	I/O	DDR3L
SA_MA[15:0]	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.	O	DDR3L
SA_CKP[3:0] SA_CKN[3:0]	SDRAM Differential Clock: Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CKP and the negative edge of its complement SA_CKN are used to sample the command and control signals on the SDRAM. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SA_CKE[3:0]	Clock Enable: (1 per rank) Used to: • Initialize the SDRAMs during power-up • Power-down SDRAM ranks • Place all SDRAM ranks into and out of self-refresh during STR - Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SA_CS#[3:0]	Chip Select: (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SA_ODT[3:0]	On Die Termination: Active Termination Control. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L

Note:

1. These signals can be left as a no connect for non-ECC design implementations.

Table 9. Memory Channel B (Sheet 1 of 2)

Signal Name	Description	Direction	Buffer Type
SB_BS[2:0]	Bank Select: These signals define which banks are selected within each SDRAM rank.	O	DDR3L
SB_WE#	Write Enable Control Signal: Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O	DDR3L
SB_RAS#	RAS Control Signal: Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SDRAM Commands.	O	DDR3L
SB_CAS#	CAS Control Signal: Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SDRAM Commands.	O	DDR3L
SB_DQSP[7:0] SB_DQSN[7:0]	Data Strobes: SB_DQSP[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQSP[7:0] and its SB_DQSN[7:0] during read and write transactions.	I/O	DDR3L
SB_DQSP[8] SB_DQSN[8]	ECC Check Bit Data Strobes: SB_DQSP[8] and its complement signal make up a differential strobe pair. The data is captured at the crossing point of SB_DQSP[8] and its SB_DQSN[8] during read and write transactions[1].	I/O	DDR3L
SB_DQ[63:0]	Data Bus: Channel A data signal interface to the SDRAM data bus.	I/O	DDR3L
SB_DQ[71:64]	ECC Check Bit Data Bus: Channel A data signal interface to the SDRAM data bus[1].	I/O	DDR3L
SB_MA[15:0]	Memory Address: These signals are used to provide the multiplexed row and column address to the SDRAM.	O	DDR3L

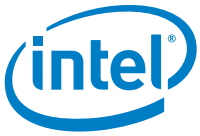

Table 9. Memory Channel B (Sheet 2 of 2)

Signal Name	Description	Direction	Buffer Type
SB_CKP[3:0] SB_CKN[3:0]	SDRAM Differential Clock: Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CKP and the negative edge of its complement SB_CKN are used to sample the command and control signals on the SDRAM. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SB_CKE[3:0]	Clock Enable: (1 per rank) Used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR. -Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SB_CS#[3:0]	Chip Select: (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
SB_ODT[3:0]	On Die Termination: Active Termination Control. Bits [3:2] used only for a >2 rank per channel system	O	DDR3L
Note: 1. These signals can be left as a no connect for non-ECC design implementations.			

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4.0 Electrical Specifications

4.1 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 10. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals and selected DDR3L signals have On-Die Termination (ODT) resistors.

Table 10. Signal Group

Signal Group	Signal Type	Buffer Type	Signal
DDR3L Reference Clocks [1]			
Differential	Output	DDR3L	SA_CKP[3:0], SA_CKN[3:0], SB_CKP[3:0], SB_CKN[3:0]
DDR3L Command Signals [1]			
Single ended	Output	DDR3L	SA_BS[2:0], SB_BS[2:0], SA_WE#, SB_WE#, SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS#, SA_MA[15:0], SB_MA[15:0]
DDR3L Control Signals[1]			
Single ended	Output	DDR3L	SA_CKE[3:0], SB_CKE[3:0], SA_CS#[3:0], SB_CS#[3:0], SA_ODT[3:0], SB_ODT[3:0], SM_DRAMRST#
DDR3L Data Signals[1]			
Single ended	Bi-Directional	DDR3L	SA_DQ[71:0], SB_DQ[71:0]
Differential	Bi-Directional	DDR3L	SA_DQSP[8:0], SA_DQSN[8:0], SB_DQSP[8:0], SB_DQSN[8:0]

Note:
1. SA and SB refer to DDR3L Channel A and DDR3L Channel B.

4.1.1 AC Specifications

The processor timings specified in this section are defined at the processor pads. Therefore, proper simulation of the signals is the only means to verify proper timing and signal quality.

Note: Please refer to the 4*th Generation Intel® Core™ Processor EDS* for more processor pin and signal information.

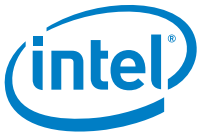


Table 11. DDR3L Electrical Characteristics and AC Timing at 1333MT/s

Symbol	Parameter	Channel A and B		Unit	Figure	Note [1,7]
		Max	Min			
System Memory Clock Timings						
TCK	CK Period	1.50	-	ns	-	-
System Memory Command Signal Timings						
TCMD_CO	RAS#, CAS#, WE#, MA[16:0], BA[2:0] Edge Placement Accuracy	0.1*TCK	-	ps	Figure 3	3, 4, 5, 8
System Memory Control Signal Timings						
TCTRL_CO	CS#[3:0], CKE[3:0], ODT[3:0] Edge Placement Accuracy	0.1*TCK	-	ps	Figure 3	3, 5, 8
System Memory Data and Strobe Signal Timings						
TDVB +TDVA	DQ[71:0] Valid before DQS[8:0] Rising or Falling Edge	0.1*TCK	-	ps	-	6, 8
TSu+HD	DQ Input Setup Plus Hold Time to DQS Rising or Falling Edge	0.125*TCK	-	ps	Figure 4	1, 2, 6, 8

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. Timing specifications only depend on the operating frequency of the memory channel and not the maximum rated frequency
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the TSU and THD specifications must be increased by a derrating factor. The input single ended slew rate is measured DC to AC levels; VIL_DC to VIH_AC for rising edges, and VIH_DC to VIL_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derrating value. No derrating is required for single ended slew rates equal to or greater than 1.0 V/ ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within ±EPA. This EPA includes jitter, skew, within die variation and several other effect.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
6. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
7. These are pre-silicon estimates and are subject to change.
8. Max range is correct but center point is subject to change during MRC boot training.ocessor pad are determined with the minimum Read DQS/DQS# delay.

Table 12. DRR3L Electrical Characteristics and AC Timing at 1600MT/s

Symbol	Parameter	Channel A and B		Unit	Figure	Note [1,7]
		Max	Min			
System Memory Clock Timings						
TCK	CK Period	1.25	-	ns	-	-
System Memory Command Signal Timings						
TCMD_CO	RAS#, CAS#, WE#, MA[16:0], BA[2:0] Edge Placement Accuracy	0.1*TCK	-	ps	Figure 3	3, 4, 5, 8
System Memory Control Signal Timings						
TCTRL_CO	CS#[3:0], CKE[3:0], ODT[3:0] Edge Placement Accuracy	0.1*TCK	-	ps	Figure 3	3, 5, 8
System Memory Data and Strobe Signal Timings						
TDVB +TDVA	DQ[71:0] Valid before DQS[8:0] Rising or Falling Edge	0.1*TCK	-	ps	-	6, 8
TSu+HD	DQ Input Setup Plus Hold Time to DQS Rising or Falling Edge	0.125*TCK	-	ps	Figure 4	1, 2, 6, 8

Notes:

1. Unless otherwise noted, all specifications in this table apply to all processor frequencies. Timing specifications only depend on the operating frequency of the memory channel and not the maximum rated frequency
2. When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the TSU and THD specifications must be increased by a derrating factor. The input single ended slew rate is measured DC to AC levels; VIL_DC to VIH_AC for rising edges, and VIH_DC to VIL_AC for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derrating value. No derrating is required for single ended slew rates equal to or greater than 1.0 V/ ns.
3. Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within ±EPA. This EPA includes jitter, skew, within die variation and several other effects.
4. Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5. The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
6. The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS s rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
7. These are pre-silicon estimates and are subject to change.
8. Max range is correct but center point is subject to change during MRC boot training.

Figure 3. DDR3L Command/ Control and Clock Timing Waveform

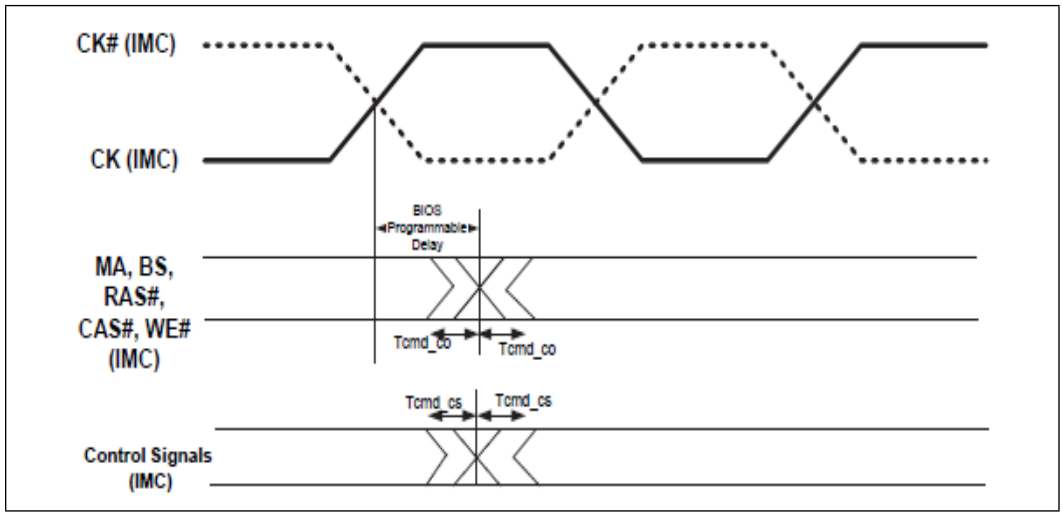
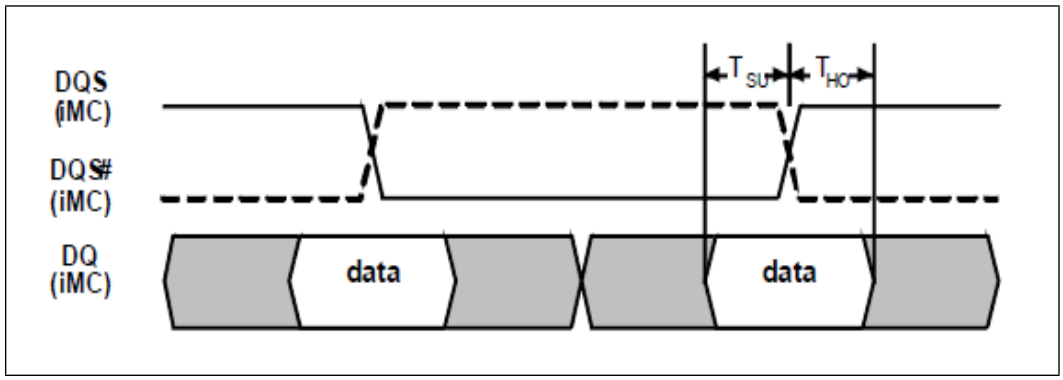


Figure 4. DDR3L Data Setup and Hold Timing Waveform



4.2 Voltage and Current Specification

For any voltage and current specifications not mentioned in Table 13, please refer to *Mobile 4th Generation Intel® Core™ Processor Family, Mobile Intel® Pentium® Processor Family, and Mobile Intel® Celeron® Processor Family - External Design Specification (EDS), Volumes 1, 2* and *[Shark Bay] Mobile Platform Power Delivery Design Guide*.

Table 13. Processor Core (V_{CC}) Active and Idle Mode DC Voltage and Current Specification

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Notes
I_{CCMAX} for processors	Maximum Processor Core ICC	47W 37W 25W	-	-	85 55 55	A	1, 3
I_{CC_TOC}	TDC at PL2 for 40 seconds starting from idle state	47W 37W 25W	-	-	33 26 26	A	2, 3
	TDC	47W 37W 25W	-	-	27 21 21	A	2, 3
I_{CC}_Dyn_VID1	Dynamic Current step size in VID1	47W 37W 25W	-	-	60 35 35	A	4
R_AC_LL	Loadline slope in response to dynamic load increase events 1KHz - 1MHz	47W 37W 25W	-	-	-2.4 -3.6 -3.6	mV/A	5
A_AC_LL_OS	Loadline slope in response to dynamic load release events	47W 37W 25W	-	-	-3.0 -5.0 -5.0	mV/A	5

Notes:

1. Processor core VR to be designed to electrically support this current.
2. Processor core VR to be designed to thermally support this current indefinitely.
3. Long term reliability cannot be assured in conditions above or below Maximum/Minimum functional limits.
4. Expected Maximum dynamic load.
5. The VR and decoupling solution should be designed to target these AC loadlines. Manufacturing tolerance bands in the validation plan will provide allowances in HVM testing.

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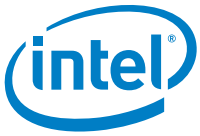

5.0 Package

5.1 Processor Pin and Signal Information

The *4th Generation Intel® Core™ Processor* (ECC Processor) Mobile BGA processor pin and signal information is available in the *Haswell Mobile Processor +ECC BGA 1364 Ballout* document (Document Number: 505026).

5.2 Package Mechanical Drawing

Refer to *4th Generation Intel® Core™ Processors and Intel® Xeon® Processor E3-1200 v3 Product Family Package - Mechanical Drawings* for the *4th Generation Intel® Core™ Processor* mechanical drawings.

Table 14. Package Mechanical Drawing Reference

Package	Functional Core	Integrated Graphics Core	PMD to Refer
LGA 1150	4	2	Desktop -> LGA1150 Processor.pdf
	2	2	
	2	1	
	1	1	
BGA 1364	4	2	Mobile -> Quad Core BGA with GT2.pdf
	2	2	
	2	1	

5.3 Processor Listing

Table 15 lists the processor and their features.

Table 15. 4th Generation Intel® Core™ Processor Family listing/package (Sheet 1 of 2)

Spec #	Processor Number	Stepping	Cache Size (MB)	Func. Core	Integrated Graphics Cores	Max Turbo Freq. Rate (GHz)	Memory (MHz)	Core Base Freq. (GHz)	Graphic Base Freq (MHz)	TDP	ECC	Package
SR1QM	i7-4790S	C-0	8	4	2	1 Core: 4.0 2 Core: 3.9 3 Core: 3.7 4 Core: 3.6	1600	1.2	350	65	Yes	LGA 1150
SR1QN	i5-4590S	C-0	6	4	2	1 Core: 3.7 2Core: 3.6 3 Core: 3.4 4 Core: 3.3	1600	1.15	350	65	Yes	LGA 1150
SR1PC	i3-4360	C-0	4	2	2	1 Core: 3.7 2 Core: 3.7 3 Core: 3.7 4 Core: 3.7	1600	1.15	350	65	Yes	LGA 1150
SR17Y	E3-1268L v3	C-0	8	4	2	1 Core: 3.3 2 Core: 3.2 3 Core: 2.7 4 Core: 2.7	1600	2.3	350	45W	See notes 1,2	LGA 1150
SR183	i7-4770TE	C-0	8	4	2	1 Core: 3.3 2 Core: 3.2 3 Core: 2.7 4 Core: 2.7	1600	2.3	350	45W	No	LGA 1150
SR17Z	i5-4570TE	C-0	4	2	2	1 Core: 3.3 2 Core: 3.2 3 Core: 3.2 4 Core: 3.2	1600	2.7	350	35W	See notes 1,2	LGA 1150
SR180	i3-4330TE	C-0	4	2	2	1 Core: 2.4 2 Core: 2.4 3 Core: 2.4 4 Core: 2.4	1600	2.4	350	35W	See notes 1,2	LGA 1150
SR1T5	i3-4340TE	C-0	4	2	2	1 Core: 2.6 2 Core: 2.6 3 Core: 2.6 4 Core: 2.6	1600	2.6	350	35W	See notes 1,2	LGA 1150
SR181	G3320TE	C-0	3	2	1	1 Core: 2.3 2 Core: 2.3 3 Core: 2.3 4 Core: 2.3	1333	2.3	350	35W	See notes 1,2	LGA 1150
R182	G1820TE	C-0	3	1	1	NA	1333	2.2	350	35W	See notes 1,2	LGA 1150
SR1T6	G1820TE	C-0	2	2	1	1 Core: 2.2 2 Core: 2.2 3 Core: 2.2 4 Core: 2.2	1333	2.2	350	35W	See notes 1,2	LGA 1150
SR17L	i7-4700EQ	C-0	6	4	2	1 Core: 3.4 2 Core: 3.3 3 Core: 2.8 4 Core: 2.8	1600	2.4	400	47W	Yes	BGA 1364

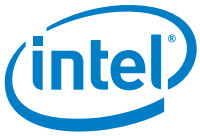

Table 15. 4th Generation Intel® Core™ Processor Family listing/package (Sheet 2 of 2)

Spec #	Processor Number	Stepping	Cache Size (MB)	Func. Core	Integrated Graphics Cores	Max Turbo Freq. Rate (GHz)	Memory (MHz)	Core Base Freq. (GHz)	Graphic Base Freq (MHz)	TDP	ECC	Package
R17M	i5-4400E	C-0	3	2	2	1 Core: 3.3 2 Core: 3.2 3 Core: 3.2 4 Core: 3.2	1600	2.7	400	37W	Yes	BGA 1364
SR1S6	i5-4590T	C-0	6	4	2	1 Core: 3.0 2 Core: 2.9 3 Core: 2.7 4 Core: 2.6	1600	1.15	350	35W	Yes	LGA 1150
R17Q	i5-4402E	C-0	3	2	2	1 Core: 2.7 2 Core: 2.6 3 Core: 2.6 4 Core: 2.6	1600	1.6	400	25W	Yes	BGA 1364
SR1T4	i5-4410E	C-0	3	2	2	1 Core: 2.9 2 Core: 2.9 3 Core: 2.9 4 Core: 2.9	1600	2.9	400	37W	Yes	BGA 1364
SR1T1	i5-4422E	C-0	3	2	2	1 Core: 2.9 2 Core: 2.8 3 Core: 2.8 4 Core: 2.8	1600	1.8	400	25W	Yes	BGA 1364
R17N	i3-4100E	C-0	3	2	2	NA	1600	2.4	400	37W	Yes	BGA 1364
SR1PA	i3-4350T|	C-0	4	2	2	1 Core: 3.0 2 Core: 2.9 3 Core: 2.7 4 Core: 2.6	1600	1.15	200	35W	Yes	LGA 1150
R17R	i3-4102E	C-0	3	2	2	NA	1600	1.6	400	25W	Yes	BGA 1364
SR1T2	i3-4110E	C-0	3	2	2	1 Core: 2.6 2 Core: 2.6 3 Core: 2.6 4 Core: 2.6	1600	2.6	400	37W	Yes	BGA 1364
SR1T0	i3-4112E	C-0	3	2	2	1 Core: 1.8 2 Core: 1.8 3 Core: 1.8 4 Core: 1.8	1600	1.8	400	25W	Yes	BGA 1364
R17S	2000E	C-0	2	2	1	NA	1600	2.2	400	37W	Yes	BGA 1364
R17P	2002E	C-0	2	2	1	NA	1600	1.5	400	25W	Yes	BGA 1364

Notes:
1. ECC enabled when paired with C226 PCH Chipset
2. No ECC when paired with Q87/H81 PCH Chipset

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6.0 Thermal

Refer to the *Haswell Mobile Processor Thermal Design Guide for Embedded Applications* and *Haswell Desktop Processors for Embedded Applications Thermal and Mechanical Design Guide.*

6.1 Thermal Design Power (TDP)

For any thermal design power parameters not identified in Table 16, refer to Mobile Haswell Processor External Design Specification (EDS) Volumes 1, 2.

Table 16. Thermal Design Power (TDP) Specification

Segment	State	Processor Core Frequency	Processor Graphics Core Frequency	Thermal Design Power	Units	Notes
Dual Core BGA Processor with GT2/GT1 Graphics (M-Processor) (25W)	HFM	2.0 GHz up to 3.6 GHz	400 MHz up to 1300 MHz	25	W	1, 2, 3
	LFM	800 MHz	200 MHz	N/A		

Notes:

1. The TDPs given are not the maximum power the processor can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2. TDP workload may consist of a combination of processor-core intensive and graphics-core intensive applications.
3. At T_j of T_{jMAX}

6.2 Junction Temperature Specification

For any junction temperature specification not identified in Table 17, refer to Mobile Haswell Processor External Design Specification (EDS) Volumes 1, 2.

Table 17. Junction Temperature Specification

Segment	Symbol	Package Turbo Parameter	Min	Default	Max	Units	Notes
Dual Core BGA Processor with GT2/GT1 Graphics (M-Processor) (25W)	T_j	Junction temperature limit	0	-	100	°C	1,2,3

Notes:

1. The thermal solution needs to ensure that the processor temperature does not exceed the maximum junction temperature (Tj_{MAX}) limit, as measured by the DTS and the critical temperature bit.
2. The processor junction temperature is monitored by Digital Temperature Sensors (DTS).
3. Digital Thermal Sensor (DTS) based fan speed control is required to achieve optimal thermal performance. Intel recommends full cooling capability well before the DTS reaches Tj_{MAX}. An example of this s Tj_{MAX} - 10°C.

6.3 Package Turbo Parameters

For any package turbo parameters not identified in Table 18, refer to Mobile Haswell Processor External Design Specification (EDS) Volumes 1, 2.

Table 18. Package Turbo Parameters

Segment	Symbol	Package Turbo Parameter	Min	HW Default	Max	Units	Notes
Dual Core BGA Processor with GT2/GT1 Graphics (M-Processor) (25W)	Turbo Time Parameter (package)	Processor turbo long duration time window (POWER_LIMIT_1_TIME in TURBO_POWER_LIMIT MSR 0610h bits [23:17])	0.015	1	448	S	1
	Long P (package)	'Long duration' turbo power limit (POWER_LIMIT_1 in TURBO_POWER_LIMIT MSR 0610h bits [14:0])	-	25	-	W	-
	Short P (package)	'Short duration' turbo power limit (POWER_LIMIT_2 in TURBO_POWER_LIMIT MSR 0610h bits [46:32])	-	1.25 x 25	-	W	-

Note:

1. "Turbo Time Parameters" is a mathematical parameter (unit in seconds) that controls the processor turbo algorithm using a moving average of energy usage. Do not set the Turbo Time Parameter to a value less than 0.1 seconds.

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7.0 ECC Memory Configuration

This chapter contains additional information for the ECC Error Syndrome on the memory bus for any 3rd Generation Intel® Core™ Processor that supports Error Correcting Code (ECC) on the Memory Bus.

7.1 Registers Summary

Refer to *EDS Volume 2 of 2 in Chapter 4.0 Memory Configuration Registers* for complete information on DMIBAR, MCHBAR, and GFXVTBAR Registers.

7.2 Error Syndrome – ERRSYND field in ECCERRLOG0

ECCERRLOG0 register is responsible to logs ECC error information. In bit range 23:16 of ECCERRLOG0, ERRSYND field contains the error syndrome. A value of 0xFF indicates that the error is due to poisoning.

Table 19 explains the error correction syndrome associating with the error signal/data bit. Signal names match the Datasheet and are listed as Sx_ where 'x' is either 'A' for channel A signals or 'B' for channel B signals. This document names the ECC Check Bit signals Sx_DQ[71:64]. The *[Haswell-EP/EP 4S] Processor - External Design Specifications (EDS) Vol.3: Electrical* names the ECC Check Bit signals as DDRx_ECC[7:0] where 'x' is an assigned memory channel.

Table 19. Error Correction Syndrome (Sheet 1 of 2)

Syndrome Value (decimal)	Syndrome Value (Hex)	Error on Data Bit	Error on Signal	Syndrome Value (deci-mal)	Syndrome Value (Hex)	Error on Data Bit	Error on Signal
0	x0	No Error	No Error				
1	x1	64	DDRx_ECC[0] Sx_DQ[64]	81	x51	2	Sx_DQ[2]
2	x2	65	DDRx_ECC[1]	82	x52	18	Sx_DQ[18]
4	x4	66	Sx_ECC_CB[2]	84	x54	34	Sx_DQ[34]
7	x7	60	Sx_DQ[60]	88	x58	50	Sx_DQ[50]
8	x8	67	DDRx_ECC[3]	97	x61	21	Sx_DQ[21]
11	xB	36	Sx_DQ[36]	98	x61	38	Sx_DQ[38]
13	xD	27	Sx_DQ[27]	100	x64	54	Sx_DQ[54]
14	xE	3	Sx_DQ[3]	104	x68	5	Sx_DQ[5]
16	x10	68	DDRx_ECC[4]	112	x70	52	Sx_DQ[52]
19	x13	55	Sx_DQ[55]	128	x80	71	DDRx_EC[7]
21	x15	10	Sx_DQ[10]	131	x83	22	Sx_DQ[22]
22	x16	29	Sx_DQ[29]	133	x85	58	Sx_DQ[58]
25	x19	45	Sx_DQ[45]	134	x86	13	Sx_DQ[13]

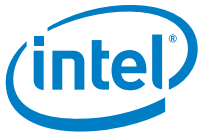

Table 19. Error Correction Syndrome (Sheet 2 of 2)

Syndrome Value (decimal)	Syndrome Value (Hex)	Error on Data Bit	Error on Signal	Syndrome Value (deci-mal)	Syndrome Value (Hex)	Error on Data Bit	Error on Signal
26	x1A	57	Sx_DQ[57]	137	x89	28	Sx_DQ[28]
28	x1C	0	Sx_DQ[0]	138	x8A	41	Sx_DQ[41]
31	x1F	15	Sx_DQ[15]	140	x8C	48	Sx_DQ[48]
32	x20	69	DDRx_ECC[5]	143	x8F	43	Sx_DQ[43]
35	x23	39	Sx_DQ[39]	145	x91	37	Sx_DQ[37]
37	x25	26	Sx_DQ[26]	146	x92	53	Sx_DQ[53]
38	x26	46	Sx_DQ[46]	148	x94	4	Sx_DQ[4]
41	x29	61	Sx_DQ[61]	152	x98	20	Sx_DQ[20]
42	x2A	9	Sx_DQ[9]	161	xA1	49	Sx_DQ[49]
44	x2C	16	Sx_DQ[16]	162	xA2	1	Sx_DQ[1]
47	x2F	23	Sx_DQ[23]	164	xA4	17	Sx_DQ[17]
49	x31	63	Sx_DQ[63]	168	xA8	33	Sx_DQ[33]
50	x32	47	Sx_DQ[47]	176	xB0	44	Sx_DQ[44]
52	x34	14	Sx_DQ[14]	193	xC1	8	Sx_DQ[8]
56	x38	30	Sx_DQ[30]	194	xC2	24	Sx_DQ[24]
64	x40	70	DDRx_ECC[6]	196	xC4	40	Sx_DQ[40]
67	x43	6	Sx_DQ[6]	200	xC8	56	Sx_DQ[56]
69	x45	42	Sx_DQ[42]	208	xD0	19	Sx_DQ[19]
70	x46	62	Sx_DQ[62]	224	xE0	11	Sx_DQ[11]
73	x49	12	Sx_DQ[12]	241	xF1	7	Sx_DQ[7]
74	x4A	25	Sx_DQ[25]	242	xF2	31	Sx_DQ[31]
76	x4C	32	Sx_DQ[32]	244	xF4	59	Sx_DQ[59]
79	x4F	51	Sx_DQ[51]	248	xF8	35	Sx_DQ[35]

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