Industrial Control Remote Lab

Use the Web to securely access and evaluate an industrial reference platform based on the Intel® Atom™ processor

From anywhere in the world, it's possible to explore the capabilities of an embedded Intel® Atom™ processor-based platform by accessing a remote virtual lab across the Internet. Just enter a URL[1] – there's no need to install anything on your PC. Furthermore, this lab enables developers to run the platform, which includes an Altera FPGA, in just a few minutes.

Are you designing PLCs, HMIs, industrial PCs or other industrial controllers? Do you need industrial Ethernet and fieldbus connectivity, a PLC runtime environment and a range of industrial I/Os? Then test drive an Intel Atom processor/FPGA system and learn about its features, evaluate applications, and most importantly, benchmark performance.

Figure 1. Gleichmann Hpe*_IRP System

Industrial Reference Platform

The Remote Lab controls a Gleichmann Hpe*_IRP system, an expandable baseboard supporting a Qseven[2] module with the Intel® Atom™ processor Z5xx series. The Industrial Reference Platform is a highly scalable and re-configurable proof-of-concept platform, targeted at low-power, high-performance industrial automation applications.

The platform, pictured in Figure 1, was designed to help engineers combine FPGA hardware and an x86 CPU, hence the name, Hardware Prototyping and Emulation (Hpe) Industrial Reference Platform (IRP). The board has connectors for two add-in boards intended for custom logic implementations, like FPGAs, and additional peripheral interfaces.

The Qseven COM (computer-on-module) standard allows the latest low-power, embedded processors, chipsets and standard system interfaces to be integrated into a highly compact package without the need for expensive connectors. Measuring just 70mm x 70mm, the module incorporates PCI Express* and other interfaces, such as SATA, USB 2.0, CAN, Ethernet and LVDS, as shown in Figure 2. The specification offers the flexibility to deploy computing systems with various speed grades and memory sizes, thus enabling the development of cost-optimized industrial solutions.

The platform is accompanied by a rich software environment. The Hpe_IRP includes OSADL (Open Source Automation Development Lab) Linux* and CoDeSys,* an IEC-61131 software development system from 3S for evaluation. The Altera Arria* GX FPGA, connected to the Intel Atom processor via PCI Express, is the device-under-test (DUT) and is easily programmed with a complete set of tools to assist engineers during the design process.

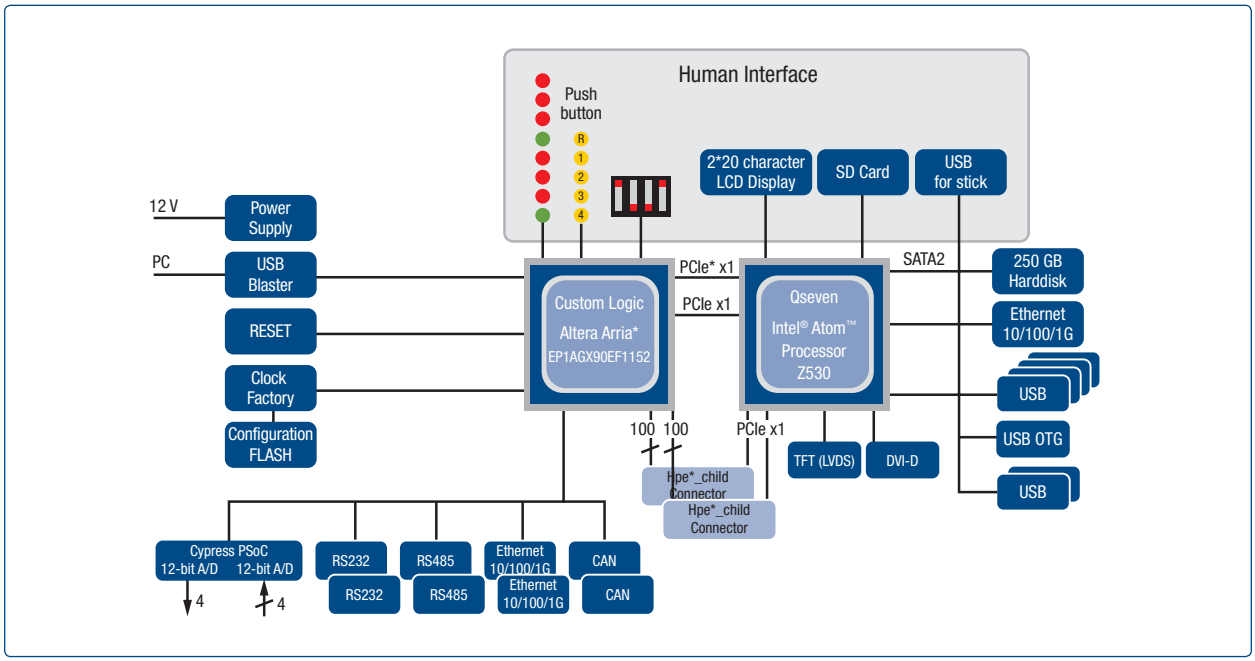

Figure 2. Industrial Reference Platform – Block Diagram

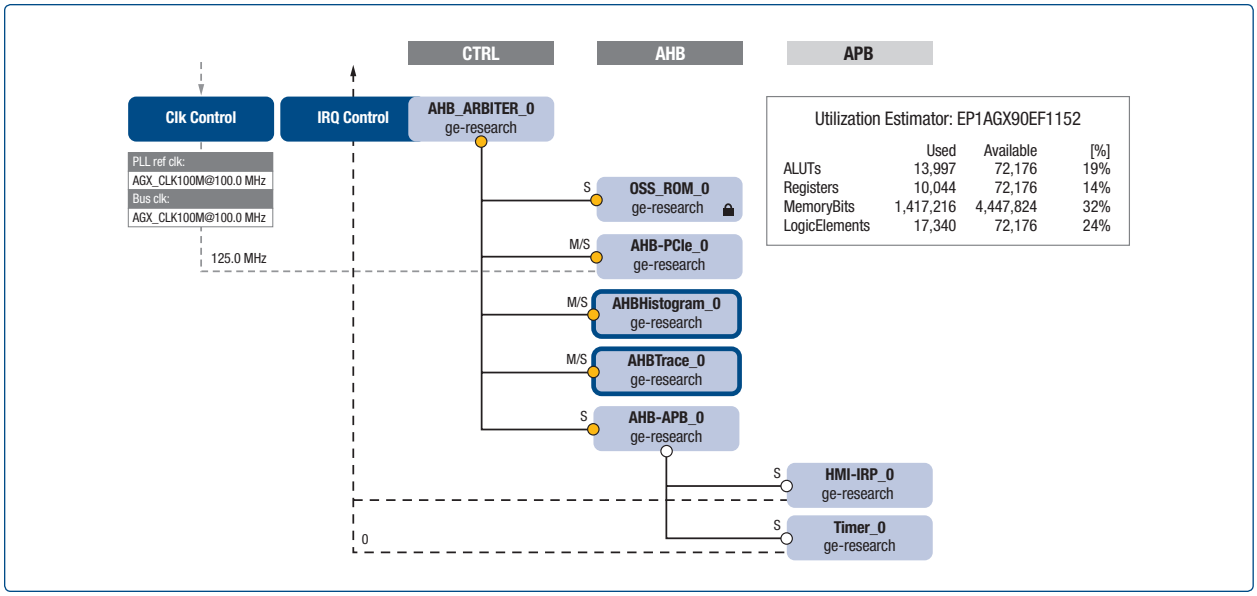

Figure 3. AMBA IP Manager.

In addition, the Hpe_desk supports various tools, such as **Clock Factory** for clock distribution, **JTAG Debugger** for printed circuit board (PCB) and functional debugging, and **AMBA IP Manager**, also called Hpe_AIM. With these tools, it's possible to develop a complete FPGA with Linux operating system support in less than two minutes – not including time to run the automated synthesis and layout, which is dependent upon the size of the FPGA content.

Getting Started

Using a Web browser, remote lab users can access an Industrial Reference Platform with a secure connection (VPN tunnel) to isolated subnets at Intel. First, create an account at **edc.intel.com**, and then select "Embedded remote labs"[1] on the Hardware platforms. If machines are available, you can get started; otherwise, make a reservation for a later time. The Remote Lab provides engineers with a comprehensive and relaxed environment to evaluate the industrial reference platform and supporting development tools. Several tutorials are included to simplify the evaluation process, including:

Tutorial 1 – Introduction to the Industrial Reference Platform

This tutorial provides an introduction to Remote Lab, where users can create an FPGA design and then test it.

Tutorial 2 – Hardware-Based Interrupt Latency Measurement

Interrupt latency is critical for most industrial solutions, and this tutorial enables the user to produce a latency histogram from millions of interrupts, which sometimes generates "interesting" results.

Tutorial 3 – Hardware-Based PCI Express Performance Measurement

The user creates a design and measures the maximum data transfer rates between the Intel Atom processor and the FPGA over the PCI Express bus under different configurations, which can be compared to theoretical numbers presented in the exercise.

Tutorial 4 – Development of an EtherCAT Master Solution

The user develops an FPGA design for an EtherCat fieldbus and runs a small application on an EtherCat system from Beckhoff.

Tutorial 5 – Development of a SERCOS III Master Solution

Demonstrating real-time Ethernet, the user develops an FPGA design with a SERCOS III communications bus and runs an application on an add-in board from Automata.

For developers already using Hpe_IRP, these tutorials are not only informative, but it's possible to download the underlying source code and modify it for a real-world application. Interested users can download the tutorials at **www.ge-research.de/support.html**.

For more information on the Remote Lab, visit **edc.intel.com/Platforms/Remote-Labs**.

[1] http://edc.intel.com/Platforms/Remote-Labs

[2] www.qseven-standard.org

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