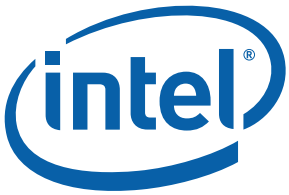

Intel® IXP43X Product Line of Network Processors: Migrating from the Intel® IXP42X Product Line

Application Note

April 2007

Document Number: 316845; Revision: 001US

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Revision History

Date	Revision	Description
April 2007	001	Initial release

1.0 Introduction

This application note facilitates migration of designs based on the Intel® IXP42X Product Line of Network Processors to the Intel® IXP43X Product Line of Network Processors, and Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. Details on hardware design and platform implementation features of the Intel® IXP4XX Product Line of Network Processors are not described in this document.

The following primary subsystems are new or modified from:

The Intel® IXP42X Product Line of Network Processors **to** the Intel® IXP43X Product Line of Network Processors**:**

- Intel XScale® Processor speeds
- Power-supply consideration
- DDRII 400MHz/DDRI 266MHz memory controller with ECC
- Expansion Bus Controller
- USB 2.0 Host controller (high-speed, full-speed and low-speed) and EHCI-compliant SPI/SSP Serial Peripheral Port (supports Motorola* Serial Peripheral Interface, National Semiconductors* MicroWire*, and Texas Instruments* Synchronous Serial Protocol operations)
- Intel XScale processor Memory Port Interface
- NPE Memory Increase
- Interrupt Controller (increase to 64 interrupts)
- GPIO Update (added multiplex for Spread-Spectrum)

The Intel® IXP42X Product Line of Network Processors **to** the IXP45X/IXP46X network processors**:**

- Intel XScale processor speeds
- Power-supply consideration
- DDRI 266 memory controller with ECC
- Expansion Bus Controller
- USB 2.0 Host controller (full-speed and low-speed) and EHCI-compliant
- I^2C hardware
- Three Ethernet ports with MII/SMII interfacing
- SPI/SSP Serial Peripheral Port (supports Motorola* Serial Peripheral Interface, National Semiconductors* MicroWire*, and Texas Instruments* Synchronous Serial Protocol operations)
- IEEE 1588 hardware assistance
- Ethernet Switching Coprocessor (SWCP)
- Cryptography Engine (Random Number Generator, SHA, and Exponentiation Unit)
- Intel XScale processor Memory Port Interface
- NPE Memory Increase
- Interrupt Controller (increase to 64 interrupts)
- GPIO Updates (added multiplex for Spread-Spectrum and IEEE-1588 hardware assistance)

Note: This application note discusses all features supported on the IXP43X network processors and the IXP45X/IXP46X network processors. A subset of these features is

supported by certain processors in the Intel® IXP43X Product Line/IXP4XX product line such as the IXP420 or IXP455 network processors. For details on feature support listed by processor, see the *Intel® IXP43X Product Line of Network Processors Datasheet.*

The basic functions in the board support package (BSP), device driver, and application software are discussed to assist users to easily migrate the existing platforms into the new processors with the advanced features.

The following sections provide a general description of the architectural and functional differences between the IXP42X processors to the IXP43X network processors and the IXP4XX product line. This application note is not intended to provide in detail how a specific feature or function is implemented or used in applications. See the technical manuals listed in Section 1.1, "Related Documentation" to know more about feature implementation.

1.1 Related Documentation

Title	Document Number
Intel® IXP43X Product Line of Network Processors Datasheet	316842
Intel® IXP43X Product Line of Network Processors Developer's Manual	316843
Intel® IXP43X Product Line of Network Processors Hardware Design Guidelines	316844
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual	306262
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Hardware Design Guidelines	305261
Intel® IXP4XX Product Line of Network Processors Specification Update	306428
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP42X Product Line of Network Processors Hardware Design Guidelines	252817
Intel® IXP400 Software Programmer's Guide	252539

1.2 Acronyms

BSP	Board Support Package
DDR	Double-Data-Rate SDRAM
GPIO	General-Purpose Input/Output Interface
MAC	Media Access Control
MCU	Memory Controller Unit
MII	Media-Independent Interface
MPI	Memory Port Interface
NPE	Network Processor Engine
PWB	Printed Wiring Board
SDRAM	Synchronous DRAM
SMII	Serial, Media-Independent Interface
SPI	Serial Peripheral Interface
SSP	Synchronous Serial Protocol

2.0 Product Feature Comparison

This section describes the architectural feature set of the Intel® IXP4XX Product Line of Network Processors and the differences between the Intel® IXP42X Product Line of Network Processors, Intel® IXP43X Product Line of Network Processors and the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors.

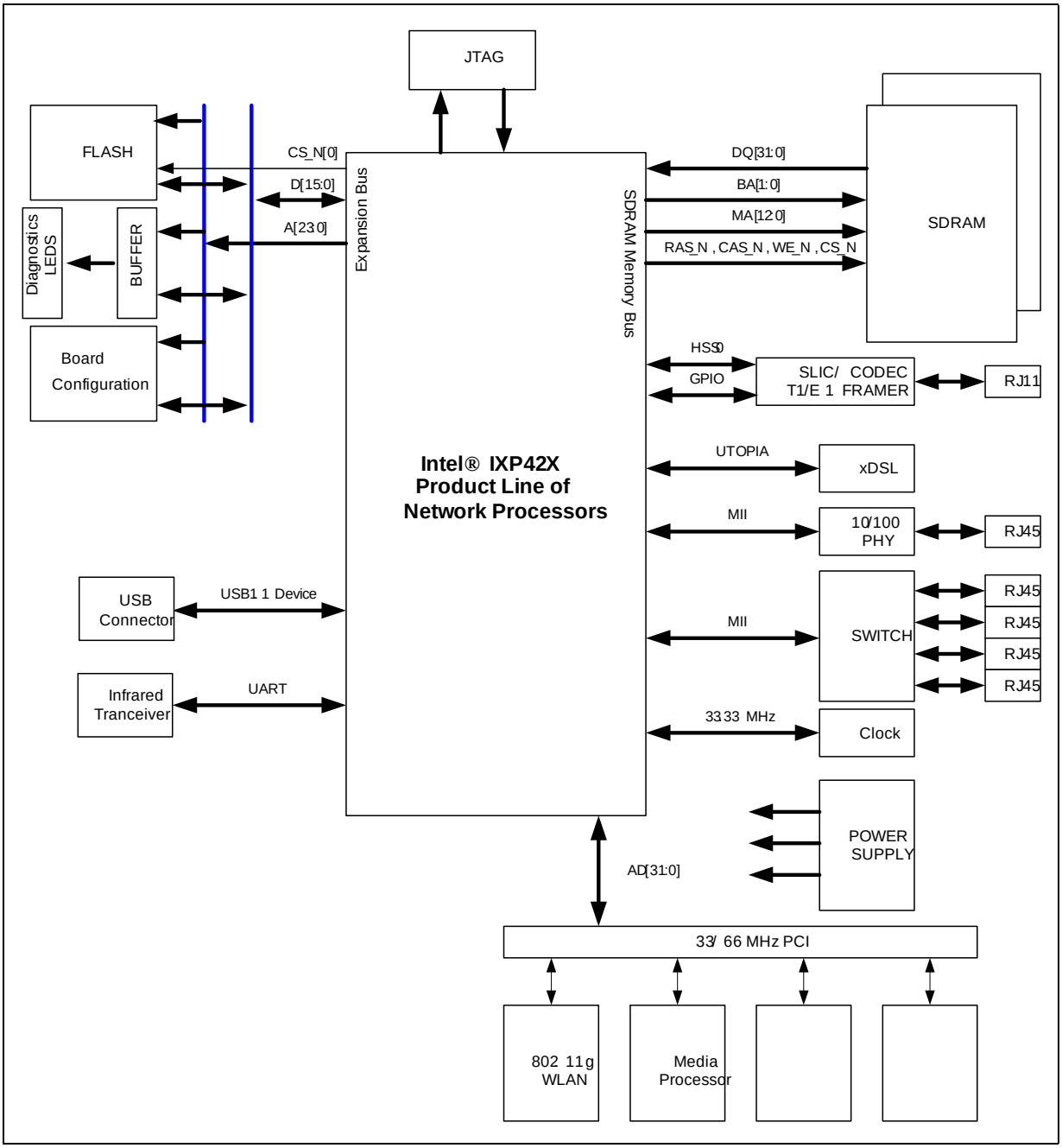
2.1 Features of the Intel® IXP42X Product Line of Network Processors

The IXP42X processors are highly integrated devices designed to provide design flexibility and reduce system-development costs. The IXP42X processors include features such as the UARTs, watch-dog timer (WDT), general-purpose timers, three Network Processor Engines (NPEs) for two Ethernet and one UTOPIA interface, PC 133 SDRAM, GPIO, PCI 2.2 and a 16-bit Expansion Bus Controller that is interfaced and implemented in many applications such as embedded networking and communications.

Figure 1 illustrates an example of the basic system block diagram of the IXP42X processors. Features of the IXP42X processors include:

- Intel XScale® Processor up to 533 MHz
- Three Network Processor Engines (NPE's)
- PCI 2.2 Interface
- Two MII Interfaces
- UTOPIA Level 2 Interface
- USB 1.1 Device Controller
- Two High-Speed Serial Interfaces
- PC 133 SDRAM Interface
- Encryption/Authentication
- High-Speed UART
- Console UART
- Internal Bus Performance Monitoring Unit
- 16 GPIOs
- WDT Watchdog Timer
- General-Purpose Timers
- Packaging: 492-Pin PBGA
- Commercial/Extended Temperature

Figure 1. Intel® IXP42X Product Line of Network Processors System Block Diagram



2.2 Features of the Intel® IXP43X Product Line of Network Processors

The IXP43X network processors are designed with Intel 0.13-µ process technology targeting low cost networking applications with industry leading performance

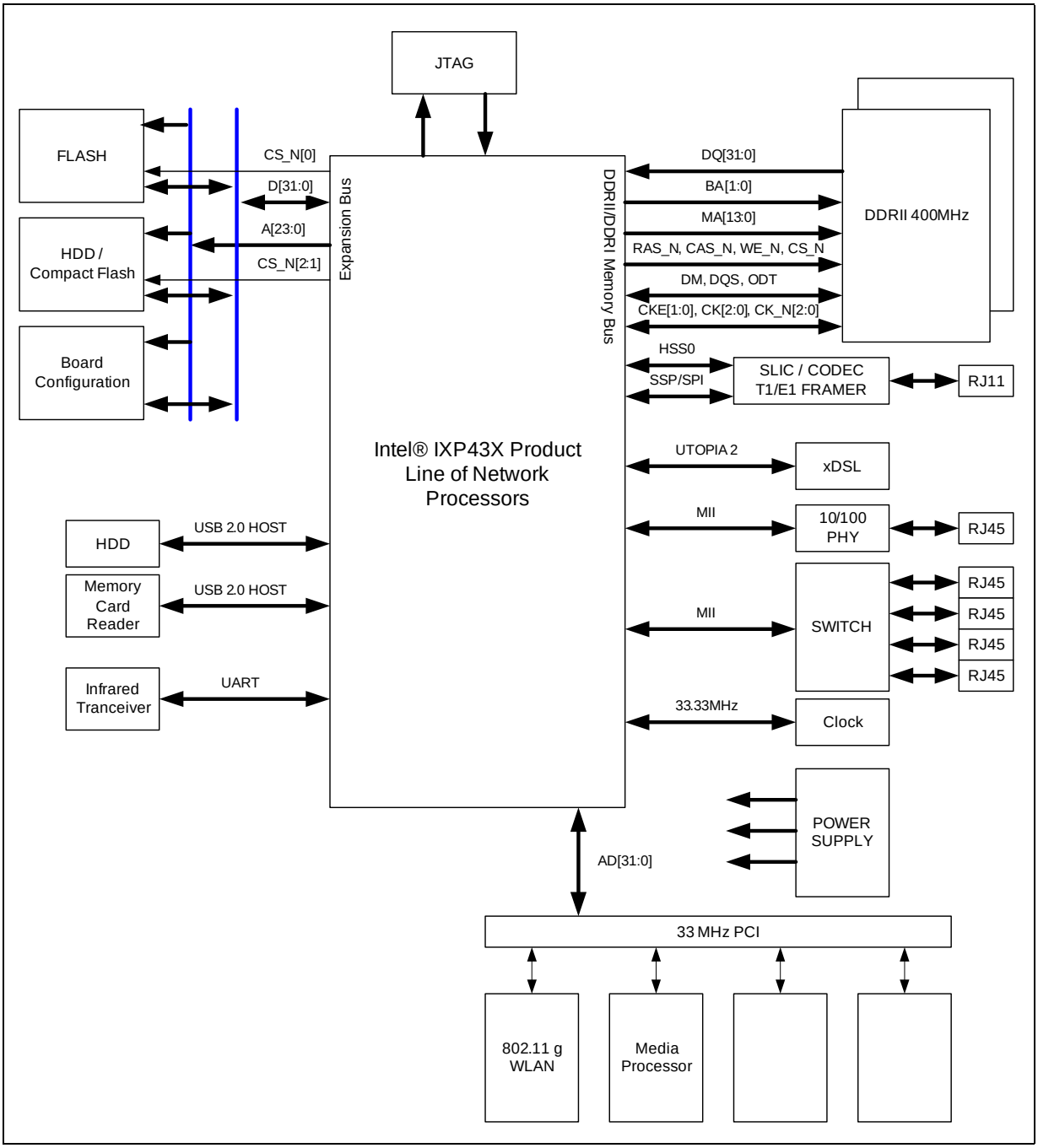
Features include functions such as the UART, a watch-dog timer (WDT), general-purpose timers, two Network Processor Engines (NPEs), for up to two Ethernet and/or one UTOPIA interface, 16-bit/32-bit DDRI-266/DDRII-400 SDRAM; SPI/SSP; GPIO; PCI-2.2, bulk-encryption acceleration; HSS; 8-bit/16-bit target capable expansion bus and two USB 2.0 Host high-speed support.

Figure 2 illustrates an example of the basic system block diagram of the IXP43X network processors. Features of the IXP43X network processors include:

- Intel XScale processor with speeds up to 667 MHz
- Dedicated Memory Port Interface for the Intel XScale processor
- Two Network Processor Engines with expanded, internal memory
- PCI v2.2 33 MHz (Host/Option)
- Up to two MII Interfaces
- Up to one UTOPIA Level 2 Interface
- Two USB 2.0 Host controllers
- One High-Speed Serial Interface
- 16-bit/32-bit DDRII 400MHz/DDRI 266MHz SDRAM Interface with ECC
- Target Capable Expansion Bus
- Spread-Spectrum-Clock clocking for reduced EMI
- Encryption/Authentication (AES/AES-CCM/3DES/DES/SHA-1/SHA-256/ SHA-384/SHA-512/MD-5)
- One UART
- Internal Bus Performance Monitoring unit
- 16 GPIOs
- Four Internal Timers
- Synchronous Serial Protocol (SSP) port
- Packaging: 460-pin PBGA lead-free compliance
- Commercial temperature

Note: ECC is implemented only over 32-bit mode of operation.

Figure 2. Intel® IXP43X Product Line of Network Processors System Block Diagram



Note: Only one 10/100 MAC is available if the UTOPIA interface is used.

2.3 Features of the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors

The Intel® IXP45X and Intel® IXP46X Product Line of Network Processors extend the capabilities of the existing IXP42X processors. These processors introduce a variety of advanced features integrated on the device.

The IXP45X/IXP46X network processors are designed with Intel 0.18-µ process technology, allowing the processor to provide a high-performance Intel XScale processor and greater design flexibility which reduces system-development costs and complexity.

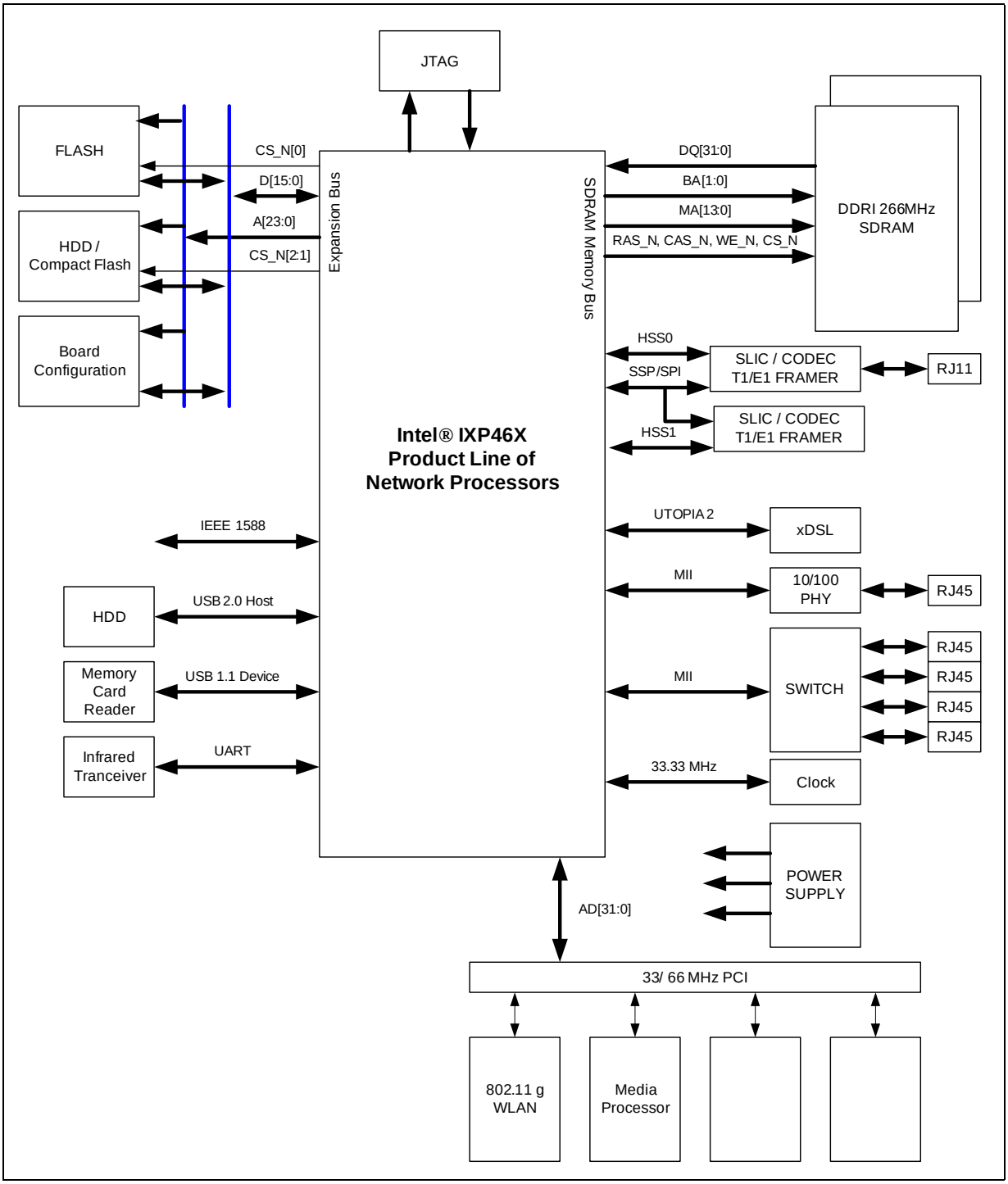
Features include functions such as the UARTs, a watch-dog timer (WDT), general-purpose timers, three Network Processor Engines (NPEs), for up to three Ethernet and/or one UTOPIA interface. Other features are faster, DDRI-266 SDRAM; I^2C; SPI/SSP; GPIO; PCI-2.2, IPSec Cryptography acceleration; bulk-encryption acceleration; HSS; and a 32-bit Host/Slave Expansion Bus controller that is interfaced and implemented in applications such as embedded networking and communications.

Features of the IXP45X/IXP46X network processors include:

- Intel XScale processor with speeds up to 667 MHz
- Dedicated Memory Port Interface for the Intel XScale processor
- Three Network Processor Engines with expanded, internal memory
- PCI v2.2 33/66 MHz (Host/Option)
- Up to three MII Interfaces
- Up to three SMII Interfaces
- One UTOPIA Level 2 Interface
- USB 2.0 Host controller
- USB 1.1 Device Controller
- Two High-Speed, Serial Interfaces
- DDRI SDRAM Interface with ECC
- IEEE-1588 hardware assist
- Master/Target Capable Expansion Bus
- Spread-Spectrum-Clock clocking for reduced EMI
- Cryptography unit (Random Number Generator and Exponentiation unit are expansions to previous NPE Crypto section implementation)
- Encryption/Authentication (AES/AES-CCM/3DES/DES/SHA-1/SHA-256/SHA-384/SHA-512/MD-5)
- Two UARTs
- Internal Bus Performance Monitoring unit
- 16 GPIOs
- Four Internal Timers
- I^2C Interface
- Synchronous Serial Protocol (SSP) port
- Packaging: 544-pin PBGA and lead-free support
- Commercial/extended temperature

Figure 3 illustrates the basic system block diagram of the IXP46X product line.

Figure 3. Intel® IXP46X Product Line of Network Processors System Block Diagram



2.4 Architecture Overview of the Intel® IXP43X Product Line and IXP45X/IXP46X Product Line

Figure 4 and Figure 5 show system block diagrams of the IXP43X network processors and the Intel® IXP46X Product Line of Network Processors - a complete system-on-a-chip designed to deliver high performance for the interchange and processing of network data.

A key functional unit is the Intel XScale processor, the main controller or **traffic cop** of the device. After the internal interfaces are configured and initialized, the Intel XScale processor gets a big assist from the Network Processing Engines (NPEs).

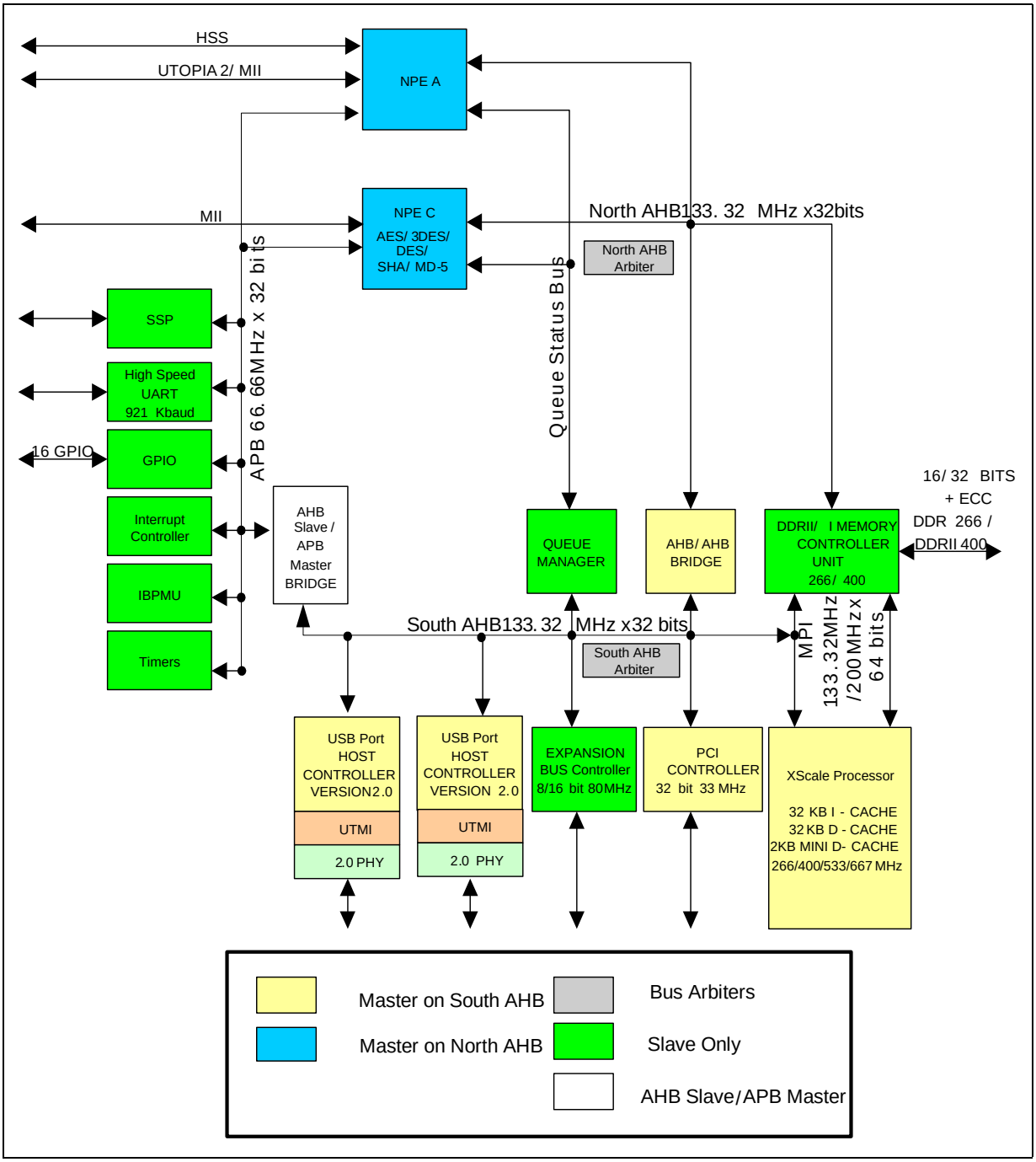
The NPE processors off-load much of the work needed to move data packets and feature additional local hardware-assist functions called coprocessors. These hardware-logic coprocessors handle the processor-intensive functions such as MII (MAC); CRC checking and generation; AAL segmentation and re-assembly; and security functions such as AES, AES-CCM, DES, 3DES, SHA1/256/384/512, and MD-5.

The data flows from all these devices are significant, so a segmented layout of internal buses is used to help the processing elements perform parallel processing of data. These buses are seen on the block diagram as the North AHB, the South AHB, the Memory Port Interface, and the APB.

All the external interfaces pathways connect to elements on these various buses and each particular interface or type of data flow being associated with an internal bus or processing element specifically tailored to the performance characteristics required for that interface.

Additional hardware elements are described in the remaining sections of this document. For more detailed information on all these architectural features and their special characteristics, refer to the technical manuals listed in Section 1.1, “Related Documentation”.

Figure 4. Intel® IXP43X Product Line of Network Processors Functional System Block Diagram



2.4.1 Advanced Features in the Intel® IXP43X Product Line of Network Processors vs. Intel® IXP42X Product Line of Network Processors

The IXP43X network processors have a variety of advanced features that are not available in the IXP42X processors, which include:

- **SPI/SSP —** This is an SPI master only and also supports National MicroWire*, SSP protocol from TI* and Motorola serial peripheral interface (SPI)* protocol.
- **GPIO —** The general purpose input/output peripheral provides dedicated functions as on the IXP42X processors. In addition, GPIO pins is configured as the alternate functions. New details include:
  - AMBA APB interface
  - Two snapshot trigger inputs
  - NPE debug functionality
  - GPIO_IN[7:0] signals are individually routed directly through to NPEs

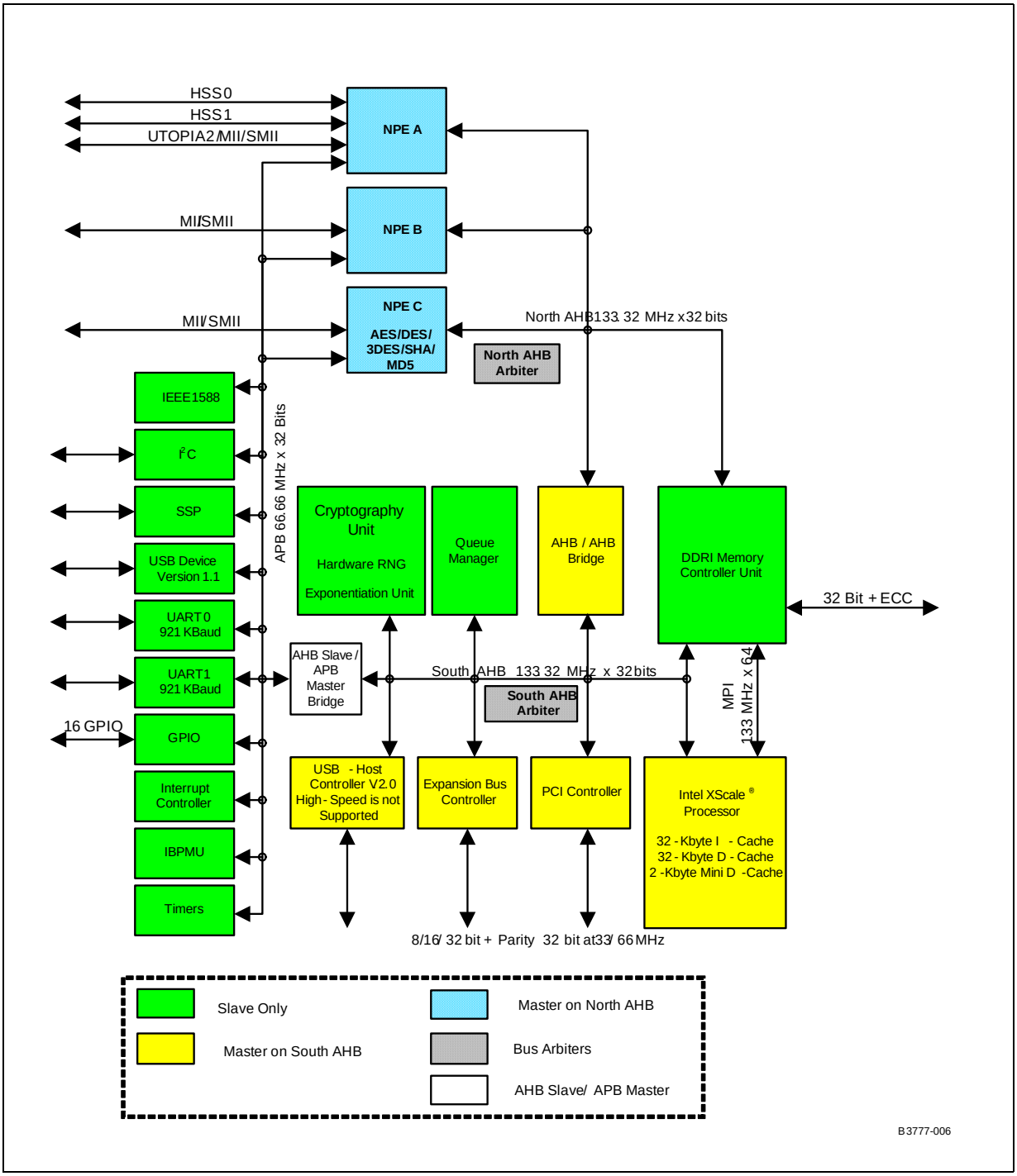
  For more information on how to interface these signals, see the *Intel® IXP43X Product Line of Network Processors Datasheet*.
- **Interrupt Controller —** The number of possible IRQ interrupts has been expanded from 32 to 64. Additional interrupt sources known as the error interrupts have also been introduced. The interrupts are configured as FIQ or IRQ interrupts.
- **Expansion Bus —** This is a target Expansion Bus controller. It provides 4 chip selects, a 24-bit address bus, a 16-bit-wide data interface and enhancement of configuration strapping to include more strapping options.

  The maximum clock rate that the expansion interface can accept is 80 MHz.
- **DDRII-400MHz and DDRI-266MHz SDRAM —** This is the DDRII-400MHz/ DDRI-266MHz SDRAM Controller with a 16-bit or 32-bit wide data path. The DDRII/ DDRI interface in conjunction with the dedicated MPI port provides higher bulk memory performance. The optional ECC support provides more system reliability for 32-bit implementation.
- **Dedicated Memory Port Interface** for the Intel XScale processor — The Intel XScale processor has a dedicated path to the memory controller; this provides effective performance in Intel XScale processor memory accesses.
- **Soft Fuses** — This feature can save the use of external pull-up and pull-down resistors, if the fused interfaces are not used.
- **USB 2.0 High Speed Host —** The USB Host controller employed on the IXP43X network processors is an EHCI-compliant controller. It is capable of supporting high-speed, full-speed and low-speed.
- Intel XScale processor **—** Supports operating frequencies up to 667 MHz.
- **Package Size** — 31 mm by 31 mm in size, 460-pin PBGA. The PWB designs of the IXP42X processors, which use a 35-mm by 35-mm package, must be re-layout with the appropriate footprint for the IXP43X network processors.

Table 1 summarizes the key feature differences between the Intel® IXP4XX Product Line of Network Processors.

Note: Table 1 lists all features supported on the IXP43X network processors. A subset of these features is supported by certain processors in the Intel® IXP43X Product Line. For details on feature support listed by processor, see *Intel® IXP43X Product Line of Network Processors Datasheet*.

Figure 5. Intel® IXP46X Product Line of Network Processors Functional System Block Diagram



2.4.2 Advanced Features in the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors vs. Intel® IXP42X Product Line of Network Processors

The IXP45X/IXP46X network processors have a variety of advanced features that are not available in the IXP42X processors, which include:

- **SPI/SSP —** This is an SPI master only and also supports National MicroWire*, SSP protocol from TI* and Motorola serial peripheral interface (SPI)* protocol.
- **GPIO —** The general purpose input/output peripheral provides dedicated functions as on the IXP42X processors. In addition, GPIO pins are configured as the alternate functions. New details include:

  - AMBA APB interface
  - Two snapshot trigger inputs
  - NPE and IEEE 1588 debug functionality
  - GPIO_IN[7:0] signals are individually routed directly through to NPEs

  Refer to *Intel® IXP43X Product Line of Network Processors Datasheet* for more information on how to interface these signals.
- **Interrupt Controller —** The number of possible IRQ interrupts has been expanded from 32 to 64. Additional interrupt sources known as the error interrupts have also been introduced. The interrupts are configured as FIQ or IRQ interrupts.
- **I^2C —** This is an I^2C master and Slave controller integrated on chip.
- **Expansion Bus —** This is an advanced master/target Expansion Bus controller. It provides 8 chip selects, a 25-bit address bus, a 32-bit-wide data interface and also supports even/odd parity generation and checking in all external modes and in some legacy modes (Intel®- and Motorola*-style bus cycles). ZBT* SRAM flow-through burst support and the enhancement of configuration strapping to include more strapping options is an additional new feature.

  The maximum clock rate that the expansion interface can accept is 80 MHz.
- **DDRI SDRAM —** This is the DDRI-266 SDRAM Controller with a 32-bit wide data path. The DDRI interface in conjunction with the dedicated MPI port provides higher bulk memory performance. The optional ECC support provides more system reliability.
- **Dedicated Memory Port Interface** for the Intel XScale processor — The Intel XScale processor has a dedicated path to the memory controller, this makes for more effective performance in Intel XScale processor memory accesses.
- **Soft Fuses** — This feature can save the use of external pull-up and pull-down resistors, if the fused interfaces are not used.
- **USB 2.0 Full-speed Host —** The USB Host controller employed on the IXP45X/ IXP46X network processors is an EHCI-compliant controller.
- **MII/SMII —** The IXP4XX product line provides up to three MII ports or up to three SMII ports.
- Intel XScale processor **—** Supports operating frequencies up to 667 MHz.
- **IEEE-1588 Controller —** This is an IEEE standard and used as a clock-synchronization protocol for network measurement and control system applications.
- **Package Size** — This is still 35 mm by 35 mm in size, but an inner row of PBGA pins have been added to make it a 544-pin PBGA. The PWB designs of the IXP42X processors, which use a 35-mm by 35-mm package, is reused by refreshing the PWB with the appropriate footprint for the IXP4XX product line.

- **Cryptography Unit** — Random Number Generator and Exponentiation Unit are expansions to previous NPE-crypto hardware. Security methods supported include Encryption/Authentication of AES/AES-CCM/3DES/DES/SHA-1/SHA-256/SHA-384/SHA-512/MD-5.

Table 1 summarizes the key feature differences between the Intel® IXP4XX Product Line of Network Processors.

Note: Table 1 lists all features supported for the Intel® IXP4XX Product Line of Network Processors. A subset of these features is supported by certain processors in the IXP4XX product line, such as the IXP420 in the Intel® IXP42X Product Line of Network Processors. Refer to the appropriate Datasheet (see Section 1.1, "Related Documentation") for details on feature support listed by processor.

Table 1. Key Differences between Processor Product Lines (Sheet 1 of 2)

Feature	Intel® IXP42X Product Line of Network Processors	Intel® IXP43X Product Line of Network Processors	Intel® IXP45X and Intel® IXP46X Product Line of Network Processors
Processor Speed (MHz)	266 / 400 / 533	266 / 400 / 533 / 667	266 / 400 / 533 / 667
Cryptography Unit †	N/A	N/A	X
Interrupt Controller	Support to 32	Support to 64	Support to 64
UTOPIA Level 2†	X	X	X
GPIO Pins	16	16	16
Alternate Functions GPIO Pins	N/A	Spread-Spectrum-Clock Support	Support IEEE 1588 (Use GPIO 7 and GPIO 8 as Alternative Functions) and Spread-Spectrum-Clock Support
UART 0	X	X	X
UART 1	X	N/A	X
HSS 0†	X	X	X
HSS 1†	X	N/A	X
MII/SMII 0†	MII	MII	MII/SMII
MII/SMII 1†	MII	MII	MII/SMII
MII/SMII 2†	N/A	N/A	MII/SMII
USB 1.1 Device Controller	X	N/A	X
USB 2.0 Host Controller	N/A	2	1 Does not support high speed mode
IEEE-1588 Hardware Assistance	N/A	N/A	Supported on the IXP46X product line only
I^2C	X (Software Emulation)	X (Software Emulation)	X
PCI	32-bit, 66MHz	32-bit, 33-MHz	32-bit, 66MHz
Expansion Bus	16-bit, 8 CS, 66-MHz	16-bit, 4 CS, 80-MHz	32-bit, 8 CS, 80-MHz, Host Support
SDRAM Controller	SDRAM 32-bit, 133-MHz	N/A	N/A
DDRI 266 Controller	N/A	16-bit/32-bit, 266-MHz	32-bit, 266MHz
DDRII 400 Controller	N/A	16-bit/32-bit, 400-MHz	N/A
AES / DES / 3DES†	X	X	X
AES-CCM †	N/A	X	X
† These features require software to be operational.			

Table 1. Key Differences between Processor Product Lines (Sheet 2 of 2)

Feature	Intel® IXP42X Product Line of Network Processors	Intel® IXP43X Product Line of Network Processors	Intel® IXP45X and Intel® IXP46X Product Line of Network Processors
Multi-Channel HDLC †	8	4	8
SHA / MD-5†	X	X	X
SPI/SSP	N/A	X	X
Commercial Temperature	X	X	X
Extended Temperature	X	N/A	Supported on the IXP46X product line only
† These features require software to be operational.			

3.0 Migration Considerations for the Intel® IXP42X Product Line of Network Processors to the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors

3.1 Hardware Migration Considerations

Refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Hardware Design Guidelines* for recommendations on how to design with the new hardware features included in the IXP45X/IXP46X network processors.

3.2 Software Migration Considerations

The IXP42X processors and IXP45X/IXP46X network processors can use the same basic set of application software and firmware drivers. They both share a common Intel XScale® Processor architecture and application feature set.

The exception to this is where there are differences due to updated/extended features or new processor features. Software programmers must be aware of the implications of the new features and changes in the operational methods of some features such as the DDR memory controller.

The implementation feature differences from the IXP42X processors' family requires software changes in existing code. This primarily applies to board support package (BSP) code, but can also apply to application-level programs. The following sections describe the areas where software changes should be anticipated, and planned for accordingly by the software engineering organizations of customers interested in using the IXP45X/IXP46X network processors. Figure 5 on page 18 shows a block diagram of the IXP46X product line.

The IXP45X/IXP46X network processors require IXP400 software v2.0 or later.

3.2.1 Processor Initialization and Boot Strap

This is a role normally handled by a boot loader. The majority of the existing bootloader code can be the same for each operating system. In any case, the processor initialization must be updated, to accommodate the updated processor register set and new features. The areas in need of updates are SDRAM configuration for DDR and timers.

3.2.2 Processor Software Advanced Features

Real-time operating systems such as VxWorks*, Linux*, Microsoft Windows* CE,.NET*, and any high-level applications running on top of those RTOS is not affected by the change from the IXP42X processors to the IXP45X/IXP46X network processors. An RTOS typically utilizes a BSP and associated device drivers to communicate with the new hardware and architectural advanced features. These BSPs and device drivers are subject to change to support new features of the IXP45X/IXP46X network processors.

These changes include, but are not limited to:

- Interrupt handling
- Ethernet physical-layer devices (PHYs) through the NPEs
- DDR devices through the DDR-SDRAM memory controller
- SPI/SSP interface

- Internal I^2C controller
- DMA controller
- Queue Manager

While porting code from the IXP42X processors to the IXP45X/IXP46X network processors, software migration and porting considerations require the most attention. New features not supported in the IXP400 software access layer, via an associated access component, must be accounted for with new device drivers or BSP changes in customer code.

Detailed software code descriptions or examples of modifications and changes to BSPs are outside this application note's scope, since these changes are not only RTOS dependent, but hardware-platform-dependent as well. Software programmers should consult the detailed descriptions of the registers, instructions and operational modes of each new hardware feature by referring to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

The following sections provide an overview of new and/or enhanced processor components that requires an update in the board support package (BSP).

3.2.2.1 DDRI-266 Memory Controller

The IXP45X/IXP46X network processors use a DDRI-266MHz memory controller instead of the SDRAM memory controller used by the IXP42X processors family. The memory controller can use error-correcting memory (ECC) to increase reliability by detecting double-bit errors and by detecting and correcting single-bit errors.

This memory needs new code to enable its operation and to allow the system using the IXP45X/IXP46X network processors to initialize the memory array. That is because the programmer-accessible configuration elements are not the same as the SDRAM-based external memory used in the IXP42X processors.

The programmer must address the DDRI SDRAM configuration, the specified JEDEC memory initialization sequence, timing, and refresh-rate setup.

In Linux, the primary impact is to the boot loader, as the Linux* kernel expects the boot loader to set up and initialize the RAM. This development is being accommodated by Intel with updates to the RedBoot* boot loader.

Additional consideration is necessary for ECC interrupt handling and scrubbing. The interrupts can be set up by the boot loader, but this is generally in the realm of the OS initialization. The OS must accommodate setup of the interrupts for the time period between boot and when the access library functionality is activated.

Note: JTAG vendors must alter their mini-ICache-based JTAG unit driver code to accommodate the new memory initialization scheme.

3.2.2.2 MPI Port Initialization

There are two additional considerations that must be addressed while coding the memory controller configuration sequences. These have to do with steering for the Memory Port Interface port to the Intel XScale processor and setting the arbitration between the MPI port and AHB buses for equal bandwidth.

The registers and bits involved with these requirements are described in the following paragraphs and Table 2.

The MPI Enable bit (MI_EN, bit 31) is located in the Expansion Bus Configuration Register 1 (EXP_CNFG1) and controls how the Intel XScale processor accesses the external DDR memory. If set to a zero, the Intel XScale processor will **not** take advantage of the increased speed possible with the new dedicated MPI port to the controller. Instead, the Intel XScale processor routes all core-initiated DDR transactions though the AHB bus.

For maximum performance, this bit should implicitly be set to a one before doing the remainder of the DDR section configuration in the boot-up process. There is another operation that should be performed before setting the MIP_EN bit to a one (1).

The BSP or platform initialization code should copy the code from 0 – 256 Mbyte in the flash to DDRI SDRAM over the same address space **before** setting the MPI_EN bit to 1.

The implications of the settings that is the default at power on/reset are the reasons behind the need for this action, and they are described as follows:

- At power on/reset:
  - MEM_MAP in the **exp bus config reg 0** is 1.
    This means that the flash is at address 0x0.
  - MPI_EN in the **exp bus config reg 1** is 0.
    This means all the Intel XScale processor bus transactions are over the South AHB. The MPI port between the Intel XScale processor and the memory controller is disabled.

  The Intel XScale processor fetches the power on/reset exception vector from address 0x0, which is in flash.
- The potential problem:

  If MPI_EN is set to 1, all Intel XScale processor access from 0 – 1 Gbyte goes to the MPI port and not to the AHB. This includes instructions fetches.

  While the Intel XScale processor is fetching instructions from 0 – 256 Mbyte (the flash) and has not copied its code from flash to DDRI SDRAM at the same address first, there is no code to execute in DDRI SDRAM and the core fetches garbage and hangs.

  By making sure that the code from 0 – 256 Mbyte in the flash is copied to SDRAM, thus covering the same address space **before** setting the MPI_EN bit to 1, this problem will not occur.

The MCU Port Transaction Count Register (MPTCR) register must be configured to have equal bandwidth between the MPI port and the AHB bus. This register is not programmed with this setting by default, requiring that it be implicitly set. A value of 0x11H sets the IXP45X/IXP46X network processors to a level that prevents unfair arbitration and indeterminate results.

Having the option to control arbitration, and thus the bandwidth utilization over these busses, can be useful for performance balancing of the buses while application optimization efforts are being made. For initial bring up of a platform based on the IXP45X/IXP46X network processors, the 0x11H value is recommended.

Table 2. MPI Port Registers

Register	Signal Name [Bit]	Description
EXP_CNFG1 Expansion Bus configuration Register 1	MPI_EN [31]	This bit should always be set while configuring the DDR during boot-up. when this bit is set, the performance between the Intel XScale processor and DDR is increased. • 0 = DDR transactions are routed through the AHB. • 1 = DDR transactions are routed through the MPI port.
MPTCR MCU Port Transaction Count Register	MPTCR [07:04]	North and South AHB Transaction Count: Number of transactions the IB MCU port can have processed in a single tenure of the DDRI SDRAM. • 1H = 1 transaction • 2H = 2 transaction • 3H = 3 transaction • ... • FH = 15 transactions • 0H = 16 transactions
MPTCR MCU Port Transaction Count Register	MPTCR [03:00]	Core Transaction Count: Number of transactions the core processor MCU port can have processed in a single tenure of the DDRI SDRAM. • 1H = 1 transaction • ... • FH = 15 transactions • 0H = 16 transactions

3.2.2.3 Timers

There are ten new registers for the timer subsystem of IXP45X/IXP46X network processors. The number of timers in the system has stayed the same.

There are two general-purpose down timers named Timer0 and Timer1. Timer0 is generally used for the OS time-keeper while Timer1 is generally available for use by application programmers. Additionally, there is a countdown Watchdog timer and a count-up Time-stamp timer.

Notes on the additional functionality:

- The timestamp timer has a reload value of `0000_0001`.
- The timers (except the watchdog) allows for a prescaler.
- The timer allows for a three-fourths-rate operation mode which is used to simulate a 20 ns (50 MHz) clock as opposed to the APB, 66.66-MHz clock.
- The time-stamp-compare register allows interrupts on a match with the time stamp count-up register. Previously, the time stamp register could only trigger an interrupt on rollover. The value does not automatically reset to 0 on interrupt trigger.
- Configuration register allows the associated timer to be stopped while in 20-ns mode. Pausing the timer is not possible as the timer can be stopped but it cannot be restarted from the place it stopped.

Refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual* for register information.

3.2.2.4 IEEE 1588 Time Synchronization

The IEEE-1588 interface is a new feature for the IXP45X/IXP46X network processors, and requires new code to enable it in any BSP or associated device driver. It is not necessary to have direct support for this in the BSP as configuration and control is handled by an IXP400 software Access Library component.

The access component enables the client application or other modules which implement the IEEE-1588 Precision Clock Synchronization Protocol (PTP) for Network Measurement and Control Systems, to configure the IEEE-1588 Time Synchronization Hardware Assist Block. The hardware assist captures the time stamps at each of the MII interfaces on NPE-A/B/C, for both incoming or outgoing PTP protocol messages, which are multicast over UDP/IP packets in IPv4 format.

This component only enables the hardware assist block and *does not implement* the IEEE 1588 protocol.

3.2.2.5 PCI Controller

The PCI controller setup is handled by the BSP code. This BSP layer is subject to change based on silicon fixes to the PCI subsystem while moving from the B1 silicon of the IXP42X processors to the IXP45X/IXP46X network processors.

The known modifications to the PCI hardware can be derived from the following errata of the Intel® IXP42X Product Line of Network Processors:

- SCR 1289 — PCI Controller returns infinite retries on PCI after AHB prefetch error
- SCR 2372 — PCI Controller DMA deadlock problem
- SCR 2370 — PCI Controller does not drive correct byte-enables on non-prefetch read
- SCR 2831 — PCI Memory Byte enables: Prefetch Reads
- SCR 3364 — PCI deadlock during outbound burst writes

The software workaround in place for the errata is required to detect the processor and disable the workaround on the IXP45X/IXP46X network processors. The PCI-device ID is updated to reflect the new processor.

3.2.2.6 Interrupt Controller

The number of possible IRQ interrupts has been expanded from 32 to 64 total. Additional interrupt sources, known as the error interrupts, also have been introduced.

None of the interrupt sources of the existing IXP42X processors have been modified or moved (address-wise) while designing the IXP45X/IXP46X network processors. BSP code of the existing IXP42X processors should be compatible with the IXP45X/IXP46X network processors. New registers are available for configuring the interrupt controller.

The Intel XScale processor supports two interrupt sources: FIQ and IRQ. The user can configure the 64 input interrupts to present as an FIQ or an IRQ. The user also sets the priority response of the configured interrupts from the possible 64 sources. Not all of these are currently valid.

The BSP must be modified to reflect the following new interrupt sources:

- Int32 — USB Host
- Int33 — I^2C
- Int34 — SSP
- Int35 — TimeSync
- Int 36 — EAU Done
- Int 37 — SHA Hashing Done
- Int58 — Switching coprocessor (SWCP) parity error
- Int60 — AHB Queue manager parity error

- Int61 —Single or multi-bit ECC parity error
- Int62 — Expansion Bus parity error

The BSP should ensure that all registers can be programmed via existing interfaces and that handlers can be attached to the new interrupt sources as with the previous interrupt sources numbered 0-31. Interrupt handlers for these new sources are provided in the IXP400 software v2.0 and above or, in the case of USB Host, by the OS vendor.

3.2.2.7 Expansion Bus Controller

The Expansion Bus has changed from the IXP42X processors family; hence the programming interface is different and requires BSP or device-driver changes.

This feature has a bus width of 32 bits, a larger memory address space, and supports a host mode. Customers who wish to take advantage of the advanced host features must take into account the register changes between the design of IXP42X processors, and the new, 32-bit Expansion Bus controller. This can be expected to require changes in any custom/vendor-developed driver or BSP, vendor-based code compared to the previous Expansion Bus Controller implementation on the IXP42X processors.

Developers using the Expansion Bus on the IXP45X/IXP46X network processors should also be aware that each of the eight chip selects EX_CS_N[7:0] can be configured to access a maximum memory window of 32 Mbytes, where the IXP42X processors have a maximum memory window size of 16 Mbytes per chip select. This should be accounted for while defining and allocating system memory map usage.

3.2.2.8 USB 2.0 Compatible Host Controller

In the IXP42X processors family, the controller was a USB 1.1 device only. The implementation for the IXP45X/IXP46X network processors adds a USB 2.0, full-speed (12-Mbps), low-speed (1.5-Mbps) compatible host controller. This is a USB 2.0, EHCI-compliant controller, but a USB 1.1 PHY. A Transaction Translator, between the host controller and the physical layer, makes the data stream USB 1.1-compliant.

The USB Controller conceptual blocks are shown in Figure 5 on page 18. The Transaction Translator with PHY provides support for USB 1.1 speeds (low- and full-speed).

The Transaction Translator is a component that is normally found in a hub, to isolate the high-speed signaling (USB 2.0) from the full/low-speed signalling (USB 1.1) environment, while there are a mixture of devices connected to a hub.

3.2.2.9 I^2C

The I^2C interface is a new feature for the IXP45X/IXP46X network processors, and new BSP or device drivers is needed to take advantage of this mode.

The IXP42X processors use GPIO **bit-banging** to implement the I^2C protocol. The IXP45X/IXP46X network processors provide a dedicated subsystem and register set for controlling the I^2C bus. This subsystem is compliant with the Philips* I^2C standard and can operate as both master and slave.

The components are consistent with the I^2C Controller used in the Intel® IOP321 I/O Processor; so any BSP device support already implemented for that processor should support the I^2C controller in the IXP4XX product line.

3.2.2.10 SPI / SSP

The SPI is a full-duplex, synchronous, character-oriented channel, supporting a four-wire interface (receive, transmit, clock, and slave select). The controller is compliant with three standards - SPI, SSP, and MicroWire* - and operates in master mode. The supported bit rates range between 7.2 Kbps and 1.84 Mbps, and external clock signal is supported.

No special software support is required for this purpose as standards compliance is ensured by the hardware. The development of an SPI driver for the IXP4XX product line can overlap with CODEC development. The SPI implementation is internal to the CODEC and, as such, any CODEC must be refactored to take advantage of SPI component.

3.2.2.11 Ethernet and Network Processor Engines (NPEs)

The Ethernet and NPE features have changed from the IXP42X processors' family to the new IXP4XX product line. The programming interface, via the associated IXP400 software release to support the IXP4XX product line is the primary interface method from RTOS BSPs and from vendor-specific, Ethernet-device drivers.

There is an increase in memory size used internally by the Network Processor Engines. The instruction and data memory has been doubled over the IXP42X processors, from 2K to 4K for each memory type. This helps to support more flexibility for NPE functions by allowing more microcode space to run the various features.

The Ethernet Access Component used in the IXP400 software release is different from the equivalent Ethernet Access Component in the family of IXP42X processors and requires slight BSP or device-driver changes. The NPE interfaces are multiplexed, supporting MII and SMII. This allows for a total of three MII ports and up to three ports of SMII. Setting up the interface connection method among these choices is an Ethernet port configuration scope of concern.

3.2.2.12 Queue Manager

The Queue Manager is an internal hardware feature of the IXP45X/IXP46X network processors and it is not relevant to software programmers.

The number of entries that can be handled has been doubled compared to the IXP42X processors, which enables enhanced capabilities for handling data flows internally. Parity has been added.

The IXP400 software release that supports IXP45X/IXP46X network processors has the desired code to support the new, expanded-size Queue Manager.

3.2.3 Changes in Unused and Reserved Bits — GPIO

There are some changes to GPIO functional registers that are common to the IXP42X and IXP4XX product line. These changes affect unused or reserved bits and their definitions and functions. (See Table 3.)

Refer to the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual* for detailed description of the registers and functional definitions of each bit field.

Table 3. Changes in Unused and Reserved Bits (Sheet 1 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP4XX product line Usage
GPIO Output Register	GPOUTR [DO8]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin, depends on testmode_data, GPOER[8] • 0 = Output a 0 on output pin, depends on testmode_data, GPOER[8] Reset Value:0 Access: R/W
	GPOUTR [DO7:DO0]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin GPOER[7:0] • 0 = Output a 0 on output pin GPOER[7:0] Reset value: 0 Access: R/W
GPIO Interrupt Type Register 1	GPIT1R [31] (gpio_npe_7)	Not used - Reserved	• 1 = A synchronized gpio_in[7] is muxed to gpio_int_npe[7] • 0 = gpisr[7] is muxed to gpio_int_npe[7] Reset value: 0 Access: R/W
	GPIT1R [30] (gpio_npe_6)	Not used - Reserved	• 1 = A synchronized gpio_in[6] is muxed to gpio_int_npe[6] • 0 = gpisr[6] is muxed to gpio_int_npe[6] Reset value: 0 Access: R/W
	GPIT1R [29] (gpio_npe_5)	Not used - Reserved	• 1 = A synchronized gpio_in[5] is muxed to gpio_int_npe[5. • 0 = gpisr[5] is muxed to gpio_int_npe[5] Reset value: 0 Access: R/W
	GPIT1R [28] (gpio_npe_4)	Not used - Reserved	• 1 = A synchronized gpio_in[4] is muxed to gpio_int_npe[4] • 0 = gpisr[4] is muxed to gpio_int_npe[4] Reset value: 0 Access: R/W
	GPIT1R [27] (gpio_npe_3)	Not used - Reserved	• 1 = A synchronized gpio_in[3] is muxed to gpio_int_npe[3] • 0 = gpisr[3] is muxed to gpio_int_npe[3] Reset value: 0 Access: R/W
	GPIT1R [26] (gpio_npe_2)	Not used - Reserved	• 1 = A synchronized gpio_in[2] is muxed to gpio_int_npe[2] • 0 = gpisr[2] is muxed to gpio_int_npe[2] Reset value: 0 Access: R/W
	GPIT1R [25] (gpio_npe_1)	Not used - Reserved	• 1 = A synchronized gpio_in[1] is muxed to gpio_int_npe[1] • 0 = gpisr[1] is muxed to gpio_int_npe[1] Reset value: 0 Access: R/W
	GPIT1R [24] (gpio_npe_0)	Not used - Reserved	• 1 = A a synchronized gpio_in[0] is muxed to gpio_int_npe[0] • 0 = gpisr[0] is muxed to gpio_int_npe[0] Reset value: 0 Access: R/W

Table 3. Changes in Unused and Reserved Bits (Sheet 2 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP4XX product line Usage
GPIO Interrupt Type Register 2	GPIT2R [23:21]	Not used - Reserved	• 000 - Active High • 001 - Active Low • 010 - Rising Edge • 011 - Falling Edge • 1xx - Transitional Reset value: 000 - Active High Access: R/W
	GPIT2R [20:18]	Not used - Reserved	• 000 - Active High • 001 - Active Low • 010 - Rising Edge • 011 - Falling Edge • 1xx - Transitional Reset value: 000 - Active High Access: R/W
	GPIT2R [17:15]	Not used - Reserved	• 000 - Active High • 001 - Active Low • 010 - Rising Edge • 011 - Falling Edge • 1xx - Transitional Reset value: 000 - Active High Access: R/W

4.0 Migration Considerations for the Intel® IXP42X Product Line of Network Processors to the Intel® IXP43X Product Line

4.1 Hardware Migration Considerations

Refer to the *Intel® IXP43X Product Line of Network Processors Hardware Design Guidelines* for recommendations on designing with the new hardware features included in the IXP43X product line of network processors.

4.2 Software Migration Considerations

The Intel® IXP42X Product Line of Network Processors and the Intel® IXP43X Product Line of Network Processors can use the same basic set of application software and firmware drivers. They both share a common Intel XScale® Processor architecture and application feature set.

The exception to this is where there are differences due to updated/extended features or new processor features. Software programmers must be aware of the implications of the new features and changes in the operational methods of some features (such as the DDRII/I memory controller, USB2.0 Host).

The implementation feature differences from the IXP42X processors' family requires software changes in existing code. This primarily applies to board support package (BSP) code, but can also apply to application-level programs. The following sections describes the areas where software changes should be anticipated, and planned for accordingly by the software engineering organizations of customers interested in using the IXP43X network processors. Figure 4 on page 16 shows a block diagram of the Intel® IXP43X Product Line.

The IXP43X network processors require IXP400 software v2.4 or later.

4.2.1 Processor Initialization and Boot Strap

This is a role normally handled by a boot loader. The majority of the existing bootloader code can be the same for each operating system. In any case, the processor initialization must be updated to accommodate the updated processor register set and new features. The areas in need of updates are DDRII/I SDRAM configuration for DDR and timers.

4.2.2 Processor Software Advanced Features

Real-time operating systems such as VxWorks, Linux, Microsoft Windows CE, .NET and any high-level applications running on top of those RTOS is not affected by the change from IXP42X processors to the IXP43X network processors. An RTOS typically utilizes a BSP and associated device drivers to communicate with the new hardware and architectural advanced features. These BSPs and device drivers is subject to change to support new features of the IXP43X network processors.

These changes include, but are not limited to:

- Interrupt handling
- Ethernet physical-layer devices (PHYs) through the NPEs
- DDRII/I devices through the DDRII/I-SDRAM memory controller
- SPI/SSP interface

- DMA controller
- Queue Manager

While porting code from the IXP42X processors to IXP43X network processors, software migration and porting considerations require the most attention. New features not supported in the IXP400 software access layer, via an associated access component, must be accounted for with new device drivers or BSP changes in customer code.

Detailed software code descriptions or examples of modifications and changes to BSPs are outside the scope of this Application Note, since these changes are not only RTOS dependent, but hardware-platform-dependent as well. Software programmers should go through detailed descriptions of the registers, instructions and operational modes of each new hardware feature as mentioned in the *Intel® IXP43X Product Line of Network Processors Developer's Manual*.

The following sections provide an overview of new and/or enhanced processor components that requires an update in the board support package (BSP).

4.2.2.1 DDRII 400MHz/ DDRI-266MHz Memory Controller

The IXP43X network processors use a DDRII-400MHz/ DDRI-266MHz memory controller instead of the SDRAM memory controller used by the IXP42X processors family. The memory controller can use error-correcting memory (ECC) to increase reliability by detecting double-bit errors and by detecting and correcting single-bit errors.

This memory needs new code to enable its operation and to allow the system using IXP43X network processors, to initialize the memory array. That is because the programmer-accessible configuration elements are not the same as the SDRAM-based external memory used in the IXP42X processors.

The programmer must address the DDRII/I SDRAM configuration, the specified JEDEC memory initialization sequence, timing, and refresh-rate setup.

In Linux, the primary impact is to the boot loader, as the Linux kernel expects the boot loader to set up and initialize the RAM. This development is being accommodated by Intel with updates to the RedBoot* boot loader.

Additional consideration is necessary for ECC interrupt handling and scrubbing. The interrupts can be set up by the boot loader, but this is generally in the realm of the OS initialization. The OS must accommodate setup of the interrupts for the time period between boot and when the access library functionality is activated.

Note: JTAG vendors must alter their mini-ICache-based JTAG unit driver code to accommodate the new memory initialization scheme.

4.2.2.2 MPI Port Initialization

There are two additional considerations that must be addressed while coding the memory controller configuration sequences. These have to do with steering for the Memory Port Interface port to the Intel XScale processor and setting the arbitration between the MPI port and AHB buses for equal bandwidth.

The registers and bits involved with these requirements are described in the following paragraphs and Table 2.

The MPI Enable bit (MI_EN, bit 31) is located in the Expansion Bus Configuration Register 1 (EXP_CNFG1) and controls how the Intel XScale processor accesses the external DDR memory. If set to a zero, Intel XScale processor does not take advantage

of the increased speed possible with the new dedicated MPI port to the controller. Instead, Intel XScale processor routes all core-initiated DDR transactions though the AHB bus.

For maximum performance, this bit should implicitly be set to a one before doing the remainder of the DDR section configuration in the boot-up process. There is another operation that should be performed before setting the MIP_EN bit to a one (1).

The BSP or platform initialization code should be sure to copy the code from 0 – 256 Mbyte in the flash to DDRII/I SDRAM over the same address space **before** setting the MPI_EN bit to 1.

The implications of the settings that is the default at power on/reset are the reasons behind the need for this action, and they are described as follows:

- At power on/reset:
  - MEM_MAP in the **exp bus config reg 0** is 1.
    This means the flash is at address 0x0.
  - MPI_EN in the **exp bus config reg 1** is 0.
    This means all Intel XScale processor bus transactions are over the South AHB. (The MPI port between Intel XScale processor and memory controller is disabled.)

  The Intel XScale processor fetches the power on/reset exception vector from address 0x0, which is in flash.
- The potential problem:

  While MPI_EN is set to 1, all Intel XScale processor access from 0 – 1 Gbyte goes to the MPI port and not to the AHB. This includes instructions fetches.

  While Intel XScale processor is fetching instructions from 0 – 256 Mbyte (the flash) and has not copied its code from flash to DDRII/I SDRAM at the same address first, there is no code to execute in DDRII/I SDRAM and the core fetches garbage and hangs.

  By ensuring that the code from 0 – 256 Mbyte in the flash is copied to SDRAM, thus covering the same address space *before* setting the MPI_EN bit to 1, this problem will not occur.

The MCU Port Transaction Count Register (MPTCR) register must be configured to have equal bandwidth between the MPI port and the AHB bus. This register is not programmed with this setting by default, requiring that it be implicitly set. A value of 0x11H sets the IXP43X network processors to a level that prevents unfair arbitration and indeterminate results.

Having the option to control arbitration, and thus the bandwidth utilization over these busses can be useful for performance balancing of the buses while application optimization efforts are being made; while for initial bring up of a platform based on IXP43X network processors, the 0x11H value is recommended.

Table 4. MPI Port Registers

Register	Signal Name [Bit]	Description
EXP_CNFG1 Expansion Bus configuration Register 1	MPI_EN [31]	This bit should always be set while configuring the DDR during boot-up. When this bit is set, the performance between Intel XScale processor and DDR is increased. • 0 = DDR transactions are routed through the AHB. • 1 = DDR transactions are routed through the MPI port.
MPTCR MCU Port Transaction Count Register	MPTCR [07:04]	North and South AHB Transaction Count: Number of transactions the IB MCU port can have processed in a single tenure of the DDRI SDRAM. • 1H = 1 transaction • 2H = 2 transaction • 3H = 3 transaction • ... • FH = 15 transactions • 0H = 16 transactions
MPTCR MCU Port Transaction Count Register	MPTCR [03:00]	Core Transaction Count: Number of transactions the core processor MCU port can have processed in a single tenure of the DDRI SDRAM. • 1H = 1 transaction • ... • FH = 15 transactions • 0H = 16 transactions

4.2.2.3 Timers

There are ten new registers for the timer subsystem of the IXP43X network processors. The number of timers in the system has stayed the same.

There are two general-purpose down timers named Timer0 and Timer1. Timer0 is generally used for the OS time-keeper while Timer1 is generally available for use by application programmers. Additionally, there is a countdown Watchdog timer and a count-up time stamp timer.

Notes on the additional functionality:

- The time stamp timer has a reload value of `0000_0001`.
- The timers (except the watchdog) allows for a prescaler.
- The timer allows for a three-fourths-rate operation mode which is used to simulate a 20 ns (50 MHz) clock as opposed to the APB, 66.66-MHz clock.
- The time-stamp-compare register allows interrupts on a match with the time stamp count-up register. Previously, the time stamp register could only trigger an interrupt on rollover. The value does not automatically reset to 0 on interrupt trigger.
- Configuration register allows the associated timer to be stopped while in 20-ns mode. Pausing the timer is not possible as the timer can be stopped but it can't be restarted from the place it stopped.

Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for register information.

4.2.2.4 PCI Controller

The PCI controller setup is handled by the BSP code. This BSP layer is subject to change based on silicon fixes to the PCI subsystem while moving from B1 silicon of IXP42X processors to the IXP43X network processors.

The known changes to the PCI hardware can be derived from the following errata of the IXP42X processors:

- SCR 1289 — PCI Controller returns infinite retries on PCI after AHB prefetch error
- SCR 2372 — PCI Controller DMA deadlock problem
- SCR 2370 — PCI Controller does not drive correct byte-enables on non-prefetch read
- SCR 2831 — PCI Memory Byte enables: Prefetch reads
- SCR 3364 — PCI deadlock during outbound burst writes

The software workarounds in place for the errata is required to detect the processor and disable the workaround on the IXP43X network processors. The PCI-device ID is updated to reflect the new processor.

4.2.2.5 Interrupt Controller

The number of possible IRQ interrupts has been expanded from 32 to 64 total. The interrupts are divided to normal interrupts and error interrupts. For normal interrupts, it is defined by their positional priority (For example, position 12 is of higher priority than position 42). The error class of interrupts has unconditional priority over normal class. For compatibility reasons, only interrupts [63:32] can be defined as error class.

Only some of the interrupt sources of the existing IXP42X processors have been modified or moved (address-wise) while using IXP43X network processors. Most of the existing BSP code of the IXP42X processors should be compatible with the IXP43X network processors; though there are new registers for configuring the interrupt controller.

The Intel XScale processor supports two interrupt sources: FIQ and IRQ. The user configures which of the total possible 64 interrupt sources is connected to the FIQ or IRQ signals that Intel XScale processor can see. The user also sets the priority response of the configured interrupts from the possible 64 sources. Not all of these are currently valid.

The BSP must be modified to reflect the following new interrupt sources:

- Int0 — NPE-A
- Int1 — Reserved
- Int2 — NPE-C
- Int12 — Reserved
- Int13 — Reserved
- Int32 — USB Host 2.0H Host 0
- Int33 — USB Host 2.0H Host 1
- Int34 — SSP
- Int60 — Queue manager parity error
- Int61 — Single or multi-bit ECC error

The BSP should ensure that all registers is programmed via existing interfaces and that handlers are attached to the new interrupt sources as with the previous interrupt sources numbered 0-31. Interrupt handlers for these new sources are provided in the IXP400 software v2.4 (or later), and in the case of USB Host, by the OS vendor.

4.2.2.6 Expansion Bus Controller

The Expansion Bus has changed from the IXP42X processors family; so the programming interface is different and requires BSP or device-driver changes.

This feature still has a bus width of 16 bits.

Developers using the Expansion Bus on IXP43X network processors should also be aware that there are only four chip selects EX_CS_N[3:0] and each is configured to access a maximum memory 16MB. Texas Instruments* HPI style accessed are not supported.

4.2.2.7 USB 2.0 Host Controller

In the IXP42X processors family, the controller was a USB 1.1 device only. The implementation for IXP43X network processors is a USB 2.0, high-speed (480-Mbps),full-speed (12-Mbps), low-speed (1.5-Mbps) EHCI-compliant host controller. This includes a UTMI and single-ported physical transceiver to support high-speed (480-Mbps),full-speed (12-Mbps), low-speed (1.5-Mbps).

Using the EHCI standard data structures, it allows direct connection to USB legacy (USB1.1) full-speed and low-speed devices without a companion USB 1.1 host controller or host controller driver.

The USB Host controller conceptual blocks are shown in Figure 4 on page 16. Being UTMI+ Level 2 compliant, the USB Host controller is able to connect directly or through a high speed hub to both USB2.0 high speed devices, or legacy USB 1.1 full and low speed devices. But the USB controller cannot connect to a low speed device via a full-speed USB hub as UTMI+ Level 2 does not support FS PREamble PID that is required to signal to all USB devices that the next transaction is in a LS protocol.

The following table shows the supported connectivities.

Hub	Device	Connectivity
No Hub/Direct	High speed device	OK
	Full speed device	OK
	Low speed device	OK
High Speed Hub	High speed device	OK
	Full speed device	OK
	Low speed device	OK
Full Speed Hub	High speed device	OK
	Full speed device	OK
	Low speed device	Not Allowed

4.2.2.8 SPI / SSP

The SPI is a full-duplex, synchronous, character-oriented channel, supporting a four-wire interface (receive, transmit, clock, and slave select). The controller is compliant with three standards - SPI, SSP, and MicroWire* - and operates in master mode. The supported bit rates range between 7.2 Kbps and 1.84 Mbps, and external clock signal is supported.

No special software support is required for this purpose as standards compliance is ensured by the hardware. The development of an SPI driver for the IXP43X network processors can overlap with CODEC development. The SPI implementation is internal to the CODEC and, as such, any CODEC must be refactored to take advantage of SPI component.

4.2.2.9 Ethernet and Network Processor Engines (NPEs)

The Ethernet and NPE features have changed from the IXP42X processors' family to the IXP43X network processors. The programming interface, via the associated IXP400 software release to support the IXP43X network processors, is the primary interface method from RTOS BSPs and from vendor-specific, Ethernet-device drivers.

There is an increase in memory size used internally by the Network Processor Engines. The instruction and data memory has been doubled over the IXP42X processors, from 2K to 4K for each memory type. This helps to support more flexibility for NPE functions by allowing more microcode space to run the various features.

4.2.2.10 Queue Manager

The Queue Manager is an internal hardware feature of the IXP43X network processors and it is not relevant to software programmers.

The number of entries that are handled has been doubled, compared to the IXP42X processors, which enables enhanced capabilities for handling data flows internally. Parity has been added.

The IXP400 software release that supports the IXP43X network processors has the needed code to support the new, expanded-size Queue Manager.

4.2.3 Changes in Unused and Reserved Bits — GPIO

There are some changes to the GPIO functional registers that are common to the IXP42X and IXP43X network processors. These changes affect unused or reserved bits and their definitions and functions. (See Table 3.)

Refer to the *Intel® IXP43X Product Line of Network Processors Developer's Manual* for detailed description of the registers and functional definitions of each bit field.

Table 5. Changes in Unused and Reserved Bits (Sheet 1 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP43X network processors Usage
GPIO Output Register	GPOUTR [DO8]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin, depends on testmode_data, GPOER[8] • 0 = Output a 0 on output pin, depends on testmode_data, GPOER[8] Reset Value:0 Access: R/W
	GPOUTR [DO7:DO0]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin GPOER[7:0] • 0 = Output a 0 on output pin GPOER[7:0] Reset value: 0 Access: R/W

Table 5. Changes in Unused and Reserved Bits (Sheet 2 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP43X network processors Usage
GPIO Interrupt Type Register 1	GPIT1R [31] (gpio_npe_7)	Not used - Reserved	• 1 = A synchronized gpio_in[7] is muxed to gpio_int_npe[7] • 0 = gpisr[7] is muxed to gpio_int_npe[7] Reset value: 0 Access: R/W
	GPIT1R [30] (gpio_npe_6)	Not used - Reserved	• 1 = A synchronized gpio_in[6] is muxed to gpio_int_npe[6] • 0 = gpisr[6] is muxed to gpio_int_npe[6] Reset value: 0 Access: R/W
	GPIT1R [29] (gpio_npe_5)	Not used - Reserved	• 1 = A synchronized gpio_in[5] is muxed to gpio_int_npe[5. • 0 = gpisr[5] is muxed to gpio_int_npe[5] Reset value: 0 Access: R/W
	GPIT1R [28] (gpio_npe_4)	Not used - Reserved	• 1 = A synchronized gpio_in[4] is muxed to gpio_int_npe[4] • 0 = gpisr[4] is muxed to gpio_int_npe[4] Reset value: 0 Access: R/W
	GPIT1R [27] (gpio_npe_3)	Not used - Reserved	• 1 = A synchronized gpio_in[3] is muxed to gpio_int_npe[3] • 0 = gpisr[3] is muxed to gpio_int_npe[3] Reset value: 0 Access: R/W
	GPIT1R [26] (gpio_npe_2)	Not used - Reserved	• 1 = A synchronized gpio_in[2] is muxed to gpio_int_npe[2] • 0 = gpisr[2] is muxed to gpio_int_npe[2] Reset value: 0 Access: R/W
	GPIT1R [25] (gpio_npe_1)	Not used - Reserved	• 1 = A synchronized gpio_in[1] is muxed to gpio_int_npe[1] • 0 = gpisr[1] is muxed to gpio_int_npe[1] Reset value: 0 Access: R/W
	GPIT1R [24] (gpio_npe_0)	Not used - Reserved	• 1 = A a synchronized gpio_in[0] is muxed to gpio_int_npe[0] • 0 = gpisr[0] is muxed to gpio_int_npe[0] Reset value: 0 Access: R/W

5.0 Conclusion

The Intel® IXP4XX Product Line of Network Processors are based on the Intel XScale® Technology design. Due to many similarities between the feature sets and architecture of the products, migrating to a new hardware platform using the IXP43X network processors or IXP4XX product line and porting low-level BSP firmware and device drivers leverages the advantages of the existing design and new processor design enhancements for next-generation products.

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