Intel® IXP45X and Intel® IXP46X Product Line of Network Processors: Migrating from the Intel® IXP42X Product Line

Application Note

May 2005

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Revision History

Date	Revision	Description
May 2005	2.0	Updated to add support for Intel® IXP455 Network Processor. Section 3.1: Removed duplicate text and replaced with a pointer to the *Intel® IXP46X Product Line of Network Processors Hardware Design Guidelines*. Section 3.2.2.7: Added clarification to Expansion Bus Controller information.
March 2005	1.0	Initial release of document.

1.0 Introduction

This application note facilitates the migration of designs based on the Intel® IXP42X Product Line of Network Processors to the Intel® IXP45X and Intel® IXP46X Product Line of Network Processors. Details on the hardware design and platform's implementation of the features of the IXP45X/IXP46X product line are not described in this document.

The primary subsystems that are new or different between the IXP42X processors and the IXP45X/IXP46X network processors are:

- Intel XScale® Core speeds
- Power-supply consideration
- DDRI 266 memory controller with ECC
- Expansion Bus Controller
- USB 2.0 host controller (full-speed and low-speed) and EHCI-compliant
- I^2C hardware
- Six Ethernet ports with MII/SMII interfacing
- SPI/SSP Serial Peripheral Port (supports Motorola* Serial Peripheral Interface, National Semiconductors* MicroWire*, and Texas Instruments* Synchronous Serial Protocol operations)
- IEEE 1588 hardware assistance
- Ethernet Switching Coprocessor (SWCP)
- Cryptography Engine (Random Number Generator, SHA, and Exponentiation Unit)
- Intel XScale core Memory Port Interface
- NPE Memory Increase
- Interrupt Controller (increase to 64 interrupts)
- GPIO Updates (added multiplex for Spread-Spectrum and IEEE-1588 hardware assistance)

Note: This application note discusses all features supported on the Intel® IXP465 Network Processor. A subset of these features is supported by certain processors in the IXP45X/IXP46X product line, such as the IXP460 or IXP455 network processors. For details on feature support listed by processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

The basic functions in the board support package (BSP), device driver, and application software are discussed to assist users to easily migrate the existing platforms into the new processors with the advanced features.

The following sections provide a general description of the architectural and functional differences between the IXP42X processors and IXP45X/IXP46X product line. It is not the intention of this application note to provide a the level of detail that shows how a specific feature or function is implemented or used in applications. See the technical manuals listed in Section 1.1, "Related Documentation" for feature implementation details.

1.1 Related Documentation

Title	Document Number
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet	306261
Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual	306262
Intel® IXP46X Product Line of Network Processors Hardware Design Guidelines	305261
Intel® IXP4XX Product Line of Network Processors Specification Update	306428
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Datasheet	252479
Intel® IXP42X Product Line of Network Processors and IXC1100 Control Plane Processor Developer's Manual	252480
Intel® IXP400 Software Programmer's Guide	252539

1.2 Acronyms

DDR	Double-Data-Rate SDRAM
GPIO	General-Purpose Input / Output Interface
MAC	Media Access Control
MII	Media-Independent Interface
NPE	Network Processor Engine
SDRAM	Synchronous DRAM
SMII	Serial, Media-Independent Interface
SPI	Serial Peripheral Interface
SS-SMI	Source Synchronous, Serial Media-Independent Interface
SSP	Synchronous Serial Protocol

2.0 Product Feature Comparison

This section describes the architectural feature set differences between the IXP42X processors and the IXP45X/IXP46X network processors.

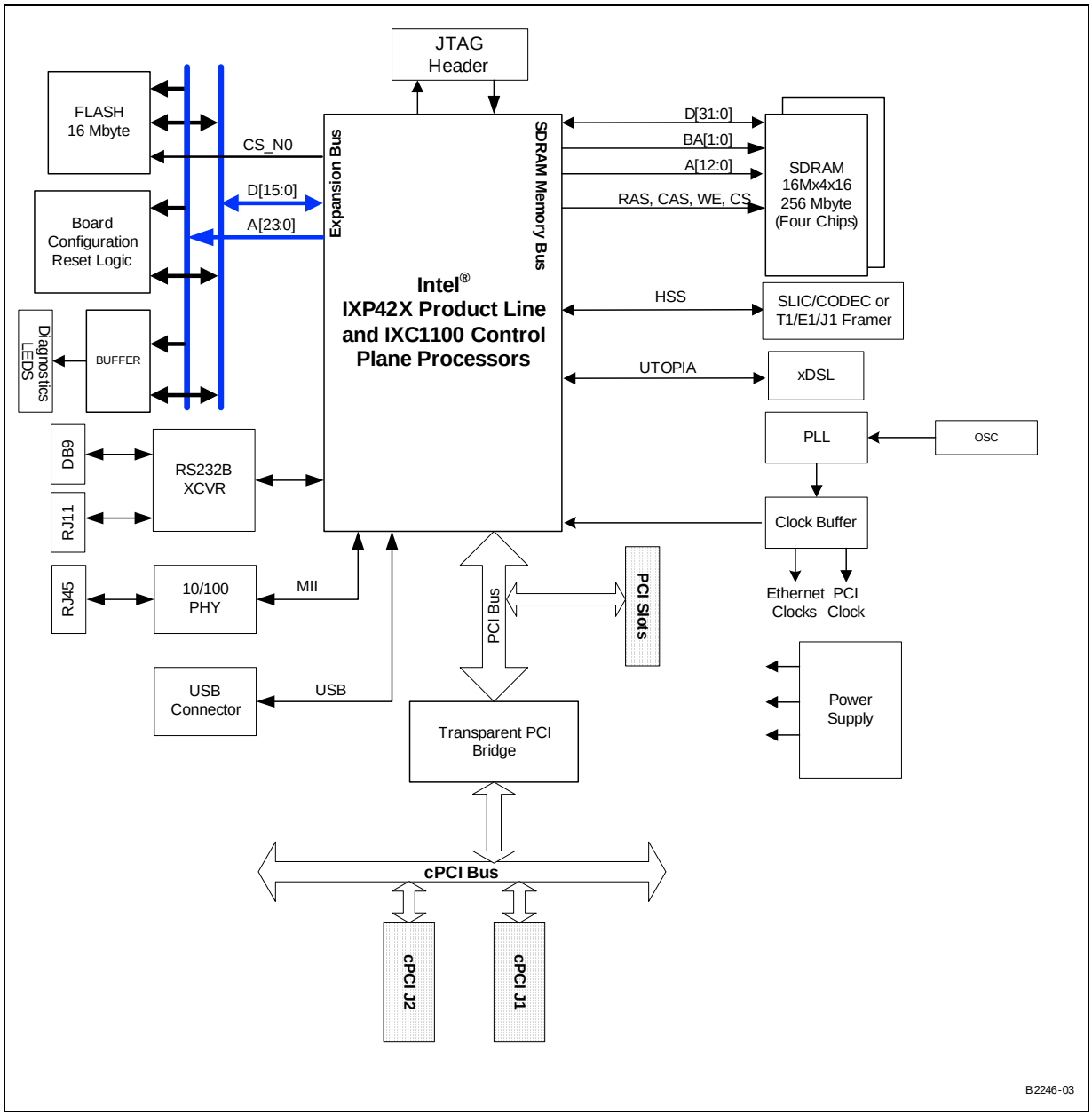
2.1 Intel® IXP42X Product Line of Network Processors

The IXP42X processors are a highly integrated System-on-a-Chip (SoC) designed to provide greater design flexibility and reduce system-development costs. These include features such as the UARTs, watch-dog timer (WDT), general-purpose timers, three Network Processor Engines (NPEs) for two Ethernet and one UTOPIA interface, PC 133 SDRAM, GPIO, PCI 2.2 and a 16-bit Expansion Bus Controller that can be interfaced and implemented in many applications such as embedded networking and communications.

Figure 1 illustrates an example of the basic system block diagram of the IXP42X processors. Features of the IXP42X processors include:

- Intel XScale core up to 533 MHz
- Three Network Processor Engines (NPEs)
- PCI 2.2 Interface
- Two MII Interfaces
- UTOPIA Level 2 Interface
- USB 1.1 Device Controller
- Two High-Speed, Serial Interfaces
- PC 133 SDRAM Interface
- Encryption/Authentication
- High-Speed UART
- Console UART
- Internal Bus Performance Monitoring Unit
- 16 GPIOs
- WDT Watchdog Timer
- General-Purpose Timers
- Packaging: 492-Pin PBGA
- Commercial/Extended Temperature

Figure 1. Intel® IXP42X Product Line of Network Processors System Block Diagram



2.2 Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Features

The Intel® IXP45X and Intel® IXP46X Product Line of Network Processors are next-generation network processors which extend the capabilities of the existing IXP42X processors. These processors introduce a variety of new advanced features, integrated on the device.

The IXP45X/IXP46X network processors are designed with Intel 0.18-µ process technology, allowing the processor to provide a high-performance Intel XScale core and greater design flexibility which reduces system-development costs and complexity.

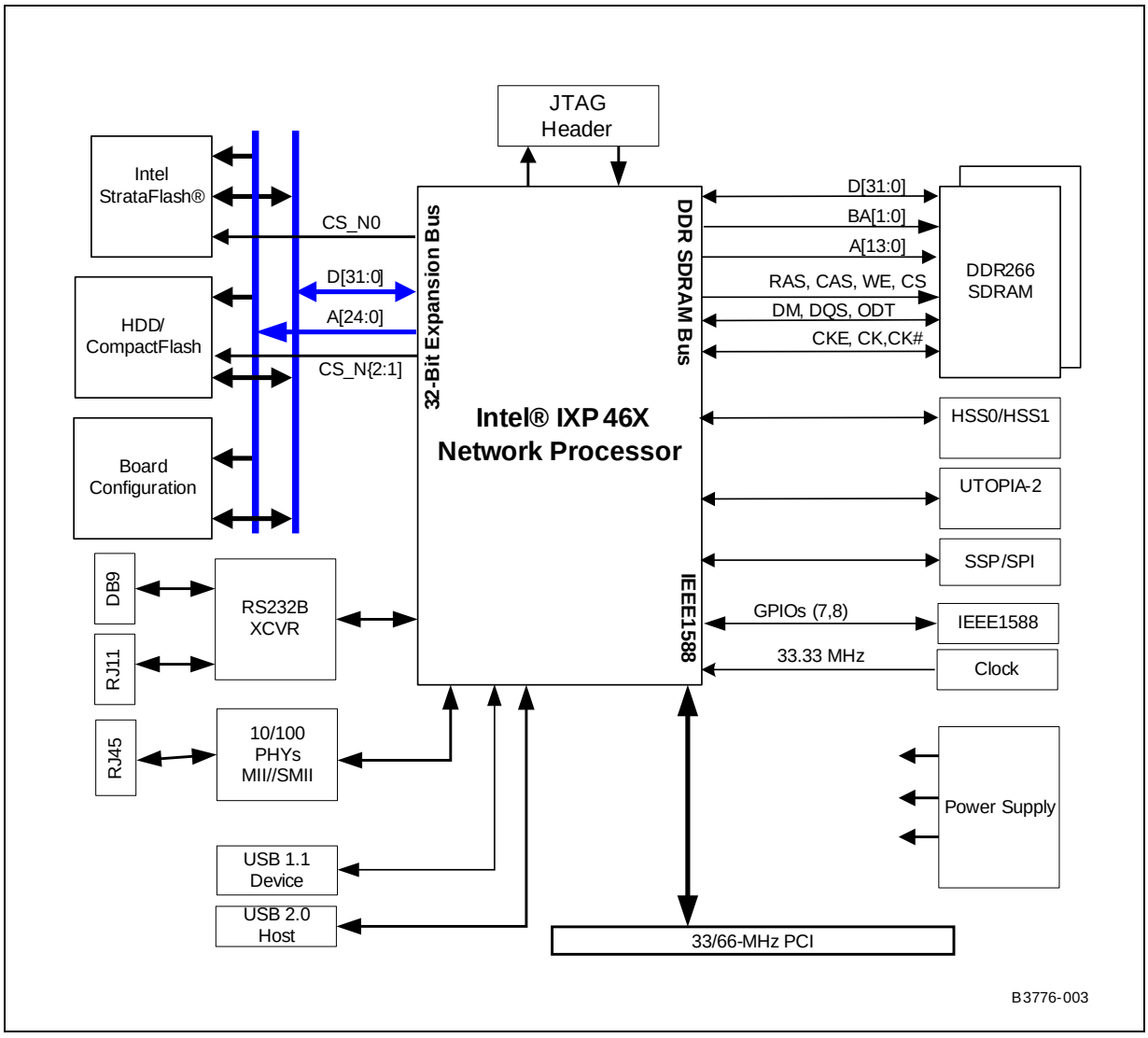
Features include functions such as the UARTs, a watch-dog timer (WDT), general-purpose timers, and three Network Processor Engines (NPEs) — for up to six Ethernet and/or one UTOPIA interface. Other new features are faster, DDRI-266 SDRAM; I^2C; SPI/SSP; GPIO; PCI-2.2, IPSec Cryptography Acceleration; bulk-encryption acceleration; HSS; and a 32-bit Host/Slave Expansion Bus controller that can be interfaced and implemented in applications such as embedded networking and communications.

Features of the IXP45X/IXP46X network processors include:

- Intel XScale® Core with speeds up to 667 MHz
- Dedicated Memory Port Interface for the Intel XScale core
- Three Network Processor Engines with expanded, internal memory
- PCI v2.2 33/66 MHz (Host/Option)
- Up to three MII Interfaces
- Up to six SMII Interfaces
- One UTOPIA Level 2 Interface
- USB 2.0 Host Controller
- USB 1.1 Device Controller
- Two High-Speed, Serial Interfaces
- DDRI SDRAM Interface with ECC
- IEEE-1588 Hardware Assist
- Master/Target Capable Expansion Bus
- Spread-Spectrum-Clock Clocking for Reduced EMI
- Cryptography Unit (Random Number Generator and Exponentiation Unit are expansions to previous NPE Crypto section implementation)
- Encryption/Authentication (AES/AES-CCM/3DES/DES/SHA-1/SHA-256/SHA-384/SHA-512/DM-5
- Two UARTs
- Internal Bus Performance Monitoring Unit
- 16 GPIOs
- Four Internal Timers
- I^2C Interface
- Synchronous Serial Protocol (SSP) Port
- Packaging: 544-pin PBGA and Lead-Free Support
- Commercial/Extended Temperature

Figure 2 illustrates the basic system block diagram of the IXP46X product line.

Figure 2. Intel® IXP46X Product Line System Block Diagram



2.3 Architecture Overview for IXP45X/IXP46X network processors

Figure 3 shows a system block diagram of the IXP46X product line, a complete system-on-a-chip designed to deliver high performance for the interchange and processing of network data.

A key functional unit is the Intel XScale core processor, the main controller or “traffic cop” of the device. After the internal interfaces are configured and initialized, the Intel XScale core gets a big assist from the Network Processing Engines (NPEs).

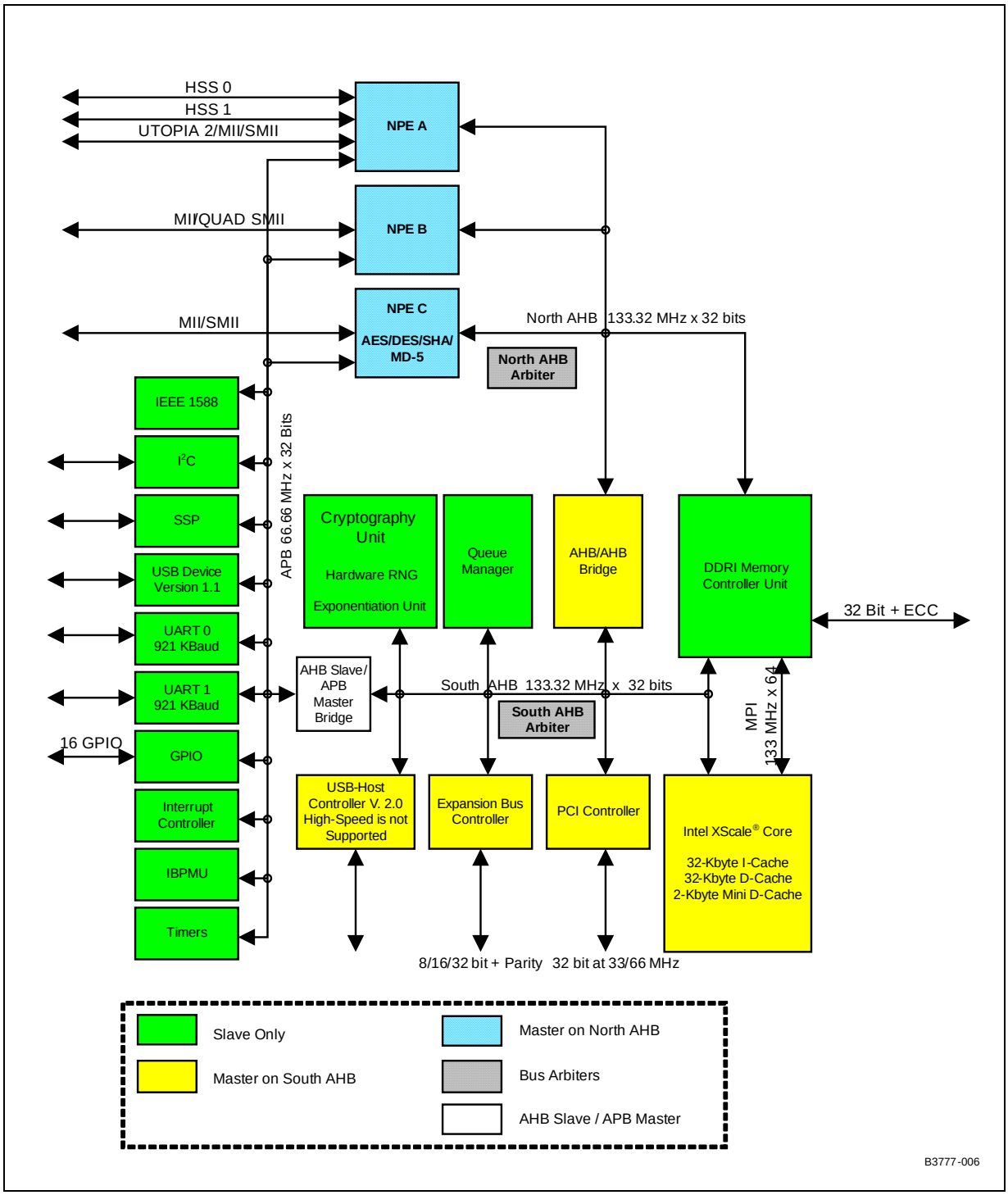
The NPE processors off-load much of the work needed to move data packets and feature additional local hardware-assist functions called coprocessors. These hardware-logic coprocessors handle the processor-intensive functions such as MII (MAC); CRC checking and generation; AAL-2 segmentation and re-assembly; and security functions such as AES, AES-CCM, DES, SHA1/256/384/512, and MD5.

The data flows from all these devices can be significant, so a segmented layout of internal buses is used to help the processing elements perform parallel processing of data. These buses are seen on the block diagram as the North AHB, the South AHB, the Memory Port Interface, and the APB.

All the external interfaces pathways connect to elements on these various buses — each particular interface or type of data flow being associated with an internal bus or processing element specifically tailored to the performance characteristics required for that interface.

Additional hardware elements are described in the remaining sections of this document. For more detailed information on all these architectural features and their special characteristics, see the documentation for the IXP45X/IXP46X network processors.

Figure 3. Intel® IXP46X Product Line Functional System Block Diagram



2.3.1 Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Advanced Features

The IXP45X/IXP46X network processors have a variety of advanced features that are not available in the IXP42X processors, including:

- **SPI/SSP —** This is an SPI master only and also will support National* MicroWire* protocol, SSP protocol from TI* and Motorola* serial peripheral interface (SPI) protocol.
- **GPIO —** The general purpose input/output peripheral provides dedicated functions as on the IXP42X processors. In addition, GPIO pins can be configured as the alternate functions. New details include:
  - AMBA APB interface
  - Two snapshot trigger inputs
  - NPE and IEEE 1588 debug functionality
  - GPIO_IN[7:0] signals can be individually routed directly through to NPEs

  For more information on how to interface these signals, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.
- **Interrupt Controller —** The number of possible IRQ interrupts has been expanded from 32 to 64. Additional interrupt sources known as the error interrupts have also been introduced. The interrupts can be configured as FIQ or IRQ interrupts.
- **I^2C —** This is an I^2C master and Slave controller integrated on chip.
- **Expansion Bus —** This is an advanced master/target Expansion Bus controller. It provides a 25-bit address bus and a 32-bit-wide data interface and also supports even/odd parity generation and checking in all external modes and in some legacy modes (Intel- and Motorola-style bus cycles). ZBT* SRAM flow-through burst support as well as the enhancement of configuration strapping to include more strapping options is an additional new feature.

  The maximum clock rate that the expansion interface can accept is 80 MHz and at 40-pF load.
- **DDRI SDRAM —** This is the DDRI-266 SDRAM Controller with an optional 8-bit support. The DDRI interface in conjunction with the dedicated MPI port provides higher bulk memory performance. The optional ECC support provides more system reliability.
- **Dedicated Memory Port Interface** for the Intel XScale® Core — The Intel XScale core now has a dedicated path to the memory controller, this will make for more effective performance in Intel XScale core memory accesses.
- **Soft Fuses** — This feature can save the use of external pull-up and pull-down resistors, if the fused interfaces are not used.
- **USB 2.0 Host —** The USB Host controller employed on the IXP45X/IXP46X network processors is an EHCI-compliant controller.
- **MII/SMII/SS-SMII —** The IXP45X/IXP46X product line provides up to three MII ports or up to six SMII ports.
- Intel XScale® Core **—** Supports operating frequencies up to 667 MHz.
- **IEEE-1588 Controller —** This is an IEEE standard and used as a clock-synchronization protocol for network measurement and control system applications.
- **Package Size** — This is still 35 mm by 35 mm in size, but an inner row of PBGA pins have been added to make it a 544-pin PBGA. IXP42X processors' PWB designs, which use a 35-mm by 35-mm package, can be reused by refreshing the PWB with the appropriate footprint for the IXP45X/IXP46X product line.

- **Cryptography Unit** — Random Number Generator and Exponentiation Unit are expansions to previous NPE-crypto hardware. Security methods supported include Encryption/ Authentication of AES/AES-CCM/3DES/DES/SHA-1/SHA-256/SHA-384/SHA-512/MD-5.

Table 1 summarizes the key feature differences between the IXP45X/IXP46X product line and IXP42X processors.

Note: Table 1 lists all features supported on the Intel® IXP465 Network Processor. A subset of these features is supported by certain processors in the IXP45X/IXP46X product line, such as the IXP460 or IXP455 network processors. For details on feature support listed by processor, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Datasheet*.

Table 1. Key Differences Between Processor Families (Sheet 1 of 2)

Feature	Intel® IXP42X Product Line of Network Processors	Intel® IXP45X and Intel® IXP46X Product Line of Network Processors
Processor Speed (MHz)	266 / 400 / 533	266 / 400 / 533 / 667
Cryptography Unit †	N/A	X
Interrupt Controller	Support to 32	Support to 64
UTOPIA Level 2 Interface†	X	X
UTOPIA Level 2 /MII/SMII †	N/A	X
GPIO Pins	16	16
Alternate Functions GPIO Pins	N/A	Support IEEE 1588 (Use GPIO 7 and GPIO 8 as Alternative Functions) and Spread-Spectrum-Clock Support
UART 0/1	X	X
HSS 0†	X	X
HSS 1†	X	X
MII 0†	X	X
MII 1†	X	X
MII/SMII (4 port SMII) †	N/A	Supported on Intel® IXP465 only
MII/SMII/SS-SMII†	N/A	X
USB 1.1 Device Controller	X	X
USB 2.0 Host Controller	N/A	X
IEEE-1588 Hardware Assistance	N/A	Supported on IXP46X product line only
I^2C	X (Software Emulation)	X
PCI	X	X
Expansion Bus	16-bit, 66-MHz	32-bit, 80-MHz, Host Support
SDRAM Controller	32-bit, 133-MHz	N/A
DDRI 266 Controller	N/A	X
AES / DES / DES3†	X	X
AES-CCM †	N/A	X
Multi-Channel HDLC †	8	8
† These features require software in order to be operational.		

Table 1. Key Differences Between Processor Families (Sheet 2 of 2)

Feature	Intel® IXP42X Product Line of Network Processors	Intel® IXP45X and Intel® IXP46X Product Line of Network Processors
SHA / MD-5†	X	X
SPI/SSPI	N/A	X
Commercial Temperature	X	X
Extended Temperature	X	X
† These features require software in order to be operational.		

3.0 Migration Considerations

3.1 Hardware Migration Considerations

For recommendations on designing with the new hardware features included in the IXP45X/ IXP46X network processors, refer to the *Intel® IXP46X Product Line of Network Processors Hardware Design Guidelines*.

3.2 Software Migration Considerations

The IXP42X processors and the IXP45X/IXP46X network processors can use the same basic set of application software and firmware drivers. They both share a common Intel XScale core architecture and application feature set.

The exception to this is where there are differences due to updated/extended features or new processor features. Software programmers must be aware of the implications of the new features as well as changes in the operational methods of some features (such as the DDR memory controller).

The implementation feature differences from the IXP42X processors' family will require software changes in existing code. This primarily applies to board support package (BSP) code, but can also apply to application-level programs. The following sections briefly describe the areas where software changes should be anticipated, and planned for accordingly by the software engineering organizations of customers interested in using the IXP45X/IXP46X network processors. Figure 3 on page 12 shows a block diagram of the IXP46X product line.

3.2.1 Processor Initialization and Boot Strap

This is a role normally handled by a boot loader. The majority of the existing boot-loader code can be the same for each operating system. In any case, the processor initialization will need to be updated to accommodate the updated processor register set and new features. The areas in need of updates are SDRAM configuration for DDR and timers.

3.2.2 Processor Software Advanced Features

Real-time operating systems such as VxWorks*, Linux*, Microsoft* Windows* CE .NET, and any high-level applications running on top of those RTOS should not be affected by the change from the IXP42X processors to the IXP45X/IXP46X network processors. An RTOS typically utilizes a

BSP and associated device drivers in order to communicate with the new hardware and architectural advanced features. These BSPs and device drivers will be subject to change to support new features of the IXP45X/IXP46X network processors.

These changes include, but are not limited to:

- Interrupt handling
- Ethernet physical-layer devices (PHYs) through the NPEs
- DDR devices through the DDR-SDRAM memory controller
- SPI/SSP interface
- Internal I^2C controller
- DMA controller
- Queue Manager

In porting code from the IXP42X processors to the IXP45X/IXP46X network processors, software migration and porting considerations will require the most attention. New features not supported in the IXP400 software access layer — via an associated access component — will need to be accounted for with new device drivers or BSP changes in customer code.

Detailed software code descriptions or examples of modifications and changes to BSPs are outside this application note's scope, since these changes are not only RTOS dependent, but hardware-platform-dependent as well. Software programmers should consult the detailed descriptions of the registers, instructions and operational modes of each new hardware feature by consulting the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

The following sections provide an overview of new and/or enhanced processor components that will require an update in the board support package (BSP).

3.2.2.1 DDR-266 Memory Controller

The IXP45X/IXP46X network processors use a DDR-266 memory controller instead of the DDR-I memory controller used by the IXP42X processors family. The memory controller now can use error-correcting memory (ECC) to increase reliability by detecting double-bit errors and by detecting and correcting single-bit errors.

This memory will need new code to enable its operation and to allow the system, using IXP45X/IXP46X network processors, to initialize the memory array. That is because the programmer-accessible configuration elements are not the same as the SDRAM-based external memory used in the IXP42X processors.

The programmer must address the DDR SDRAM configuration, the specified JDEC memory initialization sequence, timing, and refresh-rate setup.

In Linux, the primary impact will be to the boot loader, as the Linux kernel expects the boot loader to set up and initialize the RAM. This development is being accommodated by Intel with updates to the RedBoot* boot loader.

Additional consideration is necessary for ECC interrupt handling and scrubbing. The interrupts can be set up by the boot loader, but this is generally in the realm of the OS initialization. The OS must accommodate setup of the interrupts for the time period between boot and when the access library functionality is activated.

Note: JTAG vendors will need to alter their mini-ICache-based JTAG unit driver code to accommodate the new memory initialization scheme.

3.2.2.2 MPI Port Initialization

There are two additional considerations that need to be addressed when coding the memory controller configuration sequences. These have to do with steering for the Memory Port Interface port to Intel XScale core and setting the arbitration between the MPI port and AHB buses for equal bandwidth.

The registers and bits involved with these requirements are described in the following paragraphs and Table 2.

The MPI Enable bit (MI_EN, bit 31) is located in the Expansion Bus Configuration Register 1 (EXP_CNFG1) and controls how the Intel XScale core accesses the external DDR memory. If set to a zero, the Intel XScale core will *not* take advantage of the increased speed possible with the new dedicated MPI port to the controller. Instead, the Intel XScale core will route all core-initiated DDR transactions though the AHB bus.

For maximum performance, this bit should implicitly be set to a one before doing the remainder of the DDR section configuration in the boot-up process. There is another operation that should be performed before setting the MIP_EN bit to a one (1).

The BSP or platform initialization code should be sure to copy the code from 0 – 256 Mbyte in the flash to SDRAM over the same address space *before* setting the MPI_EN bit to 1.

The implications of the settings that will be the default at power on / reset are the reasons behind the need for this action, and they are described below:

- At power on/reset:
  - MEM_MAP in the “exp bus config reg 0” is 1.
    This means the flash is at address `0x0` as well as `0x5000,0000`.
  - MPI_EN in the “exp bus config reg 1” is 0.
    This means all Intel XScale core bus transactions are over the South AHB. (The MPI port between the Intel XScale core and memory controller is disabled.)

  The Intel XScale core will fetch the power on/reset exception vector from address 0x0 (which is in flash).
- The potential problem:

  If MPI_EN is set to 1, all Intel XScale core access from 0 – 1 Gbyte will go to the MPI port and not to the AHB. This includes instructions fetches.

  Therefore, if the Intel XScale core is fetching instructions from 0 – 256 Mbyte (the flash) — and has not copied its code from flash to SDRAM at the same address first — there will be no code to execute in SDRAM and the core will fetch garbage and hang.

  By making sure that the code from 0 – 256 Mbyte in the flash is copied to SDRAM — thus covering the same address space *before* setting the MPI_EN bit to 1 — this problem will not occur.

The MCU Port Transaction Count Register (MPCTR) register needs to be configured to have equal bandwidth between the MPI port and the AHB bus. This register is not programmed with this setting by default, requiring that it be implicitly set. A value of `0x11H` will set the IXP45X/ IXP46X network processors to a level that will prevent unfair arbitration and indeterminate results.

Having the option to control arbitration, and thus the bandwidth utilization over these busses, can be useful for performance balancing of the buses when application optimization efforts are being made. However, for initial bring up of a platform based on the IXP45X/IXP46X network processors, the `0x11H` value is recommended.

Table 2. MPI Port Registers

Register	Signal Name [Bit]	Description
EXP_CNFG1 Expansion Bus configuration Register 1	MPI_EN [31]	This bit should always be set when configuring the DDR during boot-up. When this bit is set, the performance is increased between the Intel XScale® Core and DDR. • 0 = DDR transactions are routed through the AHB. • 1 = DDR transactions are routed through the MPI port.
MPTCR MCU Port Transaction Count Register	MPTCR [07:04]	North and South AHB Transaction Count: Number of transactions the IB MCU port can have processed in a single tenure of the DDR SDRAM. • 1H = 1 transaction • 2H = 2 transaction • 3H = 3 transaction • ... • FH = 15 transactions • 0H = 16 transactions
MPTCR MCU Port Transaction Count Register	MPTCR [03:00]	Core Transaction Count: Number of transactions the core processor MCU port can have processed in a single tenure of the DDR SDRAM. • 1H = 1 transaction • ... • FH = 15 transactions • 0H = 16 transactions

3.2.2.3 Timers

There are 10 new registers for the timer subsystem of the IXP45X/IXP46X network processors. The number of timers in the system has stayed the same.

There are two general-purpose down timers named Timer0 and Timer1. Timer0 is generally used for the OS time-keeper while Timer1 is generally available for use by application programmers. Additionally, there is a countdown Watchdog timer and a count-up Time-stamp timer.

A few notes on the additional functionality:

- The timestamp timer now has a reload value of `0000_0001`.
- The timers (except the watchdog) will allow for a prescaler.
- The timer will allow for a three-fourths-rate operation mode which is used to simulate a 20 ns (50 MHz) clock as opposed to the APB, 66.66-MHz clock.
- The time-stamp-compare register allows interrupts on a match with the time stamp count-up register. Previously, the time stamp register could only trigger an interrupt on rollover. The value does not automatically reset to 0 on interrupt trigger.

- Configuration register will allow the associated timer to be stopped when in 20-ns mode. The timer can be stopped but it can't be restarted from the place it stopped, pausing therefore is not possible.

For register details, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

3.2.2.4 IEEE 1588 Time Synchronization

The IEEE-1588 interface is a new feature for the IXP45X/IXP46X network processors, and requires new code to enable it in any BSP or associated device driver. It is not necessary to have direct support for this in the BSP as configuration and control is handled by an IXP400 software Access Library component.

The access component enables the client application or other modules which implement the IEEE-1588 Precision Clock Synchronization Protocol (PTP) for Network Measurement and Control Systems, to configure the IEEE-1588 Time Synchronization Hardware Assist Block. The hardware assist will then be able to capture the time stamps at each of the MII interfaces on NPE-A/B/C, for both incoming or outgoing PTP protocol messages, which are multicast over UDP/IP packets in IPv4 format.

This component only enables the hardware assist block and *does not implement* the IEEE 1588 protocol.

3.2.2.5 PCI Controller

The PCI controller setup is handled by the BSP code. This BSP layer is required to change, based on silicon fixes to the PCI subsystem in moving from the IXP42X processors' B0 silicon to the IXP45X/IXP46X network processors.

The known modifications to the PCI hardware can be derived from the following errata:

- SCR 1289 — PCI Controller returns infinite retries on PCI after AHB prefetch error
- SCR 2372 — IXP42X processors' PCI controller DMA deadlock problem
- SCR 2370 — PCI controller doesn't drive correct byte-enables on non-prefetch read
- SCR 2831 — IXP46X network processors: PCI Memory Byte enables: Prefetch Reads
- SCR 3364 — PCI deadlock during outbound burst writes

The software workarounds in place for the errata will be required to detect the processor and disable the workaround on the IXP45X/IXP46X network processors. The PCI-device ID is updated to reflect the new processor.

3.2.2.6 Interrupt Controller

The number of possible IRQ interrupts has been expanded from 32 to 64 total. Additional interrupt sources, known as the error interrupts, also have been introduced.

None of the interrupt sources of the existing IXP42X processors have been modified or moved (address-wise) in going to the IXP45X/IXP46X network processors. Therefore, existing IXP42X processors' BSP code should be compatible with the IXP45X/IXP46X network processors. There are, however, new registers for configuring the interrupt controller.

The Intel XScale core supports two interrupt sources: FIQ and IRQ. The user configures which of the total possible 64 interrupt sources will be connected to the FIQ or IRQ signals that the Intel XScale core can see. The user also sets the priority response of the configured interrupts from the possible 64 sources. Not all of these are currently valid.

The BSP must be modified to reflect the following new interrupt sources:

- Int32 — USB Host
- Int33 — I^2C
- Int34 — SPI
- Int58 — Switching coprocessor parity error
- Int59 — DDR multi-bit ECC error
- Int60 — Queue manager parity error
- Int61 — NPE-A parity error
- Int62 — NPE-B parity error
- Int63 — NPE-C parity error

The BSP should ensure that all registers can be programmed via existing interfaces and that handlers can be attached to the new interrupt sources as with the previous interrupt sources numbered 0-31. Interrupt handlers for these new sources will be provided in IXP400 software v2.0 or, in the case of USB Host, by the OS vendor.

3.2.2.7 Expansion Bus Controller

The Expansion Bus has changed from the IXP42X processors family so the programming interface is different and requires BSP or device-driver changes.

This feature now has a bus width of 32 bits, a larger memory address space, and supports a Host mode. Customers who wish to take advantage of the advanced host features must take into account the register changes between the IXP42X processors' design and the new, 32-bit Expansion Bus controller. This can be expected to require changes in any custom/vendor-developed driver or BSP, vendor-based code compared to the previous Expansion Bus Controller implementation on the IXP42X processors.

Developers using the Expansion Bus on the IXP45X/IXP46X network processors should also be aware that each of the eight chip selects EX_CS_N[7:0] can be configured to access a maximum memory window of 32-Mbytes, where the IXP42X processors have a maximum memory window size of 16 Mbytes per chip select. This should be accounted for when defining and allocating system memory map usage.

3.2.2.8 USB 2.0 Full-Speed (12-Mbps), Low-Speed (1.5-Mbps) Compatible Host Controller

In the IXP42X processors' family, the controller was a USB 1.1 device only. The implementation for the IXP45X/IXP46X network processors is a USB 2.0, full-speed (12-Mbps), low-speed (1.5-Mbps) compatible host controller. This is a USB 2.0, EHCI-compliant controller, but a USB 1.1 PHY. A Transaction Translator — between the Host controller and the physical layer — makes the data stream USB 1.1-compliant.

The USB Controller conceptual blocks are shown in Figure 3 on page 12. The Transaction Translator with PHY provides support for USB 1.1 speeds (low- and full-speed).

The transaction translator is a component that is normally found in a hub — to isolate the high-speed signaling (USB 2.0) from the full/low-speed signalling (USB 1.1) environment — when there are a mixture of devices connected to a hub.

3.2.2.9 I²C

The I²C interface is a new feature for the IXP45X/IXP46X network processors, therefore new BSP or device drivers will be needed to take advantage of this mode.

The IXP42X processors used GPIO "bit-banging" to implement the I²C protocol. The IXP45X/IXP46X network processors provide a dedicated subsystem and register set for controlling the I²C bus. This subsystem is compliant with the Philips* I²C standard and can operate as both master and slave.

The components are consistent with the I²C Controller used in the Intel® IOP321 I/O Processor, so any BSP device support already implemented for that processor should support the I²C controller in the IXP45X/IXP46X product line.

3.2.2.10 SPI / SSP

The SPI is a full-duplex, synchronous, character-oriented channel, supporting a four-wire interface (receive, transmit, clock, and slave select). The controller is compliant with three standards — SPI, SSP, and MicroWire* — and operates in master mode. The supported bit rates range between 7.2 Kbps and 1.84 Mbps, and external clock signal is supported.

Standards compliance is ensured by the hardware, therefore no special software support is required for this purpose. The development of an SPI driver for the IXP45X/IXP46X product line can overlap with CODEC development. The SPI implementation is internal to the CODEC and, as such, any CODEC will need to be refactored to take advantage of SPI component.

3.2.2.11 Ethernet and Network Processor Engines (NPEs)

The Ethernet and NPE features have changed from the IXP42X processors family to the new IXP45X/IXP46X product line. The programming interface — via the associated IXP400 software release to support the IXP45X/IXP46X product line — will be the primary interface method from RTOS BSPs and from vendor-specific, Ethernet-device drivers.

Performance should be improved, due to an increase in memory size used internally by the Network Processor Engines. The instruction and data memory has been doubled over the IXP42X processors, from 2K to 4K for each memory type. This will help to support more flexibility for NPE functions by allowing more microcode space to run the various features.

The Ethernet Access Component used in the IXP400 software release will be different from the IXP42X processors family's equivalent Ethernet Access Component and will require slight BSP or device-driver changes. The NPE interfaces are now multiplexed, supporting MII and SMII. This allows for a total of three MII ports and up to six ports of SMII. Setting up the interface connection method among these choices will be an Ethernet port configuration scope of concern.

3.2.2.12 Queue Manager

The Queue Manager is an internal hardware feature of the IXP45X/IXP46X network processors. Generally, the software programmer will not need to worry about this feature.

The number of entries that can be handled has been doubled, compared to the IXP42X processors, which enables enhanced capabilities for handling data flows internally. Parity has been added.

The IXP400 software release that supports the IXP45X/IXP46X network processors will have the needed code to support the new, expanded-size Queue Manager.

3.2.3 Changes in Unused and Reserved Bits — GPIO

There are some changes to GPIO functional registers that are common to the IXP42X and the IXP45X/IXP46X product line. These changes affect unused or reserved bits and their definitions and functions. (See Table 3.)

For detailed descriptions of the registers and functional definitions of each bit field, see the *Intel® IXP45X and Intel® IXP46X Product Line of Network Processors Developer's Manual*.

Table 3. Changes in Unused and Reserved Bits (Sheet 1 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP45X/IXP46X product line Usage
GPIO Output Register	GPOUTR [DO8]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin, depends on testmode_data, GPOER[8] • 0 = Output a 0 on output pin, depends on testmode_data, GPOER[8] Reset Value:0 Access: R/W
	GPOUTR [DO7:DO0]	• 1 = Output a 1 on output pin GPOER[8:0] • 0 = Output a 0 on output pin GPOER[8:0] Reset value: 0	• 1 = Output a 1 on output pin GPOER[7:0] • 0 = Output a 0 on output pin GPOER[7:0] Reset value: 0 Access: R/W

Table 3. Changes in Unused and Reserved Bits (Sheet 2 of 2)

Register	Signal Name [bit]	IXP42X Usage	IXP45X/IXP46X product line Usage
GPIO Interrupt Type Register 1	GPIT1R [31] (gpio_npe_7)	Not used - Reserved	• 1 = A synchronized gpio_in[7] is muxed to gpio_int_npe[7] • 0 = gpisr[7] is muxed to gpio_int_npe[7] Reset value: 0 Access: R/W
	GPIT1R [30] (gpio_npe_6)	Not used - Reserved	• 1 = A synchronized gpio_in[6] is muxed to gpio_int_npe[6] • 0 = gpisr[6] is muxed to gpio_int_npe[6] Reset value: 0 Access: R/W
	GPIT1R [29] (gpio_npe_5)	Not used - Reserved	• 1 = A synchronized gpio_in[5] is muxed to gpio_int_npe[5. • 0 = gpisr[5] is muxed to gpio_int_npe[5] Reset value: 0 Access: R/W
	GPIT1R [28] (gpio_npe_4)	Not used - Reserved	• 1 = A synchronized gpio_in[4] is muxed to gpio_int_npe[4] • 0 = gpisr[4] is muxed to gpio_int_npe[4] Reset value: 0 Access: R/W
	GPIT1R [27] (gpio_npe_3)	Not used - Reserved	• 1 = A synchronized gpio_in[3] is muxed to gpio_int_npe[3] • 0 = gpisr[3] is muxed to gpio_int_npe[3] Reset value: 0 Access: R/W
	GPIT1R [26] (gpio_npe_2)	Not used - Reserved	• 1 = A synchronized gpio_in[2] is muxed to gpio_int_npe[2] • 0 = gpisr[2] is muxed to gpio_int_npe[2] Reset value: 0 Access: R/W
	GPIT1R [25] (gpio_npe_1)	Not used - Reserved	• 1 = A synchronized gpio_in[1] is muxed to gpio_int_npe[1] • 0 = gpisr[1] is muxed to gpio_int_npe[1] Reset value: 0 Access: R/W
	GPIT1R [24] (gpio_npe_0)	Not used - Reserved	• 1 = A a synchronized gpio_in[0] is muxed to gpio_int_npe[0] • 0 = gpisr[0] is muxed to gpio_int_npe[0] Reset value: 0 Access: R/W

4.0 Conclusion

Both the IXP45X/IXP46X network processors and the IXP42X processors are based on the Intel XScale core design. These network processors have many similarities between the feature sets and architecture of the two products.

Migrating to a new hardware platform — using the new IXP45X/IXP46X product line and porting low-level BSP firmware and device drivers — will leverage the advantages of the new processor design and performance enhancements for new-generation products.