FinFET and III-V/Ge technology impact on 3T1D cell behavior

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Terascale Reliable Adaptive Memory System project

System architecture

3T1D-DRAM CNFET

6T/8T-SRAM

Device modeling
Motivation

- Higher **density**.
- Lower **cost** per chip.
- Performance **improvement**.
- **Higher** frequency.

Moores Law

- **Worsening reliability**.
- **Leakage** current.
- **Device variability**.
- **Soft Errors** Rate.

Intel courtesy

Imec courtesy

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- Simulation framework
- Results
  - 3T1D-DRAM cell performance
  - Variability
  - SER impact
- Conclusions
Reliability drawbacks (I)

Introduction

Simulation

Results

Conclusions

Gate leakage currents

Mobility reduction

High-k gate dielectrics
Reliability drawbacks (II)

Device variability

Soft Error Rate

A. Asenov et al., DATE, 2011

P. Shivakumar et al., IEEE ICSN, 2002

R. Baumann et al., IEEE D&T, 2005

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Bulk MOSFETs are the conventional transistor structure, but to **improve** their performance:

1. **Adv. MOSFET**
   - Leakage reduction:  
     - **High-k** dielectrics.
   - Mobility:  
     - **Strained** channels.
   - Variability:  
     - **Difficult** to reduce doping, due to SCE.

2. **III-V/Ge MOSFETs**
   - **Significant** mobility improvement.
   - **Non** relevant fabrication process modification.

3. **FinFETs**
   - **Lower** doping.
   - **Better** SCE.
   - **Lower** leakage.
   - **Higher** mobility

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Memory cells

- Microprocessor area is **mainly** occupied by memory circuits.
- **RDF** is of particular concern in memories.
  - Designed using **minimum** feature sizes for density reasons.
- **6T-SRAM** is usually the main memory cell implemented.
Memory cells

**6T-SRAM**

- **Not** enough robust cell against the process variations.
- Relevant performance **lost** is stated, i.e. speed reduction & cell instability.

**3T1D-DRAM**

- **Dynamic** cell, refresh needed.
- **Non-destructive** read process.
- Low **area** cost.
- Higher variability **tolerance**.
- Promising for **data caches**.

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W.Luk et al., VLSI, 2006
Device models

- **16nm** technology node.
- Planar MOSFETs
  - HP PTM (ASU).
  - High-k + strained channel
- III-V/Ge MOSFETs
  - EU TRAMS project (UoG).
- FinFETs
  - HP PTM-MG (ASU).

![Graph](image)

- Sub-threshold Slope
  - FinFET stepper
  - GeMOS slower

- $I_{on}$: FinFET higher, GeMOS smaller
- $I_{off}$ (i.e., $I_{leakage}$)
  - MOSFET lower, GeMOS higher
Simulations (I)

- 3T1D-DRAM cell performance:
  - Parameters: WAT, RAT, PW & RT.
  - $V_{DD}$ relevance, 0.4 – 1V.
  - Temperature influence, 25 – 125ºC.

- Variability impact ($\Delta V_T$):
  - 10,000 Monte Carlo simulations.

<table>
<thead>
<tr>
<th>Variability Levels</th>
<th>Planar</th>
<th>FinFET</th>
<th>III-V/Ge</th>
</tr>
</thead>
<tbody>
<tr>
<td>Moderate (M)</td>
<td>10%</td>
<td>7%</td>
<td>10%</td>
</tr>
<tr>
<td>High (H)</td>
<td>20%</td>
<td>15%</td>
<td>20%</td>
</tr>
<tr>
<td>Very High (VH)</td>
<td>40%</td>
<td>30%</td>
<td>40%</td>
</tr>
</tbody>
</table>
Simulations (II)

- **Soft Error Rate (SER)**
  - Only at drain terminal.
  - Minimum injected charge (IC_{min}).
- I_{\text{pulse}} shape **differs** for each technology trend.
  - Simulated by a **double exponential** function.

L. Huichu et al., IEDM, 2012

F. Yi-Pin et al., IEEE TDMR, 2011
**FinFET-based cells show the best performance:**

- Largest RT and lowest access times.
Higher temperature **robustness** for planar cells.
- FinFET-based cells show worst behavior than planar ones, due to **self-heating** effect.
Variability impact on 3T1D

- FinFETs memories are more robust against device fluctuation.
- For memory blocks, FinFET-based 3T1D cells outperform the other two technology trends.
SER relevance on 3T1D cells

- Ion strikes @D1 & T3 aren’t regarded.
- **Highest** SER impact on T1 drain.
- **Lineal** $V_S$-shift in function of IC.
- FinFET cells are more SER robust.

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Conclusions

- **FinFET**-based 3T1D-DRAM cells outperform the other technology trends:
  - The **highest** RT, due to the lower \( I_{\text{leakage}} \).
  - Lower access times, **fastest** performance.
  - Larger **robustness** against variability (3X) and SER (10X) is also depicted.
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Thank you for your attention!

Time for questions!