Brunch with Sr. Managers at Intel Malaysia

Booth Chat -Validation Engineer
All times shown in PST

100 Most Recent Messages | **All Messages**

[01/04/13 5:56 PM]	Shari-Intel:	Welcome to the Validation Engineering Chat. Please let us know what is on your mind?
[01/04/13 5:59 PM]	vijay:	Hi
[01/04/13 5:59 PM]	SL-Intel:	Hello, and welcome to our Virtual Event!
[01/04/13 6:00 PM]	SL-Intel:	Feel free to ask if you have any questions :)
[01/04/13 6:00 PM]	vijay:	Does the functional verifications comes under the Validation Engineer?
[01/04/13 6:00 PM]	SL-Intel:	Yes Vijay
[01/04/13 6:01 PM]	vijay:	Thanks I am in the right forum
[01/04/13 6:01 PM]	Ujjwal:	Hi, Good morning everyone!
[01/04/13 6:01 PM]	SL-Intel:	Morning ...
[01/04/13 6:02 PM]	Kar:	morning, just checking out your virtual booth.
[01/04/13 6:02 PM]	SL-Intel:	Welcome .. Welcome Happy New Year to everyone
[01/04/13 6:03 PM]	Ujjwal:	SL, How much formal verification techniques are leveraged in your group?
[01/04/13 6:03 PM]	shiva:	hi everyone
[01/04/13 6:03 PM]	SL-Intel:	Hi Shiva
[01/04/13 6:04 PM]	shiva:	this is my first virtual conference and trying to understand how does it work
[01/04/13 6:05 PM]	SL-Intel:	Welcome to validation Booth . I'm SL ... Senior Manager for Atom SOC Post Silicon Validation
[01/04/13 6:05 PM]	SL-Intel:	You can ask any question regarding the job
[01/04/13 6:06 PM]	SL-Intel:	We validate and verify the logic of new architectural features of next generation ATOM SOC designs. This encompasses knowing intimately on the architecture/design of specific functional blocks to develop test plans. Develop new test content and/or test tools. Ensure effectiveness and coverage of tests developed in the qualification of new designs. Identify silicon bugs and debug (individually or as a team) to root cause and fix.
[01/04/13 6:07 PM]	SL-Intel:	Anyone interested on the job can apply through http://www.intel.com/jobs/jobsearch/index.htm?job=702095&src=CFE-12682
[01/04/13 6:07 PM]	vijay:	Is it IP level verification or system level verification
[01/04/13 6:08 PM]	SL-Intel:	Hi Vijay : Both .. We have a team covering IP as well as System level
[01/04/13 6:08 PM]	vijay:	OK thanks
[01/04/13 6:09 PM]	shiva:	Do we have work related to pre and post silicon verification and validation
[01/04/13 6:11 PM]	SL-Intel:	Hi Shiva , Yes .. the team will involved in Emulation work during Pre-Silicon Phase and move on to Post Silicon activities after we get the Silicon .
[01/04/13 6:12 PM]	SL-Intel:	We do have a Pre-Silicon Validation Team as well whose job scope targeting Pre-Silicon Simulation
[01/04/13 6:12 PM]	shiva:	does the Silicon bringup activities done by this team?
[01/04/13 6:12 PM]	SL-Intel:	You can visit the Pre-Silicon Validation Booth for more infor
[01/04/13 6:14 PM]	Diego:	Good morning everybody
[01/04/13 6:14 PM]	SL-Intel:	Hi Shiva, Silicon bringup or we refer to Silicon Power-On is the responsibility for Post-Silicon team
[01/04/13 6:14 PM]	SL-Intel:	Morning Diego
[01/04/13 6:14 PM]	shiva:	ok. thanks
[01/04/13 6:15 PM]	Ujjwal:	Hi SL, as long as pre-silicon validation i sconcerned, is it purely simulation based or you use formal techniques too?
[01/04/13 6:15 PM]	shiva:	what platform does the team use for validating the silicon
[01/04/13 6:15 PM]	SL-Intel:	I have my Lind-In Profile that everyone can refer to if you want to know more about me :) http://www.linkedin.com/profile/view?id=13042796&trk=tab_pro
[01/04/13 6:21 PM]	shiva:	For Emulation, does the team use Cadence palladium?
[01/04/13 6:21 PM]	SL-Intel:	Just for everyone knowledge ; my team involved in the latest CloverTrail (Atom Z2760) Tablet & Medfield Phone
[01/04/13 6:23 PM]	SL-Intel:	Hi Shiva, No to your answer
[01/04/13 6:23 PM]	shiva:	ok.

[01/04/13 6:23 PM]	Raghuraman:	Hi, how important are structural tests in Post Si validation? My background is primarily in Structued tests and its validation
[01/04/13 6:24 PM]	Raghuraman:	I dont have much experience in 'functional' vectors which may be used more in microprocessors.
[01/04/13 6:25 PM]	SL-Intel:	Hi Raghuraman, can you elobrate more on the structural tests in your context ?
[01/04/13 6:25 PM]	SL-Intel:	The key part is on functional tests
[01/04/13 6:26 PM]	SL-Intel:	in our validation world
[01/04/13 6:27 PM]	Somasekar:	I am facing connection issues with the chat, does any one face similar kind of problem
[01/04/13 6:27 PM]	vijay:	which verification methodology do you use
[01/04/13 6:27 PM]	Ujjwal:	How can you ensure good coverage using functional test only?
[01/04/13 6:28 PM]	Ujjwal:	As functional verification is very exhaustive but time consuming.
[01/04/13 6:29 PM]	shiva:	does the team involve in characterization of IP's.
[01/04/13 6:29 PM]	SL-Intel:	Hi Vijay , we have different validation sub groups covering Analog, Power and Performance , Thermal , Functional , Usage model .. The methodology used are vary
[01/04/13 6:30 PM]	vijay:	My question is related to Functional verif. In other words do you use OVM/VMM/UVM
[01/04/13 6:31 PM]	SL-Intel:	Hi Ujjwal, functional is the key part , we do have other coverage.
[01/04/13 6:32 PM]	shiva:	Does the team run testcases related to throughput measrements?
[01/04/13 6:32 PM]	SL-Intel:	Hi Shiva , Yes
[01/04/13 6:32 PM]	Ujjwal:	Hi SL, let me give you an example why I am saying so.
[01/04/13 6:32 PM]	Ujjwal:	Back in 1994, bug in the Intel P5 Pentium floating point unit.
[01/04/13 6:33 PM]	Raghuraman:	Structural tests refer primarily to DFT related patterns. It can be fined tuned to 'target' particular blocks or IPs but yes it is a structural test. If we take burn-in test, using say a 'LogicBIST' kind of approach, x-elimination becomes key and that falls in 'verification' domain.
[01/04/13 6:33 PM]	Ujjwal:	If you divide 4195835 by 3145727, the processor was giving teh result 1.333739068902037589
[01/04/13 6:33 PM]	Ajosh:	Hi SL good morning.
[01/04/13 6:34 PM]	Ujjwal:	Where as the correct result is 1.333820449136241002
[01/04/13 6:34 PM]	Ujjwal:	And it is very very difficult to detect this types of corner cases using pure functional techniques.
[01/04/13 6:35 PM]	Ujjwal:	Hence, I was asking whether you use other verification techniques like formal etc. along with functional.
[01/04/13 6:37 PM]	SL-Intel:	Hi Raghuram , Thanks . We have team under PDE (Product Development Team) that concentrate on the DFx related
[01/04/13 6:37 PM]	SL-Intel:	Good Morning Ajosh
[01/04/13 6:38 PM]	shiva:	Does the team run testcases related to throughput measurements and system strss tests?
[01/04/13 6:39 PM]	SL-Intel:	Hi Shiva , Yes we do run testcases related to throughput measurements and system strss tests
[01/04/13 6:39 PM]	Ajosh:	I am graduate MS in System on Chip(Degital Design) from Lund univesity. I have 3 years of experience in software development in C/C++. Can I apply for this position? I already applied for pre-silicon validation position.
[01/04/13 6:39 PM]	Somasekar:	Hi SL-Intel, I have around 6 yrs experience in firmware design and validation and recently pursued my masters in System on chip design from Linkoping university, sweden. I have the necessary skillsets (Perl, Assembly language programming, VHDL/Verilog, C, Digital logic design) mentioned in the job description. Will I be considered for the validation position?
[01/04/13 6:40 PM]	SL-Intel:	Hi Ujjwal : We do have formal verification .. mainly in Pre-Silicon Phase
[01/04/13 6:40 PM]	Ujjwal:	Hi SL, Very happy to know this.
[01/04/13 6:40 PM]	shiva:	Does the team has regression suite to run tests on silicon
[01/04/13 6:41 PM]	SL-Intel:	Hi Somasekar , Certainly ... you can apply through http://www.intel.com/jobs/jobsearch/index.htm?job=702095&src=CFE-12682
[01/04/13 6:42 PM]	SL-Intel:	Hi Ajosh , Yes can
[01/04/13 6:42 PM]	vijay:	do you use OVM/VMM/UVM in functional verif
[01/04/13 6:42 PM]	Ujjwal:	So, I mean the pre-silicon verification team use all these techniques viz. assertion based verification, static formal verification, simulation with assertions, hybrid formal verification etc. And I will be very interested to work in all these fields.
[01/04/13 6:45 PM]	Ajit:	Hi. Can you please brief on the post si validation activities covered by your group

[01/04/13 6:45 PM]	SL-Intel:	Hi Vijay , mainly internal tools & methodology
[01/04/13 6:45 PM]	Raghuraman:	Thanks for the response, do we have a booth for DFX here or does it fall under another domain?
[01/04/13 6:45 PM]	shiva:	does the team involve in low power functional validation as well
[01/04/13 6:47 PM]	SL-Intel:	Hi Ujjwal , You can visit Pre-Silicon booth
[01/04/13 6:47 PM]	Ajosh:	Thank you very much SL
[01/04/13 6:48 PM]	SL-Intel:	Hi Ajit, We validate and verify the logic of new architectural features of next generation ATOM SOC designs. This encompasses knowing intimately on the architecture/design of specific functional blocks to develop test plans. Develop new test content and/or test tools. Ensure effectiveness and coverage of tests developed in the qualification of new designs. Identify silicon bugs and debug (individually or as a team) to root cause and fix. You can refer more infor in my Lind-In Profile
[01/04/13 6:50 PM]	Ajit:	Thanks. So do you own the validation from Si-bringup phase (on the 1st eng samples) or get involved from pre-si phase itself ... (sorry if this is a repeat question)
[01/04/13 6:50 PM]	Rashid.M P:	Hi SL, Good Morning.. Does your team also invloved in any kind of Front End Verification?
[01/04/13 6:50 PM]	SL-Intel:	Hi Raghuraman, you can deposit your resume in the intel job online
[01/04/13 6:53 PM]	Ujjwal:	Thanks SL, I will go to pre-silicon validation booth now. Nice e-meeting you!
[01/04/13 6:53 PM]	SL-Intel:	Hi Ajit, we involved in both .. For Pre-Silicon Phase , mainly in Emulation + getting the Hardware & Infra ready . For Post Silicon , we own the activities from Si-bringup
[01/04/13 6:54 PM]	Mazlina-Intel:	Hi to everyone who has just joined. Please take this oppotunity to ask questions! If you're keen to apply, send your resume here http://www.intel.com/jobs/jobsearch/index.htm?job=702095&src=CFE-12682
[01/04/13 6:55 PM]	Raghuraman:	My resume is already available in intel website.
[01/04/13 6:56 PM]	Mazlina-Intel:	Great! We'll have a look at your profile after this event
[01/04/13 6:57 PM]	Ajit:	Nice to know. What is the validation test case development flow? Do you resuse/import the test suite from pre-si to post-si ? i mean is the flow similar to : pre-si -> emulation -> post-si
[01/04/13 6:59 PM]	Somasekar:	Hi SL-Intel, Thanks for your reply. I have already applied for the position through intel job portal site.
[01/04/13 7:00 PM]	SL-Intel:	Hi Ajit, Yes and No .. it will depend on area of validation
[01/04/13 7:01 PM]	SL-Intel:	But its always the practise to ensure we can have the content reuse from Pre to Post
[01/04/13 7:01 PM]	Hemraj:	@SL, do you also cover power measurements, analysis, and optimisation, in pre-silicon and post silicon phases?
[01/04/13 7:01 PM]	Ajit:	thanks ... that answers my question
[01/04/13 7:02 PM]	Ajit:	what tools / platforms are used for the post-si validation ?
[01/04/13 7:03 PM]	SL-Intel:	Hi Hemraj , Yes we do cover Power Measurements, analysis, and optimisation in my team .
[01/04/13 7:04 PM]	Hemraj:	thanks, and how about test automation, regressions, silicon screen flow ?
[01/04/13 7:04 PM]	SL-Intel:	Hi Ajit , we mainly use in house tools.
[01/04/13 7:05 PM]	Ajit:	do you also cover electrical characterization across PVT corners ?
[01/04/13 7:06 PM]	SL-Intel:	Hi Hemraj , we have an automation team that taking care of all automation tools. Regression is cover by Post Silicon .
[01/04/13 7:06 PM]	SL-Intel:	Hi Ajit , Yes we cover that
[01/04/13 7:06 PM]	Ajit:	thanks good to know
[01/04/13 7:09 PM]	Ajit:	who owns up the responsibility for debuggin the faults found Si ..... do you totally refer back to pre-si / design team or actively involve with them
[01/04/13 7:09 PM]	SL-Intel:	Hello, and welcome to our Virtual Event! If you are just now joining, please be sure you have applied online for the appropriate position so we can access your resume for positions we are looking to fill now and in the future! All active job openings posted athttp://www.intel.com/jobs/index.htm
[01/04/13 7:11 PM]	SL-Intel:	Hi Ajit , it depend on the complexity of the issue/fault. We do refer to design team on needs basis
[01/04/13 7:11 PM]	SL-Intel:	But majority of issue can be resolved/root cause by the Post Silicon team
[01/04/13 7:12 PM]	Ajit:	thanks ... i am actually trying to understand the entire flow and seek similarities with my prev exp
[01/04/13 7:13 PM]	Hemraj:	@SL, do you use silicon interposer tools to confirm the boards complete correctness before the new silicon ?
[01/04/13 7:13 PM]	SL-Intel:	Hi Ajit, you are welcome :)

[01/04/13 7:14 PM]	SL-Intel:	Hi Hemraj , Yes we do
[01/04/13 7:15 PM]	Rashid.M P:	Hi SL, I have posted my resume. Looking forward to chat with you.
[01/04/13 7:15 PM]	Rashid.M P:	Thanks
[01/04/13 7:15 PM]	SL-Intel:	Thanks Rashid
[01/04/13 7:16 PM]	Hemraj:	@SL, good to know this. What is the percentage of the first pass silicon and do you plan the engineering samples stage or target for the first pass silicon in the original plan?
[01/04/13 7:19 PM]	SL-Intel:	Hi Hemraj , We have the activities planned in .
[01/04/13 7:21 PM]	Hemraj:	@SL, Do you have the complete validation setup and debug flow at Malaysia ? OR part of the activities are covered at other sites? I mean do you distribute the acitivities of one chip across different sites? That changes the dimension of the project planning significantly, so this question?
[01/04/13 7:21 PM]	nakkeraneeran.k:	Hi SL team, You mentioned to do validation for micro-servers, will it be system level automation testing ?
[01/04/13 7:23 PM]	SL-Intel:	Hi Hemraj , we do have full capabilities in Penang . The roles & responsibility for a particular project might be distributed across different sites.
[01/04/13 7:23 PM]	nakkeraneeran.k:	What type of activities involved in micro-server validation
[01/04/13 7:24 PM]	nakkeraneeran.k:	I mean will it be BIOS/UEFI level or overall system product level
[01/04/13 7:25 PM]	SL-Intel:	Hi Nakkeraneeran, we have a team involved in uServer Pre-Silicon Validation (you can visit Logic Design/Arch). For Post Silicon , we involved in ATOM CPU validation .
[01/04/13 7:25 PM]	Ajit:	one last question .... is this current opening for a IC level or Lead role
[01/04/13 7:26 PM]	SL-Intel:	Hi Ajit ... Both
[01/04/13 7:27 PM]	Hemraj:	@SL, For the validation , how much importance you have for the CPU core level activities? OR for you the CPU core can be treated as the prooven component?
[01/04/13 7:27 PM]	nakkeraneeran.k:	So ATOM Validatiion products mean only for client. So logic design team have their own validation team?
[01/04/13 7:28 PM]	SL-Intel:	Hi Hemraj , we have 2 team , one on ATOM CPU validation , the other on SoC Validation .
[01/04/13 7:29 PM]	nakkeraneeran.k:	what is team strength of validation team, are you expanding , How diverse is the team?
[01/04/13 7:30 PM]	Hemraj:	Thanks, I wanted to confirmt he same. These two activities are different in scope and timeline, so it makes sense to have two separate teams...
[01/04/13 7:30 PM]	SL-Intel:	Hi Nakkeraneeran, ATOM validation cover products that used ATOM Core ..Phone, Tablet , uServer ..
[01/04/13 7:31 PM]	Hemraj:	So in this conxt, is it mandatory to have deep expertise with Intel CPU acrchitecture for the SOC validation activity? OR is it not mandatory?
[01/04/13 7:32 PM]	nakkeraneeran.k:	Thanks for confirming. I understand from my friends in intel bangalore - they are performing similar activities
[01/04/13 7:32 PM]	SL-Intel:	Hi Nakkeraneeran, We do have quite a number of International Hiring in our team :)
[01/04/13 7:33 PM]	nakkeraneeran.k:	Thats hearteniing to see...
[01/04/13 7:34 PM]	SL-Intel:	Hi Hemraj, No need to have deep CPU expertise for SOC validation , the ATOM Core team will cover that . Both team are working site-by-site
[01/04/13 7:34 PM]	Hemraj:	thanks for confirming again...
[01/04/13 7:35 PM]	nakkeraneeran.k:	If I need to apply for these openings, what I need to prepare myself , basically expectations
[01/04/13 7:35 PM]	SL-Intel:	Hi Nakkeraneeran, we have couples team across different Geo under the same Validation Org .
[01/04/13 7:36 PM]	SL-Intel:	Intel Bangalore do have similar team and working in different products
[01/04/13 7:36 PM]	nakkeraneeran.k:	Fine
[01/04/13 7:38 PM]	nakkeraneeran.k:	so any specific advantage working in malyasia-intel
[01/04/13 7:38 PM]	SL-Intel:	Hi Nakkeraneeran, just submit the resume .. we will contact you if you meet the requirement :)
[01/04/13 7:39 PM]	SL-Intel:	Hi Nakkeraneeran, Intel has a comprehensive pay, stock and benefits programs. You may check out this link for details http://www.intel.com/jobs/malaysia/bencomp/
[01/04/13 7:44 PM]	SL-Intel:	(15 minute warning): Just a reminder that the event will be ending in 15 minutes. We'll do our best to answer your questions in this time. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen.
[01/04/13 7:46 PM]	vinod.ch:	which language do you use for the validation
[01/04/13 7:49 PM]	SL-Intel:	Hi Vinod, it depend on which area of validation .. mainly in house

[01/04/13 7:51 PM]	Ajit:	@SL : thanks for the information, i have just submitted my resume
[01/04/13 7:53 PM]	SL-Intel:	Thanks Ajit
[01/04/13 7:53 PM]	vinod.ch:	I have submitted my resume...
[01/04/13 7:54 PM]	SL-Intel:	Thanks Vinod
[01/04/13 7:55 PM]	SL-Intel:	(5 minute warning): Just a reminder that the event will be ending in 5 minutes.
[01/04/13 7:57 PM]	SL-Intel:	Hi Nicky .. any questions you have ?
[01/04/13 7:59 PM]	jagadeesh:	Hi
[01/04/13 7:59 PM]	SL-Intel:	Hi ..
[01/04/13 7:59 PM]	jagadeesh:	I have 5+ exp in ASIC Verification (IP/SOC)
[01/04/13 8:00 PM]	SL-Intel:	Hi Jagadessh , do submit your resume :)
[01/04/13 8:01 PM]	jagadeesh:	Can I know which domain application your team is working
[01/04/13 8:01 PM]	Mazlina-Intel:	Our career fair is now ending. We appreciate your questions and the time you took to meet with us today. We hope this event helped you to better understand Intel and the jobs available. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen.For your convenience, this chat transcript will be available
[01/04/13 8:02 PM]	SL-Intel:	Hi Jagadeesh, you can refer to the previous transcript I answer .
[01/04/13 8:02 PM]	SL-Intel:	Thank You everyone :)
[01/04/13 8:02 PM]	SL-Intel:	Bye ....
[01/04/13 8:02 PM]	jagadeesh:	thanks SL have a nice day to all..