Brunch with Sr. Managers at Intel Malaysia

Booth Chat -Design gurus need to apply here
All times shown in PST

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[01/04/13 5:58 PM]	James-Intel:	Hello, and welcome to our Virtual Event! If you are just now joining, please be sure you have applied online for the appropriate position so we can access your resume for positions we are looking to fill now and in the future! Apply to:Structural Design Engineer http://www.intel.com/jobs/jobsearch/index.htm?job=702091&src=CFE-12682
[01/04/13 5:58 PM]	James-Intel:	Feel free to submit your questions
[01/04/13 6:05 PM]	James-Intel:	Hi, welcome to the Structural Physical Design booth
[01/04/13 6:05 PM]	James-Intel:	Please let me know how can I help you
[01/04/13 6:10 PM]	Nathan:	Hi James. I'm a student who just recently grad. from Wawasan Open Uni. at Penang. Currently has 7 year of PC architecture involvement. It's there any structual design for junior positions?
[01/04/13 6:11 PM]	James-Intel:	Yes, positions are available
[01/04/13 6:11 PM]	James-Intel:	If you would like to apply for the position, please go ahead and submit your resume at this link
[01/04/13 6:11 PM]	James-Intel:	http://www.intel.com/jobs/jobsearch/index.htm?job=702091&src=CFE-12682
[01/04/13 6:13 PM]	James-Intel:	Feel free to ask any questions if you would like to understand more about the job
[01/04/13 6:15 PM]	VENKATA:	Hi James
[01/04/13 6:15 PM]	Nathan:	Btw, i had a product want to develop but much of it are still in concect phase and its related to pc architecture. Can i proposal to some one at intel?
[01/04/13 6:16 PM]	James-Intel:	Hi
[01/04/13 6:16 PM]	VENKATA:	i have applied to the job 3 days agao. Did you get a chance to look at the resume ?
[01/04/13 6:18 PM]	James-Intel:	Nathan, we can probably talk about the development offline
[01/04/13 6:19 PM]	James-Intel:	Tangirala, we have yet to fully look through the resume, but for this fair, feel free to ask questions that could help you understand the job more
[01/04/13 6:21 PM]	Nathan:	can you sent me the particular address or can we meet at PG-7?
[01/04/13 6:21 PM]	Raghuraman:	Good Morning, Raghu here. Does 'Structural Design' refer to or also include 'Structural tests' in its considerations?
[01/04/13 6:22 PM]	VENKATA:	The role is more of block level implementaion or full chip implementation ?
[01/04/13 6:23 PM]	James-Intel:	Rajanarayanan, Structural Design here does not stand for structural test but more of the synthesis of the RTL
[01/04/13 6:23 PM]	James-Intel:	please elaborate on your definition on structural test
[01/04/13 6:23 PM]	James-Intel:	Tangirala, the role includes both block level and full chip level implementation
[01/04/13 6:24 PM]	James-Intel:	Nathan, I will find someone to contact you on what is your plan first
[01/04/13 6:26 PM]	James-Intel:	Structural Physical Design in Penang does involved in the design of data center ingredients, Ultrabooks, phones and tablets
[01/04/13 6:28 PM]	Saurabh:	I have 7+yrs of exp in Physical Design, and worked on Synthesis to GDSII, I guessits the same thing you call Structural design in Intel, I had already apply online, Is there anythingelase needs to be done to apply for this job?
[01/04/13 6:29 PM]	James-Intel:	Bhadoriya, if you have submitted your resume online, we would inform you if we have you shortlisted for interview
[01/04/13 6:29 PM]	Nathan:	It's called Multi Processing Unit or MPU. It like an APU (CPU + GPU) but makes it special is it's matrix architecture, allowing expansion beyond the binary method for core of processors (i.e.: 2, 4, 6, 8).
[01/04/13 6:29 PM]	James-Intel:	Nothing else need to be done to apply for the job
[01/04/13 6:31 PM]	Saurabh:	Thanks!, will wait for you to consider it then :)
[01/04/13 6:31 PM]	James-Intel:	Feel free to use this forum to know more about the job :)
[01/04/13 6:31 PM]	Saurabh:	sure, Thanks!
[01/04/13 6:31 PM]	VENKATA:	James, which technology is being used for the current designs ?
[01/04/13 6:31 PM]	James-Intel:	Nathan, thanks for your interest in collaborating with us in developing your concept
[01/04/13 6:32 PM]	James-Intel:	I will find the appropriate rep in the company to contact you :)
[01/04/13 6:33 PM]	James-Intel:	Tangirala, my guess is you are asking about the process technology? However, it is confidential for me to divulge it here. Suffice to say that we are involve in probably the

		latest and greatest process technology today
[01/04/13 6:36 PM]	Nathan:	Another question. So far has intel ramped up the production of nano carbon tubes for MOSFET transisfor in the SoC for sampling? If got, when it will be ready or as stated around 2015 - 2017 in Intel Developer Forum 2011?
[01/04/13 6:38 PM]	VENKATA:	thanks. Do we also need to chiplet ESD runs ? I have experience in mentor graphiss and Apache ESD tools
[01/04/13 6:40 PM]	James-Intel:	Tangirala, reliability verification was one of the skillset that we are looking for too
[01/04/13 6:41 PM]	James-Intel:	So any ESD experience is relevant
[01/04/13 6:43 PM]	James-Intel:	Nathan, unfortunately I do not have the answer for your question for nano carbon tubes
[01/04/13 6:44 PM]	Nathan:	It ok.
[01/04/13 6:45 PM]	Zhe:	Hi, may I know if this position is for experienced hires or RCG?
[01/04/13 6:46 PM]	Mazlina-Intel:	@Nathan - unfortunately we don't have the details to your questions
[01/04/13 6:48 PM]	Mazlina-Intel:	@Zhe Xi - today's focus is on experienced positions but we're always open to receive any profiles
[01/04/13 6:48 PM]	Nathan:	I think you guys may try locate it on IDF website but as i remember there are no past record pdfs been kept. It's ok. I understands.
[01/04/13 6:50 PM]	VENKATA:	Hi James, one more question.. does the role needs any very often travel requirements ?
[01/04/13 6:51 PM]	James-Intel:	Hi Tangirala, travelling would be based on business needs
[01/04/13 6:52 PM]	VENKATA:	okay.. thanks for all the information James..
[01/04/13 6:53 PM]	James-Intel:	However, if an employee does not have preference on travelling, managers will check for feasibility to accomodate that
[01/04/13 6:53 PM]	Ajosh	Hi Jam James Good morning
[01/04/13 6:53 PM]	Raghuraman:	Structural test is more from a DFM perspective - can we manufacture/fabricate as is expected? So to ensure that we have manufactured as desired, we need to validate the same. this is a 'structural test'. Let me know if you view it otherwise.
[01/04/13 6:54 PM]	Ajosh	Do you consider graduate in your group? I completed MS in Digital Design from Lund university.
[01/04/13 6:57 PM]	James-Intel:	Hi Jose, we do consider graduate, so feel free to submit your resume online as well
[01/04/13 6:59 PM]	James-Intel:	Hi Rajanarayanan, thanks for your clarification
[01/04/13 6:59 PM]	Vivek:	Hi James
[01/04/13 6:59 PM]	James-Intel:	I believe Ann had talked to you :)
[01/04/13 6:59 PM]	James-Intel:	Hi Bhatia
[01/04/13 7:00 PM]	Vivek:	James, I have a query regarding IORing.
[01/04/13 7:00 PM]	James-Intel:	yes Bhatia
[01/04/13 7:01 PM]	James-Intel:	go ahead
[01/04/13 7:01 PM]	Vivek:	I have specific expertise in IORing design aligned with ESD requirements.
[01/04/13 7:01 PM]	James-Intel:	Everyone, feel free to ask questions for you to have better visibility on the structural physical design in IAG-M
[01/04/13 7:02 PM]	Vivek:	This would also include driving substrate design and package requirement.
[01/04/13 7:02 PM]	Vivek:	Power/Signal integrity with package parasitics.
[01/04/13 7:04 PM]	Vivek:	Do you see a specific requirement for my expertise area?
[01/04/13 7:05 PM]	James-Intel:	Bhatia, your expertise matches the needs of some groups within IAG-M. It is however different from Structural Physical Design
[01/04/13 7:06 PM]	James-Intel:	So Bhatia, feel free to go ahead and check for possiblity in jobs.intel.com :)
[01/04/13 7:06 PM]	Vivek:	Which is the IAG-M group?
[01/04/13 7:06 PM]	Zhe:	The R&D division for Intel.
[01/04/13 7:07 PM]	Mazlina-Intel:	Be sure you visit the right booth to hear from our manager. You can see and hear what we're looking for by clicking at the presentation slide in each booth.
[01/04/13 7:07 PM]	Vivek:	OK. I saw a question on ESD earlier. What was the query?
[01/04/13 7:08 PM]	Ajosh	Thanks for the information James
[01/04/13 7:10 PM]	James-Intel:	Bhatia, the query is whether ESD verification is something that is relevant, and the answer is yes in the reliablity verification realm
[01/04/13 7:10 PM]	Vivek:	Is there a senior manager available to whom I can talk?
[01/04/13 7:12 PM]	Vivek:	in IAG-M group.
[01/04/13 7:13 PM]	Mazlina-Intel:	@Vivek - can you send your resume to http://www.intel.com/jobs
[01/04/13 7:14 PM]	Mazlina-Intel:	We'll take a look at your profile after this event and if we have a suitable position we'll get the appropriate manager to get in touch with you

[01/04/13 7:16 PM]	VENKATA:	James, thanks for the info. i am logging-out now
[01/04/13 7:26 PM]	Raghuraman:	I have heard of Intel's validation from a physical design perspective - maybe on the lines of say Mentor's Calibre tool. 'Defect based' testing is considered another USP for Intel. I guess there is a rule deck to target, say long parallel wires in the chips.
[01/04/13 7:28 PM]	Raghuraman:	So how far is 'physical design validation' (maybe you call that as Structural Design) static or validated through simulation?
[01/04/13 7:29 PM]	James-Intel:	Raghuraman, for structural physical design we do look for engineering expertise in static timing analysis
[01/04/13 7:31 PM]	yatin:	Hi James
[01/04/13 7:31 PM]	yatin:	morning
[01/04/13 7:32 PM]	James-Intel:	morning yatin
[01/04/13 7:32 PM]	yatin:	I am into synthesis and timing
[01/04/13 7:32 PM]	yatin:	Do you have a suitable opening?
[01/04/13 7:32 PM]	James-Intel:	good, that is the skillset we are looking for
[01/04/13 7:32 PM]	James-Intel:	have you submitted your resume?
[01/04/13 7:32 PM]	yatin:	not yet I think
[01/04/13 7:33 PM]	James-Intel:	do go ahead and submit your resume to this link
[01/04/13 7:33 PM]	James-Intel:	http://www.intel.com/jobs/jobsearch/index.htm?job=702091&src=CFE-12682
[01/04/13 7:33 PM]	yatin:	sure
[01/04/13 7:33 PM]	yatin:	actually i couldnt find any specific timing related opening
[01/04/13 7:33 PM]	James-Intel:	yatin, do you have experience in auto place and route as well?
[01/04/13 7:34 PM]	yatin:	no... I have little design and ATE related backround...
[01/04/13 7:34 PM]	yatin:	i generally work as a bridge between design and back end engineers
[01/04/13 7:35 PM]	James-Intel:	I see
[01/04/13 7:35 PM]	James-Intel:	your synthesis and timing knowledge expertise is what we would need
[01/04/13 7:35 PM]	yatin:	ok
[01/04/13 7:35 PM]	yatin:	i am checking your linke and applying
[01/04/13 7:36 PM]	James-Intel:	yes, thanks
[01/04/13 7:36 PM]	yatin:	thats all, right?
[01/04/13 7:40 PM]	James-Intel:	yes
[01/04/13 7:46 PM]	James-Intel:	Hi, feel free to submit your questions
[01/04/13 7:47 PM]	Santosh:	Hi
[01/04/13 7:47 PM]	Santosh:	I am mixed signal design engineer
[01/04/13 7:48 PM]	James-Intel:	I see
[01/04/13 7:48 PM]	James-Intel:	are you exploring a career in structural physical design?
[01/04/13 7:48 PM]	Santosh:	I have little bit knowledge on this
[01/04/13 7:48 PM]	Santosh:	but looking for change
[01/04/13 7:49 PM]	James-Intel:	I see
[01/04/13 7:49 PM]	James-Intel:	which area of structural physical design you are looking to change to?
[01/04/13 7:50 PM]	James-Intel:	(10 minute warning): Just a reminder that the event will be ending in 15 minutes. We'll do our best to answer your questions in this time. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen
[01/04/13 7:50 PM]	Santosh:	what are the options are?
[01/04/13 7:52 PM]	James-Intel:	we have synthesis, physical synthesis, reliability verification, static timing analysis, functional verification, clock tree design
[01/04/13 7:52 PM]	James-Intel:	with your mixed signal design expertise
[01/04/13 7:52 PM]	James-Intel:	I would recommend clock design and static timing analysis as a start
[01/04/13 7:53 PM]	Santosh:	ok
[01/04/13 7:53 PM]	Santosh:	I have submitted by cv
[01/04/13 7:53 PM]	Santosh:	I think last week
[01/04/13 7:54 PM]	James-Intel:	allright, we will be reviewing through the resumes
[01/04/13 7:55 PM]	Santosh:	Please let me know if considered further
[01/04/13 7:57 PM]	Santosh:	Thanks for your time

[01/04/13 7:57 PM]	James-Intel:	allright
[01/04/13 7:57 PM]	Santosh:	Bye
[01/04/13 7:59 PM]	James-Intel:	Thank you for participating in this Virtual Career Fair
[01/04/13 8:00 PM]	James-Intel:	Our career fair is now ending. We appreciate your questions and the time you took to meet with us today. We hope this event helped you to better understand Intel and the jobs available. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen.For your convenience, this chat transcript will be available for further