Brunch with Sr. Managers at Intel Malaysia

Booth Chat -We're glad you visited the Senior/Staff SOC Pre-Silicon Design Validation Engineer booth
All times shown in PST

100 Most Recent Messages | **All Messages**

[01/04/13 5:50 PM]	Ann-Intel:	Hello, and welcome to our Virtual Event!
[01/04/13 5:55 PM]	Ann-Intel:	If you are just now joining, please be sure you have applied online for the appropriate position so we can access your resume for positions we are looking to fill now and in the future! Apply to:
[01/04/13 5:55 PM]	Ann-Intel:	SOC Pre-Silicon Design Validation Engineerhttp://www.intel.com/jobs/jobsearch/index.htm?job=702097&src=CFE-12682
[01/04/13 6:00 PM]	Ann-Intel:	Hi Vinesh, welcome!
[01/04/13 6:01 PM]	Vinesh:	Hi Ann
[01/04/13 6:01 PM]	Ann-Intel:	Do you have any questions that i can help answer today?
[01/04/13 6:02 PM]	Vinesh:	Just was visiting the video . So does your team is responsible for emulation
[01/04/13 6:02 PM]	Ann-Intel:	Yes, we have an emulation team as well
[01/04/13 6:04 PM]	Vinesh:	So if I understand correctly nature of wrk that is being done is after varification stage , using fpga s or other emulators to run c - based test cases ?
[01/04/13 6:04 PM]	Vinesh:	*verif
[01/04/13 6:05 PM]	Ann-Intel:	We cover both Pre Silicon as well as emulation
[01/04/13 6:06 PM]	Ajosh:	Hi Ann
[01/04/13 6:06 PM]	Ann-Intel:	Hi Ajosh
[01/04/13 6:08 PM]	Ann-Intel:	Do you have questions to ask me today?
[01/04/13 6:08 PM]	Vinesh:	Ann is the recrutment for Malysia or India
[01/04/13 6:09 PM]	Ann-Intel:	In Penang, Malaysia
[01/04/13 6:09 PM]	Vinesh:	ok thanks.
[01/04/13 6:09 PM]	Vinesh:	Thanks for details.
[01/04/13 6:10 PM]	Ajosh:	I am a graduate. I am from India. I completed MS in System on Chip (Digital Design) . Am I eligible to apply for this position.
[01/04/13 6:10 PM]	Ann-Intel:	sure no problem
[01/04/13 6:11 PM]	Ann-Intel:	@Ajosh, do you have any work experience?
[01/04/13 6:12 PM]	Ajosh:	yes I have 3 years software development in C/C++
[01/04/13 6:12 PM]	Ann-Intel:	oh good, that you are eligible for this position. Pls do remember to send in your resume
[01/04/13 6:12 PM]	Ajosh:	I applied for this position
[01/04/13 6:12 PM]	Ajosh:	you can see my resume
[01/04/13 6:14 PM]	Ann-Intel:	@Ajosh, because of time constraints I will look at it after the event
[01/04/13 6:14 PM]	Ajosh:	ok thanks
[01/04/13 6:14 PM]	Ann-Intel:	thanks for submitting your resume
[01/04/13 6:15 PM]	Raghuraman:	Good morning, Raghu here. My profile is already available in Intel website.
[01/04/13 6:16 PM]	Ann-Intel:	Good Morning Raghu, thank for submitting your resume
[01/04/13 6:17 PM]	Raghuraman:	Is the job description referring to 'verification' using either Intel 'internal' tools or industry wide known constructs/tools like using Vera etc
[01/04/13 6:17 PM]	Ajosh:	I have one more question. when can I hear from you about this position? Is intel provide visa for non-malaysians?
[01/04/13 6:18 PM]	Ann-Intel:	@Raghu, we are using a mixture of both. Some of the industry tools we are using for verfication is OVM
[01/04/13 6:19 PM]	Raghuraman:	Ok, I was checking because I have heard from friends in Intel (US and India) about the usage of 'internal/proprietary' tools. Of course, flows are likely to 'internal' in every company.
[01/04/13 6:19 PM]	Ann-Intel:	@Ajosh, Intel will sponsor International candidates for their work permit and dependent pass (if required). And Response times to applications can vary. Some managers quickly review candidates and pick up the phone and call for a phone screen. Others can take more time to review their applicants. The best thing you can do is apply to all jobs that you feel interested in and at least 80% qualified for! We have many recruiters that review resumes and this is a good way to be seen by all.

[01/04/13 6:23 PM]	Ajosh:	I am maily interested in design and validation positions. Thanks for the information Ann
[01/04/13 6:24 PM]	Ann-Intel:	@Ajosh, great! Lets talk more when I review your resume later
[01/04/13 6:26 PM]	Ajosh:	i believe i requested you in linkedin
[01/04/13 6:26 PM]	Raghuraman:	Does Pre-Silicon Design Validation also include DFT in its ambit or is it 'pure Verification'? My background is primarily in DFT.
[01/04/13 6:26 PM]	Ajosh:	thank you verymuch for your help
[01/04/13 6:27 PM]	Ann-Intel:	@Raghu, Yes its includes DFT verification as well!
[01/04/13 6:29 PM]	Raghuraman:	Burn-in should be very important in Intel chips. So does Intel employ 'LogicBIST' type approach or reuse structural vectors? Does Intel do a monitored burn-in or non-monitored one?
[01/04/13 6:30 PM]	Hemraj:	@Mazlina, Hi I have sent my resume earlier to you. Can we talk about this position now?
[01/04/13 6:31 PM]	Ann-Intel:	@Raghu, we do do Burn-in Validation. For more details we can talk during the interview :)
[01/04/13 6:31 PM]	Ann-Intel:	@Hemraj, I can take your question about the postion if you have any
[01/04/13 6:35 PM]	Raghuraman:	Ann, sorry if I got 'overly' technical ;) I was curious because burn-in could mix 'verification' and 'DFT' domains. It may require an early 'DFT engagement' for the design.
[01/04/13 6:36 PM]	Ann-Intel:	Raghu, my Pre Silicon Validation team focusing on DFT Burn-in team is focusing on early DFT verifcation in simulation.
[01/04/13 6:37 PM]	Ann-Intel:	We than we alias with our QRE team to do the other post silicon burn-in validation
[01/04/13 6:37 PM]	Hemraj:	/@Ann, thanks. HAve you seen my resume? I have understood this requirement would like to check how to go further into this?
[01/04/13 6:38 PM]	Raghuraman:	oh good. thanks for the note.
[01/04/13 6:38 PM]	Ann-Intel:	@Hemraj, because of time constraints I will look at it after the event
[01/04/13 6:39 PM]	Hemraj:	@Ann, OK, so you will have one-one discussion after that ?
[01/04/13 6:40 PM]	Ann-Intel:	@Hemraj, yes I will review your resume and get back to you
[01/04/13 6:40 PM]	Hemraj:	thanks
[01/04/13 6:41 PM]	Raghuraman:	How do you 'flag' a particular IP? I mean, what are the metrics based on which you 'ok' an IP for integration into a chip?
[01/04/13 6:41 PM]	Ann-Intel:	Hi Sandeep, welcome!
[01/04/13 6:42 PM]	Sandeep:	HJi Ann
[01/04/13 6:42 PM]	Sandeep:	Hi*
[01/04/13 6:42 PM]	Sandeep:	I am a Degign Verification engineer with 8 yrs of wrk exp.
[01/04/13 6:42 PM]	Raghuraman:	How is the responsibility for the 'integration' of the IP shared across IP 'owner' and 'full chip' manager/owner?
[01/04/13 6:43 PM]	Sandeep:	was keen in knowing do you have verification work in your organization.
[01/04/13 6:43 PM]	Ann-Intel:	@Raghu, we have a detail checklist to identify which IP to choose from.
[01/04/13 6:44 PM]	Sandeep:	What I understood so far is that its a Pre silicon validation organization, which I beleive is done on a prototype board
[01/04/13 6:45 PM]	Sandeep:	what about the simulations, and verification on IP level and subsystem level. is it also done in your organization?
[01/04/13 6:47 PM]	Ann-Intel:	@Sandeep, as for the job roles of the integrator and IP Validator we have different responsibilities. The Integrator roll is more high level integration validation while the IP Validator will dive into the details of verifying the IP it elf.
[01/04/13 6:48 PM]	Ann-Intel:	@Sandeep, at pre silicon we mainly do validation at simulation and we have some on emulation too
[01/04/13 6:49 PM]	Sandeep:	what methodology is used for doing the validation? is it a C based environment or you use some HVLs ?
[01/04/13 6:49 PM]	Raghuraman:	oh! emulation for IPs? I have seen emulation for full chip, not for IP as such.
[01/04/13 6:50 PM]	Ann-Intel:	Emulation for the SOC
[01/04/13 6:50 PM]	Raghuraman:	oh,ok.
[01/04/13 6:50 PM]	Sandeep:	I understand if IPs are complex they need to be put on emulator,
[01/04/13 6:50 PM]	Ann-Intel:	@Sandeep, we use OVM and SVTB
[01/04/13 6:50 PM]	Sandeep:	We did similar work in past
[01/04/13 6:50 PM]	Sandeep:	ok,
[01/04/13 6:52 PM]	Sandeep:	Anne, I work on verification using UVM and system Verilog, on a FPGA centric design

		for wireless LTE hardware, I am interested in exploring similar work .. i.e. in verification
[01/04/13 6:53 PM]	Sandeep:	Can I be considered for the openings you have in your organization?
[01/04/13 6:53 PM]	Ann-Intel:	@Sandeeep, thats great. Pls send in your resume and I will take a look at your resume; Will get back to you
[01/04/13 6:53 PM]	Sandeep:	In past I have worked on ASICs for cable modem for STBox implementation
[01/04/13 6:54 PM]	Sandeep:	ok, thanks
[01/04/13 6:56 PM]	Raghuraman:	How much is Intel, Penang into validation of n/w IPs?
[01/04/13 6:57 PM]	Raghuraman:	I am not sure if the IPs are processor-driven/focussed.
[01/04/13 6:58 PM]	Ann-Intel:	@Raghu, to be sure, can you explain what is n/w IP?
[01/04/13 7:00 PM]	Raghuraman:	in the current company, we do mainly networking (n/w) chips and most of it is 'analog'. So to cover them 'structurally', we have to model them in an appropriate 'digital' view.
[01/04/13 7:01 PM]	Raghuraman:	correction. not most of it. a 'significant' chunk of it - from an area perspective - 25% to 40% of the die area.
[01/04/13 7:01 PM]	Ann-Intel:	@Raghu, thanks for your explanation!
[01/04/13 7:01 PM]	Raghuraman:	so I am not sure if microprocessor chips will have high 'analog' content. How is analog handled - that is what I wanted to check.
[01/04/13 7:04 PM]	Raghuraman:	I see 'Networking Lounge' in the initial Welcome page - thats why i asked.
[01/04/13 7:04 PM]	Ann-Intel:	@Raghu, our analog design are mainly high speed low power analog design. Not really into RF design
[01/04/13 7:06 PM]	Raghuraman:	As I mentioned, I am working in n/w chips and see significant analog challenge. Seeing 'Networking lounge', I was checking how you handle analog. Yes, I was not talking of RF design.
[01/04/13 7:07 PM]	Raghuraman:	Your point brings another interesting question. Do you, I mean, does Intel do 'power binning'? That is actually a 'hot' topic - pun intended ;)
[01/04/13 7:07 PM]	Ann-Intel:	@Raghu, we are currently not into network chips
[01/04/13 7:08 PM]	Raghuraman:	N/w chips dont bother about power but processors should. So I wanted to know how you validate low power.
[01/04/13 7:09 PM]	Arun:	Hi Ann, Good Morning... This is Arun... I have total 8+ years of experience in Design Verification. I have worked mainly on verification of CPU subsystem in SoC designs....
[01/04/13 7:09 PM]	Raghuraman:	do you have power ports in IPs (de)asserted appropriately?
[01/04/13 7:09 PM]	Ann-Intel:	Hi Arun
[01/04/13 7:10 PM]	Arun:	Hi Ann
[01/04/13 7:11 PM]	Ann-Intel:	@Raghu, are you talking about power gating? Looks like we are using different terms. We can talk more in the interview for sure!
[01/04/13 7:11 PM]	Ann-Intel:	Do you have any questions for me Arun?
[01/04/13 7:12 PM]	Arun:	Yes.. Do you have opening for Design verification positions...
[01/04/13 7:12 PM]	Ann-Intel:	@Arun, Yes we do. Pls send in your resume here SOC Pre-Silicon Design Validation Engineerhttp://www.intel.com/jobs/jobsearch/index.htm?job=702097&src=CFE-12682
[01/04/13 7:13 PM]	Arun:	Sure, will do that. Thanks Ann.
[01/04/13 7:17 PM]	Ann-Intel:	Thanks for visiting this booth, do you have any other questions for me today?
[01/04/13 7:17 PM]	Ujjwal:	Hi Ann, Good morning! Do you levearge formal verification techniques along with conventional functional verification?
[01/04/13 7:17 PM]	Ann-Intel:	@Ujjwal, Yes We do! We are very keen on FV
[01/04/13 7:19 PM]	Ujjwal:	So, I mean your team levearge static formal verification, assertion based verification, simulations with assertions, hybrid formal verification etc.
[01/04/13 7:19 PM]	Raghuraman:	How much reliance is on STA and how much in simulation? Is there SDF annotated simulation?
[01/04/13 7:19 PM]	Raghuraman:	IP could be a soft IP or hard IP.
[01/04/13 7:19 PM]	Raghuraman:	IP can be a soft IP or hard IP.
[01/04/13 7:21 PM]	Ann-Intel:	@Ujjwal, we have a few different FV techniques.
[01/04/13 7:22 PM]	Ann-Intel:	it can be a combination of FV and traditional functional validation
[01/04/13 7:22 PM]	Ujjwal:	@Ann, OK, thanks for the information. Is it different from the list I mentioned?
[01/04/13 7:23 PM]	Abhishek:	Hi Ann, One of friends in functional verification is looking for a change. He'd be keen o work for Intel. However, he is on vacation and can't apply right now through the link. I tried to above mentioned link (which you gave to Arun) but that would not let me update any other person's resume. Can I submit resume for someone else or do I need to ask him only to submit once he is back ?
[01/04/13 7:24 PM]	Ann-Intel:	@Abhishek, the link will be open for a few more days. So you can ask your friend to

		apply later when he is back
[01/04/13 7:24 PM]	JamesN-Intel:	@Raghu, yes, we do gate level simulations.
[01/04/13 7:27 PM]	Abhishek:	@Ann: Thanks Ann :)
[01/04/13 7:29 PM]	Ann-Intel:	@Abhishek, the different FV methods such as STE, top-down modeling
[01/04/13 7:33 PM]	Abhishek:	@Ann: Not sure if that was an answer to one of my queries, but thanks for the info. :)
[01/04/13 7:34 PM]	Ann-Intel:	@Abhishek, Perhaps we can talk more later in the interview session
[01/04/13 7:34 PM]	Abhishek:	Sure. :)
[01/04/13 7:35 PM]	Abhishek:	Have a nice day ahead.
[01/04/13 7:35 PM]	Ann-Intel:	You too!
[01/04/13 7:38 PM]	Ann-Intel:	Hi Hemraj, do you have any questions for me today?
[01/04/13 7:39 PM]	Hemraj:	@Ann, I have experience and interest in both Pre-silicon and post silicon validation activities. So I have to apply separetely for both positions or one application is enough?
[01/04/13 7:41 PM]	Ann-Intel:	Yes do submit your resume for both the position
[01/04/13 7:41 PM]	Ann-Intel:	in that way both the hiring manager can take a look at your resume
[01/04/13 7:42 PM]	Hemraj:	thanks..
[01/04/13 7:44 PM]	Ujjwal:	@Ann, Does your team work on verification of memories (SRAM, ROM, CAM register file etc.) and memory subsustems?
[01/04/13 7:45 PM]	Ann-Intel:	Yes we we do Memory verification...
[01/04/13 7:46 PM]	Ann-Intel:	Ujjwal, can you submit your resume if you havent
[01/04/13 7:47 PM]	Ann-Intel:	Just a reminder that the event will be ending in 15 minutes. We'll do our best to answer your questions in this time. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen.
[01/04/13 7:47 PM]	Ujjwal:	Just submitted for the job as mentioned inthe link http://www.intel.com/jobs/jobsearch/index.htm?job=702097&src=CFE-12682
[01/04/13 7:48 PM]	Ann-Intel:	alrite great!
[01/04/13 7:49 PM]	Ujjwal:	I have experience in formal verification along with conventional simulation based verification.
[01/04/13 7:53 PM]	Ann-Intel:	OK cool, will take a look at your resume
[01/04/13 7:59 PM]	Ann-Intel:	Our career fair is now ending. We appreciate your questions and the time you took to meet with us today. We hope this event helped you to better understand Intel and the jobs available. For more information about Intel, please visit intel.com or connect with us through social media on Facebook, LinkedIn or Twitter! We love to hear your feedback! Please complete our short event survey located in the bottom left of the screen.For your convenience, this chat transcript will be available for further