

## Brunch with Sr. Managers at Intel Malaysia

### Booth Chat -Senior Logic Design Engineer/Architect

All times shown in PST

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[ 01/04/13 5:55 PM] TA-Intel: Hello, and welcome to our Virtual Event! If you are just now joining, please be sure you have applied online for the appropriate position so we can access your resume for positions we are looking to fill now and in the future! Apply to:Structural Design Engineer <http://www.intel.com/jobs/jobsearch/index.htm?job=702091&src=CFE-12682>Senior Logic Design Engineer<http://www.intel.com/jobs/jobsearch/index.htm?job=702093&src=CFE-12682>Senior Validation Engineer<http://www.intel.com/jobs/jobsearch/index.h>

[ 01/04/13 5:59 PM] TA-Intel: Hi, feel free to ask any questions that u have, we are more than happy to answer

[ 01/04/13 6:06 PM] Kalyan: i have applied for this position

[ 01/04/13 6:07 PM] Kalyan: when will you start the recuritments

[ 01/04/13 6:07 PM] TA-Intel: @Kalyan, thanks for applying

[ 01/04/13 6:07 PM] Mazlina-Intel: @Kalyan Great! We'll have a look at your profile after this event

[ 01/04/13 6:07 PM] Kalyan: ok

[ 01/04/13 6:07 PM] Kalyan: i currently stay at bangalore

[ 01/04/13 6:08 PM] Mazlina-Intel: @kalyan - are u willing to relocate?

[ 01/04/13 6:08 PM] Kalyan: ya

[ 01/04/13 6:08 PM] Kalyan: i dont have a problem

[ 01/04/13 6:09 PM] Kalyan: i have currently 8 years of experience

[ 01/04/13 6:09 PM] Mazlina-Intel: Noted. Do you have any other questions?

[ 01/04/13 6:09 PM] Kalyan: in design

[ 01/04/13 6:09 PM] Kar: just want to understand if intel were to develop, software and hardware for cloud platform or intel does have close relationship such as with Microsoft and Amazon to develop the Cloud Platform ?

[ 01/04/13 6:09 PM] TA-Intel: We will go thru your resume and will contact you as soon as possible if we find the right match

[ 01/04/13 6:09 PM] Kalyan: ok

[ 01/04/13 6:10 PM] TA-Intel: @Chow - Intel have very close working relationship with the big industry players like MSFT and Google to develop sw/platform for the cloud space

[ 01/04/13 6:11 PM] Abhishek: Hi, Just wanted to know the kind of project you undertake in your design center.

[ 01/04/13 6:12 PM] Abhishek: As we all know Intel is super giant in Processor design, so in your design center its processor design only or design for Intel's other lines ?

[ 01/04/13 6:12 PM] TA-Intel: @Kohli - we are developing silicon that goes into phone/tablet/PC and also the server space, be it in SOC, chipset and CPU

[ 01/04/13 6:12 PM] Kar: may i assume that intel will help to optimize existing virtualization engine IA32 , IA64 ? Or more towards how to use cloud computing ?

[ 01/04/13 6:14 PM] TA-Intel: @Chow - Yes, Intel is one of the main developers in the Virtualization space. The technology is in our CPU/chipset

[ 01/04/13 6:14 PM] Abhishek: :) Thanks TA, Thats the bigger picture of Intel. I was looking for a little closer look on your center.

[ 01/04/13 6:14 PM] Kalyan: so are you working on RF Designs like bluetooth radio etc

[ 01/04/13 6:15 PM] TA-Intel: @Kohli - Intel Architecture Group Malaysia (IAG-M) develops integrated capabilities that enable our customers to deliver the best computing experiences. From Data Centers to Ultrabook™, Laptop, All-In-One Desktop Personal Computer, Tablet, Smart Phone and Embedded Devices, Intel Architecture Group Malaysia (IAG-M) engages in Microprocessor, Chipset and System-On-a-Chip (SOC) development that have made all these state-of-the-art innovations possible

[ 01/04/13 6:16 PM] Abhishek: Thanks. :)

[ 01/04/13 6:16 PM] TA-Intel: @kalyan - we have some engineers working on RF design

[ 01/04/13 6:16 PM] Kar: @TA - In this case the Cloud Platform group in Penang would help design hardware(CPU, SOC) for cloud Platform ?

[ 01/04/13 6:17 PM] TA-Intel: @Chow - yes. Thats correct

[ 01/04/13 6:17 PM] Vikram: Hello

[ 01/04/13 6:17 PM] TA-Intel: @ Kuralla - Hi, Welcome

[ 01/04/13 6:17 PM] Kar: @TA - Thanks alot

[ 01/04/13 6:17 PM] TA-Intel: @Chow - welcome

[ 01/04/13 6:21 PM] Vikram: Hi TA

[ 01/04/13 6:22 PM] TA-Intel: @Kuralla - Hi, Kuralla, any question that i can help to answer?

[ 01/04/13 6:22 PM] Vikram: i had gone through the JD of Logic designEng/Archtiect

[ 01/04/13 6:22 PM] Vikram: i didnt find yrs of exp you are looking for

[ 01/04/13 6:22 PM] Vikram: i am having around 11yrs of exp in SoC designs

[ 01/04/13 6:23 PM] TA-Intel: @Kuralla - that's great. We are continously looking for experienced folks to be part of the team

[ 01/04/13 6:23 PM] TA-Intel: @Kuralla - may i know which area of SOC design you are familiar with?

[ 01/04/13 6:23 PM] Khoo: Hi TA

[ 01/04/13 6:24 PM] TA-Intel: @Khoo - Hi Khoo

[ 01/04/13 6:24 PM] Khoo: HOw big is your team in INtel?

[ 01/04/13 6:24 PM] Vikram: i am working in frontend design group where we do RTL integration, synthesis, sta, PVT corner analysis, speed and power estimations etc.,

[ 01/04/13 6:25 PM] TA-Intel: @Khoo - the design team is usually consists of more than 100 engrs or more , depends on the complexity of the design

[ 01/04/13 6:26 PM] TA-Intel: @Kuralla - Those are very good experience. Not sure if you have applied our online position?

[ 01/04/13 6:26 PM] vishwanath: Hi Myself Vishwanath, Having exposure in SerDes Mixed Signal Design, do you have any openings?

[ 01/04/13 6:26 PM] Khoo: For a new design there will always be a new team?

[ 01/04/13 6:27 PM] TA-Intel: @Muniyappa - yes, you can apply to the logic design or the SOC jobs and we will help to direct it to the right hiring mgrs

[ 01/04/13 6:28 PM] TA-Intel: @Khoo- not necessary. Execution get better with experience

[ 01/04/13 6:29 PM] Khoo: i agree with you but that highly depends on the individual itself

[ 01/04/13 6:29 PM] TA-Intel: @khoo - true.

[ 01/04/13 6:29 PM] Khoo: what kind of resposibilities does Penang Design Team has?

[ 01/04/13 6:29 PM] vishwanath: Sure, General I have few questions, where I will be placed, if I get select ?

[ 01/04/13 6:29 PM] vishwanath: I am from bangalore

[ 01/04/13 6:30 PM] TA-Intel: @Khoo - silicon development - both pre silicon (logic/structural design ) and post silicon validation

[ 01/04/13 6:30 PM] TA-Intel: @muniyappa - Penang, Malaysia

[ 01/04/13 6:30 PM] vishwanath: how to send my profile to the concerned department

[ 01/04/13 6:31 PM] Khoo: do we have exposure to design work as well?

[ 01/04/13 6:31 PM] TA-Intel: @muniyappa - please apply to one of the jobs opening and we will connect you up to the correct hiring manager

[ 01/04/13 6:32 PM] TA-Intel: @khoo - yes, our engineers covers from spec, architectural to design implementation

[ 01/04/13 6:32 PM] vishwanath: OK how should I apply, I mean how to send my doc?

[ 01/04/13 6:34 PM] TA-Intel: @muniyappa - Pls use this link  
<http://www.intel.com/jobs/jobsearch/index.htm?job=702093&src=CFE-12682>

[ 01/04/13 6:36 PM] Vikram: i didnt get any idea on which level you are looking for in this group in the job profile

[ 01/04/13 6:36 PM] Vikram: thats the reason i didnt apply

[ 01/04/13 6:37 PM] Vikram: let me know if i need to apply for the same job id, and later on you will use the resume for right position

[ 01/04/13 6:37 PM] walton: hello

[ 01/04/13 6:37 PM] TA-Intel: @Kuralla - Sure. I am looking for senior engineers in logic/rtl design who is familiar with system verilog and various protocols (pci express, USB and etc). Knowledge of validation env such as OVM will be plus

[ 01/04/13 6:37 PM] TA-Intel: @Walton - Hi, Welcome

[ 01/04/13 6:38 PM] walton: i just want to inquire if intel has room for analog ic design engineers?

[ 01/04/13 6:38 PM] TA-Intel: @Kuralla - pls apply using the same job ID, thanks

[ 01/04/13 6:39 PM] Mazlina-Intel: @Vikram, if you're keen in a specific position, pls apply directly via the link. Otherwise we can always search for your profile

[ 01/04/13 6:39 PM] TA-Intel: @Lacorte - yes, we are. We are not posting it directly since we are only advertsing 6 reqs for this round. But you can apply the logic design req and i will help direct you to

the right hiring manager

[ 01/04/13 6:40 PM] walton: okay. thank you so much for this information.

[ 01/04/13 6:41 PM] TA-Intel: @Lacorte - You are Welcome

[ 01/04/13 6:41 PM] Vikram: Thanks TA and Mazlina

[ 01/04/13 6:41 PM] TA-Intel: @Kuralla - Hi Kuralla, you are Welcome

[ 01/04/13 6:42 PM] Khoo: Thanks TA

[ 01/04/13 6:43 PM] TA-Intel: @Khoo - Hi Khoo, your are Welcome

[ 01/04/13 6:50 PM] Khoo: i am a frontend custom design engineer responsible for Serdes/DPA logic design

[ 01/04/13 6:51 PM] Khoo: i have ~8 years of experience

[ 01/04/13 6:51 PM] TA-Intel: @Khoo - Hi Khoo, good to hear that. Are you doing RTL or analog design?

[ 01/04/13 6:51 PM] Khoo: not analog

[ 01/04/13 6:52 PM] Khoo: digital design

[ 01/04/13 6:52 PM] Cheng: Hi TA

[ 01/04/13 6:52 PM] TA-Intel: @Khoo - ok. If you are interested, pls apply to the logic design job opening. We are more than happy to talk to you more

[ 01/04/13 6:53 PM] Khoo: i am familiar with RTL

[ 01/04/13 6:53 PM] Khoo: but it is not ASIC flow

[ 01/04/13 6:53 PM] Khoo: we have mask engineer to perform our backend

[ 01/04/13 6:54 PM] Khoo: i am using HSPICE and not PT

[ 01/04/13 6:54 PM] TA-Intel: @Khoo - it is ok. We are looking for engineers with good design knowledge, familiarity with particular flow is secondary as it can be picked up over the project

[ 01/04/13 6:54 PM] Khoo: i am familiar with the flow

[ 01/04/13 6:54 PM] Khoo: but not that good with tools

[ 01/04/13 6:55 PM] Khoo: as my exposure to that is limited

[ 01/04/13 6:55 PM] Khoo: PT license is expensive

[ 01/04/13 6:55 PM] TA-Intel: @Khoo - sure. no problem

[ 01/04/13 6:55 PM] Khoo: i mean backend tool license

[ 01/04/13 6:55 PM] Khoo: not PT sorry

[ 01/04/13 6:56 PM] Khoo: anyway do you have opportunity to travel abroad?

[ 01/04/13 6:56 PM] TA-Intel: @Khoo - travel oppty are biz needs based

[ 01/04/13 6:57 PM] walton: hello, i just submitted my application to this opening as analog ic design engineer

[ 01/04/13 6:57 PM] TA-Intel: @Lacorte - Hi Lacorte , thanks a lot

[ 01/04/13 6:58 PM] TA-Intel: @Khoo - usually for acquiring new knowledge or support some critical tasks

[ 01/04/13 7:00 PM] TA-Intel: @Lacorte - will get back to you asap once we start processing the applications.

[ 01/04/13 7:00 PM] David: Hi TA..How are you?

[ 01/04/13 7:01 PM] TA-Intel: @David - Hi David, Welcome!

[ 01/04/13 7:01 PM] walton: thanks a lot T.A.

[ 01/04/13 7:01 PM] TA-Intel: @Lacorte - you are welcome

[ 01/04/13 7:01 PM] TA-Intel: @David - is there any question that i can help to answer?

[ 01/04/13 7:01 PM] David: I am looking for Front End Digital design opportunities in Intel

[ 01/04/13 7:02 PM] TA-Intel: @David - thats good to know. May i know where are u currently based?

[ 01/04/13 7:02 PM] David: I am in India.

[ 01/04/13 7:03 PM] TA-Intel: @David - sure. If you are interested, pls proceed to apply our on line jobs. Kindly let me know if you can access the link

[ 01/04/13 7:04 PM] David: Yes, I can access the job link. I will apply on the website.

[ 01/04/13 7:04 PM] TA-Intel: @David - thanks. Let me know if you have other questions.

[ 01/04/13 7:05 PM] David: I wish to know the nature and scope of this job. Does it involve Architecture development, involve in Back End activities etc.

[ 01/04/13 7:05 PM] Khoo: Hi TA, does PDC own project? or collaborate with other Mega site?

[ 01/04/13 7:06 PM] TA-Intel: @David - it is mainly for RTL design. The backend (for pre silicon work) will be in the booth for structural design. We have post silicon jobs which involve post silicon validation

[ 01/04/13 7:07 PM] TA-Intel: @Khoo - we are taking lead in some projetcts and collaborate with other teams in some other projects

[ 01/04/13 7:08 PM] David: Ok..I am a Front End Engineer...I was keen to know the scope of the project .

[ 01/04/13 7:09 PM] TA-Intel: @David - it will be from spec, architectural definition to actual RTL coding itself, plus the necessary logic/functionality verification. Need to work closely with structural design team on area/timing closure as well

[ 01/04/13 7:10 PM] David: Thats good to know that...My experience closely matches with the requirements of this job.

[ 01/04/13 7:11 PM] TA-Intel: @David - good. Will definitely like to talk to you more. Please help to apply to the req for us to have your resume and be able to contact you.

[ 01/04/13 7:11 PM] Khoo: That is nice.But does arch definition only involve certain level of people?

[ 01/04/13 7:11 PM] David: I will apply online and drop you a message. It would be great if we can discuss the position in detail later.

[ 01/04/13 7:12 PM] TA-Intel: @David - sure.

[ 01/04/13 7:12 PM] David: Thanks TA...Looking forward to talking to you further.

[ 01/04/13 7:12 PM] TA-Intel: @David - You are most welcome.

[ 01/04/13 7:20 PM] Khoo: Hi TA, i will proceed to deposit my resume in the link provided and i hope we can discuss further later thanks.

[ 01/04/13 7:21 PM] Khoo: and thank you for providing the info

[ 01/04/13 7:22 PM] TA-Intel: @Khoo - Thanks

[ 01/04/13 7:22 PM] TA-Intel: @Khoo - looking fwd to talk to you

[ 01/04/13 7:22 PM] Khoo: which job ID should i apply?

[ 01/04/13 7:24 PM] Mazlina-Intel: @ Khoo - this link will take you directly to the job  
<http://www.intel.com/jobs/jobsearch/index.htm?job=702093&src=CFE-12682>

[ 01/04/13 7:28 PM] Ajosh: Hi TA good morning

[ 01/04/13 7:28 PM] yatin: Hi TA

[ 01/04/13 7:28 PM] TA-Intel: @Ajosh - Hi, Ajosh, Welcome

[ 01/04/13 7:29 PM] Ajosh: I am graduate from Lund university Sweden in MS sytem on Chip(Digital). Do you prefer graduate for this postion?

[ 01/04/13 7:29 PM] TA-Intel: @Yatin - Hi Yatin, Welcome

[ 01/04/13 7:29 PM] yatin: Thanks

[ 01/04/13 7:29 PM] yatin: I am into synthesis and timing of SoC

[ 01/04/13 7:30 PM] yatin: do you have suitable positions?

[ 01/04/13 7:30 PM] TA-Intel: @Ajosh - We are looking for both graduate and experienced folks

[ 01/04/13 7:30 PM] yatin: I have about 11+ years of experience

[ 01/04/13 7:30 PM] Mazlina-Intel: @Ajosh - the focus today is for experienced candidates but you are more than welcome to send your resume

[ 01/04/13 7:31 PM] TA-Intel: @Yatin - Hi Yatin, if you can visit the structural design booth and talk to my collague (James). He will be able to share with you more on the oppty

[ 01/04/13 7:31 PM] yatin: sure

[ 01/04/13 7:31 PM] yatin: thanks a lot

[ 01/04/13 7:31 PM] TA-Intel: @Yatin - Welcome

[ 01/04/13 7:34 PM] Ajosh: ok Thanks for the information TA and Mazlina

[ 01/04/13 7:35 PM] TA-Intel: @Ajosh - Welcome

[ 01/04/13 7:36 PM] Ajosh: Do you have any seperate appilcation link for graduate

[ 01/04/13 7:37 PM] Mazlina-Intel: @Ajosh, you can send to the same link, easier for us to retrieve your profile later :)

[ 01/04/13 7:37 PM] Mazlina-Intel: <http://www.intel.com/jobs/jobsearch/index.htm?job=702093&src=CFE-12682>

[ 01/04/13 7:38 PM] Ajosh: Thanks Mazlina

[ 01/04/13 7:38 PM] Ajosh: thank you very much

[ 01/04/13 7:38 PM] Mazlina-Intel: My pleasure

[ 01/04/13 7:53 PM] Prakash: @TA Poh: Hi I am Prakash

[ 01/04/13 7:53 PM] Prakash: @TA Poh: I am interested in Design for Test opportunities in your group

[ 01/04/13 7:54 PM] TA-Intel: @Prakash - Hi Prakash, Welcome

[ 01/04/13 7:54 PM] TA-Intel: @Prakash - are u currently working in DFX space?

[ 01/04/13 7:55 PM] Prakash: @TA-Intel: Thanks. Yes, I have about 7 years of experience in DFT

[ 01/04/13 7:55 PM] Prakash: @TA-Intel: I have worked with both IP level and for the last few years on SOC level DFT RTL, Scan, ATPG, Memory test, etc

[ 01/04/13 7:56 PM] Prakash: @TA-Intel: I also have experience with TestKompress, Tetramax and Encounter Test, having worked with all 3 of the tools over the last few years

[ 01/04/13 7:56 PM] TA-Intel: @Prakash - Great. We have SOC team that work on DFT design also

[ 01/04/13 7:57 PM] TA-Intel: @Prakash - is it possible for you to submit your resume via applying to the logic design job opening?

[ 01/04/13 7:57 PM] Prakash: @TA-Intel: That is good to know, do let me know if there are opportunities in the team right now. And if you could shed some light on job description

[ 01/04/13 7:57 PM] Prakash: @TA-Intel: Certainly, I can send my resume via the logic design opening

[ 01/04/13 7:58 PM] TA-Intel: @Prakash - DFX team work on design/integrating DFX IP (such as TAP network, MBIST, internal debug bus ) to the SOC blocks and perform the necessary logic verification. They also work closely with the post silicon team on testing/bring up these DFX mode in real silicon as well

[ 01/04/13 7:59 PM] TA-Intel: @Prakash - we are continuously looking for senior persons to strengthen our DFX design/validation team

[ 01/04/13 7:59 PM] Prakash: @TA-Intel: Thanks for the description, I have experience in post silicon debug for the last few projects as well

[ 01/04/13 8:00 PM] TA-Intel: @Prakash - we have 1 more minute to go for this event. Please help to apply to the job opening and i will contact you asap

[ 01/04/13 8:01 PM] Prakash: @TA-Intel: Thanks, I am creating a new profile and will apply to the job opening

[ 01/04/13 8:01 PM] TA-Intel: @Prakash - Thx. Looking fwd to talk to you.

[ 01/04/13 8:01 PM] Prakash: @TA-Intel: Thanks, same here.

[ 01/04/13 8:02 PM] TA-Intel: @Prakash - Welcome

[ 01/04/13 8:02 PM] nakkeraneeran.k: I heard you validate micro servers

[ 01/04/13 8:03 PM] nakkeraneeran.k: what are activities of those validation task

[ 01/04/13 8:03 PM] nakkeraneeran.k: typical work day role

[ 01/04/13 8:03 PM] TA-Intel: @Nakeran - Yes, We do that also

[ 01/04/13 8:04 PM] TA-Intel: @Nakkeran - since the event is closing , pls help to apply to our job so that i can contact u to share more

[ 01/04/13 8:04 PM] nakkeraneeran.k: Is it post silicon system validation ? sure

[ 01/04/13 8:04 PM] nakkeraneeran.k: thanks :)

[ 01/04/13 8:04 PM] TA-Intel: Thanks