Challenges and Innovations in Nano-CMOS Transistor Scaling

Tahir Ghani

Intel Fellow

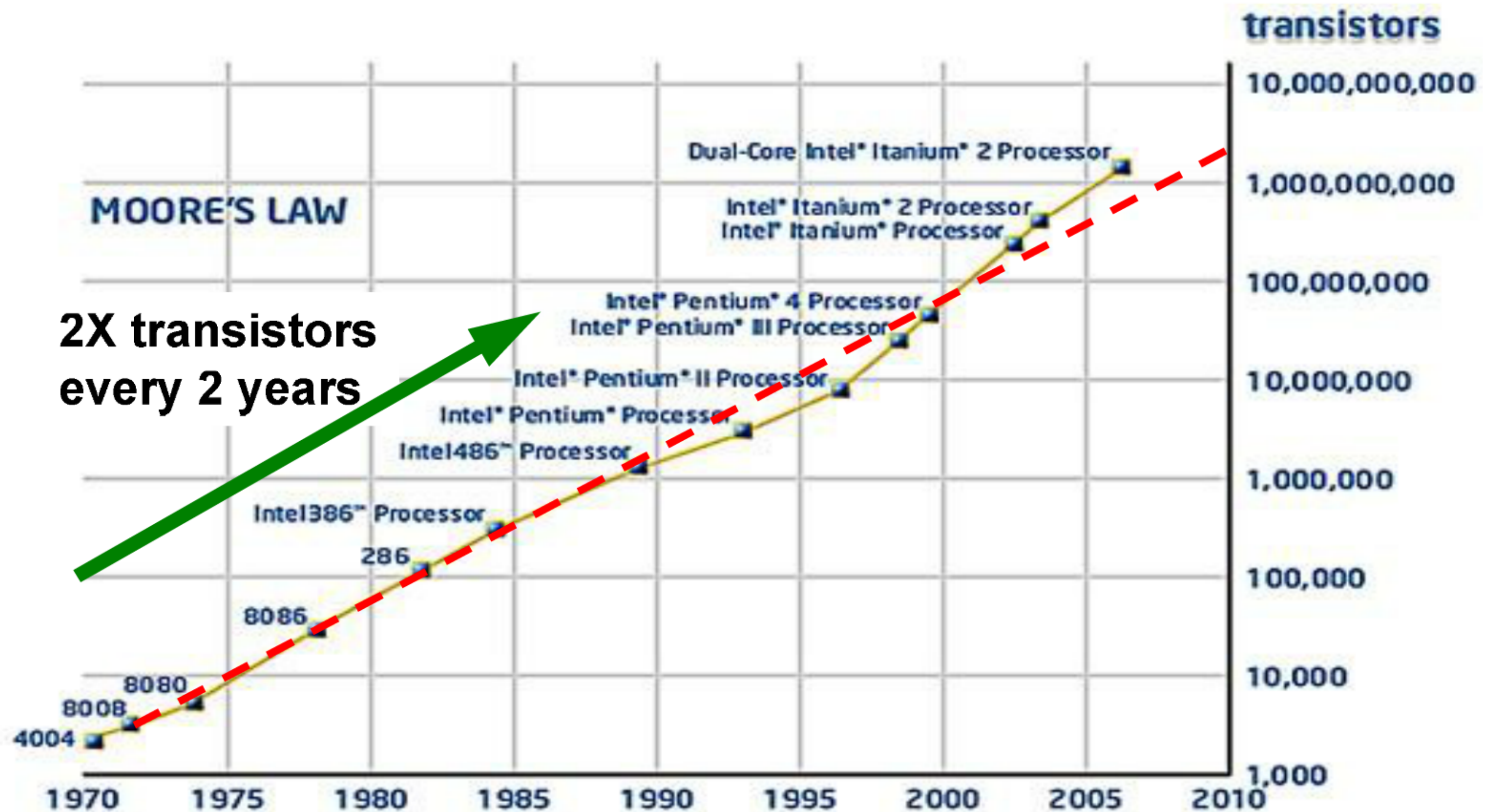
Logic Technology Development

October, 2009

Outline

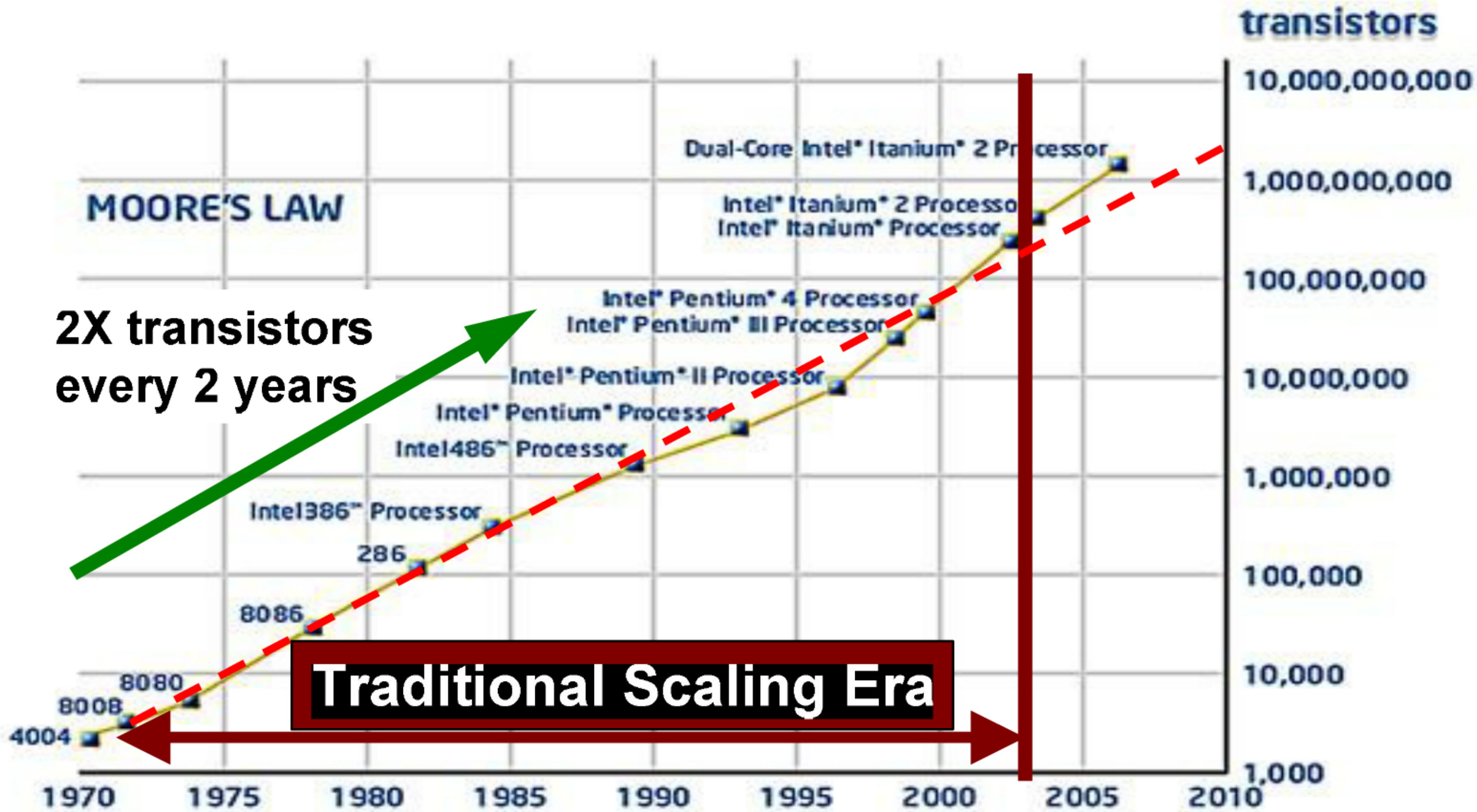
- **Traditional-Scaling**
  - Traditional Scaling Limiters, Device Implications
  - Intel's Response
- **Post "Traditional-Scaling" Innovations**
  - Mobility Booster: Uniaxial Strain
  - Poly Depletion Elimination: Metal Gate
  - Gate Leakage Reduction: HiK
- **Future Challenges and Options**
  - Power Limitation
  - Potential New Transistor Structures and Materials

40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors



Transistor Count has Doubled Every Two Years

40+ Years of Moore's Law at INTEL: From Few to Billions of Transistors

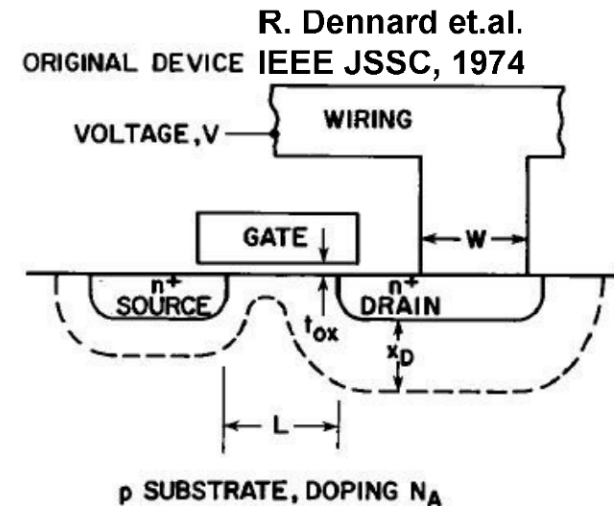


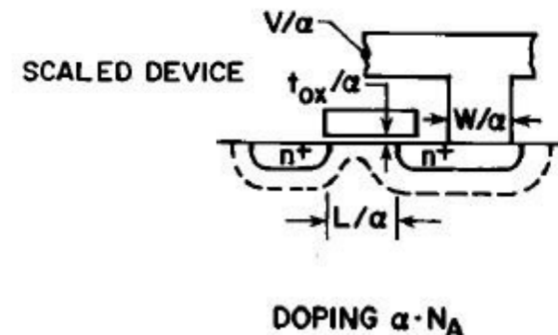
END OF TRADITIONAL SCALING ERA ~ 2003
Lasted ~40 YEARS

Top "Traditional-Scaling" Enablers

- Gate Oxide Thickness Scaling
  - Key enabler for Lgate scaling
- Junction Scaling
  - Another enabler for Lgate scaling
  - Improved abruptness (R_{EXT} reduction)
- Vcc Scaling
  - Reduce X_{DEP} (improve SCE)
  - However, did not follow const E field

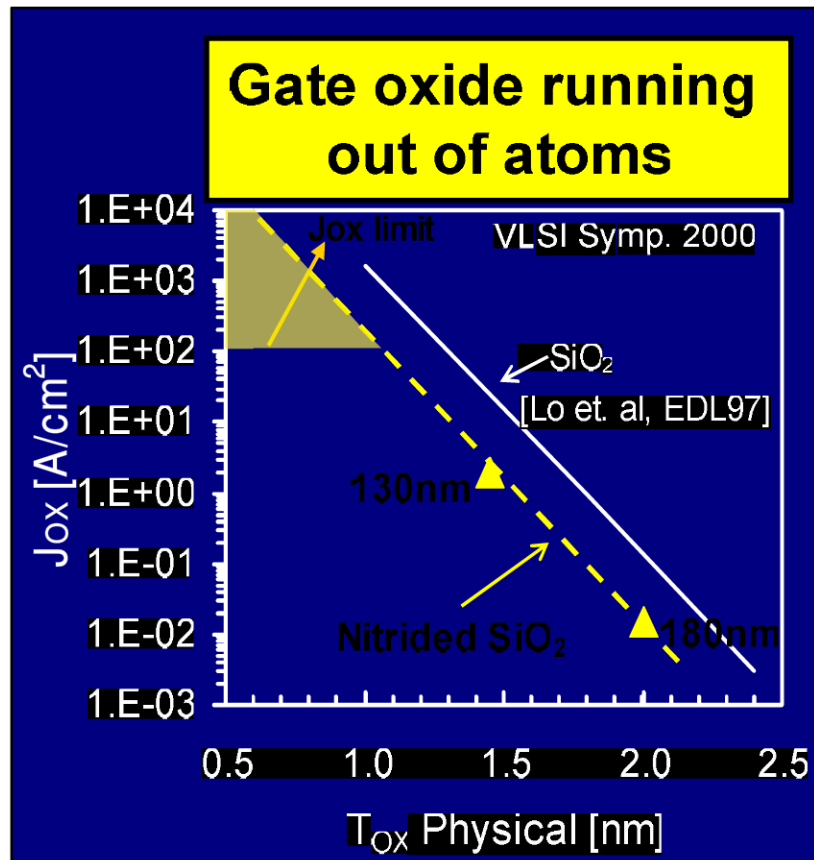
R. Dennard et.al.
IEEE JSSC, 1974

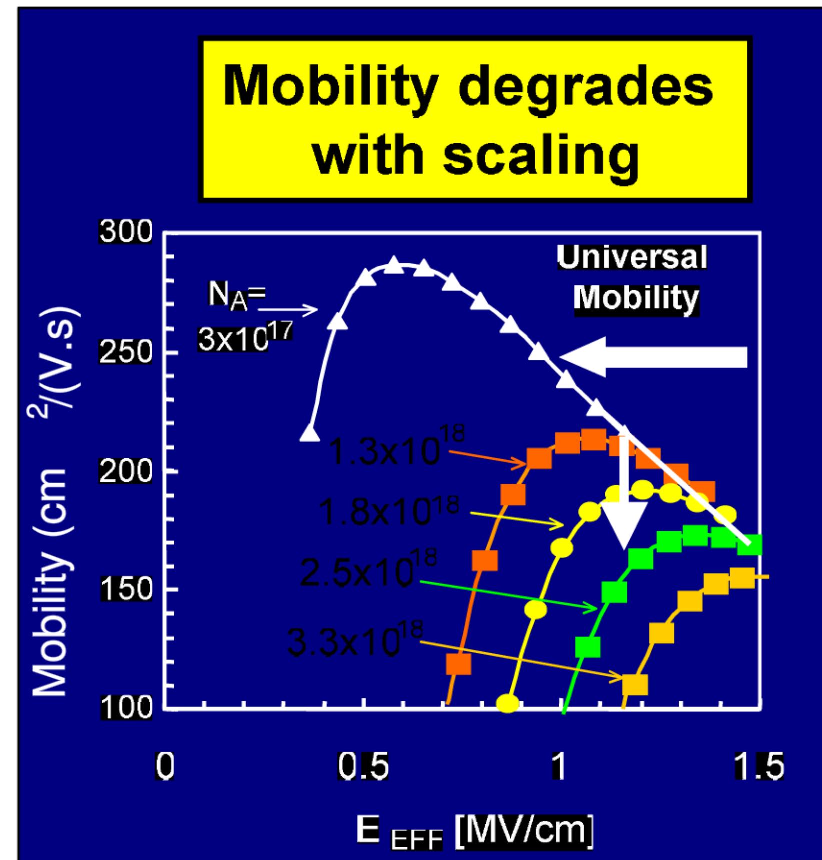




1990's: Golden Era of Scaling
Vcc, Tox & Lg scaling & increasing Idsat

Year 2000: INTEL 90nm CMOS Pathfinding
End of "Traditional-Scaling" Era



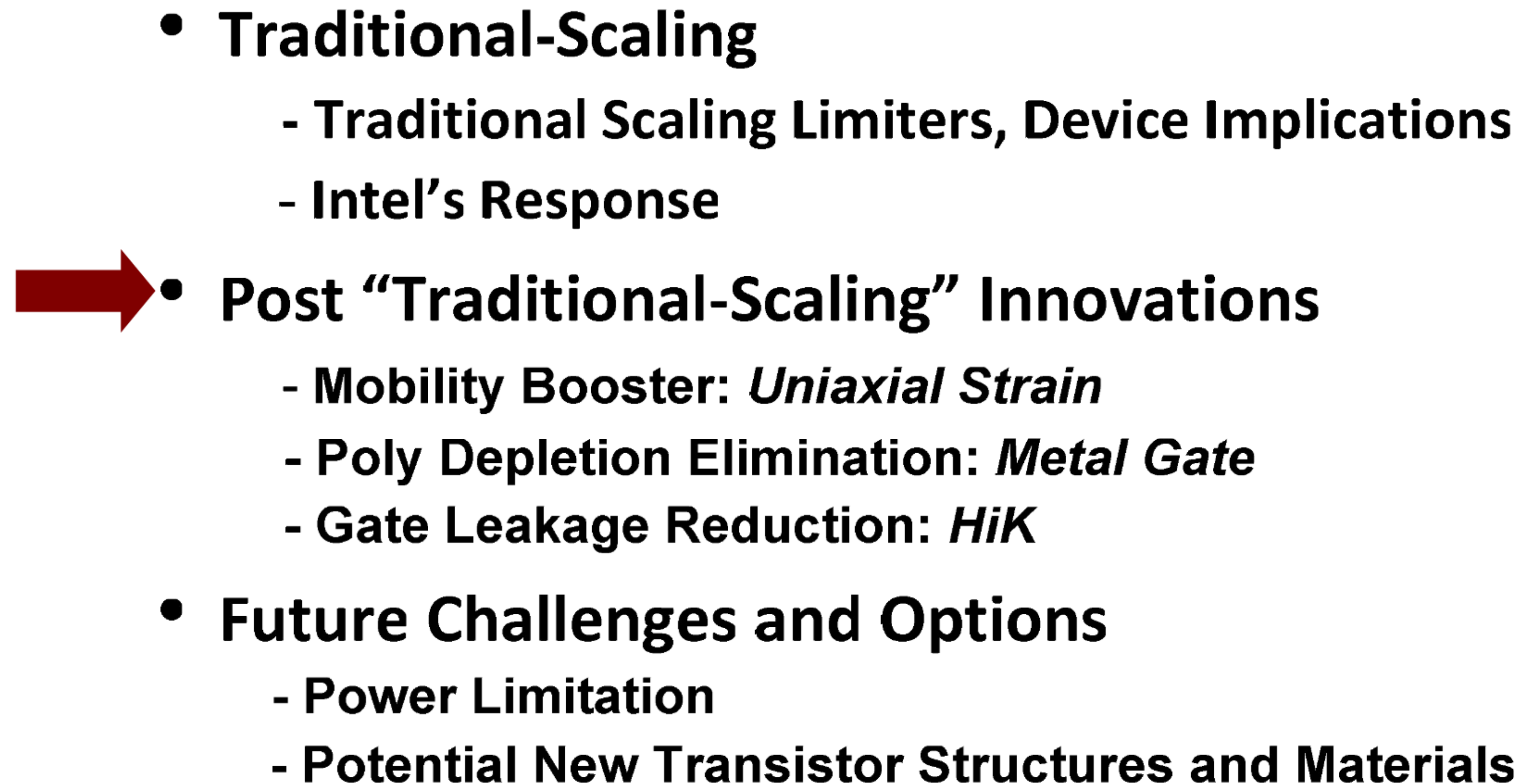


- Gate Oxide Leakage direct tunneling limited

- Universal Mobility Model
- Ionized impurity scattering

T. Ghani et. al. VLSI Symposium 2000

Outline

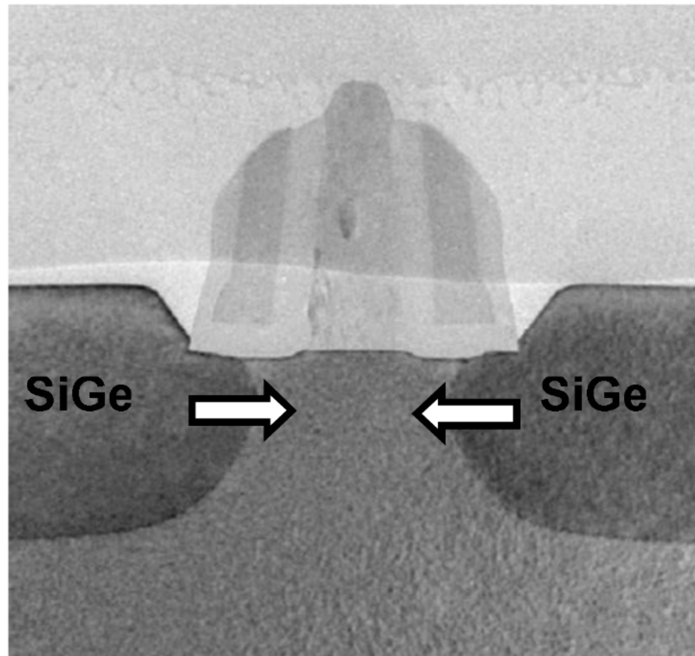


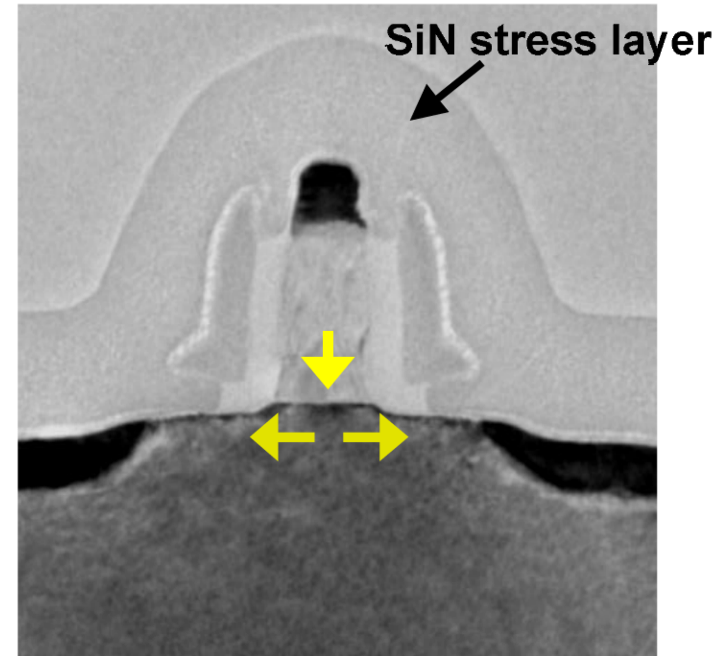
Innovations Pioneered by Intel to Overcome "Traditional-Scaling" Limiters

- Mobility enhancement through uniaxial strained silicon technology innovation introduced at 90nm node
  - **Epitaxial SiGe S/D**
  - **SiN Capping Layers**
- **HiK gate insulator** introduced at 45nm CMOS node to reduce gate leakage
- **Metal Gate** introduced at 45nm CMOS node to eliminate poly depletion

Uniaxial Strain Silicon Transistors
Intel: IEDM 2003

PMOS T. Ghani et. al. IEDM, 2003 **NMOS**

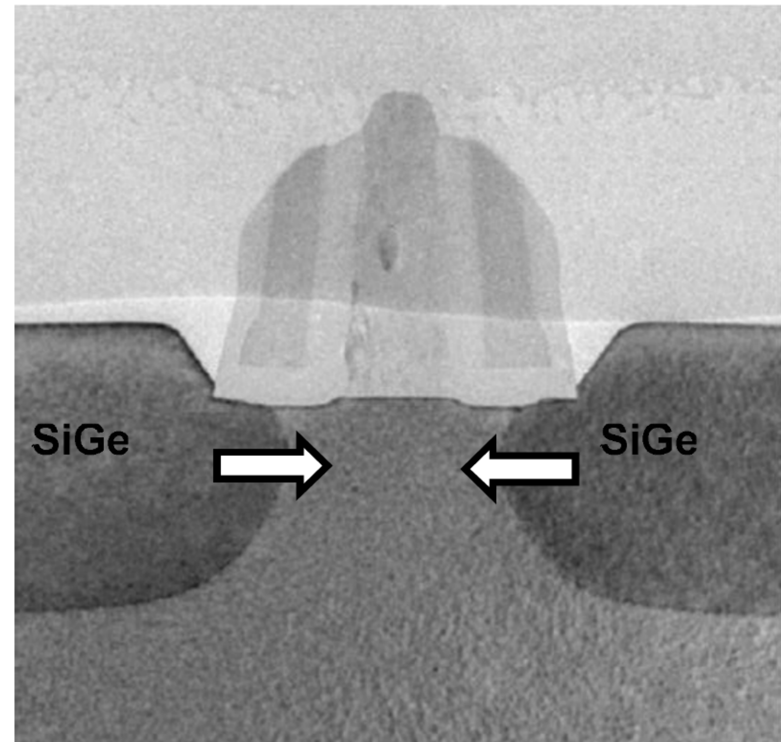




These transistor structures introduced first at Intel's 90nm CMOS node. These structures have now become industry standard for strain implementation

Strained SiGe S/D PMOS Transistor

- SiGe film embedded into source/drain
- SiGe film deposited by selective epitaxy
- Induces large uniaxial compressive strain in channel
- This strain leads to dramatic hole mobility enhancement

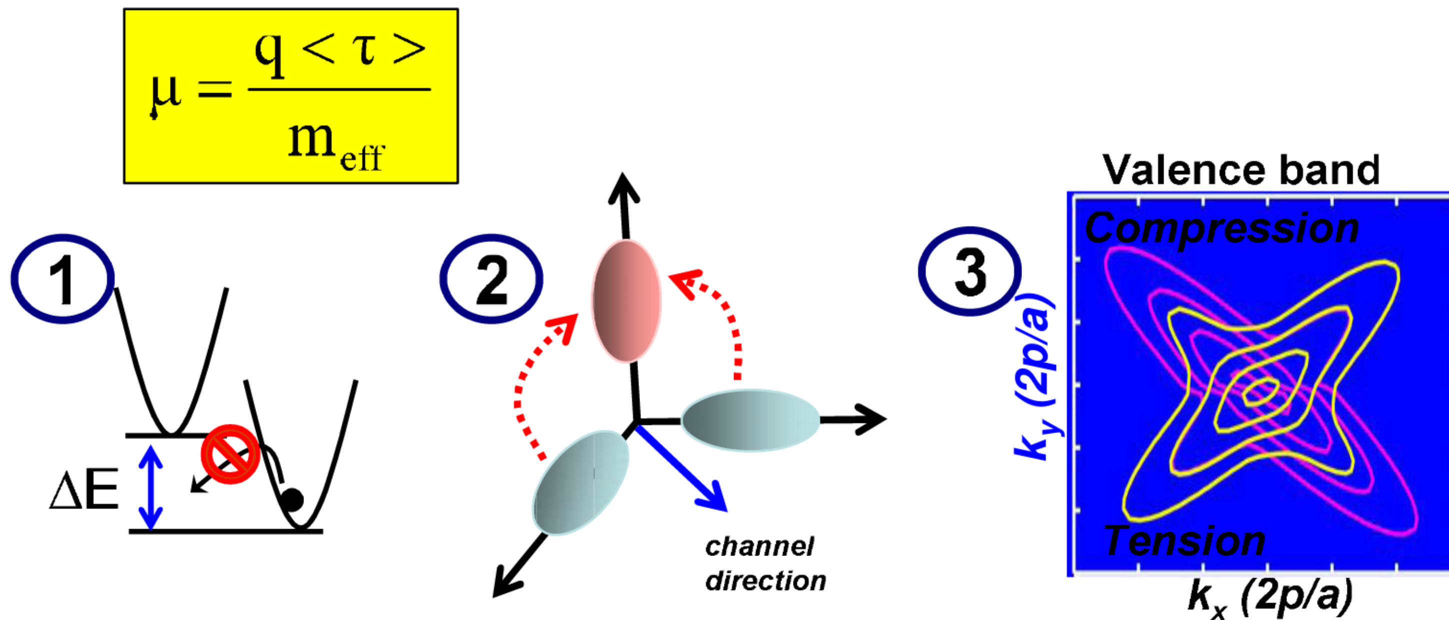


How Strain Impacts Mobility?

Strain impacts mobility through:

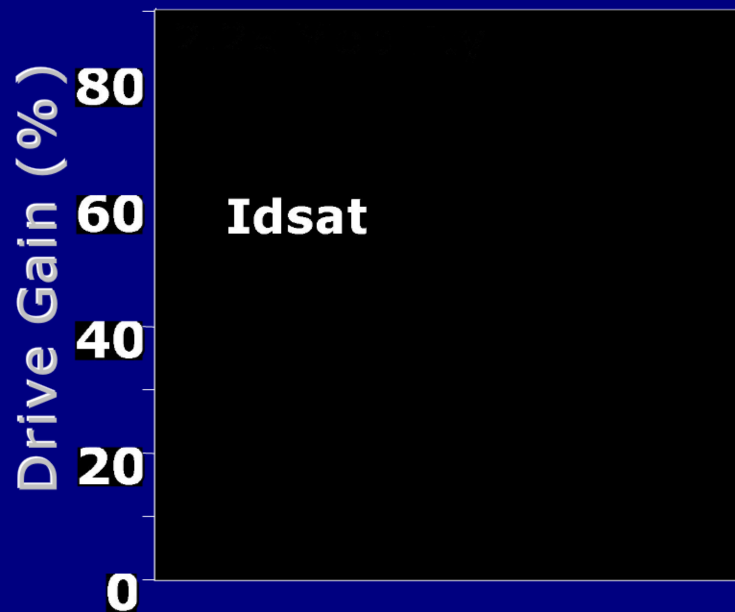
- **Energy/subband spacing which affects scattering (τ)** ①
- **Valley repopulation which changes transport mass (m_{eff})** ②
- **Band warpage which changes transport mass (m_{eff})** ③

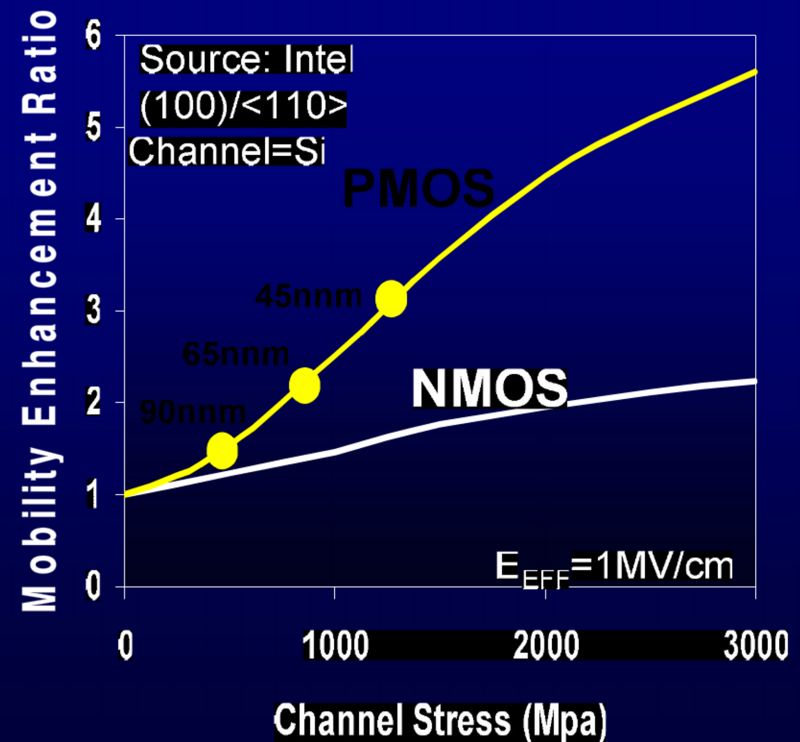
$$\mu = \frac{q < \tau >}{m_{eff}}$$



M. Stettler, 2006 SINANO Device Modeling School

Performance Gains with Uniaxial Strain



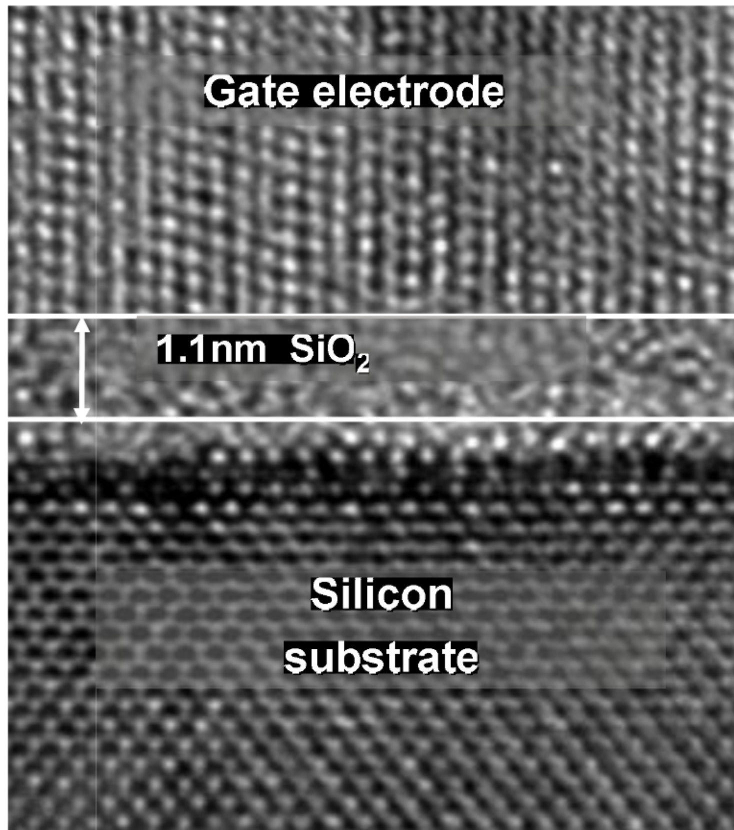


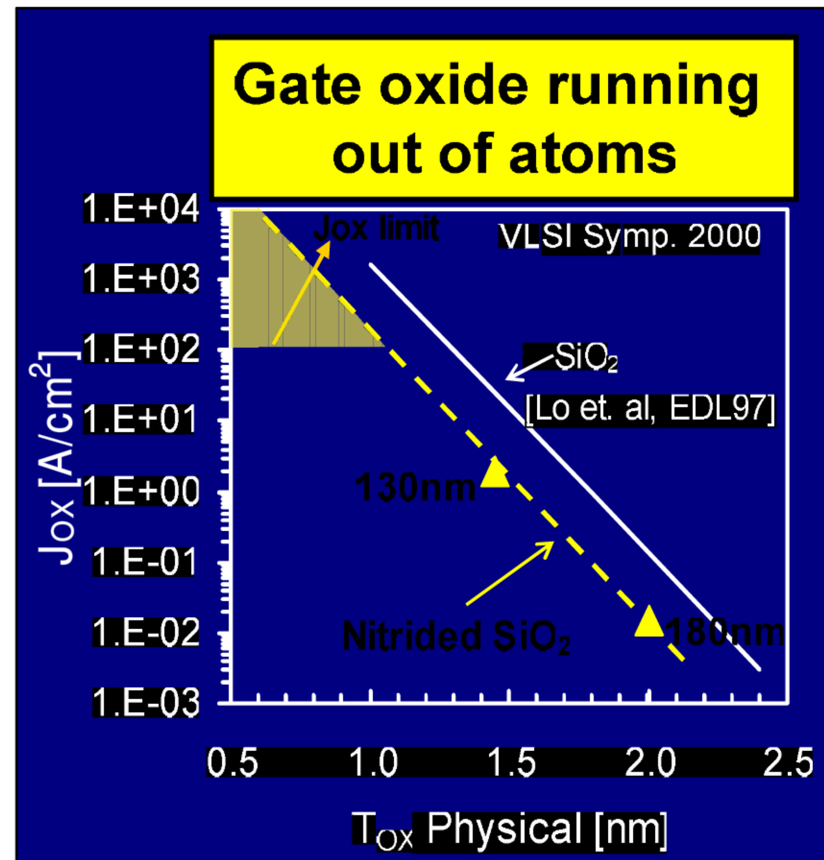
Significant headroom left to increase PMOS mobility in future (> 5x)

Innovations Pioneered by Intel to Overcome Traditional Scaling Limiters

- Mobility enhancement through uniaxial strained silicon technology innovation introduced at 90nm node
    - **- Epitaxial SiGe S/D**
    - **- SiN Capping Layers**
- **HiK gate insulator** introduced at 45nm CMOS node to reduce gate leakage
- **Metal Gate** introduced at 45nm CMOS node to eliminate poly depletion

Year 2003: INTEL 65nm CMOS Pathfinding
Gate Oxide Runs out of steam





Intel 65nm production: 2005
- Gate Oxide only 3-4 atomic layers thick.
- Gate depletion also a limiter

- **Gate Oxide Leakage direct tunneling limited**

T. Ghani .et. al. VLSI Symp. 2000

High-k + Metal Gate Benefits

- **High-k gate dielectric**
  - Reduced gate leakage
  - T_{OX}(e) scaling
- **Metal gates**
  - Eliminate polysilicon depletion
  - Resolves V_T pinning and poor mobility for high-k dielectrics

High-k + Metal Gate Challenges

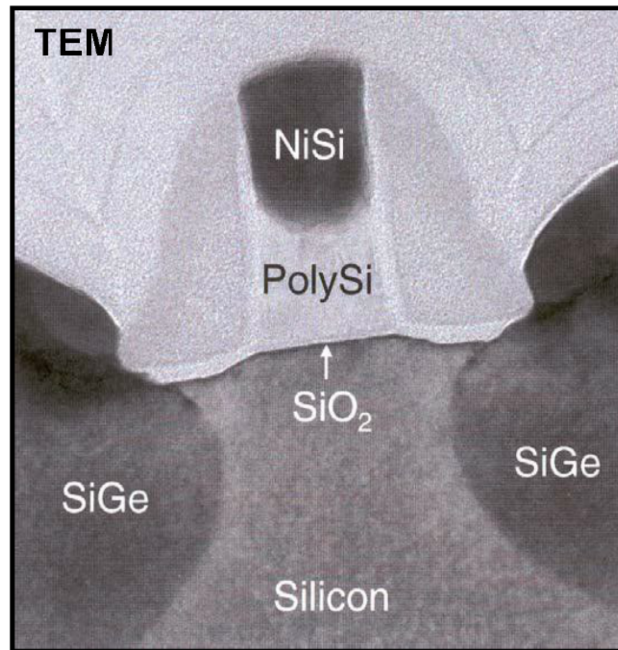
- **High-k gate dielectric**
  - Poor mobility
  - Poor reliability
- **Metal gates**
  - Dual band edge work functions
  - Thermal stability
  - Integration scheme

Transistor Process Flow

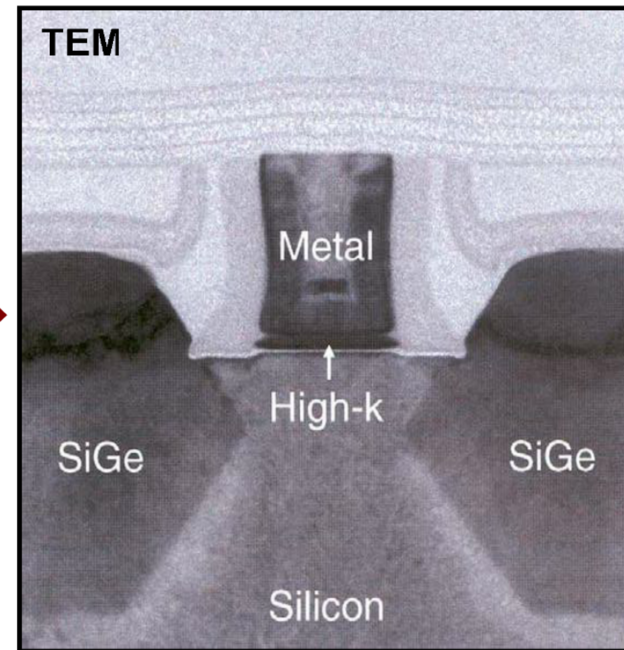
- **Key considerations**
  - Integrate hafnium-based high-k dielectric, dual metal gate electrodes, strained silicon
  - Thermal stability of metal gate electrodes
- **High-k First, Metal Gate Last**
  - Metal gate deposition after high temperature anneals
  - Integrated with strained silicon process

45nm High-k + Metal Gate Transistors

65 nm Transistor



45 nm HK + MG



Hafnium-based high-k + metal gate transistors are the biggest advancement in transistor technology since the late 1960s

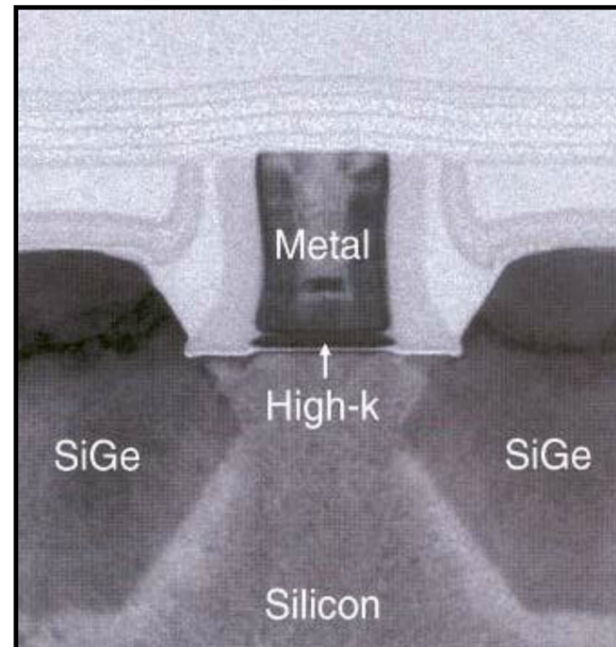
45 nm High-k + Metal Gate Transistors

Benefits compared to 65nm node

>25x lower gate oxide leakage

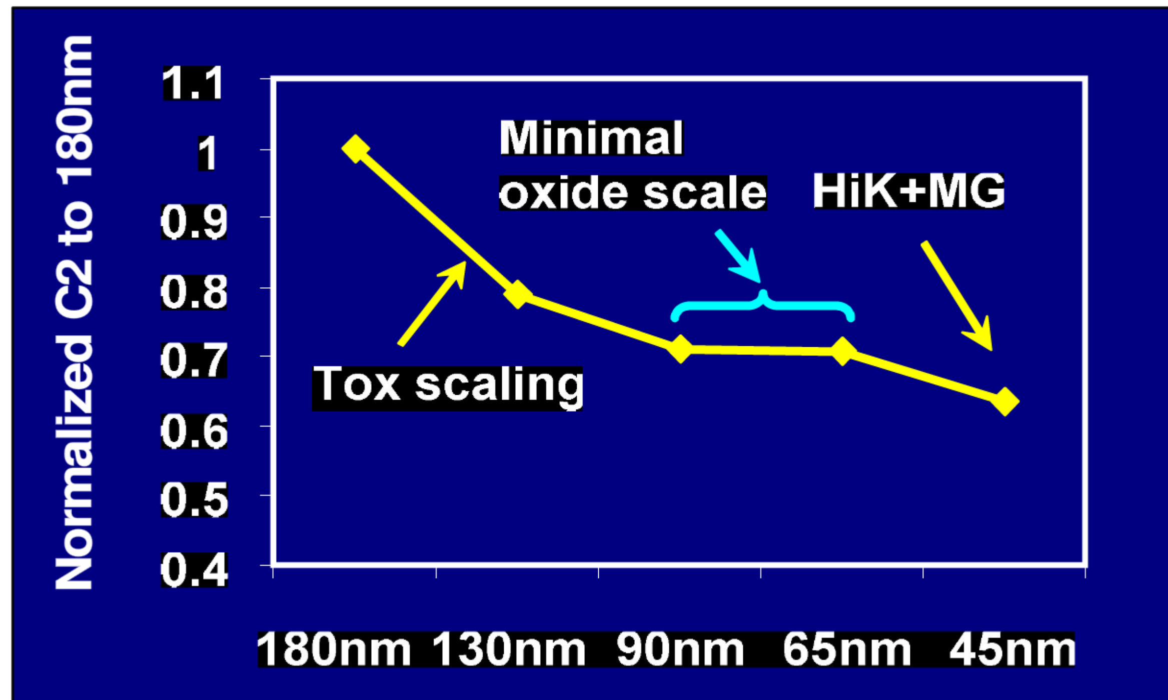
>30% lower switching power

~30% higher drive current, or
>5x lower source-drain leakage



Intel is only company with high-k + metal gate transistors in production, starting in Nov. '07

Scaling of Vt Variation

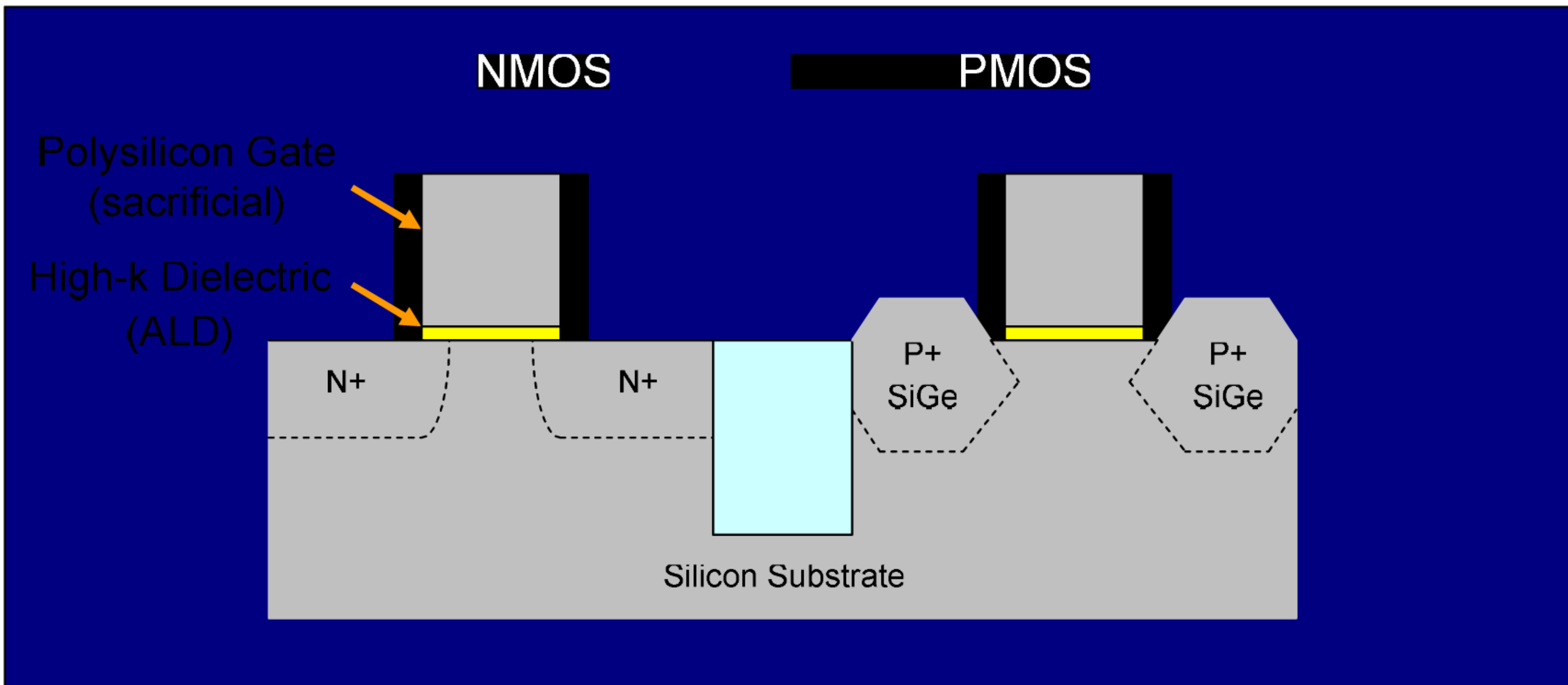


$$\sigma V_{Tran} = \left(\frac{\sqrt[4]{4q^3 \varepsilon_{si} \phi_B}}{2} \right) \cdot \frac{T_{ox}}{\varepsilon_{ox}} \cdot \left(\frac{\sqrt[4]{N}}{\sqrt{Leff \cdot Zeff}} \right) = \frac{1}{\sqrt{2}} \left(\frac{c_2}{\sqrt{Leff \cdot Zeff}} \right) \quad (1)$$

HK+MG reduces random Vt variation

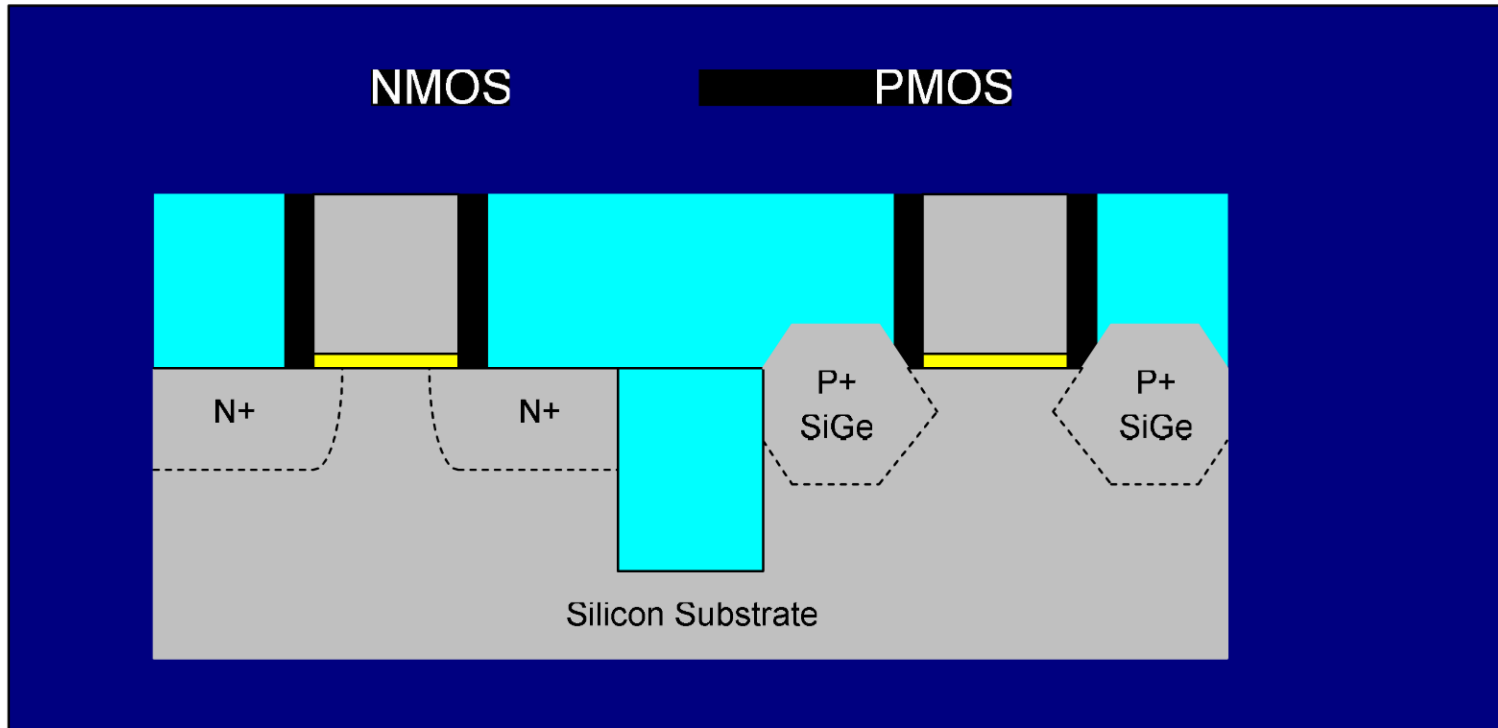
Critical to SRAM Vmin

Replacement Metal Gate Flow



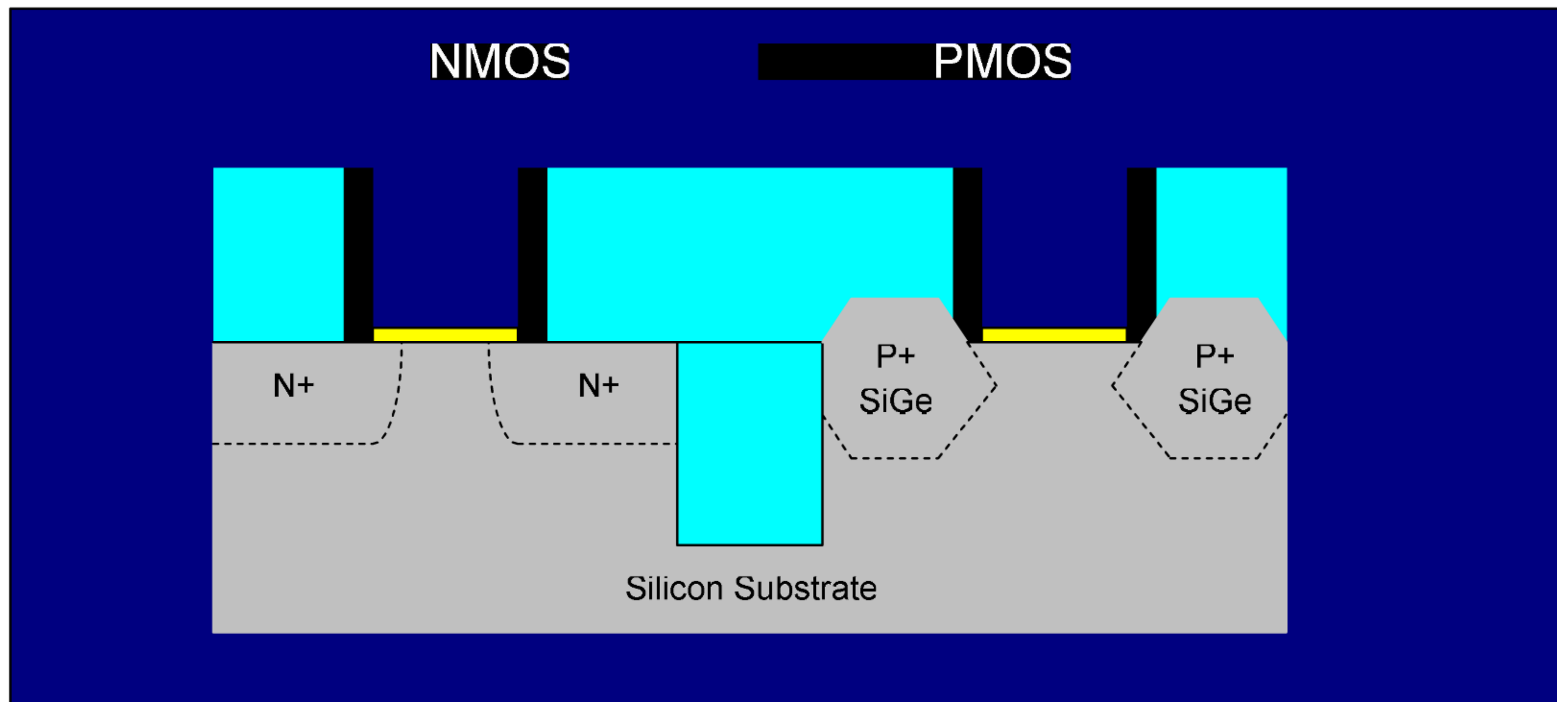
Standard transistor process through source-drain formation, but including atomic layer deposition high-k dielectric

Replacement Metal Gate Flow



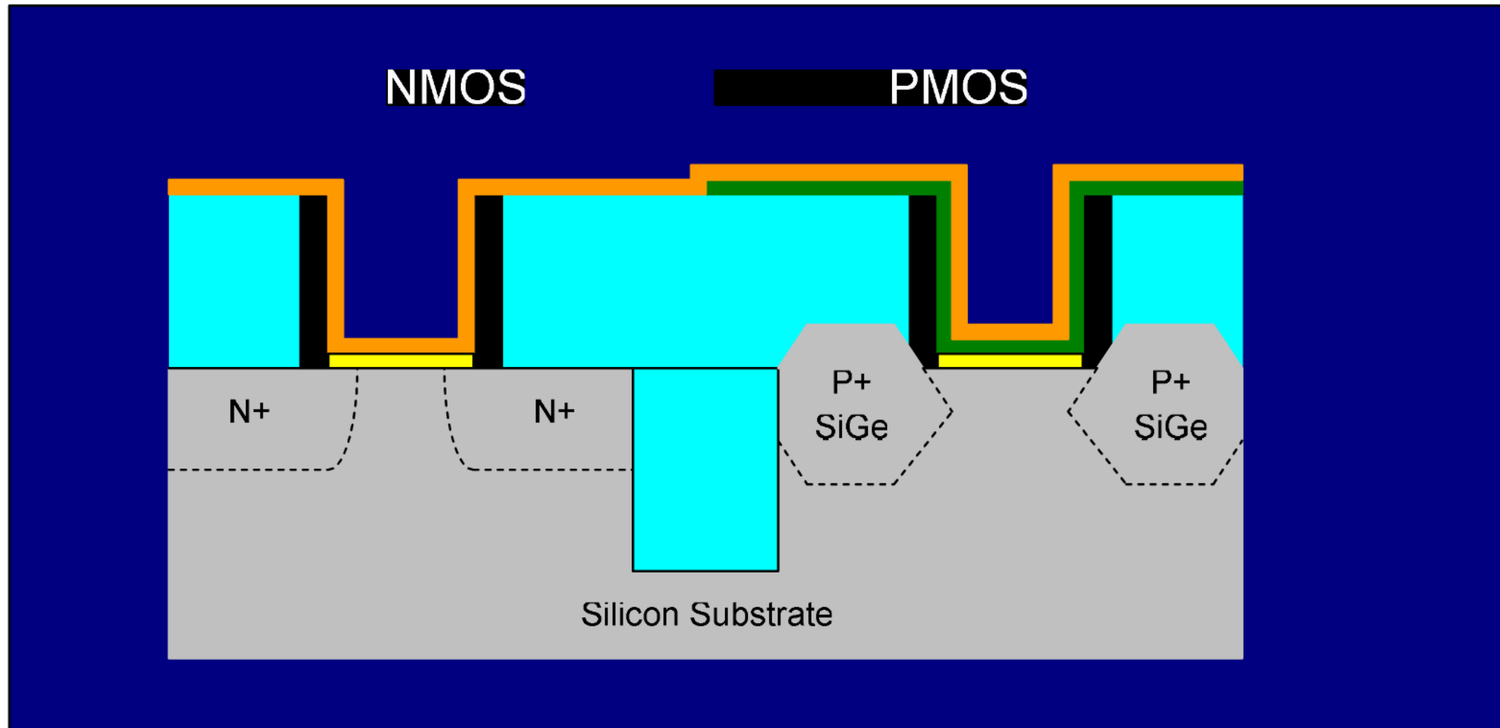
Deposit and planarize oxide layer

Replacement Metal Gate Flow



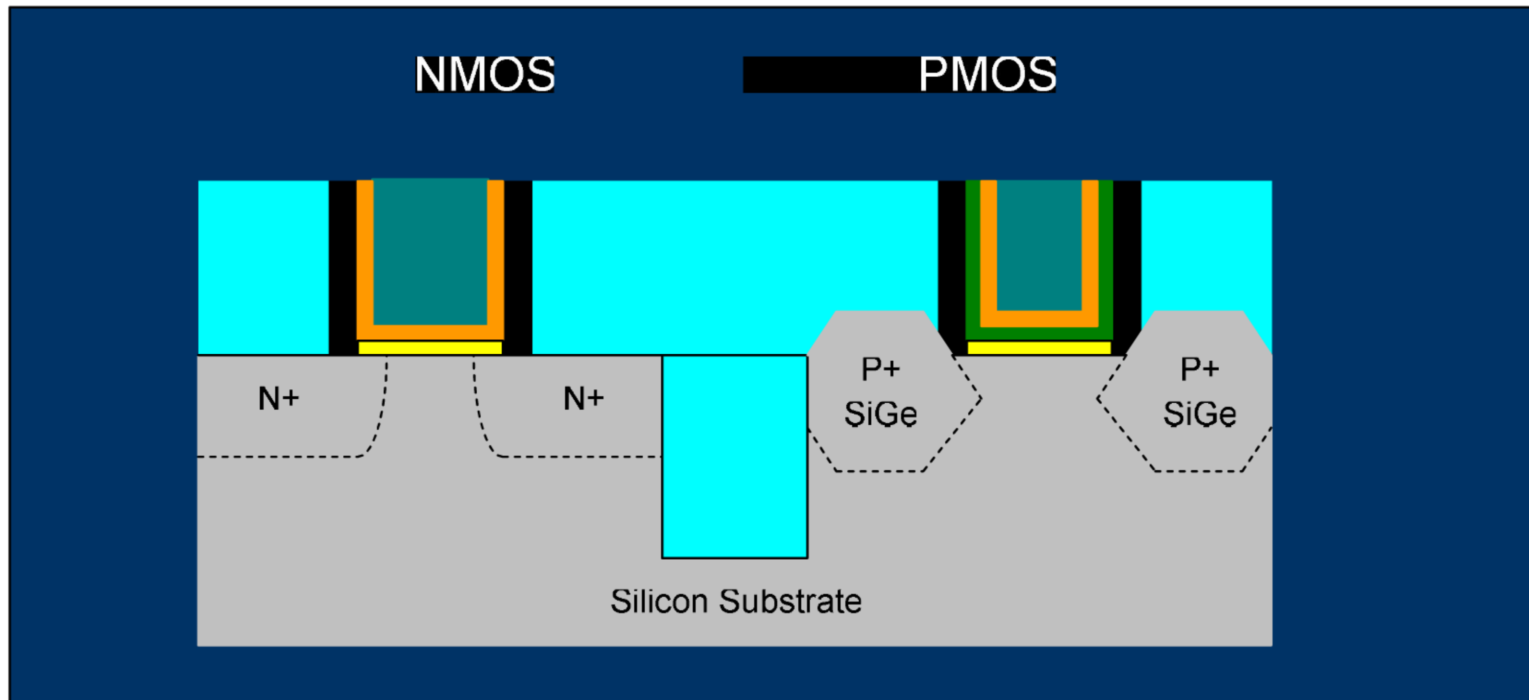
Etch out sacrificial polysilicon gate

Replacement Metal Gate Flow



Deposit separate NMOS and PMOS WF metal layers

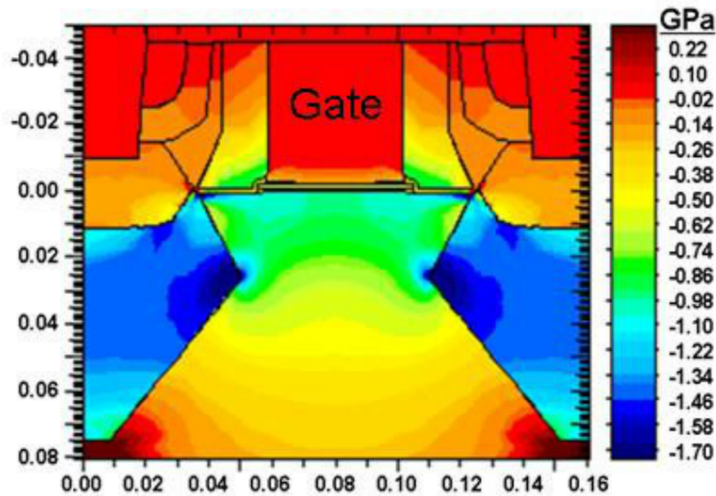
Replacement Metal Gate Flow



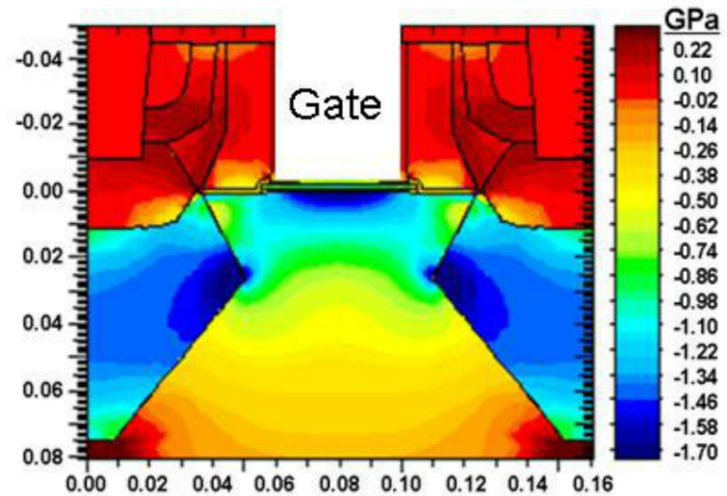
Deposit Al fill metal, planarize surface

RMG PMOS Strain Benefit

Before gate removal



After gate removal



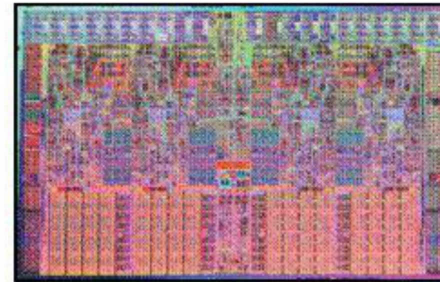
RMG process provides significant additional PMOS performance gain by increasing channel strain

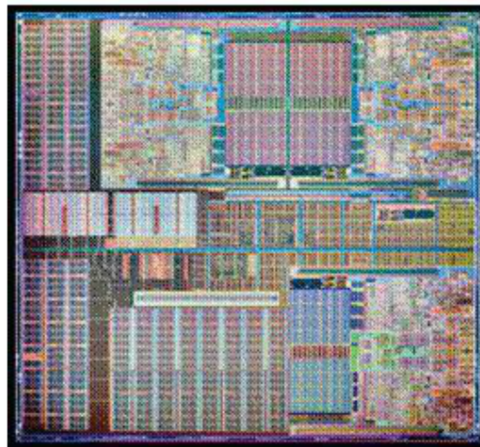
45 nm Microprocessor Products

Single Core

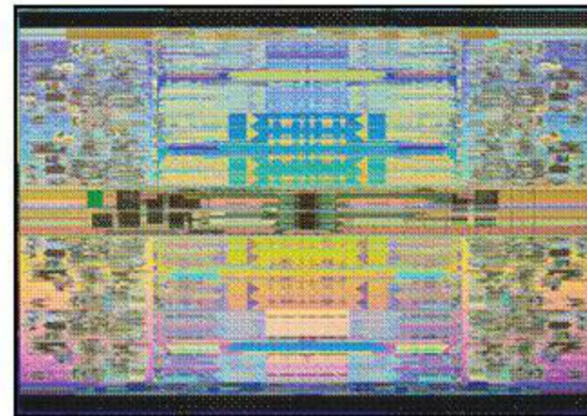
Dual Core

Quad Core





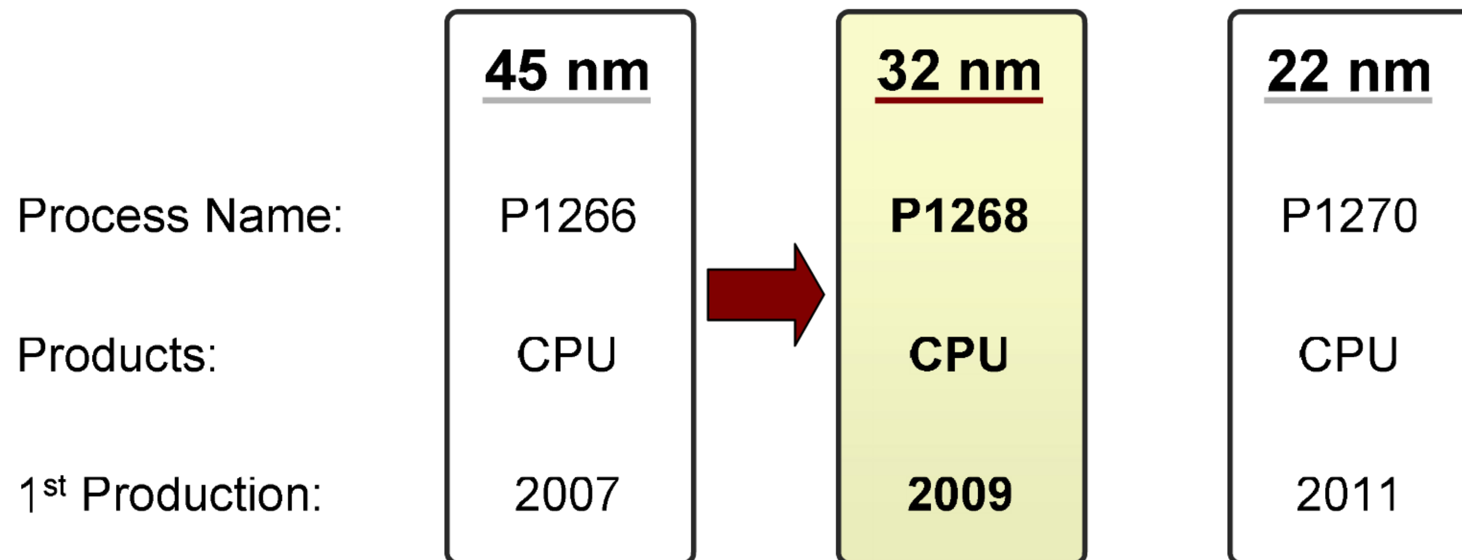
6 Core



8 Core

>200 million 45 nm CPUs shipped to date

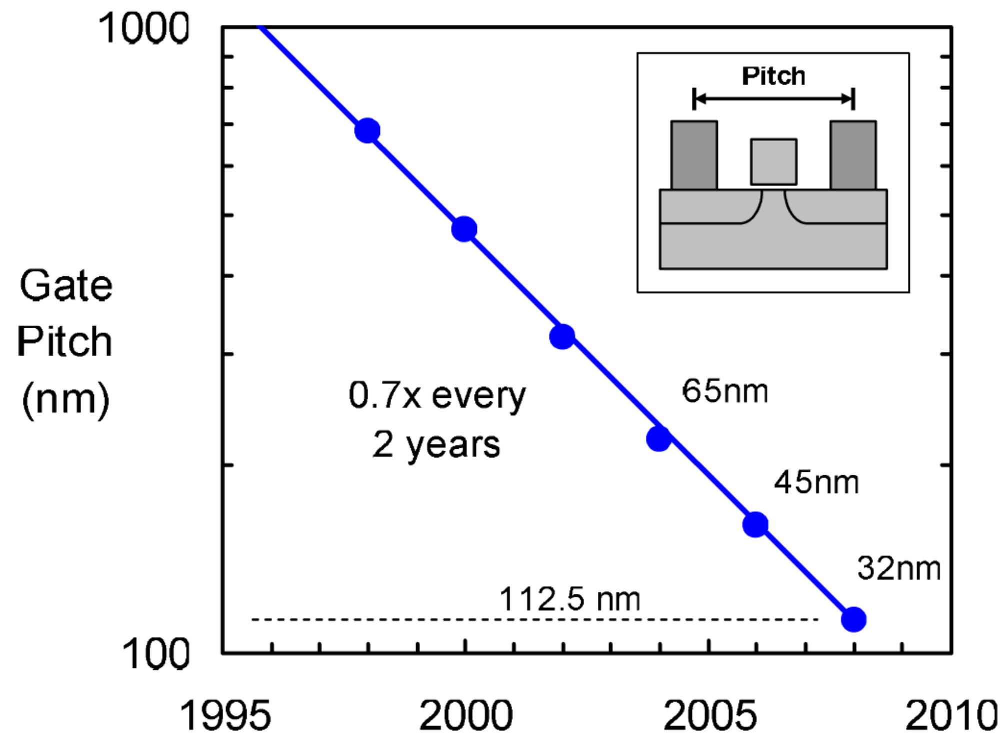
Intel Logic Technology Roadmap



	45 nm	32 nm	22 nm
Process Name:	P1266	**P1268**	P1270
Products:	CPU	**CPU**	CPU
1st Production:	2007	**2009**	2011

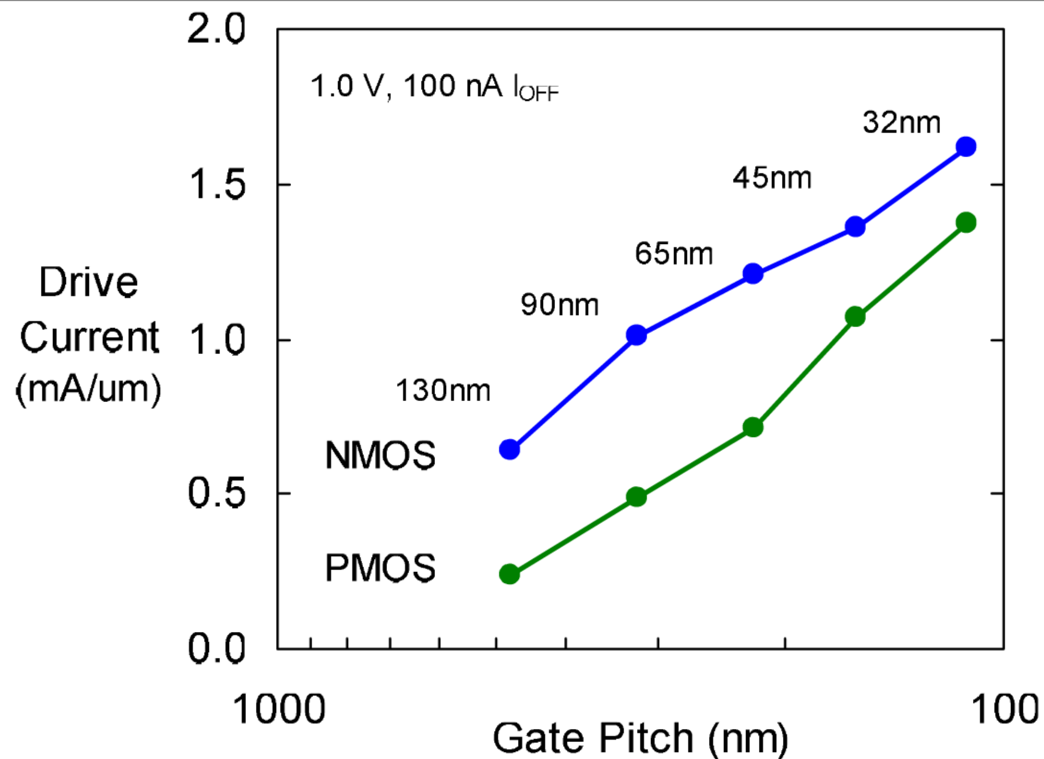
Intel 32nm: 2nd generation high-k + metal gate transistors

Transistor Density



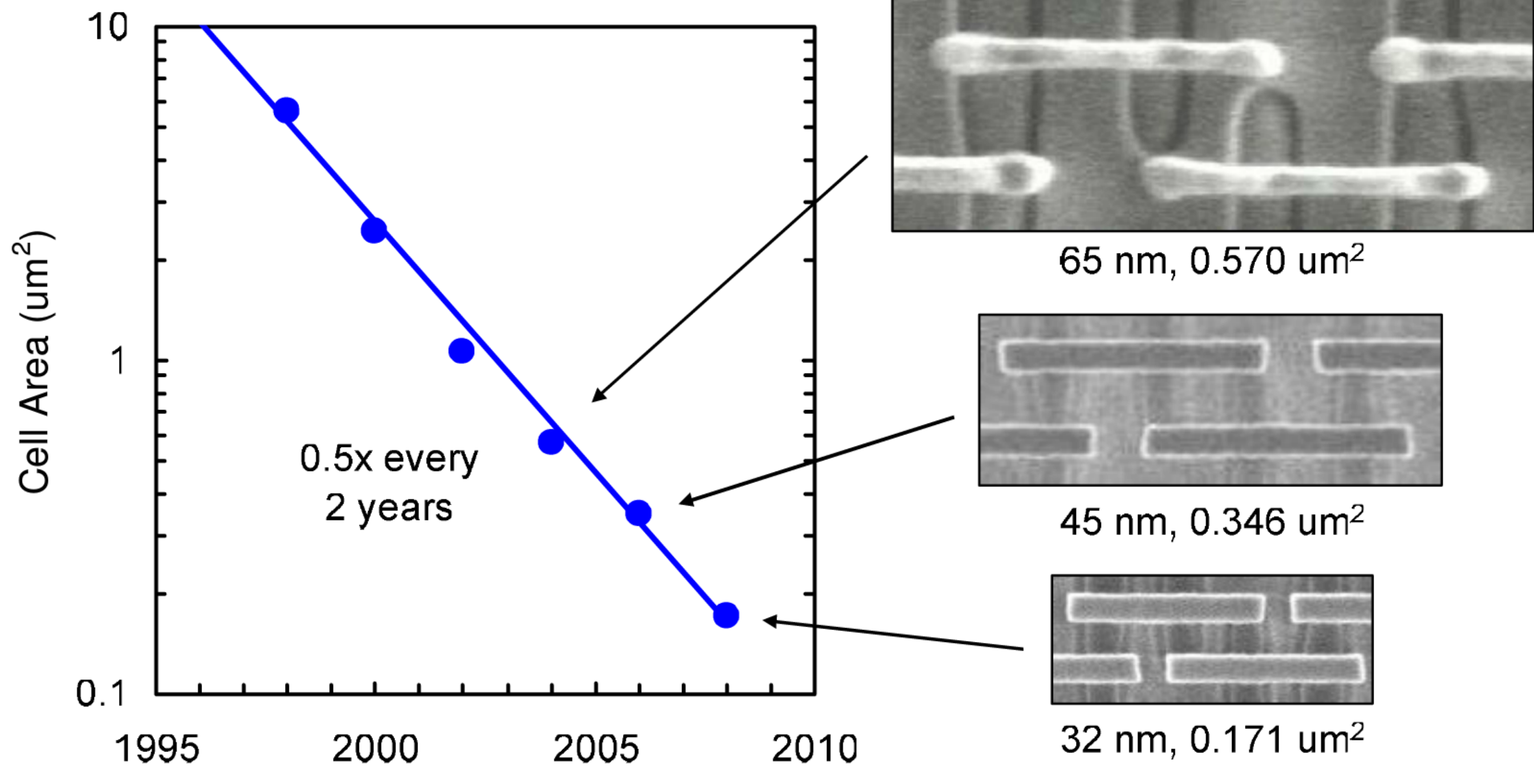
Intel 32 nm transistors provide the tightest gate pitch of any reported 32 nm or 28 nm technology

Transistor Performance



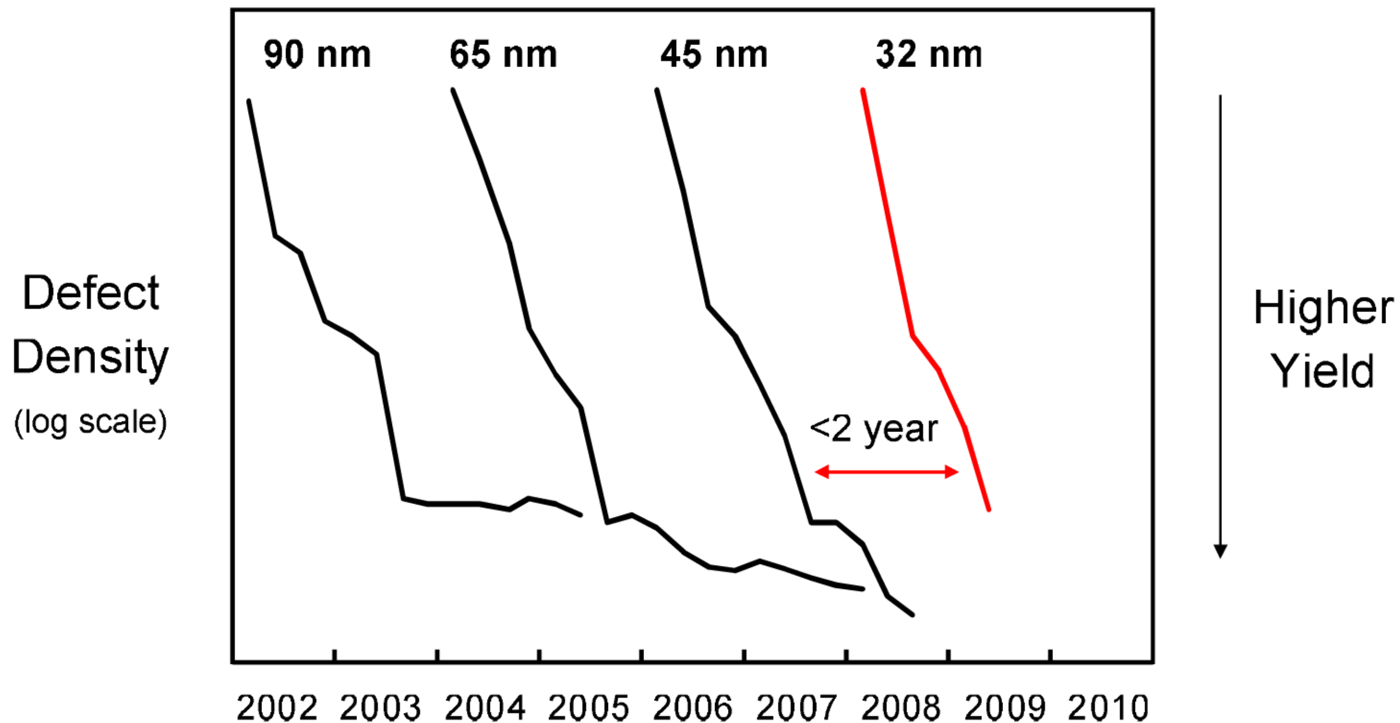
Intel 32 nm transistors provide the highest drive currents of any reported 32 nm or 28 nm technology

SRAM Cell Size Scaling



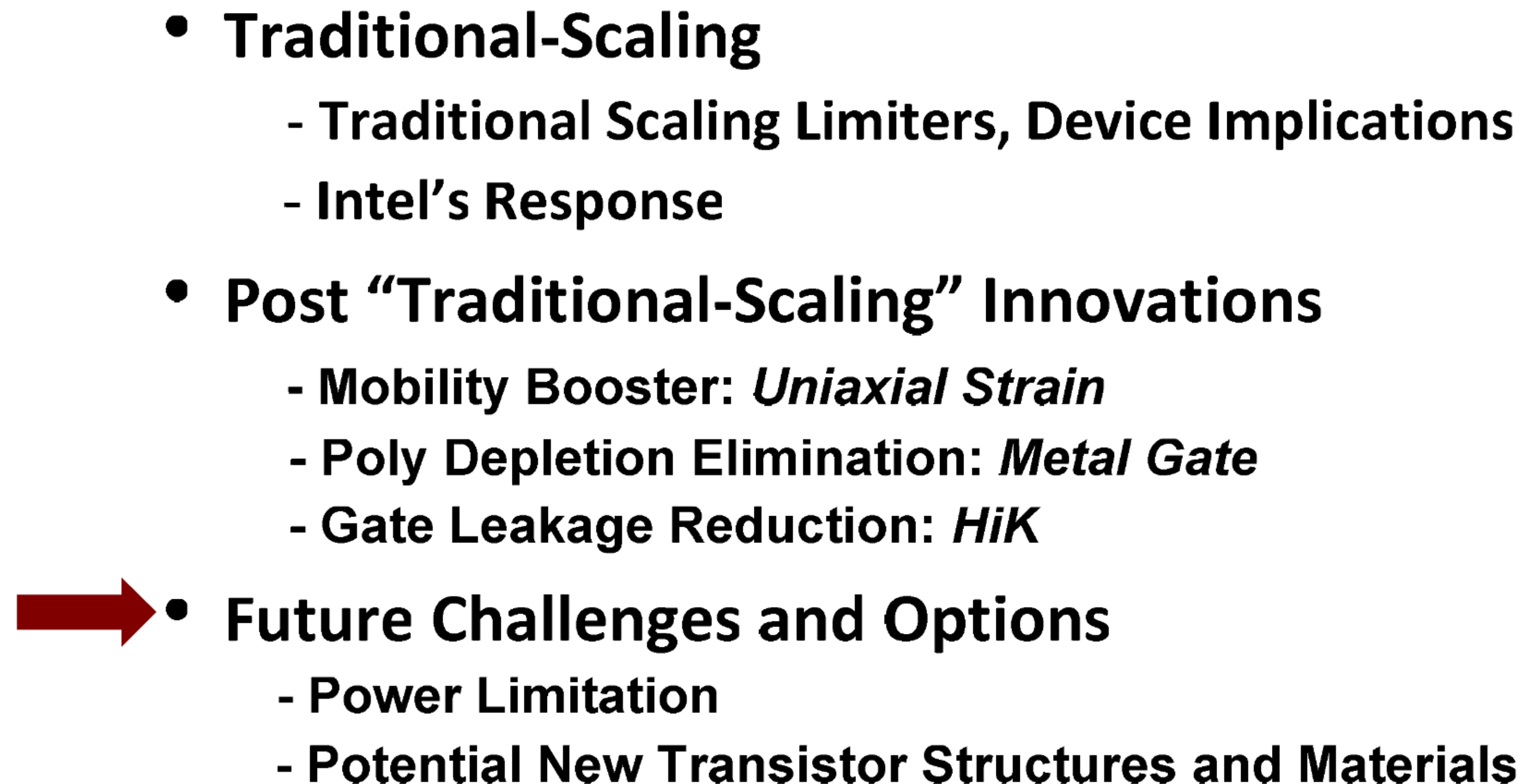
Transistor density continues to double every 2 years

32 nm Defect Density Trend

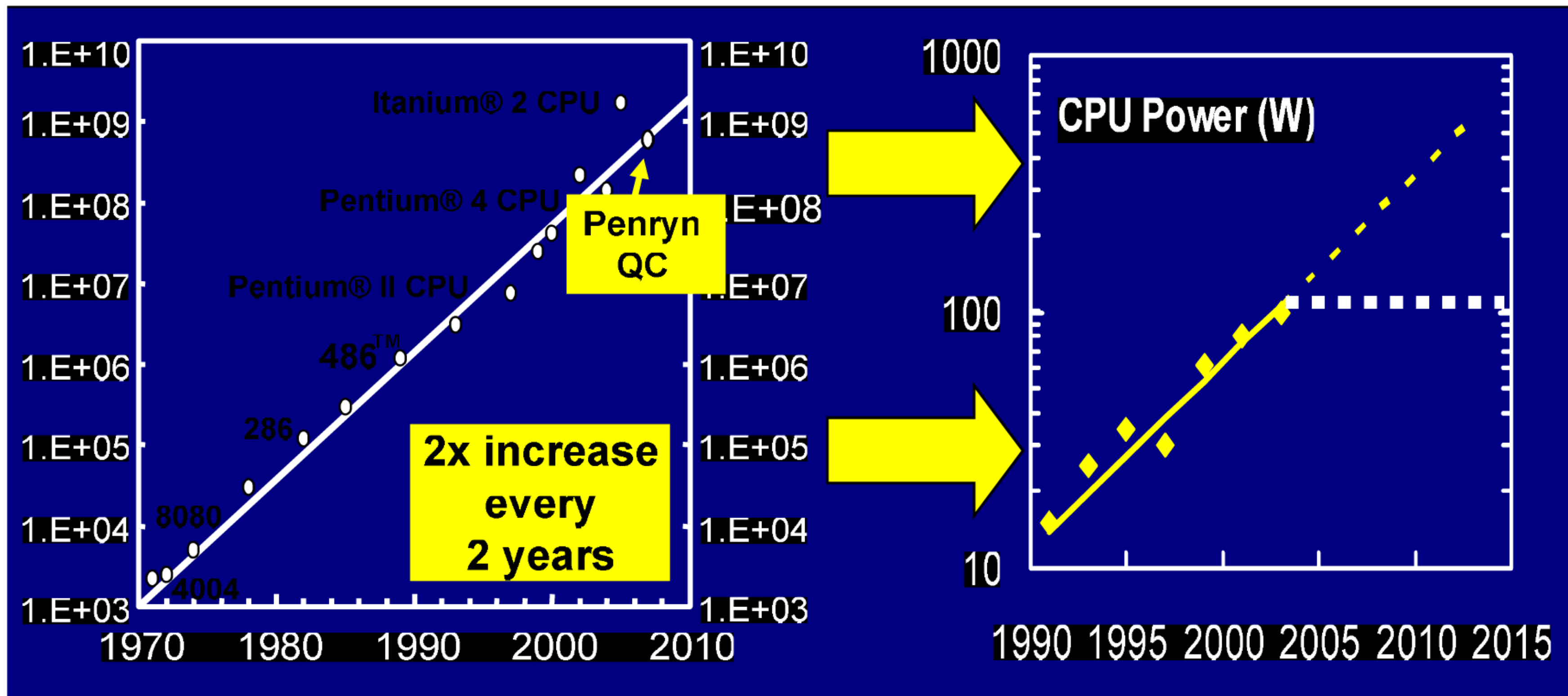


Intel's 32 nm process is certified and CPU wafers are moving through the factory in support of planned Q4 revenue production

Outline



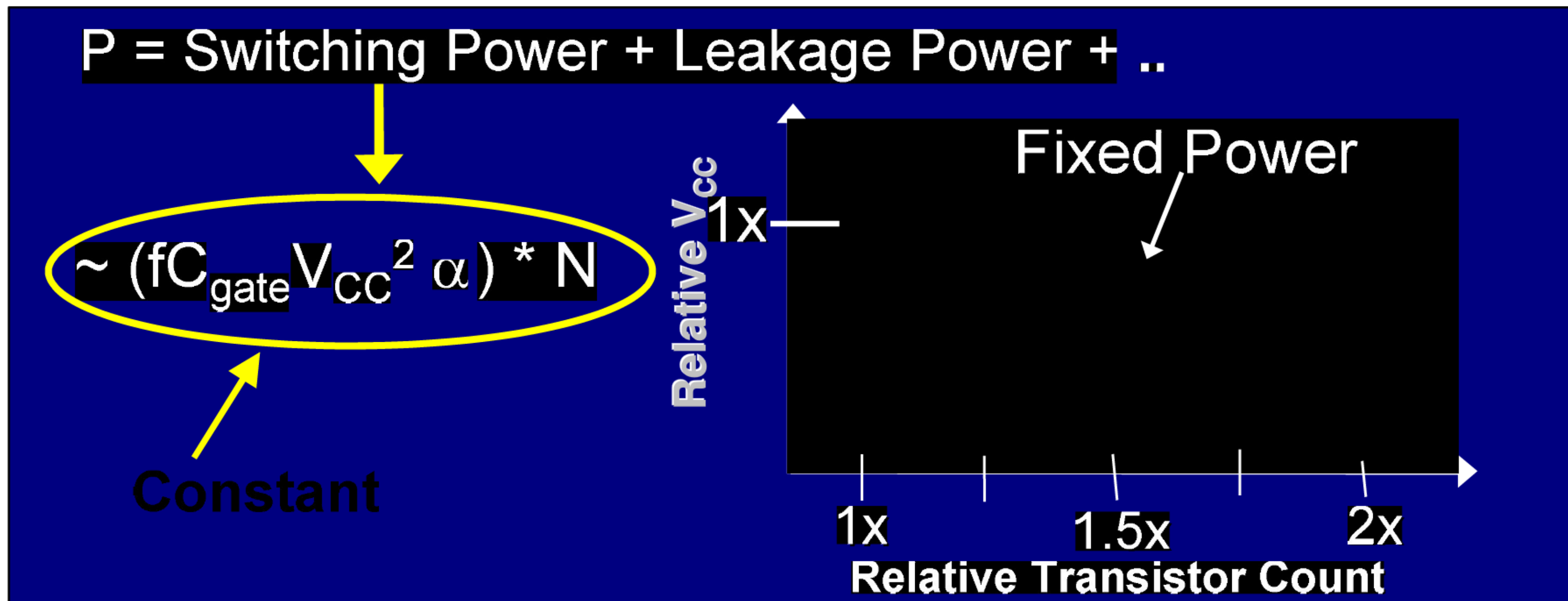
CPU Transistor Count & Power Trend



Power Dissipation Limited to ~100W

BUT increased transistor count needed in Multi-Core CPU Era !!!

Multi-Core CPU Power Limited Era



- V_{CC} scaling required for continued increase in transistor count in power limited world

Future Transistors will need to continue to achieve Higher Performance while Scaling Power Supply Voltage

Possible Future Transistor Options

- Advanced Channel Materials
  - III-V and Ge channel materials
- Multi-Gate Fin Transistors
  - Non planar architecture
- Tunnel Transistors
  - New transport mechanism

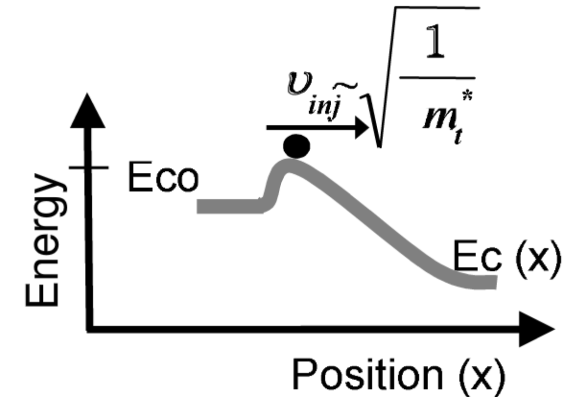
Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET

Ultimate Channel Materials: Ballistic Transport

Ultimate Ballistic Regime:

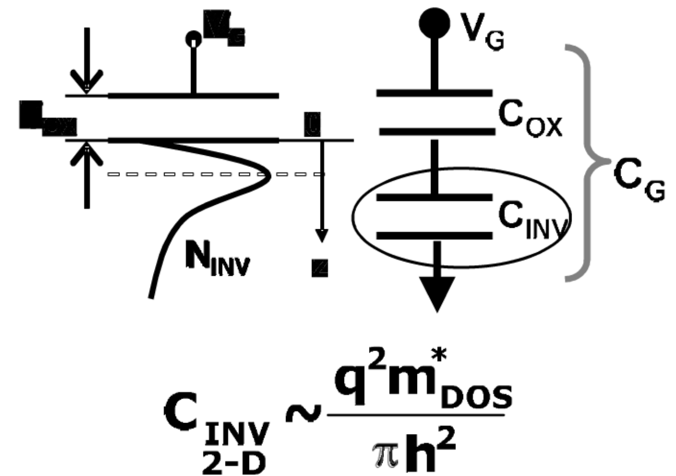
$$I_{DSAT} \sim Q_{inv}{}^{*}\upsilon_{inj}$$

1. Need low m_t^* in channel direction to achieve high υ_{inj} and maximize I_{DSAT}



Quantum Capacitance very important at thin T_{OX}

2. Need high m^*_{DOS} to achieve high C_{GATE} and Q_{inv} to maximize I_{DSAT}



$$C_{\substack{INV\\2\text{-}D}} \sim \frac{q^2 m^*_{DOS}}{\pi h^2}$$

III-V Materials for NMOS Channel?

+ Low m* Γ valley ⇒ High υ_{inj}

- Low m* Γ valley ⇒ Low m^*_{DOS} ⇒ Low Q_{INV}

- 2-D Quantization:
  - ⇒ Charge transfer from low mass Γ to high mass X & L valleys
  - ⇒ Lowers υ_{inj}

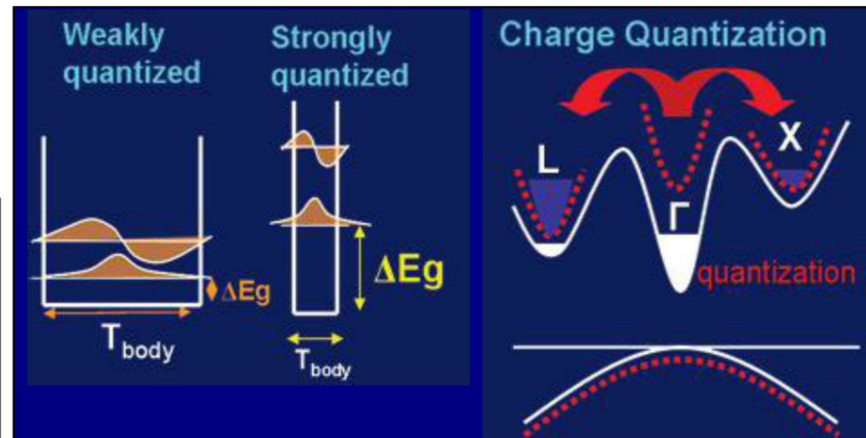
- Low Eg ⇒ Large Ioff (junction)

- High ε ⇒ Poor SCE

Projecting III-V NMOS performance based on simplistic models could lead to erroneous performance assessment.

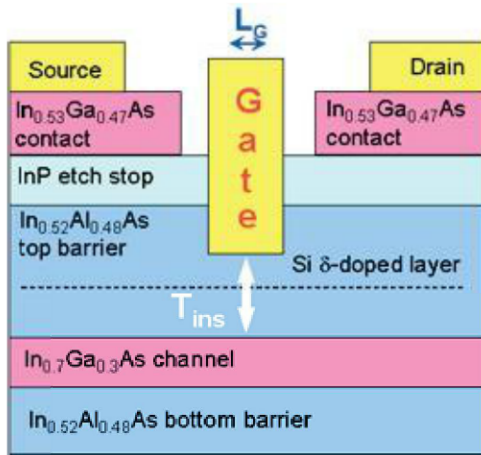
Properties of some NMOS candidates

Material/Property	Si	Ge	GaAs	InAs	InSb
m_{eff}^*	0.19	0.08	0.067	*0.023*	*0.014*
μ_n (cm^2/Vs)	1600	3900	9200	*40,000*	*77,000*
E_G (eV)	1.12	0.66	1.42	*0.36*	*0.17*
ε_r	11.8	16	12.4	14.8	*17.7*

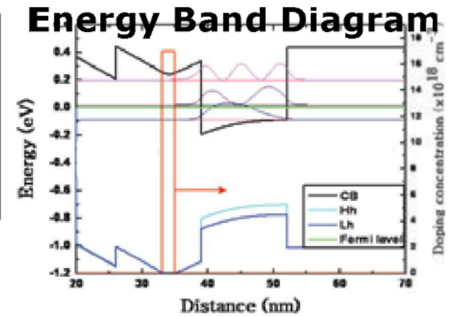


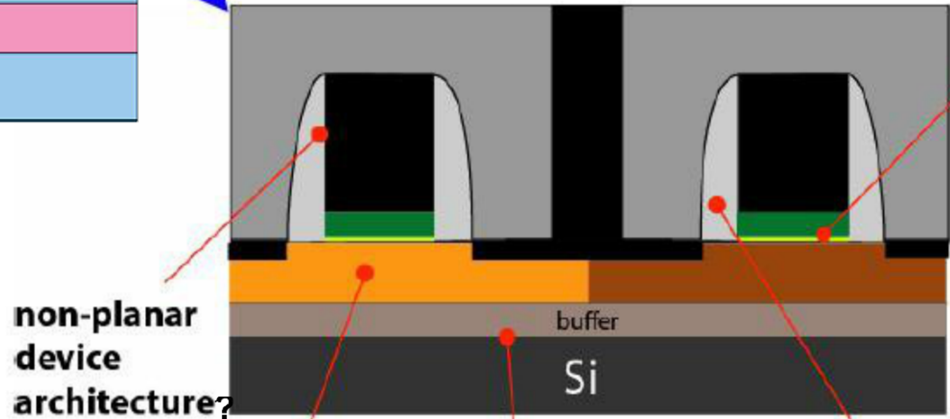
K. Saraswat et.al., IEDM 2006

The Grand Challenges for III-V CMOS



- InGaAs Quantum Well channel
- InAlAs insulator (poor Jox)
- Ti/Pt/Au gate
- Non-self aligned contacts





high-K dielectric gate insulator

J. Del Alamo IEDM 2007

III-V p-type channel device

Scalable, self-aligned, E-mode device architectures

III-V epitaxy on large-area Si wafers

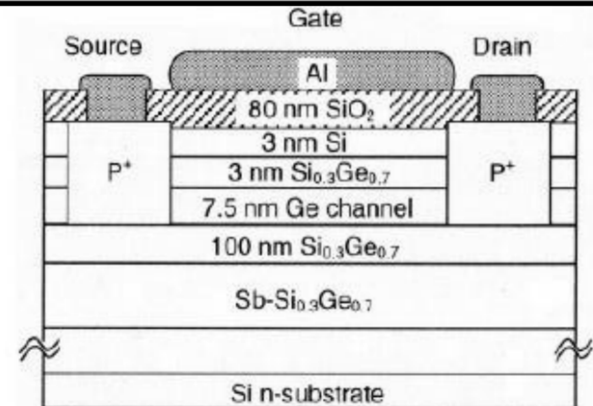
Ge Transistor- Back to the Future?

- **Advantages:**
  - + Best hole mobility (unlike III-V)
  - + Si(Ge) already used in logic tech
  - + Col-IV: Non-Polar
- **Challenges:**
  - - Reference device is highly strained silicon
  - - Poor HiK interface:
    - * Need better understanding
    - * Buried strained QW Ge
  - - Higher dielectric constant
    - * Poorer SCE
  - - Worse parasitic resistance
    - * Worse dopant activation

Material ⇒ Property ⇓	Si	Ge	GaAs	InAs	InSb
Electron mobility	1600	3900	9200	40000	77000
Hole mobility	430	1900	400	500	850
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

K. Saraswat et.al., IEDM 2006.

Buried Strained Ge Quantum Well



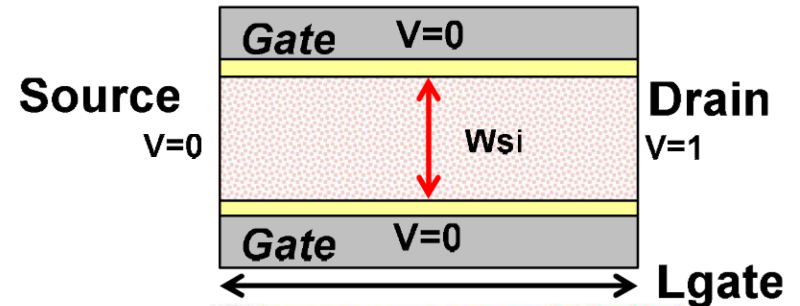
(U. Tokyo, APL 2002)

Possible Future Transistor Options

Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET

Multi-Gate Transistor Architecture

$$\frac{\partial^2 \Phi}{\partial x^2} + \frac{\partial^2 \Phi}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}}$$

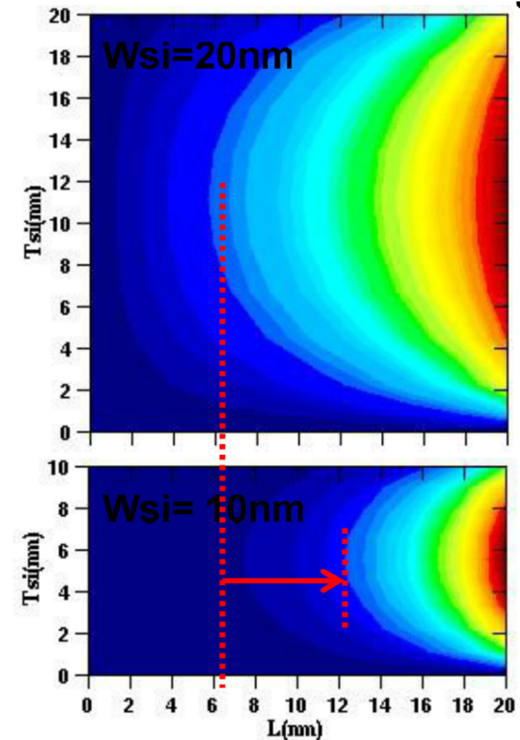


Multi-Gate Transistors have better SCE:

- Gates reduce spread of V_{drain}
  Enables lower threshold voltage (↑I_D)
- Enable lower channel doping (↑μ)

Multi-Gate Transistors have lower E_{EFF}:

- Optimum gate work function is away from band-edge leading to lower Eeff (↑μ)

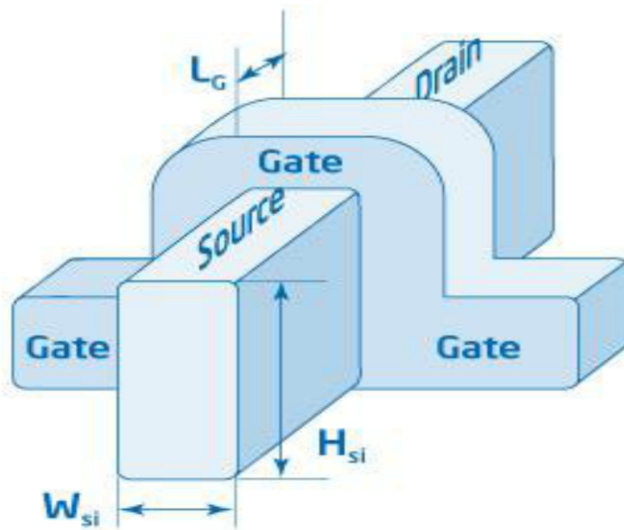


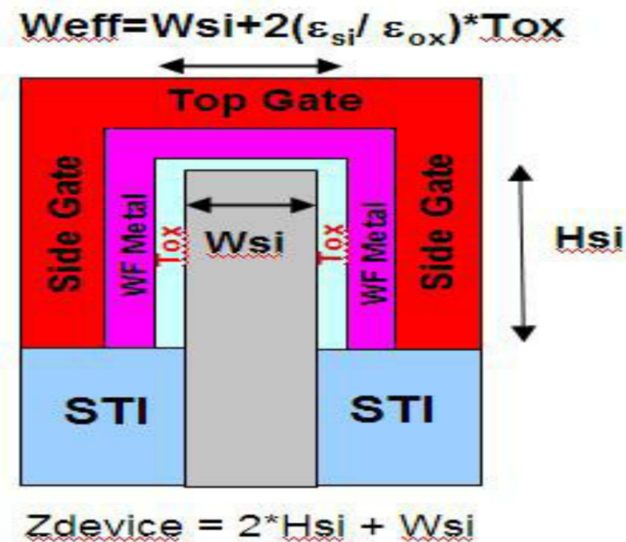
Multi-Gate Transistors Implementation

Multi-Gate Fin Transistor:

++ Self Aligned structure for S/D

-- Non-Planar structure

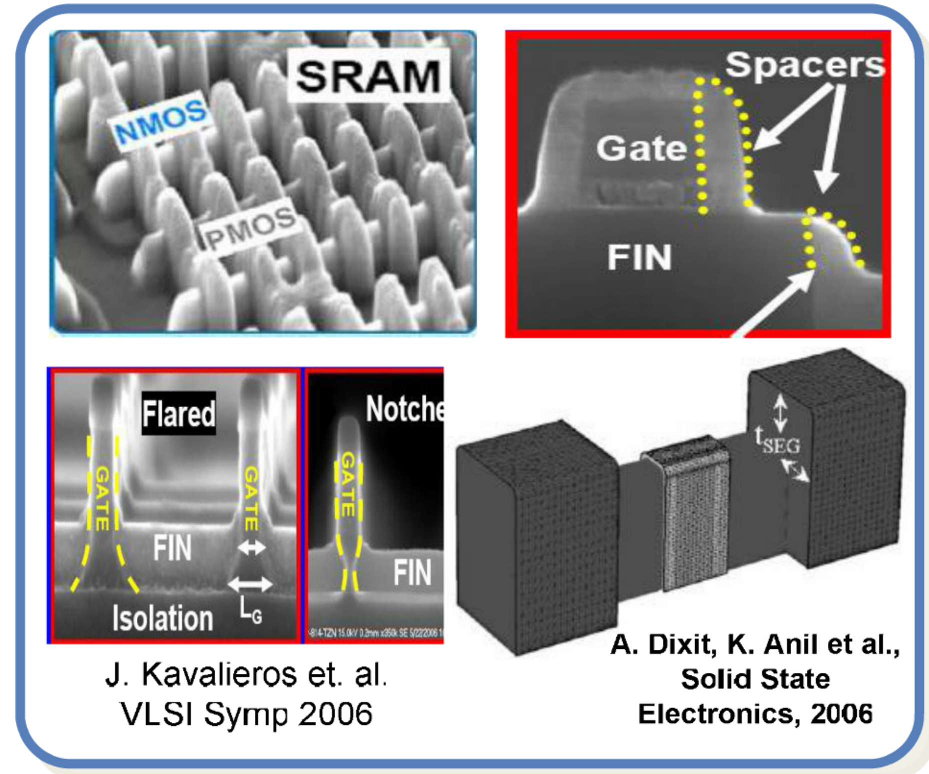




Multi-Gate Fin Transistor

Top Challenges for Multi-Gate Fin Transistors

- **Implement High Strain in Fins?**
  - Planar Ref= Highly strained 4-5x p-mobility enhancement
  - High level of fin strain NOT published to date
- **High Parasitics in Fin Transistors**
  - Narrow fins lead to high Rext
  - Fin architecture may also lead to higher fringe capacitance
- **Manufacturing worthy Patterning**
  - Fin, Gate and Spacer patterning will be extremely challenging in a manufacturing environment
- **Design**
  - Device Z increments quantized



J. Kavalieros et. al. VLSI Symp 2006

A. Dixit, K. Anil et al., Solid State Electronics, 2006

- **Best published drive currents for Multi-Gate Fin Transistors are <u>significantly lower</u> than best published planar transistors to date**
- **Many significant challenges remain to be resolved for Fin Transistors**

Possible Future Transistor Options

Each transistor structure has many significant challenges which will have to be successfully addressed if it is to become a serious contender to silicon MOSFET

Why we Need to Beat Sub-Threshold Slope of 60mV/decade?

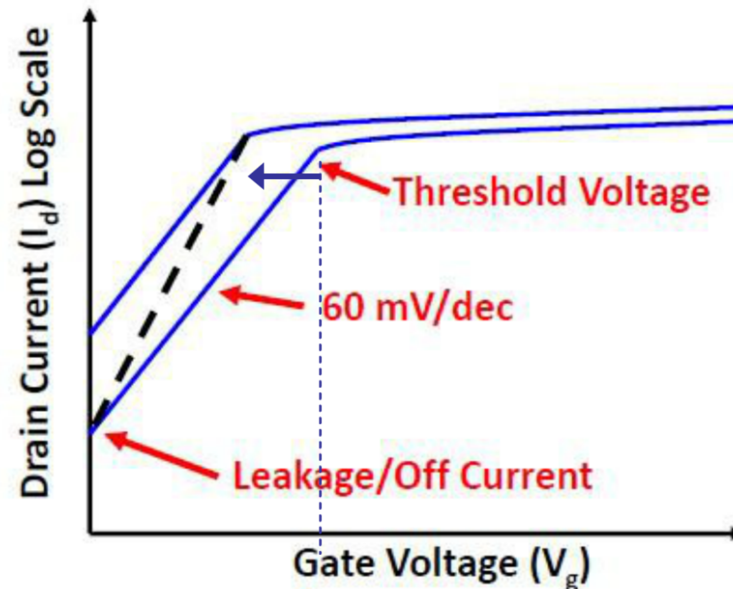
$I_D \sim (V_{CC}-V_{TH})$

At very low Vcc we need small V_{TH} for reasonable drive

BUT

Sub-threshold slope is limited by thermal kT/q limit
➔ Ioff increases exponentially with V_{TH} scaling.

HOW TO BEAT kT/q limit?

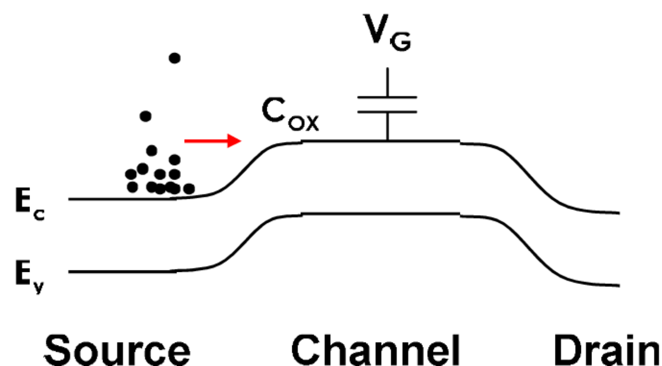


$$S = \left(\frac{d\log I_d}{dV_g}\right)^{-1} = 2.3\frac{kT}{q}\left(1+\frac{C_d}{C_{ox}}\right) \geq 2.3\frac{kT}{q}$$

Leakage current increases ***exponentially*** as device is scaled

Ultimate Frontier: Overcoming Thermal kT/q Limit

C. Hu, STEEP Program

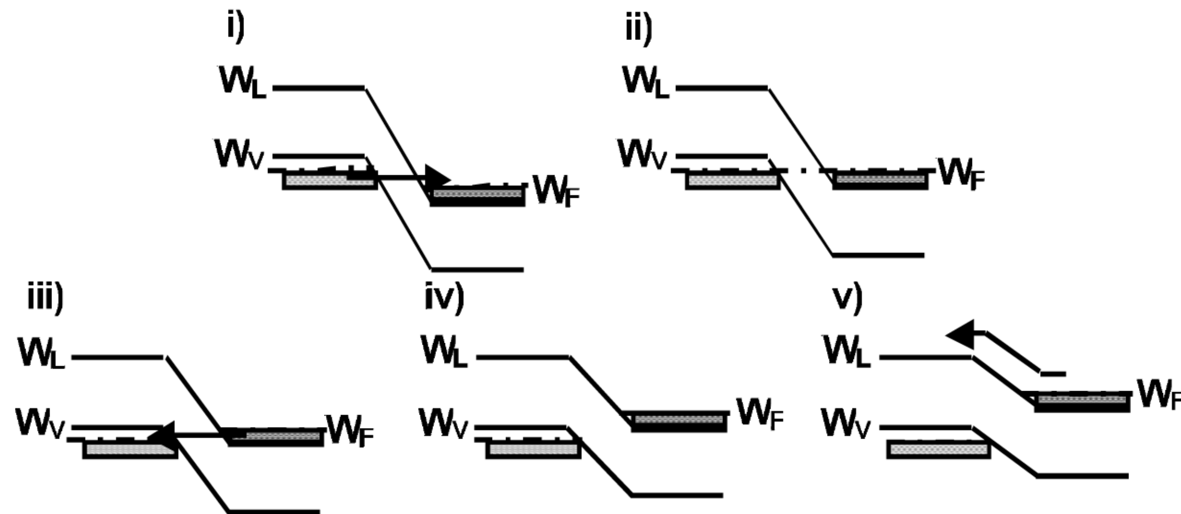


Electrons go over a potential barrier. Leakage current is determined by the Boltzmann distribution or 60 mV/decade, limiting MOSFET, bipolar, graphene MOSFET…

How to overcome the limit:

Let electrons go through the energy barrier, not over it → Tunneling

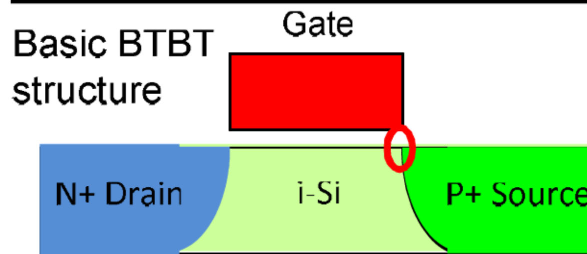
Semiconductor Band-to-Band Tunneling



- Esaki demonstrated this experimentally in 1958
- Can lead to negative resistance- Esaki diode
- Transistor: Tunneling can be controlled by gate!!

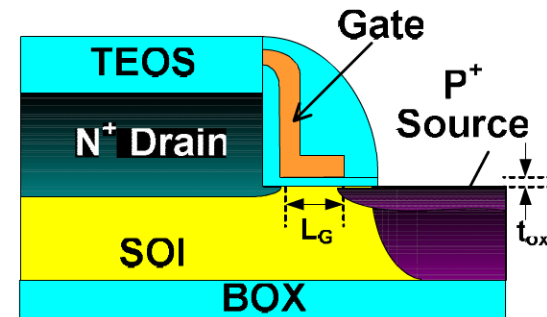
Leo Esaki
Nobel Prize for Physics 1973

Tunnel Transistor Concept and Challenges

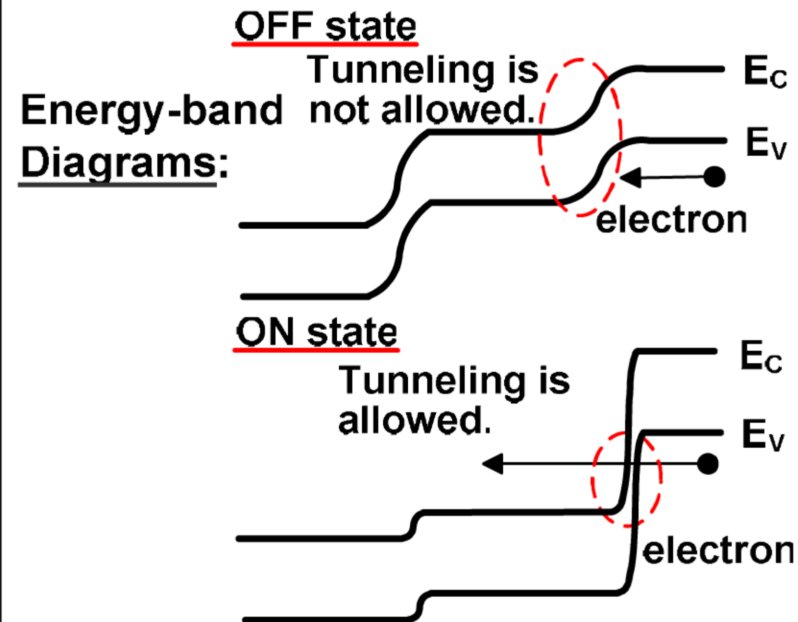


- Device behaves like reverse bias pin diode
- Positive Vgs induces electron electron channel
- Band bending allows tunneling at source channel interface ➔ Gate controlled band tunneling
- BTBT Transistor suffer from extremely poor drive current
  ➔ **Need materials with more efficient tunneling**

Structure:



Energy-band Diagrams:



W. Y. Choi *et al*. *IEEE-EDL* vol. 28, pp. 743-745, 2007

Key Messages / Summary

- **Intel's Response to end of "traditional-scaling":**
  - Uniaxial Strain (90nm and beyond): 32nm is 4th generation of uniaxial strain at Intel
  - HiK + Metal Gate (45nm and beyond at Intel)

These innovations have enabled Intel to maintain historical performance gains on recent nodes

- **Future Novel Transistors:**
  - New Channel Materials:

    Integrate Ge & III-V on top of Silicon. Many device and material challenges remain
  - Multi-Gate Fin Transistors:

    Scaling benefits BUT need to demonstrate effective strain implementation, matched parasitic resistance to planar and overcome patterning challenges
  - BTBT (Tunnel) Transistors:

    Ultimate transistors may need tunnel injection at ultra-low Vcc. Would need new materials with more efficient tunneling and atomic scale fabrication control

Many exciting materials, physics and integration challenges left to continue CMOS scaling