# Role of High-K Gate Dielectrics and Metal Gate Electrodes in Emerging Nanoelectronic Devices

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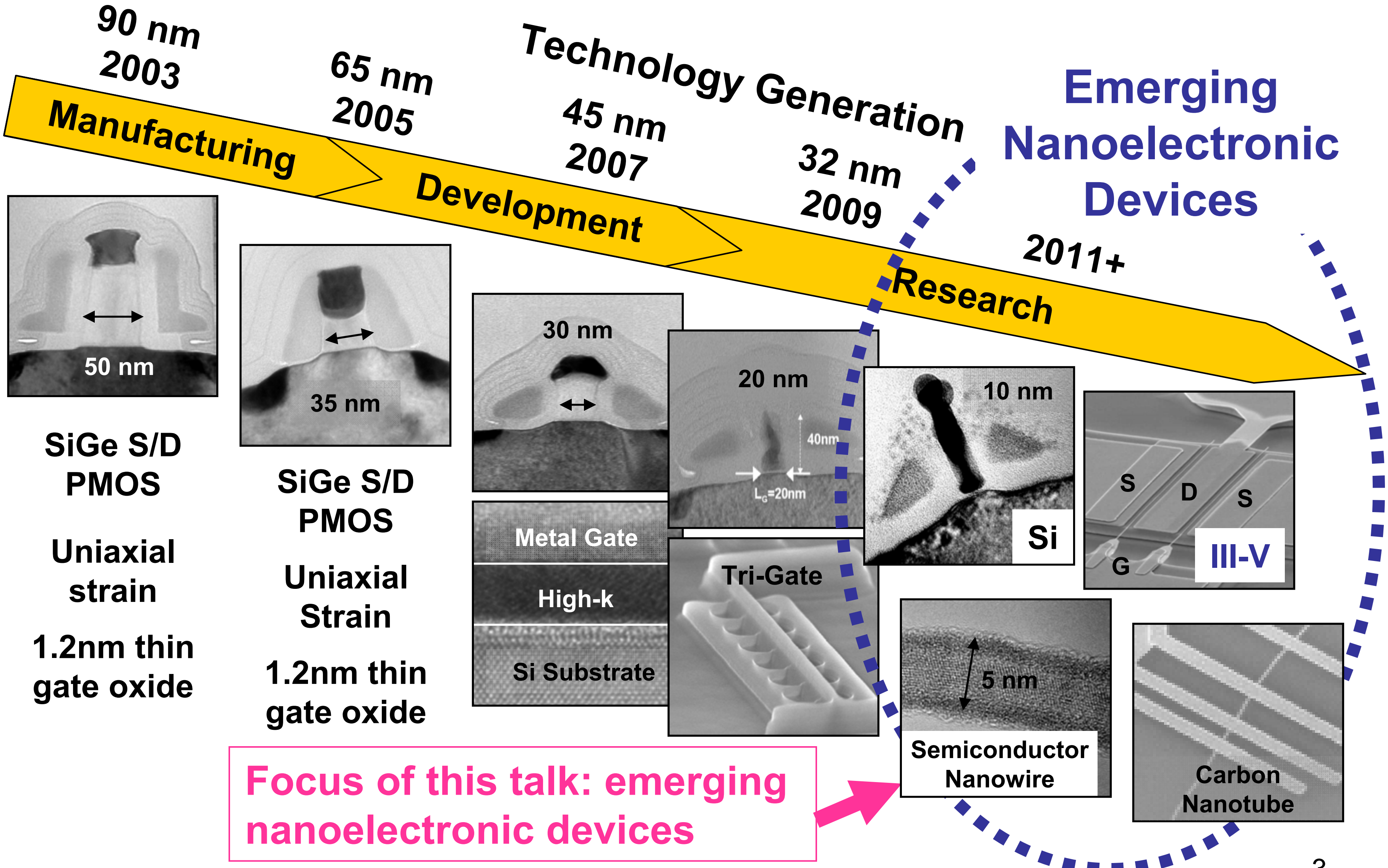
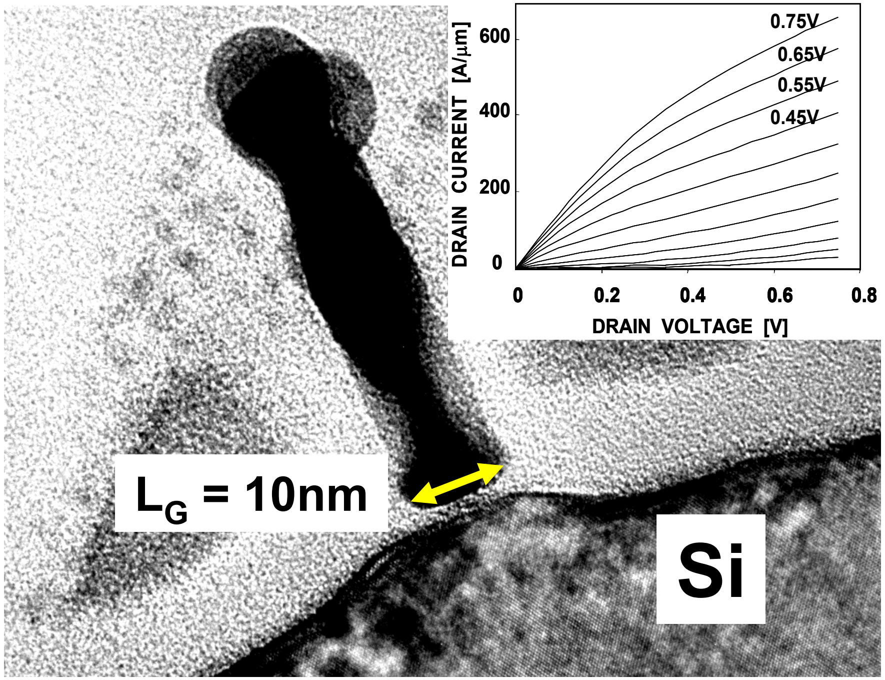
# Transistor Nanotechnology

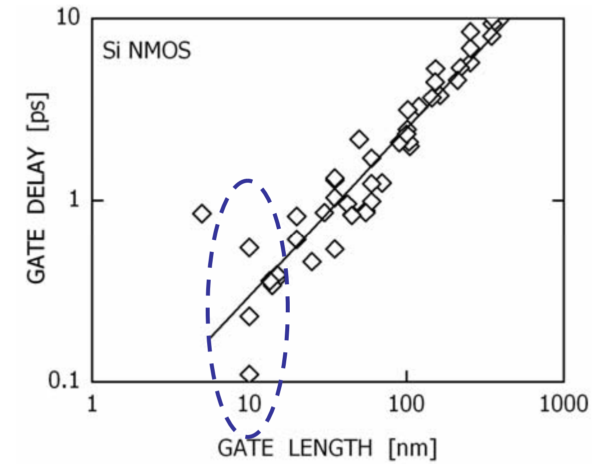


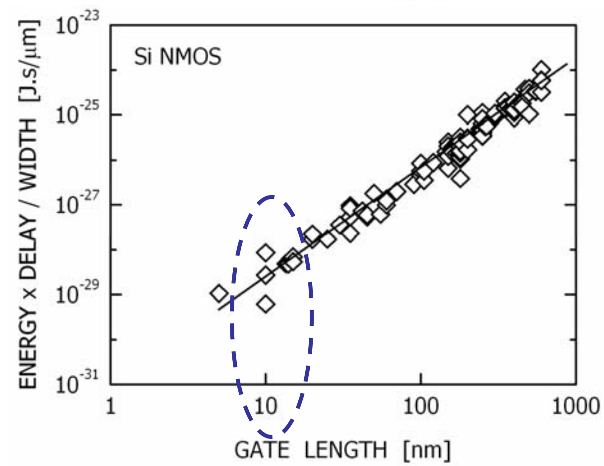

*Note: Future options subject to change*

# Experimental 10nm Si MOS Transistor

Source: R. Chau et. al., Intel Corp., 61st DRC, June 2003

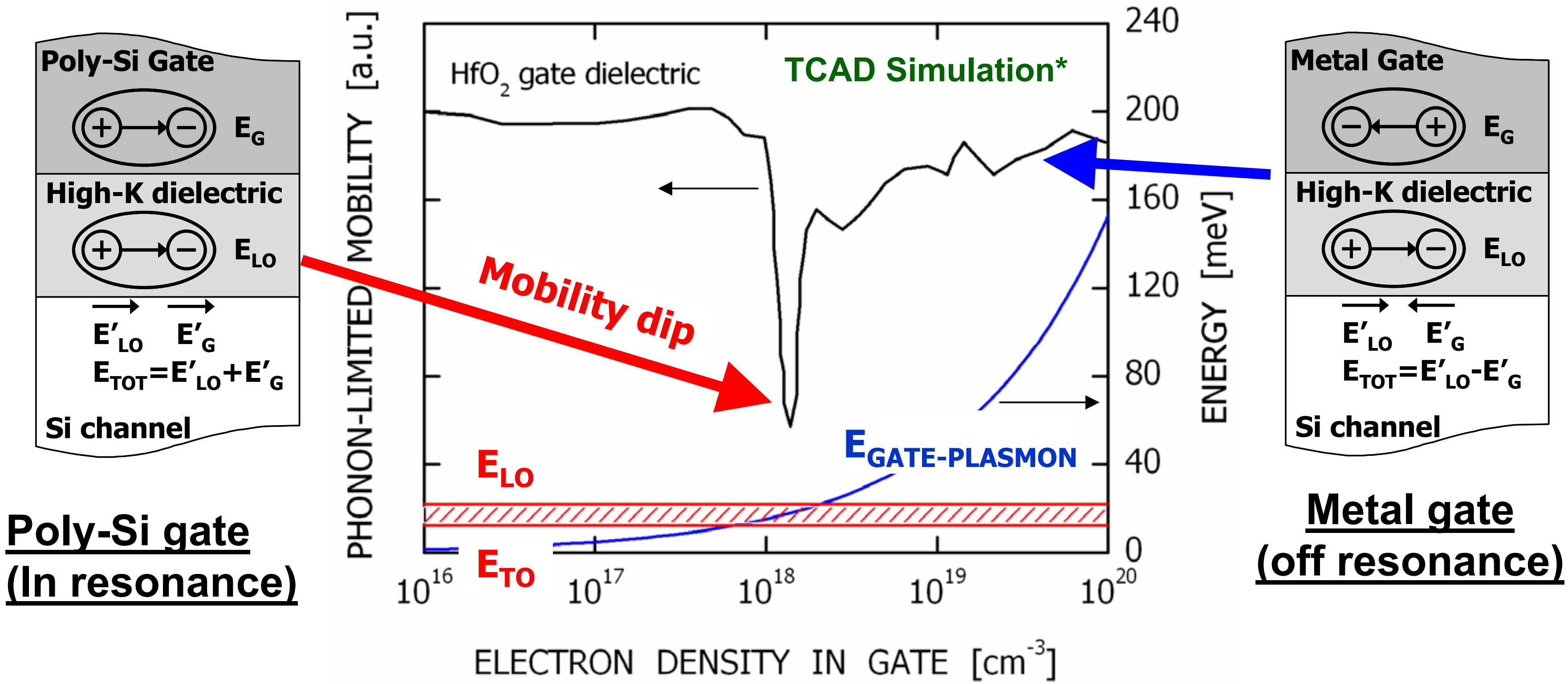



- **10nm Si transistors produced in research labs**
  - **Still a switch <u>with gain</u>**
- **Need to benchmark emerging non-Si nanoelectronic research devices versus state-of-the-art Si research transistors**

# Review of High-K Physics on Si



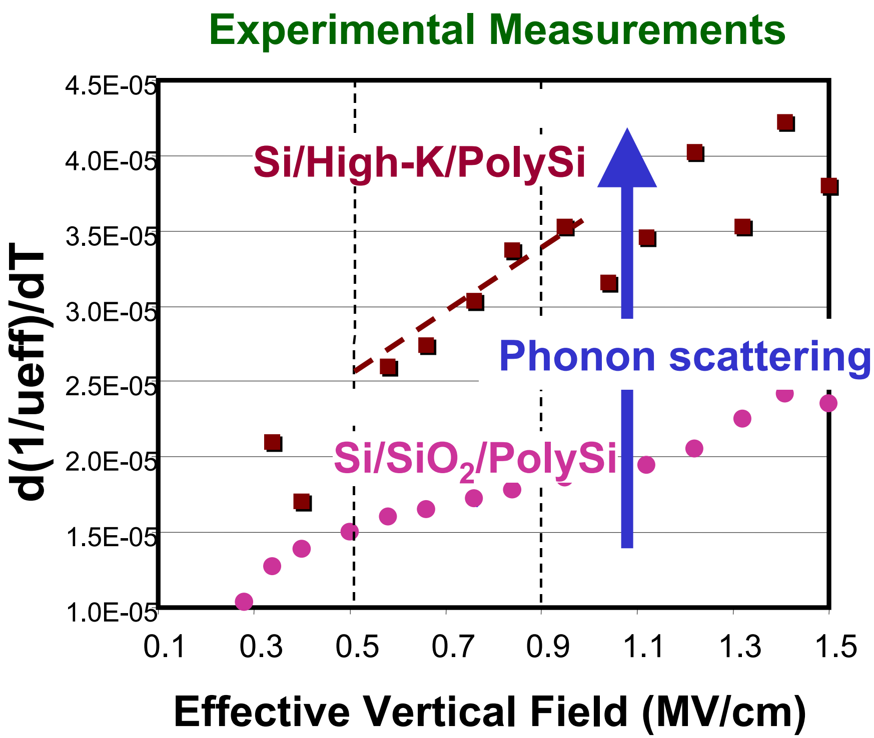

**Poly-Si gate (In resonance)**

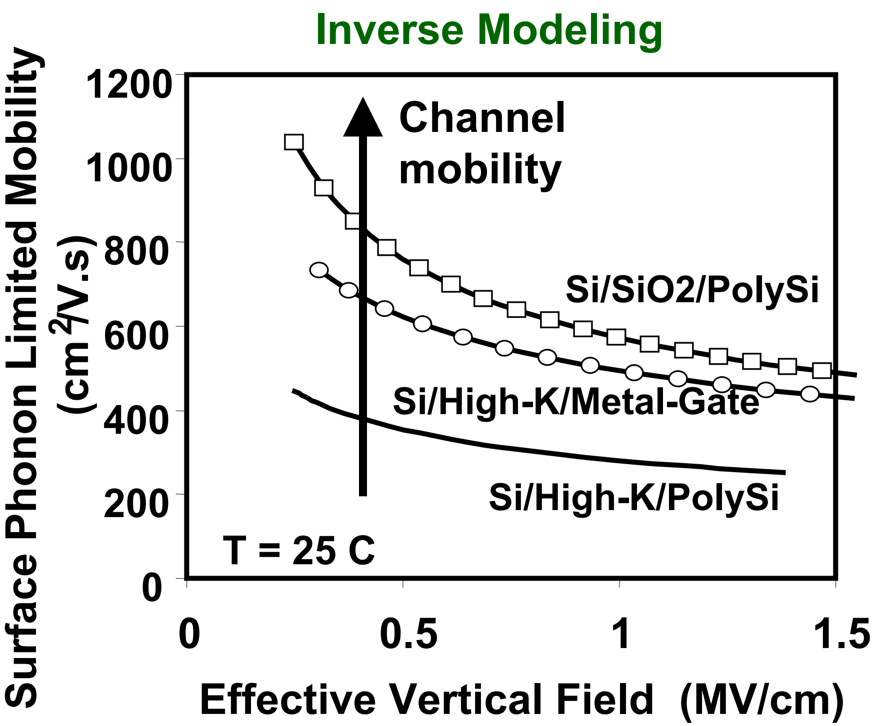
**Metal gate (off resonance)**

- **High-K phonons and gate plasmons modeled as electric dipoles**
- **Doped polySi gate (~$10^{18}$ cm$^{-3}$): When $E_{TO} < E_{GATE\text{-}PLASMON} < E_{LO}$, in-resonance condition occurs which degrades channel mobility**
- **Metal gate (>$10^{20}$ cm$^{-3}$): Off-resonance condition weakens phonon-carrier coupling, hence channel mobility is recovered**

* Source: R. Kotlyar et. al., Intel Corp., IEDM 2004

# Review of High-K Physics on Si

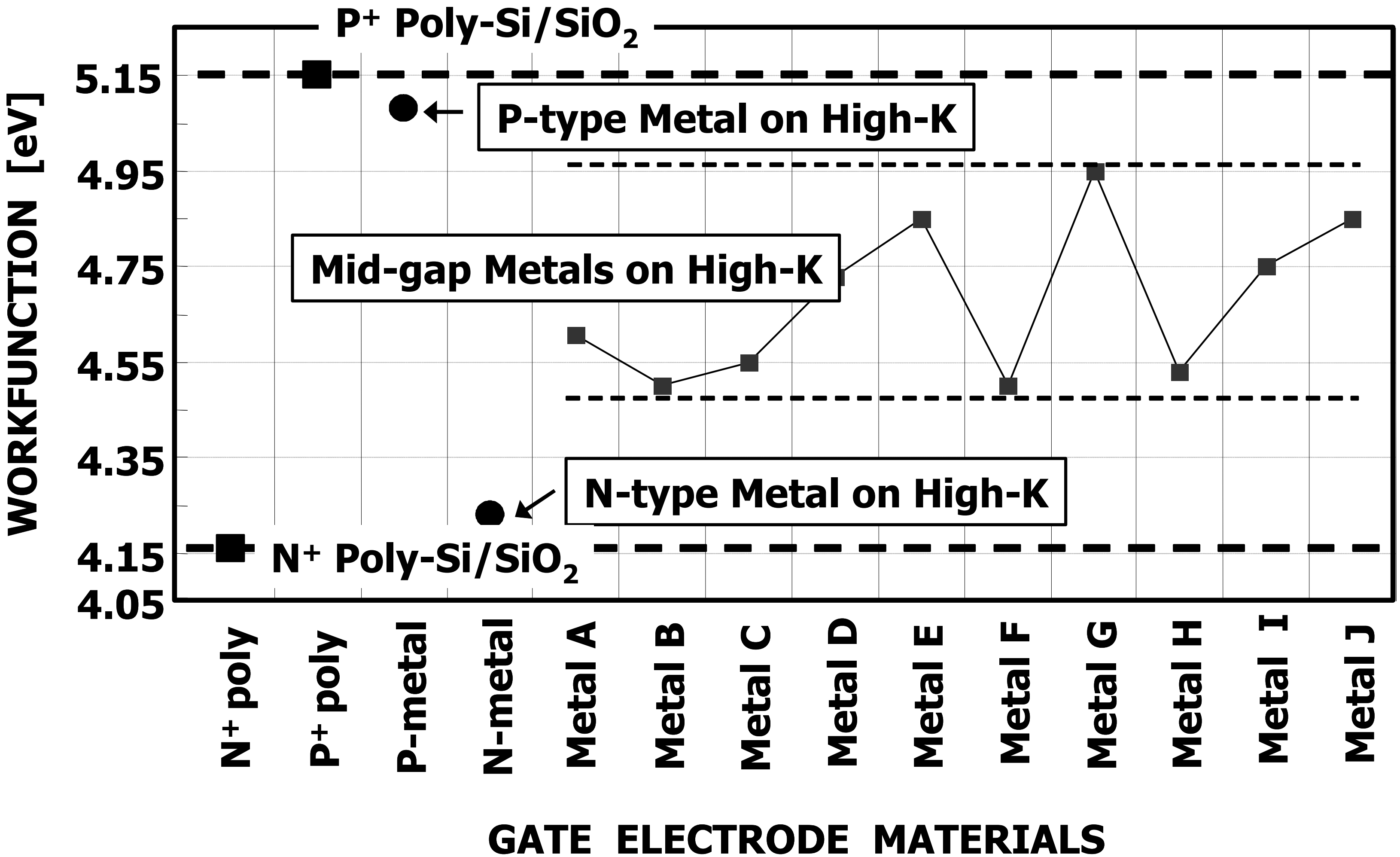



- Surface phonon scattering in high-K is primary source of mobility degradation
- Metal gate is effective for screening phonon scattering and improves channel mobility

Source: R. Chau et. al., Intel Corp., IEEE EDL, June 2004

# Review of High-K Physics on Si

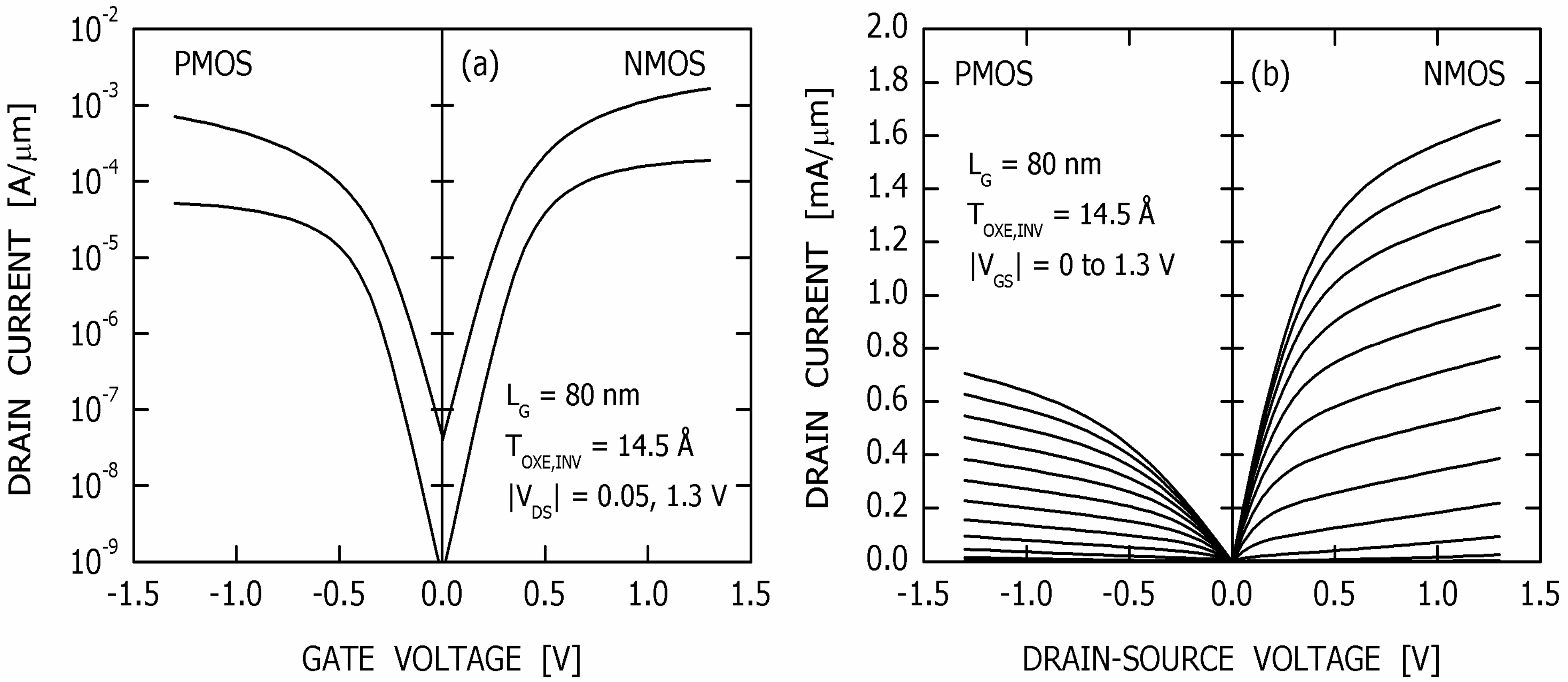



- Gate electrodes with the "right" work function are required for high-performance CMOS applications



Source: R. Chau, Intel Corp., AVS ICMI, March 2004

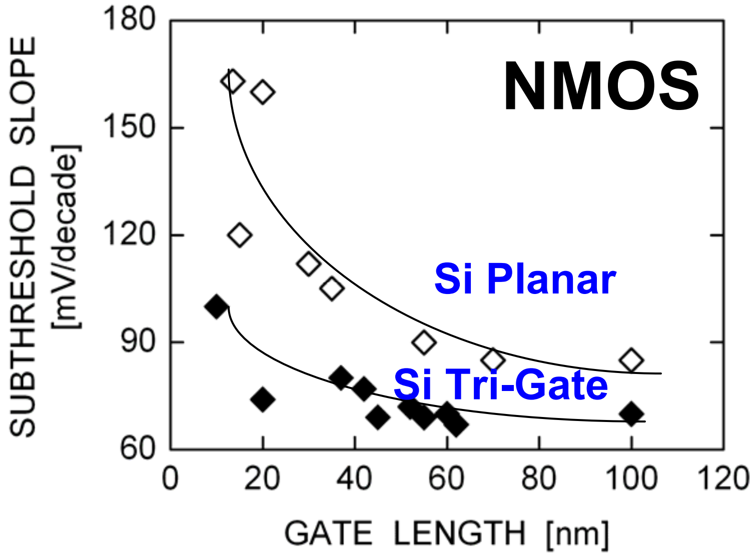
# Review of High-K Physics on Si

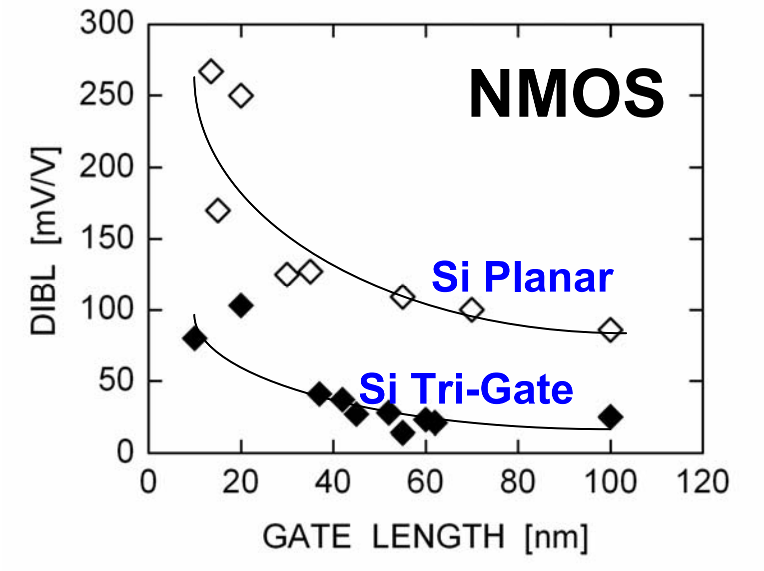


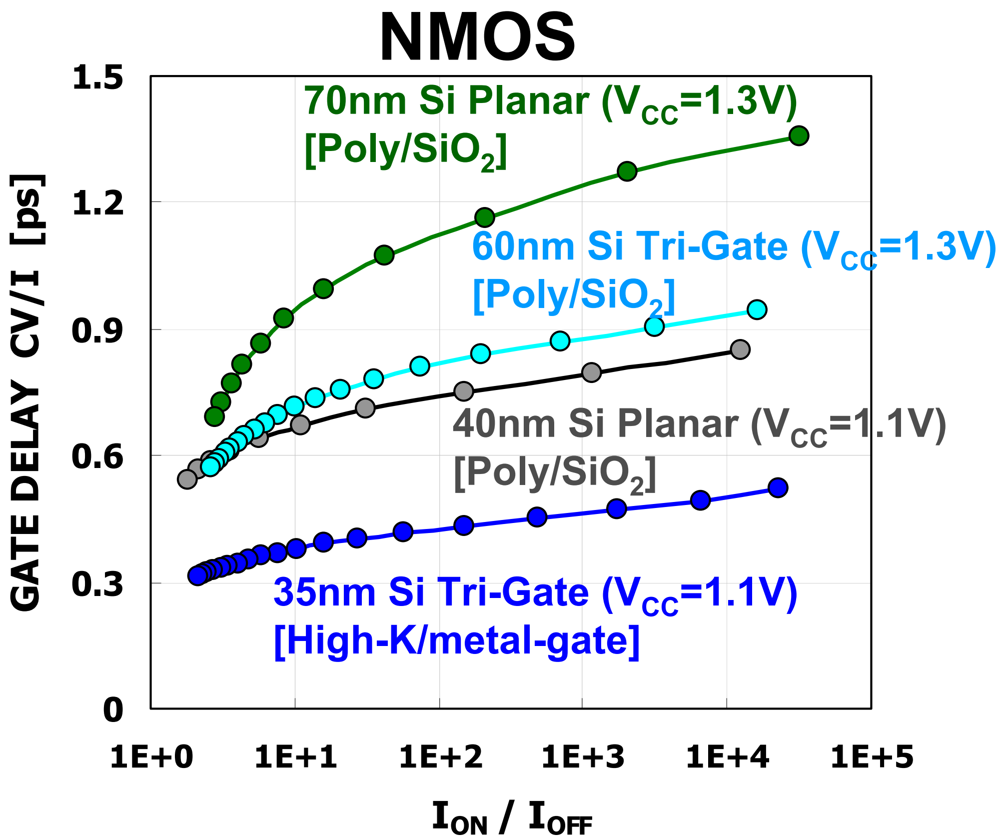

- **Example of high-performance CMOS transistors on bulk-silicon with high-K/metal-gate**
  - **Correct $V_{TH}$'s, high-mobility, low gate leakage**

Source: R. Chau et. al., Intel Corp., IEEE EDL, June 2004

# Conventional Planar and Non-Planar Si Transistors

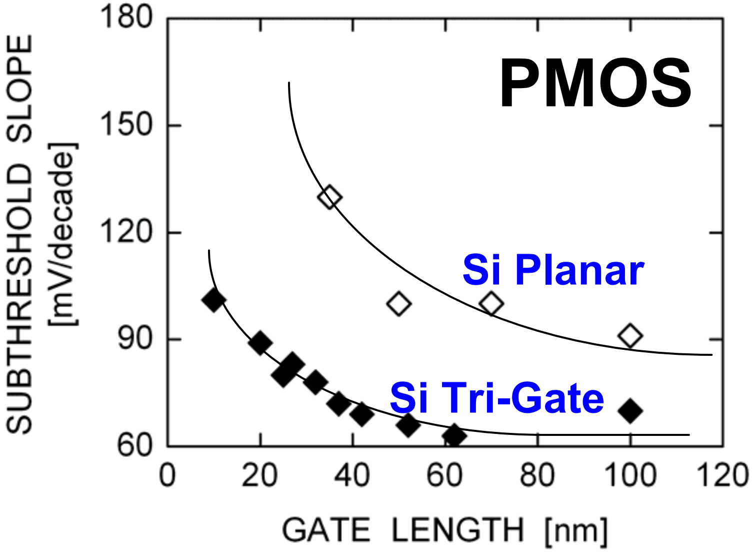


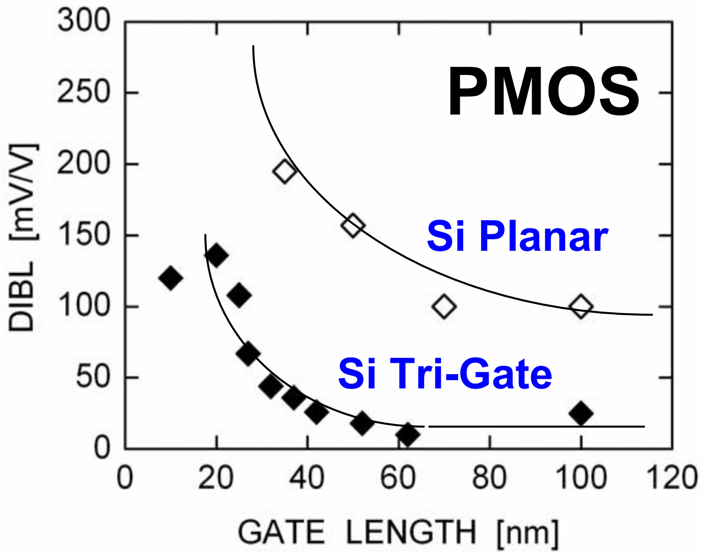



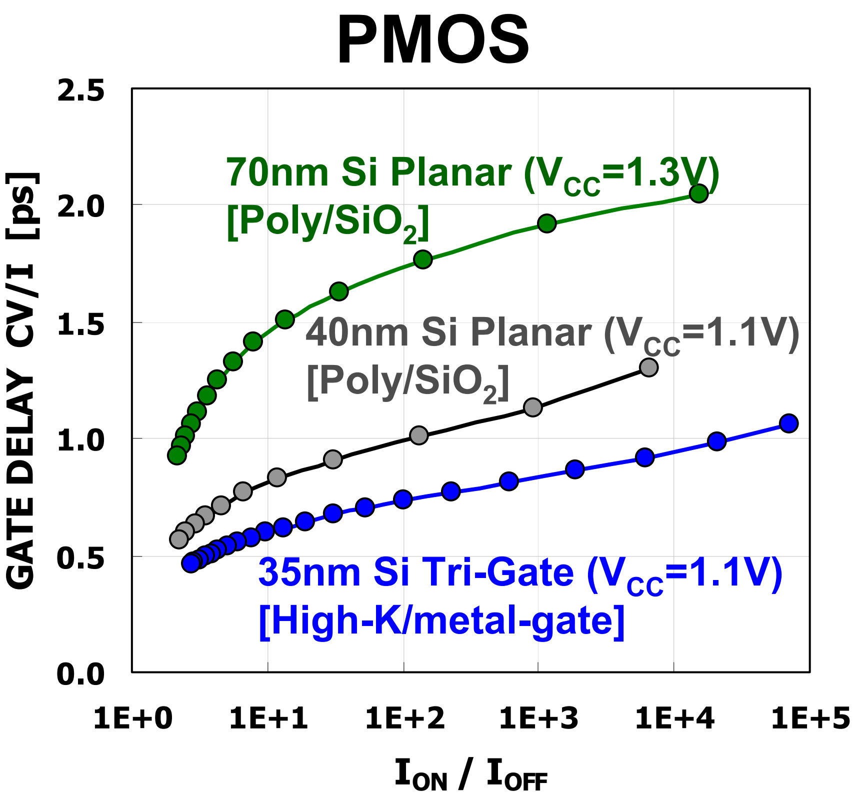




- Need to benchmark emerging non-Si nanoelectronic devices versus these conventional planar and non-planar Si NMOS transistors

# Conventional Planar and Non-Planar Si Transistors

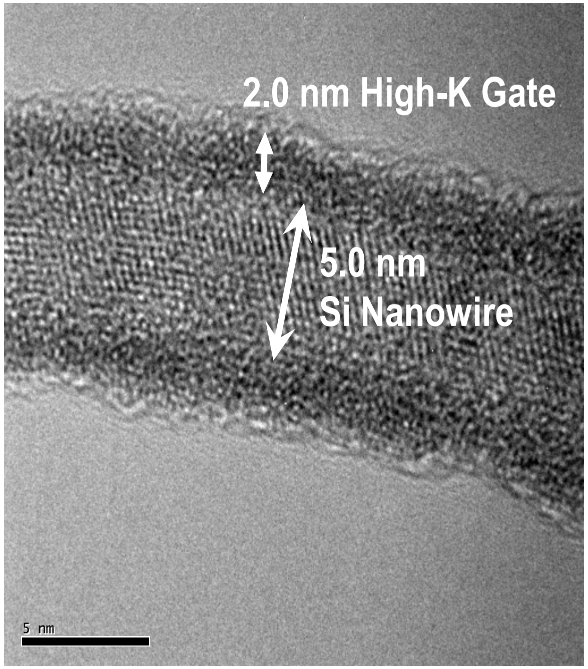


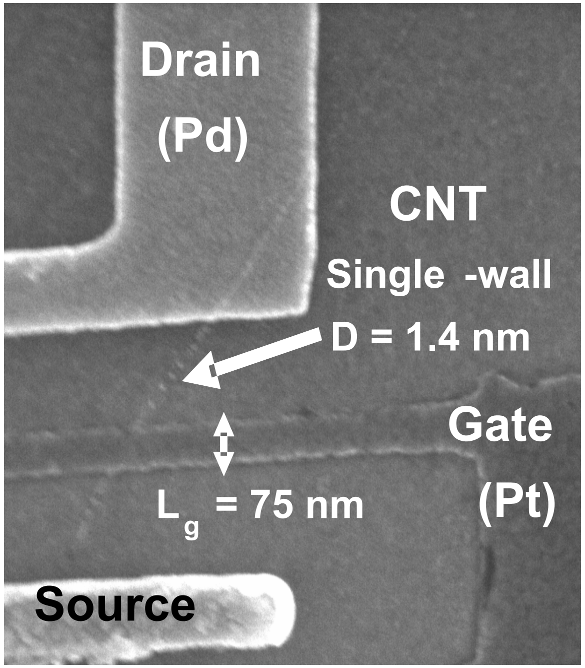




- **Need to benchmark emerging non-Si nanoelectronic devices versus these conventional planar and non-planar Si PMOS transistors**

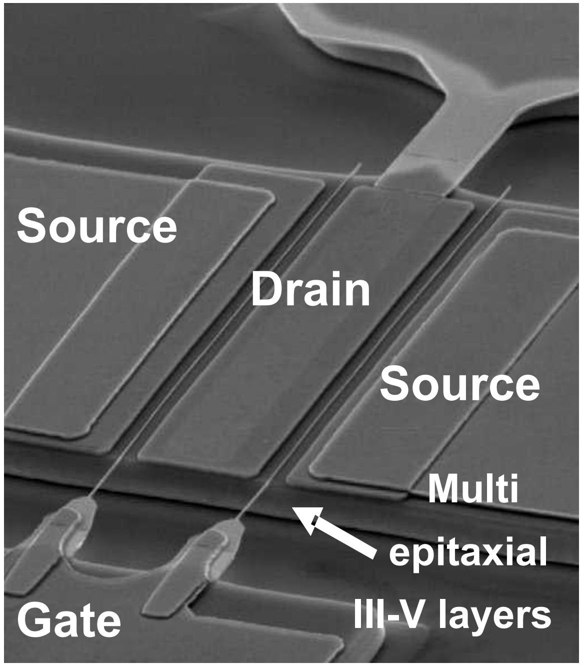
# Emerging Nanoelectronic Devices




- Semiconductor nanowires with high-K gate dielectrics




- Carbon nanotube FETs with high-K gate dielectrics



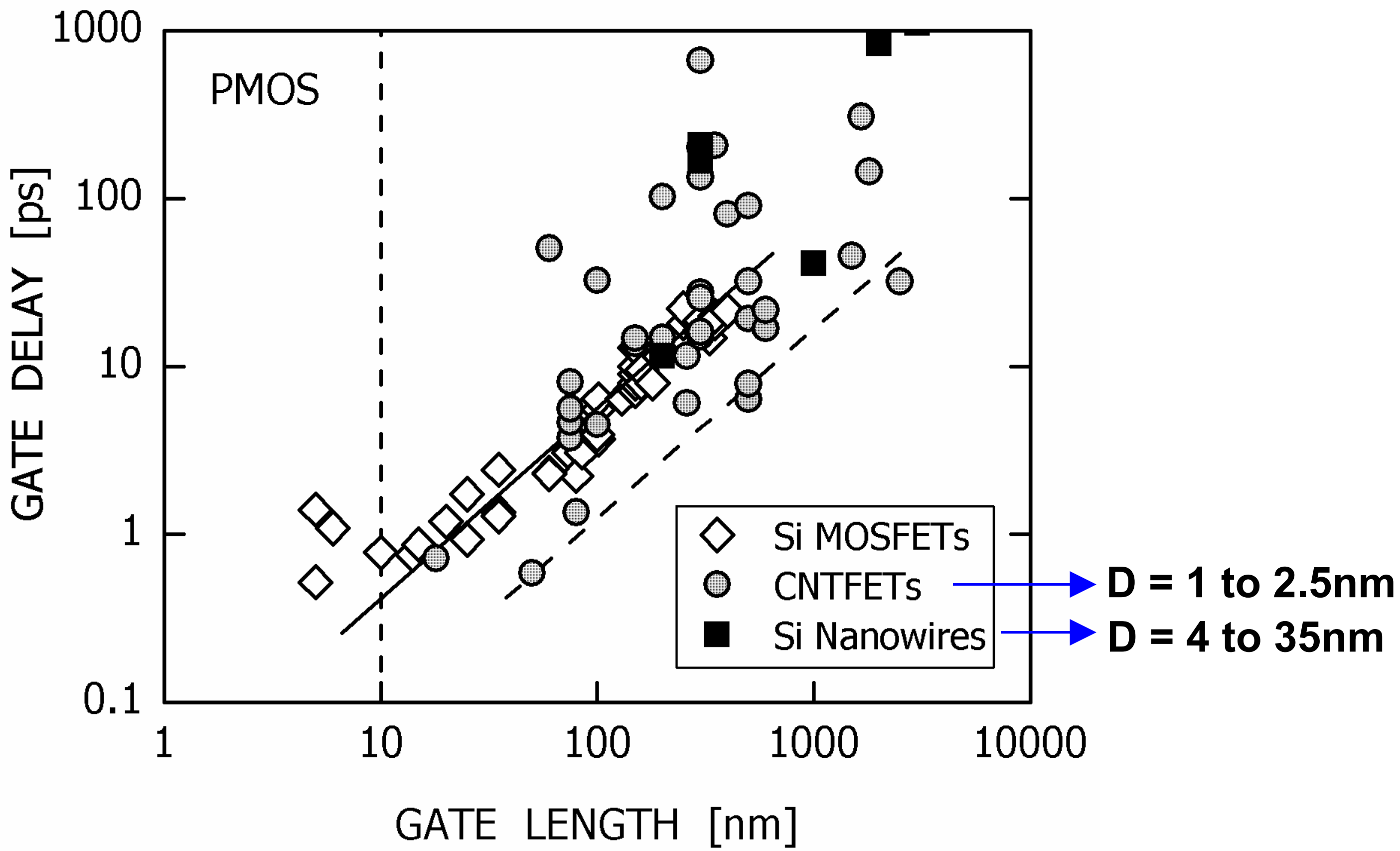

- III-V quantum-well (Q-W) transistors (high-K gate dielectric is currently absent in III-V but required for logic applications)

## Role of High-K/metal-gate:

– enabling continued equivalent gate oxide thickness scaling and hence high performance, and controlling gate leakage

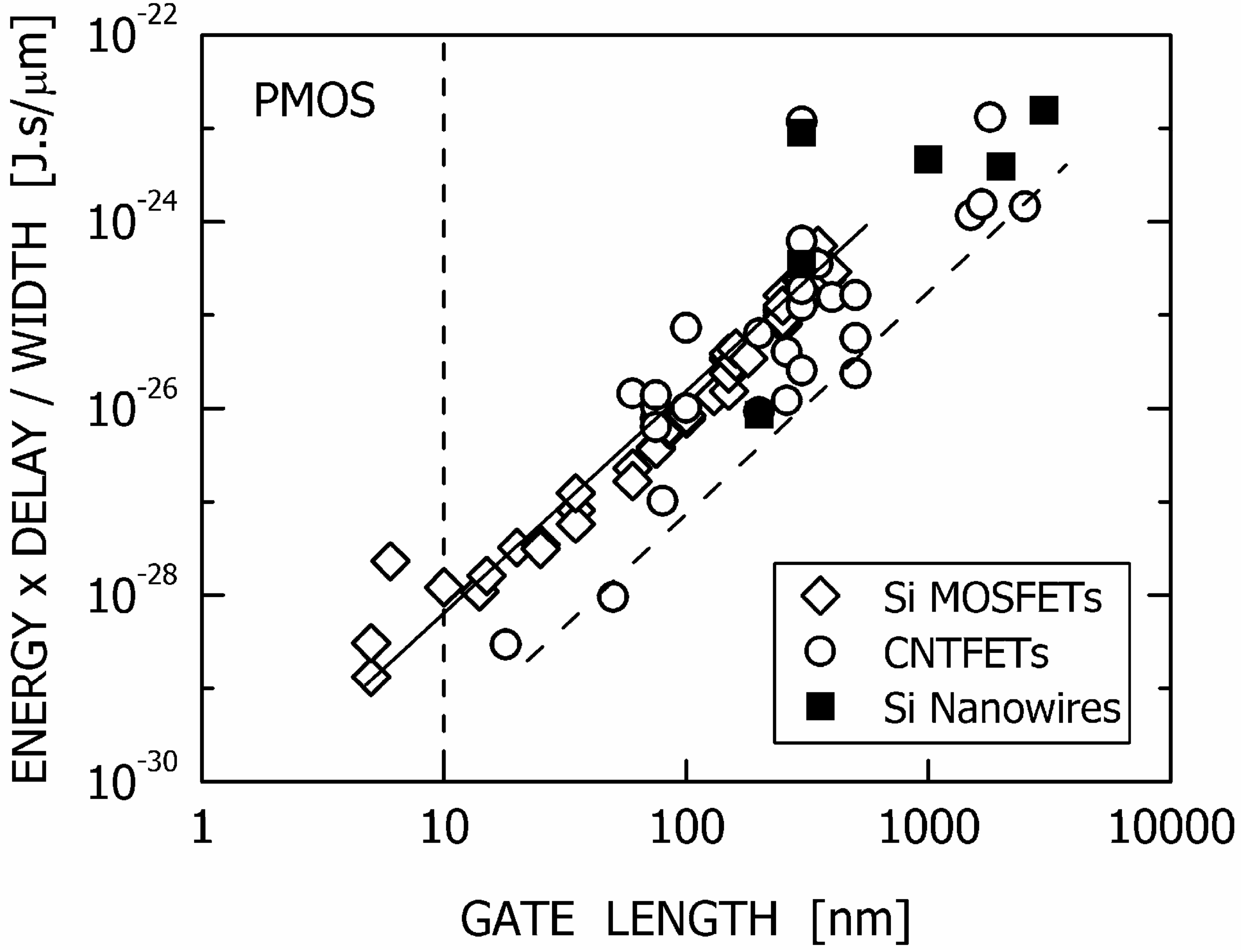
– required for high $I_{ON}/I_{OFF}$ ratios in III-V Q-W devices for logic

# Intrinsic Gate Delay CV/I for PMOS

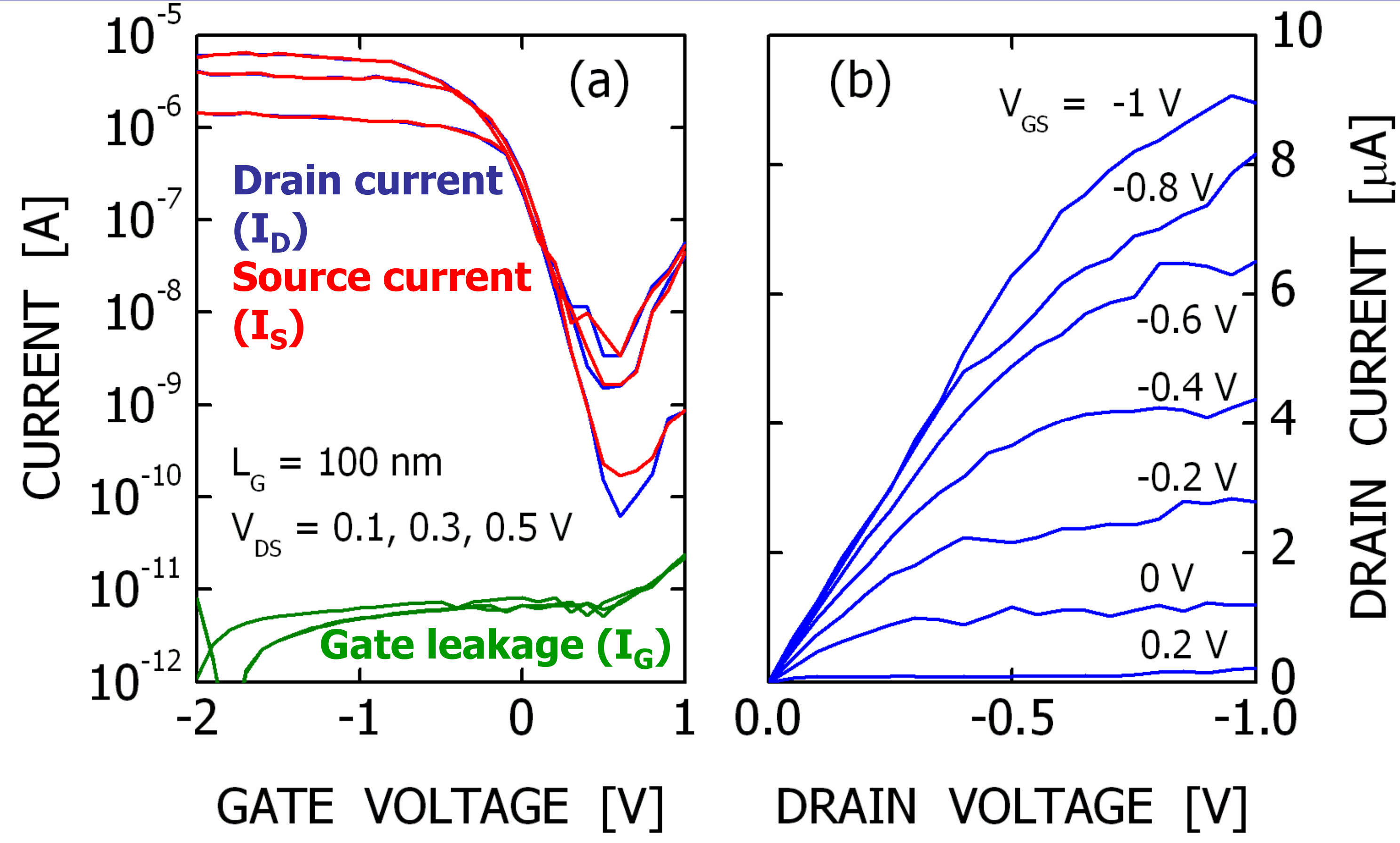



- **CNT shows significant p-ch CV/I improvement over Si**
  - **CNT has >20X higher effective p-ch mobility than Si**
- **Si nanowires currently do not show improvement over Si**

# Energy-Delay Product for PMOS

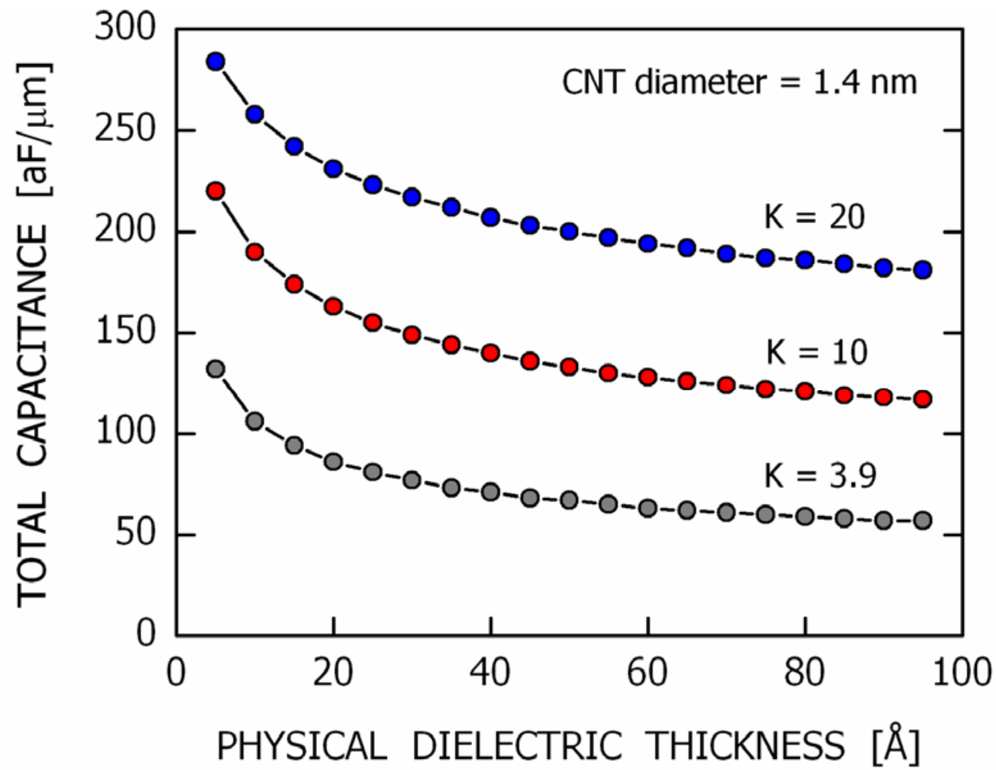


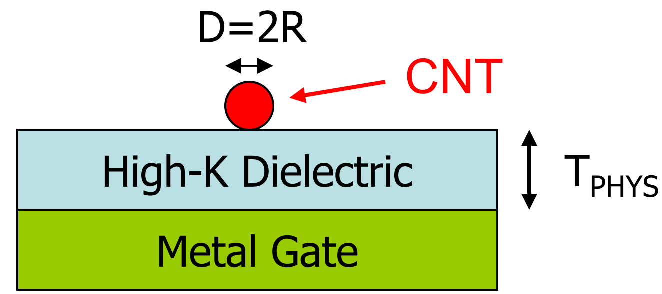
# Carbon Nanotube (CNT) p-FET with High-K/Metal-Gate




- **CNT FET exhibits low gate dielectric leakage with the use of high-K**
- **Ambipolar leakage identified as the major source of parasitic leakage in CNT (due to metal-CNT Schottky S/D contacts)**

# Capacitance of High-K/Metal-Gate on Carbon Nanotubes (CNT)




$$C_{TOTAL}^{-1} = C_{OX}^{-1} + C_{QM}^{-1}$$

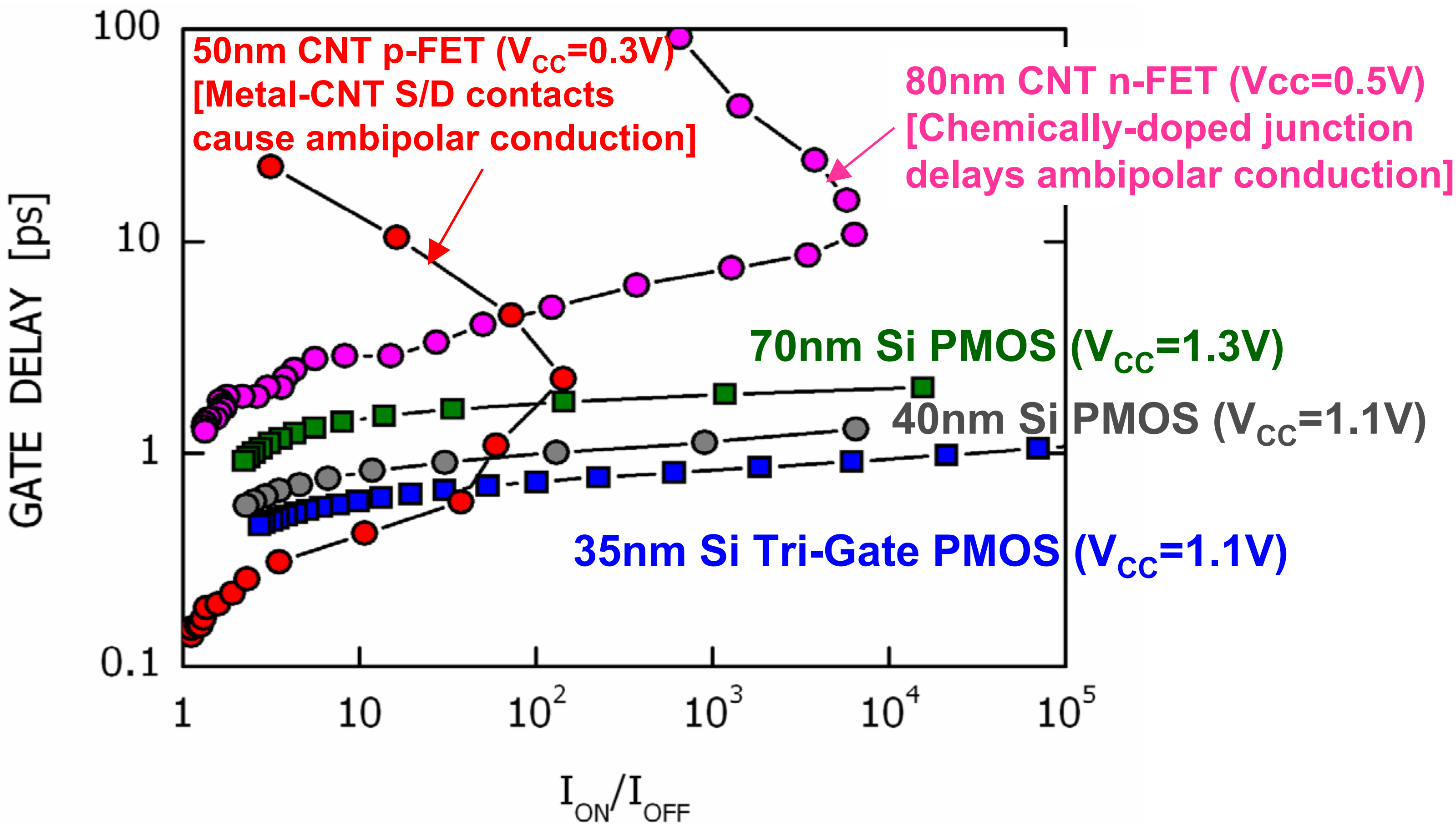
$$C_{OX} = \frac{2\pi\varepsilon_0 K}{\ln\left(2\frac{R + T_{PHYS}}{R}\right)}$$

$$C_{QM} \sim 400\ aF/\mu m\ *$$

* Guo et al, Applied Physics Letters 2002

- **High-K dielectric constant has a stronger effect than high-K dielectric thickness in increasing gate capacitance of carbon nanotube FETs**

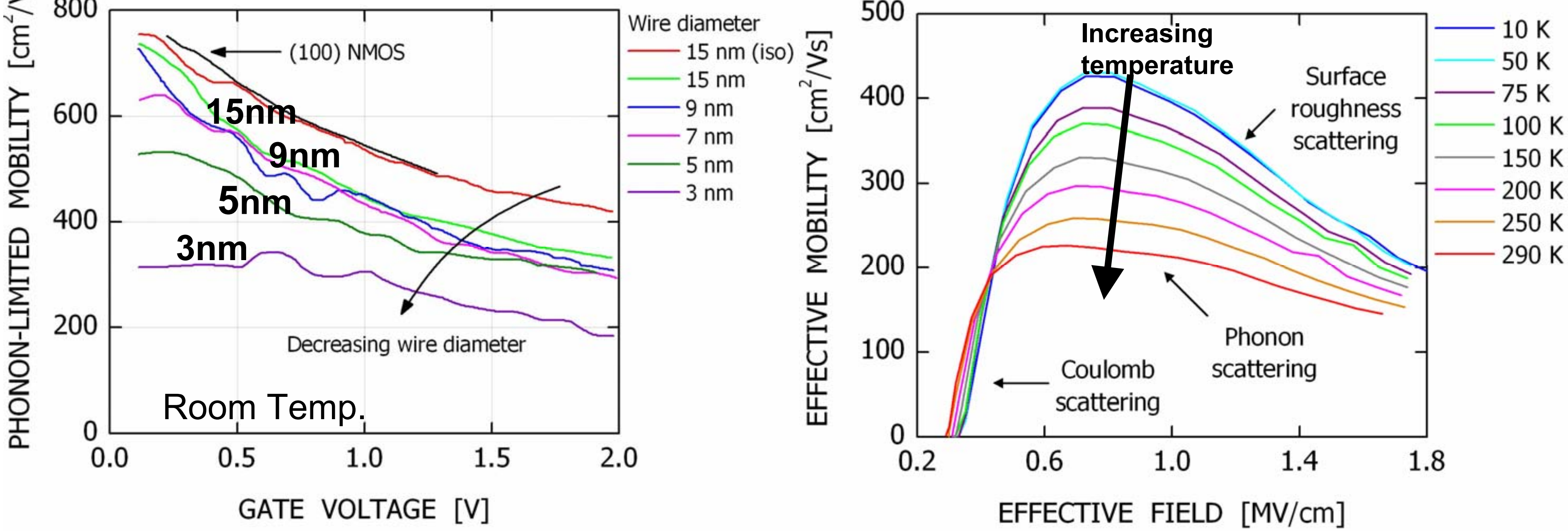
# CV/I versus $I_{ON}/I_{OFF}$ Ratio




- For $I_{ON}/I_{OFF}$ < 100, CNT p-FET shows improvement over Si due to higher channel mobility and lower $V_{CC}$ used
- Highest $I_{ON}/I_{OFF}$ ratio in CNT limited by ambipolar conduction due to metal-CNT S/D contacts; chemically-doped junctions delays ambipolar conduction despite poor CV/I performance

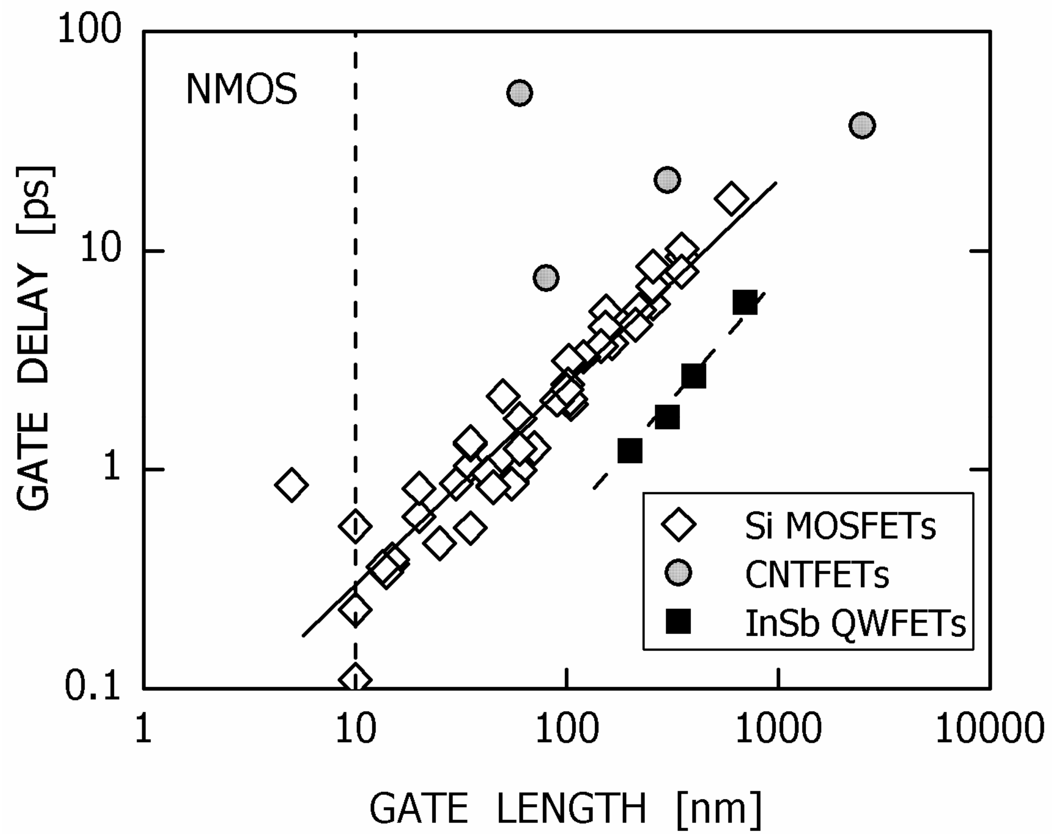
# Physics of Silicon Nanowires

**TCAD Simulation** (R. Kotlyar, Intel, APL 2004) **Measurements**



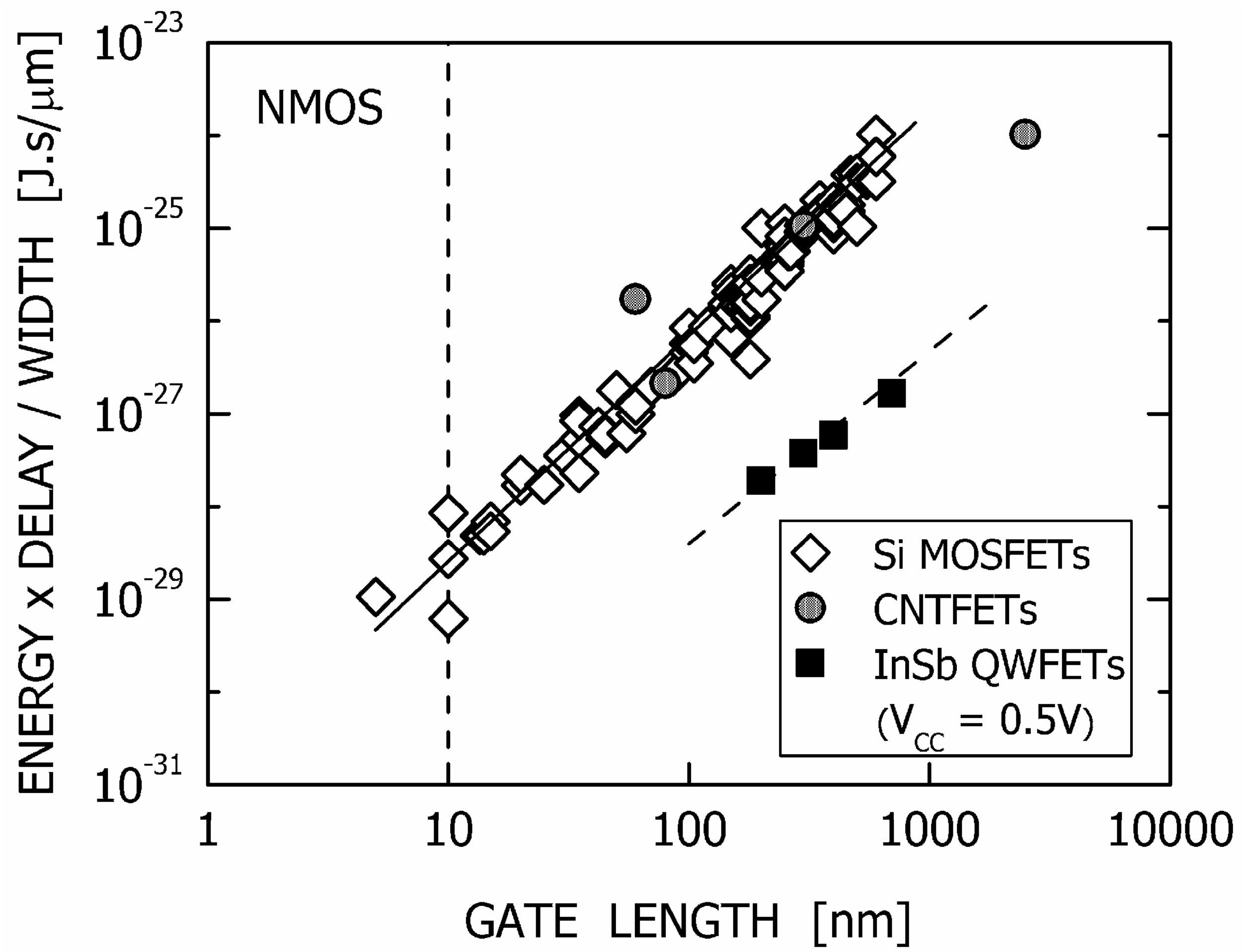

- **Previous understanding: Reducing wire diameter reduces available density of states for elastic scattering (1D), thus improving mobility**
- **Current understanding of Si nanowires**
  - **Impact of phonon scattering becomes significant above 50 K**
  - **Mobility at room temperature decreases with reducing diameter (< 10nm) due to phonon scattering**
  - **Performance of Si nanowires limited by phonon scattering at room temp**

# Intrinsic gate delay CV/I for NMOS

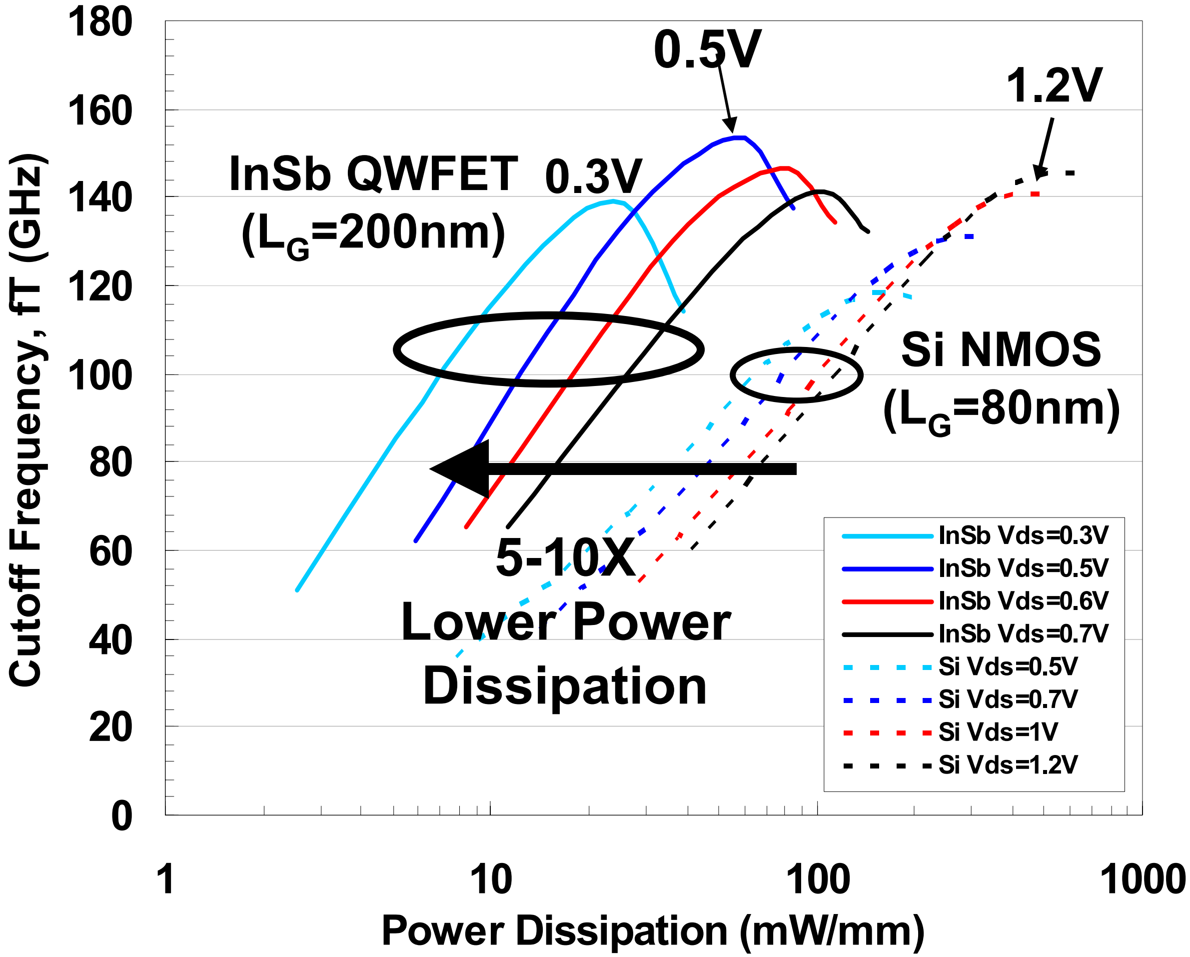


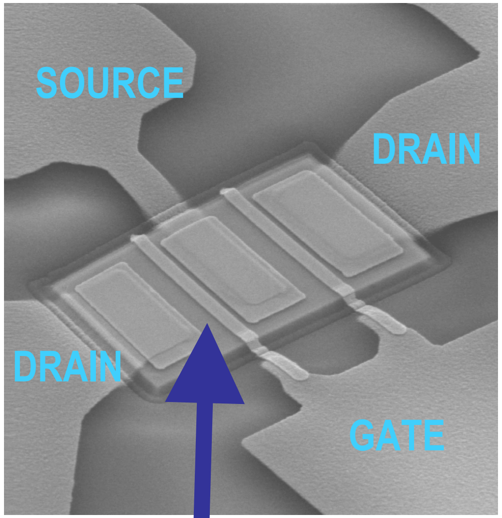

- n-channel CNT not as well established as p-channel CNT
- III-V (e.g. InSb) devices show significant CV/I improvement over Si
  - III-V devices have >50X higher effective n-ch mobility than Si
  - III-V devices operated at low $V_{CC}$ = 0.5V

# Energy-Delay Product for NMOS



# III-V Transistors for Low $V_{CC}$




**III-V (InSb) Q-W Transistor**

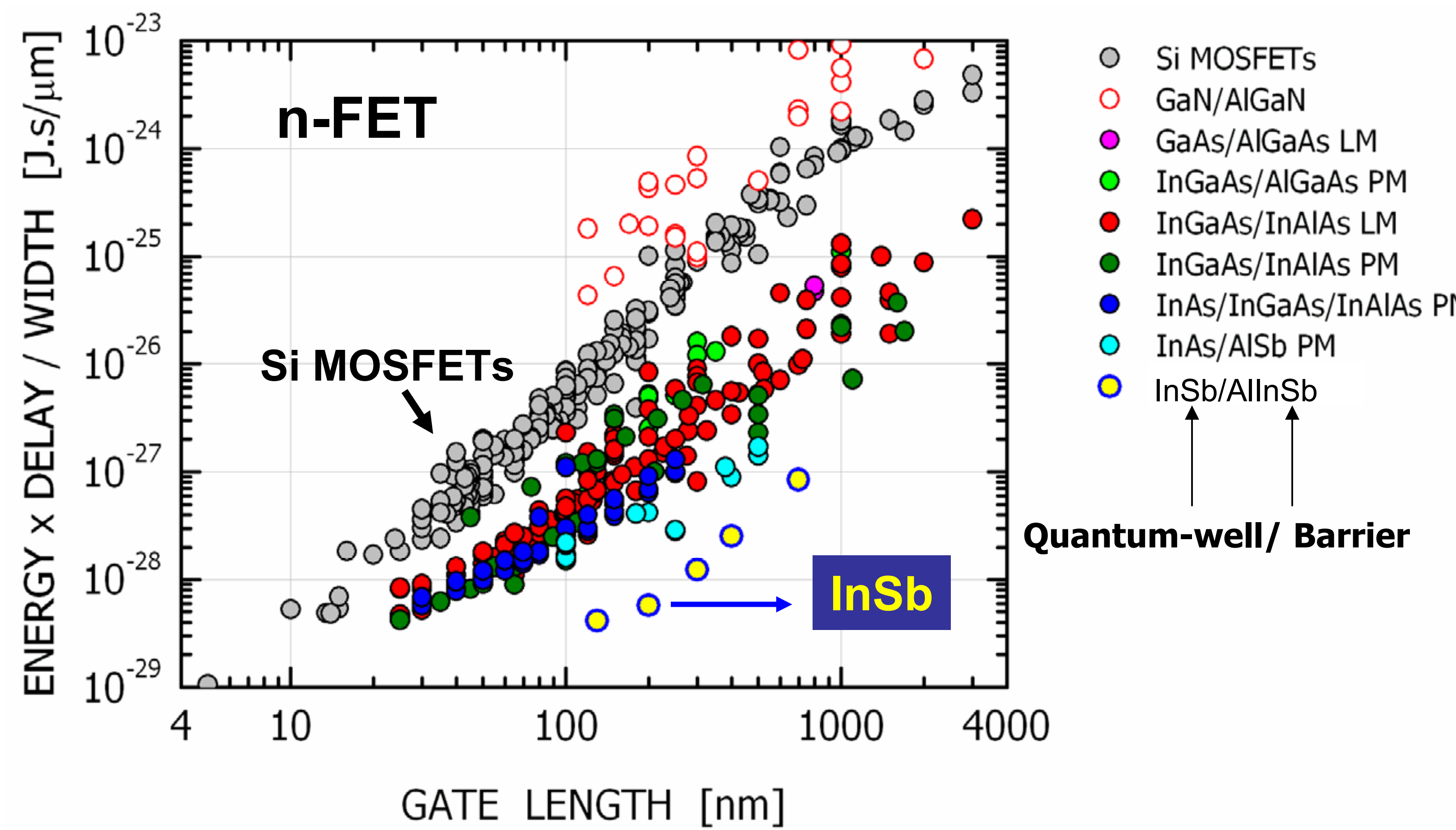
**(Schottky metal gate with no gate dielectric)**

$$\frac{CV}{I} = \frac{C_0 WLV}{I} = \frac{C_0 WL}{g_m} = \frac{L}{v_{eff}} = \frac{1}{2\pi f_T}$$



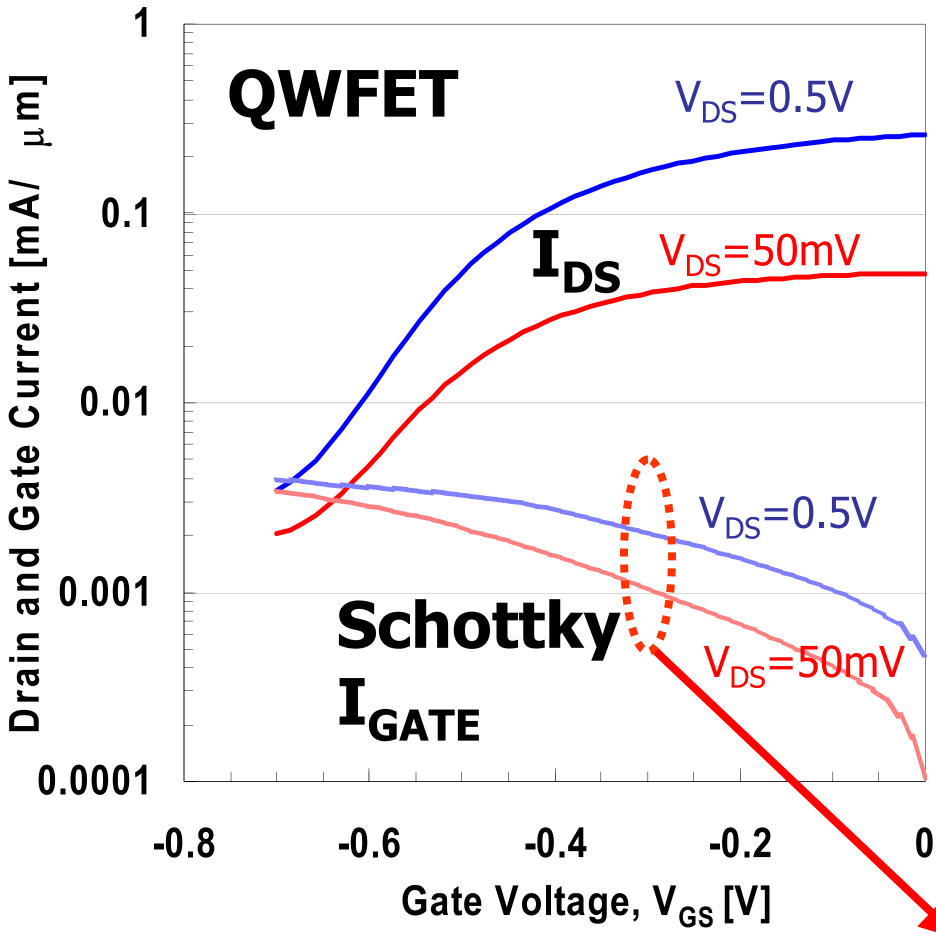
Source: Intel & QinetiQ, ICSICT, Oct 2004

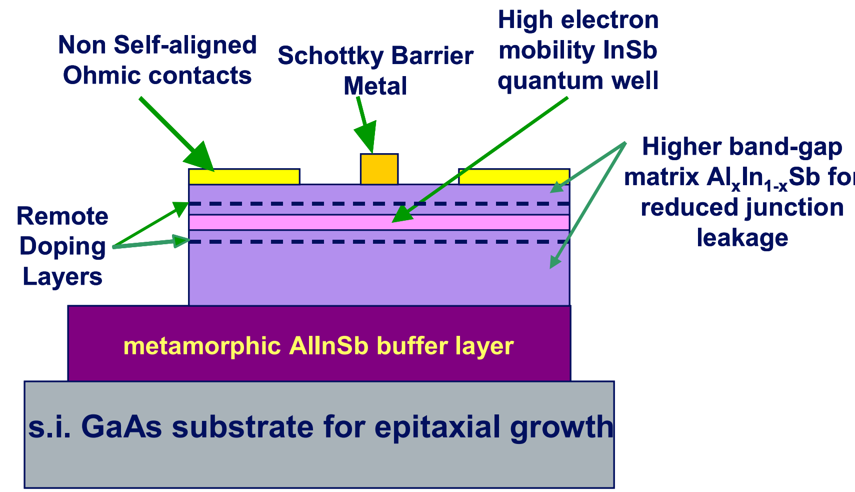
# III-V Nanoelectronics:
## Energy-Delay Product vs Device Gate Length




- **InSb QW-FETs have the lowest NMOS energy-delay product (highest mobility and lowest operating $V_{CC}$)**

# III-V Nanoelectronics:
## High-K Required to Eliminate Schottky $I_{GATE}$

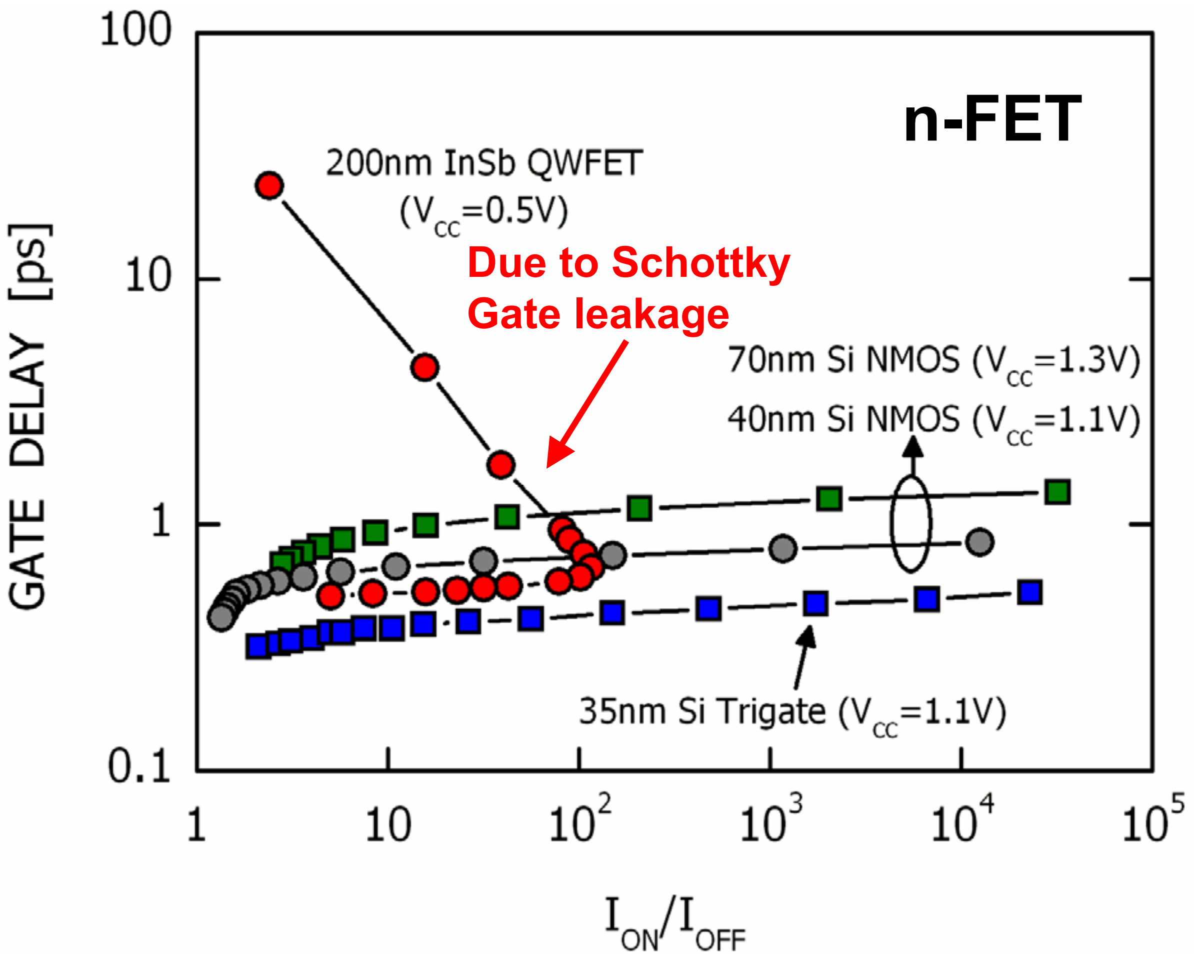



**Requires a gate stack to eliminate Schottky $I_{GATE}$, e.g. high-K/metal-gate**

Source: Intel & QinetiQ, ICSICT, Oct 2004

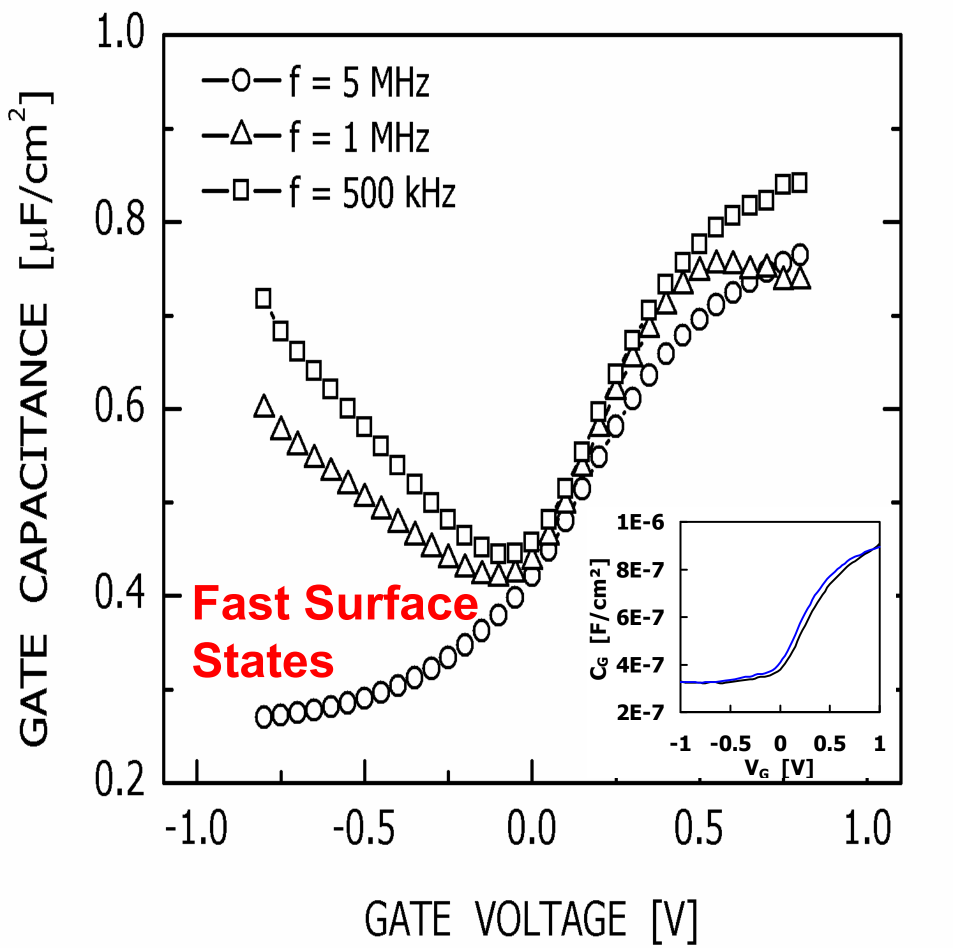
# III-V Nanoelectronics:
## High-K/Metal-Gate Required to Improve $I_{ON}/I_{OFF}$

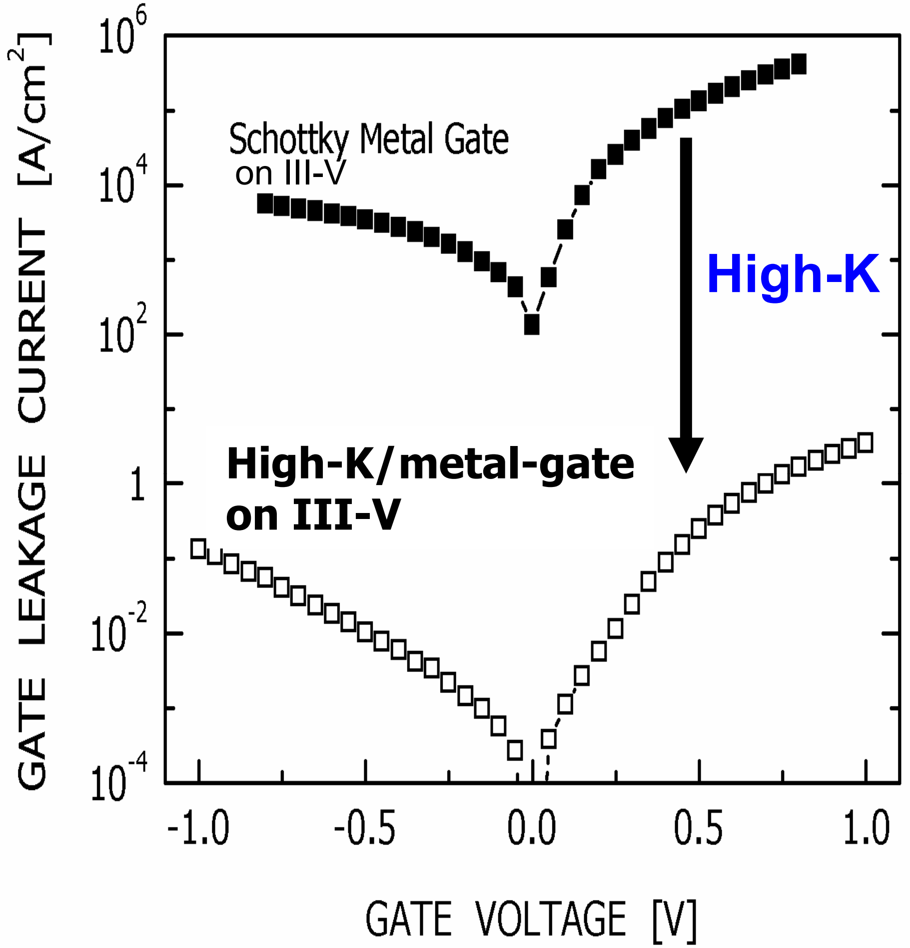



- $I_{ON}$ /$I_{OFF}$ ratio of InSb QWFET is limited by Schottky gate leakage

# One of the Grand Challenges in III-V Nanoelectronics for logic: Compatibility of III-V and High-K/Metal-gate Stack

**III-V/High-K/metal-gate**



# Summary

- High-K/metal-gate will be one of the key enablers for emerging non-Si nanoelectronic devices for future potential high-performance, low-power logic applications
- High-K/metal-gate stacks are required for improving the $I_{on}/I_{off}$ ratio of III-V quantum-well transistors for future potential low-power, high-speed logic applications