

# Advanced Metal Gate/High-K Dielectric Stacks for High-Performance CMOS Transistors

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## 1. Abstract

We have successfully engineered n-type and p-type metal electrodes with the correct work functions on high-K gate dielectrics for high-performance CMOS applications. The resulting metal gate/high-K dielectric stacks have i) equivalent oxide thickness (EOT) of 1.0nm with negligible gate oxide leakage, ii) desirable transistor threshold voltages for n- and p-channel MOSFETs, and iii) transistor channel mobilities close to those of SiO<sub>2</sub>. The CMOS transistors fabricated with these advanced metal gate/high-K dielectric stacks achieve the expected high drive current performance.

## 2. Introduction

For more than 15 years the physical thickness of SiO<sub>2</sub> has been aggressively scaled for low-power, high-performance CMOS applications. Figure 1 shows the physical thickness trend of SiO<sub>2</sub>. Recently SiO<sub>2</sub> with physical thickness of 1.2nm (see Fig. 2) has been successfully implemented in the 90nm logic node [1]. In addition, SiO<sub>2</sub> with physical thickness of 0.8nm (see Fig. 3) has been demonstrated in the laboratory [2-3]. Continual gate oxide scaling, however, will require the use of dielectric materials with higher dielectric constant (K) since i) the gate oxide leakage is increasing with decreasing SiO<sub>2</sub> thickness, and ii) SiO<sub>2</sub> is running out of atoms for further scaling. So far the most common high-K dielectric materials investigated by both academia and industry are Hf-based and Zr-based [4-5].

## 3. Challenges in Replacing SiO<sub>2</sub> with High-K Dielectrics

### 3a. PolySi/High-K Dielectric Stack

There are two typical problems in replacing polySi/SiO<sub>2</sub> with the polySi/high-K dielectric stack for high-performance CMOS applications. First, high-K dielectrics and polySi are incompatible due to the Fermi level pinning at the polySi/high-K interface [6], which causes high threshold voltages in MOSFET transistors. The Fermi level pinning is most likely caused by defect formation at the polySi/high-K dielectric interface, as illustrated in Fig. 4. Second, polySi/high-K transistors exhibit severely degraded channel mobility due to the coupling of low energy surface optical (SO) phonon modes arising from the polarization of the high-K dielectric to the inversion channel charge carriers [7-8].

### 3b. Metal-gate/High-K Dielectric Stack

Metal gate electrodes may be more effective than polySi in screening the high-K SO phonons from coupling to

the channel under inversion conditions, resulting in improved channel mobility [7-8]. However, the use of high-K/metal-gate require a n-type metal and a p-type metal with the right work functions on the high-K dielectric for high-performance CMOS logic applications on bulk Si [9]. So far, all the metal gate electrodes reported in literature have work functions that are mid-gap or close to mid-gap on high-K dielectrics (e.g. mid-gap TiN [8]), and the resulting CMOS transistors have high threshold voltages and hence poor drive performance.

## 4. New Metal Gate/High-K Dielectric Stacks to Achieve Record-setting Transistor Performance

We have successfully engineered n-type and p-type metal electrodes that have the correct work functions on the high-K for high-performance CMOS, as shown in Fig. 5. The resulting metal gate/high-K dielectric stacks have equivalent oxide thickness (EOT) of 1.0nm with negligible gate oxide leakage, and channel mobilities that are close to SiO<sub>2</sub> (Figs. 6-7). 80nm physical-gate-length CMOS transistors with the new metal gate/high-K dielectric stacks have been fabricated to produce the expected high performance (due to reduction in inversion thickness  $T_{ox(inv)}$  and increase in inversion charge) [10]. At  $V_d = 1.3V$ , the NMOS transistor achieves record-setting  $I_{on} = 1.66mA/\mu m$  with  $I_{off} = 37nA/\mu m$  (Figs 8-9), while the PMOS transistor achieves record-setting  $I_{on} = 0.69mA/\mu m$  with  $I_{off} = 25nA/\mu m$  (Figs 10-11).

## 5. Summary

We have successfully engineered advanced metal gate/high-K dielectric stacks with the correct work functions and channel mobilities close to SiO<sub>2</sub>. The resulting CMOS transistors with the new gate stacks achieve record-setting drive current performance, as expected, with negligible gate oxide leakage.

## 6. References

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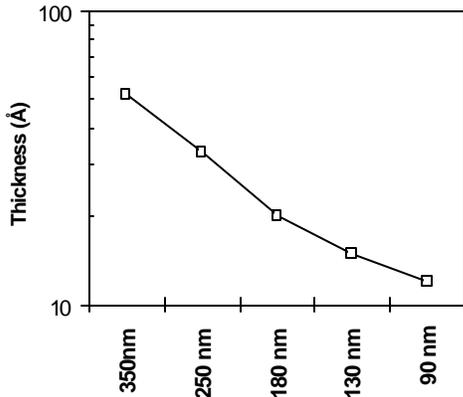


Fig. 1 Physical thickness scaling trend of SiO<sub>2</sub> gate oxide for the various logic technology nodes.

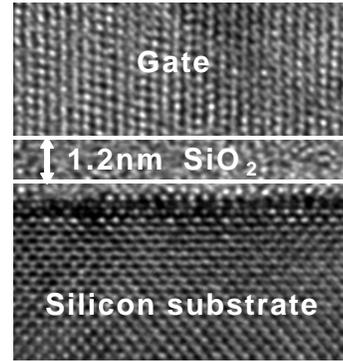


Fig. 2 TEM cross section of SiO<sub>2</sub> gate oxide with physical thickness of 1.2nm implemented in the 90nm logic technology node.

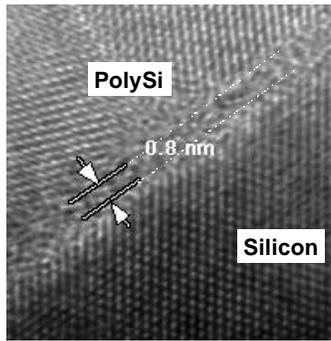


Fig. 3 TEM cross section of SiO<sub>2</sub> gate oxide with physical thickness of 0.8nm produced in the laboratory.

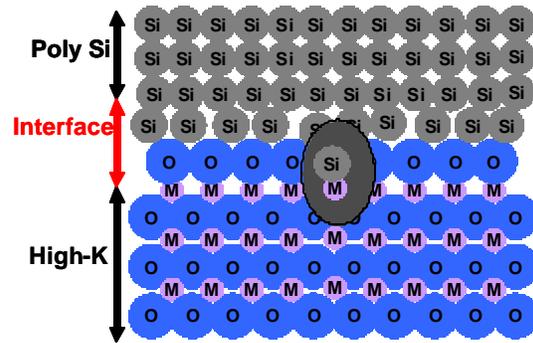


Fig. 4 Defect formation at the polySi and high-K dielectric interface is most likely the cause of the Fermi level pinning which causes high threshold voltages in MOSFET (M = Zr or Hf).

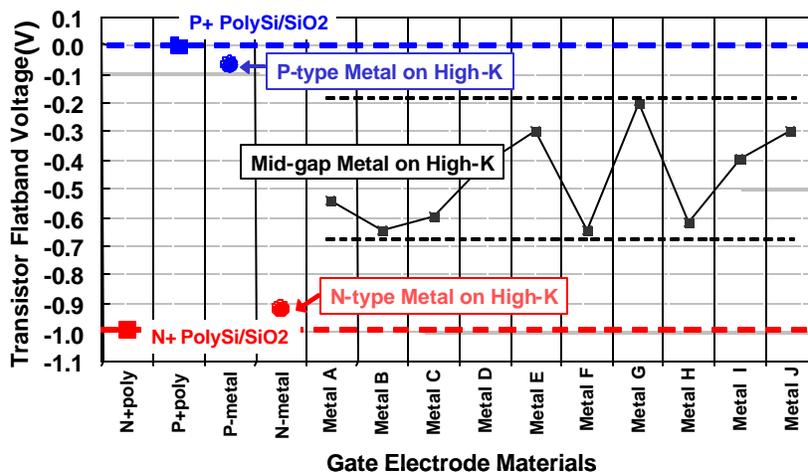


Fig. 5 N-type and p-type metal gate electrodes with the correct work functions on the high-K dielectrics have been engineered for both the NMOS and PMOS transistors for high-performance CMOS applications. Mid-gap metals produce poor transistor performance.

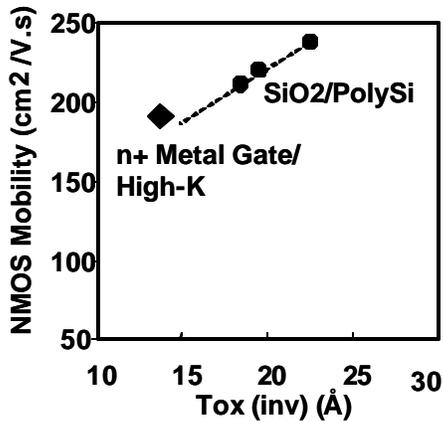


Fig. 6. Channel mobility of the NMOS transistors measured at transverse electric field ( $E_{eff}$ ) of 1.0MV/cm. The x-axis is the electrical gate oxide thickness at inversion ( $Tox(inv)$ ). The n-type metal gate/high-K dielectric stack has  $EOT = 1.0nm$  and  $Tox(inv) = 1.45nm$ .

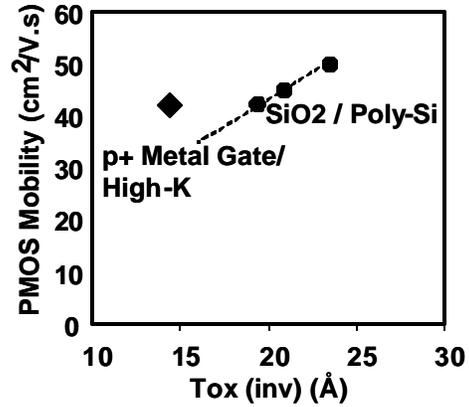


Fig.7 Channel mobility of the PMOS transistors measured at transverse electric field ( $E_{eff}$ ) of 1.0MV/cm. The x-axis is the electrical gate oxide thickness at inversion ( $Tox(inv)$ ). The p-type metal gate/high-K dielectric stack has  $EOT = 1.0nm$  and  $Tox(inv) = 1.45nm$ .

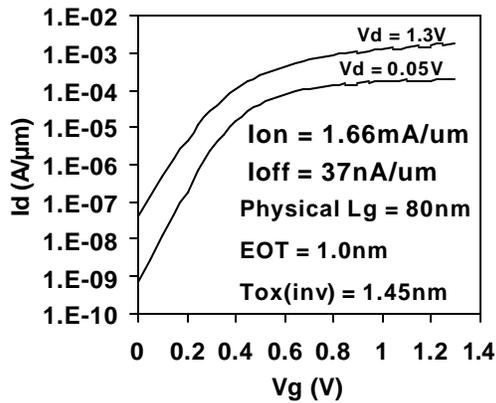


Fig. 8  $I_d$ - $V_g$  characteristics of the metal gate/high-K NMOS transistor with 80nm physical gate length, showing a record-setting drive current of 1.66mA/um at a low off-state leakage of 37nA/um at  $V_d = 1.3V$ . The gate stack has  $EOT = 1.0nm$  and electrical inversion  $Tox(inv) = 1.45nm$ .

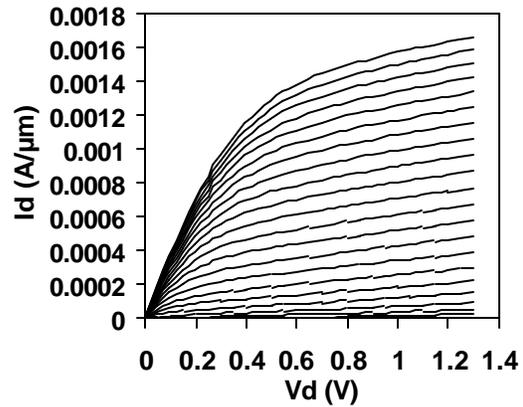


Fig. 9  $I_d$ - $V_d$  family characteristics of the metal gate/high-K NMOS transistor with 80nm physical gate length. The gate stack has  $EOT = 1.0nm$  and electrical inversion  $Tox(inv) = 1.45nm$ .  $|V_g| = 0$  to 1.3V.

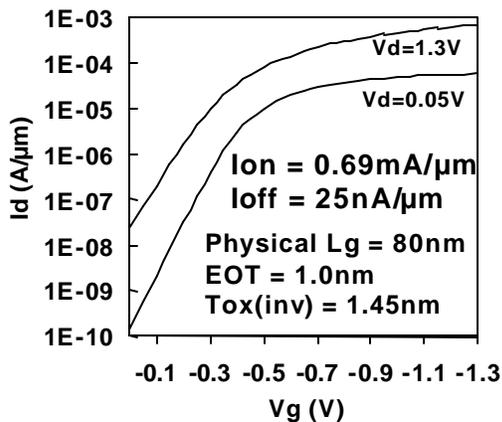


Fig. 10  $I_d$ - $V_g$  characteristics of the metal gate/high-K PMOS transistor with 80nm physical gate length, showing a record-setting drive current of 0.69mA/um at a low off-state leakage of 25nA/um at  $V_d = 1.3V$ . The gate stack has  $EOT = 1.0nm$  and electrical inversion  $Tox(inv) = 1.45nm$ .

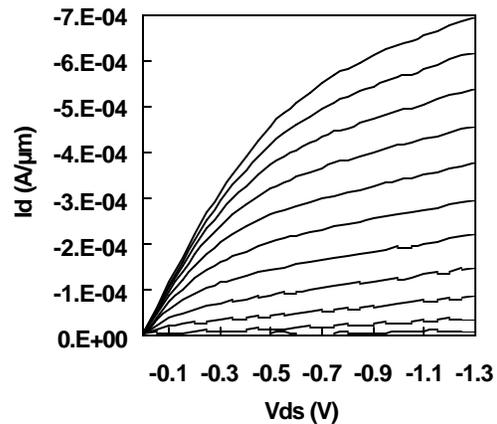


Fig. 11  $I_d$ - $V_{ds}$  family characteristics of the metal gate/high-K PMOS transistor with 80nm physical gate length. The gate stack has  $EOT = 1.0nm$  and electrical inversion  $Tox(inv) = 1.45nm$ .  $|V_g| = 0$  to 1.3V.