High Mobility Strained Germanium Quantum Well Field Effect Transistor as the P-Channel Device Option for Low Power (Vcc = 0.5 V) III-V CMOS Architecture

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Abstract

In this article we demonstrate a Ge p-channel QWFET with scaled TOXE = 14.5Å and mobility of 770 $cm^2/V*s$ at n_s =5x10^{12} cm^{-2} (charge density in the state-of-the-art Si transistor channel at Vcc = 0.5V). For thin TOXE < 40 Å, this represents the highest hole mobility reported for any Ge device and is 4x higher than state-of-the-art strained silicon. The QWFET architecture achieves high mobility by incorporating biaxial strain and eliminating dopant impurity scattering. The thin TOXE was achieved using a Si cap and a low Dt transistor process, which has a low oxide interface Dit. Parallel conduction in the SiGe buffer was suppressed using a phosphorus junction layer, allowing healthy subthreshold slope in Ge QWFET for the first time. The Ge QWFET achieves an intrinsic Gmsat which is 2x higher than the InSb p-channel QWFET. These results suggest the Ge QWFET is a viable p-channel option for non-silicon CMOS.

Introduction

Recently, III-V quantum well field effect transistor (QWFET) research for future low power CMOS logic applications has made significant progress [1,3]. While n-channel III-V studies have shown significant drive current gains over state of the art silicon at low Vcc [1], the corresponding p-channel transistor with thin TOXE and high mobility (μ) has not yet been demonstrated. In this study, we demonstrate a high mobility strained germanium (Ge) p-channel QWFET suitable for low power CMOS architecture with scaled TOXE = 14.5Å and hole mobility = 770 $cm^2/V*s$ at n_s =5x10^{12} cm^{-2}. For TOXE < 40 Å, this represents the highest hole mobility reported for any Ge device and is 4x higher than state-of-the-art strained silicon. These results suggest that the Ge QWFET is a viable p-channel option for III-V CMOS realization.

Materials Growth and Device Fabrication

Figure 1 shows a schematic of a biaxially strained undoped Ge QW structure. The boron modulation doping layer allows for Hall measurement, but is optional for implanted S/D transistors. The phosphorus doped layer is grown to suppress parallel conduction in the SiGe buffers. A cross sectional TEM image of a Ge QW grown by RTCVD on 300mm silicon is shown in Fig 2, highlighting both the 2-step SiGe buffer layers and biaxially strained Ge QW layer bounded by $Si_{.3}Ge_{.7}$ barriers. Although not shown, we also grew relaxed Ge layers on this two layer buffer to provide us with a Ge MOSFET reference structure. Figure 3 shows X-ray diffraction spectra of the symmetric (004) reflection for both the Ge QW and relaxed Ge structures indicating 1.3% biaxial strain in the Ge QW. The Hall mobility for RTCVD grown Ge QW structures, plotted in Fig 4, matches MBE grown Ge QW literature data [5-7] and shows gain over the InSb QW[3] and strained Si [2]. Figure 5 shows a TEM of a fully processed Ge QWFET utilizing shallow trench isolation (not shown), HfO_2/TiN high-k metal gate, self-aligned B-implanted S/D, W/Ti contacts, a strained Ge QW channel, and a phosphorus isolation layer. A TEM image of a Ge QWFET with an *in-situ* doped Si_xGe_{1-x} raised source/drain (RSD) is shown in Fig 6.

Silicon Cap and Gate Dielectric Interface

A thin Si cap layer is required to prevent carrier spill-out from the Ge QW. This is demonstrated in Fig 7 where k*p-Poisson simulations show that for a hole density (n_s) = 5x10^{12} cm^{-2}, a 10Å Si cap layer confines carriers in the Ge QW, whereas significant carrier spill-out occurs with a 100Å $Si_{.3}Ge_{.7}$ barrier. Figure 8 shows a TEM image of a high-k metal gate stack with a thin silicon cap on a Ge QW. Part of the silicon cap is oxidized due to thermal cycle (Dt) during the transistor fabrication process. This is suggested by the EDS depth profile of the gate stack, shown in Fig 9, indicating the presence of both Si and SiO_2 between the Ge and HfO_2. CV data in Fig 10 indicates inversion TOXE reduction with Si cap thickness scaling. Due to asymmetry of the valence and conduction band offsets between Si and Ge, the Si cap only contributes to C_{inv}. Hence, the SiO_2 thickness (T_{SiO2}) on the Si cap can be extracted from the accumulation TOXE, and in this example is 6Å for all cases due to constant thermal Dt. Since a body contact is needed to measure the accumulation CV, this data was collected from the Ge MOSFET reference device. The corresponding μ vs n_s plotted in Fig 11 shows that μ improves as Si cap thickness is reduced due to reduction in carrier spill-out. However, μ is degraded significantly without Si cap due to an increase in interface trap density (Dit). Figure 12 shows that by lowering process Dt from 700°C to 635°C TOXE can scale to 14.5Å without loss of mobility via T_{SiO2} reduction on the Si cap.

Ge QWFET Device Analysis

The minimal CV frequency dispersion in Fig 13 indicates a good quality interface for both the relaxed Ge MOSFET reference and strained Ge QWFET with the same 14.5Å TOXE process. Figure 14 shows mobility vs n_s for both devices. The experiments agree with k*p simulations, which assume Dit and surface roughness matched to state-of-the-art Si. This indicates a high quality oxide interface on Ge. At n_s = 5x10^{12} cm^{-2}, the QWFET exhibits 4x mobility gain over state-of-the-art strained Si [2]. Furthermore, in Fig 15 the Ge QWFET achieves the highest mobility (770 $cm^2/V*s$) at the thinnest TOXE (14.5Å) compared to the best Ge devices in literature [8-9]. Figs 16 and 17 plot the temperature (T) dependence of the Ge QWFET mobility, which shows no saturation of μ down to T=20K. This indicates minimal impact from Coulomb scattering due to absence of doping in the QW and low Dit.

Figure 18 shows drain current vs gate bias (Vg) at Vds = -0.5V for a Ge QWFET, with Lgate = 100 nm. The device achieves healthy subthreshold slope (SS) of 97 mV/DEC for the first time in a Ge QW structure, due to the suppression of parallel conduction through the SiGe buffer using the phosphorus isolation layer. Figure 19 plots the SS vs gate length dependence for the Ge QWFET and shows removal of modulation doping (MD) improves SCE. The raised source/drain process further improves SCE by allowing for reduction or elimination of implantation. Figure 20 plots peak intrinsic Gmsat vs SS, showing the intrinsic Gmsat of the Ge QWFET with RSD process is 2x higher than that of the InSb p-channel QWFET [3]. The RSD process exhibits a 35% improvement in intrinsic Gm due to higher short channel strain compared to the implant only flow. Figure 21 compares Ion vs Ioff characteristics of the Ge QWFET with RSD(this work) to the best reported III-V [3] and germanium devices [10] at Vcc = 0.5V. These Ge QWFETs exhibit 2x higher drive current for the same Ioff.

Conclusion

A Ge p-channel QWFET with scaled TOXE = 14.5Å and mobility of 770 $cm^2/V*s$ at n_s =$5x10^{12}$ cm^{-2} (Vcc=0.5V) has been achieved. For TOXE < 40 Å, this represents the highest hole mobility reported for any Ge device and is 4x higher than state-of-the-art strained silicon. The QWFET architecture achieves high mobility by incorporating biaxial strain and eliminating dopant impurity scattering. The thin TOXE was achieved using a Si cap and a low Dt transistor process, which has a low oxide interface Dit. Parallel conduction in the SiGe buffer was suppressed using a phosphorus junction layer, allowing healthy subthreshold slope in Ge QWFET for the first time. The Ge QWFET achieves an intrinsic Gmsat which is 2x higher than the InSb p-channel QWFET. Furthermore, at Vcc = 0.5V, the Ge QWFET exhibits 2x higher drive current at fixed Ioff than the best III-V [3] and germanium devices [10] reported to date.

References

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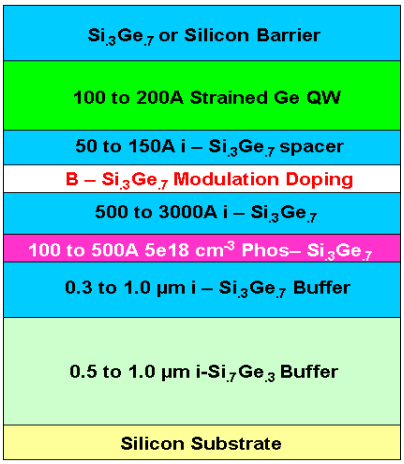

Fig 1: Schematic of biaxially strained undoped Ge QW structure on a silicon substrate. Front-side or backside B-modulation doping allows for Hall measurement, but is optional for implanted S/D transistors. Phosphorus layer is used to suppress parallel conduction in the SiGe buffers.

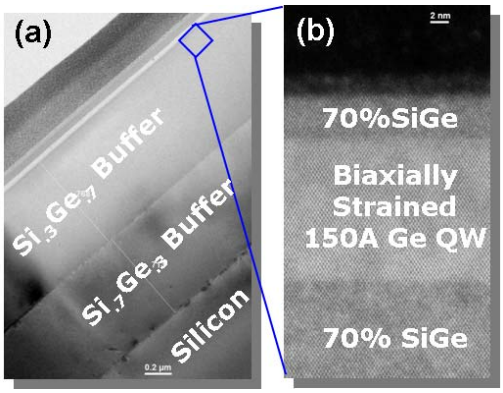

Fig 2: Cross sectional TEM image of a Ge QW structure, which was grown by RTCVD on 300mm silicon, showing (a) 2-step SiGe buffer layers and (b) Biaxially strained Ge QW layer bounded by $Si_{.3}Ge_{.7}$ barriers.

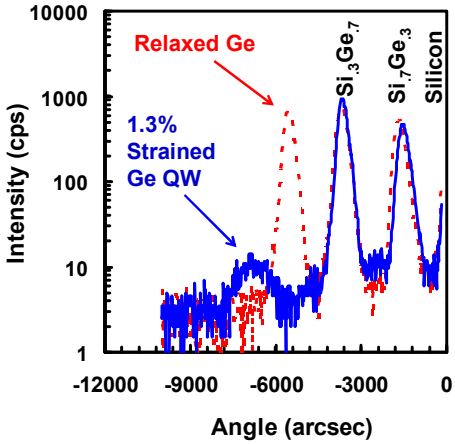

Fig 3: High resolution X-ray diffraction spectra of the symmetric (004) reflection for both strained Ge QW (solid) and relaxed Ge (dash) structures on silicon substrate, indicating 1.3% biaxial strain in the Ge QW.

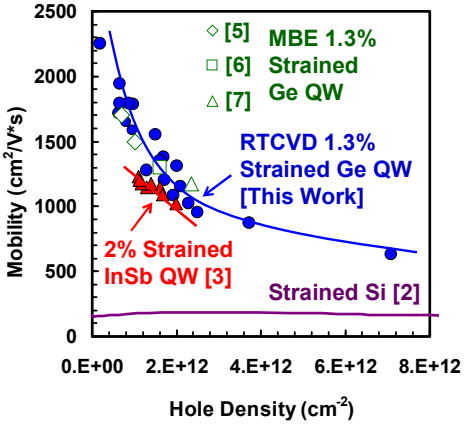

Fig 4: Hall mobility vs density for 300mm RTCVD grown 1.3% strained Ge QW structures, which exhibit mobility matched to MBE grown Ge QW literature data[5-7], and mobility gains over the InSb QW[3] and strained silicon[2].

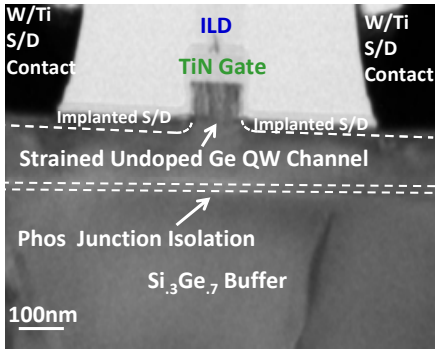

Fig 5: Cross sectional TEM image of a fully processed Ge QWFET device highlighting the strained Ge QW channel, TiN gate electrode, self aligned implanted S/D, W/Ti S/D contacts, and the phosphorus isolation layer that suppresses parallel conduction in the SiGe buffer.

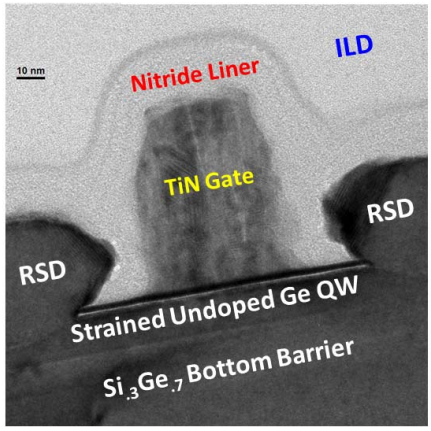

Fig 6: Cross sectional TEM image highlighting the gate stack and source/drain of a Ge QWFET incorporating a *in-situ* B doped Si-$_x$Ge$_{1-x}$ raised source/drain (RSD) which allows for reduction/removal of the S/D implantation.

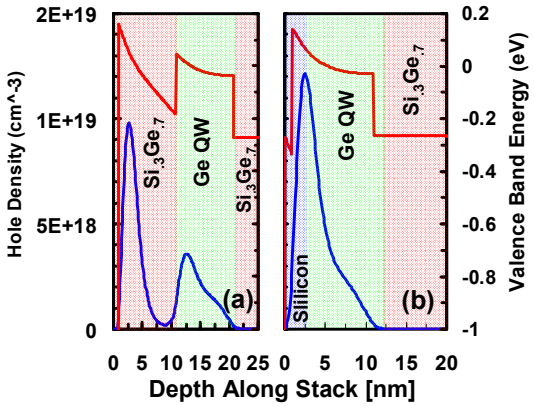

Fig 7: Valence band diagram and hole wavefunction determined using k*p Poisson technique for Ge QWFET for (a) 100A $Si_{.3}Ge_{.7}$ top barrier and (b) 10A Si Cap. In both cases, n_s=5x10^{12} cm^{-2} (Vcc=0.5V). The thin Si cap confines carriers in the QW layer.

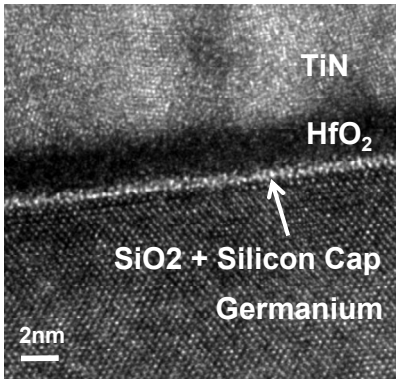

Fig8: High resolution cross sectional TEM image of a high-k metal gate stack with a thin Si cap on a Ge QWFET. Part of the Si cap is oxidized due to thermal Dt during the transistor fabrication process.

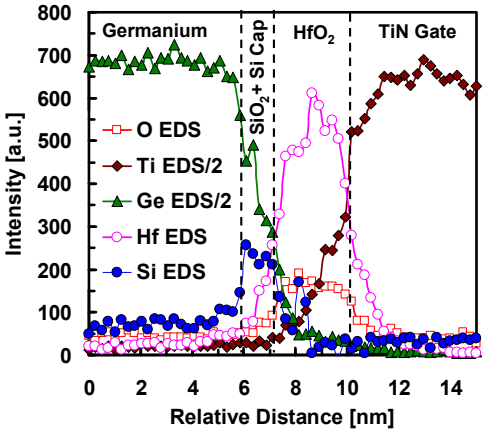

Fig 9: Energy dispersive X-ray spectroscopy depth profile of the high-k metal gate stack on Ge shown in Fig 7, indicating the presence of both Si and SiO2 between the Ge and HfO2. This confirms that part of the Si cap is oxidized due to thermal Dt during the transistor process. Further quantification was performed using electrical measurements as shown in Figs. 9-11.

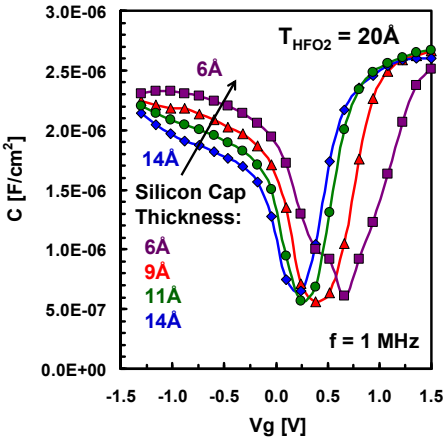

Fig 10: Full CV characteristics of Ge MOSFET reference showing inversion TOXE reduction with Si cap thickness scaling. Since the Si cap only contributes to inversion capacitance, the SiO2 thickness (T_{SiO2}) on the silicon cap can be extracted from the accumulation capacitance. In this example, T_{SiO2} = 6A for all cases due to constant thermal process Dt.

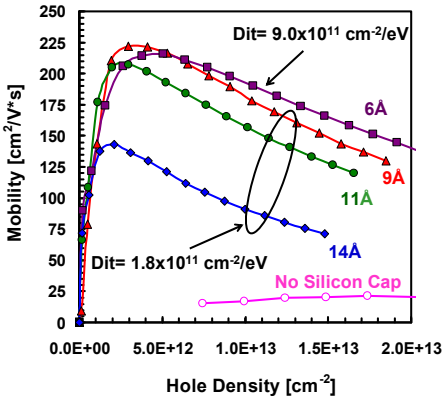

Fig11: Mobility vs carrier density for Ge MOSFET reference with different Si cap thickness. Mobility improves with reducing Si cap thickness due to reduction in carrier spill-out. Mobility degrades severely without Si cap due to high Dit.

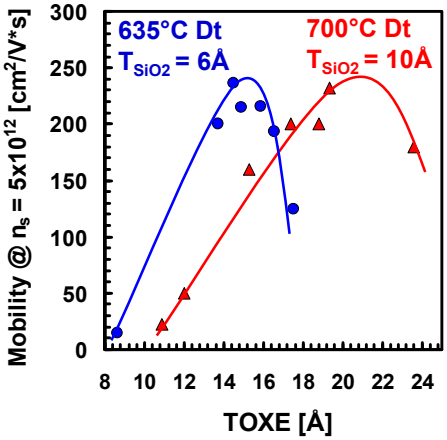

Fig 12: Ge MOSFET carrier mobility at n_s = 5x10^{12} cm^{-2} vs TOXE for 635°C (circle) and 700°C (triangle) process Dt. In both cases TOXE is scaled via Si cap thickness reduction. Lower Dt enables TOXE scaling down to 14.5Å without mobility loss, via reduction in T_{SiO2}.

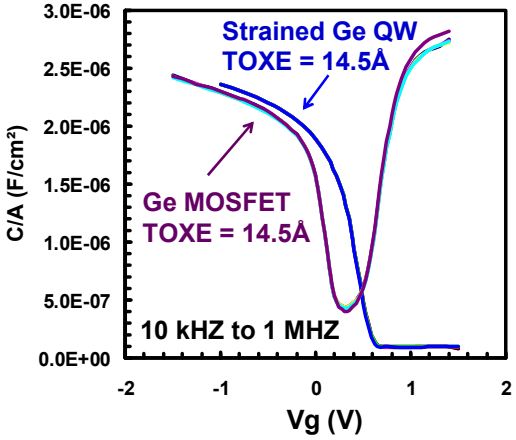

Fig13: Capacitance vs gate voltage at f = 1, 0.3, 0.1, 0.03, and 0.01 MHz for both the Ge MOSFET reference device and strained Ge QWFET using the same Si cap + high-k process. Both devices exhibit minimal CV dispersion at TOXE = 14.5Å.

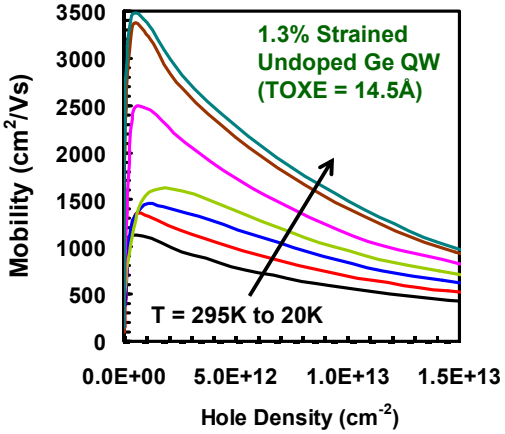

Fig 16: Mobility vs hole carrier density in a strained Ge QW FET for temperatures ranging (from bottom) 295K, 250K, 200K, 150K, 100K, 50K, and 20K. The mobility improves ~ 3x when cooled to T = 20 K.

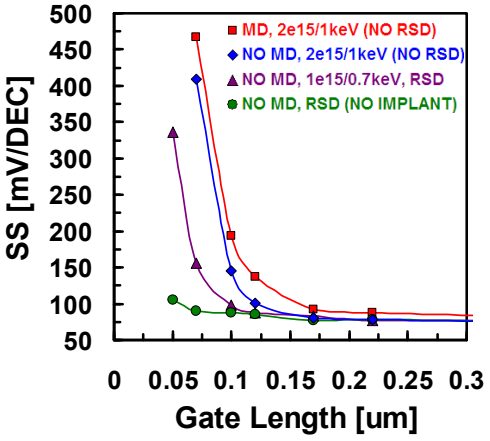

Fig 19: SS vs gate length dependence for the Ge QWFET shows removal of modulation doping (MD) improves SCE (diamond). The raised source/drain process further improves SCE by allowing for reduction (triangle) or elimination (circle) of implantation.

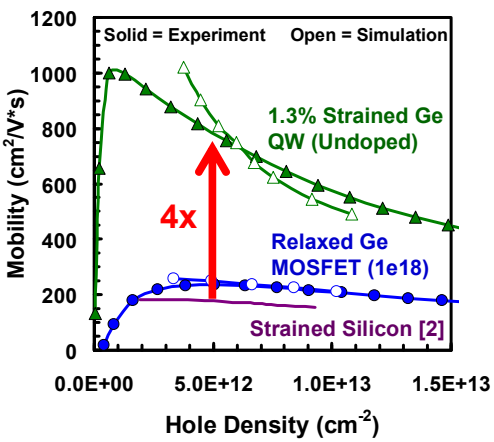

Fig14: Mobility vs n_s for the strained Ge QWFET and relaxed Ge MOSFET reference, with TOXE = 14.5Å. The experimental data match 6-band k*p simulations assuming Dit and surface roughness matched to state-of-the-art Si. At $n_s = 5x10^{12}$ cm^{-2}, the QWFET exhibits 4x gain over state-of-the-art strained Si [2]

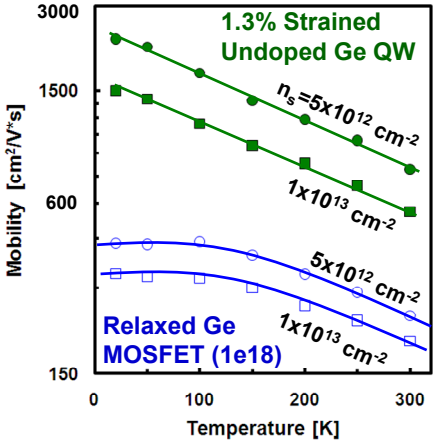

Fig17: Mobility vs T for the undoped Ge QWFET and for the relaxed doped Ge MOSFET. The data from the QWFET system indicates no saturation of mobility down to T=20 K, indicating minimal impact from Coulomb scattering due to absence of doping in the QW and low Dit.

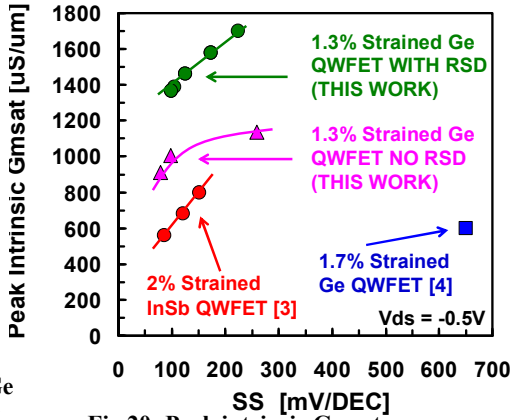

Fig 20: Peak intrinsic Gmsat vs subthreshold slope at Vds = -0.5V for the strained Ge QWFET with and without RSD. Included in the plot are the state-of-the-art InSb p-QWFET [3] and Ge QWFET [4] in the literature.

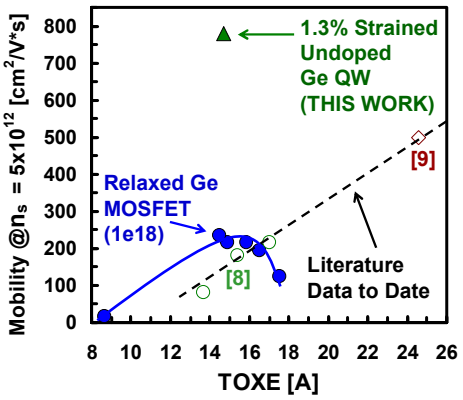

Fig15: Mobility vs TOXE at $n_s = 5x10^{12}$ cm^{-2} for the Ge MOSFET reference and the Ge QWFET. The Ge QWFET achieves the highest mobility (770 cm^2/V*s) at the thinnest TOXE (14.5Å) compared to the best relaxed [8] and strained [9] Ge literature data to date.

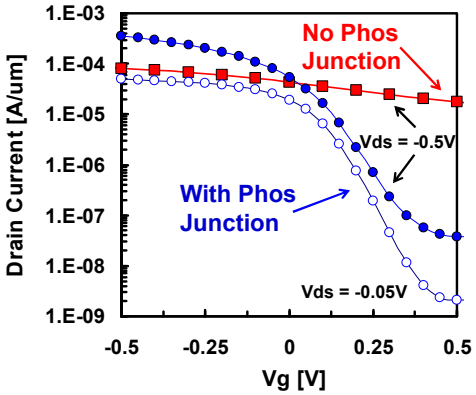

Fig18: Drain current vs Vg for a Ge QWFET with Lgate = 100nm, at Vds = -0.05V (open circle) and -0.5V (solid circle). The device exhibits a healthy subthreshold slope (SS) = 97 mV/DEC enabled by the phosphorus junction layer, which suppresses parallel conduction through the SiGe buffer.

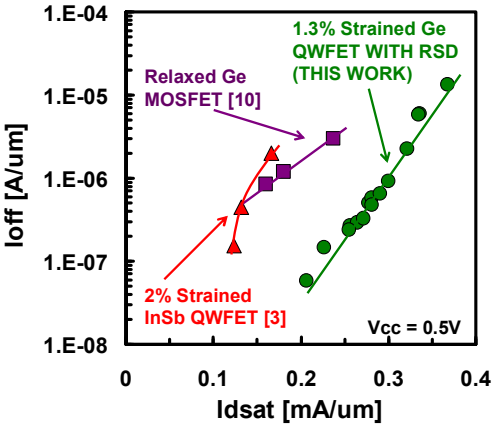

Fig 21: Ion vs Ioff for the strained Ge QWFET with RSD for Vcc = 0.5V. Included in the plot are the best InSb p-QWFET [3] and short channel Ge MOSFET data in the literature [10].
$VG_{OFF} = Vt + .125$ V
$VG_{ON} = Vt - .375$ V